Dissertation

submitted to the

Combined Faculties for the Natural Sciences and for Mathematics

of the Ruperto–Carola University of Heidelberg, Germany

for the degree of

Doctor of Natural Sciences

presented by

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Oral examination: 15.11.2006

Development, Fabrication and Characterisation of Atom Chips

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Zusammenfassung

Entwicklung, Herstellung und Charakterisierung von Atom Chips

Atom Chips sind die Grundlage für viele quantenoptische Experimente, da sie die Erzeugung von sehr genau definierten magnetischen Fallen für neutrale Atome mit minimalen Feldmodulationen ermöglichen. Die präzise Manipulation der Atome wird durch auf dem Atom Chip erzeugte magnetische sowie elektrische Felder ermöglicht. Dafür wurden im Rahmen dieser Arbeit Atom Chips mit einer sehr hohen Oberflächenqualität und präzise definierten Drähten von $< 20\,\mathrm{nm}$ Rauhigkeit hergestellt. Desweiteren wurden neue Generationen von Atom Chips mit sich kontaktfrei kreuzenden Drähten, Atom Chips mit Drahtabmessungen im Bereich von 100 nm sowie Atom Chips aus halbleitenden Materialien enwickelt.

Umfangreiche Messungen zur Charakterisierung der aufgedampften Drähte haben ergeben, dass diese Stromdichten bis zu $> 10^7\,\mathrm{A/cm^2}$ unbeschadet über Sekunden leiten und Spannungsunterschieden von über 500 V zwischen $10\,\mu\mathrm{m}$ widerstehen. Dabei stellte sich dotiertes Silizium mit einer dünnen Siliziumdioxid Schicht als das für Atom Chips geeignetste Substrat heraus.

Mit den in dieser Arbeit hergestellten Atom Chips konnten viele Experimente erfolgreich durchgeführt werden. Darüber hinaus hat diese Arbeit die Grundlage für viele weitere Experimente auf dem Gebiet der Atomphysik und der Quantenoptik geschaffen. Detailierte Anleitungen zum Bau aller entwickelten Atom Chips und Erklärungen der zugehoerigen Experimente werden dargestellt.

Abstract

Development, Fabrication and Characterisation of Atom Chips

Atom chips are robust and extremely powerful toolboxes for quantum optical experiments, since they make it possible to create exceedingly precise magnetic traps for neutral atoms with minimal field modulations. Accurate manipulation of trapped atoms is feasible with magnetic and electric fields created on the atom chip. Therefore atom chips with high quality surfaces and extremely well defined wires were build (roughness $< 20\,\mathrm{nm}$). Furthermore new generations of atom chips were developed, like the multi–layer atom chip with contact–free wire crossings, the sub–micron structured atom chip and the semiconducting atom chip.

Extensive characterisation measurements of atom chip wires demonstrated that the wires stand current densities of up to $10^7\,\mathrm{A/cm^2}$ for seconds and voltage differences of more than 500 V over $10\,\mu\mathrm{m}$. From the different materials tested doped silicon with a thin silicon dioxide layer is the best qualified substrate for atom chip fabrication.

The atom chips fabricated during this thesis have been used in many successful experiments, yielding numerous results. Moreover this thesis established the basics for many further experiments in atom physics and quantum optics and delivers complete instructions for the fabrication of all developed atom chips as well as an introduction to the experiments.

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List of Abbreviations

1D 1 dimensional

2D 2 dimensional

3D 3 dimensional

AFM atomic force microscope

Al Aluminium

AlAs Aluminium Arsenide

Au Gold

BEC Bose–Einstein condensate

CAD computer–aided design

CCD charge–coupled device

CMOS complementary–symmetry/metal–oxide semiconductor

dw-2000 Design Workshop 2000™

e-beam electron beam

FIB focused ion beam

GaAs Gallium arsenide

Ge Germanium

IPA isopropyl alcohol, Isopropanol, C_3H_8O

IR image reversal

Li Lithium

MBE molecular beam epitaxy

MIBK methyl isobutyl ketone

MIF metal ion free

MOT magneto–optical trap

N Nitrogen

Ni Nickel

PdAu Palladium Gold

PMMA poly–methyl methacrylate

Rb Rubidium

RF radio frequency

RIE reactive ion etching

rpm revolutions per minute

RTP rapid thermal processor

SEM scanning electron microscope

Si Silicon

SiO_2 Silicon dioxide

Ti Titanium

TOF time of flight

TTV total thickness variation

UHV ultra high vacuum

UV ultra violet

Chapter 1

Introduction

'Atom chip' is an established vocable in quantum optics for a few years now [Sch92]. It expresses the combination of sensitive ultra cold neutral atom experiments with micro fabrication technology [Hin99, Rei02, Fol02]. Atom chip based research is mainly performed with neutral alkali atoms. The analogy of guiding atoms in traps above a microchip, like guiding electrons in the wires of a microchip, gave the atom chip its name.

The idea of atom chips was born in 1995 have been neutral atoms were trapped for the first time with a current–carrying wire [Sch95a]. To miniaturise these wires and to implement them on a surface was proposed in the same year [Wei95]. First results from micro fabricated wire traps were published a few years later [Rei99, Dek00].

Atom chips are an essential part of the experiments of this group [Fol00, Bar00, Krü02, Kas03b, Bru05, Sch05b, Wil06b, Pie06]. They enable to create complex and extremely well defined magnetic potential traps for neutral atoms down to a microscopic range. The maximal current densities of micro fabricated gold wires is $> 10^7\,\mathrm{A/cm^2}$, which is sufficiently high for experiments with cold atoms. Trap frequencies of $\omega_\perp = 2\pi \cdot 10\,\mathrm{kHz}$ can be created. Due to the miniaturisation of the trapping wires, high currents are not necessarily needed to create steep trapping potentials. Still, high currents are possible in micro fabricated wires with large cross sections. The ultra high vacuum compatibility of atom chips enables to trap atoms at a distance of about a micrometre from the trapping wires. The strong magnetic field gradient close to micro fabricated wire traps allows to cool trapped cold atoms further, reaching Bose–Einstein condensation. These are the major advantages of micro fabricated atom chips compared to classical magnetic traps. For commercial use the scalability of atom chips might also be an advantage some day.

The atoms are cooled in a magneto optical trap before they are loaded to the magnetic traps of the atom chip. The atom chip serves as the mirror for the magneto optical trap [Lee96]. Therefore it has to be highly reflective for laser beams. Not only the reflectivity, also the cleanliness of the mirror is of high importance. Scattering is avoided by high surface qualities.

The atom chips fabricated during this thesis show significantly different properties than atom chips fabricated in other groups. In this thesis all metal structures on the atom chips are vapour deposited which leads to smooth bulk metal compared to electroplated metal wires [Drn98, For02b, Lev03, Hom05, Wil05b]. As a result the potential–roughness created by the wires is about two orders of magnitude smaller, than it is on atom chips fabricated by electroplating.

The atom chips fabricated during this thesis were manufactured at the Weizmann Institute of Science [Gro04] while the experiments with ultra cold neutral atoms on these atom chips are performed at the University of Heidelberg.

Atom chips are used in many atomic physics and quantum optic experiments [Rek04, Cir05, Dik05, Est05]. The development of atom chips is pushed further every day, and the atom chip starts to enter other fields of physics as well. Lately molecules and ions [Bou04, Sti06] have been trapped on chip based devices.

This thesis starts with an introduction to the basics of experiments with neutral atoms on atom chips. In this chapter the theoretical background from the creation of magnetic wire traps to the detection of the atoms is explained. For advanced atom chip fabrication a short introduction to semiconductors is added. The fabrication of the atom chips itself is the central topic of this thesis. It begins with designing the layout of the atom chip which is explained in Chapter 3. This is followed by a chapter about the experimental setup of the atom chip in the ultra high vacuum chambers of our group.

The following two chapters explain the fabrication of atom chips in detail. Chapter 5 describes the preparation of a regular atom chip with tall (up to 5 μm) micro fabricated and evaporation deposited gold wires. To pay attention to extremely clean surfaces and accurate fabrication is of major importance. The fabrication technique of Chapter 5 is the fundament for more sophisticated atom chips. Their fabrication is described in the second fabrication chapter. Multi–layer, sub–micron structured and semiconductor atom chips are described in this chapter, as well as atom chips with added micro optics. Also further fabricated atom chips like coated atom chips or atom chips which are machined by a focussed ion beam are discussed in this chapter.

The characterisation of atom chips is described in Chapter 7. To find the maximal save current density of a fabricated wire thermal properties of the atom chips are investigated.

Finally experiments and the results of the experiments with atom chips fabricated during this thesis are introduced in Chapter 8. All experimental setups and their results are briefly contemplated. This thesis ends with a summary and an outlook. The outlook is followed by the appendixes where short recipes of the fabrication can be found.

Chapter 2

Theoretical background of atom chip experiments

This chapter gives an introduction on the use of atom chips and provides the theoretical background needed for this thesis. Explained are techniques to cool and trap neutral atoms on atom chips. The advantages of atom chips for quantum–optical experiments like micro fabrication and disorder potentials are explained as well as the detection of the investigated atoms. This chapter begins with a very short overview of ultra cold neutral atom experiments and finishes with a brief introduction on semiconductors.

Ultra cold atom experiments

Experiments with ultra cold neutral atoms consist of the following steps:

magneto optical trap The desired atoms are trapped in a magneto optical trap. This contains a quadrupole like magnetic field with a superimposed laser field, which also cools the atoms.

optical pumping The cold atoms are pumped optically into a quantum state that can be trapped by a magnetic trap.

magnetic trapping In the atom chip experiments of this group, magnetic traps are created by electric currents. First they run through solid copper wires underneath the atom chip and finally through wires on the atom chip itself. Experiments with the atoms are performed in these magnetic traps.

imaging The experimental results are obtained by detection of the atoms.

The next sections explain the individual steps of these experiments with ultra cold atoms in detail. Most explanations are specific for the experiments of this work group which uses the atom chips fabricated during this thesis, but the concepts are very general.

2.1 The magneto optical trap – MOT

Neutral atoms can be trapped in a magneto–optical trap (MOT) [Raa87]. By using the atom chips fabricated in the context of this thesis ^{6}Lithium, ^{7}Lithium and ^{87}Rubidium are trapped. In a MOT the atoms are cooled by laser beams.

Cooling alone does not trap the atoms. An inhomogenous magnetic field causes a position dependent Zeeman–shift. Counter propagating laser beams are circular polarized with

opposite polarization (σ^+ and σ^-). These laser beams interact with the correct Zeeman–split atom [Chu85], which results in a force to the centre of the magnetic field. The static inhomogenous magnetic field can be created by a pair of anti Helmholz coils.

In the following paragraphs laser cooling and the mirror MOT are introduced. They are important for the experiment, in that they deliver pre–cooled atoms for the traps on the atom chip.

2.1.1 Laser cooling

The average kinetic energy of an atom in an ensemble is equivalent to its temperature T:

$$\langle E_{kin} \rangle = \frac{3}{2} m \langle v_i^2 \rangle = \frac{3}{2} k_B T \,. \tag{2.1}$$

While $\langle v_i^2 \rangle$ is the sum of the velocities of the three coordinates, m is the mass of an atom and k_B is the Boltzmann constant. Equation 2.1 allows to relate the velocity distribution of an atom cloud with a temperature. Reduction of the average velocity of atoms inside a cloud is called cooling.

Photons have a momentum [Ein17, Fri33], which is used to slow down atoms [Hän75, Win75]. Intensive monochromatic laser beams are pointed at the atom cloud from all directions [Wie91, Ric95]. Absorbing a photon changes the momentum p of an atom by $\Delta p = \hbar k$ as well as emitting a photon changes the momentum again. Since this photon is not necessarily emitted in the opposite direction of its absorbtion but rather statistically distributed over all directions, the atom experiences a net average momentum transfer in the direction of the laser beam. For cooling in a trap, the laser light is red detuned to the resonance of the atom. A momentum transfer is only possible, if the atom moves in the direction of the light. In this case the doppler shift compensates the detuning, and the light becomes resonant. Red detuned laser light shining at the atoms from all directions always results in a force which is antiparallel to the direction of the movement of each atom. Because of statistical absorbtion and emission of photons the velocity of the atoms can not be cooled below the Doppler temperature [Win79].

In 1997 the Nobel Prize in physics was awarded to S. Chu, C. Cohen–Tannoudji and W. D. Phillips for their work in laser cooling [Phi82, Chu85, Asp86].

2.1.2 The mirror MOT

In atom chip experiments the atom chip itself blocks half of the space around the trap. This causes a problem for the MOT and for laser cooling, as laser beams have to shine on the atom cloud from all directions. In a mirror MOT cooling laser beams are reflected by a mirror [Lee96, Rei99]. From the atoms point of view the reflected laser beams appear to come from the blocked side. In the experiment two laser beams are directed parallel to the atom chip, while two shine onto the atom chip under an angle of 45° onto the surface. The atom chip itself is reflective, and the reflections of the laser beams simulate the two missing laser beams from the backside of the atom chip (see Figure 2.1). A reflected laser beam gains a phase shift, which turns its polarisation σ^+ to σ^- and vice versa. The polarisation of the laser beams is adjusted according to the requirements of the MOT.

In such a mirror MOT, the anti Helmholz coils for the quadrupole field are rotated by 45° with the laser fields to mount the mirror (atom chip) horizontally. These coils are mounted outside of the ultra high vacuum (UHV) chamber around the windows for the laser beams. Alternatively to the two coils, a flat solid U–shaped wire can be used to generate a quadrupole like field.

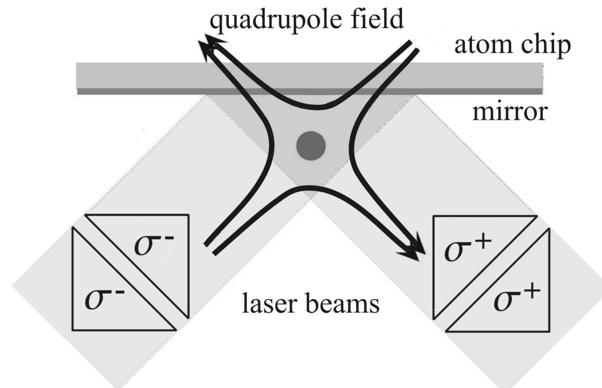

Figure 2.1: The mirror MOT. Two circular polarized laser beams are reflected in the same position on a mirror, which is the reflected surface of the atom chip. A third pair of laser beams is directed through the same point perpendicular to the image plane. The reflected cooling laser beams gain a phase shift, turning the polarisation. To build a trap, a static quadrupole field is added. Its centre is in the intersection region of the laser beams.

In atom chip experiments, the trapped atoms are transferred from the mirror MOT to a magnetic U or Z–wire trap. Additional magnetic fields and variations in the field generating currents allow displacement of the atom cloud above the mirror.

2.2 The magnetic trap

Trapping of neutral atoms in magnetic traps is possible since laser cooling is available [Mig85], as neutral atoms do not interact strongly with their surrounding, and fast atoms leave all traps. A neutral atom is manipulated by using the interaction between its magnetic moment and an outside magnetic field. The magnetic trap does not have a finite temperature limit, and is smaller and steeper than the MOT. The confinement of the atoms is stronger and the density of the atom cloud is increased. The magnetic moment μ of the mostly trapped maximal stretched state of an alkali atom is about as small as μ_B.

In the following sections, standard magnetic traps for neutral atoms are described, as well as the preparation of the atoms which are going to be trapped.

2.2.1 Magnetic traps

The potential U of an atom inside a magnetic field is:

$$U = -\vec{\mu} \cdot \vec{B}\,. \tag{2.2}$$

In the adiabatic approximation the potential is:

$$U = g_F \mu_B m_F B\,.$$

The magnetic moment of the atom is $\vec{\mu} = -g_F \mu_B \vec{F}$, where $\vec{F}$ denotes its total spin, g_F the Landé–factor of its hyperfine state and m_F its magnetic quantum number which is $\vec{F}$ for the maximal stretched state. The magnetic field is $\vec{B}$. If the Larmor frequency of a trapped atom is larger than the change of the magnetic field, its spin can follow the magnetic field adiabatically:

$$\frac{d}{dt}\frac{\vec{B}}{|\vec{B}|} < \omega_{Larmor} = \frac{\vec{\mu} \cdot \vec{B}}{\hbar}\,.$$

Two cases are distinguished. Firstly if $g_F m_F < 0$ the atom is called a high–field seeker and secondly if $g_F m_F > 0$ the atom is a low–field seeker. A high–field seeking atom follows a magnetic gradient into the direction of its maximum, while a low–field seeker is attracted to the magnetic minimum. Wings theorem [Win84] claims that it is impossible to build magnetic maxima outside charges. Most traps for neutral atoms trap low–field seekers, as it is done on atom chips.

2.2.2 Majorana spin flip losses

A trap for neutral atoms with a zero magnetic field $B_0 = 0$ looses atoms by Majorana spin flips [Maj32]. An atom flying through the zero magnetic field line ($B_0 = 0$) of the trap, is not able to adjust its magnetic moment to an outer magnetic field. The quantum states m_F are degenerated (see Equation 2.2). The atom can flip its spin to a non trapped state and leave the trap. Majorana spin flips can be suppressed by a small magnetic field, which guides the spin through the minimum. This principle is used in the Ioffe–Pritchard trap [Suk97].

2.3 The quadrupole trap

The first magnetic trap for neutral atoms was a quadrupole trap [Mig85]. A quadrupole field has a vanishing field in the centre $B_0 = 0$. Such a field is approximately realised by two coaxial coils with counter propagating currents (anti–Helmholtz configuration). Around $B_0 = 0$ the magnetic field can be approximated linearly:

$$B(x, y, z) = B' \begin{pmatrix} x \\ 2y \\ z \end{pmatrix}$$

with

$$B' = \frac{3\mu_0 I d R^2}{2(d^2 + R^2)^{\frac{5}{2}}} \ .$$

The distance between the two coils is $2d$ and their radius is R. The advantage of a quadrupole trap is a steep confinement. The higher the gradient of the magnetic field, the stronger the confinement of the trap. The disadvantage is a zero magnetic field in the centre of the trap which results in Majorana spin flip losses. Variations of the quadrupole trap, where the vanishing magnetic field in the centre is avoided, are often used for Bose condensation [Got62, Pri83].

In some of the experiments of this group, a quadrupole–like field is generated by an U–shaped wire below the atom chip [Bec02, Wil04]. The coils, which provide the homogenous field, are not necessary in this experiment.

2.4 Magnetic wire traps

To build flexible traps, electro magnets are used to create magnetic fields. A magnetic field is created by a controlled current which is pushed through a wire [Sch95b, For98, Den99, Rei99, Fol00]. These wires can be fabricated extremely precise, like on an atom chip, or machined in a workshop. In the experiment they are positioned inside the ultra high vacuum chamber.

The absolute magnetic field generated by a current flowing through an infinitesimal thin wire and the behaviour of its field at the distance r is given by:

$$B(r) = \frac{\mu_0}{2\pi}\frac{I}{r}, \tag{2.3}$$

$$\frac{dB(r)}{dr} = -\frac{\mu_0}{2\pi}\frac{I}{r^2}, \tag{2.4}$$

$$\frac{d^2B(r)}{dr^2} = \frac{\mu_0}{\pi}\frac{I}{r^3}.$$

For a wire with the radius R, the maximal gradient of the magnetic field is reached for the limit of $r \rightarrow R$. It follows from Equation 2.4 follows that the field gradient is proportional to the current density j inside the wire:

$$\frac{dB(r)}{dr} = -\frac{\mu_0}{2\pi}\frac{I}{R^2} \propto j. \tag{2.5}$$

To increase the gradient of a trap it is necessary to bring the trapped atoms close to a thin wire which carries a large current (see Equation 2.4). Atom chips are appropriate for this purpose, as they are able to withstand high currents while micro fabrication allows to tune their cross section precisely. Limits of the current in a micro fabricated wire on an atom chip are discussed in one of the following chapters.

2.4.1 The side guide

The side guide is the most simple trap for neutral atoms [Fri33]. A current pushed through a straight wire creates a radial field around it. This is superimposed with a homogenous magnetic field $\vec{B_b}$ (bias field) which is oriented perpendicular to the wire (see Figure 2.2). This superposition results in a line of zero magnetic field parallel to the wire, where the radial wire field and the bias field cancel each other. Around this line of minimal absolute field the field has a quadrupole–like shape. The position of the magnetic field minimum r_0, as well as the gradient of the magnetic field around the minimum are given by Equation 2.3. Together with the magnetic field $\vec{B}$ of the infinitesimal small wire at the distance r and the tangential unit vector $\vec{e}_\phi$, the equation becomes: $\vec{B} = 2 \cdot 10^{-7} \left(\frac{\mathrm{H}}{\mathrm{m}}\right) \cdot \frac{I}{r}\vec{e}_\phi$. With the bias field B_b follows:

$$r_0 = \frac{\mu_0}{2\pi}\frac{I}{B_b}, \tag{2.6}$$

$$B' = \frac{B_b}{r_0} = \frac{2\pi}{\mu_0}\frac{B_b^2}{I}. \tag{2.7}$$

The Equations 2.6 and 2.7 illustrate that the side guide gets closer to the wire when the current is reduced. As a result, the trap becomes steeper. The minimum of the trap has no magnetic field. A finite field in the minimum is caused by a slight misalignment ($\vec{I}$ not $\perp$ to $\vec{B_b}$) between the wire and the homogenous magnetic field.

Theoretically the wire of the side guide is assumed to be infinitely long. This causes problems in an actual experiment. Firstly an infinite wire is technically not possible, and it would secondly cause an infinite guide. This guide would not be a trap, as it does not have a 3D confinement. A actual wire is bend at some point. This opens new possibilities for atom traps.

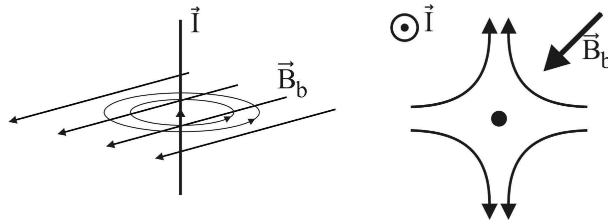

Figure 2.2: left: The magnetic field of a current in a straight wire combined with a homogenous magnetic field perpendicular to the wire creates a side guide. right: Top view onto the left figure. The resulting magnetic field around the side guide (black point). The side guide leads parallel to the wire with the current I and perpendicular to the bias field $\vec{B}_b$.

2.4.2 The U–wire trap

A wire bend twice into a U shape creates a U–wire trap if it is mounted with the leads parallel to the bias field (see Figure 2.3). The centre of the U works like the side guide. In contrast to the previously described side guide, this side guide has a finite length.

The leads add axial magnetic fields to the side guide. This leads to a longitudinal B field at the trap position, except for the middle of the trap. At this point the fields of the two leads compensate each other. Majorana spin flips appear at this position.

The size of the quadrupole–like field region is optimised by tilting the U–wire by 26° against the bias field [Sch01]. The field of the U–wire combined with the bias field can become almost identical to a quadrupole field by flattening the central part of the U–wire in the plane of the U [Bec02, Wil04].

2.4.3 The Z–wire trap

In the Z–wire trap the side guide is equally bend. Unlike in a U–wire trap, the leads are pointing into the opposite direction. The wire has a Z shape, hence the name of the trap. The opposite direction of the leads causes the current to flow in the same direction, and their fields never cancel each other (see Figure 2.3). The magnetic field minimum of the side guide is lifted to a finite value and never vanishes. This Z–wire shape creates a Ioffe–Pritchard like trap geometry which suppresses Majorana spin flips.

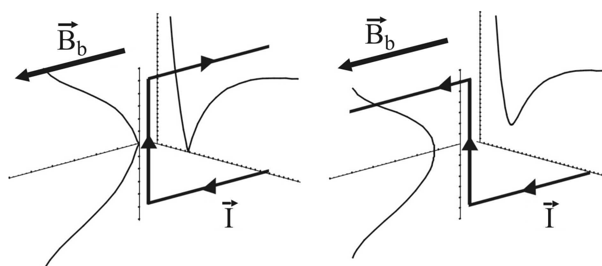

Figure 2.3: left: The bias field $\vec{B}_b$ and the U–wire trap are illustrated with the current inside the wire. The coordinate system through the centre of the trap illustrates the magnetic field parallel and perpendicular to the central trap wire. In the centre of the trap the magnetic field vanishes. right: The same illustration for a Z–wire trap. In this trap a small magnetic field remains also in the minimum.

2.4.4 Wire traps with more than one wire

The previously described trap geometries are the most common wire traps used on atom chips. It is possible to create magnetic traps with more than one wire and a homogenous bias field. A side guide created by two parallel wires with counter propagating currents needs a rotated bias field. The bias field is perpendicular to the plane of the two wires. This enables the two wires to change direction in the plane [Mül99, Lea02, Bru04, Luo04]. Everywhere they will form a side guide as $\vec{B}$ is perpendicular to the plane. The created potential is illustrated in Figure 2.4.

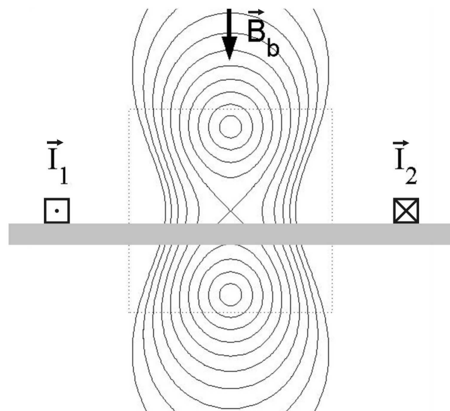

Figure 2.4: A double wire side guide is created by two parallel wires with counter propagating currents. A homogenous magnetic field $\vec{B}_b$ is added perpendicular to the wire plane. This configuration leads to two magnetic minima. One of them is located below the atom chip (grey bar) and not usable. Decreasing currents push the minima closer together, until they meet between the wires. Further decrease of the current leads to two minima between the wires.

With a few parallel fabricated wires it is possible to substitute the external homogenous bias field by the fields created by currents running through these wires [Dek00, Krü04, Est05].

2.4.5 Magneto electric traps

Neutral atoms can be trapped in magnetic potentials. They also interact with electric fields [Den97, Den98, Kle02, Fol02, Krü03]. For an alkali atom, with one unpaired electron in the s–state, the electric polarisability α is a scalar. With the induced dipole $\vec{d}$ and the electric field $\vec{E}$, the interaction is:

$$U_{el}(r) = -\vec{d} \cdot \vec{E} = -\frac{1}{2}\alpha E^2(r) \ .$$

The interaction of the induced dipole with the electric field is attractive. This draws the atom to the highest electric field. The Earnshaw theorem claims that an electric maximum cannot exist in free space which means that it is not possible to build a purely electric trap. In atom chip experiments, a magnetic trapping potential compensates the electric attraction, and prevents the atom from colliding with the charged object.

Magnetic traps interact with the magnetic quantum number m_F of an atom. While the magnetic trap depends on the quantum state m_F of the atom, an electric field interacts state independently with the atom. Therefore two different handles on the atoms are available in a magneto–electric trap. Electric fields are used to modulate magnetic traps.

2.5 Wire cross section

A fabricated wire on an atom chip has a finite cross section. This cross section is approximately rectangular and has a height H and a width W. The current density j inside the wire is:

$$j = \frac{I}{HW}\,.$$

For an infinitely long wire, the field components B_x (in the direction of the width of the wire) and B_y (in the height direction of the wire) can be calculated:

$$\begin{aligned} B_x(x,y,W,H) &= j\left[2y_-\left(\arctan\frac{x_-}{y_-} - \arctan\frac{x_+}{y_-}\right) + \right.\\ &\quad 2y_+\left(\arctan\frac{x_+}{y_+} - \arctan\frac{x_-}{y_+}\right) + \\ &\quad \left. x_-\ln\left(\frac{x_-^2+y_-^2}{x_-^2+y_+^2}\right) + x_+\ln\left(\frac{x_+^2+y_+^2}{x_+^2+y_-^2}\right)\right] \\ B_y(x,y,W,H) &= -B_x(-y,x,H,W)\,. \end{aligned}$$

The centre of the system ($x = y = 0$) is located in the centre of the wire. The edges of the wire are $x_\pm$ and $y_\pm$ ($x_\pm = x \pm W/2,\ y_\pm = y \pm H/2$). The strength of the magnetic field is maximal on the wire surface. For distances h much larger than the height H of the wire ($h \gg H$), the field above the centre of the wire ($x = 0,\ B_y = 0$) reduces to:

$$B_x(W,h) = 4j\arctan\left(\frac{W}{2h}\right)\,. \tag{2.8}$$

This is the field of a flat and broad wire. In atom chip experiments Equation 2.8 is a good approximation, as long as the cloud of trapped atoms is above a wide wire and far away from it ($h \gg H$). The magnetic field reduces to $B(h) = 2I/h$ if the distance between the atom cloud and the wire is also much larger than W ($h \gg W$), which is the magnetic field of an infinitesimal small wire.

In the middle of the wire ($x = 0$), the field gradient is given by:

$$\frac{\partial B}{\partial r}(h,W,H) = 4j\left[\arctan\left(\frac{W}{2h}\right) - \arctan\left(\frac{W}{2h+2H}\right)\right]\,. \tag{2.9}$$

The potential gradient at the trap minimum is of interest in the experiment. For $h \gg H$ equation 2.9 reduces to:

$$\frac{\partial B}{\partial r}(h,W) = 8j\left(\frac{W}{W^2+4h^2}\right)\,.$$

The field gradient grows for smaller distances between the trap and the wire. The magnetic field and its field gradient are plotted in Figure 2.5.

The width of the wire defines the area of contact between the wire and the surface of the substrate to which it is attached. Current inside a wire produces heat. This heat dissociates through the intersection to the substrate. The wider a wire, the larger the area of contact to the substrate, and the better the heat is transferred [Gro04].

2.5.1 Finite size effect

Strong confinement is caused by high magnetic field gradients. In theory the field gradient rises with decreasing distance to the wire, as visible in Figure 2.5 (right). In the vicinity of

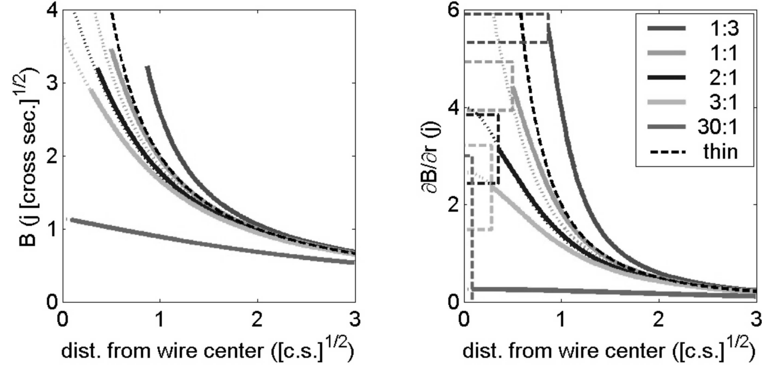

Figure 2.5: Calculations of magnetic fields and magnetic field gradients for rectangular wires with different aspect ratios of width to height. left: Magnetic field strength B plotted against the distance from the wire (in the centre above the wire). The solid lines show the calculated magnetic field, while the dotted lines refer to flat wire approximations. The field of an infinitely thin wire is illustrated by the black dashed line. right: Field gradients above the centre of the wires. The scales of the wires are displayed with dashed lines.

a real wire the gradient of the field does not rise like Equation 2.9 predicts. At a distance similar to the width of the wire, the finite size effect limits the rise of the magnetic field gradient. The distance to the edges of the wire does not change as fast as before, if the distance to the wire is reduced below its width. Even if the distance to the wire surface is zero, the distance to the edges still is $W/2$. Reducing the distance to the wire below the width of the wire therefore reduces the effective size of the wire.

The optimal aspect ratio of height to width of a wire is 1:1. A wide wire is limited by the finite size effect, while a wire which is taller than wide is due to its own height unable to bring the trap close to its centre.

Standard wires, which are fabricated for atom chip experiments, are wider than they are tall. Therefore experiments require wires with a small width. The distance to a narrow wire can be reduced much further than to a wide wire without loosing effective wire size. Micro fabrication of wires provides the techniques to structure wires as small as desired, to gain strongest confinement in the trapping potentials. Micro structured atom chips, like the ones produced during this thesis, provide narrow wires to create strongly confined traps.

2.6 Trap confinement

The potential of a magnetic trap is approximated by a three dimensional harmonic oscillator. The confinement of a trap for cold atoms is characterised by its trap frequencies. The trap frequencies of an atom with mass m are:

$$\omega_\perp = \sqrt{\frac{m_F g_F \mu_B B'_\perp}{m B_0}}$$

in the transverse direction, and:

$$\omega_\parallel = \sqrt{\frac{m_F g_F \mu_B (B_\parallel + B_0)''}{m}}$$

in the longitudinal direction, with the Ioffe–Pritchard like offset field B_0.

The trap confinement depends on the gradient of the magnetic field. The steeper the trap, the stronger the confinement. The offset field cuts off the minimum of the trap. The smaller B_0, the stronger the confinement. A graphical illustration of these relations is given in Figure 2.6.

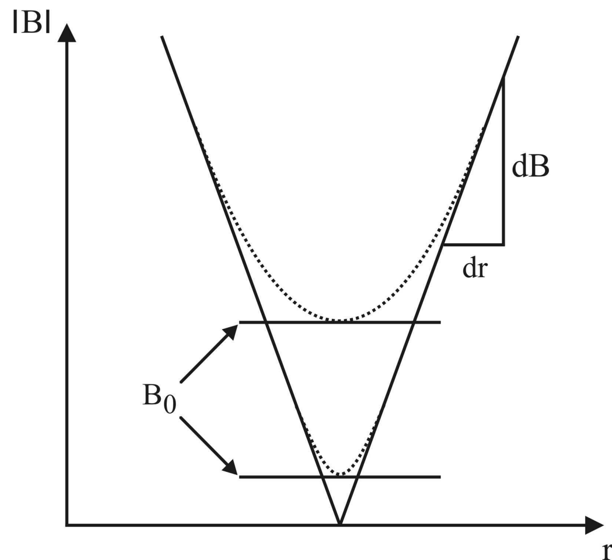

Figure 2.6: The confinement of a magnetic trap is defined by the gradient of the magnetic field and the offset field B_0. The larger the gradient and the smaller B_0, the stronger the confinement. The dotted lines indicate the harmonic trap approximations for the two offset fields.

As a result of Equation 2.7 it follows that the gradient of the magnetic field grows with decreasing distance to the wire. This is limited by the finite size effect and can be tuned with micro fabricated atom chips. Increasing the current inside the wire also increases the gradient. But high currents require solid wires. Therefore it is more efficient to miniaturise the wire.

In the experiment strongly confined traps are required to enlarge the collision rate between the atoms. High collision rates are necessary for fast rethermalisation in cooling processes. High trap frequencies are also desired to modify the potential in acceptable times adiabatically, as adiabatic changes have to be slow compared to the trap frequencies.

2.7 Disorder potentials

Numerus disorder potentials originate in non perfect wires. The field–generating current inside a wire does not flow straight. Due to grains, defects, varying wire shape (width and thickness) and material variations the current locally changes direction slightly. Also the current density is affected and changes locally with the diametre of the wire.

The gradient of the magnetic field is proportional to the current density (see Equation 2.5). A change in the direction of the current adds a bit of the magnetic field of the wire to the offset field. Both effects modulate the confinement of the trap, adding small dips and bumps into the trapping potential. They can be caused by roughness of the edge and surface of the wire [Wan04] or by changes of the current inside the wire itself [Krü05]. The modulations are visible through the behavior of trapped atoms with an energy on the order of these variations [Kas03b, Sch04a]. A trapped cloud of cold atoms splits up into several

small clouds, which locate in the local minima of the disordered potential.

Disorder potentials have been observed by many groups [Lea02, For02a, Jon03, Est04]. These groups move their ultra cold atom cloud close to the trapping wire, until it splits into fragments. Disorder potentials are visible at a distance of about $50\,\mu$m from the surface. In experiments performed within this group disorder potentials are visible only a few micrometer above the surface [Wil05b]. This is due to the technique used for wire fabrication. While most groups used electroplating, the vapour deposited wires fabricated during this thesis have a bulk material, which is about two orders of magnitude better in terms of surface roughness and grain quality. The fabrication of atom chips is a main part of this thesis and is described in the following chapters.

2.8 Atom preparation: the trapped quantum states

The experiments using the atom chips fabricated during this thesis trap neutral lithium and neutral rubidium atoms. These atoms are prepared in special quantum states, which are suitable to trap them and perform the desired experiments. The maximal stretched state with $\mu = \mu_b$ is the most commonly trapped state, as it is bound strongest in the trap. ^{7}Lithium has been trapped in one experiment, most other experiments of this group use ^{87}Rubidium. One of the experiments traps both ^{6}Lithium and ^{87}Rubidium at the same time. Other groups also trap and cool lithium [Vul98, O'H99] or rubidium [For98] and other neutral atoms (caesium [Web00, Tho04], hydrogen [Fri98], sodium [Raa87, Ket93, Dav95, Pov05], potassium [III95, Web01]). These are just some of the groups trapping ultra cold atoms, but not all of them use atom chips.

Most experiments trap neutral alkali atoms, as mentioned above. Alkali atoms have one unpaired electron in the s–state, which makes theoretical treatment of them relatively easy. Their excited states have well separated transitions, which is convenient for cooling and preparing the atoms in a desired quantum state. A short overview of the use of lithium and rubidium is given.

2.8.1 Trapping lithium – Li

Bosonic and fermionic lithium is trapped in magneto–optical traps. It is evaporated from an oven into the vacuum chamber and slowed down by laser cooling in the experimental area. Only the desired quantum state is trapped, as atoms with other quantum states leave the trap automatically.

^{6}Lithium is a fermion. In natural Lithium its occurrence is 7.3%. The trapped quantum state is $|F = 3/2, m_F = 3/2\rangle$.

^{7}Lithium is a boson. The occurrence of ^{7}Lithium in natural lithium is 92.7%. The trapped quantum state is $2^2S_{1/2}$, $|F = 2, m_F = 2\rangle$. For previous cooling in the MOT the transition to the state $2^2P_{3/2}$, F = 3 is used.

2.8.2 Trapping rubidium – Rb

The trapped quantum state of ^{87}Rubidium is $|F = 2, m_F = 2\rangle$. Before trapping in a magnetic trap, the D_2–line ($5^2S_{1/2} \rightarrow 5^2P_{3/2}$) is used for cooling in the MOT. The rubidium enters the trapped region from a dispenser inside the vacuum chamber. It is cooled and pumped by laser beams into the trapped quantum state.

2.9 Evaporative cooling to quantum degeneracy

To cool trapped atoms far below the temperature of laser cooling, evaporative cooling is used [Hes86, Lui96, Dav95, Val99]. Evaporative cooling removes the hottest atoms from a cloud. After rethermalisation by elastic scattering, the temperature of the cloud is lower than before. In a magnetic trap this is done by directing a radio frequent (RF) field into the experiment. In our experiments, this frequency ν_{RF} is between a few hundred kHz and 20 MHz. The RF selectively induces spin flips of the high energetic atoms to a non trapped state. Evaporative cooling leads to a continuous loss of atoms, but allows to cool a cloud of atoms until most remaining atoms are in the ground state.

2.10 Detection of neutral atoms

Atoms are trapped in a MOT or in a magnetic trap to the atom chip. During an experiment the atoms react on field and potential variations. The result of the experiment is encoded in the atoms themselves.

Location and density distribution of the atoms can be seen directly by taking an image of the atoms in the trap. Releasing the atoms from their trap causes free expansion of the cloud (TOF) and an image in the momentum space is taken after some time. The atom chip is mounted upside down to allow free expansion, when the atoms follow gravity (see Figure 2.1). In a released cloud of hot atoms the atoms keep their velocity and the cloud expands in the gravity potential. For a released cloud of condensed atoms, however, the chemical potential is the dominant energy. Therefore the expansion of the cloud in the two strongly confined directions is faster than in the third, which leads to the characteristic change of the shape of a cigar shaped BEC in TOF pictures. Observing at different times after the release shows the velocity distribution and the direction of their velocity in the trap.

Problematic is the resolution of the imaging system. Sometimes the atom cloud is small and close to the surface of the atom chip. Also the intensity of the signal can be weak. Two different imaging techniques are used to achieve a sufficient image resolution. Absorbtion and fluorescence imaging are used for atom observation in the experiments of this group. In both cases one picture of the atoms is taken per experiment. The cloud of atoms is heated during imaging and the information is lost [Sch02]. To take another image, the experiment has do be performed again.

Fast CCD (charge–coupled device) cameras with a high photon count efficiency are used in combination with high resolution optics to acquire these images.

2.10.1 Absorbtion imaging

To perform absorbtion imaging a pulse of resonant laser light illuminates the atom cloud, a CCD camera detects its shadow. This shadow gives information of the atom density along the path from the laser to the camera.

A second image of the background (laser beam profile) is taken when the atoms have left the area. The quotient of the two pictures shows a clear image of the atomic cloud. Many imaging problems can be compensated with this technique [Eng02].

2.10.2 Fluorescence imaging

The atoms are excited by a short pulse of resonant laser light. After the lifetime of the exited state, the atoms emit fluorescence light. Using the spontaneous emission in all directions it is possible to take images of the atom cloud from different directions at the same time.

The photon momentum transfer causes a change of the atom location and velocity. This is problematic, as the emission is spontaneous after a non defined time, which results in a blurred image of the atom cloud.

In a large or dense atom cloud the possibility of re–absorbtion of an emitted photon is high and has to be taken into account [Bar01]. Fluorescence imaging is a simple technique with some inaccuracies.

2.10.3 Phase contrast imaging

A third imaging technique is the phase contrast method. The difference of the optical density in the atom cloud compared to the vacuum causes a phase shift of light passing through it [Ket99]. With a phase plate the phase contrasts can be transferred into density information which is detected by a CCD camera.

2.11 Fermions and Bosons

In atom chip experiments the behaviour of bosons and fermions at low temperatures is studied. In some experiments bosons and fermions are trapped at the same time at the same location. Their interaction is observed and used. A fermi gas for example can be cooled by a Bose–Einstein condensate.

Fermions

Fermions are particles with a half–integer spin. The half–integer spin causes the fermion to have a antisymmetric wave function. Fermions follow the Fermi–Dirac statistic. Due to the Pauli exclusion principle [Mas05] every quantum mechanical state can be occupied by one fermion only. At zero temperature every quantum state up to the Fermi level is filled with exactly one fermion. This Fermi sea is reached and investigated with trapped and cooled fermions. Due to the different states of all fermions, collisions between the particles are prevented. Cooling and rethermalisation with only one trapped spin state is not possible. Often Bosons are used as cooling agents for fermions. Atom chips fabricated during this thesis are used to trap ^{6}Lithium fermions [Huf05].

Bosons

Bosons are indistinguishable particles with an integer spin. In experiments with atom chips from this thesis, ^{87}Rubidium and ^{7}Lithium bosons are trapped, cooled and investigated. Bosons follow the Bose–Einstein statistic. The number of bosons in one quantum state is unlimited. This leads to the Bose–Einstein condensation of particles, where all particles share the same quantum state.

Bose–Einstein condensate – BEC

A cooled cloud of bosons condenses in a Bose–Einstein condensate. This BEC is a self–contained state of matter. Below a critical temperature, bosons start condensing in the BEC. All particles in the BEC share the same quantum state, which is the ground state. Due to the low energy of the bosons, their wave functions overlap. BECs can be realised on atom chips in many groups [Ott01, Hän01, Sch03].

In 2001 the Nobel Price was awarded to E. A. Cornell, W. Ketterle and C. E. Wieman for the first realisation and experiments with BECs.

2.12 Semiconductors

Most atom chips fabricated during this thesis are fabricated onto a semiconducting substrate. The latest developed atom chip contains an entire semiconductor chip. Therefore a short discussion on semiconductors is given.

Semiconductors are materials, which can be insulating or conductive, depending on their environment. The most common semiconductors are silicon (Si) and gallium arsenide (GaAs). Both are used during this thesis to fabricate atom chips. At zero temperature, all semiconductors are insulators, as the uppermost filled electron energy band is completely occupied. At finite temperature a semiconductor has a resistance which is higher than the resistance of a conductor [Yu04].

Compared to an insulator a semiconductor has a band gap which is small enough to populate the conduction band with electrons. Room temperature adds enough energy to lift electrons from the valence band into the the conduction band. Also light often increases the conductivity of a semiconductor, as the photons are absorbed by electrons and the energy lifts them over the band gap (this is used for photovoltaic to generate electric power [Lof56], or to build a laser, by electrons emitting light, when they go the other way around [Cho94]).

The band gap of a semiconductor can be modified during its fabrication. Donators or acceptors are grown into the material with high accuracy. A heterojunction contains layers of different materials in varying composition. This leads to special features of the material, which can be for example a defined band gap, added impurities and charge carriers in conducting layers or stop layers for etching techniques.

Atom chips are fabricated from semiconductors during this thesis. The semiconductor was used as substrate and as semiconductor. Atom chips using the semiconducting abilities contain wires fabricated from–non metal material. Non–metal wires are thought to be less noisy than metal wires [Dik05]. Semiconductor wafer are grown from a perfect crystal. The wafer provides a flat surface and the processing of the material is well known. Together with the electric properties of the semiconductor its thermal attributes can be affected precisely.

In difference to metal wires on top of a substrate the charge carriers in a semiconductor are inside the substrate itself. A semiconducting material is doped in one ore more layers with special atoms. This is done by growing the substrate epitaxial in a molecular beam epitaxy (MBE). The conducting layer is structured and contacted to guide currents in a defined way. This can be done by removing the charge carriers or by depleting them.

Depletion is done by metal structures on the surface of the semiconductor. Charging these structures depletes the charge carriers in the semiconductor and the conductive film inside the substrate is structured. This is an established technique for thin doped layers. An advantage is that this technique is flexible as it is possible to tune the depletion by charging the surface structures. Most transistors operate this way. A disadvantage is that charged metal structures on the surface of the chip are needed.

Removing the charge carriers is the alternative. This is done by etching which causes a rough surface. Advantages of this technique are that no metal is needed on the surface and a thick layer of doped material can be structured as etching can enter deep inside the material. The semiconducting materials used during this thesis are described briefly in the following sections.

Silicon – Si

Silicon is element 14 of the periodic table of the chemical elements and the second most abundant element in the earth's crust. Pure Si is a group IV semi conductor. Doping Si with impurities of arsenic causes n–type, doping with boron causes p–type behavior. Silicon does

not react with acids, except for nitric and hydrofluoric acid.

During this thesis, Si is used as substrate for atom chips only. The semiconducting properties are not used to fabricate wires. For better heat conduction most substrates are doped p–type with boron. On top of the Si a silicon dioxide layer is fabricated to provide an insulating surface. Advantages of Si as substrate are its flat surface, its common usability, SiO insulation layer and its low price.

Gallium arsenide – GaAs

GaAs is a semiconductor of the III–V group. Its electron velocity and mobility are higher than the ones of Si, and less noise is generated at high frequencies (up to 250 GHz). Due to a higher break down level GaAs can be operated with higher power. The band gap of GaAs is direct which enables emission and absorbtion of photons.

GaAs is usually combined with aluminium arsenide (AlAs) or the alloy $Al_xGa_{1-x}As$. In a MBE a heterostructure of GaAs, AlAs and $Al_xGa_{1-x}As$ can be grown almost arbitrarily as their lattice constants are similar.

In atom chip fabrication of this thesis GaAs is used as a non–metallic conductor. A conducting layer is grown in a MBE and structured by etching. The details of the GaAs wafer used are given in Appendix C.5.1. Wire traps for ultra cold atoms are to be generated with the fabricated structures.

Advantage and disadvantage of GaAs at the same time is its cleavability. Cutting GaAs by cleaving is simple and generates straight edges. The disadvantage is that this brittleness makes the GaAs fragile. Another disadvantage of GaAs is that it is considered highly toxic and carcinogenic.

Chapter 3

Design of atom chips

The atom chip layout is designed with a *dw-2000*™ [1] program. The *dw-2000* program is written to design analog and mixed-signal integrated circuits.

After designing the atom chip layout in *dw-2000* the design is either transferred to a lithography mask or written directly onto the atom chip. This is both done by an electron–beam (e–beam) lithography machine[2]. The following paragraphs give an introduction into the use of the *dw-2000* program and design rules for atom chips. The specific layouts of the mostly used atom chips, designed and fabricated during this thesis are listed in Appendix C.

3.1 The *dw-2000* program

For the design of atom chips different layers are used. Each layer is transformed to a mask for optical lithography, or written directly onto the atom chip. In each layer several data types are needed, depending on the complexity of the design. The intensity of the electron beam during writing can be adjusted for every data type. This way every structure is written with the dose, which is needed for optimal results. A generally used design rule in the Submicron Center of the Weizmann Institute of Science is to use different data types for structures of these sizes: $> 5\,\mu$m; $\leq 5\,\mu$m and $> 2\,\mu$m; $2\,\mu$m and $> 1\,\mu$m; $\leq 1\,\mu$m and $> 0.5\,\mu$m; $\leq 0.5\,\mu$m and $> 0.2\,\mu$m and $< 0.2\,\mu$m. The data types are displayed in Table A.1 in Appendix A. The used base dose is $330\,\mathrm{mC/cm^2}$, but the variation of the data types has to be figured out in test writings.

For direct writing on atom chips, up to 23 different data types for a single layer are used in atom chips fabricated during this thesis. This is necessary to expose each part of the design with its optimal dose. Test writings are used to check the dose of the e-beam. If necessary, doses or design, especially the data types, are adjusted. Around small structures the dose of the writing e–beam needs to be adjusted a few times to reach high resolution. A fixed rule for data types cannot be given. It always depends on the design, the mask and its resist and the writing conditions. A single separate structure needs to be exposed with a different dose, then the same structure close to other structures. During exposure with an e–beam the surrounding of a structure is also exposed a little. This proximity effect reduces the necessary dose of the two (or more) structures close to each other. A program, which calculates the correct dose for each exposed point [RAI06] has not been available for this thesis.

Designing an atom chip requires close collaboration between the experimentalist and the fabricator, as the experimentalist has concrete conceivabilities, which kind of experiments he

[1] Design Workshop Technologies, *dw-2000*, Version: 7.50-c and higher, www.designw.com

[2] JSM 6400 Scanning Microscope, JEOL, Tokyo, Japan.

wants to perform with the atom chip, and the fabricator knows about the feasibility during fabrication. The first issue of the atom chip design is the size of the atom chip. This usually is given by the size of the used laser beams in the experiment and by the mounting. Even if the mounting should be designed around the atom chip, it is more easy to use a known mounting design, than building a complete new one. Another issue is the number of contact pads for the wires on the atom chip. They need space at the edges of the chip, and their amount is given by the number of wires needed on the chip. The size of chips produced during this work is $25 \times 30\,\mathrm{mm}^2$. This provides enough reflective area for the used laser beams which have a diameter of one inch (25.4 mm) and enough edge for electrical contact pads. The mounting is adjusted to this chip size.

The number of electrical contacts is also limited by the number of electrical feedthrough in the vacuum flange and the space the contact pads can take on the edge of the atom chip. In the beginning the standard atom chip mounting supported 24 pin feedthroughs into the ultra high vacuum chamber, without the leads for the solid copper structures below the atom chip. This design is characterized by 12 contact pads on each of the two 30 mm long sides of the chip (see Figure 3.1). The new generation of atom chips is mounted on a sample holder, which allows 35 pin electrical feedthrough from the vacuum chamber to the outside. The atom chip design has 36 contact pads (see Figure 3.2). One of them has to stay unconnected and is connected to the ground. Another one is used as the connection for the ground.

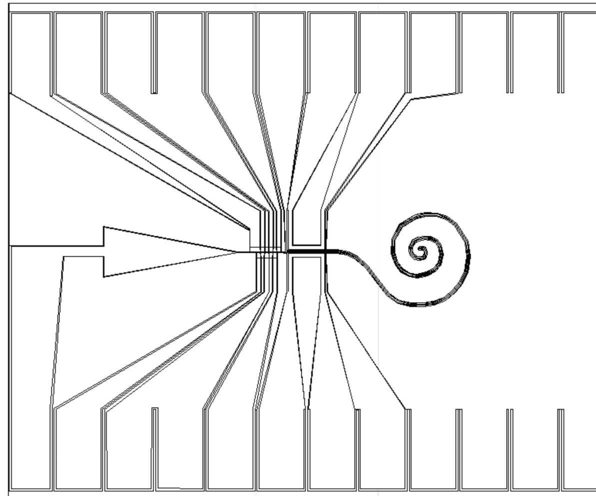

Figure 3.1: This figure shows the layout from the *dw-2000* CAD program for the spiral atom chip design. It contains 12 contact pads on each of the 30 mm long sides (top and bottom). In this special design, 7 pads on the right side are not used and grounded. U and Z shaped wires are located in the centre of this design.

Most experiments take place in the central part of the atom chip. In the old atom chip design, one optical axis to the centre of the atom chip (from left to right in Figure 3.1) is clear, while the other one (from top to bottom) is disturbed by the connections to the contact pads. In the new atom chip layout the pads are arranged in the corners. No contact pads obscure the centres of the edges, so that optical access to the centre of the chip is not disturbed by wire bonds.

Some atom chips have special features. This is according to the requirements in the experiment. For example the interferometer atom chip has an additional pad and a separate pin for the ground on one short (25 mm wide) side, next to the 12 pads. In the spiral atom

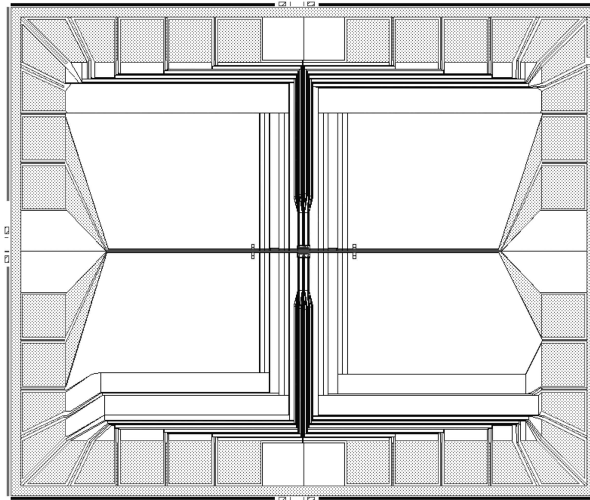

Figure 3.2: The new atom chip layout provides 36 electrical contact pads at the edges of the substrate, which are arranged with gaps in the centre of the sides to provide free optical access to the centre of the atom chip. The ground around the atom chip is separated in the top right corner. The dotted structures are multi layer structures.

chip design seven pads are not needed at all. All of them are grounded.

3.2 Designing an atom chip

To start a design in the *dw-2000*, a library and in there a structure has to be opened. To design the patterns in the desired size the scale and the grid are set according to the demands. A scale smaller than needed easily results in errors, as tiny structures or gaps, which are not visible in the current resolution, might be drawn accidentally.

The edge of the atom chip is defined first. It gives the surrounding of the atom chip. Next the contact pads are arranged. These give the first structure and show how much place is left on the atom chip. Now the experimental structures in the centre are designed. On atom chips for this group, trapping structures like U and Z shaped wires are designed. They are the largest structures and have to be aligned to the solid copper wires below the atom chip. The wires for the experiments are arranged around them. The distance between two structures is not problematic, as long as it is $5\,\mu$m or larger. The smallest size of structures and of gaps between structures in this thesis is $1\,\mu$m on a lithography mask. The size is limited by the wavelength of the light used in the optical lithography.

After finishing the structures in the central physics part, their connections to the pads are designed. To avoid high resistances of the structures, the leads from the pads to the centre are wider than the structures in the centre. This also prevents a wire from burning outside the centre where enough space is available and high current densities are not required. To gain more connections for structures, it might be possible to connect one end of different wires to the same pad. This side of the wires will be on the same potential. Usually it is grounded.

After all structures are finished, the ground is designed. The areas between the wires is grounded to avoid floating structures. The ground is also used as a mirror for the laser beams. The gap between ground and structures should be at least as big as the gap between the structures. A save distance is $5\,\mu$m. Outside the centre area the gap is drawn large

enough, to avoid any trouble during fabrication (about 10 μm and more), as the specific wire design far away from the trapping region does not effect the trap significantly any more.

The last few μm of acute angles are cut off. The tip of an acute angle is so small, that the e–beam would expose it with a dose between full and nothing. The mask becomes blurred (grey) in this part and the fabrication will become difficult, especially during lift–off. All grounded areas are connected to a grounded ring around the pads, to avoid floating surfaces.

Ground loops are closed circles in the ground wires of the experiment. They act like coils and can modulate the magnetic fields when currents are induced in them. They can interact with the trapped atoms and cause changed results of the measurement. Ground loops are avoided, especially on the atom chip which is close to the trapped atoms. As there are many grounded areas on the atom chip for the mirror surface, ground loops are likely to appear. The grounded ring around the pads, is disconnected in one place (see Figure 3.2). Around the atom chip cutting lines are drawn. These two 10 μm wide lines 100 and 200 μm away from the edge of the atom chip help during precise cutting of the atom chip to its final size in the end of fabrication.

Atom chips which need more than one mask during fabrication have alignment markings on all four edges. These markings help to align the next mask onto the pre–fabricated atom chip. One part of the marking is on the first mask, the second part is on a second mask. With these markings, illustrated in Figure 3.3 a pre–fabricated sample can be aligned to a mask with an accuracy of less than 1 μm (for their position see Figure 3.4.b).

A full multi–layer atom chip design is shown in the double Figure 3.4 and 3.5. This figure also illustrates the size relations of the different structures. So far the smallest patterns are 300 nm wide on the 30 mm long atom chip. This difference in scale of 10^5 can be easily enlarged to 10^6 by the use of direct e–beam writing.

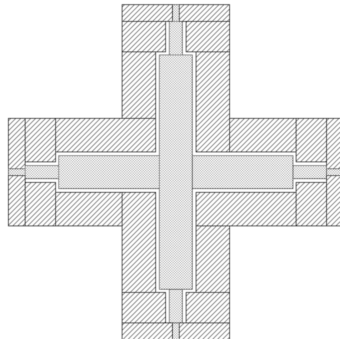

Figure 3.3: This *dw-2000* design of a marking is used to align a sample to a mask. The dotted cross is fabricated onto the sample, while the hatched surrounding appears on the next mask. For alignment the cross is moved into the surrounding. The ends of the cross are 2 μm wide. The different width allows rough and fine alignment with the same marking. In the wider parts a 1 μm gap is designed between cross and surrounding, since for the eye this is easier to align. The gap is well visible and can be equalized smooth. These markings make alignment to about 0.5 μm possible.

The completed design is converted to the data format required by the e–beam machine. The e–beam either writes a mask from the design or transfers it directly to the atom chip. In mask writing the design is transferred to a glass plate. During atom chip fabrication the glass mask is turned upside down. This causes the design on the atom chip to be mirror imaged, compared to the design in the *dw-2000*. The flip during lithography can be compensated by turning the design in the *dw-2000* just before writing it onto the mask. For direct writing there is no flipping.

3.3 Mask fabrication

In this thesis, e–beam lithography is used to fabricate masks for optical lithography. A chrome blank[3] is a glass plate evaporated with chromium. The chromium is covered with an electron sensitive resist[4]. This is the raw material for an optical lithography mask. An e–beam lithography system[5] writes the designed structure into this electron sensitive resist with an electron beam. After writing the resist is developed. Development of a 4000 Å thick resist takes 4 minutes in MF 312[6]. The developed resist partly covers the chromium in the shape of the written design. The uncovered chromium is etched away in an ATP 915[7]. The etching time in CR–7[8] is 45 to 50 seconds. Afterwards the remaining resist is removed with solvents, and the *dw-2000* design is transferred into the chromium on the glass. This mask is used for further fabrication. The mask is cleaned after each use and holds for many lithography processes.

Writing a mask for atom chips with e–beam is problematic due to the written size. Almost the full area of $25 \times 30\,\text{mm}^2$ has to be written. This takes time (about 10 hours in the machine used) and contaminates the electron beam lithography machine, as shooting high energetic electrons into the resist causes small particles to leave the sample. These contaminate the vacuum and the parts inside the vacuum.

Chrome blanks for this thesis were bought from a company[3]. These chrome blanks are covered with chromium and resist already. An e–beam lithography machine is not necessarily needed to produce a mask for photo lithography. Different techniques are introduced shortly:

Electron beam lithography: This technique is used for mask fabrication during this thesis. The resist on top of the chrome blank is exposed to electrons. These are accelerated and focussed onto the resist. The resolution is extremely high, due to the small wavelength of the electrons. Feature sizes of less than 10 nm are possible but not needed during this thesis. In e–beam lithography the resist is exposed to the narrow beam. This exposes one dot after the other. This is slow, but each dot can be exposed with the ideal dose. In e–beam lithography the sample is divided into squares. One of these squares is written, before the e–beam moves to the next square. At the edge of these squares stitching effects can occur. Stitching is a slight misalignment between two squares. During this thesis stitching inaccuracies have not been observed.

Laser lithography: The resist on the chrome blank is exposed to a laser beam. Like in e–beam writing, every point structure has to be exposed by itself. The limiting factor is the wavelength of the used exposure light. Structure sizes of $0.6\,\mu$m are achieved [Ins06]. Laser lithography is cheaper than e–beam writing, but not as accurate. For less accuracy it is also faster.

Optical pattern generator: The chrome blank is exposed by light through a groove diaphragm. Its limit is the minimal opening size of the groove diaphragm and its step size ($\sim 1\,\mu$m). In this technique every structure is exposed by itself through the rectangular diaphragm. It is cheaper than e–beam writing, but slower, as it works mechanically and its accuracy is worse than laser lithography.

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[3] EQZ 4006 2C AR3*–LD SAL601H, Hoya, London, UK.

[4] SAL–601 H, Room and Haas Electronic Materials Europe Ltd., Coventry, UK.

[5] 5FE lithography machine, JEOL, Tokyo, Japan.

[6] MF 319, Room and Haas Electronic Materials Europe Ltd., Coventry, UK.

[7] APT 915 Photomask Processor, Applied Process Technology.

[8] CR-7 Chromium Photomask Etchant, Cyantek Corporation, Fremont, USA.

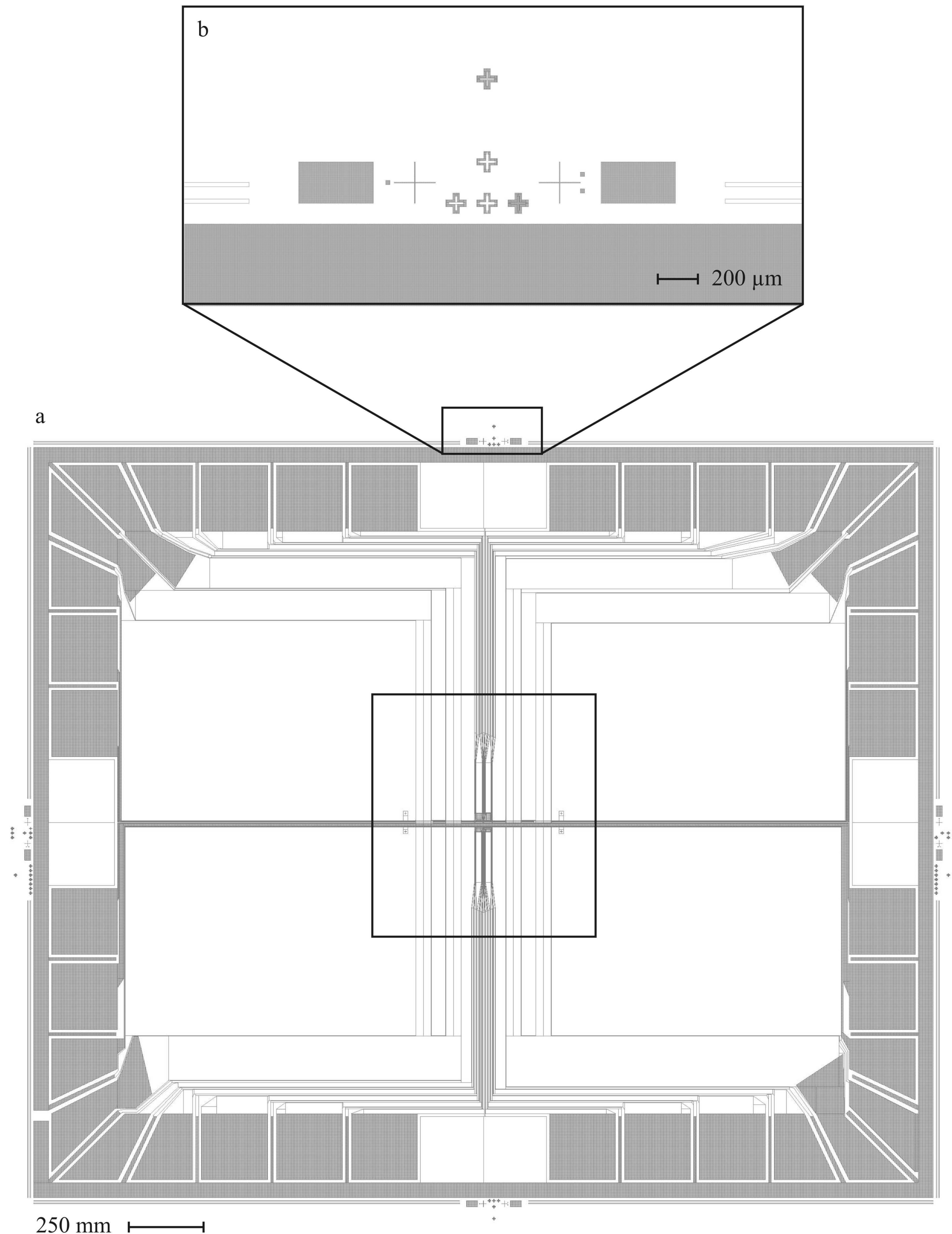

Figure 3.4: Layout of the ring multi–layer atom chip. a: The size of the atom chip is $25 \times 30\,\mathrm{mm}^2$. Different layer are hatched differently. The frame in the center illustrates part c, enlarged in Figure 3.5. b: Markings are located around the atom chip to align the different masks during fabrication to the structures on the atom chip. The thin crosses are markings for e–beam writing, the big patterns next to them are fabricated to find the e–beam crosses more easily.

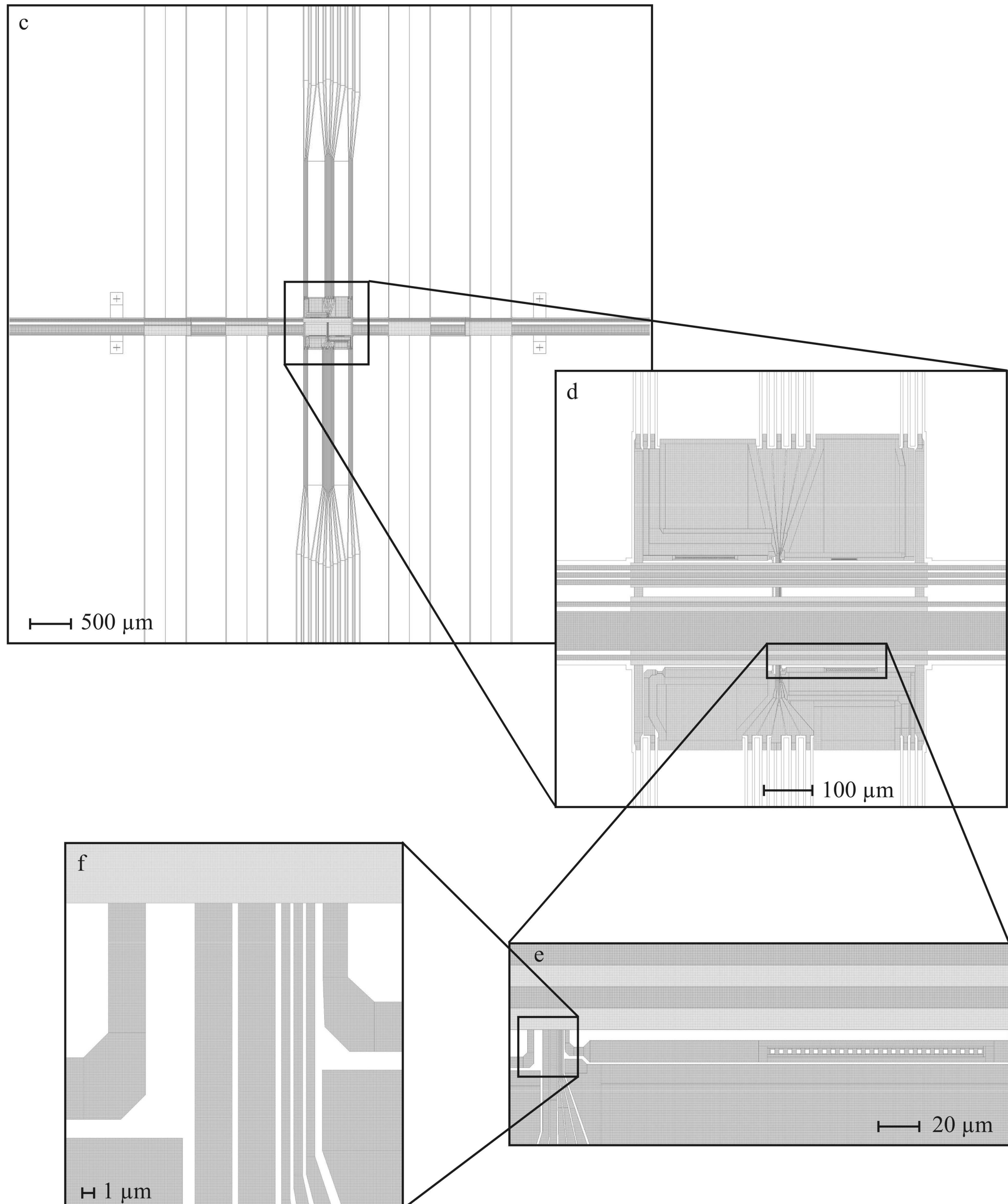

Figure 3.5: Zoom into Figure 3.4. c: The cental region of the ring multi layer atom chip. Wires from the top to the bottom are fabricated in the bottom layer. The wires in the middle from the left to the right are crossing them. They are fabricated on top of the bottom layer with a different mask. Both layers are separated by an insulation layer. This insulation is patterned during fabrication with a third mask. d: A $600 \times 600\,\mu\text{m}^2$ area in the centre of this layout is patterned by e–beam lithography. Therefore no optical mask is used but the e–beam writes directly on the sample. e and f: The feature size of the e–beam written part can be much smaller than the minimal size fabricated with a lithography mask.

Exposure through a negative: This technique is the cheapest and fastest. The design is printed onto a slide. The photosensitive resist on the chrome blank is exposed through this slide in a mask aligner. In best case the resolution is not limited by the slide, but by the wavelength of the exposing light (about $1\,\mu$m for $405\,$nm). In this case it is just as good, as the final lithography itself. This technique does not need any extra equipment in addition to the standard lithography.

The slide could be used as an optical mask for the sample directly. But its use is only for one time, as the slide becomes dirty from the resist and is not cleanable with solvents.

These are some techniques used for mask fabrication. The best resolution and accuracy is reached by e–beam lithography. The resolutions and advantages are summarised in Table 3.3.1.

machine	resolution	advantages
e–beam	$< 10\,$nm	very accurate but slow and expensive
laser lithograph	$\sim 600\,$nm	slow but cheaper than e–beam
opt. pattern generator	$\sim 1\,\mu$m	slow but cheaper than laser lithography
		and not that accurate
Light exposure	$\sim 1\,\mu$m	fast and cheap but inaccurate

Table 3.3.1: The four mentioned mask fabrication techniques are listed in this table with their resolution and advantages and disadvantages. A resolution below 1/10 of a μm is not important for mask fabrication, but it can be very important for direct patterning of structures on the sample.

Chapter 4

Atom chip setup

The mounting of the atom chip holds the atom chip inside the UHV chamber in a position close to the quadrupole trap, and supplies the connection from the atom chip to the outside of the experimental chamber. The mounting has to be solid, to prevent movements or vibrations of the atom chip, and vacuum compatible. It also has to contain electrical contacts for the field generating wires and lead away the heat, which is produced in the wires during the experiment. Most elements of the mounting are machined from oxygen free copper. Machinable insulating glass ceramics (macor or shapal) are used to stabilise the electric leads. Finally the heat is transferred to a water cooled steel stage. A mounting is displayed in Figure 4.1.

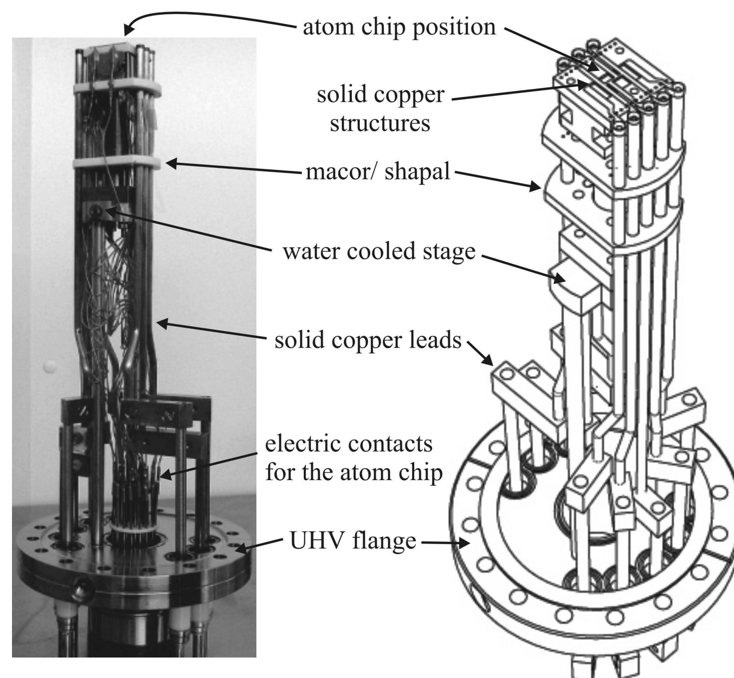

Figure 4.1: left: photo of the current atom chip mounting. right: CAD layout of the mounting from the photo on the left. The atom chip is mounted on top. Below the atom chip the solid copper wires are mounted. They are embedded in macor or shapal. This head of the mounting is connected by solid copper leads and wires, and it is fixed to a water cooled stage. The transition from the UHV chamber to the outside builds the vacuum flange with its electric feedthrough.

4.1 Ultra high vacuum – UHV

An atom chip experiment is done in an ultra high vacuum (UHV) chamber. The pressure inside the chamber is about 10^{-11} mbar. Rest gas inside the experiment chamber leads to collisions with the trapped atoms. The collisions cause an energy transfer to the trapped atom, which either changes its inner state to a non trapped state or gains enough energy to leave the trap. This results in a lifetime for a trapped cooled atom cloud off about 1 minute (in the experiments of this group).

The rest gas inside the UHV chamber mainly contains hydrogen molecules and atoms of the kind of the trapped atoms (mostly ^{87}Rb in the experiments of this group). The pressure is $\sim 10^{-11}$ mbar. The ^{87}Rb comes from the trap itself or from the time, when it was evaporated into the chamber, to be trapped. Only a few of these atoms, released from the dispensers, are trapped in the MOT and the wire traps. Evaporative cooling always frees some atoms and in the end of the experiment all atoms are released.

4.2 Mounting the atom chip

In the beginning of this work the atom chips were held on the mounting by mechanic clamps. These pressed the atom chip to the mounting and connected the electric pads on the chip. A picture of this is shown in Figure 4.2.

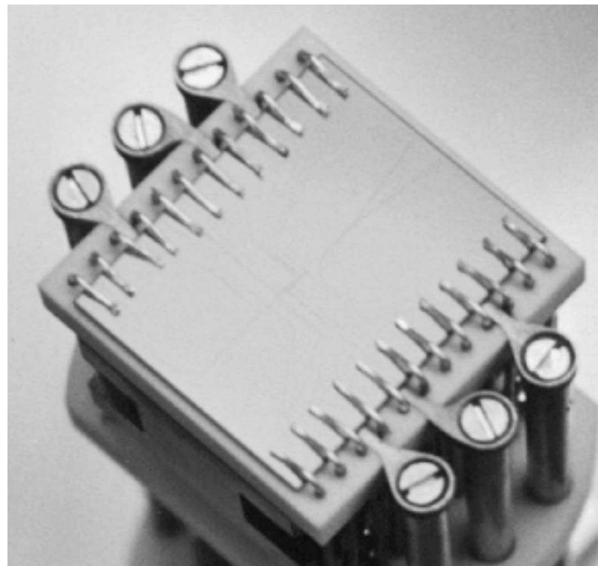

Figure 4.2: This picture shows an old sample holder. The atom chip is clamped by the electrical contacts. The 12 clamps on both sides of the chip are well visible. Next to them, the six leads for the solid copper structure below the atom chip are screwed to their leads.

The clamps have some disadvantages. It is difficult to move all clamps with a good contact to the atom chip at the same time. The main disadvantage is their size. The clamps are big, and they disturb the optical access to the atoms. An advantage of the clamp system is, that changing the atom chip can be done very fast. The same mounting is used for two atom chips in a few minutes. To change the atom chip, the mounting is taken out of the vacuum chamber, the old atom chip is unclamped and replaced by the new one. The same mounting is returned into the vacuum chamber with a new atom chip immediately. Before

use the UHV chamber has to be evacuated again.

In the new mounting, the electric contacts are established by wire bonds. These are much smaller than the clamps, so they disturb the optical access much less. Bond wires have good electric contact without adding any significant force to the atom chip. As they are thin (used are 25 μm aluminium or gold bond wires) several bond wires have to be used on one electric contact to guarantee sufficient current without burning them. Wire bonds are not able to hold an atom chip in a fixed position, if the mounting is mounted upside down in the vacuum chamber. To fix the atom chip and provide a contact between the back side of the atom chip and the mounting, the atom chip is glued with vacuum compatible glue to the mounting [Bec02].

To change an atom chip on a new mounting takes a lot of time. As the old atom chip is glued to the mounting, and the new one has to be contacted by wire bonds, it is more easy to build a second mounting for the new atom chip. By changing the whole mounting the atom chip can be changed fast. The new mounting and atom chip have to be prepared before the change. A new mounting is displayed in Figure 4.1 and a bonded atom chip is shown in Figure 4.3.

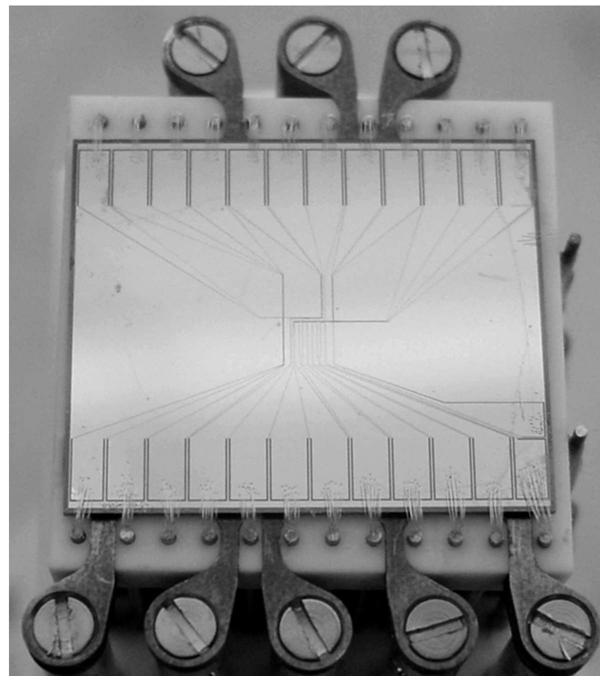

Figure 4.3: The new mounting for atom chips has wire bond contacts. These connect the electric pins with the pads on the atom chip. As the current through one wire bond is limited several bonds are set between appropriate pin and pad.
For this specific interferometer atom chip two additional contacts are used. These are glued to the mounting at the right side and connected by wire bonds. This has been one reason for the next atom chip and mounting design generation which has 36 contact pads.

Figure 4.4 shows a close up view of bonded and of clamped electric contacts. The clamps are much bigger than the bonds. They block the optical access from left and right, and produce much more stray light than the wire bonds. Also their connection is more difficult and not as reliable. As bonds need much less space, the pins can be set closer together. More connections on the edge of an atom chip are possible.

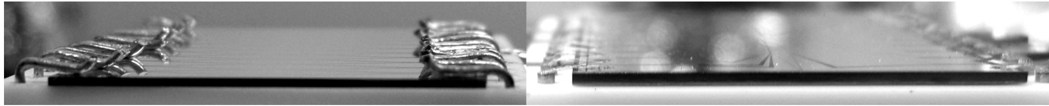

Figure 4.4: These two photos compare a mounted atom chip, which is contacted with clamps (left) to a wire bonded atom chip (right). The clamps are much larger than the bond wires. They disturb the optical access and scatter more light. Their size also limits the number of connections on one edge.

4.3 Solid copper wires

The connections to the atom chip are done by copper wires. These end in copper–beryllium pins, which are held by the ceramic next to the atom chip. The head of the pin is polished and sometimes covered with an evaporated gold layer (see Appendix E.0.8). The atom chip is connected by wire bonds from the pin to the pad of the atom chip. Next to the pins solid copper rods lead from the vacuum flange to the atom chip. A solid machined copper structure is screwed to these rods. The copper structure (see Figure 4.5) is implemented into the ceramics below the atom chip. The copper structure of this experiment has a shape like an H. With this shape it is possible to build U and Z–wire traps by pushing currents through the appropriate wires. Due to the solid copper and its diameter of about 1 mm^2 currents up to 60 A are pushed through this structure. Before the use of this copper H, solid silver wires have been used in U and Z shapes below the atom chip.

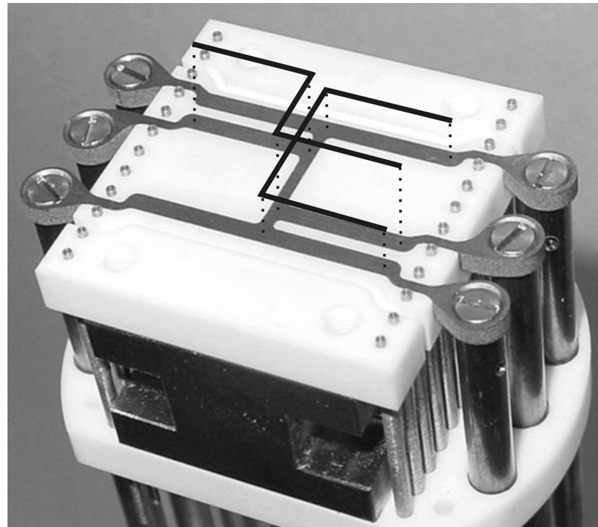

Figure 4.5: This picture shows the solid copper H mounted below the atom chip (without atom chip). The copper has a cross section of 1 mm^2 and up to 60 A are pushed through it. This shape allows U and Z–wire traps, which are illustrated. The copper is embedded in macor or shapal and screwed to the solid copper leads. Two times 12 copper–beryllium bond pins to contact the atom chip are visible at the edge of the macor.

The big current in the copper H structure builds a huge U or Z–wire trap at large distance from the atom chip to collect many atoms from the MOT. In this trap up to $> 10^8$ atoms are caught. They can be cooled in 10 – 20 seconds to a temperature below 1μK. The remaining $\sim 10^6$ cold atoms are transferred to smaller traps, created by wires on the atom chip.

Chapter 5

Fabrication of atom chips

The heart of atom chip experiments is the atom chip itself. The regular atom chip consists of a substrate with wires on top of it. Atom traps are generated by currents pushed through these wires. All fabrication is done in a clean environment (cleanroom of class 100) to protect the surface against dust and to allow well defined fabrication of clean structures on nanometre scale. For almost all atom chips this is the clean room in the Joseph H. and Belle R. Braun Center for Submicron Research in the Weizmann Institute of Science in Rehovot, Israel [Hum99]. There this thesis was supervised by Professor Dr. Israel Bar–Joseph. He holds the Jane and Otto Morningstar Professorial Chair in Physics.

A mayor part of this thesis is the development and fabrication of atom chips. The fabrication of atom chips is described in this chapter. For advanced atom chips special techniques are needed. First a regular atom chip production is explained. On this base special applications for more sophisticated atom chips are described in the following chapter. All fabrication recipes and the common atom chip layouts are listed in Appendix C.

5.1 Cutting atom chips

Most atom chips are fabricated on 700 μm thick doped silicon substrates. The silicon is doped, to provide good heat conductivity. A defined silicon oxide layer on top of the silicon insulates the wires from the substrate[1]. The oxidised side is polished. The thickness of the insulating silicon oxide layer is varied from 25 nm to 500 nm. A thick insulation layer has the disadvantage of bad heat conductivity. The heat conductance of silicon oxide is $\sim 1.5\,\mathrm{W/m{\cdot}K}$ (see Appendix D). Most used substrates have a 100 nm thick silicon oxide layer. These substrates have total insulation between the wire and the substrate and sufficient high heat conductivity.

While the size of an atom chip is $25 \times 30\,\mathrm{mm}^2$, the size of the original wafer is larger. Usually the fabrication starts with a 6 or 8 inch (150 – 200 mm) wafer. The substrate for an atom chip is cut out of one of these wafer. Before cutting, the polished surface of the wafer is protected with a hard resist. Shipley S1805[2] is dropped onto the surface. Redundant resist is removed by tilting the wafer. Spinning of such big substrates is not possible with the available equipment. To harden the resist, the coated wafer is baked at 100°C in an oven for about two hours. The back side is not protected, as it is neither polished, nor used for the atom chip. The hardness of the protection resist is verified by scratching it with a piece of plastic. After baking, the resulting protection layer is thick and strong enough to prevent

[1] MEMC Electronic Materials, Novara, Italy.
[2] Microposit® S1805 Photo Resist, Shipley Company, Marlboro, Massachusetts, USA.

scratches on the surface by slivers. These emerge during cutting, and can be squeezed into the resist.

For the further fabrication an additional edge around the atom chip area is needed. Therefore the wafer is cut into pieces of $32 \times 37\,\mathrm{mm}^2$. With a ruler and a diamond scratcher a straight groove is scratched through the protection layer into the surface of the silicon. To break the substrate at the scratched line, it is laid with the scratch on an straight edge and the overlapping part is pushed down softly. For example a microscope slide provides the edge.

In the beginning of this thesis the substrate was cut by a company[3]. Therefore the substrate was protected with resist and send to the company. They used a diamond saw for cutting. The edge of a sawed substrate is much smoother and more accurate. Advantages of the developed cutting of silicon is that it is much faster and cheaper. Both techniques produce dust. Particles break of the sample and some fall onto the resist which protected the surface against these.

5.2 Names of atom chips

Every sample cut for this thesis is catalogued and gets a name. Every sample has its own process data sheet, where every fabrication step of this sample is listed. Independently if it is going to be an atom chip or a dummy sample. The first letter of the name is a capital and tells about the wafer the sample origins from (in case of silicon). Table 5.2.1 shows the letters and the description of the wafer.

Wafer	size (inch)	SiO_2 layer thickness (nm)	doping
A	6	unknown	unknown
B	8	500, front and back	no
C	8	25	n–type
D	8	17.5, front and back	n–type
E	6	100	p–type

Table 5.2.1: The first letter of the name of a silicon substrate tells about the wafer it origins from. Not a lot was known about the first wafer. The n–type doping of the other wafer is presumably phosphor, the p–type doping is done with boron.

For example the atom chip B VIII_{Si}, Spiral, $5\,\mu$m is build on a silicon sample from wafer B. It has 500 nm SiO_2 layer on the top and on the back. The roman number VIII behind the B tells, that it is sample number 8 from this wafer while the $_{Si}$ indicates the substrate which is silicon in this case.

On the sample box additional information are mentioned. In this specific case the layout (spiral) and the thickness of the gold wires ($5\,\mu$m) on this atom chip.

Several wafer of type E are used. Therefore the first capital E is followed by a small letter which indicates the exact wafer of type E.

With these names the process data sheet of every sample fabricated during this thesis can be found in one of the two clean room binders called 'Atom Chips' and 'Atom Chips II'.

[3]Shamraz, Jerusalem, Israel.

5.3 Cleaning atom chips

The cut substrate is covered with protection resist which is extremely dirty. The dirt comes from cutting. To clean the sample it is put upside down into Acetone. The solvent solves the resist. The dirt, which is on an inside the resist, falls down to the bottom of the beaker. For bad contamination or hard resist it is recommended to heat the Acetone. Care is taken with the hot Acetone, as it evaporates fast and boiling retardation is common. Covering the beaker prevents fast evaporation and safety goggles protect the eyes of the fabricator in case of defervescence.

To clean very dirty samples, as after cutting, the Acetone is changed some times, dependent on the amount of dirt in the beaker. Two or three beakers are filled with acetone. The sample is put from one beaker into the next. Dirt on the back side of the substrate fells of, when the sample is spilled with acetone between the beakers. In the second or third bath acetone is spilled with pressure onto the surface of the sample to flush away particles. For hard contamination the solvent bath can be put into an ultrasonic bath. Samples with special size or samples, which have a small crack already are endangered, to break into pieces. Therefore the ultrasonic bath is only used if really necessary. For very dirty samples the surface is softly rubbed with a solvent resistent q–tip. This is especially useful for burned resist. A damage of previously fabricated wires by this technique was not observed.

A cleaning chain is a combination of beakers with acetone of increasing cleanness. The beakers are labelled to keep the clean beakers clean. During cleaning, the sample never dries, as acetone leaves residues behind, when it evaporates. The sample is moved fast from one beaker to the next or spilled with acetone in between. The cleaning chain ends with isopropanol. The sample is put directly from the acetone beaker into isopropanol. Isopropanol removes the acetone. It does not evaporate as fast as acetone. Removing the acetone takes about 30 seconds and can be seen by eye. Cords above the sample indicate that there is still acetone on the sample. When the acetone is removed, the sample is taken out of the isopropanol and it is blown away with pure nitrogen gas. Instead of isopropanol methanol can be used to replace the acetone. Methanol does not need to be blown away, as it evaporates without leaving residues.

Cleaning of the substrate or sample is a very important step during the fabrication process. A clean chip can not be manufactured, if it is not clean during the complete fabrication process. Any kind of contamination can destroy the chip by breaking a wire or causing shorts between the wires. At least the quality of the atom chip suffers when it is dirty. Cleaning does not harm the chip and should always be done, if contamination is possible. Every particle is remove immediately, as it can be irremovable after the next preparation step. Dedusting the chip with Nitrogen gas is done before any fabrication step, to remove particles from the surface. Particles are rare in a clean room, but they are still there.

The major source of contamination is the fabricator himself. The cleanroom is clean and the air is particle free. To prevent a sample from his own dirt, a fabricator never talks into the direction of his sample, not to spit on it. He also never moves anything above the sample. Particles tend to fall down from things onto the sample. This is essential especially for ungloved hands and the head of the fabricator, as they are the most dirty things in the cleanroom.

5.4 Optical lithography

A clean sample is a requirement for lithography of small features. Optical lithography is the basic process step to fabricate well defined structures on or into the surface of a substrate. It transfers the design from a mask into a resist pattern for further use.

5.4.1 Primer

For good adhesion of photo resist, a primer[4] is applied onto the surface. Therefore the sample is put onto a spinner and the liquid primer is dropped onto the surface, till it covers it completely. After 30 seconds the sample is spun for 40 seconds with 3000 rpm. After spinning, the sample is baked for 3 minutes on a 80°C hot plate. Before further preparation, the sample is cooled down to room temperature. The substrate is covered with primer once. Even when lithography is redone after cleaning or lift–off no new primer is added to the surface, as a thin layer of primer stays after these processes on the surface.

5.4.2 Photoresist

Lithography itself starts with spinning photosensitive resist onto the sample. As the resist is exposed by light the process is done in a yellow illuminated room[5], a yellow room. Yellow light does not expose the resist as its sensitivity is in the UV. The sample is put onto a spinner and covered with photosensitive image reversal resist[6] (IR, photo resist). Sometimes tall wires are favoured on atom chips. As the thickness of the resist will limit the height of the fabricated wires, several spinning methods were tried to get optimal thickness of the resist. The height of the resist depends on the spinning speed, the spinning time and the number of layers spun onto the substrate. The spinning process used before this thesis was started is described briefly in Appendix E.0.2.

To gain thick resist, spinning speed is reduced to the minimum revolutions per minute (rpm) of constant rotation of the spinner. The sample is spun with 470 rpm for 40 seconds. The height of the resulting resist also depends on the age of the resist. The older the resist, the thinner it is. Table 5.1 shows a general height dependence of image reversal photo resist on the spinning speed. This table is taken from Figure 5.1, which shows the measured image reversal resist height in dependance of the spinning speed.

spinning speed (rpm)	height of IR resist (nm)
5000	1000
3000	1500
1500	2000
1000	2500
500	4000

Table 5.1: The height of the IR resist depends mainly on the spinning speed. The slower the rotation speed, the thicker the resist.

[4]HMDS Microposit Primer, Rohm and Haas Electronic Materials, Coventry, UK.

[5]Wavelength 500 – 700 nm, maximum at 570 nm and peak at 545 nm; 'TL'D 36W /16; Philips; Amsterdam; The Netherlands.

[6]AZ 5214 E Image Reversal Photoresist, Clariant, Muttenz, Switzerland.

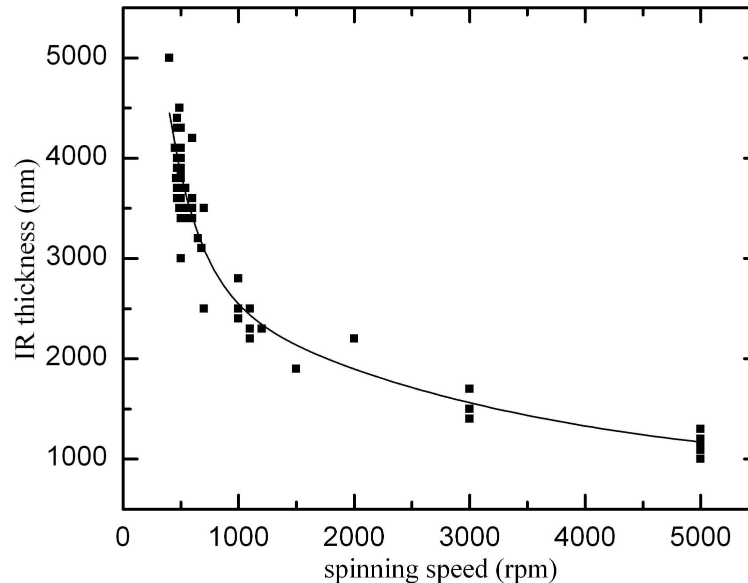

Figure 5.1: The height of the image reversal (IR) resist depends mainly on the spinning speed during fabrication. It is measured with a profilometer. Each point represents at least one fabricated sample. The measured values are fitted with an exponential decay.

After slow spinning, the sample is baked for 6 minutes on a 100°C hotplate and cooled down to room temperature. The resist is hard and can be exposed by light. Due to the slow spinning speed the resist builds bulges at the edges of the sample. These have to be removed, as the resolution and accuracy of the lithography will be reduced otherwise. Without removing the bulges, the mask does not have good contact with the covered sample in the mask aligner (see Figure 5.2). The bulges are removed with a q–tip soaked with acetone. Resist, which sticks on the back side of the sample is removed too, as this resist causes a tilt of the sample in the mask aligner. Care has to be taken with the fumes of the acetone. They also solve resist and can cause damage to it. To be able to remove the bulges and to have a sufficient area for lithography left during cutting, the size of the sample is chosen about 2 mm wider on each side than the atom chip will be in the experiment (see Section 5.1). A backed sample can be stored for a few days, before it is exposed.

5.4.3 Exposure

In a mask aligner[7] the resist on the sample is exposed by UV–light with a wavelength of 405 nm and 15 mW through a mask. The lithography mask covers parts of the resist with its chrome layout from the UV–light (for mask fabrication see Section 3.3). The sample lyes on a movable table below the mask. The sample is aligned to the mask by moving the sample table. Both, sample and mask can be seen through a microscope. With the sample in the desired position under the mask, the table is moved up, to push the sample at the mask. The exposure time of the resist with the UV–light is defined precisely by a timer.

In the highest resolution of the mask aligner microscope it is difficult to see the mask and the sample in focus at the same time. If magnification is turned back the focus area becomes larger and it is easier to align the sample under the mask. During exposure no gap between mask and resist is recommended, to avoid diffraction and loss of resolution. The

[7]Karl Suss MJB 3, Garching, Germany.

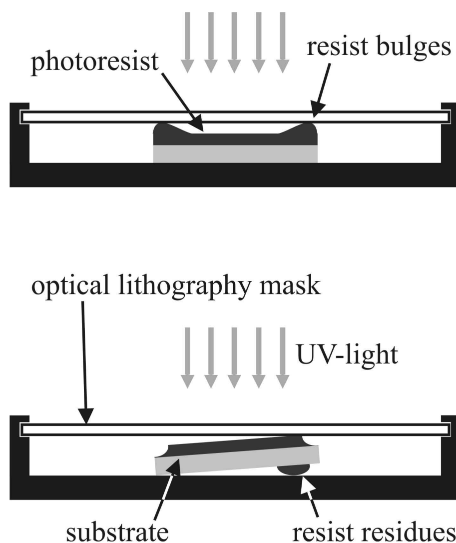

Figure 5.2: For high resolution optical lithography, the mask has to be in good contact with the exposed resist. top: The resist bulges at the edge of the sample prevent the mask to be in contact with the resist in the centre of the sample. bottom: The bulges at the edges are emoved, but resist residues below the sample tilt it in the mask aligner. The mask is not in good contact with the sample either. For good contact between resist on the sample and the lithography mask resist bulges and resist on the back of the substrate are removed before exposure.

sample is pushed as strong to the mask as possible, without breaking mask or sample. Use high pressure and vacuum chamber to gain best contact.

Wrong baking causes the sample to stick together with the mask. If this happens the sample can be removed from the mask carefully by using tweezers. Care is taken, not to damage the mask. If the sample is not removable with tweezers it is removed by rinsing sample and mask with acetone. The acetone solves the resist and the sample slides off the mask. After both techniques sample and mask are cleaned and the lithography process is redone. Damaging the mask is to be avoided in any case. A damaged mask is destroyed and has to be redone, which takes a lot of time and money.

The aligned sample is exposed for 0.9 seconds in the mask aligner by UV-light with a wavelength of 405 nm. At least 30 seconds after exposure the sample is laid untouched, before it is post baked with vacuum contact on a 120°C hotplate for 3 minutes. After cooling down flood exposure is done in the same mask aligner for 50 seconds. Flood exposure is exposure of the resist without a mask.

During the exposure the mask occludes parts of the resist with its chrome pattern. The resist is sensitive on the UV-light. Two kinds of photo resist are distinguished. Positive resist stays unsolvable by developer on the sample, as long as it is not exposed, while the exposed parts are removed by the developer. Negative resist behaves opposite. The exposed resist is resistant against the developer and the unexposed resist is removed. To prepare samples during this work, mainly negative image reversal resist is used. The design of the mask defines which kind of resist is required during fabrication. The mask has to fit negative or positive resist.

5.4.4 Development

Half a minute after flood exposure the resist is developed. As the thickness of the resist varies with spinning speed and age of the resist, development is done by eye. The sample is dipped into the developer[8] fast to assure equal development of all the resist. It is shaken inside the developer until it looks completely developed plus additional 15 seconds. Developing a sample with resist is like developing a photo. The pattern is visible, when the resist structure is ready. Total development time for this process is about one minute, depending on the height of the resist. Water is used as stop bath. The developer is washed of by the water in a beaker. After stopping the sample is dried from the water by blowing it away with N_2 gas.

The design of the mask is transferred into the resist on the sample. This is the last reversible step. The resist structure is checked under a microscope, as a defect in the structure will destroy the sample. In case of a defect in the resist structure, the sample is cleaned and used again. The lithography is redone as often as the resulting resist structure is not sufficiently good. A compromise in this step will directly affect the quality of the atom chip and this is the last opportunity to correct a failure or inaccuracy.

5.4.5 Undercut

Flood exposure causes the reversal process of the image reversal resist [Cla06]. Image reversal photo resist is a positive resist. If exposed, it builds a positive resist pattern of the layout on the mask. The reversal process with post bake and flood exposure turns the image reversal into a negative resist. All the resist, that would remain in a positive process is removed during development. This results in a negative wall profile of the resist, an undercut (see Figure 5.3). The name undercut describes the trapezium shape of the resist pattern. Its upper part is wider, than the bottom. This resist builds an undercut of about 0.6 μm when it is about 2 μm high.

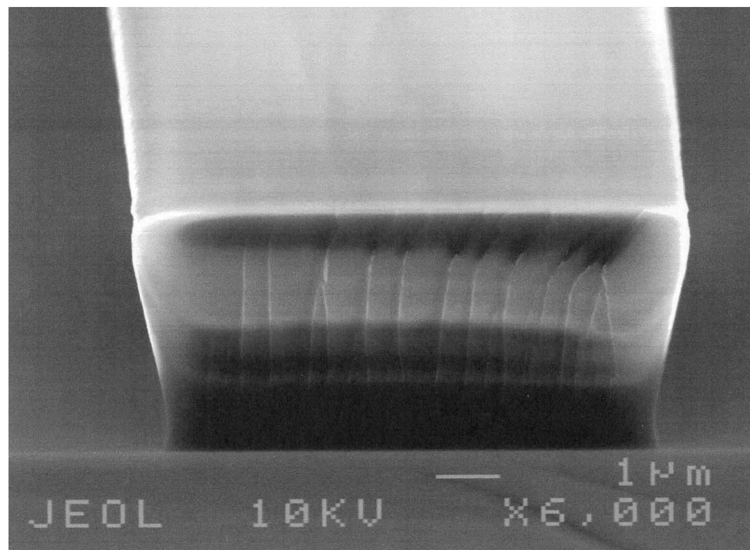

Figure 5.3: Resist with an undercut has a trapezium shape, while the narrow side is its base. In this particular case the resist is $\sim 2\,\mu$m high (sample in picture is tilted), and its undercut is $\sim 0.6\,\mu$m.

[8]AZ 726 MIF, Clariant, Wiesbaden, Germany.

The height of the resist limits the next fabrication step. It is measured with a profilometer[9]. A small needle scans a line on the surface of the sample and shows the profile of the resist pattern on a screen. After this the sample is put into an ozonator[10] for 7 minutes. In the ozonator resist is slowly removed by ozone, activated by UV–light. It is used to remove thin resist residues, which are left after development. In the next step metal is evaporated onto the resist patterned sample.

5.5 Evaporation

To build wires, metal is evaporated onto the surface of the sample with the resist pattern on it. Before evaporation the height of the resist is measured. In the evaporator the sample is mounted in a vacuum chamber (about 2×10^{-7} torr) above the required metal. The metal is heated until it evaporates. The metal is deposited everywhere in direct line to the heated metal, also on the sample with the resist pattern.

In a thermal evaporator the metal is stored in a crucible. This is heated by a current running through it. The crucible is made of wolfram (melting point $T_W = 3410°\text{C}$) and covered with ceramics, if the evaporated material reacts with it. The amount of current defines the temperature. It is dependent on the evaporated material and between 2 to 30 A. During one evaporation the temperature of the crucible changes with time, as metal evaporates. An e–gun evaporator heats material in a pot by shooting a continuous electron beam into the metal. The temperature is controlled by the intensity of the electron beam.

Both evaporators operate in vacuum, to enable the evaporating metal to reach the sample. The better the vacuum, the cleaner the evaporated film gets, as less foreign atoms from the surrounding gas are integrated.

A thermal evaporator[11] is mostly used during this thesis. Due to the system, up to five different materials can be used and the distance between crucible and sample is easy to adjust. Four of the crucibles are mounted on a rotation stage. The evaporation point of all of them is the same. This avoids different evaporation angels between different crucibles. This is especially important at a short distance between crucible and sample. A short distance between sample and crucible is needed to be able to evaporate enough metal for thick layers, without opening the evaporator during the evaporation to refill the evaporated metal. To have a defined short distance between crucible and sample a special sample holder was build. This sample holder reduces the distance by a factor of ~ 3.3 to 103 mm. Figure 5.4 shows a photo of the evaporator with the long sample holder. The calibration of this sample holder is displayed in Appendix B. This distance reduction not only avoids opening the evaporator to provide cleaner surfaces, also the evaporation speed is ~ 7 times higher. This safes a lot of time, as the evaporation still takes about an hour, and it also saves about 85% of metal, which is gold for most atom chips. During the time when evaporation is objectionable a shutter covers the sample. It is moved between crucible and the new sample position, as the long holder does not allow its use in the regular position. After evaporation the shutter is moved back to its normal position, as the evaporator is used by other people too. Evaporation may fail and destroy their samples, in case they do not pay attention and do not recognize the different position of the shutter.

The metal used for wires is gold[12]. To assure good adhesion between the gold and the

[9] Dektak 6M Bench-Top Stylus Profiler, Veeco Instruments Inc., Woodbury, USA or an AS 250, Alpha–step; Tencor Instruments.

[10] UV & ozone dry stripper, UV-1; Samco; Kyoto; Japan.

[11] Edwards Auto 306, BOC EDWARDS, Crawley, UK.

[12] Gold quality 99.999%, CERAC incorporated, Milwaukee, USA.

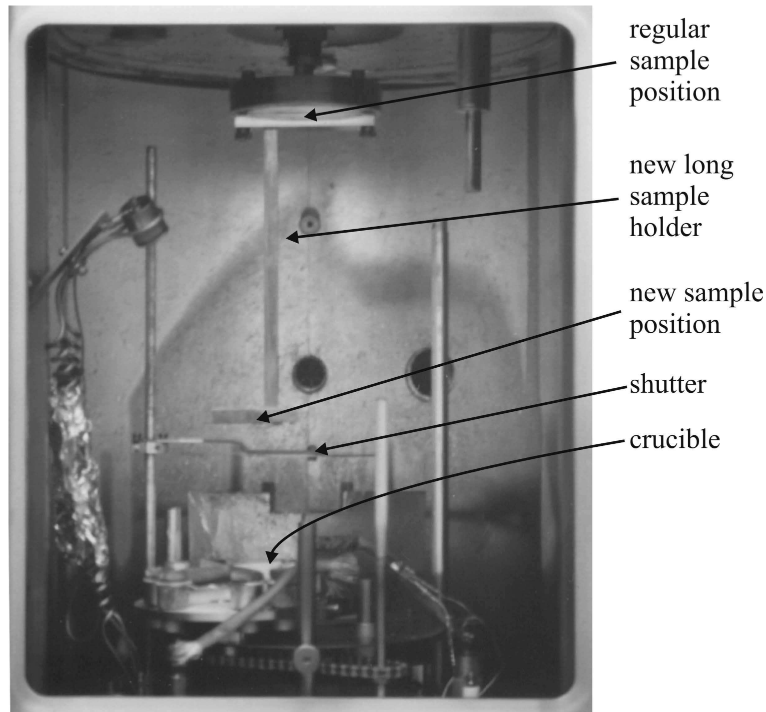

Figure 5.4: The long sample holder allows to mount the sample in the evaporator 103 mm above the crucible. The speed of evaporation in this position is about 7 times faster than in the regular position. The shutter is moved down, so it can be placed between sample and crucible.

substrate a thin titanium[13] layer of about 10 to 30 nm is evaporated. Titanium is sticky and holds on SiO_2, while gold does not. Due to its stickiness the titanium sticks on all the walls of the evaporator after heating. The rest gas inside the evaporator is partly caught by the titanium and the vacuum gets better. During this time the sample is covered by the shutter. The titan gettering is used in titanium sublimation pumps and ion pumps, which are also used in the experiments of the fabricated atom chips. The evaporation speed of titanium is 0.05 nm/ second using the long sample holder. Gold is evaporated onto the titanium layer, where it sticks. The first 5 nm of gold are evaporated with a speed of 0.05 nm/ seconds, before the speed is increased to 0.4 nm/ second. The last 5 nm are evaporated slowly again. This procedure produces good quality gold edges and surfaces. Due to the height of the wires, which is required for some atom chips, the other two crucibles of the evaporator are filled with gold, too.

The short distance between the crucible and the sample causes the sample to heat up during the evaporation process by radiation and the hot material deposited on it. Therefore a cool down safety stop of 10 minutes is done every 1000 nm of evaporated metal. During this time part of the heat is transferred through the solid copper holder to the water cooled stage. Without safety stop the resist pattern on the substrate can burn. Overheated resist can deform and is difficult to solve. This causes a difficult lift–off, which can harm the sample. Every safety stop starts end ends with 5 nm of slow deposition.

An unequal deposition of metal on the sample is caused by the short distance between crucible and sample using the long sample holder. The centre of the sample is closest to the crucible, the edges are further away. A slight decrease of the deposited material is measurable

[13]Titanium quality 99.995%, CERAC incorporated, Milwaukee, USA.

for thick evaporations. On a 3 μm thick metal film a decrease of about 100 nm was observed over 1 cm . This is not problematic, as the wires on the edge are wider than in the middle of the sample (see Chapter 3). The maximum height of evaporated metal is up to 5 μm on atom chip B $VIII_{Si}$. This has been a mistake, as the resist has only been 4.2 μm high. Luckily lift–off worked and this atom chip gave good results in the experiment.

5.6 Lift–off

Lift–off removes the resist pattern and the metal on top of it from the substrate, while the metal on the surface remains. The evaporated sample is taken out of the evaporator and put upside down into acetone. Lift–off is similar to the cleaning process. To protect the surface a holder is build. The sample fits into it, so the sample is hold upside down in the acetone without touching the surface. If needed it can stay in the acetone for some hours.

The resist pattern between sample surface and evaporated metal is solved by acetone. The metal evaporated on the resist falls of from the sample. The solvent reaches the resist through a gap between the two evaporated metal structures. This gap appears due to the undercut of the resist and the amount of evaporated metal (see Chapter 5.4 and Chapter5.5). The full atom chip preparation process is illustrated in Figure 5.5.

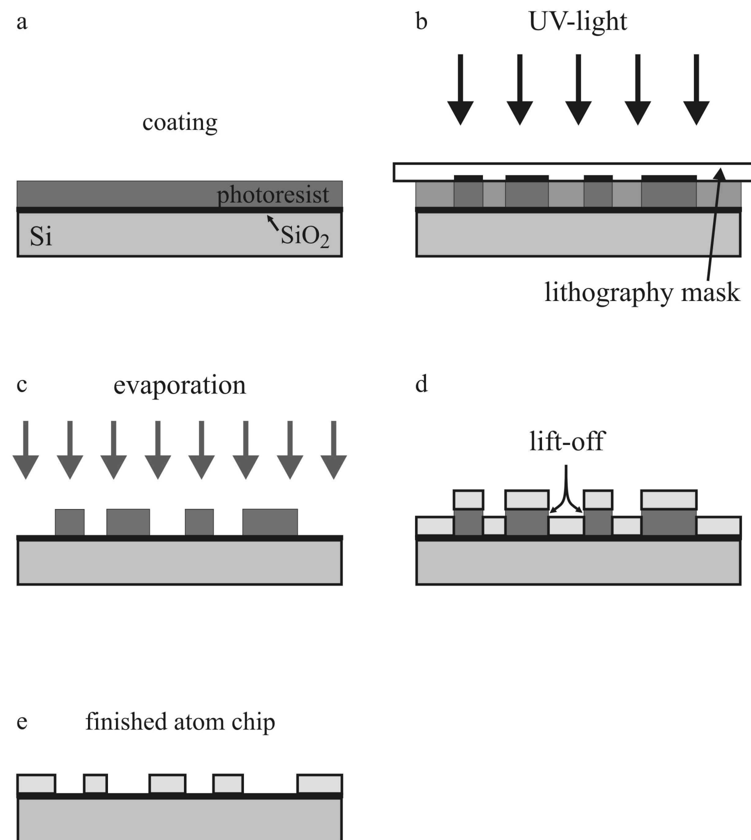

Figure 5.5: The fabrication process is illustrated in this figure. a: The Si substrate with its SiO_2 cover layer is spin coated with photoresist. b: The resist is exposed through a lithography mask. c: After development the sample with its resist pattern is evaporated with titanium and gold. d: Lift–off removes the resist and the metal on top of it. e: The atom chip is finished and ready to use.

Fabrication failures may cause problems during lift–off. The most common are mentioned briefly.

burned resist: The resist got to hot either during baking or during the evaporation. The resist is difficult to solve.

undercut closed: The metal film on top of the resist is connected with the metal film on top of the substrate. Too much metal has been evaporated. The gap is closed and the solvent does not reach the resist, to solve it. Or the two metal films stick together even when the resist is solved.

evaporation angle to big: The undercut is closed by the angle of evaporation. The two metal films are connected on one side, like in the case of a closed undercut. With rotating samples during evaporation the undercut can be closed on all sides.

Another problem appears in lift–off of large areas (larger than half a square cm). Here it takes a lot of time for the solvent to crawl below the metal film to the centre of it to solve all the resist. To succeed difficult lift–off the same techniques like for cleaning are used. Heating the acetone for long time, ultrasonic and using q–tips force lift–off. Pushing a jet of acetone onto the sample only helps a bit. The thick metal film does not break. For thick evaporated metal, tweezers are helpful to get rid of metal structures, which are partly loose. Pulling slowly at the disconnected end of thick metal layer removes all the metal if done carefully. This is useful to remove the metal on the edge of the sample. The metal on the edge is difficult to lift–off. Before evaporation the resist bulges at the edge are removed. In this area, the evaporated metal is partly connected to the surface. The acetone solves the resist from one side only, as the other side is closed. Pulling at the disconnected metal breaks the film. The metal on the surface stays, the rest is removed with tweezers and cautious q–tip rubbing.

Lift–off is difficult, if too much metal is evaporated. The gap between evaporated metal on the surface of the substrate and the metal on the resist closes, the more metal is evaporated. To solve the resist the acetone has to penetrate through this gap. If the gap is closed, the metal layer on the surface connects to the metal layer on the resist. Dependent on the strength of the bond between the two metal structures lift–off is not successful or the result is insufficient. In bad lift–off the edges suffer, parts of the metal on the surface is removed too or residues of the top metal stick to the ground metal.

If metal from the surface of the sample is removed during lift–off either the adhesion layer was not good, or the development of the resist has not been complete. Metal with good adhesion to the surface is connected strongly.

Small separated areas without metal are to be avoided in the design. During lift–off, these small metal pieces on top of the small resist patterns can fall onto the surface of the sample and connect to it. This problem appeared several times with small pieces and has never been a problem with larger parts. Small metal pieces stick very good in gaps of the same size in the metal film. This combination is avoided too. A short recipe of the fabrication process of regular atom chips is shown in Appendix C.1.

5.7 Precise cutting of atom chips

After lift–off, the atom chip is ready to be used. But it still has the fabrication edge around it. The preparation for cutting is as described in Chapter 5.1. This final cutting has to be accurate compared to the previous cutting. The protection layer on the almost finished atom chip is very important. It hast to be thick and strong enough, as the surface is much more

delicate now. A lot of work will be lost, if the finished sample suffers only from cutting. As the sample is smaller it is spin coated. Image reversal resist is spun onto it for 40 seconds with 3000 rpm. Baking time is 2 to 3 minutes on a 100°C hotplate. Alternatively Shipley S1805 resist is used with a spinning speed of less than 2000 rpm to avoid a too thin layer.

Precise cutting is done with a diamond scratcher mounted above a moving stage, which allows straight scratches under a microscope. This mounting enables to scratch the sample with an accuracy of a few 10 th of microns. Therefore breaking with an accuracy of less than 100 μm is possible. For precise cuttings three microscope slides are used. The scratched sample is clamped between two of the slides in a way, that the edge of the glass slides is at the scratch on the sample. The atom chip is clamped between the two slides, while the fabrication edge sticks out of them. The edge is broken off at the scratch by pushing it down. This is illustrated in Figure 5.6. To press with a force equal all over the length of the edge, the third slide is used. It is laid onto the overhang and pushed down, while the other two slide fix the atom chip behind the scratch. A broken edge is rough compared to an edge which has been sawed. It is possible to break of particles from the edge of the broken atom chip, if it is not handled with care. It is also more likely to lose a sample because it slides of the tweezers, when the edge is rough from breaking. Broken samples are also more likely to die in the ultrasonic bath. They already have small cracks at the edge, which can extrude through all the sample in an ultrasonic bath. Still breaking is used to cut regular atom chips, as it is much cheaper and faster than sending the atom chip to be sawed. After cutting the sample to the right size it is cleaned. This removes the protection resist with the residues inside it. The atom chip is finished.

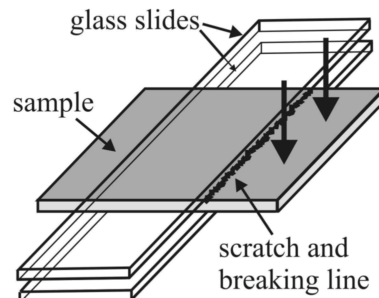

Figure 5.6: For precise cutting, a scratch is mad with a diamond into the surface of the atom chip. The sample will break in this line, if it is clamped between two microscope slides in the displayed way. The scratch is at the edge of the two slides. The overhang is broken off by equal force to it. To push the full length of the overhang homogeneously, a third slide (not displayed) is laid on it. This is also helpful, if the overhang is short.

Before the breaking technique has been developed, atom chips were cut by sawing. This was done by a company. As sawing has advantages compared to breaking, the last atom chips were cut by sawing again. Mainly, because breaking is not that save, and a unique atom chip was lost by breaking. The last cutting was done by Xiyuan Liu in the group of Prof. K.-H. Brenner in Mannheim. In Mannheim sawing is done with a circular diamond saw[14]. The sample is aligned with a microscope and sawed with an accuracy of about 20 μm. During sawing the sample is covered by protection resist to prevent contamination by the sawdust, which is spilled over the sample together with cooling water. The width of the saw blade is 200 μm. The edge of a sawed atom chip is smooth and perpendicular to the surface.

[14]DAD321 automatic dicing saw, Disco Corporation, Tokyo, Japan.

This makes the sample easier to grip with tweezers from the top and particles do not break of easily.

This fabrication process of atom chips has been developed during this thesis. In the end the loss rate during this process went down to about 5% including the cutting by hand.

5.8 Material variations in processing

To obtain the best atom chip, different materials were used for fabrication and compared afterwards. In the first part of this section diverse substrates are introduced, in the second part evaporation techniques for different materials are discussed.

5.8.1 Substrates

The substrate of an atom chip has to fulfill several requirements. It has to be strong enough and manufacturable. More important are smoothness of the surface, insulation, transparency, heat conductivity and heat capacity. Values are given in Appendix D.

Gallium arsenide – GaAs

Before this thesis was started, atom chips were fabricated on GaAs. The biggest problem of GaAs is its fragility. It cleaves under small pressure. The first mountings of atom chips were mechanically contacted by electric clamps, which were able to destroy the chip.

In this work, test atom chips were fabricated on GaAs. They do not have as good thermal properties as atom chips with Si substrates (see Table D.1 in Appendix D). They are not used in experiments, even if the new chip mounting does not use contact clamps but wire bonds.

In the newest atom chip design, GaAs is added as patterned semiconductor (not as substrate) onto an atom chip.

Care is to be take because of the toxic and carcinogenic effect of GaAs.

Sapphire

Sapphire (Al_2O_3) has a good heat conductivity as an insulator and it is transparent. Two atom chips were build on sapphire during this work. These are one test atom chip and one spiral design atom chip. The spiral atom chip was used in the ^{7}Li experiment and gave many results [Luo04, Bru05]. The thermal properties of Sapphire are not as good as the of Si (see Table D.1 in Appendix D). Sapphire is hard (9 on Mohs Scale [Oli92]), which makes it difficult to fabricate. Its transparency does not affect the lithography parameters. Imaging or laser cooling through the sapphire atom chip substrate could be done. Compared to Si sapphire is expensive and its surface is rough compared to the one of Si.

Silicon – Si

Mainly silicon substrates are used to fabricate atom chips in this thesis. Due to its huge circulation in commercial chip fabrication Si is very well known, easy to purchase with a defined heterostructure, easy to handle, clean and smooth.

Si wafer polished on one side with a roughness of $\sim 1.4\,\mu$m TTV (total thickness variation) were bought[15]. For having high heat conductivity the substrate is highly doped. The insulation is ensured by a SiO_2 layer on top of the doped Si. The thickness of the SiO_2 layer

[15]For substrate E: 150MM/po/100HM/oxide, MEMC Electronic Materials, St.Peters, USA.

is varied for different purposes. SiO_2 layers of 17.5, 25, 100 and 500 nm thickness are used. The 17.5 nm thick layer is to thin and could not provide the needed insulation. The 25 nm thick layer insulates the substrate and the wires. The 500 nm thick layer was chosen to be able to etch a few 100 nm into the surface. Mostly wafer with a 100 nm thick insulation layer are used. The data sheet of these wafer is printed in Table 5.8.1.1. The wafer are p^+ doped with boron and their crystal orientation is 1-0-0. The doping is approximately $5 \cdot 10^{15}$ (atoms of boron)/cm^3. The specific resistance is ~ 3 Ohm·cm and the relative fraction of boron is $\sim 10^{-7}$. Seven of these 6" wafer were used for atom chip fabrication during this thesis.

parameter	average	standard deviation
warp (μm)	9.126	4.254
TTV (μm)	1.356	0.3
polished thickness (μm)	676.975	2.11
STIR on all sites 1 (μm)	0.309	0.092
slice off orientation	-0.007	0.022
Resistivity (mOhm×cm)	17.133	0.352
primary flat length (mm)	57.6	0
LPD >= 0.16 micron (#/slice)	6.6	5.452
Oxygen (new-ppma)	15.79	0
diameter (mm)	150	0

Table 5.8.1.1: The parameters of the mainly used Si wafer for atom chips are listed in this table. The dopant is boron, p^+ type and the orientation is 1-0-0. TTV – total thickness variation; LPD – light point defects; PPMA – parts per million atomic.

5.8.2 Different evaporated materials

On some atom chips, other materials than gold are needed. The preparation techniques for these atom chips are discussed in the following chapter. Here the used materials and their evaporation properties are explained.

Grain size

To achieve better fabrication qualities, different wire and mirror materials have been tested. Gold and some other metals build grains, when they are evaporated. These are columns, standing in contact next to each other. From top, an evaporated gold surface looks grainy due to the columns. Figure 5.7 shows, that the grains grow in columns. The grain size is the average diameter of the columns. The grain size of a metal depends on the used material and the temperature of the sample during the evaporation. Tested metals during this thesis are gold (Au), palladium gold (PdAu) and aluminium (Al). Other groups use silver [Du04] or copper [Val04] on their atom chips. Atom traps from silver and copper wires are used in this group only by the solid copper structure below the atom chip (see Section 4.3).

The quality of the fabrication is important for precise measurements. A surface with high reflection allows to trap more atoms due to the higher efficiency of the laser cooling. Also imaging is more efficient with less scattering, so the resolution gets higher with increasing

smoothness of the surface. Most important, the current density inside a wire depends on the homogeneity of the wire. Changes in the current density modulate the trapping potential (see Section 2.7). This will affect the atoms, once they are cold enough to feel the modulations [Wil05b, Krü05, Wil06a]. Defects in the wire shape are avoided by careful fabrication. The grain size is controlled during fabrication too.

Micro fabrication of Au, PdAu and Al during this thesis is done in the Weizmann Institute of Science. The smallest grain size is achieved with palladium gold. It builds grains of about 25 nm at room temperature, while the grain size of gold is about 50 nm. Aluminium evaporated at room temperature builds an inhomogeneous surface. The grain size of all three materials is reduced by a factor of two by cooling the sample during the evaporation process with liquid nitrogen to 77 K. The grain size is measured with a SEM or an AFM (scanning electron microscope and atomic force microscope). The measured grain size values are listed in Table 5.8.2. Cooling the sample with liquid nitrogen also has the advantage of better vacuum during evaporation. Some of the rest gas inside the vacuum chamber of the evaporator freezes out at the cooled rod of the sample holder. As the sample itself is the hottest piece of the cooled components the rest gas does not freeze out on the surface of the sample. By heating the sample, the grain size can be increased. Measurements in the group of Prof. Ron Folman from the Ben–Gurion University in Beer–Sheva, Israel were done with heated samples during gold evaporation. The achieved grain sizes are: ~ 50 nm – 30°C; ~ 80 nm – 100°C; ~ 140 nm – 200°C and ~ 160 nm – 300°C.

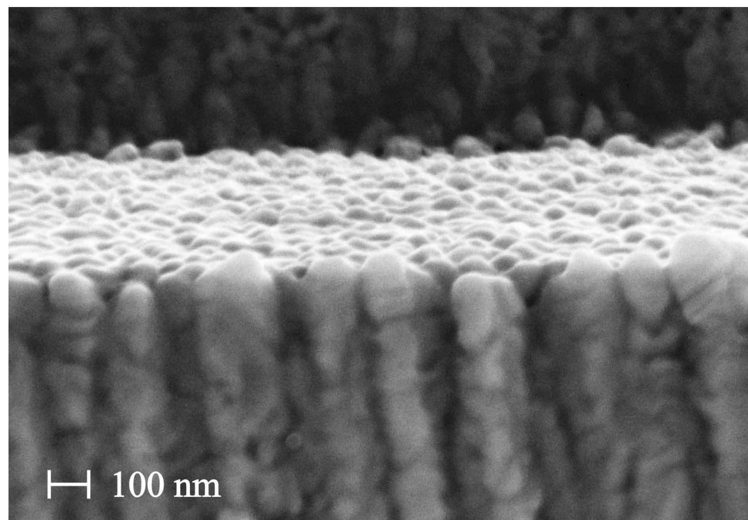

Figure 5.7: Grains of deposited gold are growing in columns. This SEM picture shows a wire of atom chip B VII Si. The picture is take under an angle of 80° and perpendicular to the wire, which leads from left to right. The top of the wire and its edge are visible. This picture was taken in the department of applied physical chemistry of the University of Heidelberg together with Alexander Küller from the group of Prof. M. Gunze.

metal	grain size (nm) (room temperature)	grain size (nm) (liquid nitrogen temperature)
PdAu	25	15
gold	50	25
aluminium	70 – 90	50

Table 5.8.2: The grain size of evaporated metals depends on the temperature of the sample during evaporation. The grain size is about half as big, if the sample is cooled with liquid nitrogen compared to grains which are evaporated at room temperature. The size of the grains is taken from SEM and AFM images.

Evaporation speed

The evaporation speed of other materials than titanium is mostly 0.4 nm/sec (calibrated display for the standard holder). The same evaporation speed is used with the long sample holder, where the effective speed is seven times higher than displayed. The upper limit of the evaporation speed is 0.4 nm/sec in the used evaporator. Higher currents may cause the crucible to burn. This destroys the sample inside the evaporator. A dependance of the grain size from the evaporation speed has not been observed. To gain a good surface the speed of evaporation is low (about 0.05 nm/sec) for the first and last 5 nm of an evaporation step. This is also done if the evaporation is stopped after 1000 nm to cool down the sample.

The speed of evaporation is measured with an oscillating crystal inside the vacuum chamber. During evaporation metal is also evaporated onto this crystal, which causes a change of its oscillation frequency. To calculate the correct evaporation speed, the crystal is calibrated for all used materials and is adjusted before each evaporation.

Most materials melt, before they start to evaporate. At least, the crucible radiates when it becomes hot. Both can be seen through a window in the vacuum chamber. Dark glasses are used to protect the eyes.

Titanium – Ti

Gold is used as standard metal to construct wires on atom chips. As adhesion layer titanium is used. Titanium melts at $T_{Ti} = 1660°\mathrm{C}$ and evaporates right after melting. The current needs to be turned down a little just after the Ti melts. During evaporation Ti is vapour deposited at the walls of the evaporator. Here it getters some of the rest gas inside the chamber. As long as the pressure inside the evaporation chamber drops due to the Ti pumping, the sample is covered by a shutter. In case of stable pressure, the shutter is opened and Ti is evaporated onto the sample with a speed of 0.05 nm/sec. The thickness of the Ti adhesion layer is 10 to 30 nm. Other materials like nickel or chrome are not used as adhesion layer, as they are magnetic and may affect the results of the experiment.

Gold – Au

On top of the adhesion layer a different metal is evaporated. For the standard atom chip this is gold. The adhesion layer is needed, as gold has bad adhesion on SiO_2. Au melts at a temperature of $T_{Au} = 1064°\mathrm{C}$. The evaporation temperature of Au is higher and the speed

of evaporation 0.4 nm/sec. It is limited by the crucible inside the evaporator, which burns at even higher currents. Crucibles for gold can be used several times. Than the remaining gold in the crucible is not wasted. With the long sample holder (see Appendix: B) the evaporation speed is also 0.4 nm/sec. In e–gun evaporators spitting of gold has to be avoided.

Each crucible can be filled with up to five pellets of gold of about 0.4 g. One pellet results in an $\sim$ 50 nm thick Au film on the surface of the sample for the standard holder. With the long sample holder each pellet results in $\sim$ 350 nm. A maximal amount of evaporated metal could not be observed. Up to 5 μm the fabrication went straight forward. All three crucibles (one is needed for the Ti adhesion layer) had to be filled with five pellets of pure 99.999% gold for this atom chip.

The grain size of evaporated gold is about 50 nm. It is reduced to about 25 nm by cooling the sample during evaporation with liquid nitrogen. Figure 5.8 illustrates the change of the grain size. An advantage of evaporated gold is its smooth surface. Figure 5.9 shows an AFM picture of a regular $1 \times 1\,\mu\text{m}^2$ gold area. The roughness is $\sim$ 15 nm.

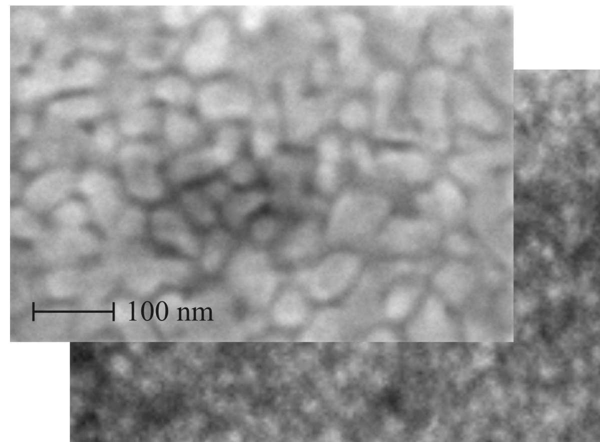

Figure 5.8: These SEM pictures show the grain size of gold evaporated at room temperature (top), and evaporated at 77 K in the picture below. The grain size of regular evaporated gold is about 50 nm (top), and about 25 nm for cooled evaporation (bottom). For both pictures the scale is the same.

Palladium Gold – PdAu

Palladium gold builds smaller grains than pure gold. The grain size is illustrated in Figure 5.10. PdAu has bad adhesion to many materials. Due to the bad adhesion, PdAu peels of the substrate once the evaporated film reaches a certain height. For used substrate (Si with SiO_2 layer) and the used PdAu (40% palladium and 60% gold) the maximal amount of evaporated metal is about 1 μm with a Ti adhesion layer. The melting point of Pd 25/ Au 75 is $T_{PdAu} = 1410°\text{C}$.

Silicon dioxide – SiO_2

SiO_2 is used as cover layer above the deposited metal. Before SiO_2 melts, it starts evaporating. Its melting temperature is $T_{SiO_2} = 1723°\text{C}$. The thickness monitor is observed to realize when the evaporation starts.

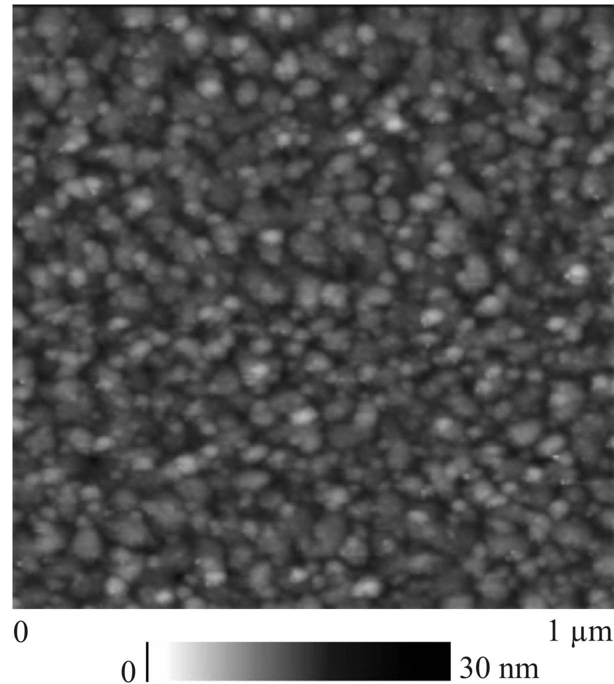

Figure 5.9: This AFM image of a regular deposited gold surface illustrates the smoothness of the gold surface. The roughness is in the order of 15 nm over huge areas. The height information is coloure coded.

Nickel – Ni

To evaporate Ni, a higher current than for the other materials is needed. Therefore it has special high current holders for the crucible in the evaporator. As the used current is about a magnitude higher than the one for other materials, it has to be handled with even more care. Ni melts at $T_{Ni} = 1453°C$. As soon as the Ni melts it starts evaporating. In the moment the Ni melts the current is turned down a bit.

The high current crucible is located in a different place than the other crucibles. This leads to a different evaporation angle and it also has a closer distance to the sample inside the evaporator. Because of the special position, the long sample holder is not used for Ni vapour deposition.

On atom chips nickel is used for ohmic contacts on semiconducting samples only. Thick layers are not required and the long sample holder is not needed. Nickel is magnetic. Therefor it is used far away from the trapped atoms, so it does not disturb the measurement.

Germanium – Ge

Like nickel, germanium is needed for ohmic contacts on semiconductors. Germanium melts at $T_{Ge} = 937°C$ long time before it starts evaporating. Melted germanium strongly wets the crucible. The Ge reacts with the wolfram crucible if it leaves the ceramic covered part. The crucible will burn, which destroys the sample. The area of crucible, which the Ge wets is tuned by the current and the amount of material.

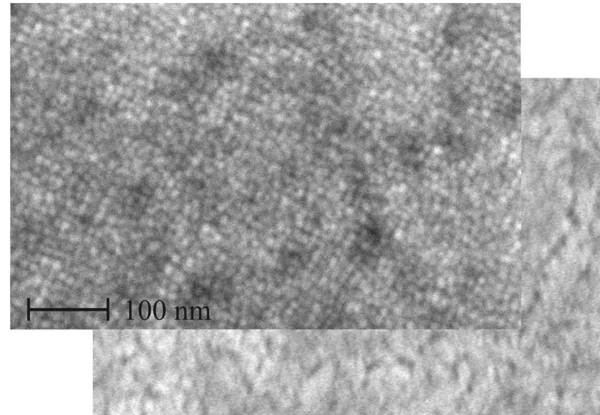

Figure 5.10: The grain size of PdAu deposited at room temperature is about 25 nm. The figure below shows PdAu deposited at 77 K. Here it is difficult to see grains at all. Their size is about 15 nm and it looks like a smooth surface with small cracks.

Aluminium – Al

Aluminium evaporates like gold. It melts at $T_{Al} = 660°C$ and evaporates immediately. The current is turned down a little, the moment the Al melts. Care is to be taken at the end, when only a little bit of Al is left in the crucible. The Al ends suddenly, not slowly compared to gold. Two pellets of Al are enough to evaporate up to 50 nm, three pellets last for 80 nm. Adding four pellets into one crucible is too much. Either the Al jumps out of the crucible when it melts, or it touches the wolfram below the ceramics, which burns when it comes in contact with the Al. For thick evaporations of Al more than one crucible is needed.

Chapter 6

Preparation of special atom chips

In the previous chapter, the fabrication of regular atom chips was described. These atom chips do not fulfill all requirements needed for successful state of the art experiments. Additional fabrication techniques are essential to manufacture suitable atom chips. These techniques are described in this chapter.

First atom chips with thin wires and atom chips with a protection layer on top of their surface are described. Than the fabrication of double and multi layer atom chips is explained, before submicron e–beam patterned and semiconducting atom chip fabrication is shown. Finally an atom chip which is supplementary FIB patterned is mentioned.

The preparation of these special atom chips bases on the fabrication process of regular atom chips, described in Chapter 5. The combination of all the special procedures is possible and some have been combined in this thesis.

The *dw-2000* CAD layouts of the most common atom chips are illustrated in Appendix C.

6.1 Atom chips with thin wire grids

To build steep magnetic potentials, thin wires are required (see Section 2.4.1). The resolution of the mask aligner is given by the wavelength of the UV–light during exposure. This lithography resolution limit is not reachable with the process, described in Chapter 5, as it is optimised for high resist structures. To achieve narrow features the parameters of the standard lithography process are tuned. Atom chips with 1 μm wide wires and a gap of 1 μm between them over a distance of 2 mm are fabricated. The grid with a period of five times the wavelength of the light causes problems, as well as the aspect ration of 2000. This section explains the parameters used to fabricate these structures.

6.1.1 Fabrication of wire grids with a period of 2 μm

The substrate is broken to the desired size and cleaned like described in Section 5.1. For adhesion, a Primer is spun onto the substrate with 3000 rpm for 40 seconds. Baking time is 3 minutes on a 80°C hotplate. After cooling down, the sample is spin coated with image reversal photoresist. Spinning speed is 5000 rpm for 40 seconds. The baking time is 45 seconds on a 100°C hotplate. The bulges at the edges and the resist residues on the back side of the sample are removed with a q–tip dipped in acetone. For this high resolution lithography, the sample has to lie flat in the mask aligner and has to have good contact to the mask. Exposure time is 2.6 seconds with 405 nm UV-light of 15 mW. The post bake time is 45 seconds on a 120°C hotplate with vacuum contact. After cooling down, the resist is flood exposed for 1.3 minutes and is developed in AZ 726 MIF for 25 seconds. The development is stopped by

water, which is blown from the sample with N_2 gas. After development the sample is put for 7 minutes into the ozonator, where resist residues are removed.

The exposure time and the development time are changing slightly due to the daily conditions of the resist and the weather. The age of the resist and mainly the humidity influence this process. For sensitive samples the parameters are checked before lithography with dummy samples. The height of the fast spinned resist is above $1\,\mu$m. This limits the maximal height of the evaporated metal to $1\,\mu$m. Lift–off is done in the standard way. Figure 6.1 shows a wire grid with a period of $2\,\mu$m fabricated in the described way. In Appendix C.2 the fabrication process for the narrow wire grid atom chip is listed.

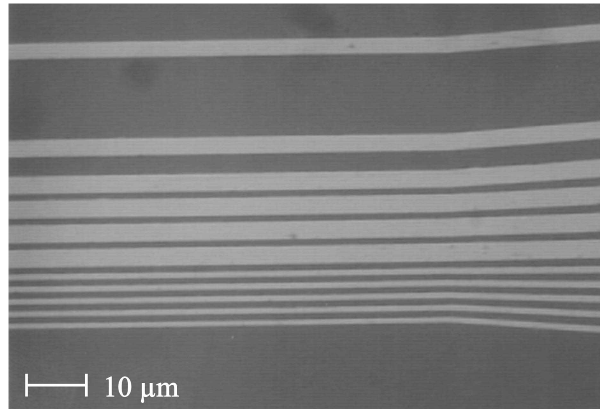

Figure 6.1: This photo shows a photo lithographically fabricated grid of $1\,\mu$m wide wires, separated by a gap of $1\,\mu$m. Above the the narrow wires $3\,\mu$m wide wires are fabricated, also separated by a $1\,\mu$m wide gap. The length of these wires is 2 mm to the left. On the right side the wires fan out and expand.

6.2 Coated atom chips

The surface of an atom chip is crucial for the experiment. As it is used as a mirror, it has to be as smooth and reflective as possible. Irregularities cause scattering light, which interferes with the cooling and the imaging laser beams. Particles on the atom chip can also cause shorts between wires.

During an experiment atoms are evaporated into the vacuum chamber and partly caught close to the surface of the atom chip (see Chapter 2). Some of the atoms collide into the surface and stick to it. To avoid problems with the surface an atom chip can be covered with an insulator. The insulator also avoids chemical reactions between the metal and particles or atoms.

Diamond, Si_3N_4 and SiO_2 are used as insulator [May93, Ash94]. In this thesis Si_3N_4 and mainly SiO_2 are used as insulation layer for some atom chips. After preparation of the regular atom chip (see Chapter 5) a SiO_2 layer is deposited onto the atom chip. The atom chip is mounted on the holder of the evaporator. Outer parts of the atom chip are covered with aluminium foil, to prevent the contact pads from evaporation. The pads remain uncovered, as they will be contacted electrically, which would be difficult with an insulation layer on top of them. Contamination of the unprotected pads is not critical, as the pads are far away from the physics region, where a clean surface is essential. Shorts caused by atoms deposited in this region are unlikely, as the gaps between the metal patterns at the edge are ten times wider ($\sim 100\,\mu$m) than in the centre of the atom chip and atoms are not trapped close to the

pads. This leads to much less contamination of the surface. For coatings of precise regions lithography and lift–off is possible. During this thesis there was no need for this.

Figure 6.2 shows a coated atom chip. Atom chip $E_f V_{Si}$ is currently used in the combined ^{87}Rubidium/ ^{6}Lithium experiment. On top of the 2.8 μm gold structures a 50 nm thick SiO_2 layer has been evaporated.

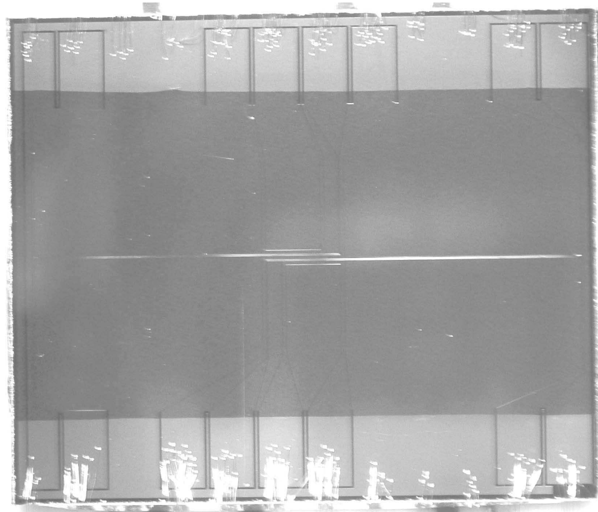

Figure 6.2: Photo of atom chip $E_f V_{Si}$. This atom chip is partly coated with SiO_2. The upper and lower parts, where the contact pads are, are not covered. The darker color in the middle of the atom chip is protected by SiO_2. This photo was taken imminent before the mounting was placed inside the UHV chamber. Bond wires are visible on the contact pads.

Coating atom chips with an insulation layer is required, if the surface reacts with something during use of the atom chip. The SiO_2 coating protects the surface from contaminations. The reflectivity is reduced slightly ($\sim 5\%$), which is negligible compared to the losses of the laser light by the windows of the UHV chamber.

6.2.1 Surface contamination

In the Li/ Rb experiment a layer appeared on top of the surface of an atom chip. The surface changed its colour and the reflectivity for the laser beams went down to 20%. This atom chip has been researched by Marcus Lehto from the Ångström Laboratory of the Uppsala University, Sweden. He found a 200 nm thick titanium layer with some rubidium on top of the gold and 20 nm of Ti between the gold and the surface. The second layer is the adhesion layer, evaporated during the fabrication process. The system is not able to detect Lithium. The titanium might come from the titan getter pump or from the adhesion layer between substrate and gold. The direct axis from the pump to the atom chip was blocked during the experiment. The titanium adhesion layer does not contain enough material for this layer. In this group this phenomena also has never been observed before with the same adhesion layers. And titanium was found between the wires too, where no titan was evaporated during fabrication.

The destroyed atom chip was replaced by the partly coated atom chip $E_f V_{Si}$. The uncovered edges of this atom chip again changed their colour, and reflectivity, but the SiO_2 covered centre stayed as fabricated and has been in use for a few month already.

6.3 Double–layer atom chips

For some experiments, high currents have to be pushed through wires on the atom chip. To minimize the heat appearing in these wires, the wire has to be as voluminous as possible. The easiest way is to enlarge the width of the wire. This leads to a larger amount of current carrying metal and a larger heat contact to the surface. But the width of a wire limits the minimal height of the trapped atoms above the surface. Therefore and for the steepness of the trap the cross section of a wire is important (see Section 2.5).

The width of a wire is given by the experiment, which should be done with this wire. It is designed and written to the mask. The height of a wire is limited in fabrication by the height of the resist pattern during evaporation. A quadratic cross section of the wire would be the best. To be able to push higher currents through wires, a technique was developed to enlarge the cross section of single wires above the limit given by the lithography resist.

This technique for double–layer atom chips bases on a standard lithography process as described in Chapter 5. On top of the lithographically patterned gold layer, a second one is fabricated. For the second lithography step, a different optical lithography mask is used. This mask contains the parts, which are to be enlarged. The second layer is done only in the regions, where it is needed. The wires on top of the first layer are designed one micron smaller on both sides. This prevents an overhang of the top layer over the edge of the bottom layer. Such an overhang appears, when the two layers are not perfectly aligned. An overhang could fall of the chip and lay down in a bad place, or it peels off during lift–off. An overhang causes ill defined current flow and scatters light when it bends. This is avoided by reducing the width of the top layer. An alignment accuracy of less than one micron is feasible.

To obtain good adhesion between the two layers, the first layer is cleaned carefully. The first evaporated gold layer has a certain height, which makes the resist spun on top of it wavy. The contact of the lithography mask for the second step to the resist is not as good as for the first step. Still for the second lithography step the same parameters as for the first step are used. Image reversal resist is spun onto the sample with 500 rpm. The edges and resist residues on the backside of the substrate are removed and the resist is exposed for 0.9 seconds in the mask aligner. The sample is pressed against the mask with strong contact and high precision and vacuum chamber are used. The baking time is 3 minutes on 120°C with vacuum contact to the hotplate. Flood exposure takes 50 seconds and development is done in AZ 726 MIF by eye. Seeing when the resist is fully developed is a little more difficult, as the substrate has a structure on its surface already. Looking at the layout before developing helps recognizing the structure. Water is used as stop bath. Before evaporation, the sample is ozonated for 7 minutes. This removes thin resist residues, which can be left after development. As gold is evaporated on gold, an adhesion layer is not needed. A titanium adhesion layer would cause forces inside the wire due to the different material properties, and bad heat transport. Lift–off is performed after evaporation.

Light scatters on the second surface much more, than on the first. This is observed in the experiment. A higher scattering rate is expected, as every additional process step pollutes the surface. During the double–layer fabrication process the rest of the atom chip is protected by the lithography resist. Consequently only the second layer has an inferior scattering character. The higher scattering rate of the second layer did not disturb the experiment significantly.

The double–layer technique allows to build atom chips with different wire heights. For the experiments of this group one double–layer structure was sufficient. If desired, more than two layer can be build with the same technique. This technique also enables the combination of different materials.

6.3.1 Examples of double–layer atom chips

A double–layer atom chip is one of the most successful atom chips of the last years of this group. Atom chip B XIV$_{Si}$ is mounted in the second rubidium BEC experiment for about three years and produced many results [Wil02, Hal04, Hof04, Krü04, Gar05, Sch05a, Wil05a, Wil05b, Krü05, Wil06a]. On this atom chip some of the central wires were enlarged in their cross section by adding a second layer. Figure 6.3 shows an sector of this atom chip.

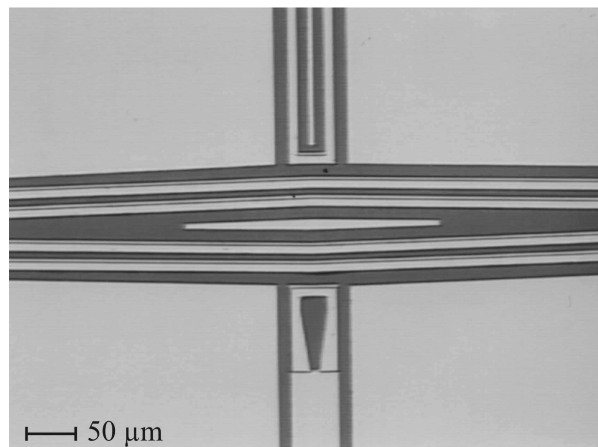

Figure 6.3: This picture shows a part of the double–layer atom chip B XIV$_{Si}$. All wires are 10 μm wide double layer metal films, while the ground surface is a single layer. Visible is the change from single to double–layer at the static charge connection which leads from the bottom to the centre. It is double–layered around the hole. The bottom layer has a height of 1.3 μm, while the top layer has a height of 1.8 μm.

The test atom chip B VII$_{Si}$ also contains a double–layer structure. To save e–beam writing time for the mask writing and to build an easy design, only the narrow part of the wires are enlarged by a second layer. Outside the central region, the first layer is wide enough to carry all the current by itself. Figure 6.4 illustrates the design of atom chip B VII$_{Si}$. This has been the first double–layer atom chip and the overlap was not taken into account. A mismatch of the two layers results in a bad edge at the right side of the wire. Figure 6.5 shows a view onto the same wire from the left side. In this figure, the sample is mounted with an angle of 80° into the SEM.

A kind of double–layer is fabricated on the e–beam atom chip, where the e–beam part is connected with the optical lithography. Also on the multi layer atom chips the pads are fabricated in double–layer technique. In both cases an adhesion layer of Ti is evaporated between the two gold layer, as these second layers are not fabricated on gold everywhere.

6.4 Multi–layer atom chips

The double–layer atom chip described in Section 6.3 is a simple multi layer atom chip. This atom chip contains two layers which have electric contact to each other. A second two layer atom chip is the coated atom chip (see Section 6.2). The multi layer atom chip described in this section consists of several different layers. At least two of these layers are structured metal films, which cross each other. Contact between the two layers is avoided by an insulating separation layer prepared between them.

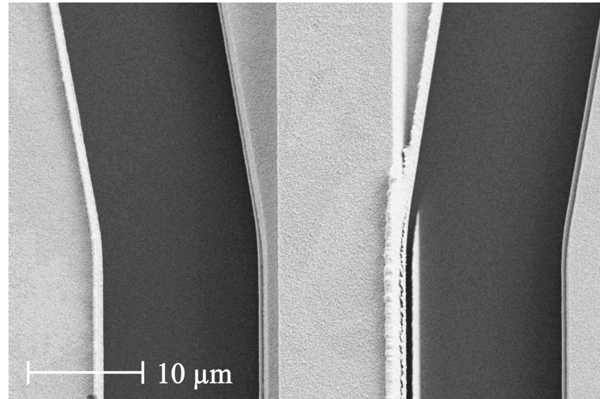

Figure 6.4: This SEM image shows a top view of a 10 μm wide double–layer wire of the test atom chip B VII$_{Si}$. The wire is double layered to enlarge its cross section. The width of the top layer is not reduced. A slight mismatch between the two layers leads to the rough edge at the right side of the wire. Both layers have a height of 2.3 μm. In the top part of the figure the bottom layer widens up. At the left and right side the single layer ground pattern is visible.

Free standing bridges which use vacuum as separation between two metal layers are fabricated on microchips with small wires [AK05]. They are not suitable for the purposes of atom chips. The stability over the distance needed on atom chips is not sufficient, they are difficult to produce for such big wires and the heat conductivity is the worst. Unsufficient tries of different materials used as separation layer are described in Appendix E.

On multi layer atom chips fabricated during this thesis, thick wires lead above thin wires. This is due to the used technique. An insulating separation layer is processed on top of the thin wires. On top of this insulation layer, the thick wires are fabricated. The advantage of thick wires above thin wires is that thick wires are able to climb steps. These steps appear because the bottom and the separation layer are already fabricated on the surface of the sample and the thick wires have to surmount them.

Heat is produced when a current is pushed through a wire. To prevent the wire from damage, this heat has to be lead away. The heat produced in a wire on top of an insulation layer is transported inside the wire, until the wire contacts the substrate. Here the heat dissipates into the substrate. The heat is not transported through the insulator, as it has a bad heat conductivity. As heat transport is better in a wire with a big cross section than in a small cross section, the wire on top of the insulator should be solid. Another reason to fabricate the thick wires on top of the insulator is, that thin e–beam written wires are more easy to fabricate on a flat sample surface than on top of a rough separation layer. Atom chips with e–beam fabricated wires will be discussed in the following sections.

6.4.1 Sample size

The final size of the multi layer atom chip is the same $25 \times 30\,\mathrm{mm}^2$ as for regular atom chips. The special fabrication technique of the separation layer requires more space around the evaporated area. In the beginning of preparation, the sample is cut to a size of $38 \times 38\,\mathrm{mm}^2$. This size is chosen to fit into 2" holders, which are used in the present mask aligner and e–beam lithography machine. A squared sample gives better surfaces uniformity of the separation layer than a rectangular. For the use of the existing 2" e–beam holder a few mm^2 of one edge of the sample are chopped of.

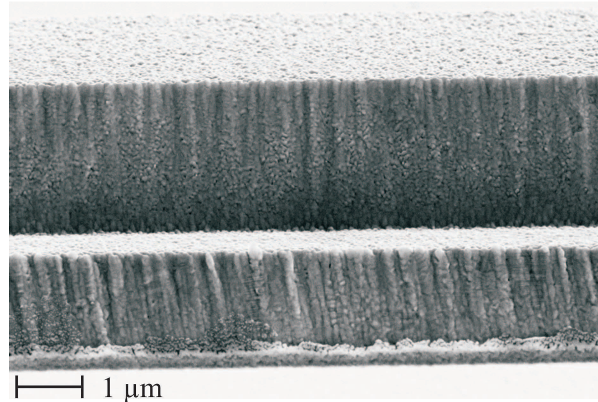

Figure 6.5: This figure shows a SEM picture of a double–layer wire from the test atom chip B VII_{Si}. The figure is taken with an angle of 80° to the surface of the atom chip. Each layer has a height of 2.3 μm. By misalignment during fabrication, the top layer is shifted with respect to the bottom layer. A step appears.

6.4.2 Starting the fabrication

To align several different layers, the fabrication of the multi layer atom chip starts with the preparation of alignment markers. In case of standard lithography, the first (bottom) layer contains all necessary alignment markings for the following steps. Like fabrication of a regular atom chip the bottom layer contains wires, grounded areas which are used as mirror, contact pads and additional alignment markings. The evaporated height of this layer is about 400 nm. The fabrication technique is described in Chapter 5. The separation layer is fabricated after the wires, which have to be thin or are to be below other wires, are manufactured.

Fixing a design defect

A design defect slipped into the layout of this specific mask. The layout is displayed in Figure C.6 in Appendix C.4. An electrical contact has to be blocked by hand to cancel this defect. After development of the photoresist pattern, a tiny drop of image reversal resist is put into the resist structure. This disrupts a 100 μm wide wire close to the edge, where the surface quality is not important. The dropping is done with a tiny needle, dipped into resist. The resist on the needle tip is put in the desired location. To harden this drop, the sample is baked on a 100°C hotplate for two minutes and the sample is put into the ozonator for 7 minutes. After evaporation lift–off is more difficult in this spot. As the drop does not have an undercut, the surrounding metal film might start peeling off from this point. Tweezers or a q–tip are used to break the metal film in this place. Figure 6.6 shows the resist drop and the gold layer after lift–off.

6.4.3 Separation layer

For separation, a material is needed, which isolates two metal films of different layers electrically from each other (see Figure 6.7). Required is a material, which is easy to handle, has good thermal conductivity, holds the wire in a defined way and is suitable for ultra high vacuum. Thermal expansion coefficients and adhesion of titanium, which is used as adhesion layer below the gold during evaporation, are also important.

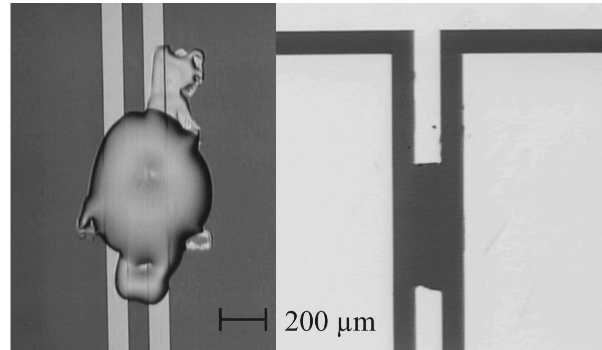

Figure 6.6: Fixing of resist structures by hand. Due to a mistake in the *dw-2000* layout, wires are hot–wired in the mask design. To fix this, an electrical contact is disconnected. left: A tiny drop of image reversal resist is placed between the two bright 100 μm wide resist patterns by hand. right: A disconnected 100 μm wide wire after lift–off. The left and right pictures show different atom chips.

Polyimide[1] (relevant properties of polyimide are listed in Table D.1 in Appendix D) is utilised as separation layer for the atom chips fabricated during this thesis. Polyimide is electrical insulating, possible to pattern lithographically and its height is tunable by fabrication techniques developed during this thesis. The heat conductivity is not good and it is nasty ho handle, as its consistence is like honey and it sticks everywhere, while it is difficult to remove. After processing it is hard and stable.

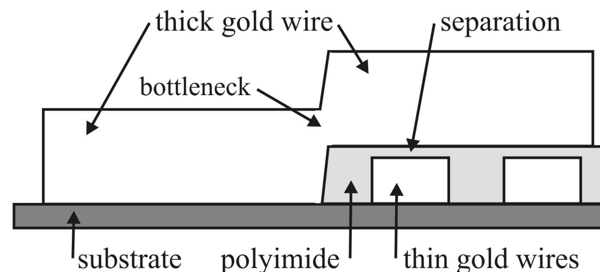

Figure 6.7: Graphic of a thick wire climbing onto a polyimide resist layer. Thin wires are covered by the polyimide, which separates the two gold layers. The cross section of the thick wire is reduced in the place, where it climbs the polyimide. This builds a bottleneck for the current and the heat transport inside the wire.

6.4.4 Preparation of polyimide

Polyimide is spun dynamically onto the sample. While spinning the sample with 300 rpm the polyimide is dropped onto the surface. Therefore the tip of the pipet top is cut off, to enlarge the opening, so the polyimide gets in and out of the pipet top more easy. The covered sample is spun for 7 seconds with 1000 rpm and finally for 90 seconds with 10400 rpm. This is the highest speed and time for the used spinner. This fast spinning speed for the long time is needed, to reduce the hight of the laminar polyimide as much as possible. After spinning,

[1]Durimide (R) 7505; Arch Chemicals; Zwijndrecht; Belgium.

the sample is put on a flat horizontal surface for 10 minutes. During this time the bulges of polyimide at the edge of the sample flatten a little and the spinner and working place are cleaned carefully. Polyimide is nasty to use, but it is even worse, once it dried. To avoid this, everything is cleaned immediately and carefully after use.

The baking time is 5 minutes on a 100°C hotplate. After cooling down, the polyimide film is patterned lithographically with a mask and UV–light in the mask aligner. The used polyimide is photosensitive to 405 nm UV–light. The same mask aligner as for the previous optical lithography is used. Exposure time for this polyimide is 7 seconds. The sample is softly pushed against the glass mask. Strong contact or high pressure can cause the sample to stick together with the mask. As polyimide is difficult to remove, sample and mask might be lost in such a case. After exposure, the sample is soft baked for 1 minute on a 100°C hotplate. Before developing, the sample is laid untouched for 15 – 30 minutes. Development in QZ 3501[2] takes 40 seconds. The development is stopped by n–butyl acetate[3] for two minutes. The pattern of the polyimide is visible now. To harden this pattern the sample is cured for one hour at 300°C. This oven is continuously flooded with nitrogen. The temperature is ramped to 300°C with 4°C/ minute. After baking, the sample is taken out of the oven at a temperature below 100°C. As cooling the oven takes about three hours, the full polyimide fabrication process takes about a day.

After curing the process is finished. The polyimide is hard and looks and behaves like plexiglass. During the fabrication process of polyimide contact with water is avoided. Water influences the processing as long as the polyimide is not cured.

This process results in a polyimide height of about 550 nm. The height of the polyimide depends on the spinning speed and the spinning time. The exposure time is almost independent on the height of the polyimide. Only the development time is dependent on its height. The height decreases slightly in n–butyl acetate, but a further decreasing after two minutes was not observed. The height dependence on spinning speed and time, and the dependance from the development and stopping time is listed in Table 6.4.4.1.

The thickness of the polyimide can be tuned during fabrication. This is not very precise, and is measurable only when the preparation process is finished. For atom chips, the fabrication recipe is chosen, which delivers the thinnest polyimide film. This film of approximately 550 nm is still too thick. It was observed, that the ozonator removes polyimide slowly. This process is calibrated and utilised for thinning the polyimide. Figure 6.8 shows the removal speed of polyimide in the ozonator. The average removal speed of polyimide in the ozonator is 7.4 nm/ minute.

The polyimide layer is thinned in the ozonator to a value, which is a little higher, than the bottom gold layer of $\sim$ 400 nm. This ensures an insulation film between the bottom layer and the crossing wires, which are fabricated onto the polyimide. The polyimide layer is $\sim$ 100 nm thicker than the bottom layer. A short recipe of the polyimide process is listed in Appendix C.3.

[2]Polyimide Developer QZ 3501; Arch Chemicals; Norwalk; Belgium.
[3]n–butyl acetate, GR for analysis; Merck; Darmstadt; Germany.

spinning speed (rpm)	spinning time (sec)	development time (sec)	stop bath time (sec)	height (nm)
3000	30	60	20	4000
5000	30	40	20	2200
5000	60	45	20	1700
10400	30	35	120	950
10440	60	40	120	930
10400	100	40	120	720
10400	90	40	120	700
10400	90	40	120	630
10400	90	25	120	630
10400	90	25	20	600
10400	100	40	120	570
10440	80	30	120	560
10440	80	30	150	540
10400	90	40	120	540
10400	90	28	127	510
10440	90	40	120	260*
10440	100	40	120	240*

Tabel 6.4.4.1: The height of polyimide, resulting from spinning speed, spinning time, development time and stop bath time is listed in this table. The maximum spinning speed of 10440 rpm and the maximum operation time of 120 seconds of the spinner are used. As it is dynamic spinning, with dropping the polyimide onto the rotating sample and additional spinning for 7 seconds with 1000 rpm, only ~100 seconds are left for high speed spinning. The spinning time is estimated, because it changes in a dynamic spinning process. The height of the polyimide is measured with a profilometer. The thickness slightly varies with the position of the measurement.

* The last two height values are measured after curing and putting the sample for one hour into the ozonator.

6.4.5 Crossing wire fabrication

On top of the thinned polyimide, wires are fabricated. The preparation process is the same as the one described in Chapter 5. The image reversal resist is not as flat as usually, but the parameters are the same. Ozonation is done after development for 7 minutes, to remove resist residues. This reduces the polyimide film thickness at the location of the wire about 50 nm (see Figure 6.8). This is taken into account, when the sample gets into the ozonator or is cleaned to be processed again. The design defect is fixed by hand again, as this design also contains the disconnected wire at the edge. This mask of the top big wires also contains the contact pads. This makes the pads double–layered. Enough metal for good bond contacts is deposited by this technique.

Lift–off is done carefully. The adhesion of the titanium on the polyimide is not as good, as on SiO_2. The most difficult step is drying the sample with N_2 gas after the isopropanol bath. The N_2 is blown onto the atom chip in the direction of the wires and from a larger distance than for normal atom chips. Figure 6.9 shows a gold wire climbing the step onto a polyimide separation layer, while Figure 6.10 shows crossing wires on a completed multi layer atom chip. These wires are separated from each other by a polyimide layer.

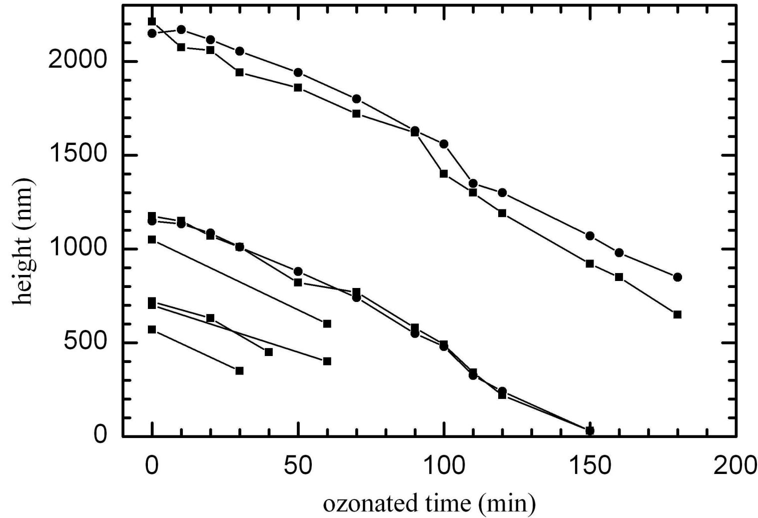

Figure 6.8: The decrease of the height of the polyimide of different samples is plotted against the time it was ozonated. Two samples are measured in two different places. To distinguish between the two places squares ■ and circles • are used.

The heat transport through an insulation layer like polyimide is not good. To prevent the top wires from burning, the polyimide covered area is kept as small as possible. Lithographically structuring allows to pattern the polyimide. Wires are able to climb from the substrate onto the polyimide. To manage this, the wire has to be taller than the step. A thin separation layer is essential. Every wire on the polyimide also has contact to the substrate in an other place. This enables the produced heat to flow through the metal of the wire down the step into the substrate.

The height of the step depends on the height of the wires, which are covered by the polyimide. The thin wires as bottom layer build a thin step (∼450 nm), which is easy to climb for the thick wires (>1 μm). The other way around is not possible. A thin wire on the surface of the sample is unable to get in contact with its continuation on top of the polyimide, which builds a tall step above 1 μm high wires.

The height of a wire is reduced in the place, where a wire climbs a step (see Figure 6.7). This is a bottleneck for the current and for the heat transport. The reduced cross section enlarges the resistance for the current in the wire and it limits the heat, transported through the wire from the top of the separation layer to the substrate.

A disadvantage of the fabrication technique of big wires above thin wires is the optical access. The thick wires are dedicated to trap atoms and guide them to the experimental region, while the thin wires are build to manipulate these atoms. Atoms trapped close to the thin wires might be difficult to observe. Close to the thin wires they are between the big wires, which are on top of the separation layer, above the thin wires.

Other groups build thin wires completely on top of thick wires, without steps [Sch05a]. There is no problem with the optical access. Electric contact, heat transport and the distance to the thick wires due to thick separation layers become problematic.

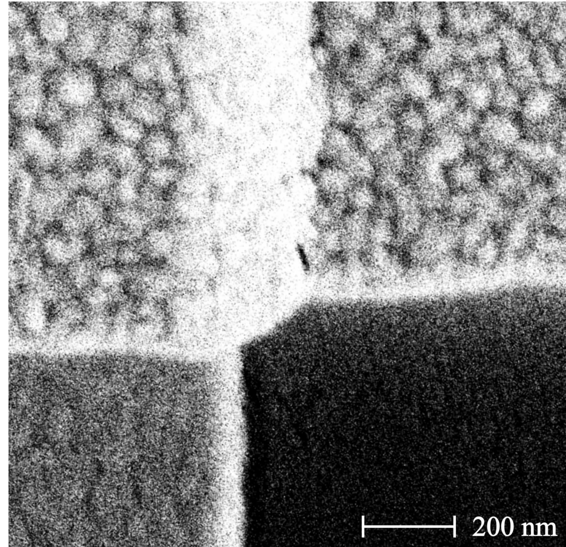

Figure 6.9: This SEM picture shows a polyimide separation layer on the left side, which is climbed by a gold wire, shown in the upper part of the figure, from right to left. The grains of the gold layer are visible. On this atom chip E_gVI_{Si} the thickness of the polyimide layer is 560 nm, while the thickness of the climbing gold layer is 1.37 μm.

6.5 Sub–micron structured atom chips

In micro electronics, everything gets faster and smaller [Moo65]. Also the width of a wire affects the magnetic field and its gradient (see Section 2.5). For some experiments, narrow wires are required. The regime, where trapping potentials are generated so close to each other, that tunnelling of atoms between them becomes possible, opens the way for new experiments of quantum physics.

The minimal width of wires on an atom chip fabricated with optical lithography is limited by the wavelength of the light used during exposure. To minimize the possible feature size this light is UV–light for standard processing. The smallest feature size with UV–light of 405 nm wavelength is about 1 μm. For these and other atom chip experiments one micron feature size is too large. To reach smaller sizes the use of a standard mask aligner is inapplicable. Either the wavelength is reduced to extreme UV–lithography (a resolution of up to 65 nm is achieved with a wavelength of 193 nm) or electrons are used. To fabricate sub–micron wide features on atom chips, electron–beam lithography (e–beam) is used in this thesis and in other groups [Est05]. The resolution limit of e–beam lithography is below 10 nm for 100 kV acceleration voltage [JEO06].

To save writing time and money it was decided to build a regular atom chip with a separate e–beam written part. The layout of the optical lithography multi layer atom chip contains a $600 \times 600\,\mu\text{m}^2$ free area in the centre of the design. This vacancy is filled with evaporated gold wires and grounded areas, which are e–beam patterned. This provides a cheap and flexible atom chip. The size of $600 \times 600\,\mu\text{m}^2$ is chosen, as $700 \times 700\,\mu\text{m}^2$ is the writing field of the e–beam.

Using more than one writing field can cause stitching effects, which are small missalignments between the different fields. A 50 μm border around the $600 \times 600\,\mu\text{m}^2$ area is needed to allow an overlap with the optical lithography. This overlap assures electrical contact between the e–beam and the optical lithography layer. A $600 \times 600\,\mu\text{m}^2$ written field is big

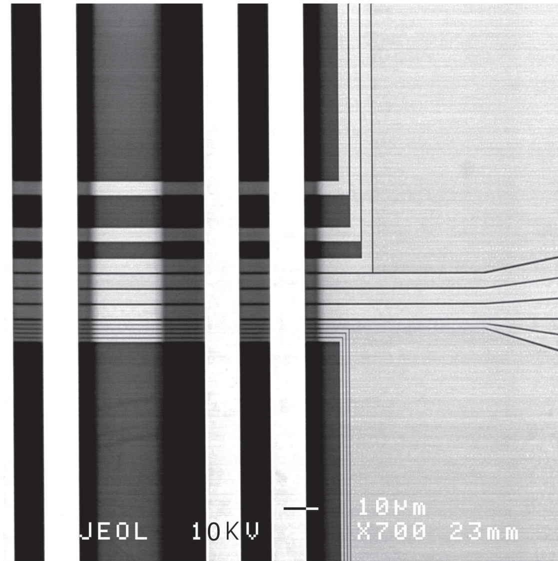

Figure 6.10: SEM picture of crossing wires on multi layer atom chip E_e7_{Si}. The 110 nm thick gold wires from left to right are covered by an insulating polyimide layer. The separation layer, visible as grey shadow, is 630 nm thick. On top of this layer, 1.3 μm high wires are fabricated. These are leading from the top to the bottom. The thickness of the polyimide has this height, as the bottom layer of this atom chip is 400 nm thick, and the trick with the ozonator was not discovered when this atom chip was build.

enough to enable many different experiments with e–beam patterned wires.

The same lithography masks are used for all multi layer e–beam atom chips, while the inner structure of the e–beam part is designed for each single e–beam atom chip individually. This is a very powerful tool, together with the advantage of the high resolution of the e–beam, which is in the order of a few tens of nm in standard use. During this thesis the smallest feature size of e–beam written features is 300 nm. This is due to the needs of the experiments, not due to the fabrication limits.

The fabrication of an e–beam patterned atom chip starts with the lithographic preparation of markings. Markings are used to align all layers of the multi layer atom chip to each other during fabrication. One of these layers is the e–beam structured layer. For e–beam alignment special markings are used. These are simple crosses of 4 μm wide bars, which are at least 80 μm long (see Figure 3.4). These crosses are recognized by the e–beam machine automatically once one of the crosses is located by hand. Searching the first cross with the e–beam is critical. The e–beam used for imaging the sample and finding the cross already exposes the resist. Therefore the location of the cross on the sample holder is known as good as possible, and the cross is fabricated far from the exposed region. To be able to find the tiny cross more easily on the huge sample, big metal structures ($200 \times 500\,\mu\text{m}^2$) are fabricated next to them. These are well visible and easy to find.

For e–beam lithography, a sample is covered with a resist. This resist is sensitive to electrons of a certain energy. The electrons are accelerated and precisely directed onto the sample. The electron beam is moved over the sample in a way defined by the layout of the *dw-2000*. The designed pattern is written into the resist. After development the sample fabrication is continued with evaporation and lift–off like in the standard process described in Chapter 5. The exposure in the e–beam, is done point by point. The writing time depends on the size of the structure.

6.5.1 Fabrication of a multi layer e–beam atom chip

The fabrication process of the e–beam atom chip starts with the e–beam patterned part. Alignment markings are needed to locate it in its accurate place. These are prepared in a standard lithography process (see Chapter 5). The e–beam alignment markings are special. They are described in the previous paragraph. The alignment layer provides orientation markers for all future process steps and ensures, to have good alignment between all layers. With these alignment marks the central e–beam written part is positioned. To write the e–beam part, the e–beam sensitive resist has to be prepared on the sample. In the previous standard lithography step for the markings primer has been prepared on the sample surface already.

Electron sensitive resist is spun on the clean sample. To achieve an undercut after development, two different resists are prepared on top of the sample. The bottom layer is poly–methyl methacrylate[4] (PMMA) 495K 5% spun for 60 seconds at 5000 rpm. PMMA is also known as plexiglass. This resist layer is baked for one hour at 180°C in an oven. During baking the sample is put into a small box which is made from aluminium foil to protect the oven from dirt. PMMA resist sticks at the back side of the sample and would partly stay in the oven. After cooling down, the second layer is spun onto the first. Cooling down takes short time and spinning is done quickly.

The second resist is PMMA 950K 5%. Spinning time is again 60 seconds with 5000 rpm. Baking time again is one hour at 180°C in the aluminium box in an oven. The solvent inside the second resist slowly solves the previous resist layer. To minimize damage on the first layer, the second resist layer is applied to the sample quickly and spinning is started fast. When the sample is covered, the important central part, is covered last. The resist in this region is damaged the least. After spinning the sample is put into the oven immediately. A short recipe of the e–beam process is shown in Appendix C.4.

The colour of the resist is uniform, except for the corners, where the thickness of the resist is slightly changing. Noticeable areas or dots are signs for defects in the resist. These areas should not be at the location, where writing will be done. The writing area of $600 \times 600\,\mu\mathrm{m}^2$ is small compared to the sample size of $38 \times 38\,\mathrm{mm}^2$. The needed clean resist area is located in the centre, and easy to check due to the alignment markings. The thickness of the resist layers is checked after each baking. A tiny scratch is done into the resist at the edge of the sample using plastic tweezers which scratch the resist but not the surface. The thickness of the resist is measured in this place with a profilometer. The height is about 180 nm for the first layer and about 400 nm for both layers together. The spin coated sample is put into the e–beam lithography machine[5] and exposed to the electron beam.

After exposure, the sample is developed for 60 seconds in a mixture of one part methyl isobutyl ketone (MIBK) and two parts of isopropyl alcohol (IPA, isopropanol). To assure equal development the sample is moved during development. The stop bath for the developer is pure isopropanol, which is blown away with nitrogen gas afterwards. Development is done directly before evaporation. In case of delayed evaporation, the development is delayed also, until the evaporation can be done.

The e–beam patterned resist structure is very small compared to the full sample size. Holes in a non critical place of the resist are covered by hand. A pipet is filled with S 1805[6] resist. A thin film of this resist is carefully drawn with the pipet around the pattern over the holes to cover them. After fixing the holes, the sample is baked for two minutes on a 100°C hotplate to harden the additional resist. Samples saved in this way do not need cleaning

[4]ESS environmental sampling supply, Oakland, USA.
[5]5FE lithography machine, JEOL, Tokyo, Japan.
[6]Microposit® S1805 Photo Resist, Shipley Company, Marlboro, Massachusetts, USA.

and new e–beam writing. This hand cover technique is also done in the previous standard lithography step of marker fabrication. Only the small areas of the markings are important in this mask layout and holes in the resist are easy to fill.

The height of the developed e–beam resist is measured with a profilometer. It limits the amount of the deposited metal. Evaporation is described in Section 5.5. The e–beam patterned part of atom chips fabricated in this thesis comprise of an evaporative deposited titan/ gold layer of 10/ 110 nm respectively. Standard lift–off follows the evaporation. Figure 6.11 shows e–beam patterned gold wires. The recipe of the e-beam process is shown in Appendix C.4.

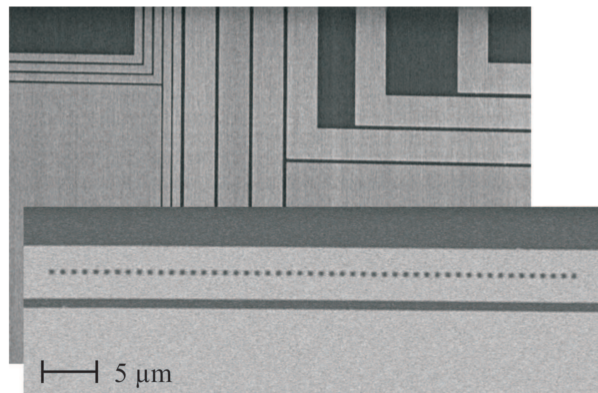

Figure 6.11: SEM pictures of e–beam patterned wires. top: The gaps between the wires on the left are 300 nm wide, while the wires themselves are 700 nm wide. The wide wires are 3 μm wide separated by a 1 μm gap between them. bottom: A SEM picture of a 5 μm wide wire with a line of holes in it. Each hole is a square of $500 \times 500\,\mathrm{nm}^2$, the period is 1 μm. These holes are fabricated to modulate the current density inside the wire, which affects the generated trapping potential [Pie06]. The scale is valid for both pictures.

After lift–off, the preparation of the e–beam atom chip continues with standard lithography of multi layer structures. To contact the e–beam part, regular gold wires are evaporated with a small overlap onto the ends of the e–beam wires. The alignment of less than 1 μm accuracy is done by the alignment marks, which are evaporated in the first step, before the e–beam lithography. The full e–beam region with its connections, the separation layer and the crossing wires are shown in Figure 6.12. Figure 6.13 illustrates the fabrication process of an e–beam atom chip with photos taken during the fabrication.

6.5.2 Advantages of the e–beam atom chip

The fabrication of a small e–beam patterned part also allows to use different materials just in the centre of the chip. This yields the advantages of a well known surrounding gold structure and new materials close to the measured atoms. Also combinations of metals are possible.

Another powerful advantage of the e–beam written part is its flexibility. As the e–beam patterned area has to be written for each atom chip, its layout can be changed for each atom chip. The optimal design can be produced without changing the design of the optical lithography masks. This flexibility is extremely efficient in time and money.

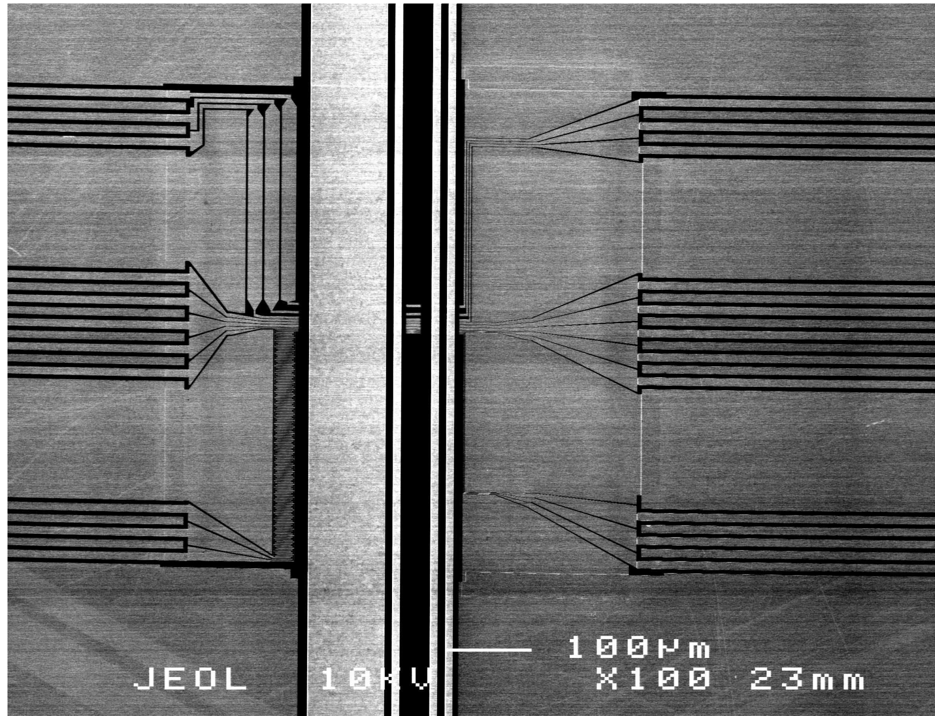

Figure 6.12: The full $600 \times 600\,\mu\text{m}^2$ e–beam written field with its surrounding is shown in this figure. To its left and right the connections for the e–beam part are visible. The pale wires leading from the top to the bottom are crossing the e–beam patterned wires in the centre without having contact to them. The two gold layers are separated by a non visible polyimide film.
On this atom chip $\text{E}_e\text{VII}_{Si}$ the e–beam layer is 110 nm thick, the contacting layer 400 nm, the polyimide has a thickness of 630 nm and the top gold layer of the crossing wires has a thickness of $1.3\,\mu$m.

6.5.3 Difficulties during sub–micron structuring

Special care is taken to the fact, that lithography masks are mirror imaged in use, and direct e–beam written parts not. This might cause problems, if not taken into account during designing the layout (see Chapter 3).

As the e–beam writes the pattern with a current of electrons, exposure is done slowly dot by dot. If exposure or development are not done correctly, small bubbles of resist remain on the sample surface. These are difficult to see before evaporation. After evaporation they are visible in the metal structure, but impossible to remove. Figure 6.14 shows such a sample after evaporation. These bumps lead to a rough surface and to a not straight current flow. To avoid these defects on a real sample, dummy samples are written with different doses before the real one. The correct exposure dose and development time is determined or the design is modified.

A possible feature of e–beam patterned wires are tiny holes inside them as seen in Figure 6.11. In the experiment they are going to modulate the current density inside the wire, which modulates the potential shape. During lift–off the metal pieces covering the holes fall off. These particles are likely to connect to the surface. To prevent this, the sample is turned upside down. The metal pieces stick extremely good in gaps of the same size. Here they are irremovable and shorten the wires. Gap and particle sizes are designed with small differences to lower the possibility of connected wires.

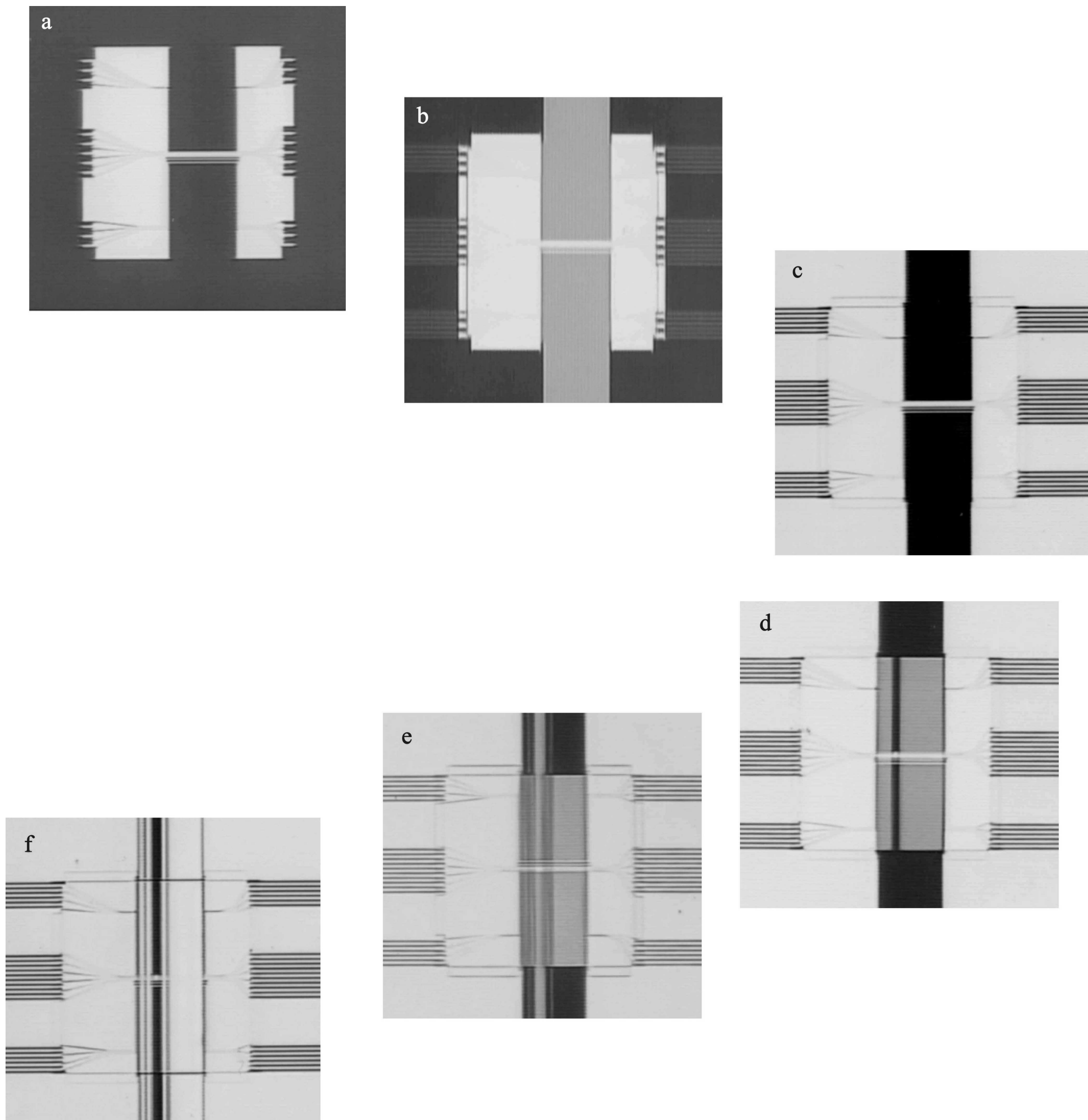

Figure 6.13: This series of figures shows the photo lithographic fabrication process of the multi layer e–beam atom chip $E_g VI_{Si}$. Each photo shows the previous sample after the next fabrication step. a: e–beam patterned wires after evaporation and lift–off. The size of the square is $600 \times 600\,\mu m^2$. The wires in the middle are going to be crossed without contacting them, the fingers at the left and the right border are connections for the wires in the middle. The dark ground is the Si/ SiO_2 substrate. b: The e–beam written gold layer with a photo lithographically patterned resist structure. The resist defines the leads to the gold area and the grounded areas around. c: The leads to the e–beam part and the grounded areas after evaporation and lift–off. d: The polyimide separation layer is photo lithographically patterned and cured. It partly covers the e–beam structured wires in the centre. e: Photolithographic structured photo resist on top of the polyimide. This resist defines the wires which cross the wires below the polyimide. f: After deposition of the top wires and lift–off, the e–beam atom chip is ready to use.

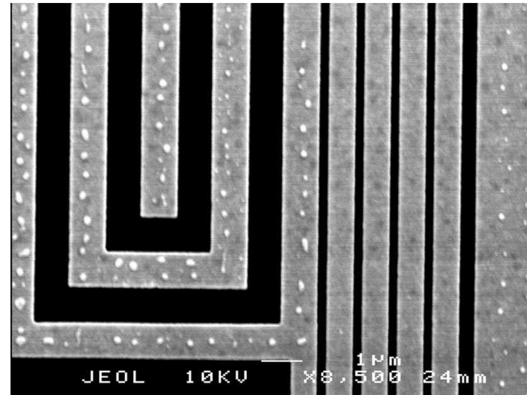

Figure 6.14: SEM picture of e–beam patterned gold wires on the atom chip E_eVII_{Si}. The wire on the right and the wires on the left are underexposed. Humps of PMMA resist are left below the deposited gold. The gold is deposited on top of the surface and keeps its shape. Exposure and development of the narrow wires on the right are good. They have a smooth surface. For a better quality of the spotted wires, their exposure dose is increased. This is possible due to the different data types in the layout of the *dw-2000*.

6.6 Semiconductor atom chips

The previously described atom chips contain fabricated gold wires on Si/ SiO_2. Theoretical calculations predict different behavior of trapped atoms close to metals, than to insulators or semiconductors [Hen99, Hen00, Dik05].

For common use in future, atom chips might be build like integrated circuits from a single semiconductor substrate. An advantage of using semiconducting wires is to build the atom chip itself out of the substrate (see Section 2.12). This technique is more robust than wires manufactured onto the surface. Structured semiconductors might be used as atom chips to measure the current flow inside the semiconductor by using the cold atoms as a detector, to study atoms close to semiconducting surfaces or for other experiments.

Removing doped substrate by etching is the technique used to fabricate semiconductor atom chips in this thesis. The fabrication will be explained in detail in the next paragraphs. After etching the remaining structure builds the wires. This technique results in a rough surface, but it is suitable for thick doped layers and no metal is used. These reasons caused the decision for this technique. The doped layer has to be thick, to push enough current through the wires and build atom traps. Depletion is not promising for this thick doped layer, and has the disadvantage of charged metal on top of the surface.

To start the new generation, semiconducting atom chips have been fabricated during this thesis. They are ready to use, but not inside an experiment yet. This section explains the applied fabrication techniques of semiconducting atom chips. The used semiconductor is doped GaAs. The short fabrication process is listed in Appendix C.5 together with the data sheet of the GaAs.

6.6.1 Fabrication of semiconducting atom chips

The semiconducting atom chip is a combination of a multi layer atom chip using gold wires on Si/ SiO_2 (see Section 6.4) with a small added semiconductor chip on top of it. This combination is chosen, to unite the well understood fabrication, atom trapping and transportation

techniques of multi layer atom chips, with the use of semiconductors. The atoms are to be trapped and cooled in a pure multi layer region of the atom chip. From here the atom cloud or BEC is guided to the semiconductor.

A GaAs wafer is cleaved to the size needed. A small scratch parallel to a crystal axis is made with a diamond scratcher at the edge of the wafer and the sample breaks along this line if soft pressure is put on it. The size is chosen by the design on the mask. In this thesis five samples of different size are prepared at the same time on one piece of GaAs. They are separated from each other at the end of the fabrication process. Five of the small samples together are more handy than one tiny, and it safes time to prepare five at once. Also in the end reference samples of exactly the same quality are available.

Primer is spin coated onto the surface of the GaAs piece with 3000 rpm for 40 seconds. Baking takes 3 minutes on a 80°C hotplate. After cooling the substrate down, image reversal photoresist is spun with 5000 rpm for 40 seconds onto the sample. Soft baking of this resist takes 45 seconds on a 100°C hotplate. The resist is exposed through a lithography mask for 2.6 seconds with UV light of 405 nm wavelength and 15 mW power. The resist is post baked on a 120°C hotplate with vacuum contact for 45 seconds. The cold sample is flood exposed for 1.3 minutes. Half a minute later the resist is developed for 25 seconds in AZ 726 MIF and stopped in water. The sample is ozonated for 7 minutes to remove remaining resist left overs.

The sample is dry etched by reactive ion etching[7] (RIE). The samples were grown with a super lattice below the donators (see Appendix C.5.1). The etching is stopped when the super lattice is reached, which can be detected. In case of the fabricated atom chips during this thesis, the etched deeps is 930 nm, which is the height of the conducting layer. RIE etching is dry physical etching, in contrast to wet chemical etching. It builds straight walls. The resist pattern is transferred into the surface of the sample, without underetching the resist. For further preparation, the resist pattern is removed in a cleaning process (see Section 5.3).

The patterned semiconductor wires are contacted by alloying. The charge carriers in the semiconductor are located below the surface, which is insulating. To contact the conductive layer, the lithography process previously described is redone. This time lithography is done to evaporate metal onto the regions, where the semiconductor is going to be contacted. These regions are located outside the area, where the atoms are going to be trapped during the experiment. Metal is not designated close to the atoms. Especially not the used nickel, which is magnetic. The metal is also used as contact pad to bond wires from the GaAs to the multi layer atom chip. The bond wires disturb the optical access, so they are located as far away from the atoms as possible, and outside the direct optical line.

This evaporation is different to previously described evaporations. Several metal films are evaporated in defined order and amount. This is relevant to be able to alloy the metal into the surface. Alloying builds an electric contact between the metal on the surface and the semiconductor below.

For evaporation a standard process is used. The first evaporation layer is 50 Å of nickel. It is needed for alloying and used as adhesion layer. On top of the nickel, 400 Å germanium, 800 Å gold, again 200 Å nickel and in the end again 2000 Å gold are deposited. The first four evaporated layers are mainly to be alloyed into the surface and contact the semiconductor. The top gold layer supports enough metal to contact the layer on the surface by bonding. Lift–off is done the usual way. Just before alloying the sample is put into the ozonator for 5 minutes. A fabricated GaAs sample is shown in Figure 6.15.

[7] NEWE SCVI 101, Nextral, this company does not exist any more.

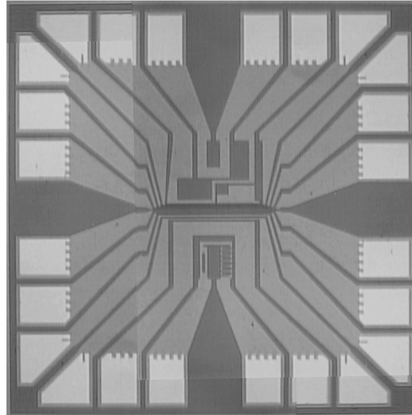

Figure 6.15: Picture of the GaAs semiconductor atom chip. Its size is $2 \times 2\,\mathrm{mm}^2$. The bright lines are semiconducting wires. They are separated by dark lines, which are RIE etched areas, where the doped conducting GaAs is removed. The bright ends of the wires at the edge of the sample are the metal contact pads for the semiconductor and the wire bonds. They are going to be alloyed in the next fabrication step.
The layout provides U and Z shaped wires, as well as a grid of wires with different width and other shaped wires. The layout also provides doped and undoped semiconducting surfaces. The optical access to the centre is free from bond pads, which are located at the edge to move the metal away from the centre.

6.6.2 Alloying

During alloying, the sample is heated. The metal layers alloy and penetrate into the surface of the semiconductor. The penetrating metal contacts the conductive layer inside the semiconductor. Alloying is done in a rapid thermal processor[8] (RTP), where the sample is heated for 30 seconds to 150°C, immediately afterwards for 30 seconds to 345°C and than the temperature is ramped during 10 seconds linearly to 430°C, where it stays for another 30 seconds. During alloying, the metal on the surface changes its appearance. Figure 6.16 shows partly alloyed metal. The temperatures were changed to the given parameters, to solve the problem of only partly alloyed metal. The shown sample could be saved by alloying it again. The full preparation process of a semiconducting sample is illustrated in Figure 6.17.

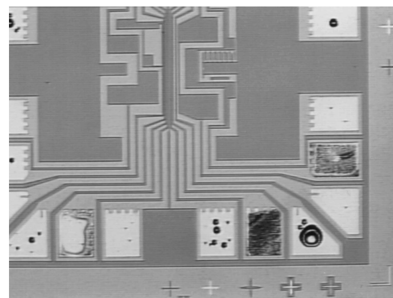

Figure 6.16: The contact pads at the end of the wires of this GaAs chip are in different states of the alloying.
At the bottom and the right side of the picture alignment markings are visible. The L shaped structure in the low right corner is an orientation marking for cleaving the sample to its exact size.

[8] ADDAX, this company does not exist any more.

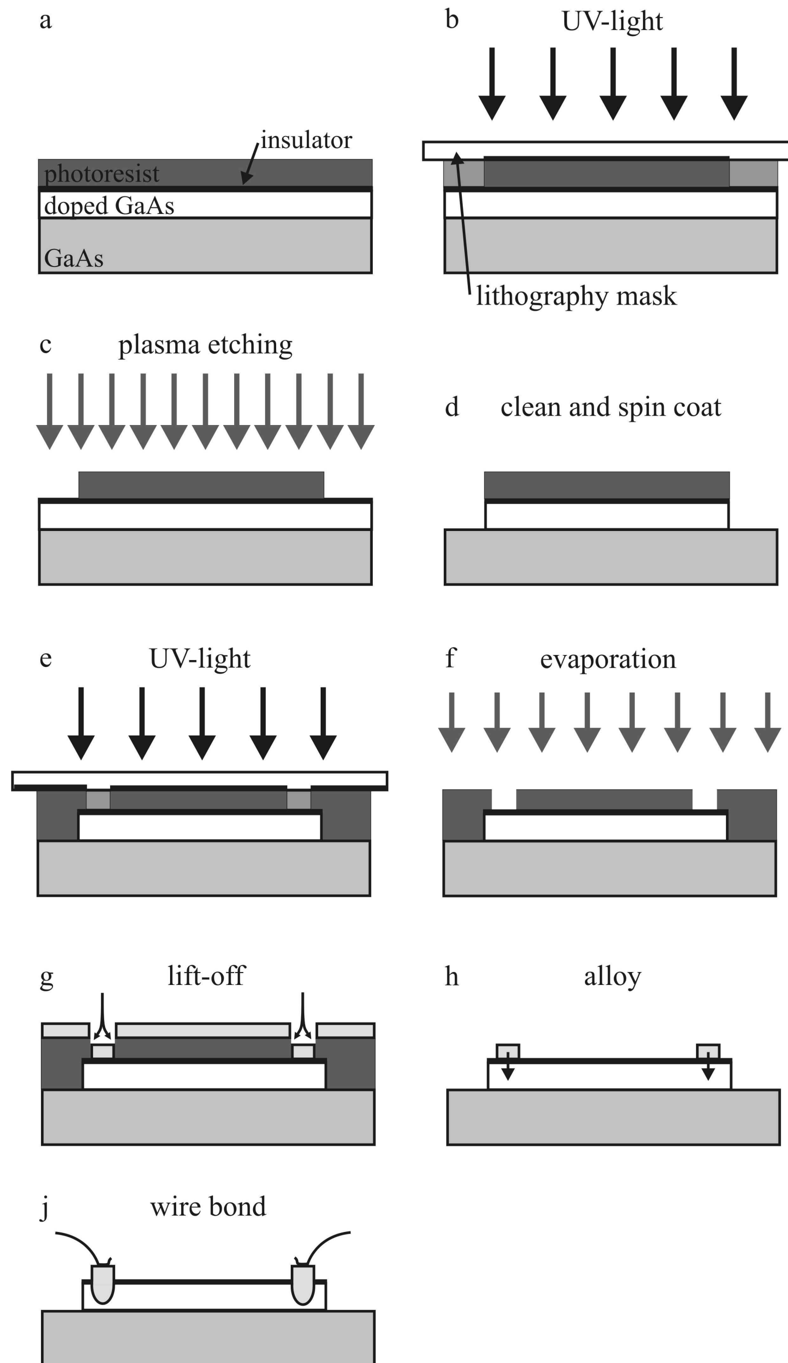

Figure 6.17: The preparation process of a semiconductor is illustrated in this figure. a: The GaAs substrate contains a conductive doped layer below its surface. For lithography photoresist is spun onto it. b: The resist is exposed through UV–light. A lithography mask defines the exposed pattern. c: After development the resist structure is used as mask for RIE etching. d: The structured sample is cleaned and new resist is spun onto the whole sample. e: A second optical lithography is done. f: Metal is deposited onto the sample with its resist pattern. g: Lift–off removes the resist and the metal on top of it. h: By alloying, the evaporated metal penetrates through the insulating surface of the substrate into the doped semiconductor. This metal connects the conductive layer. j: Wire bonds connect the metal pads on the surface. Electric contact is realised from one wire bond through the alloyed pad into the semiconductor. Current can flow inside the doped layer to the second alloyed area and out through the other wire bond.

6.6.3 Cleaving

The sample is a miniature chip now. It is cleaved to its required size. This is done accurately by cleaving with a precision diamond scratcher under a microscope. The size of the GaAs pieces fabricated for atom chips during this thesis is either $2 \times 2\,\mathrm{mm}^2$ or $3 \times 3\,\mathrm{mm}^2$. This is determinated by the amount of connections on the GaAs sample and the required distance of the alloyed metal and the bonds to the centre of the piece.

6.6.4 Wetching

The height of the GaAs sample is about $700\,\mu$m. Before it is mounted onto a multi layer atom chip the piece is thinned to $\sim 100\,\mu$m.

The sample is fixed to a special holder, which allows to adjust the distance of the sample accurately in respect to a parallel surface. The structured side of the sample is connected with wax[9] to the holder. A tiny bit of wax is melted (melting temperature 52°C) on the holder and the sample is pushed into it. With a micrometer screw the parallelism and the height of the sample is verified. The holder with the sample is mounted in the device with the sample overlapping the device for a few $100\,\mu$m. Figure 6.18 illustrates the device and its function. The device is moved over a fine emery paper which is parallel to the sample. Sample and emery paper are flooded with clean water to cool and to avoid dust flying around.

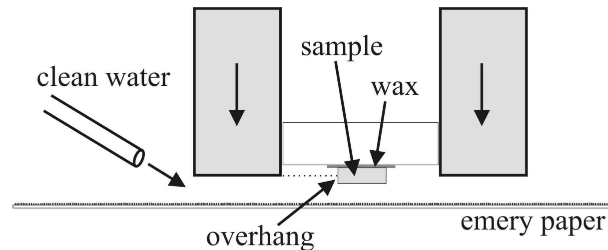

Figure 6.18: This illustration shows the steel sample holder for wetching. The sample is fixed with wax on a movable part. This is held parallel to the emery paper, which is fixed on a flat surface. The holder together with the overlapping sample is scrubbed in circles above the emery paper. The final height of the sample is defined by the overlap of the sample over the holder. During wetching, the sample is wetted with clean water.

Graining is done in a chemistry hood and protective gloves and clothes have to be worn, as GaAs is toxic.

The overlap of the sample is grained away. After some graining, the thickness and flatness of the sample is measured with a micrometer screw. By defining the overlap, the thickness of the sample after graining is defined. Afterwards the wetched sample is removed from the holder by melting the wax. The sample is extremely dirty, but the structured side is protected during the wetching by being inside the wax. The wax is solved by hot acetone and the sample is cleaned. The final thickness of the sample is about $100\,\mu$m. It is correspondingly much more fragile now and more difficult to handle.

[9]Thermoplastic Wax G3881, Agar Scientific, Stansted, UK.

6.6.5 Gluing a GaAs sample onto a Si atom chip

The GaAs is glued onto the prepared multi layer atom chip with UHV suitable glue[10]. A tiny drop of glue is put onto a clean surface. The samples backside is pushed slightly into this drop, so some of the glue sticks to the sample. The sample is put in position onto the atom chip. Lithographically patterned alignment markings on the atom chip help to place the GaAs in position. The GaAs is aligned with a precession of about 50 μm under a microscope. The glue is cured by baking the atom chip for 3 minutes on a 100°C hotplate.

The GaAs chip is fixed on the multi layer chip. The wires on the GaAs are bonded with gold wires to the wires on the multi layer chip. Figure 6.19 shows a completed semiconductor atom chip. In the inset the semiconductor is enlarged. Also the bonds from the GaAs to the multi layer atom chip are visible.

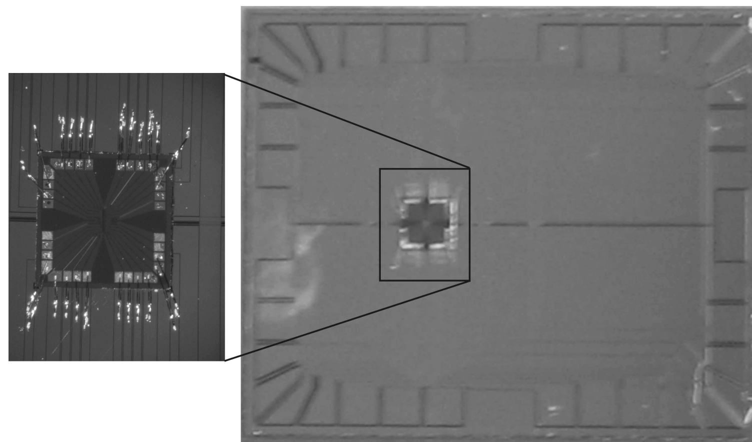

Figure 6.19: Photos of an atom chip with a semiconductor chip mounted on it. right: The GaAs is located off centre to provide space to trap atoms in a mirror MOT. left: Enlargement of the semiconductor part of the atom chip. The etched wires, the alloyed contact pads, the bond wires and the connections on the atom chip are visible. The size of this GaAs chip is $3 \times 3\,\mathrm{mm}^2$. On the right edge crossing wires of the multi layer atom chip are observable.

For the accomplishment of this thesis, two GaAs wafer were grown by Vladimir Umansky in his MBE at the Weizmann Institute of Science. An approximately one micron thick conducting layer is grown below the surface. The details of these wafer are listed in Appendix C.5.

6.7 Micro–optic atom chips

The fibre atom chip is a joint venture with the optoelectronics group of Prof. K. – H. Brenner from the computer engineering centre of the University of Mannheim. One field of research of his group is micro–optics [Liu05, Wil06a]. The basic atom chip is build in the Weizmann Institute of Science. This atom chip is shipped to Mannheim, where holders for optical fibres are fabricated onto its surface. This atom chip not only combines microelectronics with atom physics, it also implements micro–optics.

Optical fibres consist of a core, which guides light. A surrounding cladding holds the core and the cladding is protected by a surrounding plastic coating. Fibres used on these atom

[10]Vacseal VS–301–B, Huntington, Mountain View,CA, USA, usually used to close holes in vacuum chambers.

chips have a core with a diameter of 4.9 μm, a cladding of 125 μm and the coating is 250 μm in diametre. By integrating optical fibres onto the atom chip, single atoms are going to be detected with it [Haa06]. Two fibres are either aligned facing each other or perpendicular to each other. Figure 6.20 shows mounted fibres on an atom chip held by $SU - 8$ resist[11] structures. Facing fibres build cavities or detect a passing atom by the change of the coupled light. To reach higher finesse, different mirrors in the fibre and on the fibre tips are checked. With perpendicular fibres, one fibre illuminates an atom, while the second fibre guides the fluorescence light to a detector.

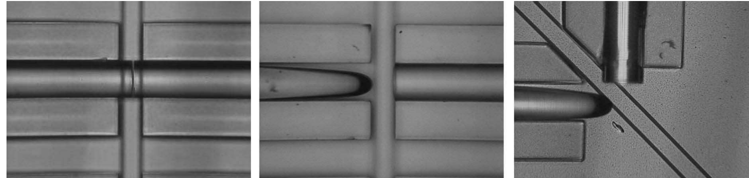

Figure 6.20: Light microscope photos of optical fibres mounted on an atom chip. The fibres have a radius of 62.5 μm. They are held by SU–8 structures. A 50 μm wide wire is fabricated between the fibres to guide the atoms to the place of detection. left: Two polished fibres facing each other with a gap of a few μm between them. These micro cavities reach finesses up to several 1000.middle: A tapered fibre points to a polished fibre, to couple light directly into it. right: A tapered fibre is mounted perpendicular to a polished fibre. The tapered fibre illuminates a narrow line. Each illuminated atom fluoresces light, which is partly caught by the second fibre and guided to a detector.

Some pads in the design of the fibre atom chip are moved or reduced in their width (see layout Figure C.5 in the appendix). The fibres lead away on the surface of the atom chip. In their place no bond wire contacts can be set. To avoid shorts caused by the fibres, they are mounted on grounded surfaces and do not cross wires.

6.7.1 Fabrication of SU–8 fibre holders on an atom chip

Fabrication of the fibre holders is done by Xiyuan Liu in Mannheim. The atom chip is covered with SU–8 resist. This resist is photosensitive and thick compared to the resists previously used for lithography. The thickness of the SU–8 resist requires a big fabrication edge around the atom chip and preferably a squared sample size. Therefore the fabrication edge is not cut off, before the atom chip is send to Mannheim. The sample size is even enlarged to $5 \times 5\,\text{cm}^2$. The SU–8 is exposed accurately by laser light of a wavelength between 365 – 436 nm. After developing and baking the atom chip contains huge SU–8 resist structures, with very straight edges. The SU–8 resist pattern is designed, to hold optical fibres in accurate positions (better than 1 few 100 nm). The height of these structures is $\sim 90\,\mu$m. The end of the fibre is polished, and the coating is stripped off with a mechanic stripper. This reduces the height of the core above the atom chip, when the fibre is put onto it. The cladding without the coating is fragile and is handled with care. After removing the coating the radius of an optical fibre is 62.5 μm. The fibre is pushed into the SU–8 holders, which have exactly the right size to fix the fibre. Figure 6.21 shows an atom chip with optical fibres mounted on it.

The alignment of two fibres held by SU-8 structures is sufficiently good to build a cavity between them. With external optical cavities, trapped atoms have been detected successfully

[11] SU–8 resist, MicroChem Corp., Newton, USA.

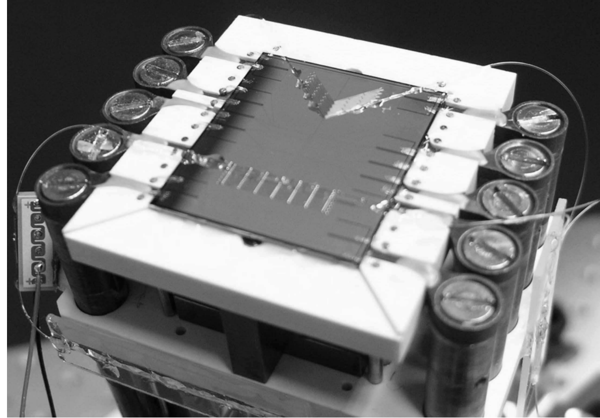

Figure 6.21: This photo shows atom chip $E_d III_{Si}$ with fibres attached to it. The photo is taken just before the mounting is moved into the experiment. The structures on the atom chip are the SU–8 resist patterns, which hold the optical fibres. At the edge of the mounting the optical fibres are visible.

in this group [Haa05]. They are replaced by the atom chip shown in Figure 6.21. Trapping atoms on this atom chip and detecting them with the mounted fibres is in progress currently [Sch04b, Wil06b, Wil07, Hei08].

To align the SU–8 structures with respect to the wire pattern on the atom chip special alignment markings were designed. These are rings with decreasing width and increasing diameter around one point. One of these Fresnel zone plates is on the atom chip and one is on the mask to simplify the alignment. Slightly shifted against each other a line pattern appears perpendicular to the misaligned direction. Nevertheless, Fresnel zone plates are not recommended, as the rings fall of during lift–off and they appear to stick on the surface of the atom chip. Here they shorten wires and scatter light. Figure 6.22 shows lithographically patterned alignment Fresnel zone plates and rings, that stick on the surface.

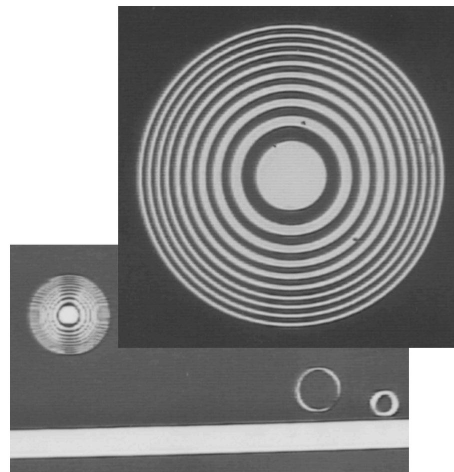

Figure 6.22: top: A photo of a lithographically patterned Fresnel zone plate on a fibre atom chip for SU–8 alignment. Its total diameter is 150 μm, the outer ring and its gap are 4 μm wide. bottom: Photo of a Fresnel zone plate on a fibre atom chip with rings sticking close to it. These rings fell off during lift–off and stuck to the surface.

6.7.2 Mounting optical fibres with SU–8 holders onto an atom chip

Before mounting the fibre onto the atom chip, fibre and atom chip are prepared separately. The SU–8 resist structures are fabricated on the atom chip. The coating of the fibre is stripped of, the tip is polished and covered with a mirror or tapered. A tapered fibre is a fibre which gets narrower to its tip. A lens like behaviour can be realised this way. If a mirror is fabricated inside the fibre or on its tip, this is also done before mounting the fibre onto the atom chip.

The stripped fibre is fragile. It is pushed softly into the SU–8 pattern, which holds it in the desired place. A picture of a fibre held by SU–8 is shown in Figure 6.23. The second fibre is mounted and in case of two fibres facing each other the alignment is checked by shining light through the fibres. The alignment can slightly be modified by pushing and rotating the fibre. In the end the fibres are fixed in their holders with vacuum compatible UV–glue.

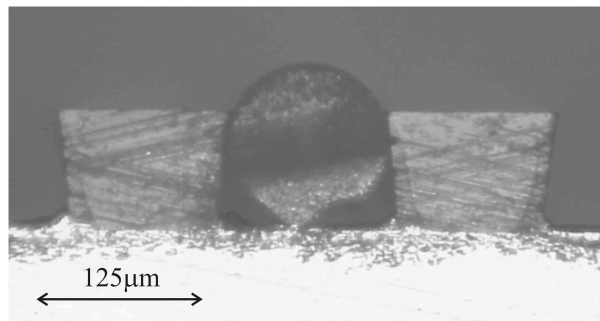

Figure 6.23: View onto the tip of a fibre, hold by two SU–8 resist patterns. The SU–8 structures are slightly taller, than the radius of the fibre. A slight undercut in the SU–8 holds the fibre in a fixed position on the surface of the atom chip.

6.8 Focussed ion beam patterned atom chips – FIB

For one experiment, a fully fabricated atom chip was further nano–manufactured with a focussed ion beam (FIB) [Pie06]. This was done by Henry J. Lezec from the ISIS at the Université Louis Pasteur de Strasbourg, France. In a FIB gallium ions are accelerated and focussed onto a spot on the sample. The ions cut the material with a precision of 20 nm. Wires on the atom chip BXV_{Si} (2.5 μm thick gold wires) were cut this way. Figure 6.24 shows some of the FIB patterned areas of this atom chip. With the FIB wires on the atom chip were cut, structured and polished. This is possible due to the high accuracy of the FIB.

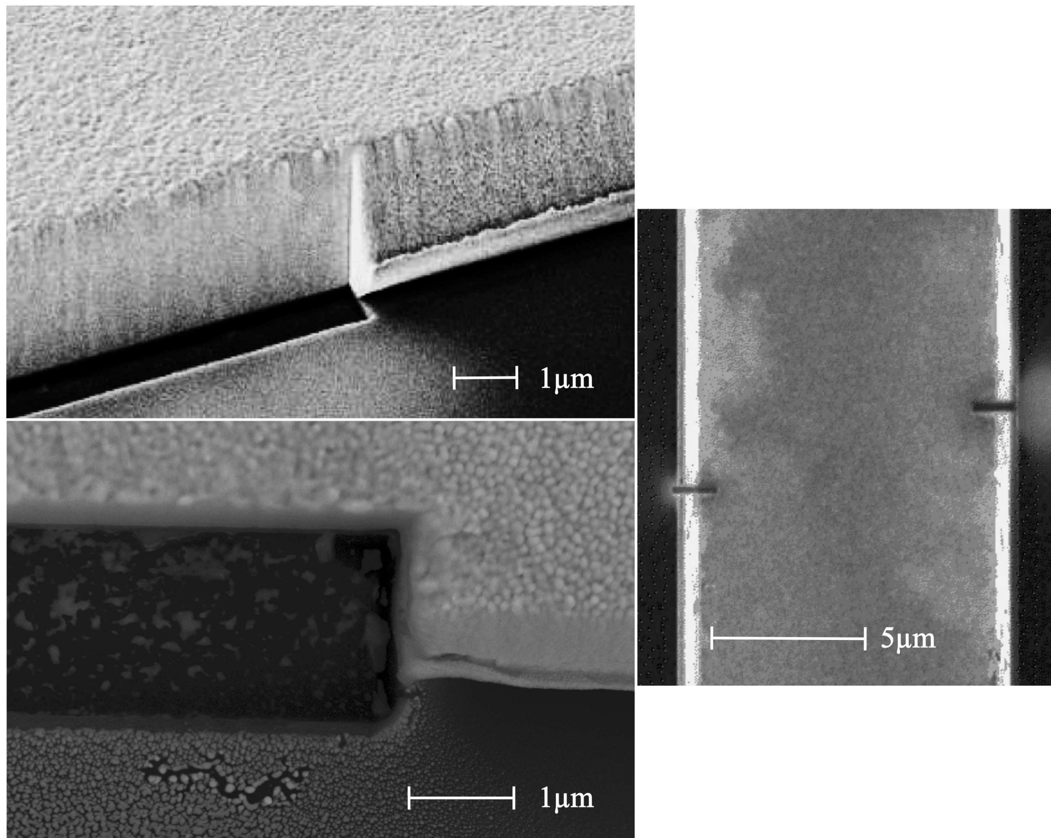

Figure 6.24: SEM picture of the FIB patterned atom chip B XV$_{Si}$. left: The edge of a wire is partly polished by removing the edge with high precession. top: View from the side. The left side is polished by FIB while the right side is the original edge of the lithographically fabricated wire. bottom: View from top onto the same area. right: The shape of a wire is modified by cutting two small gaps into it. At these places the current flow through the wire will slightly change its direction. This modulates the created magnetic potential for trapped atoms.

Chapter 7

Thermal properties of atom chips

The thermal properties of an atom chip are crucial for the experiment. The trapping potential becomes larger and the gets steeper the more current is pushed through a wire. The current density in a wire defines the magnetic field gradient of the trap (see Section 2.4). The total amount of current and the current density are limited by the thermal conductance of the wire because of electric heating. The heat has to be guided away to prevent the wire from burning. Reflectivity and cleanliness of the atom chip are important too. A simple surface quality check is done all the time during fabrication by eye and in the end in SEM and AFM microscopes. The real optical properties are quantified in the experiment. Even a slightly scattering surface does not cause trouble. The electric properties are more important. Bad electric features prevent an atom chip from being used in an experiment, because it would burn inside the experiment. To prevent a wire from burning inside the experiment, test measurements are done. A special atom chip design was developed for these tests. This chapter introduces the test measurements and shows the results of these measurements. They can be used as orientation for the wire layout of new atom chips and as guideline for atom chips inside the experiments. Some of the results are published in [Gro04].

7.1 Test measurements

In the previous chapters, the fabrication of atom chips was described. The completed atom chip is mounted and installed into the experiment. In the experiment, atoms are trapped in electro–magnetic potentials on the atom chip. These potentials are created by currents, pushed through the wires of the atom chip (see Section 2.4). The possibilities of an experiment rise with the amount of current, which can be pushed through the wires. An important question is, how much current does a wire stand? At a certain point, it will overheat and burn. This has to be avoided, as it destroys the experiment permanently. A burned wire is broken and the area around it is damaged too. The hot metal splashes away, contaminates the surface and possibly shortens nearby wires. Burned wires are shown in Figure 7.1.

A destroyed atom chip is a catastrophe for an experiment. It has to be avoided in any case, as the atom chip has to be exchanged. This takes a lot of time in which the experiment does not work. Maybe even a new atom chip has to be prepared. Changing the atom chip with a new mounting takes at least one month. More probably it takes some months before the experiment delivers results again.

To explore how much current a wire can stand before it burns, a special atom chip was designed and fabricated. The test atom chip is described in the following section. The technique of test measurements is described afterwards.

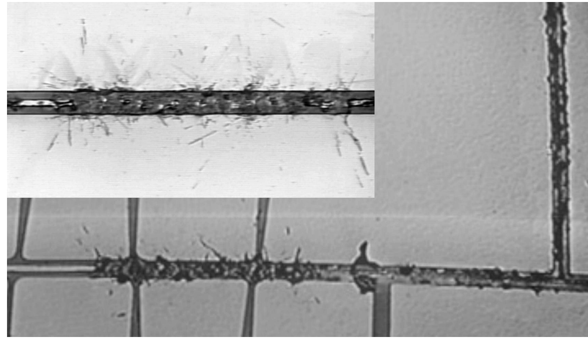

Figure 7.1: Light microscope photos of burned wires. inset: Increasing current was pushed trough this 10 μm wide wire of a test atom chip until it overheated and burned. The gold melted and spattered on the surrounding surface. big photo: A 10 μm wide wire burned on an atom chip inside the experiment. In this case the current was pushed far above the limit and it burned the wire over a long distance. Even the side arms of the wire burned. This atom chip had to be exchanged after this mistake, as it is completely destroyed.

7.1.1 The test atom chip

The best test measurement would be done on the atom chip in use. This is not possible, as the limit can not be tested out without burning wires. Having access to a number of identical atom chips would solve this problem. But for this the atom chip has to be build before the test. Also destroyed wires may influence the results on other wires close by. And some atom chips are so difficult to build, that two identical atom chips are not available.

These problems are solved with the test atom chip. The design of the test atom chip contains 12 straight wires of 2 mm length and different width. For the atom chip, which is going into the experiment and the test atom chip the same fabrication parameters are used (see Section 5). Ideally the two atom chips are evaporated at the same time next to each other. The test atom chip is build to simulate the atom chip which will enter the experiment. The test atom chip wires are heated to the limit, until they burn. This gives a benchmark for the currents limits in the wires of the atom chip in the experiment. Figure 7.2 shows the design of the test atom chip. The 12 wires have a width of 100, 50, 10, 5, 2 and 1 μm. Each wire width is fabricated on the test atom chip twice. The narrow wires are located in the middle of the design, while the wider they are, the closer to the edge they are.

This design of the test atom chip has several advantages. The length of a wire is well defined and easy to compare to all other wires, especially on other test atom chips with different height. The different wires are fabricated far away from each other (2.5 mm), to avoid influencing one another. Also after burning one wire the others are still untouched. The width of the wires are the most common widths on atom chips. The test atom chip is very easy to fabricate and delivers results before a new atom chip for the experiment is designed. This allows to design the new atom chip layout with wires which fulfill basic current requirements.

The test atom chips give good guide values for the standard atom chip in the experiment. Due to the special properties of some atom chips it is not possible to simulate them with such a test atom chip. These are especially:

- The multi–layer atom chip with its step climbing wires and bad head contact.
- The e–beam atom chip with its small wires, which are not manufacturable with optical lithography.

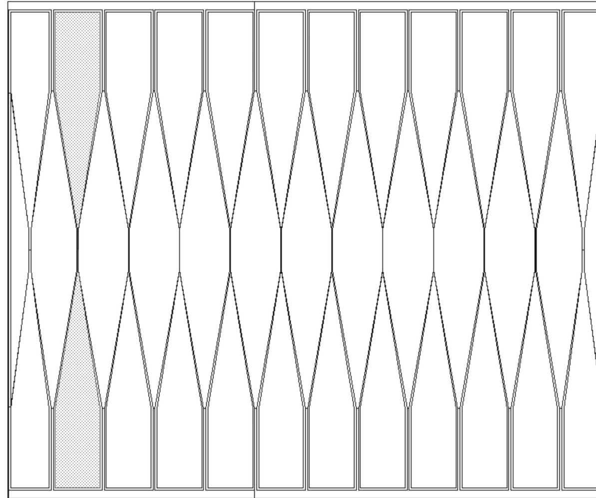

Figure 7.2: Design of the test atom chip. From left to right, the widths of the wires in the centre are: 100, 50, 10, 5, 2, 1, 1, 2, 5, 10, 50 and 100 μm. The length of each wire is 2 mm and their connection to the pads are smooth and much wider than the wires, like on atom chips for experiments.
The second wire from the left and its pads are hatched to illustrate the structure. At top and bottom the connecting pads are located, while the 2 mm long and 50 μm wide wire is connecting them in the middle. Twelve of these structures are fabricated next to each other and separated by a grounded area.

- The semiconductor atom chip with its combination of materials.

The small 1 and 2 μm wide wires on the test atom chip are problematic anyway. For thick metal layers, the resolution in the lithography step is not sufficient to resolve them. On many test atom chips they do not exist. This does not present a significant problem, since on most atom chips for experiments also no optical lithography wires below 5 μm are fabricated.

Designing rules follow from measurements of test atom chips. The experimental requirements define the potentials needed. The necessary currents to create these potentials can be calculated (see Section 2.4). Either the width of the wires for this experiment is adjusted or the height of the deposited metal needs to be at least a certain height to stand the current.

Test atom chips are also used to explore new materials. Different metal films are evaporated on different test atom chip substrates. The results of the measurements are compared, to find a combination of metal and substrate which fit the purposes of an experiment the best. After explaining the measurements results of the test atom chip measurements will be shown in the following sections.

7.1.2 Measuring test atom chips

First the resistances of the wires on an atom chip are measured using a multimeter. This gives a guideline. Also the resistances between wires are checked this way to detect shorts between wires. It is a tedious work to measure 36 contacts (in the new design) against each other.

For more significant measurements the time evolution of the resistance of a wire is observed. Therefore the voltage drop is measured while a constant current is pushed through the wire. These measurements are done in a moderate vacuum of 10^{-6} mbar to simulate an experiment–like environment. The measurements are performed in a pulsed manner to allow

the wire and the atom chip time to cool between two measurements. For measurement without observed heating the time between two measurements is about 10 seconds. The cooling time for hot atom chips can be tested by redoing the same measurement. If the measurement did not reproduce the previous result, the atom chip probably has not had enough time to reach room temperature.

In the beginning the resistance measurement was done by a two point measurement. Here the voltage drop of the wire including its connections is measured. In a four point measurement the current is pushed through the wire and two separate needles connect the wire on both sides (one for the current, one for the voltage). This allows to measure the voltage without the connections. The resistance is given by Ohms law. The ideal measurement would be a Wheatstone bridge [Chr33, Whe43] or a compensator circuit [Wag04b]. In the four point measurement current and voltage are measured with an error in the current, as the current flows through the chip wire and the voltage measurement device. This error is small, as long as the resistance of the wire is much smaller than the resistance of the voltage measurement device. The resistances of wires on atom chips are ~ 1 to 1000 Ohm, while the resistance of the voltage measurement device is much higher ($\sim 20\,\mathrm{M}\Omega$). The resulting error in the current measurement is thus less than 1%.

For all wires, a resistance rise of less than 50% was taken as the limit, if the wire was to be used for other purposes afterwards. This was controlled by the amount of current and the duration of the pulse. The rise of less than 50% proved to be save value. After stronger heating, the measurements were partly irreproducible or the wire was destroyed (see Figure 7.1).

7.2 Material properties

The substrates and wire metals used for atom chip fabrication behave differently due to their properties. Some of them are listed in Table D.1 in Appendix D. The thermal and electrical properties of the materials are the most interesting for atom chips. The thermal heat conductivity and the specific heat capacity of the materials used in atom chip fabrication are displayed in Figure 7.3.

The wires on atom chips are fabricated from gold (see Chapter 5). Figure 7.3 shows that silver and copper have better heat conductivity and capacity than gold. Also their electrical resistivity is lower than the one of gold. The advantage of gold is that it is inert and very pure. It is also very well known and easy to process. The Weizmann Institute of Science has long–running experience using gold and the facility is arranged for gold fabrication. The resistivity of gold is sufficient for atom chip experiments, since it allows current densities of more than $1 \times 10^7 \mathrm{A/cm^2}$ with the used fabrication technique and does not react with the rest gas in the UHV chamber, it builds straight edges and surfaces and the reflectivity for the used laser light of 780 nm is high.

As substrate for atom chips Si is used. The disadvantage of GaAs is its fragility. The heat conductivity of Si was further increased by doping the substrate (see Section 5.2). The drawback of Si is its SiO_2 layer which insulates the wires from the substrate. Different substrates are researched and compared in the next paragraphs. In the mounting the atom chip is located on macor or shapal (see Figure 4.1). The heat transport from the atom chip to the solid copper through the glass ceramic was strongly increased when the macor was exchanged against shapal. The polyimide separation layer on a multi–layer atom chip has a bad heat conductivity.

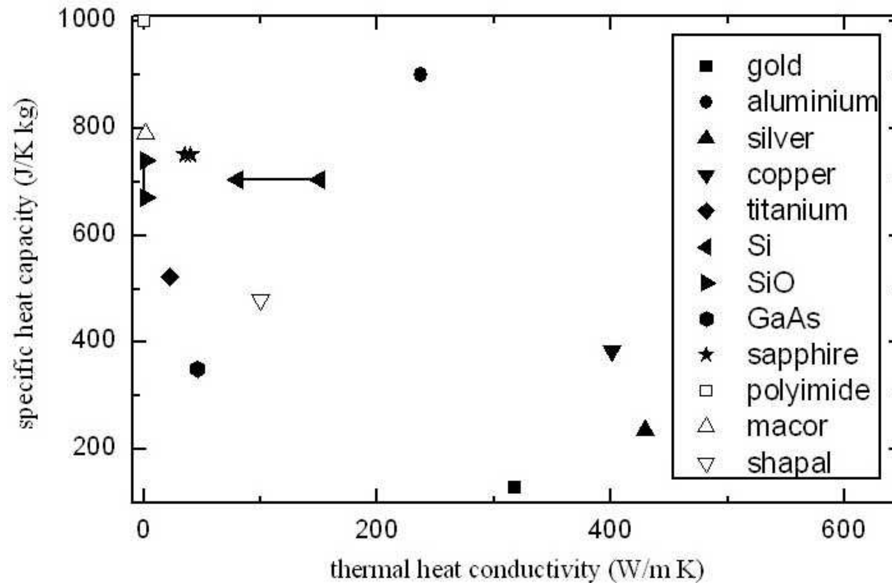

Figure 7.3: The thermal heat conductivity and the specific heat capacity of the materials used during fabrication or in the mounting are plotted. The values are listed in Table D.1 (see Appendix D). The thermal heat conductivity of Si and sapphire, as well as the specific heat capacity of SiO_2 vary in the plotted range. The given values are the thermal heat conductivity between 0 and 100°C and the specific heat capacity at 25°C.

7.3 Heat transport

Wires on an atom chip burn, when they overheat. The heat generated in a wire is equal to the power in the electric circuit: $P = UI$.

The gold wire is heated and the heat dissipates through the SiO_2 layer into the Si substrate. The resistance of the wire changes with temperature. If the heat is not transported into the substrate fast enough, the wire burns. This also happens when the substrate becomes hot and not able to take heat from the wire anymore. The second case has not been observed during this thesis. All wires burned because the heat could not be transferred from the wire to the substrate fast enough.

7.3.1 Wire heating measurements

The temperature change of a wire has a linear relation to its resistance change. This is valid for gold in the observed temperature range from 250 to 600 K. The temperature coefficient of gold is $\alpha \approx 4 \times 10^{-3}$/K [Mat79]. A heating measurement of a wire under moderate vacuum conditions of 10^{-6} mbar is shown in the inset of Figure 7.4. The resistance plotted linearly versus time shows fast heating and a slow saturation over seconds.

In the logarithmic time plot the resistance does not saturate (see Figure 7.4). Even after long periods the temperature in the wire is still rising. The heat produced inside the wire can not be transported away completely. This is due to a heating process of the substrate. The heat produced inside the wire is transported through the insulation layer (SiO_2 in case of an Si substrate) into the substrate. The substrate is heated and leads the heat away. The hotter the substrate, the less heat it can take from the wire.

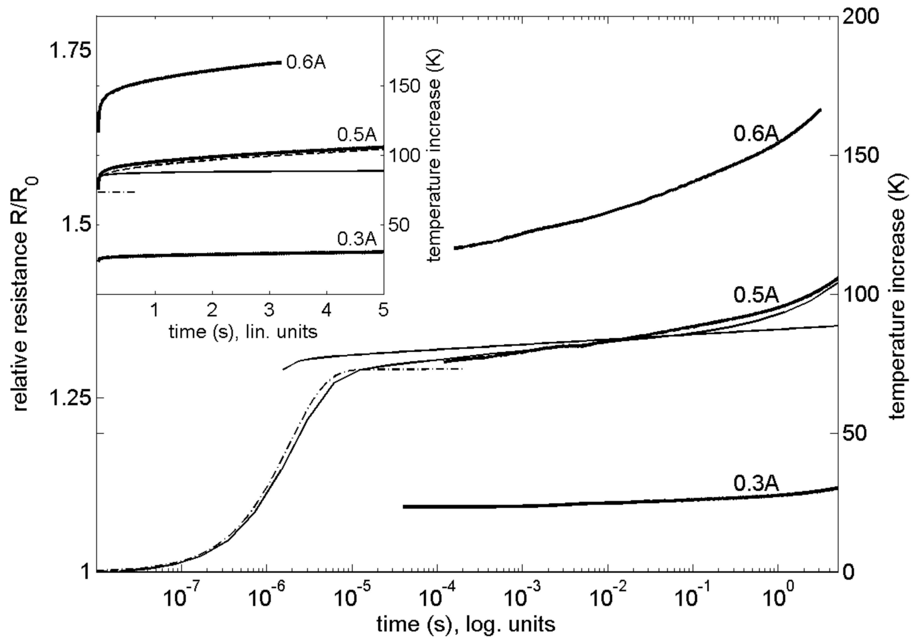

Figure 7.4: The temperature evolution of a 5 μm wide wire on the test atom chip B III_{Si} is plotted for 0.3, 0.5 and 0.6 A current pulses of 10 seconds on a logarithmic and in the inset on a linear timescale. The height of the gold is 1.4 μm, and the substrate is Si with a 500 nm thick SiO_2 insulation layer. The change of the resistance and the change of the temperature of the wire are plotted versus time.
For 0.5 A the data are simulated. The simulation fits the data good without fitting parameters. The dashed–dotted line shows the fast temperature increase, while the thin solid line is the analytical model for the long time heating. It only holds as long, as the approximation of the half space model for the substrate is valid. A 2D numerical model indicated by the dashed curve fits the measurement accurately.

Wires on polyimide

The heat measurements with wires on polyimide were done with a simple current supply, without measuring the time dependence. Better equipment has not been available for this measurement. A burned wire is visible in Figure 7.5.

On this test sample the polyimide has a thickness of 510 nm. This is comparable to the separation layers on multi–layer atom chips. The evaporated gold, which climbs the polyimide has a height of 1.15 μm. Both 10 μm wide reference wires did not show heating up to 0.7 A. Their resistance is about 40 Ω.

The thin 10 μm wide wire on top of the polyimide burned at 0.7 A. At 0.6 A it showed 20% heating. The save value of 50% resistance increase for standard fabricated wires are not true for wires fabricated on polyimide. Figure 7.5 shows, that the wire burned in the middle of the polyimide. In this place the heat transport is worst, because the distance to the heat sink is longest. In this place the wire reaches its highest temperature and burns.

It also could have been that the wire burned at its thinnest place. The cross section of the wire is reduced in the place, where it climbs the polyimide. The current density is higher than in the rest of the wire (see Figure 6.7). But the wire did not burn at the edge of the polyimide. The bottleneck for wires on polyimide is the heat transport to the heat sink. Therefore the distance a wire is fabricated on top of polyimide has to be designed as short

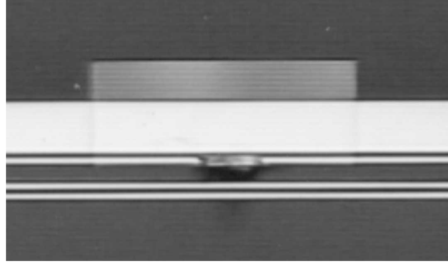

Figure 7.5: Four wires are fabricated on sample E_dS X_{SI}. The two wires on top are partly fabricated on polyimide which is fractionally visible above them. The lower 10 μm wide wire burned in the middle of the polyimide. The 100 μm wide wire did not burn at the maximum current of $\sim$ 2A for 15 seconds, but it became hot. The two 10 μm wide wires at the bottom are fabricated for reference.

as possible.

The 100 μm wide wire did not burn. It could stand 1.88 A for more than 15 seconds. The sample was located on a plastic box to avoid heat transport away from the substrate. The cold resistance of this wire is 6.7 Ω. The resistance after turning on 1.88 A is 7.3 Ω and during 15 seconds it rises to $\sim$ 11 Ω. This is equivalent to an temperature rise inside the wire of $\sim$ 380°C. The whole sample became so hot that it merged with the plastic box on which it was lying.

7.3.2 Sub–micron wires

Test measurements on sub–micron wires were done without heating the wires. An atom chip to destroy during test measurements has not been available, as the fabrication process of e–beam structured atom chips is difficult. Also every e–beam patterned atom chip layout is different. The cold resistances of the wires on a sub–micron structured atom chip (atom chip E_fIV_{Si}) have been measured. Like on the other multi–layer atom chips, the resistance of the tall wires on top of the polyimide is in the order of 50 and 7 Ω for 10 and 100 μm wide wires respectively. The resistance of $\sim$ 200 μm long and 0.7 μm (3 μm) wide wires is $\sim$ 400 Ω ($\sim$ 200 Ω, respectively). These values should give an orientation for further sub–micron atom chip layouts. The current density of specific wires can be calculated with the formulas given in the next section.

7.3.3 Semiconducting wires

Two semiconducting atom chips have been fabricated successfully during this thesis. None of them was destroyed during test measurements, as only the cold resistance of their wires was measured. Including the bond wire contacts of the GaAs and the leads on the multi–layer atom chip, the resistance of the semiconducting wires is between 1.5 and 3 kΩ. The size of the measured wires ranges from 400 μm long, 50 μm wide to 600 μm long and 3 μm wide.

7.4 Simulation of the heating process

The heating process can be separated int a fast and a slow heating process. They have different origins and are discussed in the following paragraphs. Figure 7.4 shows measured heating data with a theoretical fit, resulting from the two simulated heating processes. In the

observed range of temperatures radiation is negligible and performing the same measurement in vacuum or in ambiance pressure yields identical results.

Both heating processes depend on the heat flow from the wire (width W and height H) with the current density $j = I/WH$ to the substrate. The heat dissipates through the contact between wire and substrate. The contact resistivity (thermal conductance k) together with the heat conductivity λ of the substrate and its heat capacity per volume C determine the heat transport. Two temperature transport processes with different timescales result form this. A fast and a slow heating process.

7.4.1 Fast wire heating

The fast wire heating process can be seen in Figure 7.4. The initial resistance and temperature of the wire is not the cold resistance/ room temperature. A heating process took place before the first data point of the measurement was taken. The first heating process is not resolved, thus it has to be faster than the time resolution of the measurement which is $\sim 100\,\mu$s.

This fast process is the heat flow from the wire through the insulation layer to the substrate. It is given by:

$$\tau = \frac{C_w H}{k - Hj^2\alpha\rho}\,. \tag{7.1}$$

With the heat capacity (per volume) C_w of the wire, and ρ its cold resistivity at room temperature. For a standard atom chip, with gold wires, an Ti adhesion layer and a SiO_2 insulation on a Si substrate, the time scale of this process is in the range of 1μs. This leads to an quasi instant equalisation of the temperature difference between the wire and the substrate. The temperature difference is:

$$\Delta T_f(t) = \frac{H\rho j^2}{k - Hj^2\alpha\rho}(1 - e^{-t/\tau})\,. \tag{7.2}$$

This holds as long as the current density does not exceeds the limit of $j = \sqrt{k/H\alpha\rho}$. For higher current densities an exponential rise of the temperature inside the wire will destroy it almost instantaneously. In fact in the test measurements many wires burned immediately, while burning wires have never be observed during the test measurements. All wires either survived the test measurement or burned in the moment when the current was switched on.

7.4.2 Slow wire heating

The fast heating process is followed by a slow rise of the temperature during the time of the current pulse. This is the slow heating process, which describes the heat transport inside the substrate. The heat produced in the wire and transported through the isolation (described by the fast heating process) is distributed into the substrate. This time scale is in the order of $\sim 1\,$ms.

The slow wire heating process is observed all over the time of the current pulse inside the wire. This heating behavior can be simulated with a two dimensional model of a line like heat source on the surface of a half space substrate. Neglecting the temperature dependance of the resistivity the temperature increase $\Delta T_s(t)$ is given by the incomplete Γ function:

$$\Delta T_s(t) = \frac{HW}{2}\frac{\rho j^2}{\pi\lambda}\Gamma\left(0, \frac{CW^2}{4\pi^2\lambda t}\right) \approx \frac{\rho I j}{2\pi\lambda}\ln\left(\frac{4\pi^2\lambda t}{CW^2}\right)\,. \tag{7.3}$$

This model estimates the substrate as a half space heat sink. The real substrate is about $700\,\mu$m thick. For times longer than $\sim 100\,$ms the heat transport from the substrate into

the mounting has to be taken into account too. In Figure 7.4 the slow heating process (thin solid line) does not describe the data for times longer than a few 100 ms. This is only done by a 2D numerical calculation (dashed line), which accurately reproduces the data.

7.4.3 Wire width

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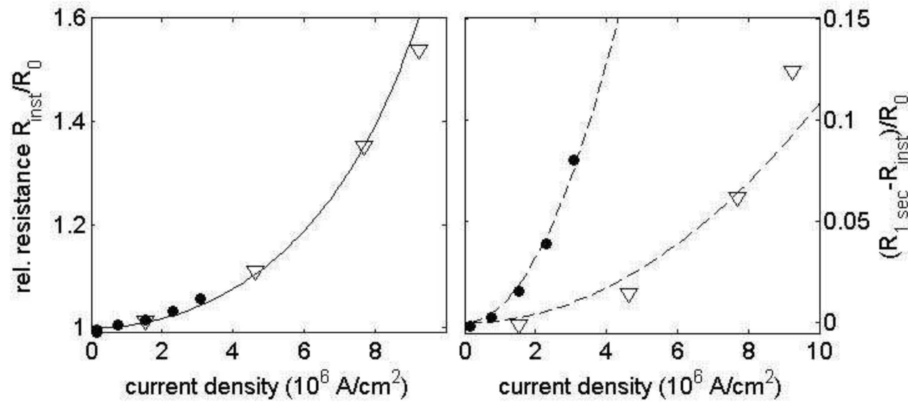

Figure 7.6: left: The instant heating (after 300 μs) of a narrow 5 μm (▽) wide wire is the same as the heating of a 50 μm (•) wide wire with the same current density. The theoretical model for fast heating (solid line) does not depend on the wire width, only on the current density. The model fits the data well and does not use any fitting parameters. right: For long time heating (after 1 second), the wire width influences the temperature. More heat is dissipated into the substrate when the same current density floats through a wider wire with the same height. The slow heating model (dashed lines) describes the heating of the wires well. These two wires are fabricated on the atom chip B III and are 1.4 μm tall.

Comparing equal current density, the immediate heating of a wire is independent on its width (see Figure 7.6). On a long time scale small wires do not heat as much as wide wires. This is due to the total amount of heat transported to the substrate. A higher current is flowing in a wide wire to achieve the same current density as in a narrow one. Therefore the produced heat is higher and the substrate heats up faster.

The size of the intersection between the wire and the substrate is defined by the width of the wire. The wider the wire, the larger the intersection. The heat transport of the fast process (see Equation 7.2) takes place faster. Therefore a wide wire can stand more current than a narrow one with the same cross section. But wide wires limit the distance of the trapped atom cloud to the wire in the experiment due to the finite size effect (see Section 2.5.1).

7.5 Different substrates

The temperature dependence of the wire depends on the thermal properties of the substrate. Thermal properties of the used materials are listed in Table D.1 in Appendix D. Measurements of different substrates are shown in Figure 7.7. The fast heating process depends on

the thermal contact resistance k from the wire to the substrate (see Equation 7.2). For the data fits of the fast heating process the thermal conductances of the test atom chips were obtained from the data.

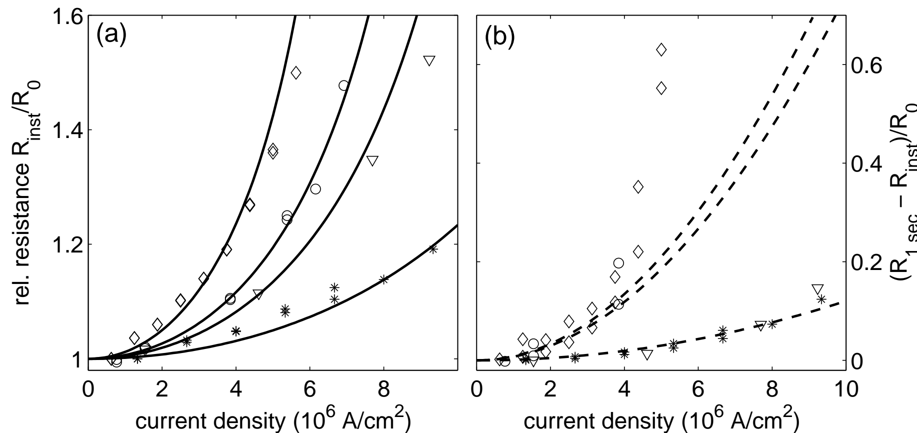

Figure 7.7: Different materials are researched as substrate for atom chips. Heating of $5\,\mu$m wide Au wires fabricated on a commercial GaAs wafer ($\diamond$), sapphire without isolation layer ($\circ$), and Si substrates with a 500 nm ($\bigtriangledown$) and a 25 nm ($*$) thick isolation layers. The heights of the gold wires are $1.4\,\mu$m (Si), $2.6\,\mu$m (sapphire) and $3.2\,\mu$m (GaAs). left: The prediction of the model for the fast process (solid lines) is compared to the wire resistances (in units of their respective cold resistance R_0) measured a few ms after the beginning of a current pulse. The thermal contact resistance ($k \sim 10^6$W/Km^2) was used as a fitting parameter. right: The slow heating process data are taken after 1 second of current flow. No fitting parameters were used to compare the model (dashed lines) to the measured data. The temperature rise of the GaAs and sapphire samples above a current density of 4×10^6 A/cm results from the limited size of the substrate.
Both figures confirm, Si to be the best substrate for atom chips, preferable with a thin SiO_2 layer.

This heat measurement has been carried out with four atom chips. GaAs 32 is a test atom chip on a GaAs substrate, which is covered with a SiO_2 layer for insulation. The height of the gold wires is $3.2\,\mu$m. The thermal conductance of this atom chip is 2.3×10^6 W/K m^2. One test atom chip has a sapphire substrate, where the sapphire itself acts as a insulator. The height of the gold wires on this test atom chip is $2.6\,\mu$m. The thermal conductance resulting from the data is 3.5×10^6 W/K m^2. For the test atom chips C II_{Si} and B III_{Si} on Si/ SiO_2 k is 6.5 and 2.6×10^6 W/K m^2 for 25 and 500 nm SiO_2 layer respectively.

Figure 7.7 shows, that Si is the best suitable substrate for atom chips. For the fast heating process the thickness of the insulating SiO_2 layer on the Si is important. The GaAs substrate is worst while sapphire is a little better. The Si substrate with the thick SiO_2 layer is a little better than GaAs and sapphire. A wire on top of a thin SiO_2 layer on a Si substrate heats up least.

Also for the long time heating Si is the best suiting substrate for atom chips. While the GaAs and sapphire atom chips heat up similarly intense, both Si substrates heat up equally less. The slow heating is not affected by the thickness of the insulating SiO_2 layer. It only affects the fast process, which is always equalised on the time scale of the slow heating process. Comparing the temperature rise on the long time scale, Si is better than GaAs and sapphire, because the heat conductivity of Si is 2 to 4 times larger than the of GaAs and

sapphire.

The theoretical models fit the data very well. Only in the long time scale and above 4×10^6 A/cm^2 GaAs and sapphire heat faster than the model . This again is due to the assumption in the model that the substrate is a half space heat sink. In the experiment the heat capacity of the substrate is limited and this effect causes the rise of the temperature above the prediction of the model for high current densities.

Chapter 8

Experiments with atom chips

The atom chips fabricated during this thesis supported all atom chip experiments of this group. Many diploma thesis and dissertations were finished successfully with results of the atom chips fabricated during this thesis. Still researchers are working on their theses (finished: [Bec02, Gim02, Kle02, Wil02, Hau03, vH03, Kas03a, Bru04, Hal04, Hof04, Krü04, Wag04a, Huf05, Sch05a, Wil05a, Rot06, Wic06] to be finished: [Fis06, Aig07, Bau07, Hof07, Kol07, Pie07, Wil07, Göb07, Hei08, vH08, Man09]). More experiments with even more people continuing to work with the atom chips of this thesis or the knowledge gained from it will follow.

In this chapter some of the results of the experiments using atom chips fabricated during this thesis are introduced.

8.1 The ^{7}Lithium experiment

One of the first experiments using atom chips fabricated during this thesis has been the ^{7}Lithium experiment. In the mean time this experiment has been modified to the combined Li/ Rb experiment. The achieved results are mentioned. In detail these experiments are explained in the theses of [Wil02, Bru04].

8.1.1 Two wire atom guide

Two wires with a bias field perpendicular to the plane of the wires, builds a magnetic trap. The direction of the wires in their plane is free (see Section 2.4.4). This configuration has been used to build an omnidirectional atom guide. A guide in the shape of a spiral was designed and fabricated on the atom chips B VII_{Si} and Al_2O_3 II. The second one has a sapphire substrate. Figure 8.1 shows pictures of atoms guided in the spiral shaped guide.

This experiment demonstrated, that atoms can be moved arbitrarily in the atom chip plane. Two publications resulted from this topic [Luo04, Bru05].

8.1.2 Electrostatic atom manipulation

In the ^{7}Lithium experiment atoms were also manipulated electrically [Krü03]. Figure 8.2 shows pictures of this experiment. The theory is described in Section 2.4.5 and in detail in [Kle02]. In this specific experiment an atom cloud was split, by charging electrical pads close to the side guide.

The electric pads are charged with $\sim 300\,\text{V}$ in case of a Si substrate and with $\sim 500\,\text{V}$ on the sapphire substrate. The distance between charged and grounded metal patterns is $10\,\mu\text{m}$. The technique of atom manipulation has also been used to move an atom cloud in a

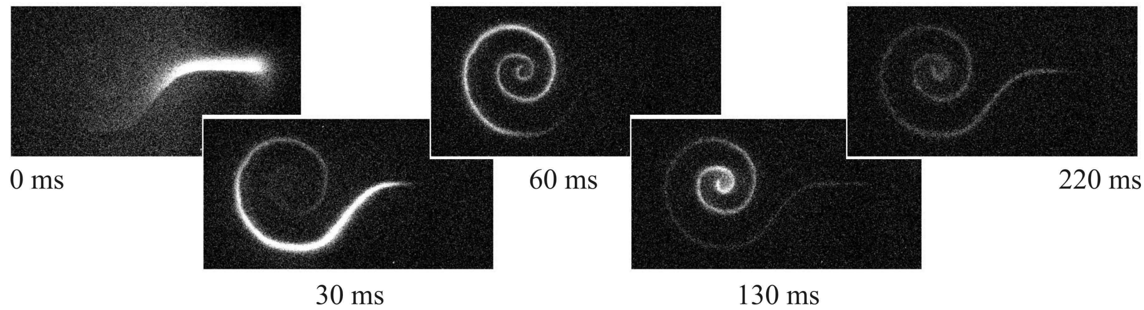

Figure 8.1: Atoms are trapped in a Z–wire trap at the right side of the small picture (0 ms). They are released and expand into the spiral guide (30 ms). After 60 ms they left the trapping region completely. About 130 ms after releasing, the atoms collect in the end of the spiral guide, where they are reflected. Finally the atoms distribute equally along the whole spiral shaped trap (220 ms).

controlled way. In principal manipulating atoms with electric charges provides an additional handle to control atoms.

8.2 The ^{40}Potassium – ^{87}Rubidium experiment

During the last year, a combined experiment was build in this UHV chamber. ^{6}Lithium fermions were cooled with a cold ^{87}Rubidium sample. The Rb bosons are cooled like in a regular experiment. It is not possible to cool fermions with this technique, as they do not rethermalise after removing the hottest atoms. The necessary S–wave scattering process is forbidden for identical fermions by the Pauli principle.

The cool bosons interact with the fermions. A temperature exchange between the cold bosons and the fermions takes place and the fermions are cooled by the bosons. The theory and first trapping tests are noted in [Huf05]. This experiment has had problems with the surface of the atom chip. These problems were solved by coating the atom chip with a SiO_2 layer (see Section 6.2).

Now this experiment is rebuild and the ^{6}Lithium will be replaced by ^{40}Potassium fermions. The advantage of potassium is, that its scattering cross section with Rb is about a magnitude higher than the one of Li. The cooling process becomes much more efficient this way.

8.3 The focused ion beam atom chip experiment

The Rubidium I experiment has been the first experiment, which produced a BEC in Heidelberg. It contains a double MOT [Sch03]. The Rb atoms are trapped and pre cooled in one MOT and transported from there to a second MOT close to the atom chip. The experiments are done on the atom chip. This technique allows better vacuum in the experimental region, as the first MOT is in a separate UHV chamber together with the dispensers. The cooled atoms are guided through a small hole to the second MOT, where the rest gas is less. Many theses were finished at this experiment [vH03, Kas03a, Wag04a, Huf05, Sch05a]. In the mean time this Rubidium I experiment changed its orientation twice. First a FIB structured atom chip (see Section 6.8) was mounted into the UHV chamber. These experiments will be discussed in the following section. This FIB atom chip was replaced by an atom chip fabricated in the group of Prof. Ron Folman, Ben–Gurion University of the Negev, Be'er Sheva, Israel.

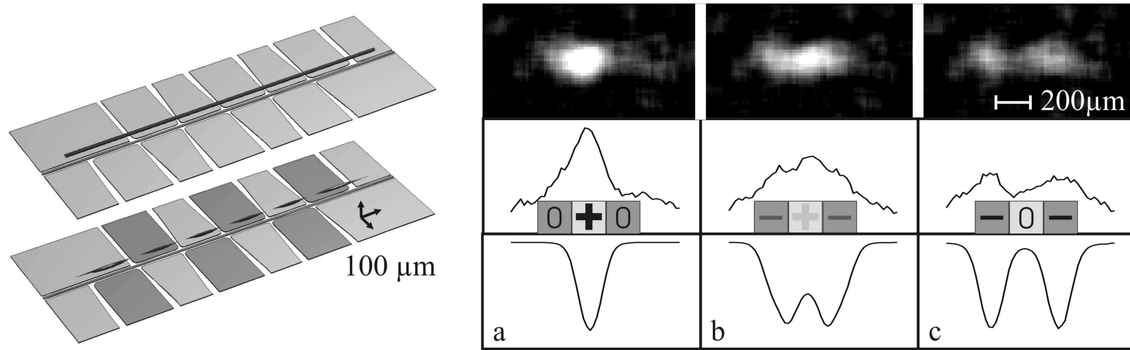

Figure 8.2: left: A side guide is modulated by adding electric fields to the trap. top: The trapping potential is calculated and plotted above the current carrying wire. bottom: the straight side guide is modulated by charging the electrical pads next to the wire. Each charged structure close to the side guide (dark grey) creates a small trapping potential from the guide.
right: The electric pads are used to split an atom cloud. The top shows pictures of the cloud, the middle the measured distribution together with the indicated charge distribution of the pads. At the bottom the calculated trapping potential is illustrated. a: One pad is charged and a cloud of atoms is trapped. b: The charge in the pad is decreased and the two pads next to this one are slightly charged. c: The middle pad is uncharged and the two next to it are completely charged. The atom cloud split into two by ramping the charges in the pads.

8.3.1 The FIB atom chip

The atom chip B XV$_{Si}$ was fabricated during this thesis at the Weizmann Institute of Science. After finishing the fabrication, it was further nano–machined with a FIB by Henry J. Lezec from the ISIS at the Université Louis Pasteur de Strasbourg, France. The results of this experiments are published in [Pie06] and will be explained in detail in [Aig07, Pie07].

Reducing disorder potentials

To reduce disorder potentials (see Section 2.7) the sides of one of the lithographically patterned wires was polished by a FIB. The precision of a FIB is < 20 nm, which is below the size of the gold grains. Figure 8.3 shows a picture of this wire. In this figure also measurements on the disorder potential of the wire are demonstrated.

About 10^5 Rb atoms are trapped in a $\sim 600\,\mu$m long quasi 1D BEC. It is kept for 300 ms in the trap. After 1.8 ms TOF a density distribution picture is taken from the expanding atom cloud. The polished part of the wire is compared to the unpolished, and the resulting disorder potential from the wire edge can be compared to the disorder potential generated by current modulations inside the wire.

A smoother potential is observed over almost the full range of measured heights. The full corrugation in the unpolished part can not be taken into account, as it is partly bigger than the chemical potential. These data are excluded from the analysis. In total, the polished wire gives a smoother potential. Here the corrugations are about a factor of two smaller. This indicates an effect of the wire edge roughness to the disorder potential of the magnetic trap.

Below a distance of $10\,\mu$m to the wire, the disorder potential generated by the edge of the wire becomes weaker compared to other effects (like bulk or top surface effects) which cause disorder too. This is conditioned by the finite size effect (see Section 2.5.1). Below the

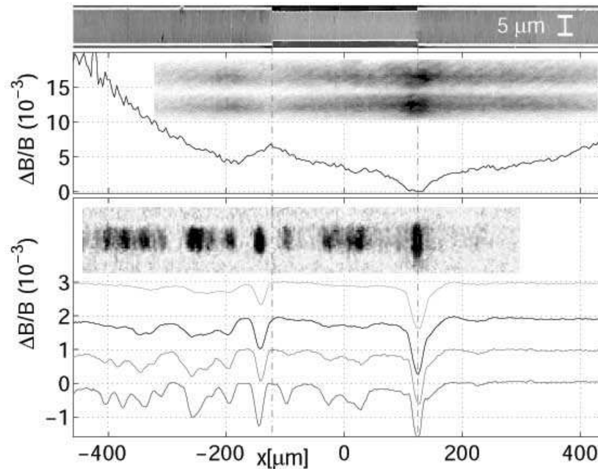

Figure 8.3: Figure of changed disorder potential by FIB polishing. top: Electron microscope picture of a 10 μm wide and 2.5 μm tall gold wire. The edges in the middle of this wire are polished with a FIB over a length of 250 μm. centre: Change (ΔB) of the magnetic field along the elongated trap in units of the total local wire field B. It was measured with thermal atoms at $z = 35\mu m$ from the surface. inset: Cloud of thermal atoms (Time Of Flight: 2ms). bottom: Measurement of the potential roughness using a 1D BEC at $z = 20$, 16, 12 and $8\mu m$ distance to the atom chip (top to bottom). The curves are interrupted where the roughness exceeds the chemical potential. inset: absorption image of a BEC around the wire's polished region at a distance of $z = 9\mu m$, and TOF=1.8 ms.

distance of the wire width, the effective size of the wire shrinks and other influences become dominant as the wire edge does not participate in the effective potential creation any more.

Surprisingly this atom chip B XV$_{Si}$ shows much more disorder than atom chip B XIV$_{Si}$ which was prepared during the same time in double–layer technique. Fragmentation of atom chip B XIV$_{Si}$ will be discussed in the next section. The stronger disorder caused by atom chip B XV$_{Si}$ could be caused by atoms deposited in the bulk material of the wire during FIB fabrication.

Building a trap

Changing the direction of the current or a change in the current density leads to spatial modulations in the potential of the trap. This is explained in Chapter 2 and can be seen in Figure 8.3. In this experiment the current density changes twice drastically. In the beginning and in the end of the polished part of the wire. With the change of the diameter of the wire also the current density changes. A reduction of the wire size causes a barrier (left in Figure 8.3) while an enlargement results in a dip (right in Figure 8.3). At the right side of the polished part atoms are collected while a second atom pool is located before the beginning of the polished region at the left.

8.4 The Rubidium II experiment

Many results were achieved with atom chip B XIV$_{Si}$ in this experiment during the the last years. Two experiments are introduced exemplarily. All measurements are described in the theses finished on the Rb II setup, using atom chips fabricated during this thesis [Bec02, Gim02, Hau03, Hal04, Hof04, Krü04, Sch05a, Wil05a].

8.4.1 Fragmentation of BECs, the atom microscope

Cold atoms are sensitive to small variations in the trapping potential. These variations can be caused by changes in the direction of the current, by current density fluctuations and by external reasons. A magnetic field variation outside the wire or an electrical charge changes the trapping potential (see Chapter 2). The cooler the trapped atoms, the more sensitive they are on changes in their trapping potential. In a wire trap the distance to the probe is important, as the disorder potential smoothes out with increasing distance. Figure 8.4 shows the dependence of the trap distance from the atom chip wire versus the current inside the wire, together with the fragmentation of the BEC in the trap. The decrease of the disorder potential with the distance to the wire is also visible in Figure 8.3.

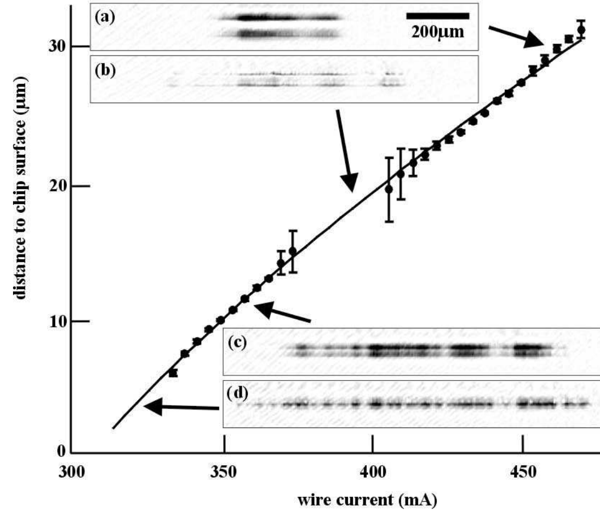

Figure 8.4: The distance of a magnetic trap from the generating wire on atom chip B XIV$_{Si}$ decreases with decreasing current in the wire. The inset pictures show the fringes of the condensate due to the disorder potential. Real fringes appear on the atom chips fabricated during this thesis at a distance around 10 μm.

In this experiment a BEC was held above a current carrying wire. The current fluctuations inside this wire were detected by the disorder behavior of the BEC. It splits into fragments according to the variations in the trapping potential caused by the current modulations of the probed wire. The BEC was moved to 28 equally spaced positions above the wire and a landscape of the magnetic field of the probed wire was measured by the atom density distribution (see figure 8.5). The current density in the probed wire could be reconstructed from the measured distribution [Wil05b, Krü05, Wil06a].

This experiment demonstrates, that disorder potentials also result from the current fluctuations in the bulk material of the wire and not only from the edge roughness, which also causes disorder as shown in Section 8.3.1.

This technique allows trapping of the analysing BEC with a second wire which is far away from the probe. The measurement is not disturbed by the trapping wire as its disorder smoothes out over the distance. This makes research of magnetic and electric properties of non current carrying samples possible. In principle the sample can be anything, that can be put close to the BEC [McG04]. The main issue is, that it has to be UHV prove.

The sensitivity of this technique depends on the measurement (for example the used atoms, the temperature of the atoms and the distance from the sample). For a ^{87}Rb BEC at

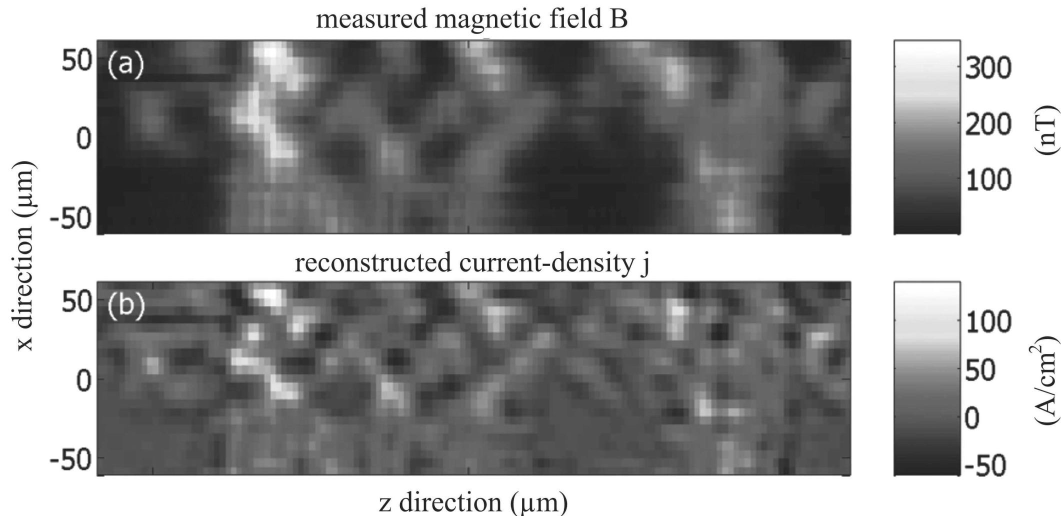

Figure 8.5: A current carrying wire on atom chip B XIV$_{Si}$ is analyzed by trapped atoms. a: Elongated BECs are moved to 28 equali spaced locations along the 100 μm wide and 3.1 μm tall wire. The current inside this wire is 340 mA. The density distribution of the atoms is similar to the magnetic field 10 μm above the wire, where the BECs are placed. b: the current density j inside the wire, is reconstructed from the measured magnetic field.

a distance of about 1 μm from the surface a sensitivity to magnetic field changes of about 1 nT is achieved. Figure 8.6 shows a plot of the sensitivity and the resolution of the BEC compared to other magnetic microscopes. The magnetic field measurement via BECs closes the gap between Hall probe measurements and the measurements with SQUID magnetometry. The results of these experiments are published in [Wil06a].

8.4.2 Coherent splitting of BECs with RF potentials

This experiment enables to realise a miniaturised matter wave interferometer. A BEC was split without perturbing its quantum evolution for the first time on an atom chip. A phase preserving matter wave beam splitter is fabricated and matter wave interference experiments are performed. First experiments are published in [Sch05b].

The operation principle of the matter wave beam splitter is illustrated in Figure 8.7. An atom trap is build with a current carrying wire and an external bias field. A second wire carries an alternating current with a RF oscillation. This RF field couples different internal magnetic states of the atoms. The distance between the state can be controlled. Overlapping states build an anti crossing which leads to a double well potential.

The BEC is smoothly split, by changing the RF current, which turns the tight magnetic trap adiabatically into a steep double well potential. The implementation of the wires on an atom chip leads to a domination of the near field, while a sufficiently strong and precisely orientated RF field is generated with a moderate current. The BEC is not excited during this operation, and the splitting distance can be controlled as well as the potential barrier between the two wells. The distance between the two wells is precisely tuned from 3 – 80 μm. The coupling between them is controlled from tunnelling till complete separation.

The atoms in the two separated wells are condensed in a BEC. Releasing the BECs from their traps causes expansion of the condensates. After a certain time of flight the expanding clouds overlap. The quantum behaviour of the BECs, with a single wave function describing

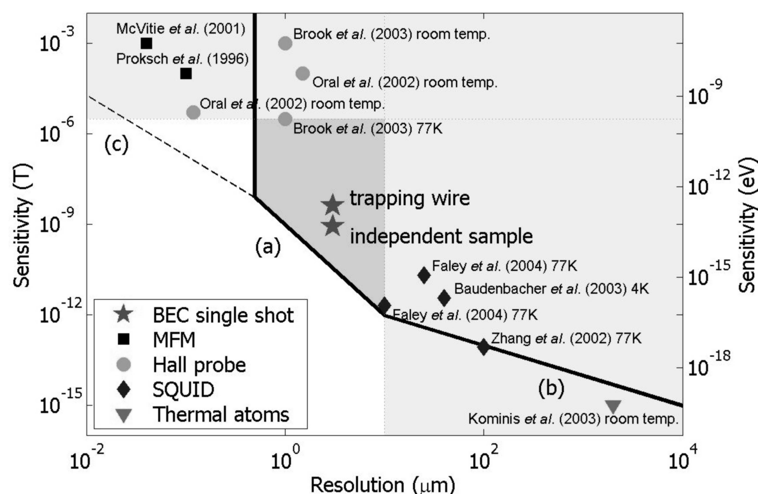

Figure 8.6: Comparison between different magnetic field measurement techniques. The potential sensitivity is plotted versus the spatial resolution. BEC measurements fill the gap between scanning Hall probes and SQUID magnetometery. The black line illustrates the theoretical limit for magnetic measurements with Rb BECs. The dark grey region indicates the sensitivity–resolution range, which is currently accessible with BEC sensors only.

the atoms, appears in the interferences which shows up in the overlapping region of the two clouds. The matter wave interference is shown in Figure 8.8.

The splitting of the BEC into two is done coherently, as a phase preservation of the phase relation is observed for interaction free condensates. Changing the order of the experiment, with the creation of a separated double well potential with a cloud of hot atoms, and cooling these atoms into two condensates afterwards, shows no phase correlation between them.

Advantages of this splitting technique are, that the distance of splitting is not limited by the structure sizes of the wires. It is limited by the size of the ground state of the initial single well potential, which can be orders of magnitude smaller than the trapping wire. The splitting process is done without exciting the trapped atoms.

This miniaturized matter wave interferometer is a highly sensitive sensor. Any kind of different interactions on the two BECs can be observed. Currently RF dressed state potentials are researched in this experiment [Hof, Les06].

8.5 The fibre atom chip experiment

Modulation of trapping potentials with light is performed in some atom chip experiments. Standing waves are generated with counter propagating laser beams, or with the use of the atom chip as a mirror (currently done in the double MOT experiment of this group). Other groups attach extra mirrors onto their AC s [Wan05].

In this experiment atoms have been detected in cavities which are not connected to an atom chip [Haa05]. Recently optical fibres have been added to an atom chip (see Section 6.7). The fibre atom chip is mounted inside the UHV chamber (see Figure 6.21) and the experiment currently delivers its first results. Atoms are detected by the fibres on the atom chip. One of the next steps will be to guide the atoms in a wire traps to fibre cavities on the atom chip, where experiments are performed. Recently this experiment published a paper about detection of neutral atoms on atom chips [Wil06b]. The fibre cavity on the atom chip

is a sensitive measurement device which can resolve distance changes with an accuracy of $\sim \lambda/400 \approx 2\,\mathrm{nm}$. Running a current in the wire between the cavity heats the atom chip. The atom chip expands and the resonant mode inside the cavity changes. Thus deformations of the substrate can be measured. This is observed by the group and will be published in [Wil07].

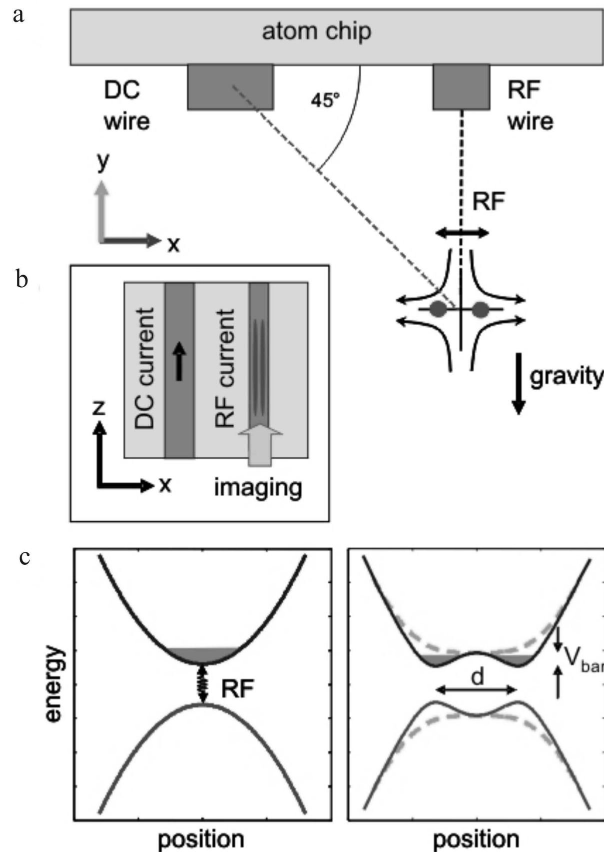

Figure 8.7: Potential splitting via a RF field. a: The left wire carries a constant current. With a rotated homogenous magnetic field Ioffe–Pritchard trap is created below a second wire. The second wire carries a RF current. The RF field splits the dc trap into a double well. b: Top view of the illustrated experiment. An elongated BEC is split by the RF field below the oscillating current carrying wire. The imaging direction is shown. c, left: The RF field couples different magnetic spin states. For simplicity only two are shown. The BEC is trapped in the upper state. right: The initial potential is split by the RF field into a double well. The BEC is split coherently into the two wells. The distance d between the new traps and the barrier height V_{bar} can be tuned precisely. The dashed line indicates the trapping potential in the y direction. It is slightly relaxed compared to the initial trapping potential.

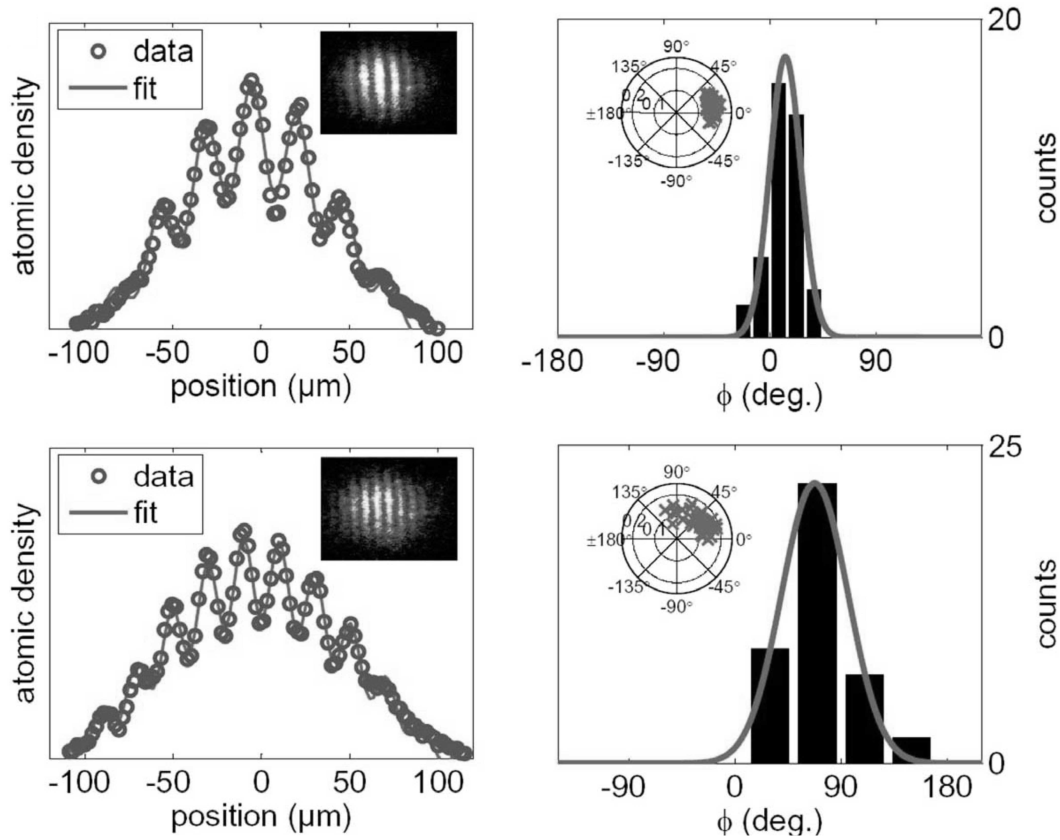

Figure 8.8: A BEC is split coherently on the atom chip B XIV$_{Si}$ as displayed in Figure 8.7. The data shown in the top line are taken directly after (~ 0.1 ms) splitting the BEC to a distance of d= 3.4μm. The trapping double well potential is extinguished fast and a time of flight picture of the interfering atom clouds is taken after 14 ms. The data from the bottom line are taken after splitting to a distance of d= $3.85\,\mu$m during 0.8 ms and TOF of 14 ms. The left side shows the atomic density distribution dependance form the position. This distribution is fit with a cosine function with a gaussian envelope. The data are taken from pictures like shown in the insets. The right figures show the narrow distributions of the differential phase of the two condensates. The same experiment was realized 40 times for the short and the long separation. Both show narrow phase distributions of 13 deg. and 28 deg. respectively. These phase spreads are significantly smaller, than what is expected for a random phase distribution. The insets show a polar diagram of contrast and relative phase for these 40 measurements.

Chapter 9

Summary and outlook

During this thesis new atom chips for quantum optic experiments with neutral atoms were developed. These new developed atom chips have been fabricated and analysed to determine their properties for the desired experiments. Requirements of the atom chips are UHV compatibility, high reflectivity of laser light with minimal scattering and high currents, respectively high current densities, in the fabricated wires.

This thesis started with the explanation of the theoretical background of atom chip experiments with neutral atoms. The background of fabrication was explained in the chapter on designing atom chips and the chapter on the experimental setup of atom chip experiments. A new fabrication process has been developed and established for the production of high quality atom chips. Compared to the previously used fabrication process this new fabrication process is faster, more reliable and delivers cleaner atom chips with higher quality. Furthermore the maximal amount of deposited gold for wire fabrication and the maximal current density of the wires has been increased by a factor larger than two. To this end new techniques were developed. In the meantime these techniques have been adopted by different fabricators for their own purposes ranging from atom chip fabrication to very different processes in micro fabrication.

The developed technique of thick metal layers with single slow spinning of photosensitive image reversal resist has been a major achievement, also the fabrication of high quality gold surfaces for almost perfect mirrors. The scattering attributes of a regular atom chip are negligible. The extremely precise fabrication of wires enabled this group to build highly accurate magnetic microscopes which are two orders of magnitude better in sensitivity and resolution than the ones of competing groups. Microscopes on the atom chips fabricated during this thesis reach a resolution of $\sim 1\,\mu$m with a sensitivity of $\sim 1\,$nT.

Many different atom chip layouts have been designed and fabricated. Special focus is given to three of theses atom chips.

The multi–layer atom chip This developed technique enables the fabrication of crossing wires without electric contact between them. The possibility of creating magnetic trap geometries rises enormously with this technique. During the experiment trapping potentials can be created and changed almost arbitrarily by using this atom chip layout.

The sub–micron atom chip The use of e–beam patterned wires was added to the array of fabrication techniques of atom chips. The move below the resolution limit of optical lithography in atom chip fabrication enables the fabrication of wires in the nanometre regime. From now on the full cross section of a wire is tunable in this regime. In principle this allows to create trapping potentials with different wires so close together that tunnelling of atoms from one potential well to the next becomes possible.

The semiconductor atom chip The implementation of semiconductors to the atom chip fabrication opens a whole area of new experiments. Trapping neutral atoms with non metallic wires is possible now. Quantum optics and micro fabrication meet semiconductor physics.

The latest fabrication of atom chips combined these techniques to even more capable atom chips. Sub–micron structured and semiconductor atom chips are both combined with the multi–layer technique. A combination of all three of these techniques is prepared and can be implemented on the next fabricated atom chip.

This thesis also set the basics for successful continuation of the group in the field of experiments with ultra cold atom chips. Currently three of the fabricated atom chips are mounted inside the UHV chambers and used daily. Also several state–of–the–art atom chips are ready to enter into the experiments. For example the ring e–beam multi–layer atom chip and the semiconductor atom chip promise to deliver exciting results of new physics for many years. Also first test samples with structures for the implementation of microwaves onto atom chips were delivered. This technique opens a new regime of atom physics to atom chip experiments, too.

The fabricated atom chips have been characterised and their quality has steadily been improved. Extensive tests with the heating characteristics of gold wires and the substrates used for atom chips have been performed. From the researched substrates, highly doped silicon with a thin SiO_2 insulation layer turned out to be the best suiting substrate for atom chips. Gold wires fabricated on these atom chips stand current densities of more than $10^7\,A/cm^2$ over times of > 10 seconds. A theoretical model for the heating of atom chip wires has been developed. It fits the measured data well without fitting parameters.

One of the next atom chips could be fabricated on a narrow substrate like a needle or on a transparent substrate. Both setups allow laser cooling from all directions as well as complete free optical access to the trapped atoms for imaging. Building the vacuum chamber partly from glass is done in some other groups and is an option for this group too. The fabricated atom chips are compatible with this technique.

Reflection losses and scattering of laser beams on an atom chip could be eliminated by a perfect mirror fabricated on top of it. A disadvantage is that the atoms can not be trapped close to the wires as the mirror is still on top of them and that the mirror is made of metal.

Using the back side of the atom chip could replace the solid copper structures below the atom chip or the wide trapping wires in the atom chip layout. Tall wires fabricated on the back side of the atom chip substrate could be lithographically aligned to an accuracy of micrometers to the wires on top of the atom chip.

In the future atom chips will further be developed to more complex devices. Some examples for features on future atom chips are given. Cooled atom chips might contain supra conductive wires. Also more optical elements will be implemented on atom chips in the future. Lenses or tilted mirrors can be fabricated on the atom chip. On a full semiconductor atom chip integrated optical elements could be possible. Wave guides can be grown in the heterostructure and patterned during fabrication. Even full laser diodes might be implemented in the atom chip, or some of the experimental control and analysis electronic in integrated circuits.

Atom chips are not only able to trap neutral atoms. With some modifications trapping of molecules and ions is also possible. Implementation of micro–electro–(optical)–mechanical systems (MEMS and MEOMS) could also be realised in the future. Given their versatility

and broad range of applications atom chips might as well be used in chemistry, biology or medicine in years to come.

This thesis delivered a solid base for atom chip fabrication and characterisation as well as several atom chips for experiments in the past, present and for the future.

Appendix A

Data types of the *dw-2000* program for atom chip layouts

The atom chip layout is designed using the *dw-2000* program. Different data types are used, to write each structure with an adequate dose by the e–beam. Generally the feature sizes for masks are classified as shown in Table A.1. The base dose of the resist is $330\,\mathrm{mC/cm^2}$. For the 50 kV electron beam the exposure time per pixel is calculated automatically by the e–beam machine[1]. A limit is the maximum writing speed of 6 MHz (point to point) of the e–beam. In the mean time this machine has been replaced by a new one[2]. The adequate dose for each structure and its data type have to be figured out in test writings. These settings depend on the resist.

data type	line width
0	$> 5\,\mu$m
1	$\leq 5\,\mu$m and $> 2\,\mu$m
2	$\leq 2\,\mu$m and $> 1\,\mu$m
3	$\leq 1\,\mu$m and $> 0.5\,\mu$m
4	$\leq 0.5\,\mu$m and $> 0.2\,\mu$m
5	$< 0.2\,\mu$m

Table A.1: Different structures need different exposure doses. These are separated by data types in the layout. Rules for standard structures help designing an atom chip layout. The first six data types are taken for standard structures and shown in this table. For mask design only the first three data types are used. More data types are used for special structures if needed.

Many more data types may be needed for more delicate layouts, especially in direct e–beam writing. One direct e–beam writing (the ring layout) during this thesis was as complex as 23 different data types were necessary to reach a sufficient result. Especially close to small features several data types are used to reach high resolution. Figure A.1 shows layout regions from direct e–beam writing and the amount of used data types.

[1] 5FE lithography machine, JEOL, Tokyo, Japan.
[2] JBX–9300FS, JEOL, Tokyo, Japan.

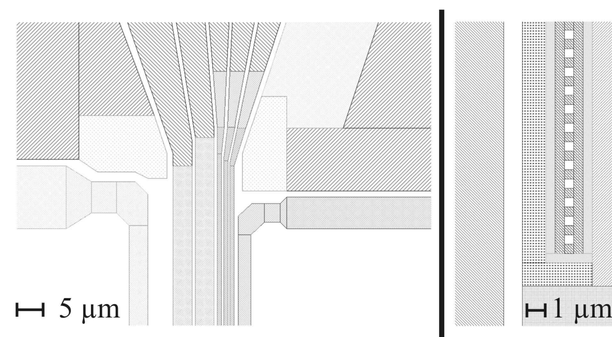

Figure A.1: The designs on the left and on the right side of the black bar show different areas of the layout of the e–beam written pattern of the multi–layer e–beam atom chip (see Figure C.8 in the appendix). Different data types are indicated through different patterns in the layout. left: To reach a sufficient quality of the patterns on the atom chip, the layout contains 7 different data types for different sizes and locations of wires. right: To fabricate $0.5\,\mu$m wide holes in a wire 6 data types are used.

Appendix B

Calibration of the long evaporation sample holder

Some atom chips are fabricated with gold layers of up to 5 μm thickness. To achieve such a huge thickness with a high surface quality and with a comparable small amount of gold and time during the evaporation, a modification in the thermal evaporator was done. For fast evaporation and to reduce the gold consumption a sample holder has been build to decrease the distance between the crucible and the sample. The distance is decreased by a factor of ~ 3.3 to 103 mm. The size of the table for samples at the holder is chosen to accept two regular samples, or one of the special size for fibre atom chips. Evaporating two samples together saves time and gold. Evaporating more than two sample at the time is difficult, as the evaporation angle gets too large for the samples which are not directly above the crucible. When the area of evaporation is increased above the size of the sample holder, more radiation is absorbed and more hot atoms are deposited, which heats the samples, while the samples do not have good heat contact to the holder. To much heat burns the resist.

During its use in the Edwards evaporator AUTO 306, the following calibration table was measured (see Figure B.1). As a result, the calibration factor of the sample holder is ~ 6.46 with an offset of 480 nm. This offset is related to the evaporation of a thin adhesion layer of Titanium, which is evaporated before the gold. The variation of the thickness is related to the position of the sample, and the place, where the measurement of the thickness took place. The size of the sample does not allow an equal evaporation everywhere. The centre of the atom chip is located above the evaporation crucible, as it is the most important place of the sample. The edges of the sample are more far away from the crucible and the amount of evaporated material depends on the distance. Thickness variations of up to 10% around the edge have been observed.

A second variation is conditioned by the measurement of thickness during evaporation. The thickness monitor is driven by an oscillating crystal. This crystal is exchanged every few evaporations and attached to a flexible holder. Small variations of this monitoring have huge effects, as the evaporation speed is about seven times faster than displayed.

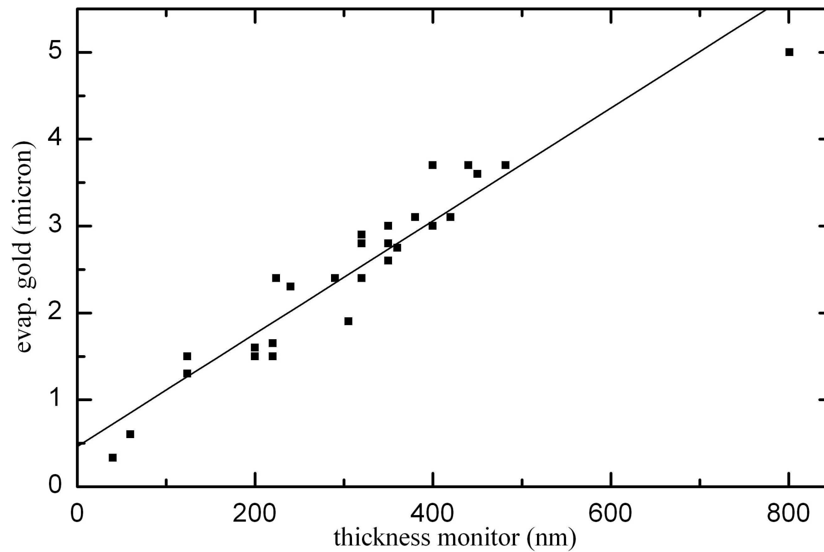

Figure B.1: This graph shows the calibration of the thickness monitor for the long evaporation sample holder. The distance between the gold crucible and the sample is 103 mm. The thickness of the gold is measured with a profilometer. The linear fit gives a slope of 6.46 with an offset of 480 nm.
Each point represents at least one fabricated sample. Before this holder was machined more samples were fabricated with a different holder. As their position of evaporation was varying slightly they are not plotted in this graph.
The variations appear due to the change of the measurement crystals, and mainly due to the place of measurement on the sample. The height of evaporated material changes across the sample. The sample size is big, and the distance from two points on the sample to the crucible is different. To conserve the important wires in the centre of the atom chips, only the metal at the edge was measured. The offset stems from the Ti adhesion layer, which is deposited below the gold.A photo of this sample holder is shown in Figure 5.4.

Appendix C

Process recipes and atom chip layouts

All fabrication process parameters are listed in this appendix. Also the *dw-2000* layouts manufactured with these recipes are illustrated for different atom chips. The size of all atom chips is $25 \times 30\,\text{mm}^2$. Designs of less importance are not described, as more than 40 lithography masks were written for the fabrication of atom chips.

C.1 Process parameter: regular atom chip

This section shows a short form of the fabrication process for a standard atom chip. The detailed process is described in Chapter 5.

1. Cover the wafer with protection resist
2. Cut the wafer
3. Clean the sample
4. Spin coat the sample with primer
   (a) Cover the sample with primer (Microposit Primer)
   (b) Spin the sample 40 seconds with 3000 rpm
   (c) Bake the sample 3 minutes on 80°C hotplate
   (d) Cool down the sample
5. Spin coat the sample with photoresist
   (a) Cover the sample with photoresist (Photoresist AZ 5214E image reversal)
   (b) Spin the sample 40 seconds with 470 rpm
   (c) Bake the sample 6 minutes on 100°C hotplate with vacuum contact
   (d) Cool down the sample
   (e) Remove edges of resist and resist from the back side of the sample
6. Expose 0.9 seconds in mask aligner with 405 nm and 15 mW under strong contact, 'high precession' and 'vacuum chamber'
7. Wait half a minute
8. Post bake 3 minutes on 120°C hotplate with vacuum contact

9. Cool down the sample
10. Flood exposure 50 seconds
11. Wait half a minute
12. Develop in AZ 726 MIF about a minute by eye
13. Rinse with clean water
14. Ozonate 7 minutes at 67°C
15. Measure the thickness of resist
16. Evaporate with a distance of 103 mm above the crucible
    (a) Titan: 35 Å, speed 0.05 nm/sec
    (b) Gold: dependent on the thickness of the resist structure, speed 0.05 – 0.4 nm/sec
17. Lift-off
18. Cover the sample with protection resist
19. Cut the sample
20. Clean the sample
21. Measure resistance of wires

Five designs are used to fabricate atom chips with this process:

Test atom chip

The test atom chip contains 12 straight wires of different width and 2 mm length. It is used for research of wires on the atom chip (see Chapter 7). The design of the test atom chip is illustrated in Figure C.1.

Spiral atom chip

This atom chip got his name from the characteristic spiral shaped double wire in its design. It is shown in Figure C.2. This atom chip also contains pads for electrostatic experiments.

Fermion and boson atom chip

The atom chip used to trap fermions and bosons is shown in Figure C.3. This atom chip basically provides trapping structures and long side guides.

Interferometer atom chip

This design is named after the three different types of interferometer, which were proposed while it was designed. An atom cloud interferometer has been build with this atom chip using a different fourth technique (see Section 8.4), which was not taken into account during designing the layout and fabrication of the used atom chip.

The interferometer atom chip is a double–layer atom chip. The layout is illustrated in Figure C.4 and a picture is shown in Figure 4.3. Comparing the layout to the photo shows, that the atom chip is mirror imaged after fabrication (see Chapter 3).

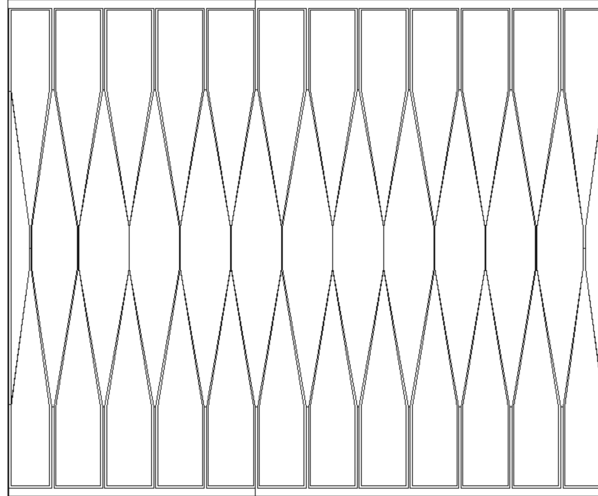

Figure C.1: Layout of the atom chip used for most of the test measurements. 12 wires of different width (100, 50, 10, 5, 2 and 1 μm, each twice) lead from top to the bottom.

Optical fibre atom chip

The optical fibre atom chip is designed to add optical fibres on it. The design offers the possibility to add fibre holders for two rectangular fibres and for fibres facing each other. The design of the fibre atom chip is illustrated in Figure C.5.

The fibres are mounted outside the centre of the atom chip, to provide space for a MOT and to transfer the trapped atoms to the atom chip. Wires guide the trapped atoms to the optical fibres. Electrical contact pads of the atom chip are reduced or moved away from the area of the fibres.

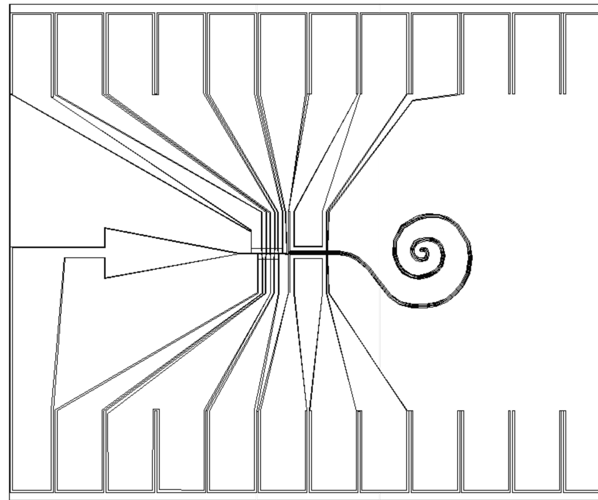

Figure C.2: The *dw-2000* design of the spiral atom chip contains the characteristic spiral on the right and electric pads to modulated a side guide on the left side. The side guide ends in a beam dump, where the wire becomes wider. Next to the spiral seven pads are not used and grounded.

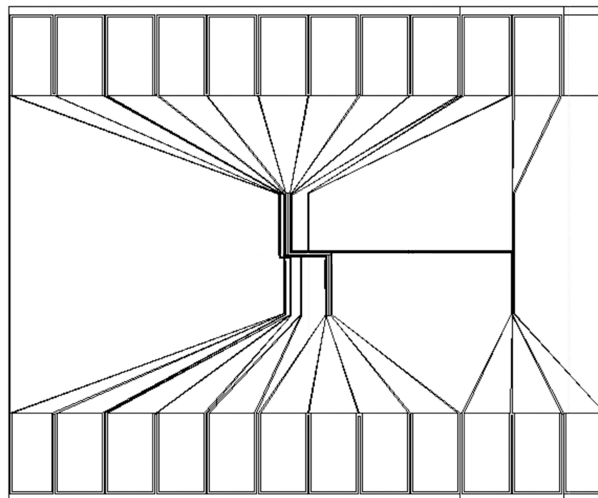

Figure C.3: This atom chip has many trapping wires in U and Z shape. It also provides more than 1 cm long side guides. One of the pads (top right) is used to contact the ground.

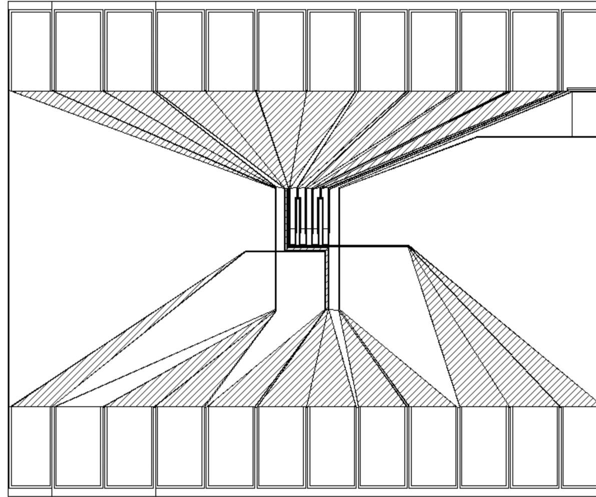

Figure C.4: The interferometer atom chip has his name from three interferometers, which are included into its wire design. To provide enough electrical contacts, a 25th pad was added on the top right. A second additional contact had to be made for the grounding.
This atom chip is fabricated in double–layer technique (see Section 6.3). All double–layer areas are hatched.

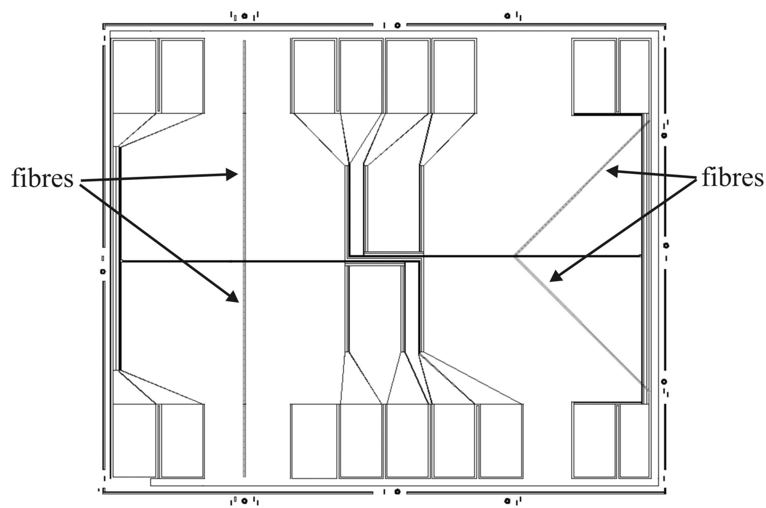

Figure C.5: The layout of the fibre atom chip contains U and Z-wires for trapping in the centre of the atom chip and long side guides up to the edges. Place for optical fibres is available along these side guides. The fibres are also illustrated in the layout. Some contact pads are removed or scaled down to clear space for the fibres. On the left side of this layout two fibres are facing each other, on the right side two fibres are aligned with an angle of 90°. Cutting lines and markings for the fibre alignment are visible around the atom chip.

C.2 Process parameter: narrow wire grid atom chip

Chapter 6.1 explains the fabrication process of the narrow wire grid atom chip. This fabrication is close to the regular atom chip fabrication. The difference is, that this technique allows to prepare long thin wire grids at the resolution limit of the optical lithography. This appendix lists a short recipe of this technique.

1. Cover the sample with primer
2. Spin the sample 40 seconds with 3000 rpm
3. Bake the sample 3 minutes on 80°C hotplate
4. Cool down the sample
5. Spin coat the sample with photoresist
   (a) Cover the sample with photoresist (Photoresist AZ 5214E Image reversal)
   (b) Spin the sample 40 seconds with 5000 rpm
   (c) Bake the sample 45 seconds on 100°C hotplate with vacuum contact
   (d) Cool down the sample
   (e) Remove edges of resist and resist from the back side of the sample
6. Expose 2.6 seconds in mask aligner with 405 nm and 15 mW under strong contact, 'high precession' and 'vacuum chamber'
7. Wait half a minute
8. Post bake 45 seconds on 120°C hotplate with vacuum contact
9. Cool down the sample
10. Flood exposure 1.3 minutes
11. Wait half a minute
12. Develop 25 seconds in AZ 726 MIF
13. Rinse with clean water
14. Ozonate 7 minutes at 67°C
15. Evaporate metal
16. Lift-off

C.3 Process parameter: multi–layer atom chip

On multi–layer atom chips different metal layer are fabricated on top of each other. They do not have electric contact to each other as they are separated by a layer of polyimide. For the preparation of a polyimide separation layer a special recipe is used. This is shortly written in this appendix. While using polyimide water is avoided. As dry polyimide is hard to remove everything is cleaned immediately. The evaporation techniques of the gold layers on the multi–layer atom chip are described in the previous appendix paragraphs.

This recipe gives a polyimide pattern with a height of about 550 nm, which can be reduced with the ozonator. The detailed description is given in Chapter 6.4.

1. Dynamical spin polyimide (Durimide (R) 7505)
   (a) Drop polyimide on rotating sample, 300rpm
   (b) Spin 7 seconds with 1000 rpm
   (c) Spin 90 seconds with 10400 rpm
2. Wait 10 minutes
3. Softbake 5 minutes on 100°C hotplate
4. Expose 7 seconds in mask aligner with 405 nm and 15 mW
5. Softbake 1 minute on 100°C hotplate
6. Wait 40 minutes
7. Develop 40 seconds (QZ 3501)
8. Rinse 2 minutes in n–butyl acetate
9. Cure 1 hour in oven at 300°C
10. Thinning in ozonator

C.4 Process parameter: e–beam patterned atom chip

A short form of the fabrication process for e-beam patterned wires on an atom chip is listed in this paragraph. Before this process, a regular lithography step (see Appendix: C.1) is done to align the e–beam pattern in the right place on the substrate. The whole process is explained in detail in Section 6.5.

Multi–layer e–beam atom chip

The multi–layer e–beam atom chip consists of several layers. Two metal layer are separated by a layer of polyimide. Accessorily this multi–layer atom chip contains an e–beam written region of $600 \times 600\,\mu\text{m}^2$ in the centre of the atom chip. This area is attached to the bottom metal layer. The design is illustrated in Figure C.6.

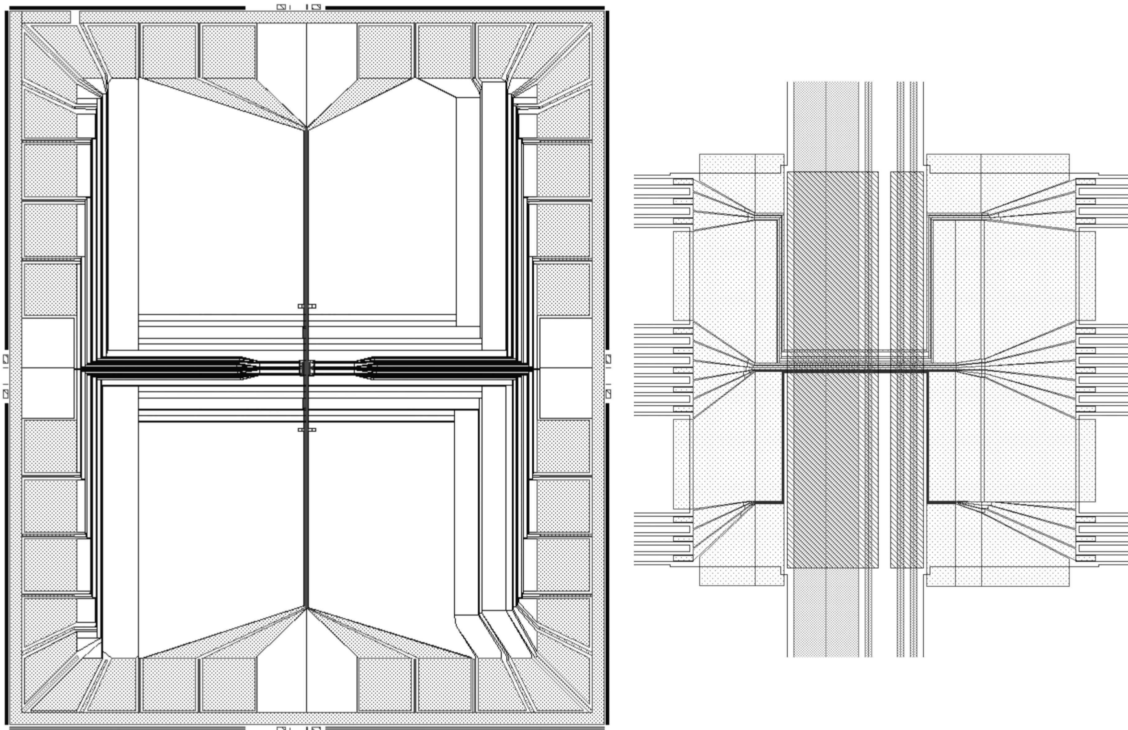

Figure C.6: left: Layout of the e–beam multi–layer atom chip. The white areas with the lines is the bottom layer. Most wires and grounded patterns are build by this layer. The dotted structures are the 36 pads around the sample and the big crossing wires from the top to the bottom fabricated in double–layer technique. The pads are arranged in a way, to provide free optical access to the centre of the atom chip. The grounding around the atom chip is intermitted in the top left corner. The cutting lines around the atom chip are interrupted in the middle to implement the markings for e–beam and mask alignment. right: The centre of the atom chip on the left is enlarged. This structure shows an e–beam pattern (dotted). The $600 \times 600\,\mu\text{m}^2$ field is written for every atom chip independently. The leads to the e–beam written part are coming from left and right in the bottom layer. The broad top wires from top to the bottom cross the e–beam wires. The separation between the e–beam and the top layer is ensured by the polyimide layer (hatched).

Figure C.7 illustrates the new layout of the multi–layer e–beam atom chip. This atom chip is called ring atom chip. The top layer, which is crossing over the polyimide contains three wires to create RF potentials. This layout is also shown in more detail in the double page Figure 3.4 and 3.5.

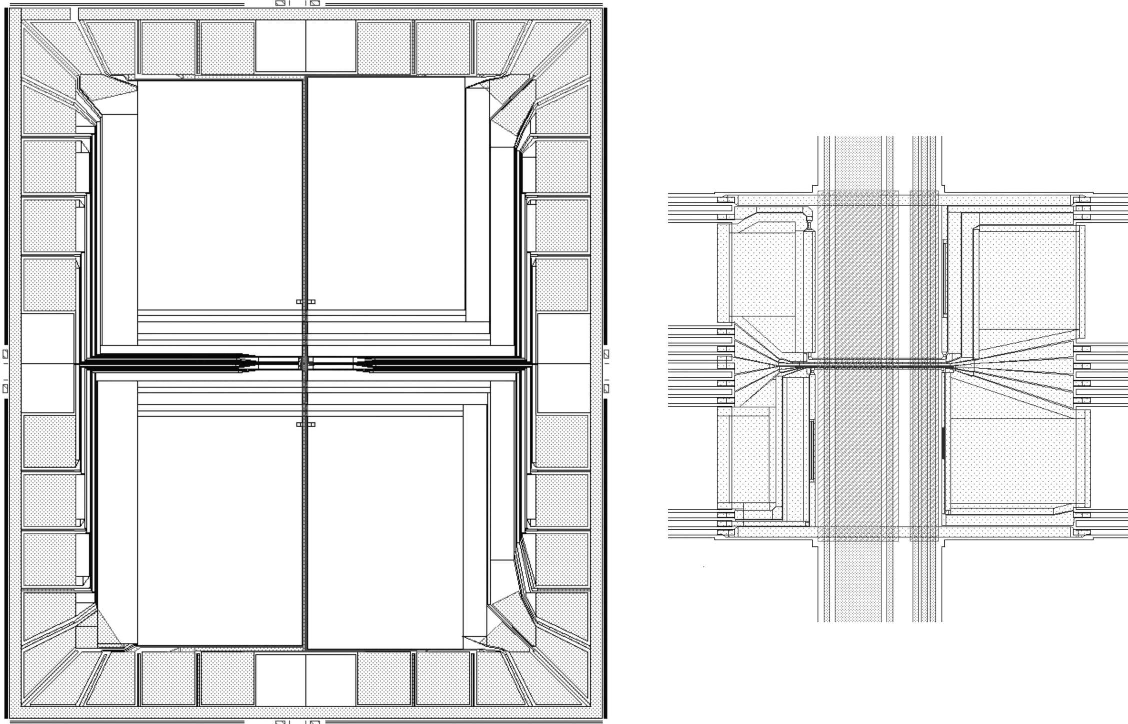

Figure C.7: left: Layout of the new e–beam multi–layer ring atom chip. It is similar to the multi–layer atom chip shown in Figure C.6. right: The centre of the ring atom chip on the left is enlarged. This figure displays e–beam patterned wires (dotted). The $600 \times 600\,\mu\text{m}^2$ field is written for every atom chip independently. The leads to the e–beam written part are coming from left and right in the bottom layer. The big wires from top to the bottom cross the e–beam wires. The separation is ensured by the hatched polyimide layer. In this design two times three wires cross the e–beam patterned part. The top wires are 10/ 80/ 10 and 10/ 10/ 10 μm wide (from left to right). The gap between these wires is 10/ 10/ 35/ 5/ and 5 μm respectively.

1. Coat the sample with PMMA 495K (5%)
2. Spin the sample 60 seconds with 5000 rpm
3. Bake the sample for 1 hour at 180°C in oven
4. Cool down the sample
5. Coat the sample with PMMA 950K (5%)
6. Spin the sample 60 seconds with 8000 rpm
7. Bake the sample for 1 hour at 180°C in oven

8. Cool down the sample
9. Develop 60 seconds in MIBK:IPA, 1:2
10. Rinse in IPA
11. Evaporate metal
12. Lift-off

C.5 Process parameter: semiconductor atom chip

The semiconductor atom chip is based on a multi–layer atom chip (see Section 6.4). In this appendix the fabrication technique of the semiconducting part of this atom chip is listed and the data sheets of the used wafer are given. Detailed fabrication information are written in Section 6.6.

Semiconductor atom chip

The semiconductor atom chip is a multi–layer atom chip with an additional semiconductor chip mounted on top of it. The semiconducting part is structured. Electric contacts are assured by 25 μm gold bond wires. The semiconducting part is glued to the multi–layer atom chip of centre. Figure C.8 illustrates the design of this atom chip.

1. Cleave GaAs
2. Spin coat primer with 3000 rpm, 40 seconds
3. Bake the sample for 3 minutes at 80°C hotplate
4. Spin coat image reversal with 5000 rpm, 40 seconds
5. Bake the sample for 45 seconds at 100°C hotplate
6. Expose 2.6 seconds in mask aligner with 405 nm and 15 mW
7. Post bake 45 seconds on 120°C hotplate with vacuum contact
8. Cool down the sample
9. Flood exposure 1.3 minutes
10. Wait half a minute
11. Develop 25 seconds in AZ 726 MIF
12. Rinse with clean water
13. Ozonate 7 minutes at 67°C
14. Plasma etching down to super lattice
15. Clean the sample
16. Repeat the steps 4 – 12 to build a resist pattern for evaporation
17. Evaporation
    (a) Nickel, 50 Å
    (b) Germanium, 400 Å
    (c) Gold, 800 Å
    (d) Nickel, 200 Å
    (e) Gold, 2000 Å
18. Lift–off

19. Ozonate 5 minutes
20. Alloy
    (a) 30 seconds 150°C
    (b) 30 seconds 345°C
    (c) 10 seconds linear ramp to 430°C
    (d) 30 seconds 430°C
21. Cleave the sample
22. Wetch the sample to required height
23. Clean the sample
24. Glue GaAs onto multi–layer atom chip
25. Bond contacts from multi–layer atom chip to GaAs

C.5.1 Data sheets of the GaAs wafer

The two used GaAs wafer are grown by Vladimir Umansky in his MBE at the Weizmann Institute of Science. The details of these 2 inch wafer are given in the following paragraphs and listed in Table C.5.1.1.

Wafer 7–182

The heterostructure of this wafer is grown on GaAs. It contains a super lattice of twenty layers of GaAs and AlGaAs. This is used as etch stop layer for selective etching. On top of it about one micron of Si doped (n^+) GaAs is grown as conductive layer. The measured 3D charge carrier density is $N \sim 6.4 \cdot 10^{18}$, the mobility is $\mu = 1160\, cm^2/V sec$ and the resistance per square of this layer is $8.5\,\Omega/\square$.

Wafer 7–183

Like wafer 7–182 the heterostructure of this wafer is grown on GaAs. This has two super lattices. The low one has twenty layers of GaAs and AlGaAs the one on top of it 25 layers. They are separated by a GaAs layer of about 60 nm. They are used as etch stop layers. On top of them about one micron of Si doped (n^+) GaAs is grown as conductive layer. The measured properties of 7–183 are: 3D charge carrier density $N \sim 5 \cdot 10^{18}$, mobility $\mu = 1080\, cm^2/V sec$ and the resistance per square of this layer is $12.4\,\Omega/\square$.

	wafer 7–182	wafer 7–183
super lattice 1 (layer)	20	20
super lattice 2 (layer)	none	25
doping layer thickness	930 nm	930 nm
donators	Si/ n^+	Si/ n^+
charge carrier density	$\sim 6.4 \cdot 10^{18}$	$\sim 5 \cdot 10^{18}$
mobility	$1160\, cm^2/V sec$	$1080\, cm^2/V sec$
resistance	$8.5\,\Omega/\square$	$12.4\,\Omega/\square$

Table C.5.1.1: Properties of the GaAs wafer 7–182 and 7–183.

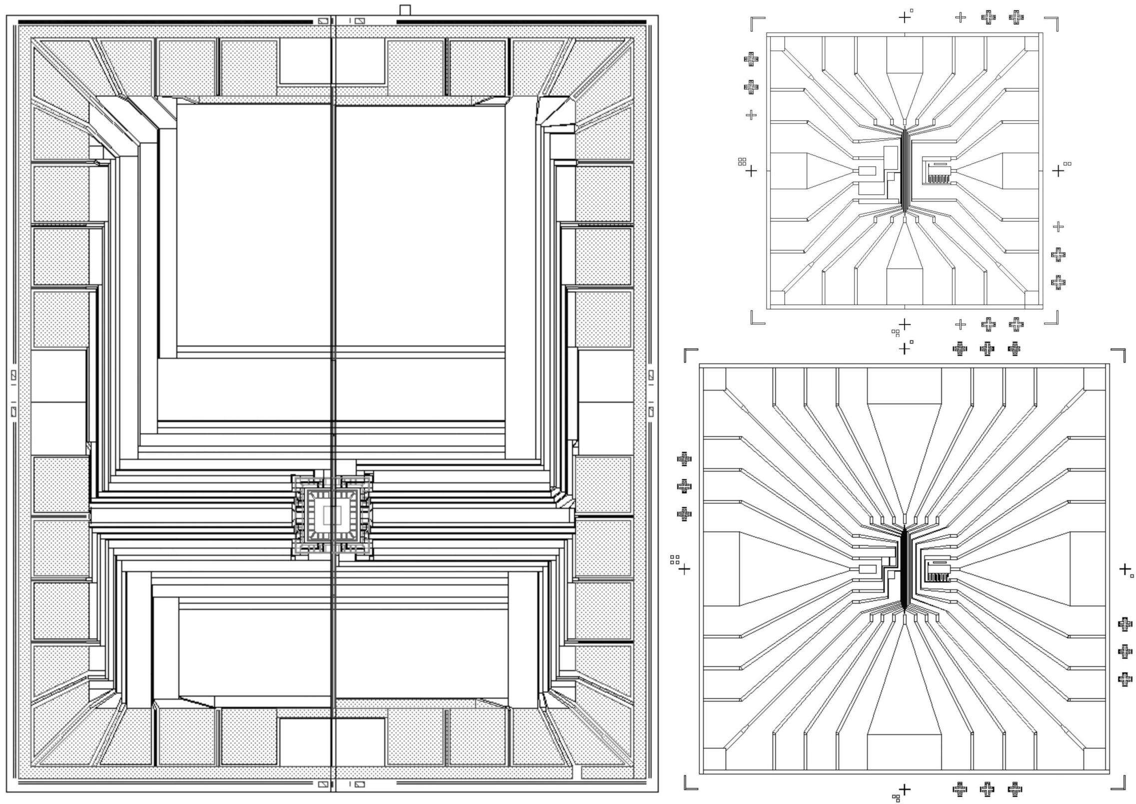

Figure C.8: left: Layout of the Si multi layer part of the semiconductor atom chip (see Section 6.4). The centre is assigned to trap and cool atoms. From there the atoms are to be guided by the wires from top to bottom to the GaAs part. The GaAs slice is attached to the atom chip between the centre and the bottom. Wires lead from left and right to this position to provide electric contacts for the GaAs. right, top: Layout of a $2 \times 2\,\mathrm{mm}^2$ GaAs piece. The wires are structured semiconducting material. The structure provides wires for trapping the atoms and wires for the experiments. Outside alignment marks and cutting corners are visible. right, bottom: Layout of a $3 \times 3\,\mathrm{mm}^2$ GaAs piece. It is structured like the $2 \times 2\,\mathrm{mm}^2$ GaAs piece. Both pieces fit with their connections onto the Si atom chip on the left. The $3 \times 3\,\mathrm{mm}^2$ GaAs piece provides more structures, and the alloyed contact pads are further from the central region. The many contacts also causes more wire bonds, which are again further from the centre. Both GaAs layouts provide free optical access to the centre. The inner part of both designs have a size of $600 \times 600\,\mu\mathrm{m}^2$. A layout, which allows to pattern this area by e–beam lithography is available on the same lithography mask.

Appendix D

Material properties

Table D.1 lists electric and thermal properties of most of the materials used during fabrication [Goo06]. The metals are used to build wires with them. Also doped GaAs is used to carry currents. Si, GaAs and sapphire are tested as substrates for atom chips. The polyimide is used as separation layer for multi–layer atom chips and the insulators are used in the mounting of the atom chips (see Figure 4.1).

material	thermal heat conductivity at 0 – 100°C (W/m·K)	specific heat capacity at 25°C (J/K·kg)	electrical resistivity at 20°C ($\mu\Omega$·cm)	dielectric constant
gold	318	129	2.2	
aluminium	237	900	2.67	
silver	429	237	1.63	
copper	401	385	1.69	
titanium	21.9	523	54	
Si	80 – 150	703	23×10^{10}	
SiO_2	~ 1.5	670 – 740		
GaAs	46	350	$\sim 10^9$	13.1
sapphire	35 – 40	750	$>10^{14}$ *	7.5 – 11.5
polyimide	0.26 – 0.54	1000	$0.08 - 2 \times 10^{17}$ *	3.9 – 5.4
macor	1.5	790	$>10^{14}$ *	5.9
shapal	100	480	1.8×10^{13} *	7.3
kapton	1090	0.1 – 0.35	10^{18} *	3.4

Table D.1: This table lists the thermal and electric properties of the materials used during this thesis. The metals are used as bulk material for wires on atom chips. Si with SiO_2 is used as substrate, as well as sapphire and GaAs. Doped GaAs is also used as conductive material for wires. Polyimide is used as separation layer between metal wires on atom chips, while macor, shapal and kapton are insulators used in the mounting of the atom chip.
* Volume resistivity (Ω cm)

Appendix E

Difficulties encountered during this thesis

Several problems appeared during this thesis. Some of them have not been solved yet. To prevent other people from doing the same mistakes again, or to help them solving these problems, they are mentioned briefly.

E.0.2 Multi spinning process

To achieve high resist structures it is possible to spin coat a substrate with resist, and to spin coat onto the fabricated resist again. The number of resist layers spun onto each other is not limited, and the height of the structure grows with every layer. This technique has been used for atom chip fabrication in the very beginning of this thesis and before.

During this thesis, the multi spinning process was substituted by the described single spinning process (see Section 5.4). The new single layer spinning process delivers more smooth resist, is more reliable and faster to fabricate than a multi spinning process. As every additional fabrication step harms the sample, the single layer spinning process is also more clean. With the new single layer process the thickness of the resist pattern is even higher than the one of the previously used multi spinning processes.

The multi spinning process can be varied in the number of layers and the spinning speed of each layer. Two used processes from the time of the beginning of this thesis are listed in the following.

Multi spincoat process 1

1. Cover the sample with Primer
2. Spin the sample 40 seconds with 3000 rpm
3. Bake the sample 3 minutes on 80°C hotplate
4. Cool down the sample
5. Spin coat the sample with photoresist layer 1
   (a) Cover the sample with photoresist (Photoresist AZ 5214E Image reversal)
   (b) Spin the sample 40 seconds with 3000 rpm
   (c) Bake the sample 2 minutes on 100°C hotplate with vacuum contact
   (d) Cool down the sample

6. Spin coat the sample with photoresist layer 2
   (a) Cover the sample with photoresist (Photoresist AZ 5214E Image reversal)
   (b) Spin the sample 40 seconds with 1500 rpm
   (c) Bake the sample 2 minutes on 100°C hotplate with vacuum contact
   (d) Cool down the sample
7. Expose 3 seconds in mask aligner with 405 nm and 15 mW under strong contact, 'high precession' and 'vacuum chamber'
8. Wait half a minute
9. Post bake 6.5 minutes on 120°C hotplate with vacuum contact
10. Cool down the sample
11. Flood exposure 3 minutes
12. Wait half a minute
13. Develop by eye in AZ 726 MIF
14. Rinse with water

The height of this resist pattern is about 2.2 μm.

Multi spincoat process 2

The process mainly used for atom chip fabrication before this thesis was started was even more complicated, as it used dynamic spinning for three different resist layers. The height of the resulting resist is 3.5 to 4.2 μm.

1. Cover the sample with Primer
2. Spin the sample 40 seconds with 3000 rpm
3. Bake the sample 3 minutes on 80°C hotplate
4. Cool down the sample
5. Spin coat the sample with photoresist layer 1
   (a) Cover the sample with photoresist (Photoresist AZ 5214E Image reversal)
   (b) Spin the sample 40 seconds with 3000 rpm
   (c) Bake the sample 50 seconds on 100°C hotplate with vacuum contact
   (d) Cool down the sample
6. Spin coat the sample with photoresist layer 2
   (a) Cover the sample with photoresist (Photoresist AZ 5214E Image reversal)
   (b) Dynamic spin coating 300 – 3000 rpm, last for 30 seconds
   (c) Bake the sample 1 minute and 20 seconds on 100°C hotplate with vacuum contact
   (d) Cool down the sample

7. Spin coat the sample with photoresist layer 3
   (a) Cover the sample with photoresist (Photoresist AZ 5214E Image reversal)
   (b) Dynamic spin coating 300 – 4000 rpm, last for 30 seconds
   (c) Bake the sample 2 minutes on 100°C hotplate with vacuum contact
   (d) Cool down the sample
8. Expose 3 seconds in mask aligner with 405 nm and 15 mW under strong contact, 'high precession' and 'vacuum chamber'
9. Wait half a minute
10. Post bake 6.5 minutes on 120°C hotplate with vacuum contact
11. Cool down the sample
12. Flood exposure 3 minutes
13. Wait half a minute
14. Develop $\sim$ 1 minute in AZ 764 MIF
15. Rinse with water

E.0.3 Silicon oxide layer on Silicon

Silicon was bought with different silicon oxide layer thicknesses. The thinnest has been 17.5 nm and was too thin. Shorts between wires were measured. The SiO_2 layer did not insulate the wires from the substrate. A 25 nm thick SiO_2 gave sufficient results.

E.0.4 Etched V–grooves for fibre mounting

To reduce the height of the core of an optical fibre above the atom chip and to align the fibres on the atom chip, tests were done with V–grooves etched into the surface of the atom chip. The wet–etched grooves were not as accurate as required. Also etching close to a wire was not possible. Either the wire was underetched, which leads to bad heat conductivity and a fragile wire, or the groove was far away from the wire. Structures of SU–8 delivered successful results (see Chapter 6.7).

E.0.5 Separation layers of Al

Aluminium oxide was tested as separation layer on multi–layer atom chips. The advantages of aluminium oxide are, its easy handling, the thin layer (compared to polyimide) and its high heat conductivity. Therefore aluminium was evaporated on lithographically patterned areas and exposed to air. This was repeated three times to enlarge the thickness of the layer with good oxidation. But still this layer was not able to separate two conducting layers completely. This was probably due to the size of the area between the wires. On the multi–layer atom chips the separation areas are $100 \times 500\,\mu\text{m}^2$ big, and have to be without a single pinhole. The currents, which have to be separated are in the order of some amperes.

E.0.6 Plasma deposited SiN as separation layer

As separation layer of SiN between crossing wires was tested. With plasma deposition[1] 14 – 20 nm, 40 nm and 60 nm thick SiN layers were deposited onto a gold layer. On top of the SiN another gold layer was evaporated. The SiN did not separate the metal layers electrically. SiN would have advantages compared with polyimide. It is thinner and has a better heat conductance. More successful might be sputtering of SiN.

E.0.7 Silicon monoxide as separation layer

Like the aluminium oxide, SiO has been tested as separation layer. Between two gold layers SiO was deposited with different heights. An insulation between the two conductors has not been observed.

E.0.8 Metallization of bond pins

In the mounting, the heads of the copper–beryllium pins are polished. From here wire bond contacts are set to the atom chip. To achieve a better electric contact and mainly to increase the adhesion of the bond wires, a metal layer was deposited onto the heads. This layer contained 30 nm of Ti for adhesion and about 3 μm of Au. These layers did not stick strong enough at the polished heads. During bonding the evaporated metal partly left the pins. A better adhesion of the gold or aluminium bonds could not be achieved by this technique.

[1] NEWE SCVI 101, Nextral.

Appendix F

List of publications

During this PhD thesis and the preceding diploma thesis, the author published the following articles together with his coworkers:

- L. Della Pietra, S. Aigner, Ch. vom Hagen, S. Groth, I. Bar–Joseph, H. Lezec and J. Schmiedmayer. *Designing potentials by sculpturing wires.* eprint: arXiv:cond-mat/0604619

- T. Schumm, P. Krüger, S. Hofferberth, I. Lesanovsky, S. Wildermuth, S. Groth, I. Bar-Joseph, L. M. Andersson, and J. Schmiedmayer. *A Double Well Interferometer on an Atom Chip.* accepted to be published in: Quantum Information Processing (2006)

- M. Wilzbach, A. Haase, M. Schwarz, K. Wicker, X. Liu, K.–H. Brenner, S. Groth, T. Fernholz, B. Hessmo and J. Schmiedmayer. *Detecting Neutral Atoms on an Atom Chip.* Fortschritte der Physik **54**, 746 –764 (2006)

- S. Wildermut, S. Hofferberth, I. Lesanovsky, S. Groth, I. Bar–Joseph, P. Krüger and J. Schmiedmayer. *Sensing electric and magnetic fields with Bose-Einstein Condensates.* Appl. Phys. Lett. **88**, 264103 (2006)

- T. Schumm, S. Hofferberth, L. M. Andersson, S. Wildermuth, S. Groth, I. Bar–Joeseph, J. Schmiedmayer and P. Krüger. *Matter–wave interferometry in a double well on an atom chip.* Nature Physics **1**, 57 (2005)

- P. Krüger, L. M. Andersson, S. Wildermuth, S. Hofferberth, E. Haller, S. Aigner, S. Groth, I. Bar–Joseph and J. Schmiedmayer. *Disorder Potentials near Lithographically Fabricated Atom Chips.* eprint: arXiv:cond-mat/0504686

- S. Wildermuth, S. Hofferberth, I. Lesanovsky, E. Haller, M. Andersson, S. Groth, I. Bar–Joseph, R. Folman and J. Schmiedmayer. *Bose–Einstein condensates: Microscopic Magnetic Field Imaging.* Nature **435**, 440 (2005)

- K. Brugger, P. Krüger, X. Luo, S. Wildermuth, H. Gimpel, M. W. Klein, S. Groth, R. Folman, I. Bar–Joseph, and J. Schmiedmayer. *Two–wire guides and traps with vertical bias fields on atom chips.* Phys. Rev. A **72**, 023607 (2005)

- S. Groth, P. Krüger, S. Wildermuth, R. Folman, T. Fernholz, D. Mahalu, I. Bar–Joseph, and J. Schmiedmayer. *Atom Chips: Fabrication and Thermal Properties.* Appl. Phys. Lett. **85**, 2980 (2004)

- X. Luo, P. Krüger, K. Brugger, S. Wildermuth, H. Gimpel, M. W. Klein, S. Groth, R. Folman, I. Bar–Joseph, and J. Schmiedmayer. *Atom fiber for omnidirectional guiding of cold neutral atoms* . Opt. Lett. **29**, 2145 (2004)

- P. Krueger, X. Luo, M. W. Klein, K. Brugger, A. Haase, S. Wildermuth, S. Groth, I. Bar–Joseph, R. Folman, and J. Schmiedmayer. *Trapping and manipulating neutral atoms with electrostatic fields.* Phys. Rev. Lett., **91**, 233201 (2003)

- M. P. Schwarz, M. A. Wilde, S. Groth, D. Grundler, Ch. Heyn, and D. Heitmann. *Sawtoothlike de Haas–van Alphen oscillations of a two-dimensional electron system.* Phys. Rev. B **65**, 245315 (2002)

- M. P. Schwarz, D. Grundler, H. Rolff, M. A. Wilde, S. Groth, Ch. Heyn, and D. Heitmann. *De Haas–van Alphen effect in a two–dimensional electron system.* Physica E **12**, 140 (2002)

- S. Groth. *Mikromechanische Cantilever–Magnetometrie an chemisch hergestelltem Zinkoxid.* Diploma thesis, Universität Hamburg, (2001).

In addition, the atom chips fabricated during this thesis led to more publications, where the author of this thesis is acknowledged. Also 17 PhD and diploma theses benefitted from the atom chips developed during this thesis and 11 PhD and diploma theses are still benefitting from them. Even more will follow. He further contributed in several conference proceedings and was invited for talks.

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