DESIGN OF AN FPGA-BASED HIGH-SPEED FILTER-DECIMATOR FOR THE GIFTS IMAGING INTERFEROMETER

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ABSTRACT

This paper presents the design of an FPGA-based frame filter-decimator for the Geostationary Imaging Fourier Transform Spectrometer (GIFTS). The decimator reduces samples from two 128x128 sample imaging arrays from 1638.4 fps to 102.4 complex fps for the Long Wave IR (LWIR) band and from 1638.4 fps to 204.8 complex fps for the Medium Wave IR (MWIR) band. The design uses a novel parallel pipeline architecture to handle the bandpass sampling and decimation of the 16k array samples which arrive a frame-at-a-time. The design is challenging because of significant speed, size, weight, and power restrictions for satellite implementation.

1. INTRODUCTION

The Geostationary Imaging Fourier Transform Spectrometer (GIFTS) instrument is a high spectral resolution satellite-based imaging interferometer sponsored by NASA to collect sounding data over a large footprint on the earth. It is capable of up to 0.6 cm^{-1} resolution in the 685 cm^{-1} to 1130 cm^{-1} long wave IR (LWIR) band and the 1650 cm^{-1} to 2250 cm^{-1} medium wave IR (MWIR) band using two 128x128 sample focal plane arrays (FPAs). GIFTS is intended, among other purposes, to "space validate advanced technologies which will improve the general capability, and reduce the cost of, future remote sensing satellites...[1]"

One of the challenges presented by the GIFTS instrument is the need to handle the high data rate generated by the FPAs for both the LWIR and MWIR bands. During a 10 second scan, the combined data rate from the FPAs is approximately 134.4 Msamples/s. The array sampling rate is required to be high to increase the sensitivity of the instrument without saturating the FPAs. Since this sampling rate is much higher than required by the band of interest, it is desirable to perform filtering and decimation to reduce the data rate to a manageable amount.

This paper presents a description of the filter-decimator required to reduce the data rate from the interferometer FPAs to a lower-rate data stream that contains the information in the band of interest. Section 2 describes the requirements and general approach used to implement the decimation-filter. The top level Implementation of the MWIR filter is presented in Section 3. The design of the two-stage LWIR filter is discussed in Section 4, and a summary and discussion is presented in the final section.

2. GENERAL FILTER DESIGN APPROACH

Due to the sensitivity of the FPAs used in the instrument, it is necessary to oversample the signal by a factor of greater than 32 for the LWIR and greater than 4 in the MWIR. Furthermore, the bandpass nature of the bands of interest allows for processing the signal so that the bands are aliased to baseband for more efficient exploitation of the signals. Additional efficiency is achieved by using complex decimation filters that exploit features of the the transition bands in the bandpass filter to reduce the number of coefficients in the filters.
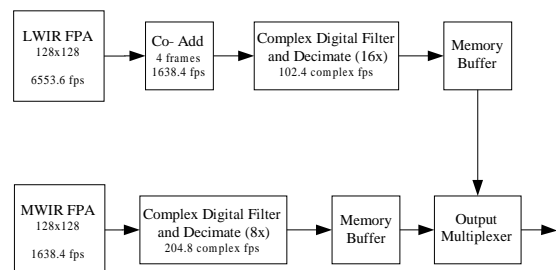

Figure 1: Signal processing chain for the GIFTS interferometer data.

The two signals pass through different, but similar, filter and decimation stages in the signal processing chain,

as shown if Figure 1. The LWIR band is first decimated in a simple 4-frame co-adder from the original 6553.6 fps to 1638.4 fps, where the signal is then bandpass filtered and decimated in a two-stage multi-rate complex polyphase structure to the required 102.4 complex fps over a nominal 10 second scan. To reduce the complexity of the design, the first stage operates on the real input signal, and the second stage implements a complex filter. The MWIR band requires only a single stage multi-rate complex polyphase filter to reduce the original 1638.4 fps to 204.8 complex fps for the same 10 second scan.

The major challenge in the implementation of the filter-decimator is the requirement that the 16,384 samples in each FPA frame must be filtered with a nominally 72-tap filter in the LWIR band (composed of an 8-tap real FIR filter followed by a 64-tap complex FIR filter), and a 32-tap complex FIR filter in the MWIR band, where each filter is applied to each of the input samples, resulting in 16k parallel filters per band. This requirement has led to a FPGA-based design which circulates the input data through a highly parallel pipeline architecture to meet both the computational and memory I/O access rate. A significant restriction on the design comes from the satellite requirements for size (limited to four standard sized VME boards), weight (less than six pounds including heatsinks), power (less than 20 watts of total operating power), processing speed (up to 30×10^6 samples per second) and radiation tolerance (SEU/SEI immune, 200k rad total dose) which limit the processing and I/O capabilities of the FPGAs chosen for the design.
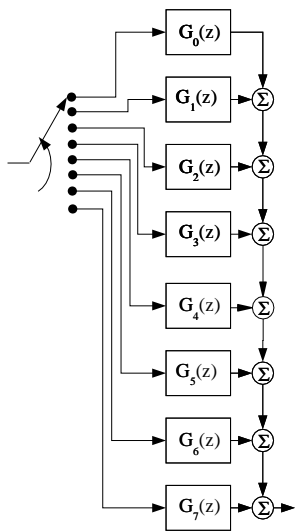
The basic processing algorithm is a multi-rate complex polyphase filter which is used to reduce the number of multiplies per unit time (MPU) and adds per unit time (APU) [2]. An example of the multi-rate structure for the MWIR band is given in Figure 2. In this structure, each of the eight complex polyphase filters, $G_0, G_1, G_2, \ldots, G_7$, are made up of the filter coefficients from the $k, k+1, k+2, \ldots, k+7$ coefficients of the original complex bandpass filter. Each time the commutator makes one sweep through the filters a single output sample is created. Since only one-eighth of the filter coefficients are used for each input sample, the total number of MPU and APU are reduced by approximately one-eighth.

The two-stage LWIR filter is designed based on an interpolated FIR (IFIR) design to reduce computational requirements by allowing smaller filters in each stage [3]. The LWIR filter has much greater processing demands than the MWIR filter due to location of the passband and particularly because of the narrow transition band required at the upper bandedge of the filter.

The basic concept behind the IFIR method is given in Figure 3. Using multi-rate processing theory [2], it can be
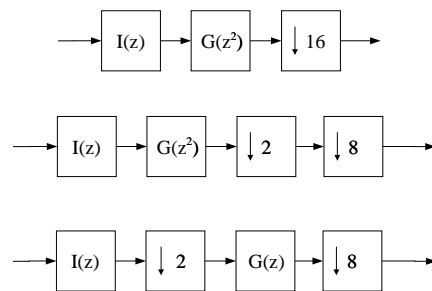

Figure 3: Equivalence of decimation filters using the IFIR method.

Figure 2: Multi-rate complex polyphase filter structure for the MWIR band. Each of the G_i filters is complex.

shown that the block diagram at the top of Figure 3 is equivalent to the the block diagram at the bottom of the figure. The first filter, $I(z)$, is used to filter out the extra spectral image created when a bandpass filter with *twice* the desired bandwidth and transition bands, and thus requiring fewer coefficients, is interpolated with zeros to create the filter $G(z^2)$. The output of the filter can then be downsampled to the desired rate.

The first stage of the LWIR filter, the pre-filter, implements a filter/decimate by two with the frequency response given in Figure 4. Note that this is a low-order lowpass filter
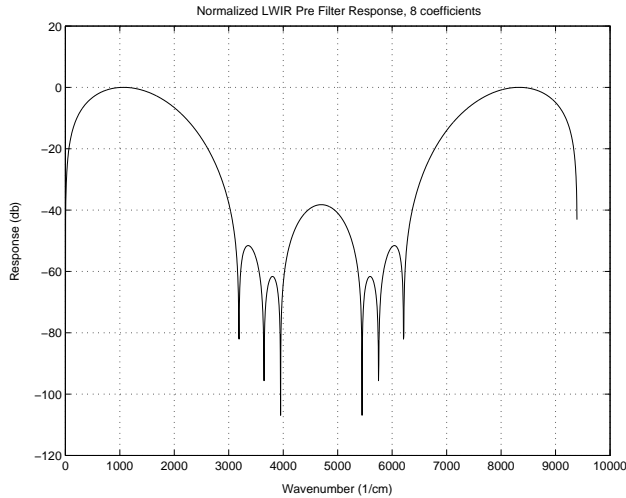
Figure 4: Frequency response of the LWIR pre-filter.

with a fairly flat response in the band of interest, and >50 dB attenuation in the band 5250–6000 cm^{-1}.

The lowpass filter is followed by a complex post-filter which has the frequency response given in Figure 5. This
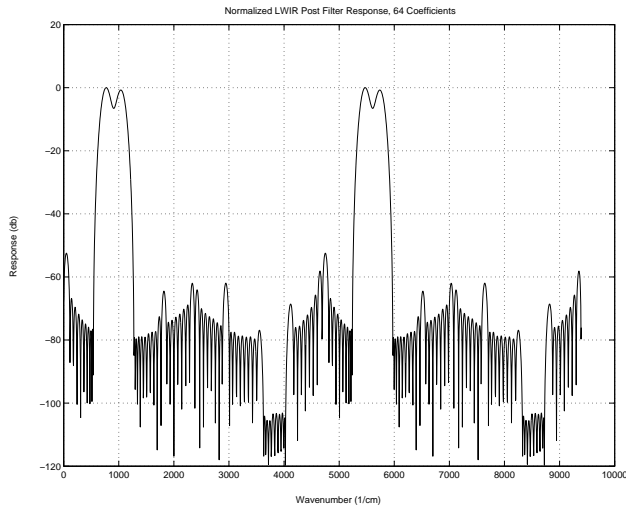

Figure 5: Frequency response of the LWIR post-filter.

filter includes the spectral image caused when the interpolation in $G(z^2)$ is performed.

The combined filter is given in Figure 6, which meets the design requirements. Here we see that the unwanted spectral image of Figure 5 in the band 5250–6000 cm^{-1} is removed by the pre-filter of Figure 4.
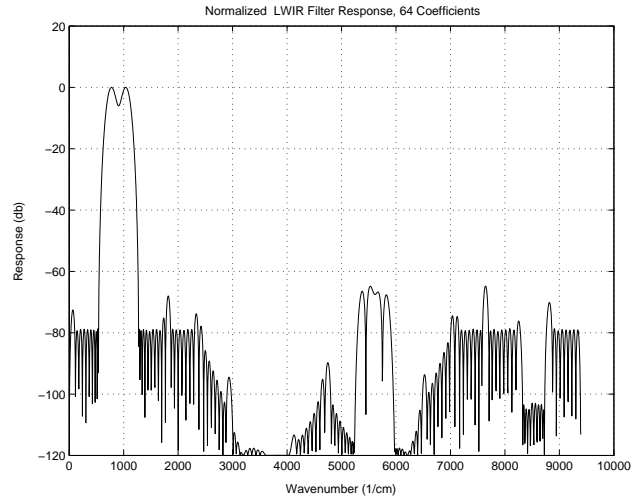

Figure 6: Combined frequency response of the LWIR filter.

3. MWIR FILTER HARDWARE DESIGN

The implementation of the filters has been designed to use several radiation-hardened Actel FPGAs. The implementation takes advantage of the fact that only one of the eight polyphase filters (in the MWIR filter and the second stage of the LWIR filter) are active at any one time, realizing a factor of seven in component reduction. Taking advantage of the filter coefficient symmetry reduces the number of multipliers by an additional factor of two. The top-level block diagram for the MWIR multi-rate polyphase filter is given in Figure 7
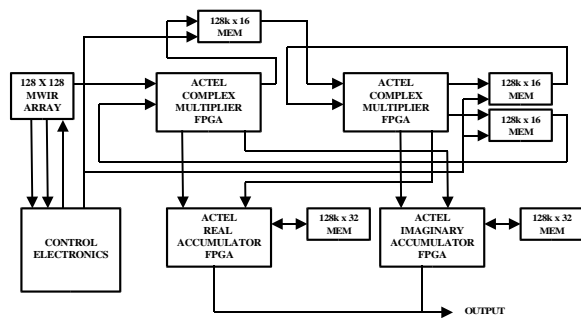

Figure 7: Implementation of the MWIR multi-rate complex polyphase filter.

As seen in the Figure, memory array addressing provided by the control electronics selects the proper memory block range as a function of the selected polyphase filter. As

each sample is serially read out of the FPA during a frame scan, the control electronics call up the memory pipeline locations for the same sample number from previous scans so that the proper sample information from frame scan n, $n + 8$, $n + 16$, and $n + 24$ arrive at the filter tap input at the proper time. The same clock cycle that loads data into the multiplier chip shifts the data in the memory pipeline, making the next sample information available for the next clock cycle. The multiplier chip outputs the final result after 9 clock cycles.

The multiplier building block FPGA for each complex polyphase filter for the MWIR band is given in Figure 8. Each of the Actel multiplier FPGAs has two multiplier sec-
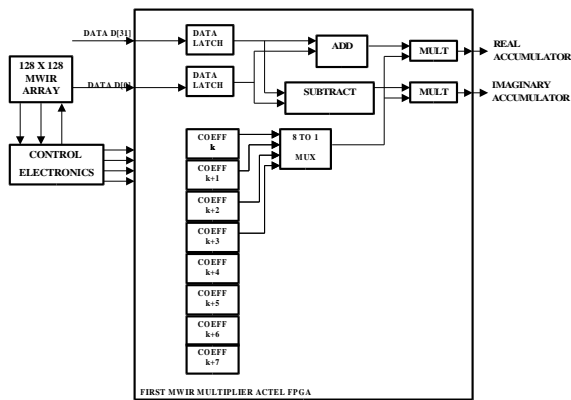

Figure 8: Basic complex multiplier FPGA block diagram.

tions, one for the real component and one for the imaginary component. As shown in the figure, the sum and difference of the input samples is computed to take advantage of the conjugate symmetry of the complex filter. Prior to a scan of the MWIR FPA, the proper coefficients for the polyphase filter ($G(0), G(8), g(16)$, and $G(24)$ for G_0; $G(1), G(9), G(17)$, and $G(25)$ for G_1; $G(2), G(10), G(18)$, and $G(26)$ for G_2, etc.) are loaded onto the corresponding multiplier units. Since the coefficients are the same for each of the 16k interferograms, the coefficients do not need to be changed during a sample of the FPA.

The output of each multiplier FPGA is fed into the accumulator section shown in Figure 7, where the final sum for the selected complex polyphase filter is stored until it is recalled and added with the sum of the other complex polyphase filter sections. It takes 32 scans of the MWIR array before the accumulator outputs the first valid scan sample. After that, a valid sample is output every eight array scans.

4. LWIR FILTER HARDWARE DESIGN

The LWIR is bandpass filtered and decimated in a two-stage multi-rate polyphase structure. The LWIR pre-filter stage is the eight-tap decimate-by-two real filter shown in Figure 9. Using coefficient symmetry and polyphase techniques, this eight tap filter is reduced to just two multiplier stages and an accumulator. Since it is a real filter only one 32-bit accumulator is required.
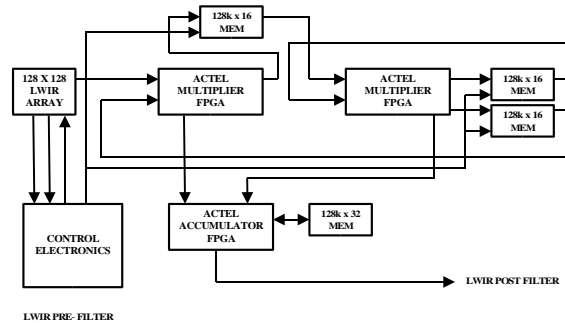

Figure 9: LWIR pre-filter block diagram.

The first multiplier FPGA for the LWIR pre-filter is shown in Figure 10. Here the symmetry of the filter coefficients is
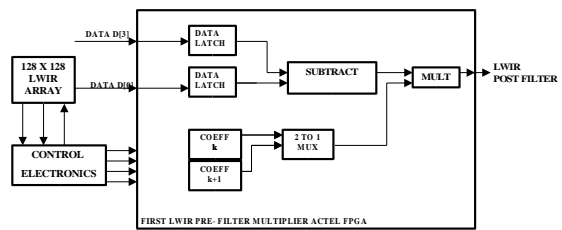

Figure 10: LWIR pre-filter multiplier FPGA block diagram.

exploited by taking the difference of the input samples before the multiplication by the filter coefficient.

Using coefficient symmetry and polyphase techniques, the 64 tap decimate-by-eight LWIR complex post-filter is reduced to just four multiplier stages, as shown in Figure 11. Since it is a complex filter it uses the same multiplier block used by the MWIR filter (see Figure 8). In Figure 11, the pipelined memory architecture is clearly visible.
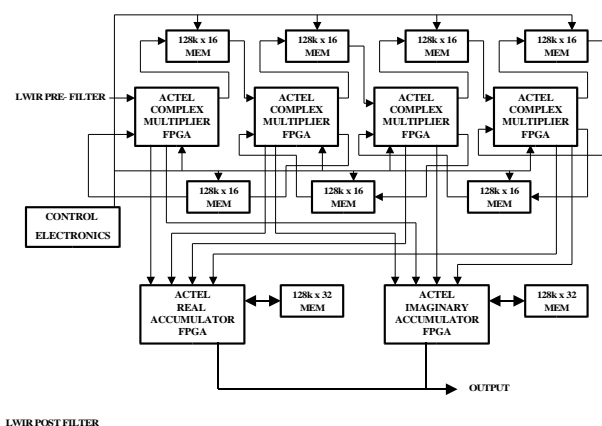
Figure 11: LWIR post-filter block diagram.

5. SUMMARY AND DISCUSSION

In this paper we have presented an efficient, parallel, memory pipelined architecture to implement filter-decimators for the dual FPA GIFTS interferometer. The design exploits the computational rate savings available from cascaded multirate structures and the symmetry of the decimation filter coefficients due to linear phase constraints. The design presented here is currently in the process of prototype development and testing. Simulation, preliminary layout, and chip counts all indicate that the strict requirements for size, weight, power, processing speed, and radiation tolerance necessary for a satellite design will be met by this architecture.

6. ACKNOWLEDGEMENTS

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7. REFERENCES

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