THE JOHNS HOPKINS UNIVERSITY
APPLIED PHYSICS LABORATORY
LAUREL, MARYLAND

SPACE - RADIATION QUALIFICATION OF A MICROPROCESSOR IMPLEMENTED FOR THE INTEL 80186

R. H. Maurer, J. D. Kinnison, B. M. Romenesko, B. G. Carkhuff, and R. B. King
Johns Hopkins University Applied Physics Laboratory
Laurel, Maryland 20707

WPC 88-356

SPACE - RADIATION QUALIFICATION OF A MICROPROCESSOR IMPLEMENTED FOR THE INTEL 80186

R. H. Maurer, J. D. Kinnison, B. M. Romenesko,
B. G. Carkhuff, and R. B. King
Johns Hopkins University Applied Physics Laboratory
Laurel, Maryland 20707

ABSTRACT

The Intel 80186 sixteen-bit microprocessor is an example of a high performance device (8 MHz) needed to carry out advanced experimentation on Low Earth Orbit missions. However, this key complex microprocessor is not space-qualified. We will discuss the procedures necessary to qualify a microprocessor for the natural space radiation environment. We also present the results from our single event upset tests on the 80186. The upset cross-section exhibited a threshold of 0.4 MeV•cm^2/mg, a knee at 7 MeV•cm^2/mg and an asymptotic value of 5×10^{-4} cm^2. The upset cross-section did not depend on frequency in the 4-8 MHz range and increased by 40% when conductive heat sinking was eliminated causing a 50°C temperature rise. Finally, we show how to estimate the single event upset rate for a typical low earth orbit mission.

I. INTRODUCTION

The need for advanced computing power has increased as space systems have grown more complex. Designers want faster microprocessors than those currently space-qualified, as well as ones with the lower power requirements found in newer technology; this desire for better performance often means using non-qualified parts and qualifying them. Radiation testing is a crucial part of the qualification process. Any microprocessor selected should be able to withstand the damage seen in the orbital environment due to accumulated dose and should be free from latch-up due to energetic heavy ions. Since heavy ions can also cause soft errors within digital devices, the ability to predict upset rates is necessary to completely characterize a microprocessor. The purpose of this paper is to summarize radiation test methodologies with respect to the schedule and cost constraints associated with the development of small satellite digital systems. In particular, we will discuss several different methods of measuring the susceptibility of microprocessors to single event upset. We will give the results of our evaluation of the Intel 80186 microprocessor as an example of the implementation of the radiation test methodology.

II. RADIATION TEST METHODOLOGY

A. Total Dose Testing

There are essentially two ways to test the susceptibility of a microprocessor to accumulated radiation dose. The first is to test the functionality of the device while it is exposed to radiation - typically protons, electrons, gamma rays, or X rays. This method is usually easier to implement than other methods and gives the dose at which the device ceases to function. Unfortunately, functionality of the microprocessor is sometimes not the only important criterion for use; radiation often causes an increase in the standby and operating currents of the part, which means it uses more power. Thus, a device may be functioning while the increase in power consumption makes it unusable. The second method tries to remedy this problem: if the part is exposed to the dose we expect it to receive in orbit, and then the AC and DC parameters are measured along with the functionality of the device, we know how well the device will operate after the desired exposure. In practice, the parameters are measured at intermediate dose levels as well, to give a complete characterization of the radiation response. This method usually requires much more sophisticated test equipment and more time to set up the test, while yielding information that is limited by the number of intermediate levels at which the device is tested. Removing samples from the radiation test chamber and making parametric electrical measurements at a remote location also introduces uncertainties related to the radiation dose rate, the period of potential annealing between cessation of radiation and beginning of measurement and the bias conditions prevailing throughout these periods. Our test scheme combines both methods to give not only parameter data at specific dose levels, but also a correlation with the DC parameter values at which the 80186 stops functioning.

B. Single Event Upset Testing

A single energetic ion traveling through a semiconductor device loses energy mainly by ionizing the material as it passes; the induced photocurrent is a short duration, large amplitude pulse. The major effects of this photocurrent are:

1. transient upset in which there is a bit flip (non-destructive);

2. permanent failures, such as junction burnout due to large currents induced during low voltage states.

The first is called single event upset (SEU) and the second is known as single particle induced latch-up,[1] a phenomena usually associated with bulk CMOS semiconductor technology.

Since latch-up is a permanently damaging condition, it is important that any microprocessor used in space applications be latch-up free. Generally, the only way to test for this is to expose the microprocessor to a heavy ion beam. If the device stops working, draws current in excess of operational values, and needs a power reset to restart it, a latch-up has occurred. Typically, the fission fragments of Californium-252 are used for latch-up screening because it can be done inexpensively in one's own laboratory.[2,3,4]

It is also important to be able to predict the number of soft errors caused by single event upset. The error rate of a device is determined by both the number of particles interacting with the device and by the susceptibility of the part to upset. The error rate of a device, N, is given by

$$N = s * F. \qquad (1)$$

Here, F is the particle flux in particles/(area*time) and s is the effective interaction cross-section with units of area. Both s and F are functions of the amount of energy deposited in the material per unit length, also called the linear energy transfer (LET). If we can measure s, then we can predict the error rate for any environment.[5,6,7]

A device cross-section is virtually zero at low LET values. As the LET increases past a threshold value, the cross-section rises sharply. This sharp rise continues over a short range of LET values; beyond this range, the cross-section reaches a knee and begins a gradual approach to an asymptotic value. The LET values at which the threshold and knee occur play an important role in accurately determining the error rate, so it is important to determine these values as well as the asymptotic cross-section. The most straightforward way of finding these parameters is to put the device in a monoenergetic ion beam and to measure the error rate. Eq. (1) then gives the cross-section for the

LET value of the beam. Repeating this over many LET values (the same ion with different energy or different ion species) produces a complete SEU characterization of the device.

Perhaps the most interesting and complex part of the problem is the measurement of the error rate. A microprocessor must be exercised such that all possible soft errors are tested. Both dynamic logic gates and static registers should be tested. Five methods of exercising the microprocessor and detecting errors are

1. Self-test: use a single board computer to self-test the microprocessor; errors are reported to a CRT, etc.

2. Controller-Assisted Single Computer Method: the microprocessor, in a single board computer, executes a set of instructions and periodically sends the results to a controller. The controller compares these results to a "correct" set in its memory to detect errors.

3. Controller-Assisted Golden Chip Method: the microprocessor under test and a chip not subjected to irradiation execute the same instruction set. The controller compares the output of both devices.

4. Controller-Dominated Single Computer Method: the microprocessor is fed instructions one at a time by the controller, which checks for errors as each instruction is executed.

5. Controller-Dominated Golden Chip Method: the controller feeds instructions to both the tested microprocessor and a device not under test. At each step, the outputs of both are compared.[8]

Fig. 1 is a summary of the advantages and disadvantages of each method (from Koga, et al.).[8]

III. IMPLEMENTATION ISSUES

The Intel 80186 is a 16 bit, 8 MHz microprocessor. Functionally, the device can be broken down into seven blocks interconnected by an internal bus. Fig. 2 shows a block diagram of this device. Blocks such as the DMA Controller, the Interrupt Controller, and Chip Select Unit are common peripherals that in this case have been integrated onto a single chip with the CPU. This architecture allows the higher throughput needed for some high-speed space applications. This 80186 is available in a military package and for military temperature ranges, but is not space qualified.

The total dose hardness was measured using Cobalt 60 gamma rays at 1.25 MeV. The device was exercised while under irradiation with a single board computer running an instruction set intended to check the functionality of each block of the microprocessor in turn. At periodic intervals, the AC and DC parameters of the device were measured to monitor any timing and power consumption degradation. This test represents a combination of the two methods discussed above and is designed to maximize the amount of information collected at the price of increasing the complexity of the test.

The single board computer hardware configuration was also used in the single event upset test. We chose to implement test method 2 (controller assisted single computer method) with an IBM PC-AT as the controller. Our test had five main objectives: to measure the device SEU cross-section as a function of linear energy transfer, to test the angular dependence of the cross-section, to study the effect of higher operating temperatures on the error rate, to determine the frequency dependence of the cross-section, and to identify the most sensitive areas of the chip.

We performed these tests at the Brookhaven National Laboratory SEU Test Facility. This facility consists of a three stage Van de Graaff accelerator and associated test chamber designed to allow efficient experimental set-up and execution (see Fig. 3). All beam calibration and diagnostics, vacuum system, and device positioning functions have been fully automated so that the user interface is as friendly as possible. Fig. 4 shows the SEU test hardware configuration at Brookhaven.

To conduct the SEU test, several electronics packaging matters had to be addressed. First, the microprocessor test article had to be physically held in the ion beam inside the test chamber. This was done by mounting the device on a test plate attached to the position control system provided by the SEU Test Facility at Brookhaven. Second, a power dissipation of up to three watts required attention to thermal control. Third, the microprocessor had to function electrically as part of the single board computer residing outside the vacuum chamber.

The 80186 was contained in a "quadpack," a ceramic package with leads coming laterally out all four sides; the package leads were soldered to a printed circuit test board in which a hole was cut to pass the package body (Fig. 5). The soldered-on package lid was removed (by peeling off with a sharp knife) to expose the die to the ion beam. For thermal control, the bottom of the package was put in contact with a brass stud mounted on the test plate; a small quantity of thermal grease was used to assure a low and reproducible thermal resistance. The test plate was cooled with a cooling water loop inside the vacuum chamber provided by the Brookhaven SEU Test Facility. With this cooling arrangement, a temperature monitor on the package body indicated a temperature rise of only 4 to 5 degrees C above ambient while operating in vacuum.

To make the microprocessor function electrically while physically separate from the single board computer required careful design. Printed traces on the test boards brought the signals to three connectors on the periphery of each board. To minimize cross talk, twisted pair ribbon cable was used, with one wire of every pair being a ground wire. An input clock buffer was added to the test board to assure a clean clock input to the microprocessor under test; although a clock waveform coming from the single board computer was considerably distorted by the added capacitance of approximately 10 feet of cable, the microprocessor functioned without difficulty using the buffered clock.

IV. 80186 TOTAL DOSE RESULTS

Total dose testing of the 80186 microprocessor from several different manufacturing processes has been carried out at Harry Diamond Laboratories and at APL. Results on total dose hardness levels of 16 and 32 bit microprocessors have become information restricted by the Arms Export Control Act (export controlled technical data). These results are available only to U.S. citizens.

V. 80186 SEU RESULTS

The SEU cross-section was measured using five different ions at normal and 60 degree incidence over four devices. We found that for each ion, there was an increase in the error rate at 60 degrees incidence. As the angle of incidence becomes more oblique, the track length of the ion within the active region of the device increases, which increases the LET value. The increase in the error rate that we found was caused solely by the increase in LET value due to the increased path length; the cross-section has only a geometric and no dynamic angular dependence.

The results of the first experiment allowed us to use both the normal and oblique incidence measurements in the characterization of the SEU cross-section. This result is shown in Fig. 6. The threshold occurs at about 0.4 MeV*cm^2/mg, and the knee at 7 MeV*cm^2/mg. The asymptoptic cross-section is $5*10^{-4}$ cm^2. This information will be used to make a prediction of the device error rate in a low Earth orbit (LEO).

The operating temperature of the microprocessor was monitored throughout the experiment. It was typically 28 degrees C with little variation. At the end of our tests, we allowed the temperature to rise to 80 degrees C and measured the cross-section at an LET of 11 MeV*cm^2/mg. We found that the cross-section increased by about 40%.

We also reduced the clock frequency by a factor of 2 (to 4 MHz) and measured the cross-section over an LET range of 0.4 - 11 MeV*cm^2/mg. In this case, we found that the upset cross-section did not change.

By masking approximately one-half to three-quarters of the 80186 chip with glass slides and using a laser to align, place and focus the particle beam we were able to make a crude comparison of the four quadrants of the chip with respect to upset sensitivity. The quadrant containing the Direct Memory Access (DMA) Controller and possibly some of the register files upset at a rate about four times greater than any of the remaining three quadrants. We used the silicon ion beam at normal incidence for this study; thus, we were on the asymptotic portion of the cross-section curve of Fig. 6.

VI. ORBITAL ERROR RATE ESTIMATE

The single event upset cross-section contains all the information about how the device susceptibility changes as the type and energy of the ion is changed or as the incident angle between the beam and device is changed. Since we observed no intrinsic angular dependence up to an angle of 60° with respect to the normal to the 80186 chip in our experiments, the increased upset rate observed at oblique angles was due solely to the increased linear energy transfer caused by the increased path length through the chip.

$$(\mathrm{LET})_{\mathrm{oblique}} = (\mathrm{LET})_{\mathrm{normal}}/\cos\theta \qquad (2)$$

where θ is the angle of incidence with respect to the normal. We assumed that the SEU cross-section had no intrinsic angular dependence for all angles of incidence. Thus, by using Eq. (2) we have found that the cross-section, s, is only a function of LET. This result is usually the case but one must be careful when complex dynamic logic circuits are involved. The function F in Eq. (1) is the omni-directional integral particle flux in particles per square centimeter per day available from the work of Adams.[5] Fig. 7 is a plot of this flux spectrum for a 1300 km altitude, 60° inclination orbit behind 200 mils of aluminum shielding.

The error rate is then computed from an integral over the product of the particle flux (Fig. 7) with the cross-section (Fig. 6) between the threshold LET of the device (L min) and the effective cut-off LET of the natural environment (L max). Eq. (1) becomes

$$N = \int_{L\,\mathrm{min}}^{L\,\mathrm{max}} \frac{dF(L)}{dL}\, s(L)\, dL \qquad (3)$$

where L is used as shorthand notation for LET. The error rate, N, is in upsets per day. dF/dL is the omni-directional "differential" flux – but it is only differential in LET. The integral is done numerically using the trapezoidal rule, so that

$$N = \sum_{i=1}^{m} \bar{\sigma}_i \Delta F_i \qquad (4)$$

where $\bar{\sigma}_i$ is the average cross-section for the ith ΔL interval and ΔF_i is the number of particles in the same interval. The sum occurs over all intervals from the device threshold to the natural environment cut-off. The reason for the numerical integration is that simple continuous analytic functions for s(L) and F(L) are difficult to define over the complete range of LET. Doing the summation of Eq. (4) gives an estimate of

$$N = 0.0043 \text{ errors per day}$$

which is one error every 230 days due to the ionization of cosmic ray ions.

Since the 80186 microprocessor has an LET threshold of less than 0.4 MeV*cm^2/mg, it is also susceptible to upsets from proton-initiated nuclear reactions in the silicon. Experiments have shown that this is generally true for devices with thresholds below 6 MeV*cm^2/mg. There are two basic physical mechanisms for an upset of this type; they are

$$p + Si \rightarrow \alpha + \text{other products}$$

$$p + Si \rightarrow \text{Heavy ion (e.g., Mg)} + \text{other products}$$

in which the alpha or heavy ion recoil deposits the ionization charge needed to cause upset.

Following the method of Petersen [6,7], we know that the probability of a proton initiating a nuclear reaction (for the naturally occurring energy range) is $3.6*10^{-5}$. This means that an average of 3.6 out of every 100,000 protons striking the device will lose their energy by nuclear reaction instead of by ionization. Many nuclear reactions are possible, but only a few can cause upset. The total atomic cross-section for the p+Si reaction is 700 millibarns (mb), but the cross-section for a reaction producing a heavy recoil is only 20 mb. Similarly, the cross-section for a reaction that produces alpha particles is 220 mb. Thus, the probability per proton of obtaining a heavy ion secondary is $(20/700)*3.6*10^{-5} = 1.02*10^{-6}$, and the probability per proton of obtaining a secondary alpha particle is $(220/700)*3.6*10^{-5} = 1.13*10^{-5}$.

Now, the heavy recoil ions usually have an LET in the asymptotic region of the device cross-section, and the alpha particles usually have an LET value near the device threshold. When we multiply the device cross-section per bit (or bistable element) with the probability of reaction per proton,

$$(\text{Fission Probability})*\sigma_{asymp} + (\alpha \text{ probability})*\sigma_{thresh} = 5.9*10^{-14} \text{ Upsets*cm}^2\text{/proton*bit}$$

where we have assumed that there are 10,000 sensitive bistable elements in the 80186 and used the appropriate cross-section values from Fig. 6. The 5.9×10^{-14} number provides a figure of merit called the A parameter which can be used to compare with data on other devices (see Ref. 10). The A parameter for the 80186 is 23.5 MeV. In a 1330 km, 60 degree inclination orbit, a device such as the 80186 will experience $3*10^{-5}$ upsets per bit-day using the method of Ref. 9. Scaling by the number of bits gives an error rate of 0.3 upsets per day.

The error rate due to primary heavy ions is 0.0043 upsets per day, and the error rate due to proton initiated reactions is 0.3 upsets per day. The total error rate, then, is just the sum of these two components:

$$N = 0.0043 + 0.3 = 0.3043 \text{ upsets/day}$$

or, one upset every 3.3 days. Since the proton initiated upsets dominate, it does not matter whether we use a nominal solar maximum or 90% worst case environment for the cosmic rays[5].

One final problem remains. The mission will be exposed to periods of increased solar activity during the solar maximum epoch circa 1991. Anomalously large solar events similar to the August 1972 event may occur. Using the work of Adams and Gelman[11] and Chenette and Dietrich[12] we estimate that the upset rate due to ionization can increase by a factor of 1000 at a shield depth of 200 mils aluminum. These large events typically last from 12-72 hours depending on the size of the flare, its emission spectrum and the position of the spacecraft relative to the interplanetary magnetic field lines which emanate from the sun. The total error rate in this case becomes (worst case)

$$N_{max} = 4.3 + 0.3 = 4.6 \text{ upsets/day}$$

or one upset every 5 hours.

VII. CONCLUSIONS

The need of many space systems designers for the performance of more recent technology demands an understanding of the changes in the performance of new devices in a space radiation environment. We have summarized the most widely used methods for space-qualifying a microprocessor. We have described our testing of the Intel 80186 microprocessor as an example of one implementation of these methods. The single event upset cross-section is shown in Fig. 6. For a typical low earth orbit mission at solar maximum, we have calculated an upset or error rate of 1 upset every 3.3 days with a worst case estimate of one every 5 hours during an anomalously large solar flare.

The upset cross-section did not depend on frequency in the 4-8 MHz range and increased by 40% when conductive heat sinking was eliminated resulting in a temperature increase of 50°C. The quadrant of the chip containing the Direct Memory Access (DMA) Controller and some register files was approximately four times more sensitive to upset than any of the remaining three quadrants.

ACKNOWLEDGEMENT

The authors acknowledge the cooperation of Bob Ferrar of Intel Corporation in supplying a map of the 80186 die.

REFERENCES

1. F. B. McLean, "Interactions of Hazardous Environments with Electronic Devices," IEEE Nuclear and Space Radiation Effects Conference, Short Course, Snowmass, Colorado, July 1987.

2. J. H. Stephen et al., "Cosmic Ray Simulation Experiments for the Study of Single Event Upsets and Latch-up in CMOS Memories," IEEE Trans. Nucl. Science NS-30, p. 4464, 1983.

3. J. H. Stephen et al., "Investigation of Heavy Particle Induced Latch-up Using a Californium-252 Source in CMOS SRAMs and PROMs," IEEE Trans. Nucl. Science NS-31, p. 1207, 1984.

4. J. T. Blandford, Jr. and J. C. Pickel, "Use of Cf-252 to Determine Parameters for SEU Rate Calculation," IEEE Trans. Nucl. Science NS-32, p. 4282, 1985.

5. J. H. Adams, Jr., "The Variability of Single Event Upset Rates in the Natural Environment," IEEE Trans. Nucl. Science NS-30, p. 4475, 1983.

6. E. L. Petersen, "Single Event Upsets in Space: Basic Concepts," IEEE Nuclear and Space Radiation Effects Conference, Short Course, Gatlinburg, Tennessee, July 1983.

7. E. L. Petersen, "Soft Errors Due to Protons in the Radiation Belt," IEEE Trans. Nucl. Sci. NS-28, p. 3981, 1981.

8. R. Koga et al., "Techniques of Microprocessor Testing and SEU-Rate Prediction," IEEE Trans. on Nucl. Sci. NS-32, p. 4219, 1984.

9. W. L. Bendel and E. L. Petersen, "Proton Upsets in Orbit," IEEE Trans. on Nucl. Sci. NS-30, p. 4481, 1983.

10. W. L. Bendel and E. L. Petersen, "Predicting Single Event Upsets in the Earth's Proton Belts," IEEE Trans. Nucl. Sci. NS-31, p. 1201, 1984.

REFERENCES (Cont'd.)

11. J. H. Adams, Jr. and A. Gelman, "The Effects of Solar Flares on Single Event Upset Rates," IEEE Trans. Nucl. Sci. NS-31, p. 1212, 1984.

12. D. L. Chenette and W. F. Dietrich, "The Solar Flare Heavy Ion Environment for Single-Event Upsets...," IEEE Trans. Nucl. Sci. NS-31, p. 1217, 1984.

	Self – Test	Single Computer Assisted	Golden Chip Assisted	Single Computer Dominated	Golden Chip Dominated
Effective Clock Frequency	High	Medium	Medium	Low	Low
Individual Element Testability	Low	High	High	High	High
Error Table Structure	Simple	Complex	Complex	Complex	Complex
Test Preparation Lead – time	Short	Medium	Medium	Medium	Long

Figure 1. A comparison of the five test methods (Koga, et. al.)

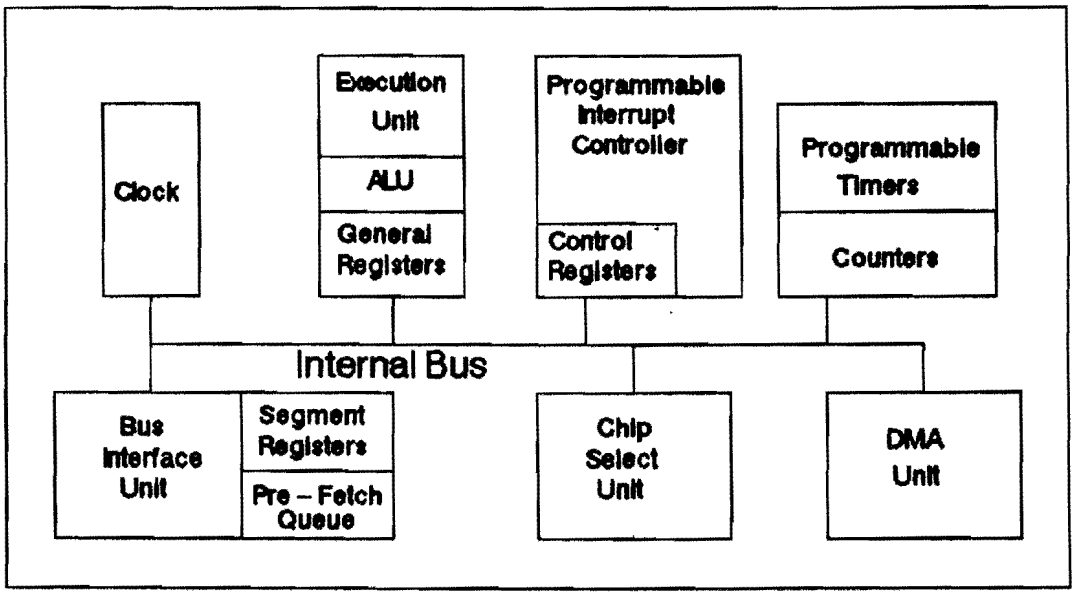


Figure 2. Block Diagram of the Intel 80186

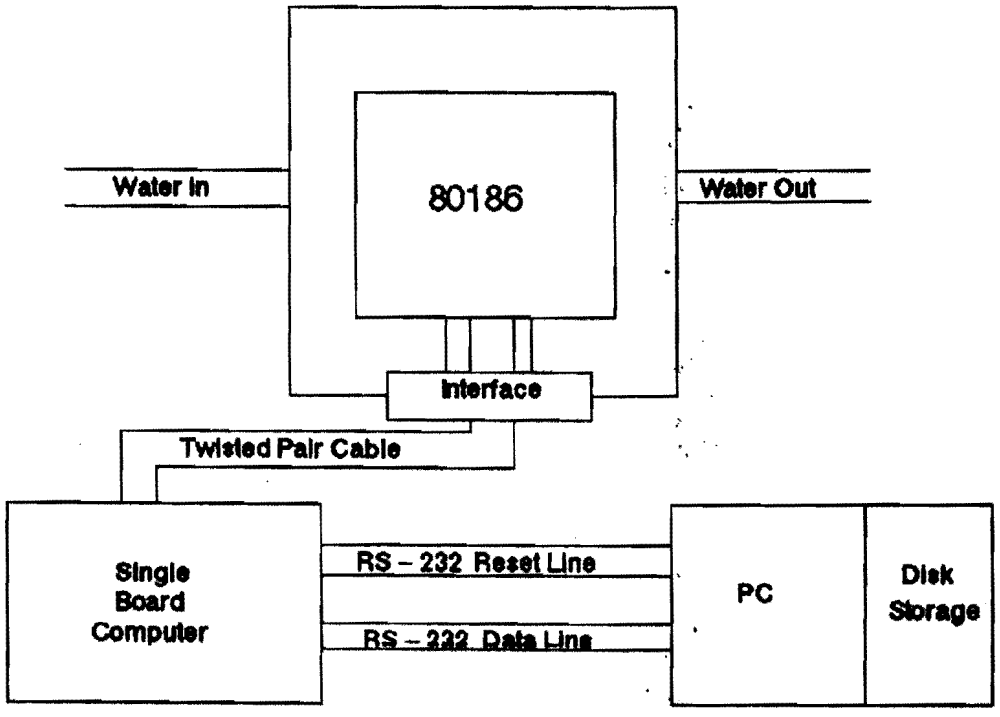
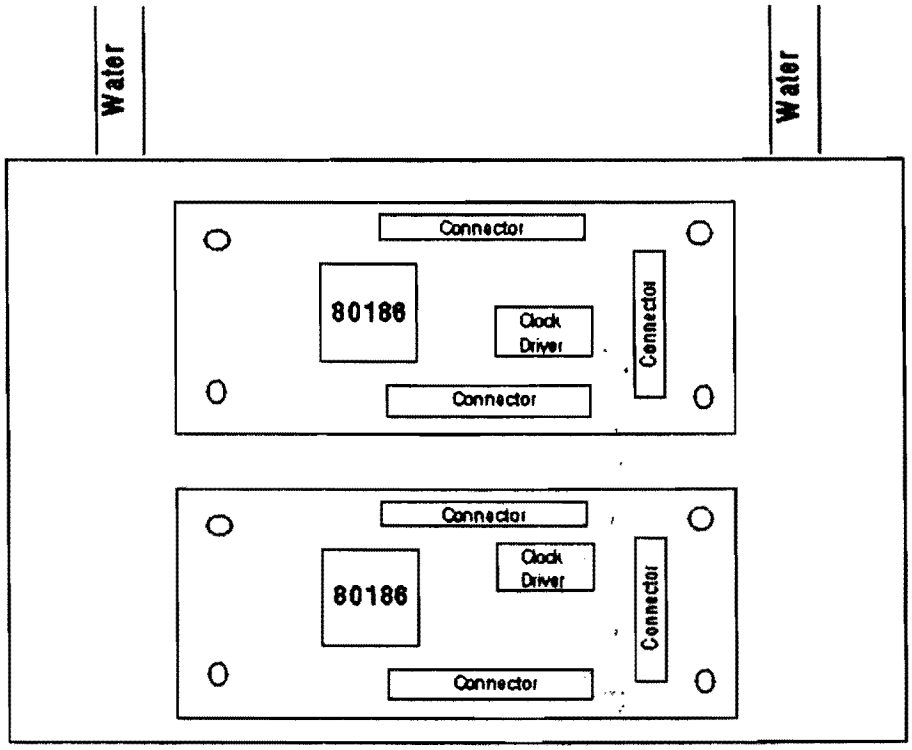
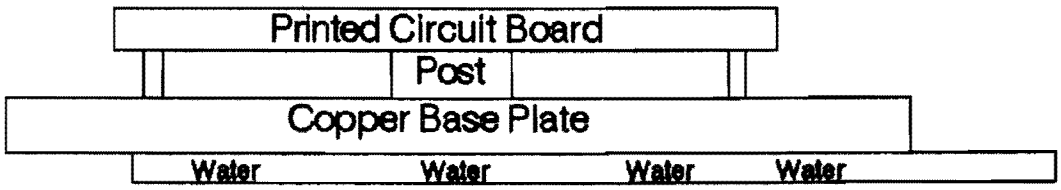


Figure 3. Controller – Assisted SEU Test Configuration for the 80186



a. Front View



b. Side View

Figure 4. Mounting of 80186 in test board.

SEU EXPERIMENT AND TEST FACILITY

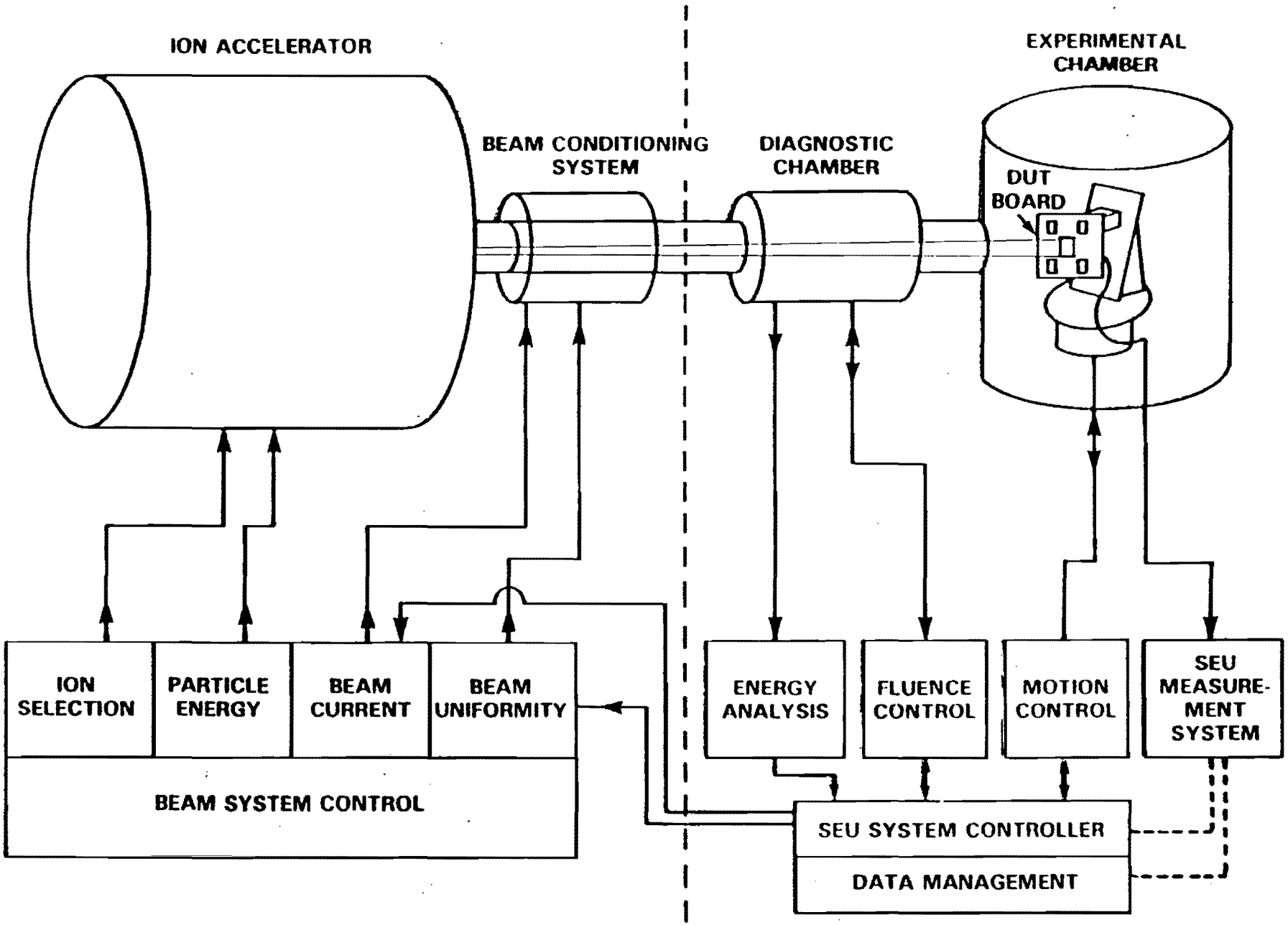


Figure 5. Brookhaven Tandem Van de Graaff Generator Experimental Chamber

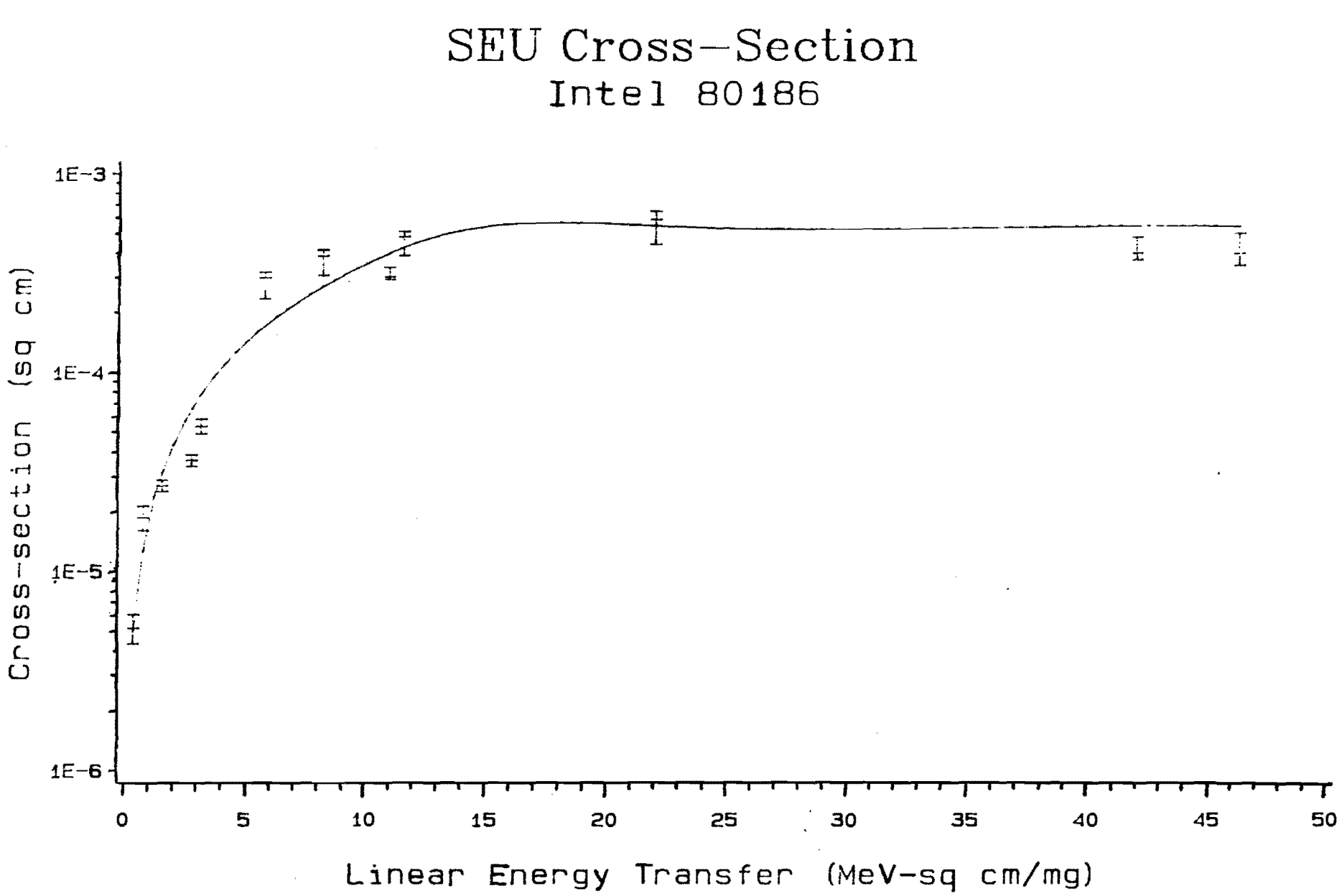


Figure 6. 80186 single event upset cross-section

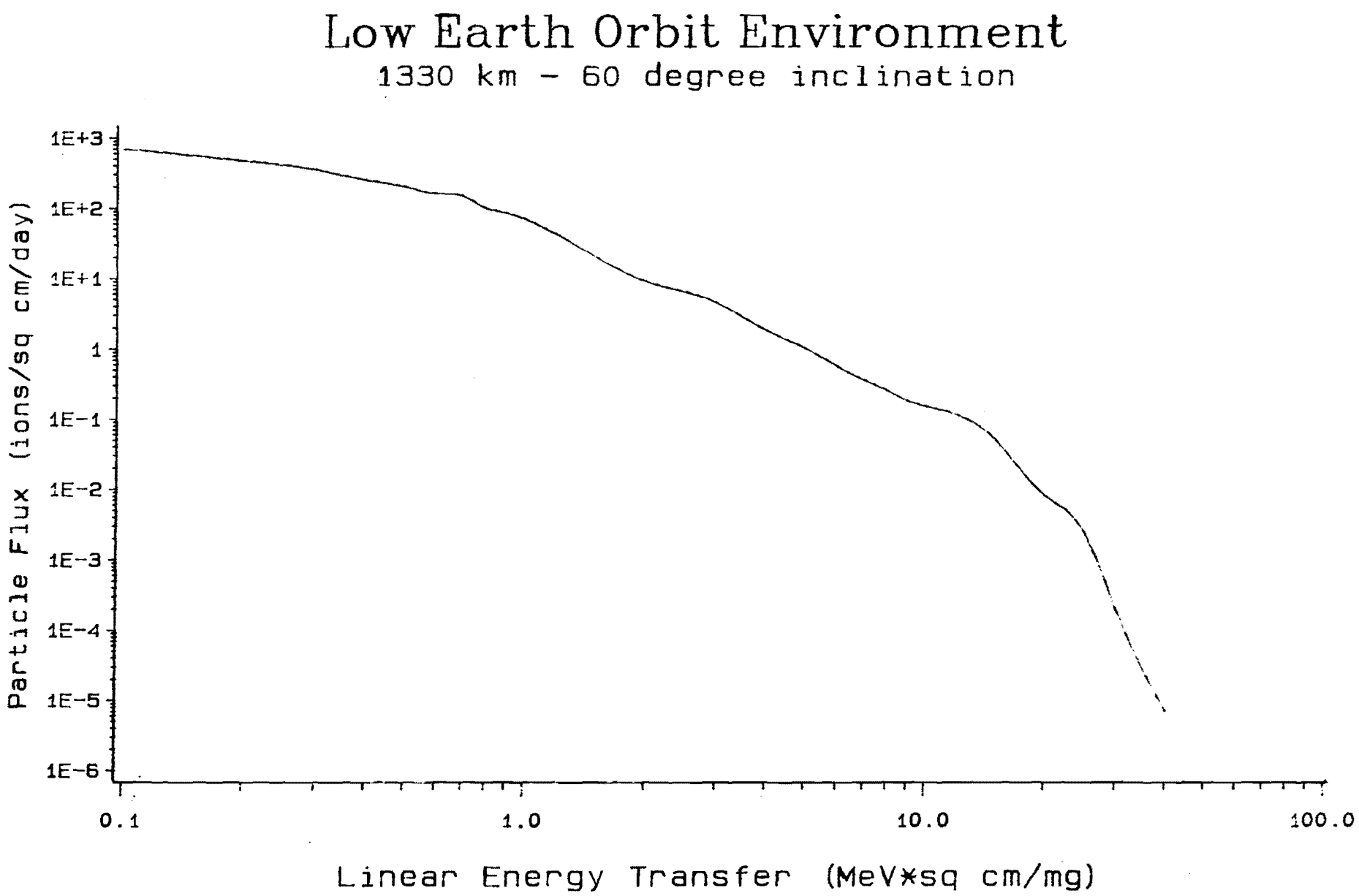


Figure 7. Heavy ion flux for 200 mils of Al.