Command and Data Handling In Your Palm

R.F. Conde, B.Q. Le, J.F. Bogdanski, A.L. Lew, J.A. Perschy
The Johns Hopkins University Applied Physics Laboratory
Johns Hopkins Road
Laurel, MD 20723
(301) 953-5000 x8876

Ann Garrison Darrin
National Aeronautic and Space Administration
Goddard Space Flight Center
Code 310
Greenbelt, MD 20771
(301) 286-8884

The shift in emphasis to smaller, better, and cheaper spacecraft, resulting from the NASA New Millennium Program (NMP) and similar initiatives in DoD-sponsored programs, demands highly innovative designs that standard electronic packaging cannot meet. Current technology primarily uses conventional packaging with surface mounted or through hole components. This approach increases the board size and the overall system weight owing to the larger sizes of the board and the components mounted on it. Chip-on-Board (COB) technology, where active dice are directly mounted onto a substrate without the need for an intermediate package, provides the basic vehicle to miniaturize electronic hardware. This technology allows the use of both bare dice and packaged components when parts availability, cost and schedule become major factors influencing design decisions. In a cooperative effort between The Johns Hopkins University Applied Physics Laboratory (JHU/APL) Space Department and the Goddard Space Flight Center Code 310 Assurance Technologies Division, a family of miniaturized, stackable electronics modules is under development. These modules can implement anything from a standalone Instrument Processor, to a Command & Data Handling system, or the entire electronics needed by a spacecraft. The small size of these modules makes them ideal for use in small satellites.

Introduction

The Johns Hopkins University Applied Physics Laboratory (JHU/APL) has invested in Chip On Board (COB) technology development for several years. This technology makes use of standard wire bonding techniques, appropriate coatings, and the availability of Known Good Die (KGD) and low cost commercial die to enable the production of low cost, miniaturized flight hardware. The Goddard Space Flight Center Code 310 Assurance Technologies Division is also interested in COB technology and has joined with JHU/APL in the Command and Data Handling In Your Palm (C&DH IYP) project. The goal of the C&DH IYP project is to produce a family of miniaturized, stackable electronics modules whose development is made possible with the use of COB and other technologies developed by JHU/APL. These modules can be stacked up in varying combinations for different applications. Currently, three modules are in development: an RTX2010 Processor and I/O module; a Solid State Recorder module; and a Mongoose V Processor and I/O module.

System Concept and Architecture

A combination of stackable connector technology, COB technology, and a JHU/APL designed IEEE-1394 protocol chip allows the design of miniature stackable electronics modules which can be assembled into systems with minimal non-recurring costs. A block diagram of a system assembled from four stackable modules is shown in figure 1. This system is 4.0" x 4.0" x 2.0" in size and weighs about 20 ounces. A family of modules is being developed that will allow a variety of flight systems to be built.

Module Design

In order to produce low cost miniature flight systems, both recurring and non-recurring costs must be minimized. Electronics systems have been traditionally packaged as daughter cards plugged into a custom backplane that is housed in a custom chassis. Even if board designs are re-usable from project to project, usually a new chassis and motherboard are required because the total number of boards has changed. Technology now permits the design of
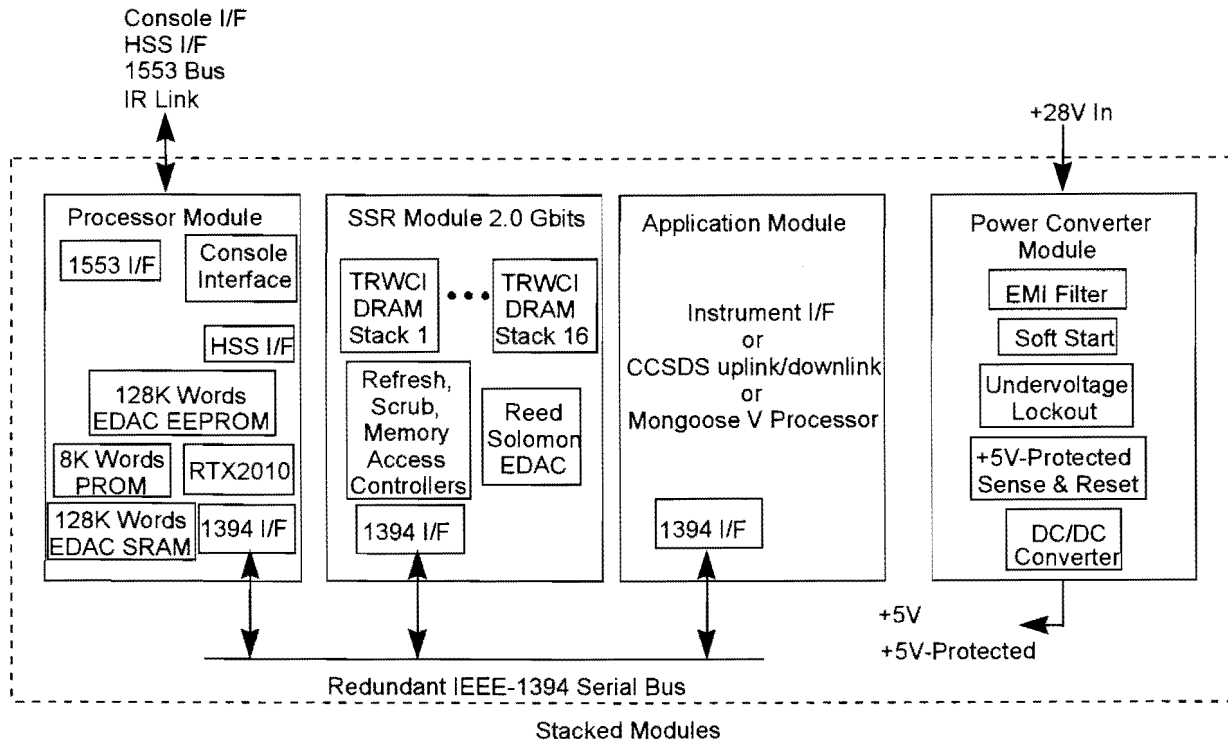
Figure 1. C&DH IYP Block Diagram

stackable electronics modules that are electrically connected through stackable connectors. The connectors themselves form a scaleable motherboard that extends as far as the number of modules in the stack. No unique motherboard is required.

Each module weighs about 5 ounces and consists of a 4.0" x 4.0" x 0.5" aluminum frame that encloses a small polyimide multi-layer PC board. The frame functions as a handling fixture during fabrication and test of an individual module, and becomes part of the flight chassis as modules are stacked up. Only two standard end plates need to be added to complete the flight chassis. Two modules containing test boards used in vibration and thermal vacuum testing of the stackable connector are shown in figure 2.

Module Size

The module size, 4.0" x 4.0", allows several packaged parts to be used on each board in addition to dice. This is a reflection of the fact that not all ICs can be economically obtained in die form, so that in many designs it is necessary to use some packaged parts. If a smaller area were used, a few packaged parts could crowd out many dice and overly limit the number of parts in module. The module height, 0.5", provides

enough room for dice and most packaged parts. If the height is insufficient for a particular part, either a thicker frame can be used, or the adjacent module can be examined to see if the tall part can be allowed to intrude into its space.

Intermodule Communication

A critical aspect of the architecture is how the modules communicate with one another. The primary decision is serial bus or parallel bus. A parallel bus offers higher throughput, but at the expense of more pins, greater power, and more board area required on each module. A serial bus can be implemented with less board area and lower power but with lower throughput. The approach taken is to use a serial bus as the primary means of communications between modules, and to use a connector that can be expanded to allow for implementation of a local parallel bus between adjacent modules when greater throughput is required.

The serial bus selected is the IEEE-1394 "Firewire" bus that has been developed for commercial applications. The Firewire bus is not just an I/O channel; it is a read/write memory architecture in which data packets are sent between nodes on the bus. IEEE-1212 addressing is used on the bus. Packet

2

generation, transmission, and reception is largely transparent to the user. A protocol chip designed by JHU/APL implements most of that functionality, much like MIL-STD-1553 protocol chips implement it in a 1553 bus.

Use of Commercial Grade Parts

In order to meet cost and performance goals, more and more commercial chips are being incorporated into spacecraft electronics. Many commercial chips have adequate radiation total dose, but some chips will latchup due to high energy particles. In order to be able to use these chips, the C&DH IYP DC/DC Converter module will have a +5V-Protected bus in which the current is sensed and maximum current is limited. If a part latches up on this power bus, the current limit will prevent the part from being damaged, and the DC-DC converter will automatically cycle power to all the modules in order to extinguish the latchup and allow normal operation to resume. Presently only one part type (a Chip Express gate array) is used that is susceptible to latchup.
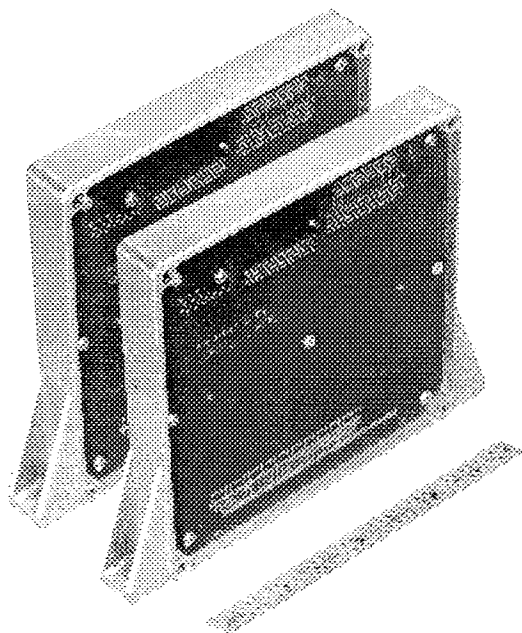

Figure 2. Modules with Test Boards

Technology

IEEE-1394 Protocol Chip

JHU/APL has designed a protocol chip that implements the IEEE-1394 standard. The chip is fabricated on a Chip Express Laser Programmed Gate Array (LPGA). The chip allows implementation of the bus with minimal board area. This makes it especially suitable for miniaturized applications such as C&DH IYP where board space is at a premium. The IEEE-1394 standard includes features that are desirable for high reliability applications. The standard implements a flexible memory mapped architecture. Asynchronous and low latency block transfers are defined. Fair bus arbitration allows all bus users to be serviced. Extensive error detection and retry are defined by the standard. The standard can accommodate higher data rates in the future. It defines operating speeds from 25 to 400 Mbps, with upgrades planned to 3.2 Gbps.

The JHU/APL chip includes features beyond what the IEEE-1394 standard defines. The chip makes use of redundant buses for increased reliability. It includes an easy to use board interface and RAM for buffering incoming and outgoing packets.

Snapstrate Mounting of Actel Field Programmable Gate Arrays

Use of Field Programmable Gate Arrays (FPGAs) is essential for compacting flight electronics, but packaged FPGAs take up considerable board area. One possible solution is to mount FPGA dice directly on COB boards, but it is difficult to program and test FPGAs in die form. An alternate solution is to package FPGA die on snapstrate adapters. With this approach an FPGA die gets wirebonded onto the snapstrate. The snapstrate fans out the die I/O to pads that are in the same location as the leads on an FPGA in a quad flat pack. The snapstrate can be mounted in a carrier that fans out the snapstrate pads to PGA pins. This carrier makes the FPGA electrically identically to an FPGA in a PGA package. At this point the FPGA can be programmed and tested as if it were in a PGA. Once testing is complete, the snapstrate is removed from the carrier and the outer edges of the snapstrate are snapped off, leaving a ring of pads that can be wirebonded to the board. After snapping, the snapstrate is much smaller than an FPGA in a quad flat pack or PGA.

3

IR Transceiver

As board size is reduced, it becomes more difficult to probe or connect to the board. One solution is to use IR links for communicating with the board. Miniature IR transceivers are now available that include both an IR transmitter and receiver. To demonstrate the usefulness of IR links, the RTX2010 processor module includes an IR transceiver for test purposes. This transceiver is used to establish an asynchronous UART style link to a PC for transferring data. Commercially available transceivers are available that plug into a PC that can communicate with the IR transceiver on the module.

Packaging

COB Characteristics

The most important benefit of COB technology is that once a well controlled process is established, COB can be low cost compared to standard multi-chip module (MCM) technology. This cost competitiveness is regarded as a result of the generally greater availability and lower cost of known good die (KGD). Coupled with the elimination of the first level of packaging (chip package), compact, high density circuit boards can be realized with low cost printed wiring boards (PWB) that can now be made with ever-decreasing line width and via hole feature sizes. In recent years, significant improvements have been made in die coating materials which further enhances the appeal of COB.

Aside from the various major developments and trends in the space and defense industries that are favorable to the acceptance and widespread use of COB packaging technology, implementing COB can be appealing in other aspects. Since the interconnection interface is usually the weak link in a system, the overall circuit or system reliability may actually be improved because of the elimination of a level of interconnect/packaging at the chip. Because some devices are only available in commercial plastic packages, populating a multi-layer laminate substrate with both bare dice and plastic-packaged parts is inevitable. With COB, mixing packaging technologies is possible. Another attractive feature of COB is that re-workability is possible. It allows replacement of defective dice instead of replacing an entire board. This feature is especially important for space electronics due to schedule and cost constraints.

COB technology utilizes the interconnections of bare dice on a substrate without the need for the component's package. Eliminating the component package reduces the required substrate area and assembly weight. Information in Table 1 indicates that the area occupied by a bare die is much less than that required by the packaged part. The area saving can be as much as 90% in some cases. With conventional high density printed wiring board and standard wire bonding technology, COB technology can yield a factor of ten or more in weight and volume saving. Using bare die rather than packaged device can accommodate more components on a given board area, thus reducing the inductance created by the next level of interconnection between components. It also reduces the thermal resistance and the number of interfaces between the active die and the substrate (i.e., the package pins). This can potentially improve the speed of the circuit and the reliability of the design. In terms of thermal management, un-packaged devices offer a shorter thermal resistance path than their packaged counterparts thereby improving thermal sinking and heat removal from the parts.

Table 1. Area of Bare Chip in Standard Package

Package Type	Pin Count (Pitch in 10^{-3} in)	Outside Package Dimension (in)	Max. Cavity for Bare Chip (in)	Bare Chip Area in Package (%)
PGA	68 (100)	1.10 x 1.10	0.55 x 0.55	25
	84 (100)	1.10 x 1.10	0.47 x 0.47	18
	100 (100)	1.32 x 1.32	0.50 x 0.50	14
	132 (100)	1.40 x 1.40	0.45 x 0.45	10
	208 (100)	1.77 x 1.77	0.45 x 0.45	6
LCC	24 (50)	0.40 x 0.40	0.27 x 0.27	46
	32 (50)	0.55 x 0.55	0.39 x 0.39	46
	68 (50)	0.95 x 0.95	0.63 x 0.63	44
	84 (50)	1.15 x 1.15	0.70 x 0.70	37
	100 (50)	1.35 x 1.35	0.39 x 0.39	8
QFP	24 (50)	0.40 x 0.40	0.28 x 0.28	49
	32 (50)	0.40 x 0.40	0.26 x 0.26	44
	68 (50)	0.95 x 0.95	0.50 x 0.50	28
	84 (50)	1.15 x 1.15	0.47 x 0.47	17
	132 (50)	0.95 x 0.95	0.40 x 0.40	18
SOJ	28 (50)	0.72 x 0.43	0.60 x 0.35	60
	32 (50)	0.83 x 0.42	0.65 x 0.27	50
DIP	24 (100)	1.20 x 0.61	0.65 x 0.43	38
	32 (100)	1.60 x 0.31	0.56 x 0.22	25
	48 (100)	2.40 x 0.61	0.49 x 0.40	13
	64 (100)	3.20 x 0.91	0.55 x 0.43	8

Comparison with Other Packaging Approaches

In theory, there is no distinct difference between MCM and COB technologies. In practice, MCM is often related to a smaller substrate with fewer active dice as compared with COB design. MCM technology is being supported by many companies. Three major

4

substrate technologies for MCM are: MCM-D, MCM-C and MCM-L. MCM-D provides the highest density in substrate design since it uses thin film processes to deposit metals and dielectric layers on a variety of rigid bases. MCM-C provides moderate density in substrate design. It uses thick film technology to form conductive patterns on ceramic or glass ceramic materials. MCM-L uses laminate structures and employs PWB technology to form conductive patterns over reinforced dielectric laminates. Conventional PWB technology with the etching process can provide 0.005 in. feature sizes. To date, with the development of the additive process in the PWB technology, laminated substrates can have very fine line widths and spacing features as small as 0.004 in. These characteristics make MCM-L technology very popular and attractive due to its low-cost process. COB technology is similar to MCM-L technology. It supports the use of both conventional soldered components and bare dice on a laminate dielectric substrate. COB offers more weight and volume saving than MCM-L since it eliminates the intermediate substrate and pins of a MCM-L device. It supports rework and rapid prototyping without the need to complete intermediate MCM devices. These are the major characteristics and potential advantages of COB over MCM technology. Figure 3 provides the schematic comparison between the COB, MCM and single chip package technologies.
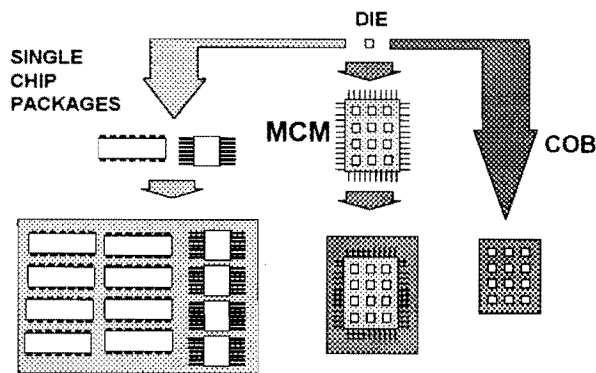

Figure 3. Comparison of Various Packaging Technologies

Packaging Design for the C&DH IYP

The C&DH IYP uses a standard module design with an overall dimension of 4 x 4 x 0.5 in and a typical weight of 5 ounces. This 3-D modular design provides flexibility to accommodate future modules. The frame for each module is made from aluminum alloy 6061-T6 with interlocking design features to provide lateral support for the complete assembly, and also to provide

alignment for the interconnections between modules. Interconnections between the modules are done by a custom designed solder-less fuzz button connector with a pin-to-pin spacing of 0.050 in. To achieve a high density packaging design, all active and passive components are mounted on both side of the boards. The board design consists of eight to twelve layers of interconnections with 0.005 x 0.005 in. line width and spacing. Buried and blind vias are used to interconnect conductors from different layers. The bond pads on the outer layers are electroless plated by a JHU/APL proprietary process. It forms layers of nickel and gold materials over bare copper pads to support the thermosonic wirebonding assembly. Thermosonic is a wirebonding technique that uses force and associated capillary and substrate heat along with ultrasonic energy to effect the bond. The material selection of the board is particularly important in this design, since it has to be compatible with both soldering and wirebonding processes. The most suitable material for this application is polyimide. The advantages of the polyimide material are its high glass transition temperature (above 300 °C) and its low thermal expansion (40 ppm/°C). During assembly, the board temperature can be as high as 150 °C for wirebonding. It can also reach 180 °C at the soldered joints. Due to these high temperature environments, having a material with high glass transition temperature will ensure that the plated vias in the substrate design will not see undesired high thermal stresses.

Die Coating Material

Another important issue in the COB design is the selection of the die coating material. Selection of coating material requires a thorough understanding of the material behaviors and is based on the following five major criteria:

1. The TCE should be close to that of the wire material (Gold wire has TCE=14.2 x 10^{-6} in/in/^{0}C),
2. High glass transition temperature (Tg),
3. Low cure shrinkage,
4. Void-free fill over wires and chips,
5. Low ionic contamination content (< 20 ppm Na$^+$, K$^+$, Cl$^-$).

JHU/APL has developed a process that uses both inorganic and organic coating materials to protect bare dice from handling and orbital environments. The selected coating combination has survived a life test

5

that includes temperature cycling, high humidity with biased voltage, shock and vibration conditions.

Modules in Development

Three modules are currently in development: an RTX2010 processor and interface module, a Solid State Recorder module, and a Mongoose V processor and interface module.

RTX2010 Processor and Interface Module

This module is suitable for use as a spacecraft processor, C&DH processor, instrument controller, or for other onboard processing needs. The use of a microprocessor that is immune from bit upsets plus the use of memory with error detection and correction (EDAC) makes it suitable for high reliability applications.

The RTX2010 is a radiation hardened 16-bit microprocessor manufactured by Harris that directly executes the FORTH language. It has been used extensively by JHU/APL for command and data handling processors and instrument controllers. A

block diagram of the module is shown in figure 4. The module has a throughput of 2-3 MIPs while dissipating 3 Watts. The module contains 16 Kbytes of boot PROM, 128 Kbytes of RAM and 128K bytes of EEPROM. Both the RAM and EEPROM are protected against bit upsets with the use EDAC circuits. The EEPROM can be reloaded in flight. After a reset, the processor boots from PROM, then downloads the application code from EEPROM to RAM. The module communicates with other modules over the IEEE-1394 serial bus. The module board top and bottom side layouts are shown in figure 5.

The module I/O includes MIL-STD-1553 and high speed serial interfaces, a Mode Control input and an IR link. The MIL-STD-1553 interface is implemented with a UTMC Enhanced Summit protocol chip. The Summit chip requires RAM for configuration information and message buffering. It shares a bank of the RTX2010 processor's RAM for this purpose. This has the advantage of providing EDAC for the Summit as well as the RTX2010. The Summit chip can either be configured by jumpers on the module as a Bus Controller or Remote Terminal, or the Mode Control signal that is inputted to the module can be used to
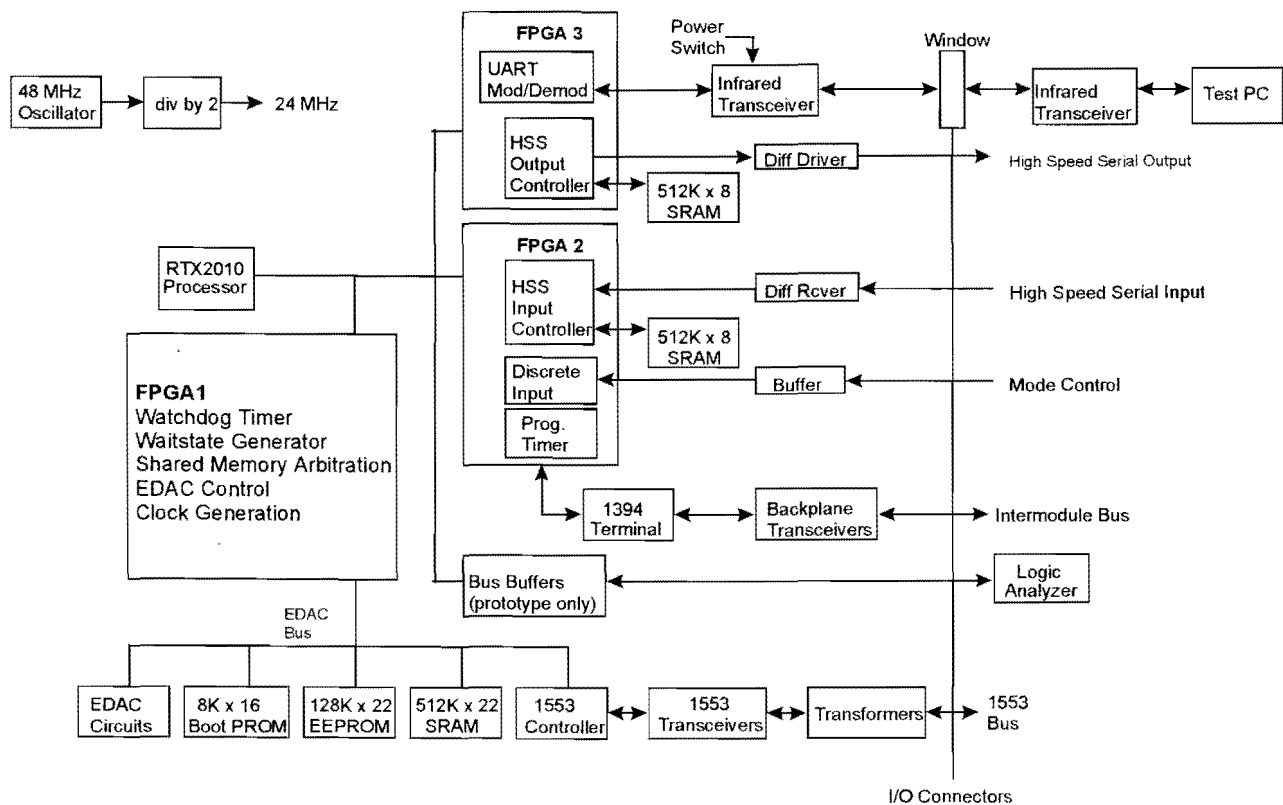

Figure 4. RTX2010 Module Block Diagram

6

configure the Summit as a Bus Controller or Remote Terminal. This feature is useful for spacecraft that use redundant stacks to avoid single point failures. One stack would be the 1553 Bus Controller and the other would be a Remote Terminal. The module Mode Control input allows this designation to be switched in flight in the event of a failure.

High speed serial interfaces include buffers for incoming and outgoing messages. The interfaces use Lock, Clock, and Data signals. Each signal is implemented as a differential pair.
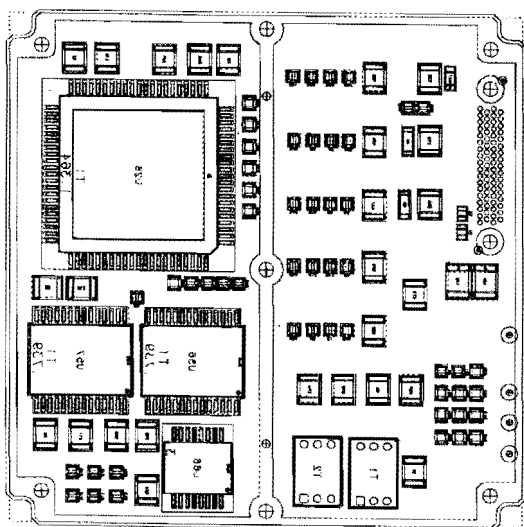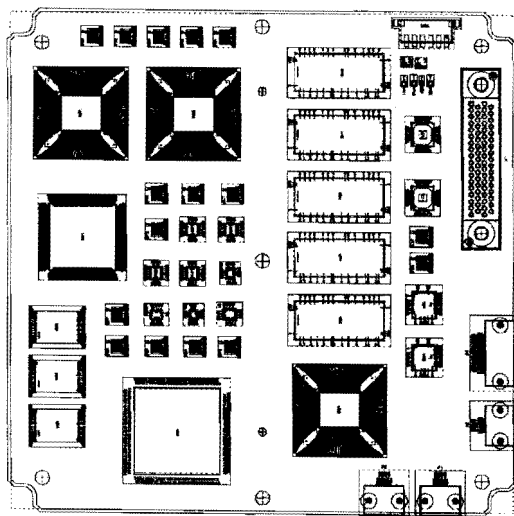

The IR link is implemented with a Novalog IR miniSIR transceiver and is used to communicate with a PC for test purposes. It complies with the Infrared Data Association (IrDA) Serial Infrared Data Link standard.

The RTX2010 has a demonstrated low cost software development environment. There are two paths: one using a JHU/APL developed FORTH kernel, plus a PC based C language development environment from Harris. The kernel uses a 9600 baud interface to a PC for interactive development. Final flight code size is minimized with the use of a JHU/APL developed PC based FORTH cross compiler. The engineering module RTX2010 processor includes an interface to a logic analyzer for tracing code. Low cost software development has been demonstrated with the kernel approach with single and multiple person development teams on the ACE and NEAR spacecraft.

Solid State Recorder Module

The Solid State Recorder (SSR) module is designed to be used as a bulk storage device for science, housekeeping, or any other onboard data. It uses stacked DRAMs to maximize capacity and Reed Solomon block coding to minimize the error rate. The SSR module can receive record data and send playback data to any other module on the IEEE-1394 intermodule bus. Commands to the SSR are also received over the bus. The SSR maintains independent read and write pointers so that it can receive data from one module while it is outputting data to another module. The SSR controllers have been designed to accommodate different numbers and types of DRAMs. Characteristics of the SSR are shown in Table 2. The layout of the top and bottom of the board in the SSR module is shown in figure 6.

Table 2. SSR Module Characteristics

Parameter	Value
Capacity	2.0 Gbits
Maximum Operating Power	5.7W
Standby Power	1.8W
Error rate in 60 degree orbit after 24 hours of no scrub	$<10^{-19}$
Error rate in 30 degree orbit after 24 hours of no scrub	$<10^{-60}$
Max I/O Rate	8 Mbps combined R-W

Figure 5. Layout of Top and Bottom Sides of the RTX2010 Processor Module Board

Error Control Coding

The Reed Solomon block code used is implemented with the EDAC-5 chip developed by the University of New Mexico Microelectronics Research Center. The Reed Solomon code used organizes data in blocks of 256 bytes. Each block contains 244 bytes of user data and 10 code bytes. The code can correct 5 and detect 10 byte errors per block. The code is robust enough so that very few scrub cycles are required for most missions and DRAMs. The SSR module performs a
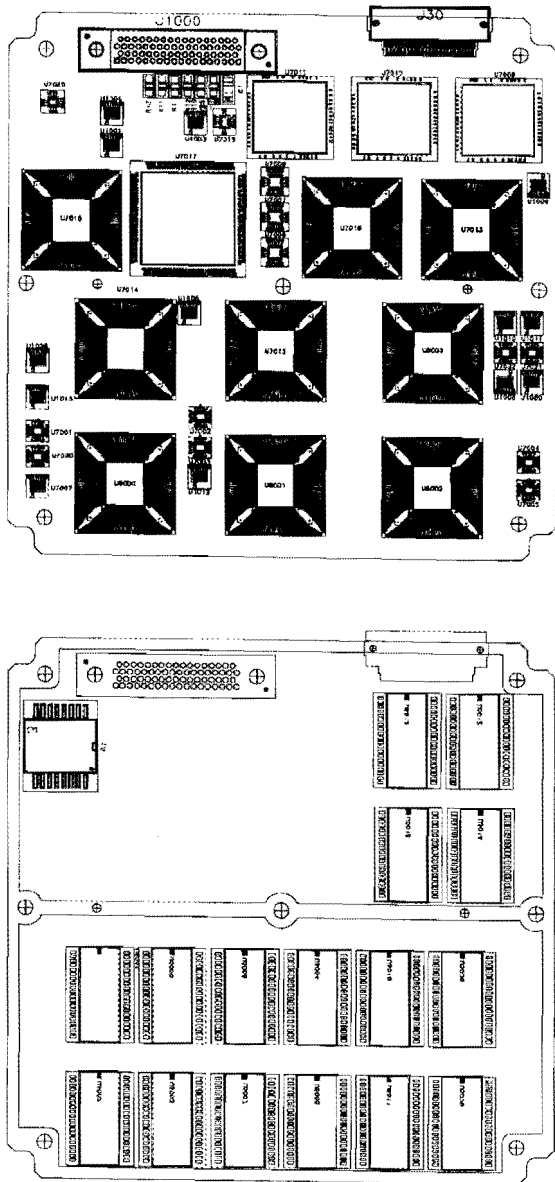
Figure 6. Layout of Top and Bottom Sides of the SSR Module Board

scrub when it receives a scrub command over the IEEE-1394 bus. A complete scrub takes under 10 seconds. Error rates after 24 hours without scrubbing are shown in Table 3 for DRAMs with a range of upset sensitivities. Most errors are corrected; most of those that are not corrected are detected.

Table 3. SSR Error Rates

DRAM Error/bit-sec	Detected Error Rate 24 Hours after Scrub	Undetected Error Rate 24 Hours after Scrub
10^{-13}	$< 10^{-31}$	$< 10^{-60}$
10^{-12}	$< 10^{-25}$	$< 10^{-49}$
10^{-11}	$< 10^{-19}$	$< 10^{-38}$
10^{-10}	$< 10^{-13}$	$< 10^{-27}$
10^{-9}	$< 10^{-7}$	$< 10^{16}$

Failure Detection and Mitigation

The SSR is designed so that it can still function if the DRAMs begin to degrade. DRAMs that have functionally failed can be skipped over during reading and writing. The degradation can be monitored as a DRAM starts to fail by making use of error statistics that are provided as data is read out from the SSR.

The SSR includes a mode in which individual bytes can be written and read instead of blocks. The Reed Solomon coding can be bypassed in this mode. By writing individual bytes of data, blocks can be stored in the SSR that have intentional errors. These blocks can be read back and the error detection and correction process can be verified.

Generic DRAM Controller Design

The DRAMs that are suitable for space flight change as manufacturers change masks and as testing is done on new lots of DRAMs. Accordingly, the controllers on the SSR have been designed to interface to and control a wide range of DRAM types with no change in the controller designs. The number and types of DRAM that can be used are shown in table 4. DRAMs are organized into banks that are controlled by a single refresh controller. A bank can consist of individually packaged parts or a 3D stack. Each bank is 8 bits wide, so it can consist of 4-bit parts arranged in pairs or 8-bit parts.

The current SSR module is designed with 16 TRWCI 32Mx4 DRAM stacks (each containing 8 4Mx4 DRAMs) with a total of 2.0 Gbits of user storage on a 14.75 in^2 board. The same controllers are being used
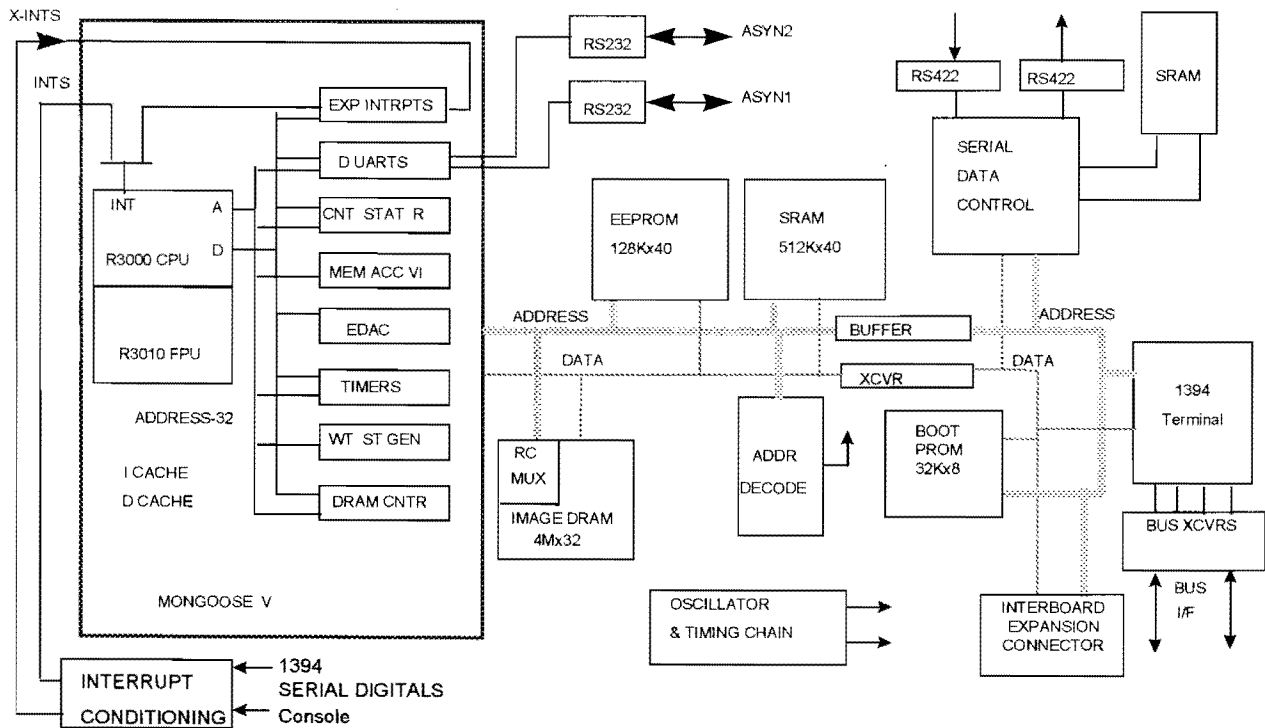
Figure 7. Mongoose V Module Block Diagram

on the TIMED spacecraft SSR board (which does not use COB) with unstacked 8Mx8 DRAMs with 2.5 Gbits of user storage on a 51 in² board. The existing controller designs can handle up to 19.5 Gbits of user storage with no changes to the controller design. A greater range of DRAM types can be handled with minor changes to the controllers.

Table 4. Controller - DRAM Compatibility

Parameter	Min	Max
DRAM Size	16 Mbits	256 Mbits
Stack or Bank Size (4-bit DRAMs)	16 DRAMs	20 DRAMs
Stack or Bank Size (8-bit DRAMs)	8 DRAMs	10 DRAMs
# Stacks or Banks	1	8
Refresh Type	4K	8K
Refresh Rate	4 ms	992 ms

Mongoose V Processor and Interface Module

The Mongoose V module is designed to be a high performance computing element. It communicates with other modules over the IEEE-1394 serial bus as well as with adjacent modules using a high speed local parallel bus.

The Mongoose V module includes a Mongoose V microprocessor, PROM, RAM, EEPROM, and DRAM memories, and high speed serial interfaces. The intermodule connector for this board can use the standard intermodule connector or an expanded connector that adds the Mongoose V address, data, and control signals for implementation of a high speed local parallel bus. The module block diagram is shown in figure 7.

The Mongoose-V is a radiation hardened MIPS R3000 architecture 32-bit microprocessor. It incorporates on-chip cache memory, on-chip peripheral functions and full hardware support for IEEE-754 floating point. The on-chip peripherals include error detection & correction circuitry, memory protection, timers, dual UARTs, expansion interrupts, waitstate generator, and a dynamic RAM controller. The Mongoose V was designed by Synova Incorporated and manufactured by Honeywell.

The Mongoose V module includes 2Mbytes of RAM and 0.5Mbytes of EEPROM, both with EDAC. 32Kbytes of Boot PROM and 16 Mbytes of DRAM are also included but do not have EDAC. The power dissipation and throughput of the module has not yet been determined.

9

Any MIPS R3000 software development tools are compatible with the module. At JHU/APL the Nucleus Plus Real Time Operating System from Accelerated Technology and the C Compiler, Cross View Debugger, Assembler, and Linker from Tasking have been used from Tasking. A development board is available from Synova.

Parts

One of the necessities of the C&DH IYP project was to procure as many of the required integrated circuits as possible in die form with a limited budget. It was found that most integrated circuits were available in die form, but the level of screening varied. A few parts could not be obtained in die form. In some cases this was due to cost (RTX2010 and Mongoose V), or packaged parts were preferable for ease of programming (PROM), or are available in high enough density in packages (stacked DRAM). An advantage of COB technology is that packaged parts can be accommodated along with dice. In addition to ICs, more basic semiconductors are also available in die form. Transistors and diodes as well as resistor networks were procured as dice. The semiconductors procured in die form are shown in Table 5. The semiconductors procured in packages are shown in Table 6.

Table 5. Semiconductors Procured in Die Form

Harris ACS630 EDAC
Harris CD40106 Schmidt Trigger
National 54ACQ240 Buffer
National 54ACQ245 Transceiver
National 54ACQ74 Dual Flip Flop
National 26LS31 Line Driver
National 26LS32 Line Receiver
UTMC UT69151E Enhanced Summit MIL-STD-1553 Chip
UTMC 63M147 MIL-STD-1553 Transceiver
Hitachi 628512 512Kx8 SRAM
Hitachi 58C1001F 128Kx8 EEPROM
Actel 1280XL FPGA
EDAC-5 Reed Solomon Chip
Chip Express 1394 Protocol Chip
2N2222 NPN Transistor
2N2907 PNP Transistor
1N5525 Zener Diode
1N5711 Diode

Table 6. Semiconductors Procured in Packages

Harris RTX2010 (QFP)
UTMC 8Kx8 PROM (FP)
Mongoose V (QFP)
Q-Tech Hybrid Oscillator (FP)
TRWCI Stacked DRAM

Part Procurement and Screening

Even given a limited budget, it was possible to procure most of the semiconductors required in die form. Some parts could be even be economically procured as rad hard KGD. For example, National rad hard 54ACQ parts procured as KGD cost in the range of $35 to $50 each (although a minimum lot buy of 100 was required). Some rad hard die were available in small lot sizes. UTMC supplied rad hard MIL-1553 protocol and transceiver die in minimum lot sizes of only 10.

As has become common even in flight electronics, some commercial parts were used, in particular the RAM and EEPROM. When commercial parts are purchased in die form they can be very inexpensive on a per part basis, but may only sold by the manufacturers in large lots. For example the Hitachi 512Kx8 SRAMs were only $23.60 each, but the manufacturer required a minimum buy of 300 parts. In this case the buy was split with another program at JHU/APL. Many parts that are only available from the manufacturer in large lots are also available in small quantities from chip distributors or hybrid manufacturers. This was the case for the EEPROM and 26LS31 and 26LS32.

Environment

Radiation Effects

Total Dose

Most of the parts in C&DH IYP modules have been selected to be rad hard to at least 15K rads, and many up to 100K. The major exception is the Actel 1280XL. Previous testing on 1280XLs have shown them to be hard to 2.5Krads. Harder versions of the 1280 can be procured and mounted on Snapstrates in place of the 1280XL version. The snapstrate size and pad layout is identical for the different 1280 versions, so they may be freely substituted without changes to the board.

If a particular mission requires electronics hardened to an increased radiation level, the most straightforward approach would be to increase the thickness of the end plates on the stack of modules. A medium term solution is to use a radiation resistant coating on the die. Rad Coat is under development for this purpose.

Single Event Latchup

All of the part types with the exception of the IR Transceiver and Chip Express IEEE-1394 chip have been tested and been found to be free of latchup. The 1394 chip is powered from a protected +5V line in which the maximum current is limited. An over current on that line is sensed and results in the power converter cycling off and back on. This will clear a latchup. In addition, it is planned to port the 1394 chip to a fully rad hard gate array. The existing board designs will be compatible with the fully rad hard version because the 1394 chips are first mounted on a substrate before being mounted on a board. The substrate has been designed to hold the largest possible rad hard gate array. The IR transceiver is used for test purposes only. It can be unpowered in flight either by removing a jumper on a connector or by having the software turn off a transistor that provides power to the transceiver.

Single Event Upset

Processor RAM and EEPROM single bit errors will be detected and corrected using ACS630 EDAC circuits. Double errors will be detected and cause the processor to be reset. The EEPROM is highly resistant to bit flips. The PROM is immune to bit upsets. Actel FPGAs use triple voted S and C modules. All triple voting modules are refreshed periodically to scrub out one error in the module before a second one occurs. Since S-modules are much more likely to upset than C-modules, triple voted S-modules are clocked or refreshed at very high rates, always greater than 1 MHz.

The SSR is protected from bit upsets in the DRAMs by the Reed Solomon code used. The EDAC-5 chip used to implement the code is highly resistant to upsets.

Thermal

The C&DH IYP modules will be thermal-vacuum tested over a range of -25C to +60C. This will accommodate spacecraft baseplate temperatures over this range minus the margin required.

Dynamic Loads

The C&DH IYP modules are designed to accommodate the mechanical environment of all known launch vehicles. The dynamic load levels that the modules are tested to are shown in table 7.

Table 7. C&DH IYP Dynamic Load Test Levels

Pre and Post Sine Survey:	5-2000 (Hz)	Acceleration 0.5g
Sine Burst	Thrust Axis = 40 g	
	Lateral Axis = 19g	
Random Vibration (in all axis)	Frequency (Hz)	PSD (g^2/Hz)
	20	0.026
	20-50	+6db/oct
	50-800	0.16
	800-2000	-6db/oct
	2000	0.026
Shock	Frequency (Hz)	Amplitude (g)
	20	20
	500	500
	10000	500

Electromagnetic Interference and Control

The primary EMI/EMC concerns have been to limit radiated emissions from the DC-DC converter module and to limit conducted susceptibility and emissions on the primary power input lines to the DC-DC converter module. EMI generation in the other modules is limited by using controlled risetime logic families. Conducted susceptibility on interfaces is avoided by using robust interfaces: transformer coupled differential signals (MIL-STD-1553), differential signals (high speed serial interfaces), and single ended signals with filtering (mode control input).

The DC-DC Converter module will use hybrid DC-DC converters as the core of the module. These modules typically have high radiated emission levels. As in previous APL design, the DC-DC converter module will include a EMI-tight chamber to hold the hybrid converters. The chamber uses a filter pin connector and EMI filters on the primary power input side to meet conducted susceptibility/emissions requirements on primary power lines. Bulkhead feedthrough filters are used to output secondary voltages to keep secondary voltages clean.

Project Status

As of August '97, breadboards for the RTX2010 and SSR modules have been fabricated and are in test. The

11

Mongoose V module is currently in the design stage. The RTX2010 and SSR COB modules are in layout. Bare board fabrication is to take place in August '97, and assembly of the modules is to take place in September '97. The flight chassis have been fabricated and used with a test board to verify connector performance during vibration and thermal vacuum (see figure 2). A PC based tester for the RTX2010 and SSR modules has been designed, fabricated, programmed, and checked out. All flight parts are on order or inhouse.

Future

Spacecraft proposed to NASA by JHU/APL have already been based on the use of C&DH IYP modules. JHU/APL can supply these modules to other government sponsored spacecraft programs. It is planned to flight qualify an RTX2010 Processor module and SSR module in the fall of 1997, and the Mongoose V module in the first quarter of 1998.

Acknowledgments

References

1. "Evaluation of Die Coating Materials for Chip-On-Board Technology Insertion in Spaceborne Applications" for the International Conference on Multichip Chip Module, April 2-4 1997, pp. 142-147. Binh Q. Le, Elbert Nhan, Richard Maurer, Ark L. Lew, Juan Lander, Seppo J. Lehtonen, M.Ann Garrison.

2. "Reliability Study of Chip-On-Board Technology for Space Applications with A 3-D Stacked DRAM as Test Vehicle", ASME International, Intersociety Electronic & Photonic Packaging Conference, June 15-19, 1997, pp. 1679-1684. Elbert Nhan, Binh Q. Le, Richard Maurer, Ark L. Lew, Juan Lander, Paul D. Schwartz, M.Ann Garrison.

12

Author Biographies

RICHARD F. CONDE is a member of APL's Principal Professional Staff and supervisor of the Flight Processors/Computers section of the Flight Systems Group in the Space Department. He obtained a B.S. in electrical engineering from Cornell University in 1981, an M.S. in electrical engineering from The Johns Hopkins University in 1985, and is currently pursuing an M.S. in computer science from The Johns Hopkins University. Since joining APL in 1981 he has worked on a variety of flight systems for the Advanced Composition Explorer (ACE), Mid-course Space Experiment (MSX), DELTA 181, DELTA 180, Polar BEAR, and GEOSAT spacecraft. His e-mail address is Richard.Conde@jhuapl.edu.

BINH Q. LE received his B.A. in mathematics from Université de Paris Sud, and his B.S. and M.S. in mechanical engineering from the Catholic University of America. Mr. Le joined the JHU/APL Space Department in 1991 and is a Principal Professional Staff Packaging Engineer in the Electronic Systems Group. He is a member of IMAPS and Tau Beta Pi. At JHU/APL, Mr. Le has been the lead electronic packaging engineer for all current JHU/APL satellite programs: MSX, ACE and NEAR. He has also contributed as a technical advisor for many space flight subsystems, including the space qualified ultra light weight transmitters for use in the SDI's Brilliant Pebbles program. Mr. Le is currently the Principal Investigator for an IR&D program to implement the COB technology to miniaturize spacecraft electronics, and the lead mechanical design engineer for the miniaturized Glacier Imager. Prior to joining APL, he spent 13 years in structural/thermal analysis, electronic packaging design and mechanical design for nuclear and space industries. His e-mail address is Binh.Le@jhuapl.edu.

JOSEPH F. BOGDANSKI is an Senior Staff electrical engineer in the Electronics Systems group at The Applied Physics Laboratory. He obtained both a BS and MS degrees from The Virginia Polytechnic Institute and State University in 1976 and 1979 respectively. He has extensive design experience in space applications connected with interface and embedded controllers in radiation harsh environments. At present his interests include single event upset proofing FPGAs. His e-mail address is Joseph.Bogdanski@jhuapl.edu.

ARK L. LEW received a B.S. degree in electrical engineering from Case Institute of Technology in 1963, an M.S. degree in electrical engineering from The Johns Hopkins University in 1968, and an M.S. degree in technical management from The Johns Hopkins University in 1985. Mr. Lew has an extensive background in design, development and management of space flight subsystems. He has been the lead engineer for command, telemetry and data handling subsystems for numerous APL satellite programs for DOD and NASA. Since his appointment as group supervisor, Mr. Lew has managed the design and development of space electronics which includes onboard processors/computers, radar signal processing, image processing, and onboard storage. Mr. Lew is a member of the APL Principal Professional Staff. His e-mail address is Ark.Lew@jhuapl.edu

JAMES A. PERSCHY received a BSEE degree from The George Washington University in1958 and an MS in Physics from the University of Maryland in 1965. In 1958 he joined APL, where he designed the data handling system and memories for the Navy navigation satellites. Recently, he led the TOPEX ocean-altimeter signal processor development. He is currently leading the TIMED spacecraft command and data handling system development. He has extensive experience in the design and development of space flight hardware and software. Mr. Perschy is a member of the APL Principal Professional Staff. His e-mail address is James.Perschy@jhuapl.edu.

ANN GARRISON DARRIN is currently Chief of the Assurance Technologies Division; overseeing efforts in Parts, Electronic Packaging and Processes, and Material Engineering. She will shortly be the Chief of the Technologies, Electronic Systems Center at Goddard. Ms. Darrin has extensive experience in microelectronics in both private industry and the public sector. Ms. Darrin earned her Bachelor of Arts from Pennsylvania State University and her Master of Science in Technology Management from the University of Maryland University College. Her e-mail address is ann.darrin@gsfc.nasa.gov.