

## HETE SATELLITE PROCESSING SYSTEM

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### Abstract

The HETE (High Energy Transient Experiment) satellite is a joint project between MIT's Center for Space Research and AeroAstro. The primary goal of the High Energy Transient Experiment is to determine the origin and nature of cosmic gamma-ray bursts. The objectives include the simultaneous broad band observation of energetic, transient astrophysical sources in the UV, x-ray and gamma-ray energy ranges, and the precise location and identification of cosmic gamma-ray burst sources. A continuous slow data rate down link of major events is to be broadcast to 20 receive-only ground stations, allowing other astrophysical assets to observe events detected by HETE.

AeroAstro is building the HETE spacecraft bus for MIT and is responsible for the development, manufacture, test, and integration of the spacecraft bus, and spacecraft bus hardware / payload hardware integration. AeroAstro will also provide the complete ground segment consisting of 2 full duplex ground stations and approximately 20 receive-only ground stations.

This paper presents a summary of the HETE satellite data processing system designed and manufactured by AeroAstro. The data handling system, which is built around a combination of the INMOS Transputer and a Motorola DSP56001 processor which is also used to manage most of the other spacecraft functions such as attitude control and power management. Payload processors, memory system and spacecraft processor are integrated in the spacecraft central electronics box, and share a common back plane.

### System Architecture

The lead science team, MIT's Center for Space Research, specified the DSP56001 as the experiment controller for the program. The instrument's interface was to use the DSP56001's two internal serial ports as the primary control and data link. Power to the instruments was to be provided separately. The DSP56001 is an extremely power efficient processor, with adequate radiation tolerance. For the experiment teams, the DSP56001 is available on cards for Sun, PC, and Macintosh computers, and it is the DSP processor included in the NeXT computer.

The memory requirements for the program included two types of large memory arrays, approximately 80 megabytes for the storage of programs, data libraries, and data to be processed and downlinked, and approximately 32 megabytes of DSP memory to store 8 frames of UV camera images. These types of memory are completely different- the former requires error correction methods to be used, since it is finished data product, and the latter requires fast access and a complex paging system to accommodate the small address space of the DSP56001 (16 bits of address = 64k words of address space).

Because of the limitations in the DSP's address space, we selected the INMOS Transputer as the general purpose processor, allowing the DSP processors to concentrate on the data reduction and correlation activities, as well as to command and control the payloads. The selection of the transputer had numerous benefits in addition to its 4 gigabyte memory space: excellent interprocessor communications capabilities are part of the processor's architecture; low level task switching and process management is also supported in hardware; a microsecond counter and a 64

microsecond counter available in the processor; a very small SEU cross section; and good power performance. The transputer provides several necessary peripherals that are generally absent from other 32 bit processors.

Additionally, the science mission requires extremely accurate time references to each of the processors in the system, on the order of 1  $\mu$ second. A global real time counter was developed that allowed all of the processors in the system to maintain a synchronized time base across the satellite, and to be able to time stamp data products and messages without external synchronization. Each processor has its own independent copy of this counter, which is synchronously re-synchronized periodically.

The architecture that emerges is one that is becoming more common in commercial industry: A general purpose processor that supervises higher performance embedded communications and control processors. This hierarchy makes sense for several reasons. First, the effort of software integration is subdivided into several parts that break along very natural lines, and you are not asking a single processor to be an all-in-one solution to all of the requirements in the system. Also, each of the processors in this system bring with them most of the communications hardware they need to do their jobs! This limits the amount of hardware development required.

### Technology Selection

HETE needs a very power efficient digital system to perform its mission. There is a 12 watt power budget for the processors and there is a large array of processing tasks being performed. CMOS devices are the only devices able to deliver this performance on this budget.

The radiation performance of the integrated circuits used in HETE is of prime importance. For the digital system, adequate knowledge of the tolerance of the parts was required for their use. Three facets to radiation performance were assessed: Total Dose,

Single Event Upsets (SEU), and Single Event Latchups (SEL). The HETE mission has an 18 month duration, and it is not the typical gold plated satellite program, so we took a different approach to the radiation issue.

Our goals for radiation tolerance are: Total Dose: 10kRad (Si); a small SEU cross section and an SEU LET of 3 to 4; and a SEL LET of greater than 40. These goals are not particularly difficult to achieve using available commercial technology. In many cases, the same IC die are used in commercial, MIL, and Class S products. The only differences between the three lie in handling and packaging after wafer fab and dicing of the semiconductor products. We were able to review the available test data for the military products, and assess the performance of their commercial brethren.

In our review of the available literature we found that many commercial CMOS processes fall into the range of our radiation tolerance goals. The decrease in feature sizes have resulted in some more favorable trends in radiation performance. One such trend is the need for thinner oxide layers in a device. Small design features requires thin oxides, which in turn requires oxides of an extremely high purity. These pure oxides yield good radiation tolerance, quite by accident. Latchup is a problem terrestrially, and so IC manufacturers design their products to be inherently resistant or immune to latchup by using specific manufacturing processes and design rules throughout the circuit.

In specific circumstances, radiation hardened technology parts are used, but the cost, power, mass, and schedule goals of the program could not be met if only MIL or Class S parts were used. For some parts, their cost per part increases between 5 and 10 times!

### Product Selection

#### •INMOS Transputer

The Transputer was selected for its good interprocessor communications support, excellent power efficiency, small SEU cross

section, and adequate Total Dose and SEU/SEL LET performance.

•Motorola DSP56001

The Motorola DSP56001 has excellent power efficiency and a very useful Host Interface with multiple boot modes that allows remote testing of a processor and its software without physical access. Its internal peripherals include 2 serial peripherals, synchronous and asynchronous, with most aspects of serial port's configuration programmable, including a multi-drop network feature.

•Actel Field Programmable Gate Arrays  
The Actel FPGAs represented an enabling technology for the program, by allowing us to design all kinds of digital glue logic, sensor controllers, and power converters in a naturally radiation tolerant technology. They were used to develop the spacecraft bus medium data rate control network, Auxiliary Bus, which is used to supervise and control all bus sensors, controllers, and actuators.

5 different Actel gate array designs reside on the processor board, implementing memory bus control, error correction, wait state generation, programmable event control, and real-time counter interfaces across the 3 processor sections on a processor board.

- 1 Mbit Static RAMs for the Transputers
- 128kbit SRAMs for the DSP processors.
- Commercial Surface Mount Technology is used extensively. This realizes significant savings in cost, volume, and mass. The ripple in savings to the rest of the satellite are significant.

An ALEXIS processor board, representing late 1980's technology and MIL packaging, with a single 7MHz 8086 processor and 0.5Mbyte of memory, weighs approximately 650 grams. The HETE processor, representing current technology and packaging, with 3 processors operating at 20MHz, and over 5Mbytes of memory, weighs 370 grams.

Many of the parts increase in cost 5 to 10 times when bought in MIL or Class S packages. In one example, Actel Act2 FPGA products increase in cost from \$174 in a

plastic quad flat pack, to over \$1000 in a ceramic quad flat pack!

Commercial packaging is preferred over MIL packaging for the simple reason that the quality of reputable commercial electronic component manufacturers is at least equivalent MIL quality, because of commercial competitive pressures. We are avoiding ceramic packages because ceramic surface mount packaging (LCCs, CQFPs) have severe temperature coefficient of expansion difference problems, especially since there is no means for mechanical compliance. Also, a review of available manufacturer's test data for quality analysis indicates several failure modes of ceramic packages that are not present in commercial plastic packaging

#### Basic Design Objectives for the Digital System

As part of the processor architecture process, we carefully considered just what test features we would want when we were faced with integrating the satellite and its software. By imagining the difficult problems that can arise from integrating so complex a processing structure, we were motivated to include several independent methods to guarantee the observability and testability of the system. We wanted all of the subsystems to be individually observable and testable without physically disturbing either the system under test or any other system on the satellite. We also wanted to avoid "golden" systems- one of a kind items that are hard or expensive to produce. Most people are less willing to rigorously test and risk damaging an expensive deliverable, and the probability of a serious problem being discovered later in the program is higher.

In fact, for the HETE program, we have built 27 development processors, including spares, which are identical to the flight processors, allowing a wide distribution of the processing system to the users, and allowing several units to be subjected to tests that would probably not be performed with less available hardware. By putting the processor out there in the user community,

the operating regimes of the processor are explored more fully earlier in the program. That means that major problems are found earlier in the program, at a lower cost to the program.

### Observability and Test Methods

#### Transputer Testing

One of the Transputer's Links is a dedicated debugging interface. From it, a user is able to command the transputer to boot either from the on-board ROM, or from the Transputer Link. This interface allows us to perform interactive debugging, post-mortem analysis, and process observation; all by plugging in one cable into HETE Electronics Box.

#### DSP Testing via the Host Interface

The Host Interface can be switched from the nominally mastering transputer, to a DSP development system external to the satellite, or to another transputer on-board the satellite. This allows the development and test of DSP instrument code in situ, but without the dynamics of the rest of the system interfering. In effect the equivalent of a bench test may be performed on each of the eight DSP processors in the system without physically disturbing the system being tested. By testing the subsystems separately without any disruption of the satellite, possible errors can be ruled out much more quickly, and the system experiences less handling and assembly work over the course of the program.

#### Satellite Bus Peripheral Testing

One of the major innovations for the HETE program is the master/slave serial control network used to control the satellite bus, which we call the Auxiliary Bus, or Aux. What is unique to this system is that all of the slaves are implemented in Field Programmable Gate Arrays, which are very reliable, and relatively cheap to develop. Slaves on this network include the Power System, Momentum Wheel, Torque Coils, Temperature Sensors, Sun Sensors, and Solar

Panel Actuators. This allows the satellite bus to be controlled in the same manner as the instruments, namely through one of the satellite processor's DSP serial ports.

We also include system redundancy in this portion of the system, by allowing either of the two spacecraft processor DSPs to master the control network. As a further test feature, the digital system includes a test port which will permit an external Aux Master to take control of the network, and test individual slaves as needed.

The protocol for this control bus is not as complex as the many RS-422 based control systems, such as ModBus, or MIL-1553. We were able to implement the network slaves with single Actel Field Programmable Gate Arrays, an extremely reliable technology. We have a completely controllable and observable system with this control network.

#### Some Other Objectives

Traditional ICD documentation of hardware and software generally results in lots of paperwork and meetings. We avoided this very expensive portion of development by encapsulating development across the traditional divisions of hardware and software, by providing a development system that provides the hardware and software required for their development. Differences between the paper specification and reality are avoided, and most errors are discovered very early when they are easier and cheaper to correct using this approach.

The developers using the system will be using an operating kernel that provides many system level functions. A commercially available kernel was purchased since it represented a far lower risk than rolling our own, and it was far cheaper to buy it than to develop it. This kernel was enhanced to reflect the architecture of the HETE processor.

We wanted to do development the way the rest of the computer industry does development: by developing and

engineering only the highest value added and specific system requirements. We are giving the developers in the program the system on which they are expected work, and we bring in commercial development tools wherever and whenever possible.

#### HETE Satellite Processing System Topology

By definition, we have a multiprocessing, multiprocessor environment. The connectivity of the system, as depicted in the figure "HETE Satellite Processing System Topology" reflects the requirements of the program- between the science processes for correlation activities, and between the science processes and the s/c bus process for data storage and downlinking. Each processor board is represented as a Transputer (larger ball) connected to two DSP processors (smaller balls).

Each Transputer in the system can be connected directly to a development system, each Transputer to DSP connection can be replaced by an external DSP development system, and the SC DSPs can be replaced as Aux Bus masters, selectively or together, by plugging in just three cables.

#### HETE Processing System Architecture

The HETE processor board is divided into 3 processor sections, any one of which can be independently powered up or down. Each processor section is power controlled, individually latchup protected and voltage and current sensed by an on board Aux slave. This Aux slave also controls the Transputer's boot from ROM, internal memory enable, reset, and analyze lines, and reads the Transputer's error line, allowing the state of the Transputer to be read and controlled by the Aux slave. In the event of a failed boot ROM on a transputer, it may be booted by another transputer in the system.

The processor boards are connected by a backplane, which carries digital and analog power, Aux Bus control signals, Transputer Links, Real Time Counter signals, the Host Interface Bus, and system wide interrupts

and synchronization pulses to each processor board. The Real Time Counter provides a 1  $\mu$ second time base to all processors in the system, allowing system wide time keeping. The Host Interface Bus is an extension of the DSP processor's Host Interface. It is used as a test and debugging interface, and as a redundant means for the control of orphaned DSP processors in the event of a transputer failure. There are several synchronization sources on the HETE satellite, including GPS derived timing pulses, RF system ranging pulses, and Ovenized clock interrupt pulses.

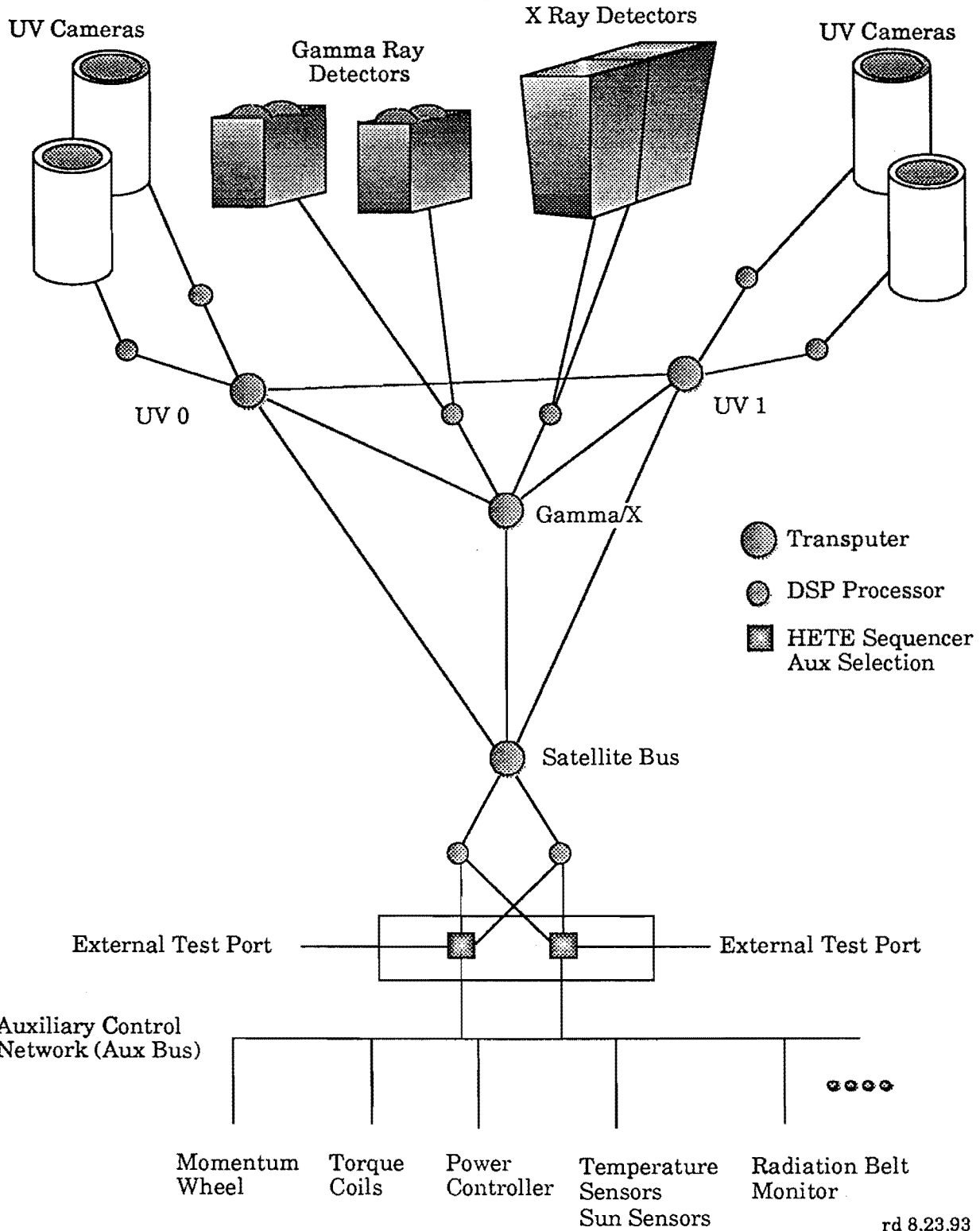
Each Transputer communicates with each of the other transputers using communications Links at 20Mbits per second. The Transputer's 32 bit data word memory system is 39 / 32 Hamming Code error corrected in hardware, with a count of SEUs detected available to the processor. 100% of all SEUs are detected and corrected, and 100% of all double bit errors are detected. In the event of the detection multiple bit upset, an address fragment is latched in a readable register, an interrupt is asserted to the Transputer and the error line of that transputer is set. The Transputer has 4Mbytes of on board SRAM, and 0.5Mbytes of on board EEROM. 1/4 of the EEROM is normally write protected.

The HETE processing system has two types of memory boards that attach to the processor board via a board to board connection system. The Transputer's memory can be extended with up to eight 16 Mbyte error corrected memory boards. One of the DSP processors can receive a 12 Mbyte image frame buffer.

Each Transputer will nominally master 2 DSP processors- the two which are on the same board as the Transputer. In the event of a 'hard' transputer failure, any other transputer in the system will be able to, asynchronously, adopt the orphaned DSP processors, with no changes in the interface between them, just a degradation in speed of transfers.

The primary Transputer to DSP interface uses the DSP Host Interfaces, which are

# HETE Satellite Processing System Topology



memory mapped into the Transputer's memory space. The Host Interface is a bootable interface that includes double buffered registers and flags for proper processor synchronization. Normal data exchanges between the processors make use of the DSP Host Interface's DMA interface and the Host Interface Controller (HIC) FPGA.

The Transputer has a 32 bit word width, while the DSP processor has a 24 bit word width. The scientists believed that they would most often package their data products in the DSP processors with 16 bit words, and would want to store their data the most efficient way possible on the transputer, as two 16 bit elements packed in a single 32 bit word. The HIC matches the DSP Host Interface DMA interface to correctly transfer and align data across the different word widths in use on either processor. This gate array implements a double buffered pseudo DMA interface for both transputer to DSP, and DSP to transputer operations, for up to 4 different DSP processor word width configurations. It also provides the necessary controls for polled operations between the Transputer and the DSP Host Interfaces, again for up to 4 DSP processors.

Each DSP's Host Interface is made available externally over the Host Interface Bus for development with the DSP processor alone, by a FPGA that switches the combined host interfaces of a processor board onto the Host Interface Bus on the backplane. In the event of a transputer failure on one processor board, a transputer from a different processor board can adopt the DSP processors on the board with the failed Transputer. This gives significant fault tolerance without any loss in functionality, just a loss in performance. Thus the intrusive debugging capability, allowing a DSP to be tested while decoupled from the rest of the system, is also a reliability enhancer.

### Auxiliary Bus

We considered several approaches to connecting HETE peripherals, such as attitude control sensors and actuators, to the processor system. One approach, used with success on the ALEXIS SC bus was to include digital and analog IO boards on the backplane of the computer system. This approach is most efficient from a power and volume point of view but can lead to some wiring harness congestion and can limit the expansion possibilities of the system. If a new peripheral is needed late in the program the incremental cost of adding it can be high.

Another common approach to connecting peripherals to the main SC computer is to connect systems with a standard serial data bus, for example RS-422 or MIL-1553. The disadvantage to this approach is the cost, power and complexity of the interfaces and the software to manage the interface. A major advantage to this approach is that subsystem can be developed to work with the standard interface hence reducing problems at integration.

The approach finally selected for the HETE electronics system represents something of a compromise between the two alternatives. We have given this interface system the name of "HETE Auxiliary Bus" or Aux. The primary objectives used in design of this system were to minimize the power required, minimize the complexity of slave devices, be compatible with the selected bus controller (DSP56001), and utilize the minimum number of conductors for operation.

Aux is a synchronous, master-slave, half-duplex, serial data bus. By nature it is redundant and robust. Data transfer rates on the order of 200 kbps are possible and the interface hardware requirements are minimal.

To date we have implemented: pulse width modulators, AD converter interfaces, event counters, async communications interfaces, power control and monitoring circuits. The

basic Aux interface circuit has been made a standard circuit in our Actel library and new designs are easy to implement for different applications. The synchronous protocol requires no local clock, thus a "one-chip" solution for many problems is possible.

It is quite simple to interface any desktop computer to the Aux bus and sub-system designers can operate their designs directly from their workstations with good assurance that the code will work in the flight system without change.

### System Performance

The HETE Satellite Processing system has 88 sustained and 168 burst processor MIPS, 80 Mbytes of error corrected memory, 2.3 Mbytes of zero wait state DSP memory, and 24 Mbytes of DSP extended memory. The DSPs and the Transputers can exchange data at a 4Mbyte/8Mbyte per second sustained/burst rate, and the Transputers communicate with each other over 20Mbit per second data links. Power consumption, dependent on processor activity, is around 12 watts for a fairly active system.