PRELIMINARY DESIGN OF THE NAVAL POSTGRADUATE SCHOOL PETITE AMATEUR NAVY SATELLITE (PANSAT) ELECTRIC POWER AND COMMUNICATIONS SUBSYSTEMS*

By

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The Naval Postgraduate School's (NPS) Space Systems Academic Group (SSAG) is continuing the design and development of the Petite Amateur Navy Satellite (PANSAT), a small communications satellite. The objectives of PANSAT are to provide: (i.) an educational tool for the officer students at NPS, (ii.) digital communications using spread spectrum in the amateur band, and (iii.) a low-cost, space-based platform for small experiments.

PANSAT is designed for an altitude of 480 km and an inclination greater than 28.5°. The satellite weight is 150 lbs and has no attitude control. The expected life of the satellite is 2 years. This paper discusses the preliminary design of the electrical power subsystem (EPS) and the communications subsystem (COMM). The EPS is a photovoltaic silicon cell system consisting of solar array, batteries, battery charge regulator (BCR) and DC to DC converters. The COMM payload uses direct sequence spread spectrum modulated BPSK with a 1 MHz bandwidth. The data rate is 1200 bps with a bit error rate of 10^{-5} with a 5 Watt output.

INTRODUCTION

The Petite Amateur Navy Satellite (PANSAT) is a continuing project of the Naval Postgraduate School's (NPS) Space Systems Academic Group (SSAG) [Ref. 1]. A new aspect of the project is the use of spread spectrum. The PANSAT spread-spectrum system will be a baseline design from which experimental results will be used to determine the operational feasibility of the system on a small satellite platform. The satellite is 150 lbs and is designed as a Get Away Special (GAS) ejectable payload. Figure 1 shows the PANSAT configuration. A GAS payload was chosen as a design constraint having conservative design limits. PANSAT can also be launched on an expendable launch vehicle as a secondary payload. The small size of the satellite imposes a design constraint for electric power generation through solar cells. Additional considerations arise from the unknown tumbling of the satellite which will affect the performance of the electrical power subsystem (EPS) and the communications subsystem (COMM).

The PANSAT EPS preliminary design uses a modified unregulated bus topology. Two lead-acid batteries with five 2.1 volt (5 Ampere-hour) cells each provide sustained power and redundancy during eclipse and when non-eclipse demands exceed solar array power supply. The solar array consists of seventeen 256 cm^2 panels of either thirty-two 2 x 4 cm silicon cells or sixty-four 2 x 2 cm silicon cells. The EPS also includes a pulse-modulated battery charge regulator (BCR). A working breadboard BCR was developed and performed as predicted. Power conditioning will be done with off-the-shelf DC-DC converters.

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* This is a summary of thesis research performed by Mike Noble (EPS Design), and Steve Paluszek (COMM) as part of their respective M.S.E.E. degree requirements.

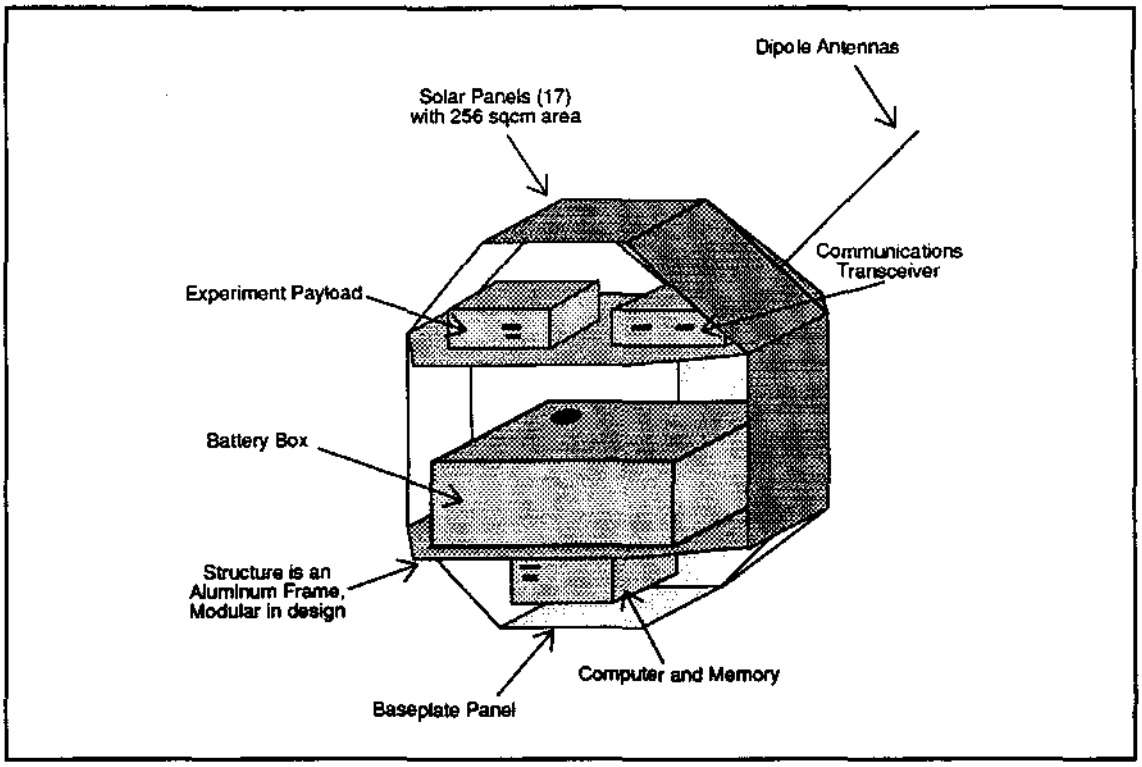

Figure 1. PANSAT Configuration

The PANSAT COMM preliminary design encompasses the link analysis, ground station requirements and operations, spread-spectrum system design, and simulation of the acquisition system. The link analysis was performed for a shuttle low-earth orbit of 28.5° inclination and 480 km altitude. Simulation of the acquisition system was done using the BOSS™ software application [Ref. 2.] on a Sun-4 workstation at the TRW Communication Laboratory, Redondo Beach, California.

EPS SUBSYSTEM DESIGN

Major factors of the EPS design are reliability, simplicity, and cost. The design should avoid any possible single point failures. Efficiency and weight are also considerations. A number of assumptions were made in the preliminary design since the development of PANSAT's subsystems is occurring in parallel. A shuttle orbit with altitude of 480 km and 28.5° inclination is considered. This is the worst case for the EPS since peak load requirements cannot be fulfilled by the solar array output. The orbital period is 94.2 min with an eclipse period of 35.8 min. It is assumed the satellite will be tumbling at a small rate (0.1 rad/sec for analysis) favoring no particular axis. PANSAT's power budget is shown in Table 1. A 10% margin is included to ensure that the EPS is capable of continuously providing power to the subsystems and payload. Heaters were not addressed since PANSAT's thermal control will be by passive means. Recent small, low-earth orbiting satellites, GLOMR and NUSAT, did not experience any malfunctions due to low temperatures. GLOMR was equipped with four 5-watt heaters which were never used [Ref. 3]. The EPS functional block diagram is shown in Fig. 2.

TABLE 1. PANSAT POWER BUDGET

Satellite Component	Nominal Power (W)	Duty Cycle (%/Orbit)	Average Power (W)	Average Watt-Hour
Microprocessor	2.6	100.0	2.6	4.1
Transmitter	15.7	25.5	4.0	6.2
Receiver	2.0	100.0	2.0	3.1
BCR	1.0	62.0	0.6	0.9
PWR Conditioning	0.5	100.0	0.5	0.8
Experiment Payload	0.5	62.0	0.3	0.5
Power/Orbit	-	-	10.0	15.7
10% Margin	-	-	1.0	1.6
Total Power	-	-	11.0	17.3

TABLE 2. ECLIPSE POWER REQUIREMENTS

SATELLITE COMPONENT	POWER (W) PER ECLIPSE	WATT-HOUR PER ECLIPSE
Microprocessor	2.6	1.6
Receiver	2.0	1.2
PWR Conditioning	0.5	0.3
TOTAL POWER	5.1	3.1

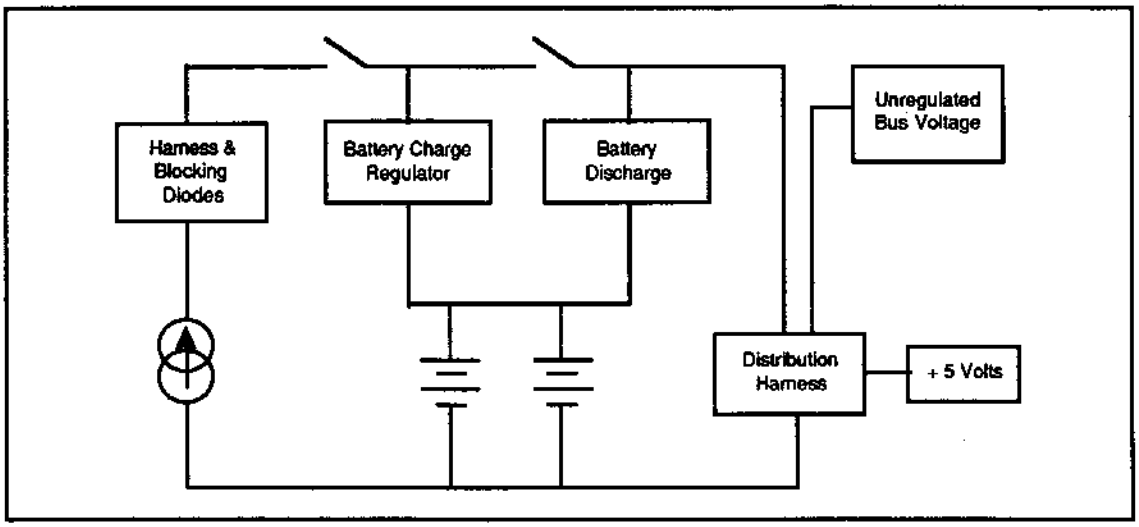

Figure 2. EPS Functional Block Diagram

Modes of Operation

Non-eclipse and eclipse are the two modes of operation for PANSAT. The transmitter and receiver will rely on the unregulated solar array voltage, less diode voltage drops, for power during non-eclipse. The other subsystems will require conditioning through dc-dc converters. Should the demand exceed the supply of the array, the array voltage will drop and be clamped by the battery voltage. If using the transmitter should further exceed the demand, the satellite will undergo lockout, inhibiting the transmitter and allowing the batteries to charge.

The battery voltage will become the bus voltage during eclipse powering the receiver, transmitter, microprocessor, and experiment payload. During this mode the pulse-modulated battery charge regulator (BCR) stops operating. Batteries are sized for transmitting at peak power during eclipse. The BCR is reactivated when PANSAT exits eclipse.

Hardware Selection

Hardware components for the EPS will be CMOS devices for low power. The input current required by a gate is typically 1 pA or less. The output current is much larger than the input current, typically 1 mA, which allows for a large fan-out limited only by the propagation delay time [Ref. 4]. CMOS 4000 B-series devices have a recommended supply voltage of 3 to 18 volts [Ref. 5]. The supply voltage for the BCR's CMOS and CMOS compatible devices can be taken directly from the unregulated solar panel voltage since the solar array nominal output voltage is 15.0 volts.

Radiation hardened devices are not a requirement for PANSAT since it will be operating in low-earth orbit. Integrated circuits of grade S are desirable, however, class B are adequate. Similarly, space-rated JANS parts are desirable for discrete components; however, JANTX and JANTXV devices are acceptable [Ref. 6].

Solar Array Design

An average effective area of 1145 cm^2 is used for the design, assuming a 0.1 rad/sec tumbling rate and no solar panel on the base plate. The minimum solar cell efficiency is arrived at by using [Ref. 7].

$$\eta_{min} = \frac{P_o}{(P_i)(A_{eff})}$$

where

η_{min} = PANSAT's minimum solar cell efficiency,
P_o = power generated by solar array (W),
A_{eff} = effective surface area = 1145 cm^2, and
P_i = solar constant = 1353 W/m^2

The total power that must be generated by the solar array, P_o, is calculated from converting the average power per orbit of 11.0 W from Table 1 to the 58 minute sunlight period-per-orbit available.

$$P_o = (11.0 \frac{W}{orbit})(\frac{94\ min}{58\ min}) = 17.8 \frac{W}{orbit}$$

This yields 11.5% for the minimum efficiency of the solar cells.

Field solar cells are selected with cost as a major criterion. The Spectrolab K6700 field cell (10 mil thickness) is a prime candidate. Electron damage is lessened with the 10 mil cell because they are less than 0.30 mm, reducing long-wavelength light absorption. Dual anti-reflective titanium and aluminum coating minimizes reflection losses. Micrometeorite protection is provided by a 6 mil ceria-doped microsheet (CMX) cover on the K6700 solar cell. The CMX cover will also prevent discoloration of the glass from ultraviolet and charged-particle radiation. Dow Corning 93-500 (DC 93-500) adhesive will be used for the CMX cover. The cells will mate with the aluminum panels by an epoxy/glass insulating layer (0.20 mm thick), and a layer of RTV-118 adhesive (0.07 mm thick).

Table 3 gives the values for the solar cell and array power output at beginning-of-life (BOL) and end-of-life (EOL) [Ref. 8]. A radiation factor of 0.96 was used to determine the EOL values. Each of the 17 panels is connected to the distribution bus via a blocking

diode, isolating the panel if it falls below the bus voltage. A suitable blocking diode is the 1MBR5825H1 schottky-barrier rectifier, a high-reliability version of the 1N5825 diode, which has a maximum instantaneous forward voltage drop of 0.36 volt and maximum ambient temperature of 65° C. The blocking diode's forward voltage drop is expected to be 0.27 volts for PANSAT, assuming a 25° C spacecraft interior temperature.

TABLE 3. SOLAR CELL POWER OUTPUT

	BOL Power Output (W)	EOL Power Output (W)
Single Cell	0.128	0.123
Solar Array	18.3	17.6

Battery and Battery Charge Regulator (BCR) Design

The battery cell selected is a Gates lead-acid X-cell providing 2.1 volts at 5 ampere-hours. The Gates X-cell is a terrestrial battery which is considered appropriate for PANSAT's mission. A lead-acid battery was chosen over nickel-hydrogen because of its ability to tolerate overcharging which will be the situation when the satellite exits eclipse. Out-gassing due to overcharging is not expected to be a problem since the batteries will be sealed in a container. The lead-acid batteries also can handle a wider range of temperatures than nickel-hydrogen. Two 10.5 V batteries (5 cells each) will be used on PANSAT.

A battery cell is at 100% at 2.18 V. The battery is considered depleted when it has reached 20% of capacity. The battery bus voltage is designed for 10.5 V. The BCR is designed to prevent reaching a bus voltage of 10.0 V, although the system is designed to operate at this value. Recharge characteristics of the cell may change requiring longer charge times should the cells discharge below 1.81 volts/cell. Charging of the batteries will be done by a float application since power is available during each orbit. At 20° C, the expected float life of a cell is greater than eight years [Ref. 9]. The power budget allows one watt for BCR charging inefficiencies. 90% efficiency is assumed.

The BCR block diagram is shown in Fig. 3. The batteries with five cells at 100% capacity will have a voltage of 10.9 V. Self-discharge will drop the cells below 2.18 V

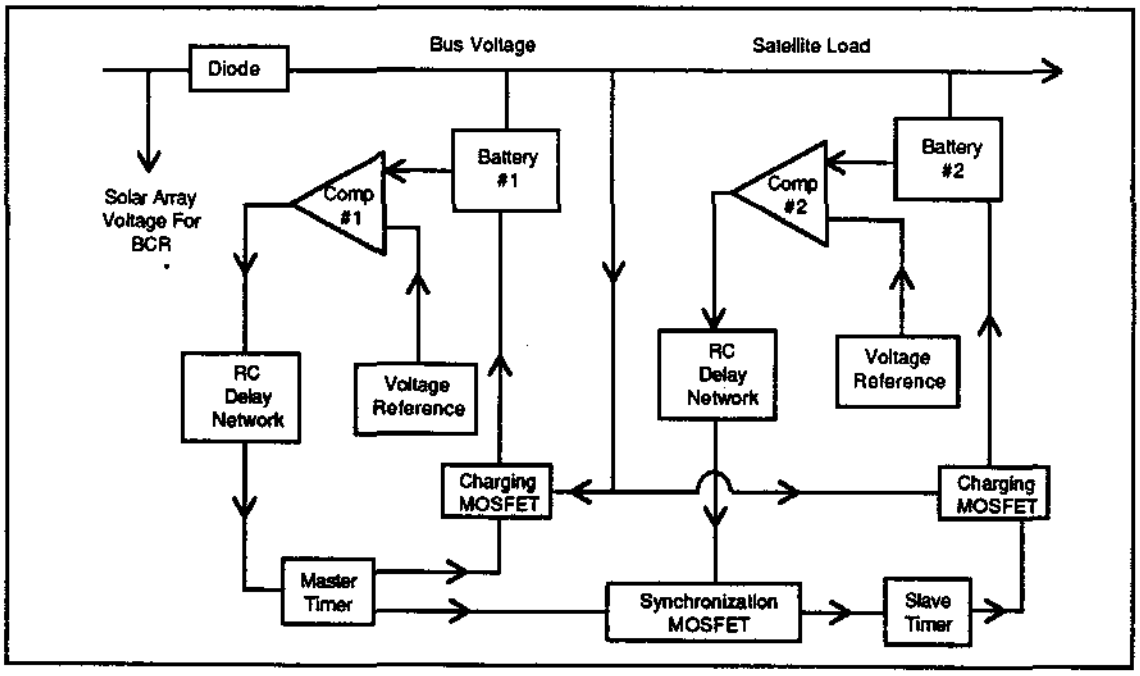

Figure 3. BCR Functional Block Diagram

after ten to fifteen minutes. 10.8 V is therefore chosen as the battery voltage when charging begins. The minimum charge voltage for the batteries is 11.5 V. The maximum charge voltage is 12.0 V. The distribution bus voltage, however, is calculated to be 13.5 V which is too high. This may not be a problem since (a.) the BCR alternates charging between the batteries, (b.) a 75% degradation of the battery life can be tolerated for this mission, and (c.) the calculated 13.5 V value did not take into account wiring losses.

The operation of the BCR is as follows. Comparator #1 measures battery #1 voltage with a 5-volt reference. If the voltage is below 10.8 V, it sends a low output to the reset function of a master-timer, an astable vibrator. The master-timer generates a square wave pulse with a duty cycle of 48%. This output opens and closes a power MOSFET connected across the distribution bus and battery #1. When the square wave is high, the charging MOSFET is closed and charging takes place. When the clock pulse goes low, the MOSFET opens and charging of battery #1 is inhibited by its diode. The square wave output of the master-timer is also sent to a synchronization MOSFET which synchronizes a second timer, the slave-timer.

The comparator for battery #2 measures the battery voltage from a second 5-volt reference source. If the sampled voltage is below 10.8 V, the comparator sends a low signal to the synchronization MOSFET. This signal, with the output of the master-timer, controls the reset function on the slave-timer, enabling or disabling the timer. The slave-timer is identical to the master-timer.

Charging occurs as the comparator receives a battery voltage less than 10.8 volts. When battery voltage exceeds 10.8 volts, the comparator output goes high, disabling the timer, and charging ceases for that particular battery after a short delay. Ideally, both batteries should begin and terminate charging within one charging cycle of each other.

Charging can only occur for one battery at a time. The slave-timer is controlled by the synchronization MOSFET. When the master-timer's output is high the synchronization MOSFET closes, disabling the slave-timer. Only when the synchronization MOSFET is open and the output from comparator #2 is low can the slave-timer generate a clock pulse closing the power MOSFET on battery #2 for charging.

A working prototype of the BCR was developed and performed as predicted. A setpoint of 10.7 V was determined the best for the comparators, removing instabilities due to self-discharge. Time to recharge the batteries from 10.0 V to near full capacity was nearly fourteen hours. This time was two hours greater than expected. These anomalies can be attributed to the degraded condition of the batteries. The setpoint value and the charging ability will probably change with new cells.

Power Conditioning Considerations

The development of PANSAT's subsystems is occurring in parallel. The power requirements of the subsystems have not been defined; however, recommendations can be made. First, non-dissipative type convertors, switch-mode, are the best choice for meeting subsystem power requirements. These convertors are low in mass and small in size. Output voltage can be greater than, equal to, or less than the input voltage based on three different configurations; buck, buck-boost, and boost. Switch mode convertors offer higher efficiencies than dissipative, or linear, regulators [Ref. 10].

A second recommendation is that redundant convertors/regulators should be used to eliminate a single point failure. The outputs of the convertors are tied together, with the primary convertor output voltage biased slightly higher than the secondary convertor. The selected convertor should be capable of remote sensing where, via a voltage divider, feedback from the load is provided to the convertor. The voltage dividers can be used to trim the base between the primary and secondary convertors.

COMM SUBSYSTEM DESIGN

The preliminary design of the COMM subsystem considers two modes of operation: the repeater mode and TT&C mode. In the repeater mode, a message is reformatted and retransmitted implementing the AX.25 protocol which has addresses embedded. The message is then received by a ground station with the correct address as well as the originating station. PANSAT will need to decipher the address and act accordingly by retransmitting if the address is not for the satellite, or by performing whatever TT&C commands are relayed.

The terminal node controller (TNC) links the TT&C with the receiver and transmitter by reading the address and sending the information to the TT&C. The TT&C controls the link operation. It switches the RF connection, enables/disables the transmitter and receiver for the half-duplex operation, and monitors the EPS to disable the transmitter if the satellite's battery charge falls below the minimum threshold.

The system design depends mainly on the orbit parameters. A shuttle mission of 480 km and 28.5° inclination is considered. The Navy Exercise Support Terminal (NEST) software was used to display orbits from various view points, including the satellite view of a ground station [Ref. 11]. Figures 4 and 5 show various ground tracks and satellite communication footprints for the orbit considered. A low-earth orbit induces a time-in-view constraint requiring quick acquisition at a low signal-to-noise ratio and data transferred with minimum errors. Table 4 shows the time-in-view for the passes of Fig. 4.

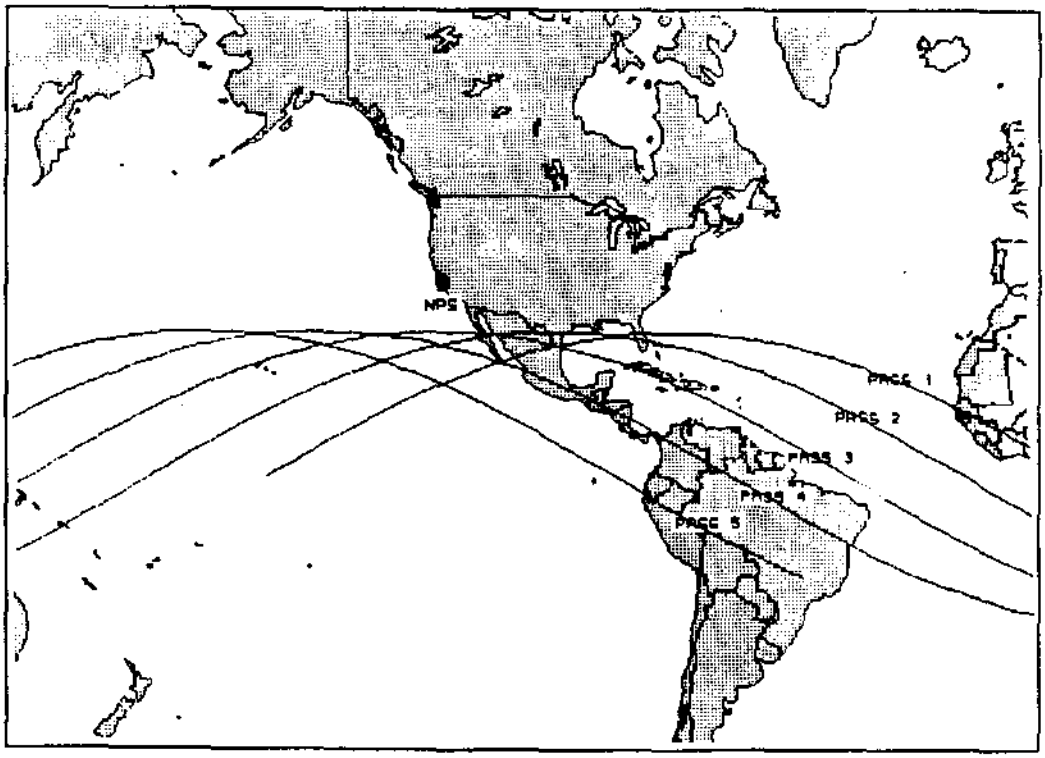

Figure 4. Ground Track for 480 km, 28.5° Inclined Orbit

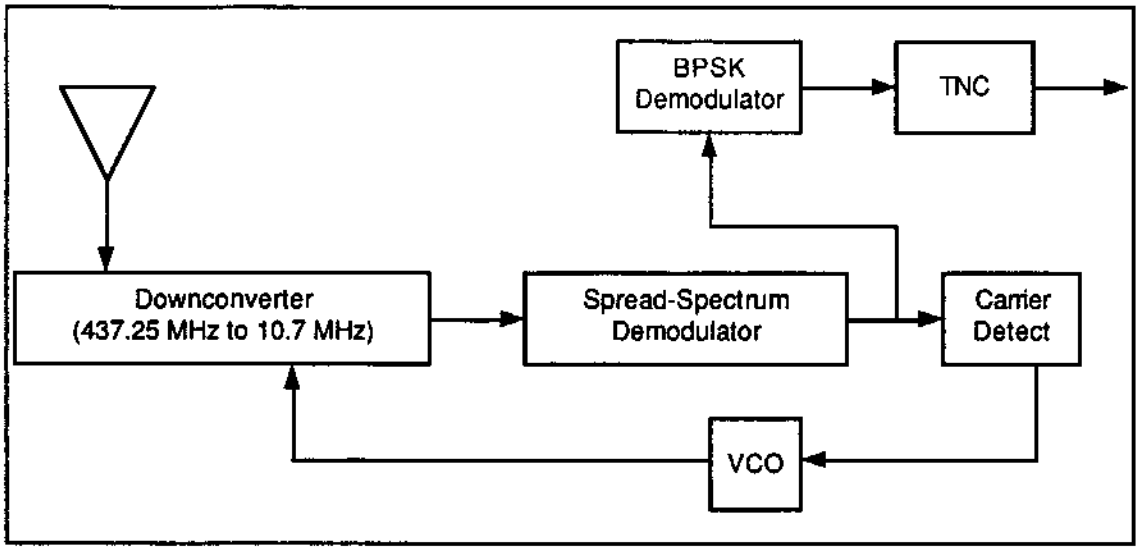

Figure 6. Receiver Subsystem

Spread-Spectrum System Design

The spread-spectrum demodulator is divided into three sections: acquisition, tracking, and demodulation. Figure 7 shows the configuration of a non-coherent demodulator. The PN-coded signal is modulated with the system's PN sequence. This signal is passed through a bandpass filter with bandwidth approximately $2R_b$. If the signal is nearly synchronized, the integrator produces a voltage greater than the specified threshold and the tracking circuit is activated. Otherwise, the PN sequence is advanced one-half chip, and the process is repeated.

The lower part of the figure is the 'early-late gate correlator' which takes the punctual PN-sequence and divides it into an early version, shifted back by one-half chip, and a late version shifted up one-half chip. These signals are then used to separately modulate the input signal. The outputs from the squaring circuit are subtracted and an error signal is produced for the loop filter. The output from the loop filter controls the timing of the PN-sequence generator to minimize the error and permit fine tracking of the input PN-sequence. With the system's punctual PN-sequence closely correlated to the input signal, the BPSK signal can be recovered in the demodulator (top of figure).

The major design constraints for a spread-spectrum system are the choice of PN-code length and method of acquisition. These decisions directly affect the complexity of the system and its acquisition time. The PN maximal length, linear-shift-register PN sequence has a predictable autocorrelation function and a noise-like waveform which enhances circuit operation. The PN-code length was determined by considering the sequence repetition rate, mission duration, and acquisition time for the circuit described below (Fig. 7).

A base-line PN-code length is determined assuming a PN code of length N, probability-of-detection of one, prabability-of-false-alarm of zero, and no doppler shifts or oscillator instabilities [Ref. 14,15]. For a T_{acq} less than 60 seconds, N is less than 205,714 chips. The longest maximal-length PN code is $N = 2^{17} - 1 = 131,071$ chips.

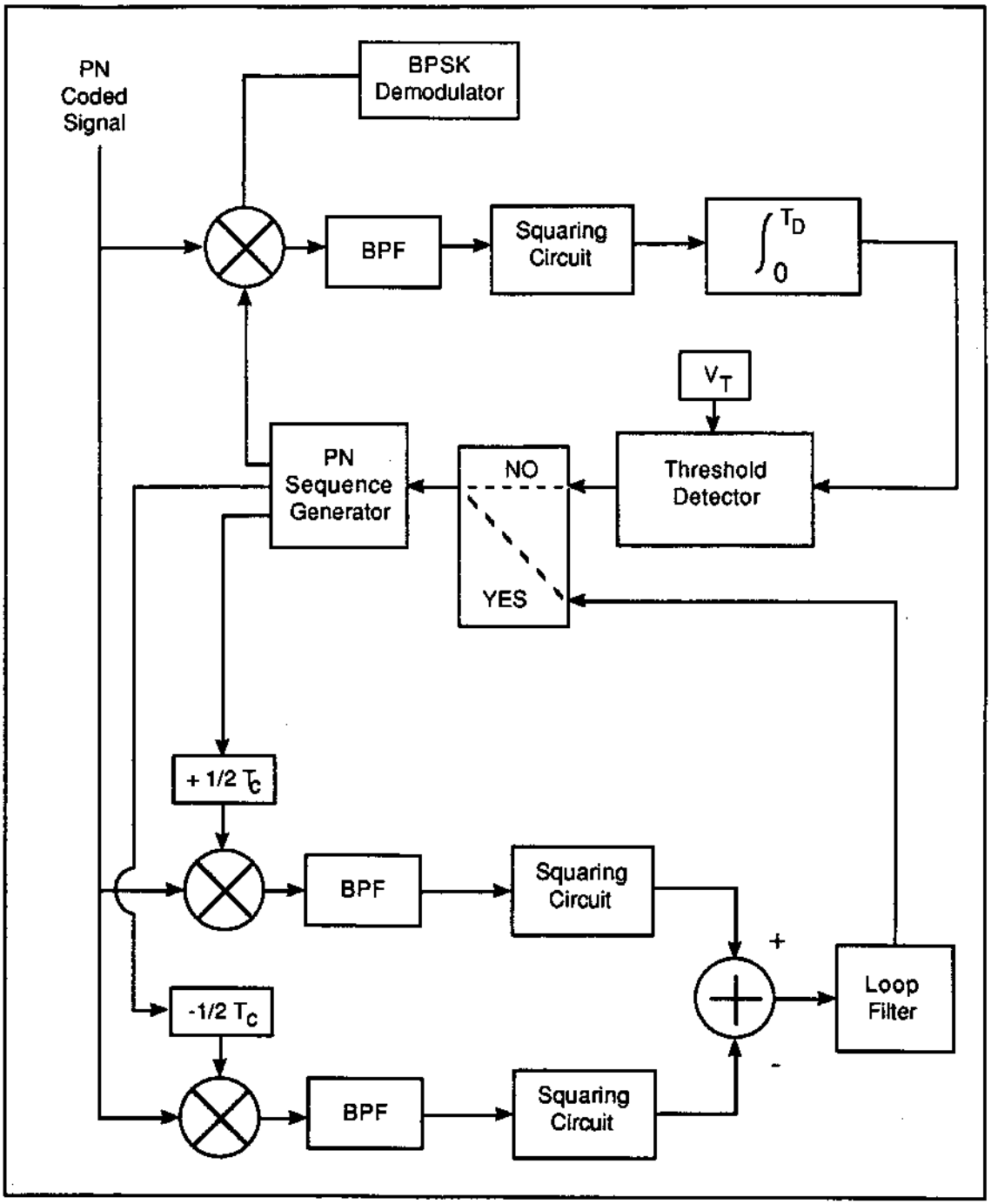

Figure 7. Spread-Spectrum Configuration

Doppler affects the acquisition process by changing the effective code sweep-rate during the integration period and during a false acquisition. An analysis was done for T_{acq} as a function of doppler assuming a probability-of-detection of 0.9, probability-of-false-alarm of 0.01, and K value of 2 [Ref. 14, p. 418]. Figure 8 shows T_{acq} as a function of doppler.

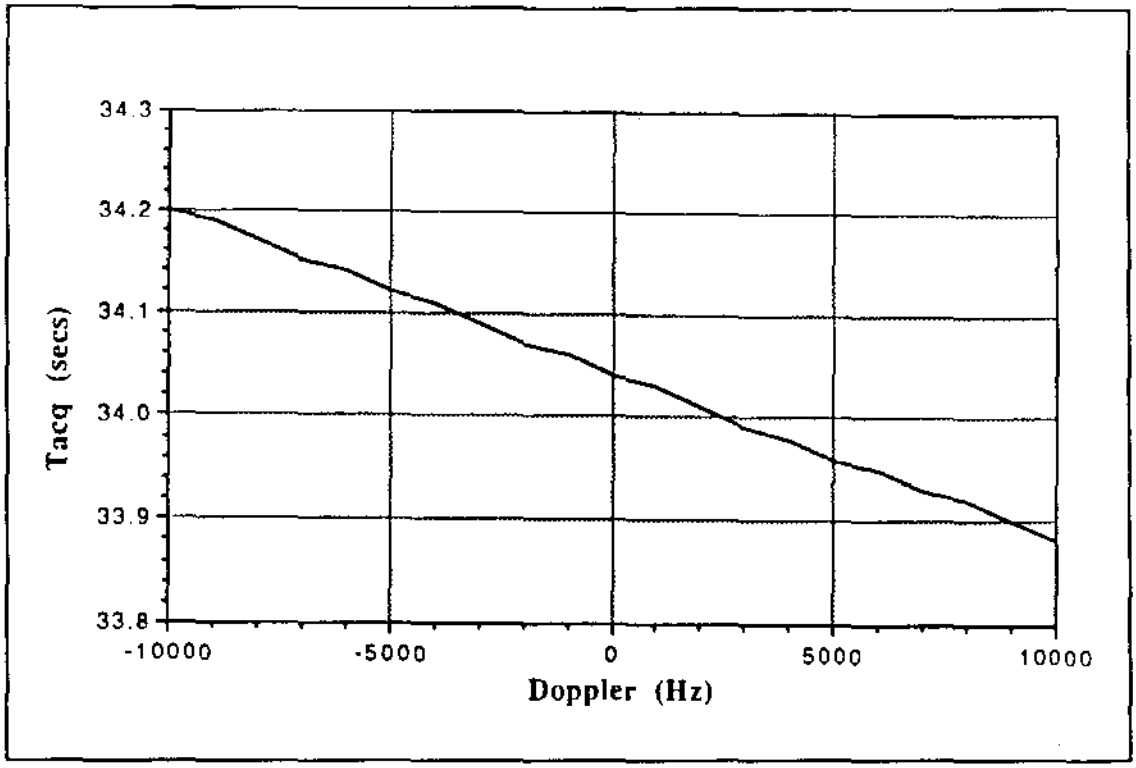

Figure 8. Acquisition Time as a Function of Doppler

A Butterworth filter was chosen because of its "maximally flat" frequency response [Ref. 16]. Two bandpass filters were considered for this design with bandwidths of 1200 Hz and 2400 Hz. The characteristics of the third-order filters in Table 7 are superior over the others since a marginal increase in peak times (t_p) provides a 6 dB increase in filter attenuation at ω_a, the cutoff frequency.

TABLE 7. COMPARISON OF FILTER CHARACTERISTICS

N	M_{dB} (@ $2\omega_a$)	t_p (msec) 1200 Hz	t_p (msec) 2400 Hz
1	-7.0	.32	.16
2	-12.3	.64	.30
3	-18.1	.66	.32
4	-24.1	.74	.38

The dwell times were chosen iteratively to ensure an average acquisition time near 60 sec. A dwell time of 200 chips (0.4 msec) was used for the 1200 Hz filter; and 100 chips (0.2 msec) was used for the 2400 Hz filter. Little difference is seen between the two filters at low SNR's for acquisition times. At high SNR's, a significant difference is evident. The 1200 Hz filter asymptotically approaches 56 seconds while the 2400 Hz filter approaches 28 seconds. The 2400 Hz filter was chosen for simulation as a result.

The initial analysis estimated a dwell time by using the step response of a single-pole filter. The step response was integrated to determine the time it took to pass the same energy through the higher-order filter selected for the system as the single-pole filter. It was found that the time to pass the same energy was 0.16 msec for the 3-pole filter vice 0.08 msec for the single-pole filter. This indicates that the 100-chip (0.208 msec) dwell

time used to determine the acquisition time permits the filter to pass enough energy to the integrator for signal detection.

Simulation of Acquisition System

A computer model of the acquisition system was developed on a Sun-4 workstation at the TRW Communication Lab at Redondo Beach, California using the BOSS™ software. The system was modeled to determine the effects of noise and a jammer on the integrator output. The level of this output and its variation due to different signal conditions is essential in setting the detection threshold and probability-of-false-alarm. A static model was produced to obtain the results under a correlated and an uncorrelated input signal. The system was also modeled as a baseband system and not at the 10.7 MHz IF expected in the design.

The simulation parameters were based on the rate of the PN-sequence, R_p. The time-step used for the simulation was $1/10R_p$ or 0.208333 msec, and the length of the simulation varied between 2.0 ms and 3.0 ms. This resulted in a frequency resolution of 500 to 333 Hz in spectrum plots [Ref. 16].

The results show that near the theoretical maximum of the jammer levels, the threshold could not be properly established. The primary cause for the degradation was the integrator bandwidth permitting excessive energy in its output sidelobes. A reduction in the bandwidth requires a reduction in the PN-code length (which is directly proportional to the acquisition time) reducing the performance of the tracking circuit. Since the tracking circuit performance is the primary factor in recovering the data, a long code is essential.

CONCLUSION

A preliminary design of the EPS and COMM subsystem for the PANSAT project has been completed. A breadboard circuit of the battery charge regulator was developed and performed as expected. As the satellite design continues, the actual power loads on the EPS will be established. Components for the EPS design have been identified for estimated power loads supporting a conservative low-earth orbit of 480 km and 28.5° inclination.

The COMM design supports direct sequence spread-spectrum modulated BPSK. It includes the preliminary design of a step-search acquisition system meeting all the constraints for the satellite mission. The COMM will need to interface with the satellite computer or terminal node controller (TNC) for implementing the AX.25 communications protocol. The design constraint of a half-duplex mode of communication has been successfully implemented in the preliminary design.

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