DEVELOPMENT OF A SPACE COMPUTER -- A LOW RISK APPROACH TO CONTROL AND DATA PROCESSING APPLICATIONS IN SMALL SATELLITES

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ABSTRACT

In early 1991, Honeywell delivered three RH-1750A based flight computers to complete the AST III program in support of a Phillips Laboratory Autonomous Navigation Demonstration Satellite. The delivery was significant for the following reasons: it was the first delivery of a space qualified RH-1750A computer, the RH-1750 Multi-Chip Module (MCM) was transitioned from a research and development effort to a B-level flight part, and, design to delivery of the first flight unit was accomplished in only 16 months.

The AST III program consists of several sequential efforts which will demonstrate and validate state-of-the-art spacecraft autonomy hardware and software in an operational space environment.

The Honeywell 1750A GVSC Flight Computer (GFC), developed for the Air Force's Phillips Lab, achieved its primary goal: develop a low-cost, low-risk computer for onboard data processing while demonstrating a secondary goal of transitioning new technologies to flight in a short period of time. The 1750A CPU utilizes the Honeywell RH-1750 Generic VHSIC Spaceborne Computer (GVSC) chipset. The RH-1750 was developed by Honeywell under an Air Force contract and is manufactured using Honeywell's Radiation Insensitive CMOS (RICMOS)™ III process.

The GFC is ideally suited for the small satellite environment. Its low cost, low weight, low power, high performance and flexibility make it an excellent candidate for control and data processing applications. The 32-bit GVSC local bus supports zero wait state access to the static

RAM resulting in a maximum throughput of 2.5 MIPS under worst-case conditions. The local expansion bus (also 32 bits), accepts up to four I/O assemblies, including DMA capability, and supports I/O throughput rates up to 2 Mwords per second.

INTRODUCTION

One of the major challenges facing the satellite industry today is low risk procurement of low cost, reliable flight computers that can be developed in short periods of time amid changing requirements. Decreased funding and increased competition for those funds make it imperative that potential flight computers be as close to "off the shelf" as possible in order to reduce development risk and avoid non-recurring costs.

This paper presents a description of a flight computer that can meet this challenge. The GVSC Flight Computer (GFC), shown in Figure 1, was developed by Honeywell for the AST III program to support the Air Forces's Phillips Laboratory Autonomous Navigation Satellite. The GFC was designed and delivered in 16 months for integration into a small spacecraft to be placed in low earth orbit for 8 to 12 months where autonomous spacecraft experiments will be performed.

The heart of the GFC is Honeywell's RH-1750 Generic VHSIC Spaceborne Computer (GVSC) chipset which provides a low weight, low power, high performance solution to satellite-based control and data processing problems. The GVSC CPU was developed by Honeywell under an Air Force contract and is manufactured using Honeywell's Radiation Insensitive CMOS (RICMOS)™ process. This 1.2 μm technology is low power, radiation hardened (>10^6 rads), and single-event upset immune (<10^{-8} errors/bit/day).

SIGNIFICANT ASPECTS OF GFC DEVELOPMENT

There were several significant accomplishments on the AST program that were critical to the development of the GFC:

- The GVSC Multi-Chip Module (MCM) was transitioned from a research and development project to a B-level flight part. This was a calculated risk to reduce the anticipated weight of the GFC to less than the original 12-lb requirement. Use of the MCM allowed the entire CPU to fit on one card, as opposed to the two cards required by the use of the 5-chip Single Chip Package (SCP) chipset approach. In addition to the resulting weight reduction, use of the MCM also improved overall reliability by reducing the total number of interconnects.

- The design to delivery cycle was a challenging 16 months. We were able to meet this schedule by applying the concepts of concurrent engineering throughout the execution of the program by maintaining a small core multi-discipline team that included hardware, software, mechanical/packaging, assembly, test, quality and management personnel.

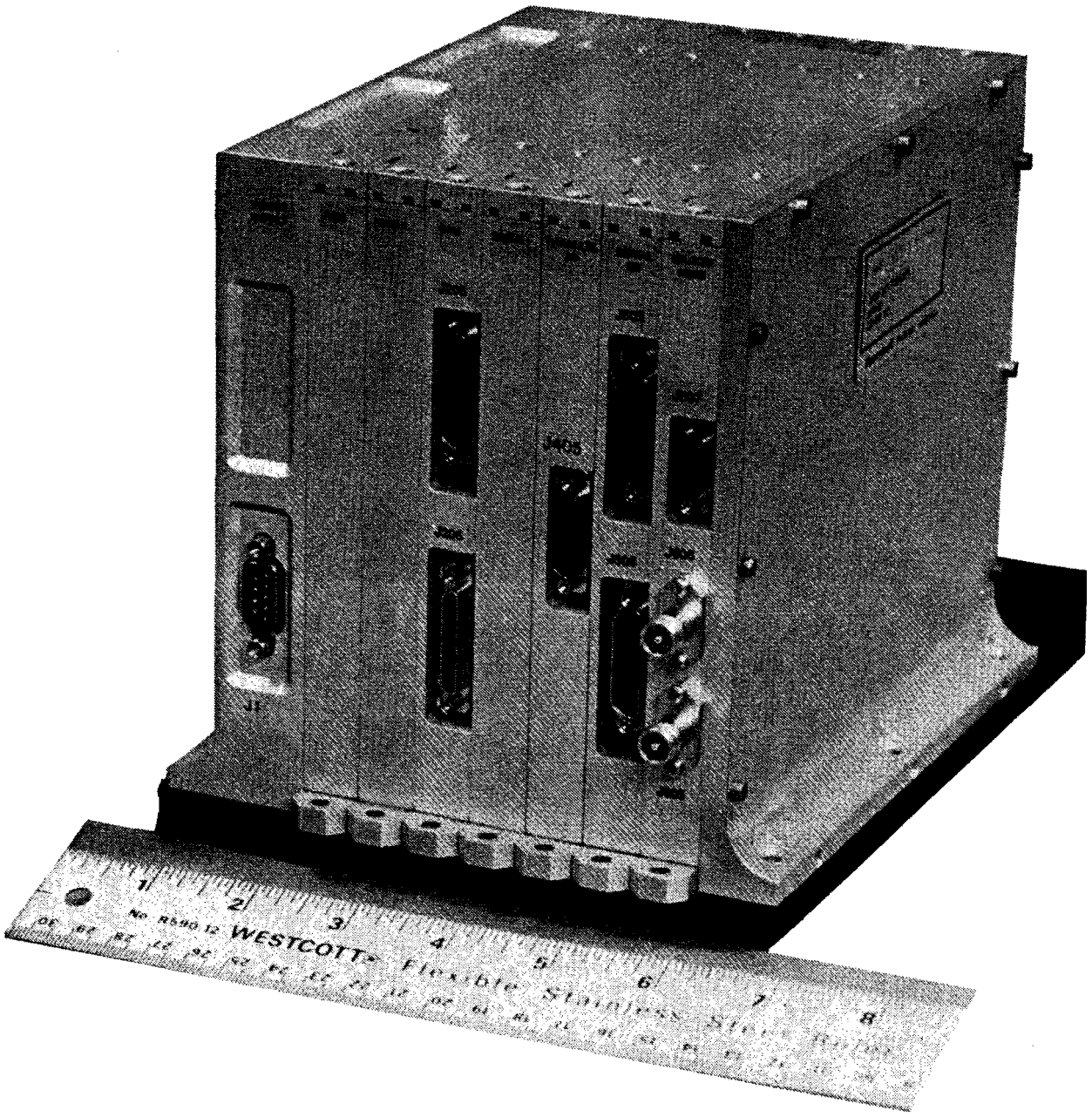


Figure 1. Small size and low power for small satellite applications

- A Prototype Development Environment (PDE) was delivered 7 months after contract start that included a Honeywell Prototype Development Unit (PDU) modified to be functionally equivalent to the flight computer and a software development system that allowed users to get hands-on Ada experience early in the flight software development cycle.

- In order to meet program specific operating system requirements, a customized operating system was developed by modifying TLD's off-the-shelf Multi-Program Kernel (MPK). This approach drastically reduced development risk associated with using a purely custom operating system.

FLIGHT HARDWARE

The GVSC Flight Computer, whose interface diagram is shown in Figure 2, provides a versatile hardware environment capable of executing 1750A-targeted Ada flight software. Based on Honeywell's GVSC MIL-STD-1750A chipset, it features 64K of startup Electrically Erasable and Programmable Read-Only Memory (EEPROM), 448K of reprogrammable user EEPROM for storage of application programs, 1 megaword of static RAM for high-speed program execution and data storage, an IEEE-488 interface, five serial ports, one parallel port and a dual redundant MIL-STD-1553B bus interface. A software programmable clock provides variable power and throughput performance. Mechanical packaging is based on the Sandia Laboratory developed Sandia Avionics Computer (SANDAC V)

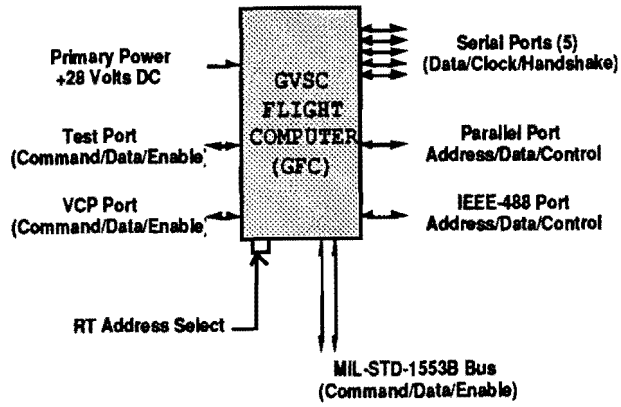


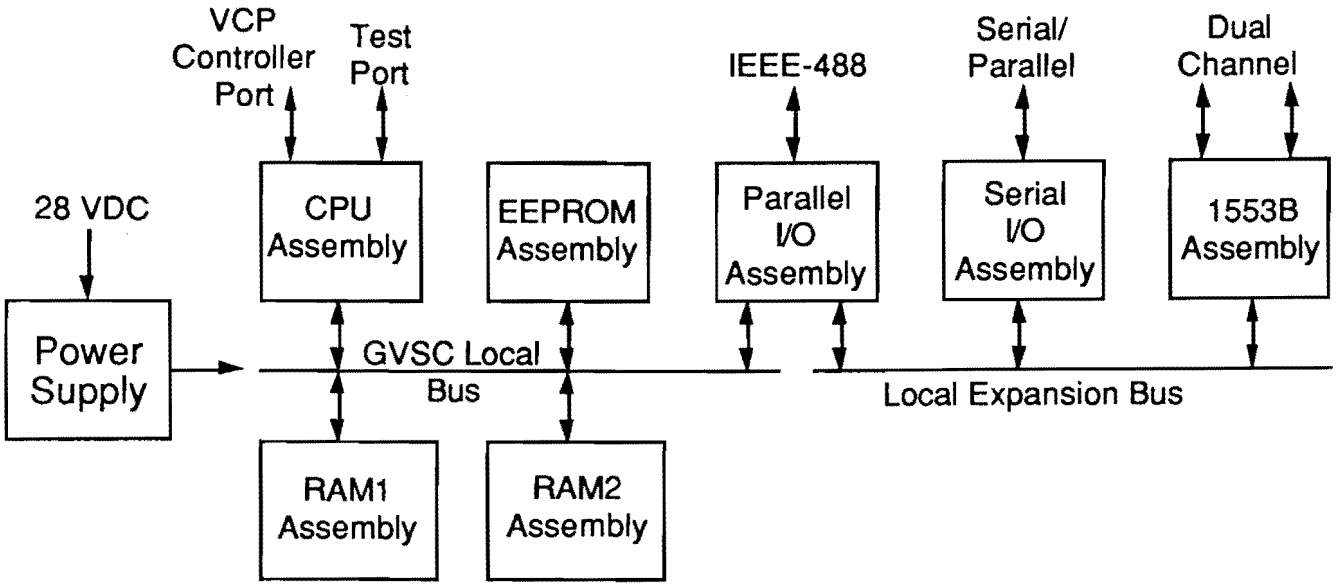
Figure 2. GFC Interface Diagram

which is manufactured by Honeywell. The weight of the GVSC Flight Computer is 10.6 pounds. Performance is achieved with a cold plate temperature range of -20° Centigrade to +60° Centigrade.

The GVSC Flight Computer's internal busses provide high performance and flexibility for small satellite applications. The 32-bit GVSC local bus supports zero wait state access to the static RAM. This results in a maximum throughput of 2.5 Million Instructions Per Second (MIPS). The local expansion bus (also 32 bits) accepts up to four I/O assemblies, includes DMA capability, and supports I/O throughput rates up to 2 Mwords per second. Figure 3 shows the GFC functional components and describes the major features of each. Table 1 lists the GVSC Flight Computer specifications. Table 2 lists the I/O rates for the various I/O interfaces.

Characteristic	Specification
Throughput	2.5 MIPS (DAIS mix at 13.5 MHz) 1.25 MIPS (DAIS mix at 6.75 MHz) 0.6 MIPS (DAIS mix at 3.38 MHz) 0.3 MIPS (DAIS mix at 1.69 MHz)
Architecture	MIL-STD-1750A (GVSC)
EEPROM memory	64k words (w/EDAC) - startup ROM 448k words (w/EDAC) - user available
SRAM memory	1 megaword (w/EDAC) - user available (512 kwords per module)
Interrupts	MIL-STD-1750A defined Parallel I/O Serial I/O MIL-STD-1553
Interval timers	2 MIL-STD-1750A defined (separate from CPU clock)
Parallel I/O	IEEE-488
Serial I/O	SANDAC system I/O module
Computer/computer I/F	SANDAC MIL-STD-1553B module
Size	7.0 x 6.5 x 6.9 in.
Weight	10.6lb
Power (typical)	25W (2.5 MIPS) 20W (0.3 MIPS)
Power (absolute maximum)	50 W
Cooling	Cold plate - (-20°C to +60°C)

Table 1. GVSC Flight Computer Specifications



CPU Assembly
- 1750A GVSC Multi-Chip Module
- Low voltage sense
- Clock rate adjust
- Watchdog timer
- Virtual Control Processor (VCP) port
- Test port
- GVSC Local Bus Interface

RAM1 Assembly
- 512 Kwords of user RAM
- Error Detection and Correction
- GVSC Local Bus Interface

Parallel I/O Assembly
- IEEE-488 Bus Interface
- GVSC Local Bus Interface
- GVSC Local Bus to Local Expansion Bus conversion
- Local Expansion Bus Interface

1553B Assembly
- MIL-STD-1553B Dual Redundant Bus Interface
- Local Expansion Bus Interface

ROM Assembly
- 64K words of startup EEPROM
- 448K of user available EEPROM
- Error Detection and Correction
- GVSC Local Bus Interface

RAM1 Assembly
- 512 Kwords of user RAM
- Error Detection and Correction
- GVSC Local Bus Interface

Serial I/O Assembly
- Five configurable serial ports
- Programmable Counters/Timers
- Input/Output Discretes
- Parallel Port Interface
- Local Expansion Bus Interface

Power Supply
- Primary input: 28 VDC
- Secondary output: +5 VDC (capable of 16 amperes source current)

Figure 3. GVSC Flight Computer Functional Description

I/O Interface	Read	Write
Parallel	560K words/sec	520K words/sec
IEEE-488	550K words/sec	580K words/sec
1553B	724K bits/sec	724K bits/sec
Serial	19,200 baud	19,200 baud

Table 2. GFC I/O Rates

FLIGHT SOFTWARE

The two major GFC flight software components are the Startup ROM (SUROM) component which provides power-up initialization and test and the Real-Time Operating System (RTOS) component which makes initialization, diagnostic, scheduling and I/O device resources available to Ada application programs.

The SUROM initializes the GVSC flight computer to a known state at power-up and tests the processor and I/O functions. An exhaustive suite of tests, comprised of a core component, an extended component and I/O component are executed to ensure the processor state. The core processor tests verify that the processor and memory are working sufficiently to execute the other power-up tests. Failures in the core tests indicate that the processor is not working sufficiently to isolate any failures. The core processor tests include the EEPROM test, RAM tests and GVSC instruction set tests. Once the core processor tests are passed, the chance that the subsequent power-up tests can isolate independent failures is good. These extended processor tests include the watchdog timer, machine error, interrupt, memory management unit and block protect RAM tests. The I/O tests include XIO instruction access, I/O device register and I/O loop back tests. Upon completion of the startup tests, the RTOS is initialized. If no failures or failures that can be ignored were identified, the RTOS is copied from EEPROM to RAM and invoked. Diagnostic and On-Orbit Reprogramming (OORP) capabilities are provided to allow on-orbit fault isolation and work around. If disabling failures were detected, a restricted Mini-OORP (MOORP) is executed from start-up EEPROM. In either case, the power-up test status is made available to the MIL-STD-1553B bus. Figure 4 depicts the power-up initialization and test sequence.

The GVSC Flight Computer RTOS, a Honeywell developed customized version of the MPK developed by TLD Systems Ltd, of Torrance, Calif., provides the hardware/application program interface. TLD's MPK, which provides standard kernel features such as timer handling, exception handling, task-context switching, interrupt vectoring and support

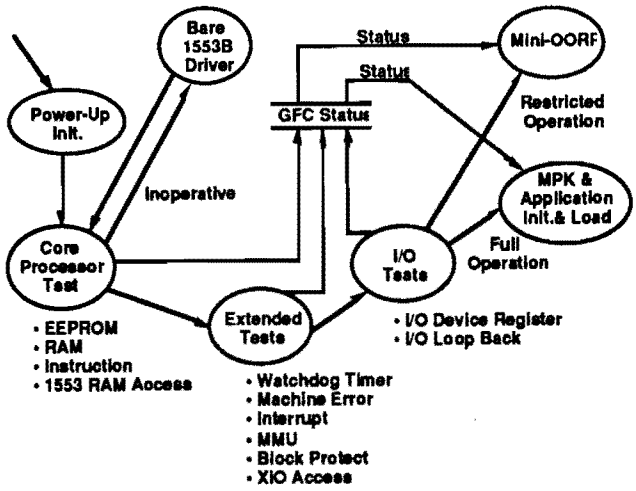


Figure 4. GFC Power-up Sequence

for multiple independent programs was combined with GVSC Flight

Computer specific test, I/O device driver, and on-orbit reprogramming functions to form the GVSC flight computer RTOS. RTOS manages multiple Ada programs running on the same processor, providing resource sharing and communication facilities among the various programs. Each program resides in its own address state and has complete access to all TLD-supported features of the Ada programmable language. Specific enhancements/additions to the TLD MPK included:

- Mailbox services
- Interlock services
- Watchdog timer services
- I/O device drivers
- Foreground memory scrubbing to prevent double-bit memory errors
- GVSC Flight Computer Built-In Function (BIF) support
- 8-megaword memory addressing
- System time accuracy improved to one microsecond
- On-Orbit Reprogramming

The GVSC Flight computer On-Orbit Reprogramming (OORP) capability is part of the MIL-STD-1553B I/O driver software. OORP enables external control of the GFC through several functions that can be accessed through the 1553B port. These functions are:

- Execution of operating system calls
- Load and dump GFC memory (RAM and EEPROM)
- Execute 1750A XIO operations and report results
- Execute power-up restart
- Begin execution at any physical address
- Suspend/resume an application program
- Synchronize system clocks

S/W DEVELOPMENT ENVIRONMENT

The purpose of the SDE, shown in Figure 5, is to reduce software development risk by providing software developers with a system that facilitates flight software development and test long before flight hardware is available.

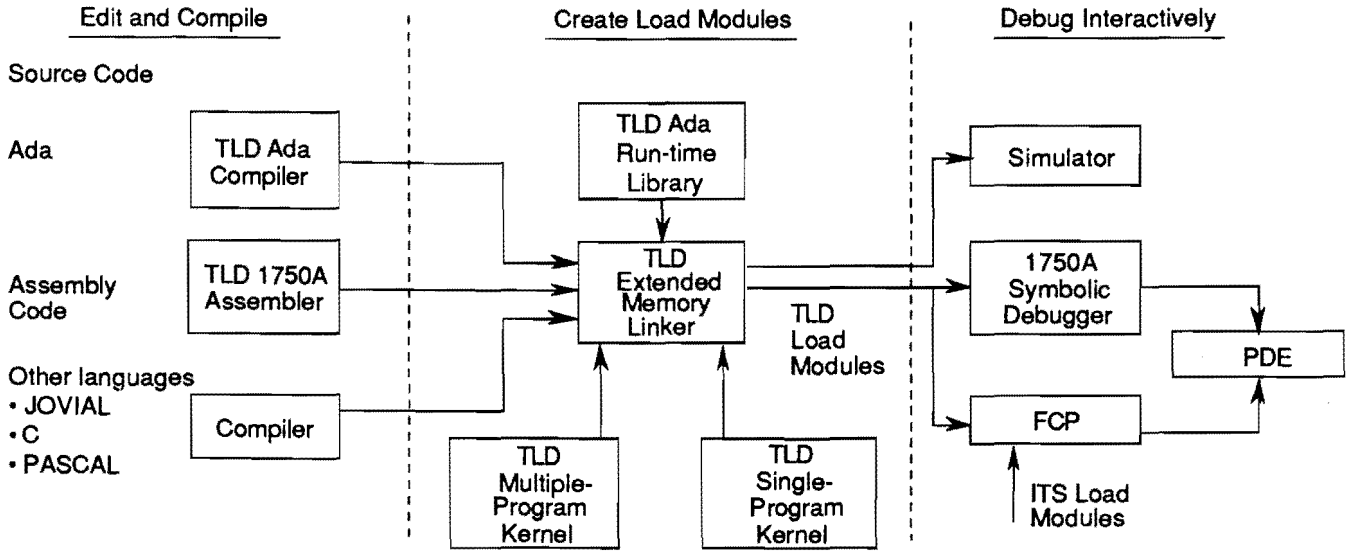


Figure 5. Software Developement Environment

Development of Ada programs is facilitated by a Vax-based integrated Ada software development toolset and the target PDE (shown in Figure 6).

The Vax-based portion of the SDE consists of the TLD Ada/1750A toolset and the Functional Control Program (FCP), which provides a user friendly software interface between the host Vax and the PDE.

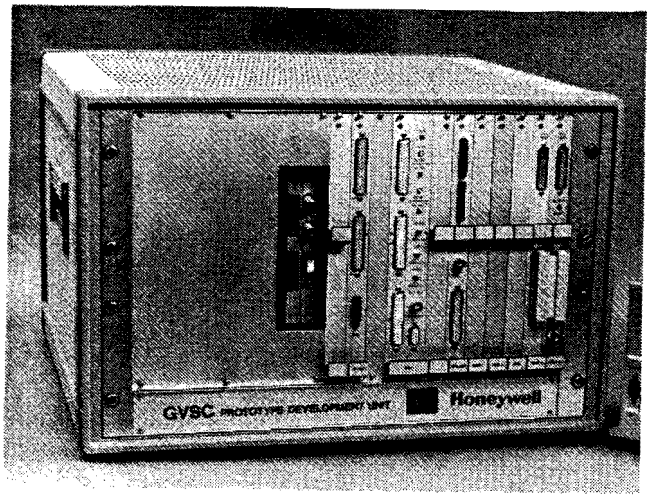


Figure 6. Prototype Development Environment

The TLD toolset provides the software developer with tools to compile Ada programs, link Ada and 1750A assembly modules, build executable load images and simulate execution of the load modules. The toolset generates the proper downloadable files and information such that multiple programs can be running on the GFC under control of RTOS (up to 15 independent programs can be controlled by RTOS). Also supplied with the toolset is a symbolic debugger that has been targeted to the GVSC that provides all standard debugger features.

Program download, test and debug is provided by a combination of FCP, the custom Program Control, Monitor and Test (PCMT) board contained in the PDE, and the Virtual Control Processor (VCP). The VCP is a simple, parallel link built into the GVSC that facilitates external control of the CPU. Superior emulation capability is provided by the FCP/PCMT/VCP subsystem because the actual target hardware is in use. The interaction between FCP (and host symbolic debuggers) and the PCMT is depicted in Figure 7. FCP, which is basically a low-level debugger, provides a user friendly interface that allows the user to download software modules, start and stop the CPU, read and write memory and CPU registers, set software breakpoints and measure program execution time. It also provides the ability to trap on any combination of 80 GVSC local bus signals and up to 16 external signals and to trace bus activity. FCP is especially valuable for test and debug of assembly routines for which a suitable symbolic debugger may not exist.

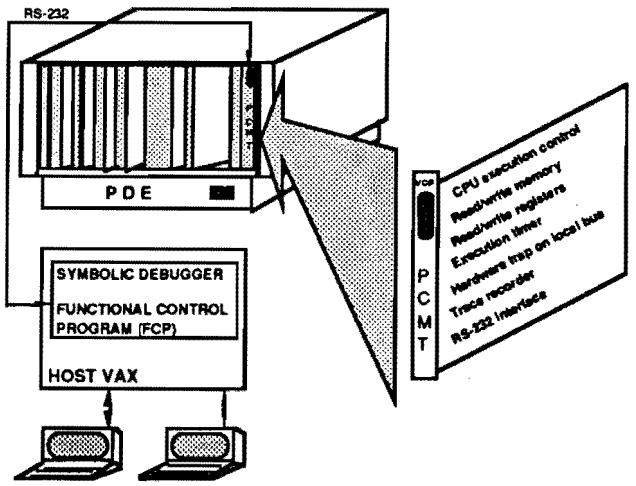


Figure 7. The PCMT provides real-time control of the target hardware.

The PDE is a modified Honeywell GVSC Prototype Development Unit (PDU) designed to operate in a lab environment. It includes the GVSC 1750A CPU, reprogrammable startup and user EEPROM with Error Detection and Correction (EDAC), SRAM with EDAC, a local expansion bus interface to support Serial I/O, Parallel I/O and the 1553B bus. The PDE provides the software developer with a Functionally Equivalent Unit (FEU) for test and debug of flight software and provides the hardware developer with a platform for functional performance verification of flight hardware modules.

A GVSC Flight Computer test adapter is available that provides external control (halt, run, examine memory, download, etc.) of the GFC during ground test. This provides a means for debugging actual flight software on actual flight hardware. The test adapter, a stand-alone version of the PCMT board packaged with its own power supply, allows communication with the GFC through the external VCP test port on the CPU module.

GVSC FLIGHT COMPUTER TEST

A full suite of hardware and software tests was developed to qualify the GVSC Flight Computers.

GFC processor tests include throughput, programmable clock, power sense, watchdog timer, machine error interrupt, instruction set and memory/block protect. ROM and RAM modules are tested for full addressability and EDAC operation. The Serial I/O and Parallel I/O data rates are verified. The Power Supply is tested for proper voltage conversion and power consumption at the various clock frequencies. Environmental tests include room temperature functional test, thermal cycle, thermal vacuum, random vibration and shock. Figure 8 shows the GFC environmental test profile.

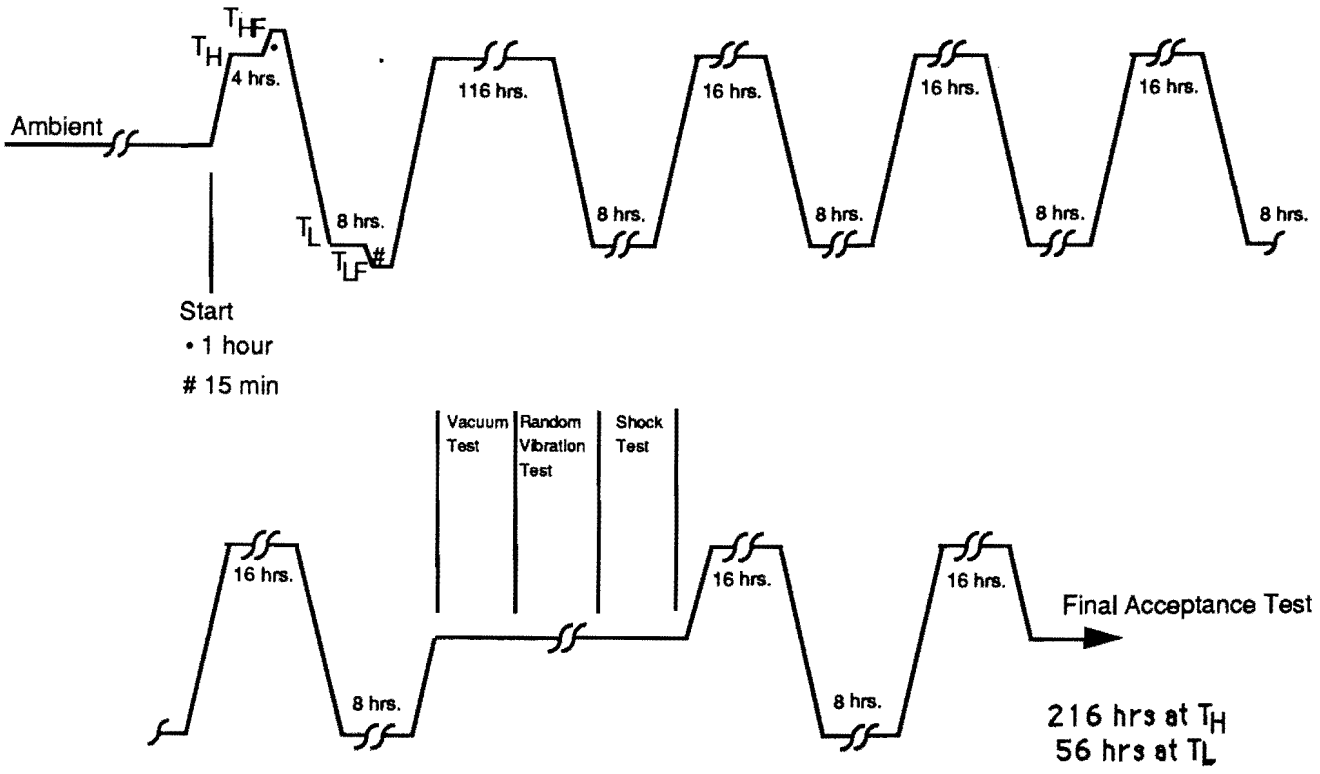
The software acceptance tests were designed to test the features of the Real-Time Operating System; both the customized and off-the-shelf portions. In addition to verifying that the RTOS satisfies the requirements developed in the software requirements analysis phase, the tests also ensure that programs do not react inappropriately for conditions not explicitly addressed in the requirements.

Two PC-based test equipment sets were designed and built for PDE and GFC functional and environmental acceptance testing. Use of off-the-shelf interface cards and the GFC test adapter provided a flexible, low cost mechanism for automated control and monitoring of PDE and GFC tests.

FEATURES

The GFC has several features which make it adaptable to potential small satellite applications. In addition, the basic design can be easily modified to meet requirements not currently supported.

The software programmable clock (13.5 MHz, 6.75 MHz, 3.38 MHZ, 1.69 MHZ) provides variable throughput from 0.3 MIPS to 2.5 MIPS with typical power con-



Notes:

1. Temperture as indicated:
   T_L = +70° C, T_H = -20° C
   T_{HF} = +80° C or First Failure
   T_{LF} = -30° C or First Failure
2. System power removed during excursion to T_L.
3. System "soaked" at T_L for 1 hr. or unit equilibrated.
4. Dryers installed in temperature chamber.
5. Tolerance per MIL-STD-810 latest revision.
6. Temperature rate of change not to exceed 4 degrees Centigrade per minute
7. Vacuum:
   0.0001 Torr: @-20°C Cold Plate Temp for 12 hrs
   @+60°C Cold Plate Temp for 12 hrs
8. Vibration: 18g for 30 sec., 8g for 15 min.
9. Shock: 3-axis Haversine; 320G peak.

Figure 8. GFC Environmental Test Profile

sumption from 20 to 25 watts, respectively. Other clock rates can be provided with minimal modification to the GFC.

Use of PC-based test equipment has tremendous cost and schedule advantages. A large selection of commercial off-the-shelf hardware is available for test interfaces. The test equipment made use of commercial MIL-STD-1553B, IEEE-488, RS-232 and discrete I/O cards. A large selection of off-the-shelf software allows the use of vendor-supplied drivers in the test software. Initial test software

development can be done on any PC, freeing up the test set for higher priority use. The test software is portable and easily modified allowing on-site functional and/or environmental testing if required.

The SANDAC V slice construction approach to packaging the GFC has several key benefits. First, by taking advantage of the existing special facilities and procedures established at Honeywell that are required to assemble and test low-cost, flight quality hardware, development risk associated with new module design can be greatly reduced. This approach provides a stable, well-documented method for design and test of flight computer modules. During GFC design, the Honeywell "skunk works" production facility was able to provide existing mechanical, electrical, assembly and environmental test information on which to base new GFC module designs. Second, the slice approach makes it possible to add and/or remove modules without chassis or backplane redesign.

The SDE provides a highly flexible and easy to use system for software development in lieu of flight hardware. The PDE can be configured to be functionally equivalent to various flight computer designs. Honeywell has excellent relationships with the major Ada toolset vendors, allowing rapid development of robust toolsets targeted to various GVSC-based hardware configurations. Currently, three major Ada toolset vendors have targeted their product to the GVSC. Each has modified its run-time kernel to provide support for Built-In-Functions (BIFs), expanded memory addressing and console I/O. Each also provides the full range of software development tools including symbolic debuggers that provide full symbolic debug capability with either the PDE or the GFC as the target. In addition, each is expanding its line of products to support SUN and DEC Station host computers.

We performed an analysis of the effects of single-event upsets (SEUs) on the GFC SRAM (Micron 32k x 8) parts. Since the RAM memories used in the flight computer were not radiation hardened, single-event upsets can occur at a high rate. Our approach to reducing the potential of SEU-induced double bit errors is to guarantee that all memory is scrubbed within a specified time period. The memory scrubbing feature of RTOS, which executes at each occurrence of the system clock interrupt, significantly reduces the probability of double bit errors due to SEUs while consuming only 3% of processor throughput. The scrub routine scrubs the entire GFC memory (RAM and EEPROM) in 1.4 minutes. At this scrub interval, the probability of no double-bit errors in one month due to SEUs, in 1.5 Mword of memory, is greater than 0.93. The capability to modify the number of words scrubbed during each RTOS clock interrupt, and thus decrease scrub overhead, is provided through the OORP interface. The memory scrub feature can also be disabled.

Based on new part data, a second approach to reducing double-bit errors is available. The Micron memories can be replaced with pin-for-pin compatible Hitachi or IDT devices which have SEU rates an order of magnitude lower than the Micron part used in the GFC. At the same 1.4 minute scrub interval,

which have SEU rates an order of magnitude lower than the Micron part used in the GFC. At the same 1.4 minute scrub interval, the probability of no double bit errors is increased to greater than 0.98. Increasing the scrub interval to 5.6 minutes, and thus reducing the scrub overhead to 0.7%, yields the original probability of 0.93.

CONCLUSION

Honeywell's on-time, on-budget delivery of the GVSC Flight Computers on the AST III program completed a highly successful intra- and intercompany effort -- the GFC went from the "drawing board to the launch pad" in only 16 months. Our "skunk works" approach allowed us to deviate from normal operating procedures and develop an efficient, multi-discipline team capable of solving design issues in real time to meet the short delivery schedule.

The GFC is a flexible, low-power, low-cost computer ideally suited for spaceborne applications such as instrument control, data processing and space-based experiments. Existing facilities and procedures make it possible to deliver the GFC as a near "off-the-shelf" unit or, if need be, easily reconfigure to support a broad range of memory, throughput and I/O requirements. The availablity of a Functionally Equivalent Unit allows end users to get a significant head start developing flight software.

The GVSC Multi-Chip Module is the heart the Honeywell Space Computer (HSC), Honeywell's generic spaceborne computer. It is also the heart of Honeywell's higher quality and strategic radiation hardened space computer products targeted for high-end operational satellite systems. These higher end (and more expensive) space computer products are being used on a variety of Air Force and Navy programs.

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