THE GEOSAT FOLLOW-ON (GFO) ALTIMETER

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Abstract

The NAVY GEOSAT Mission (1985-1990) demonstrated the ability of an altimeter equipped satellite to provide global measurements of mesoscale ocean features with 3 centimeter precision. The GEOSAT radar altimeter, developed by JHU/APL, was an enormous success. Built with early 1980's technology, the GEOSAT altimeter weighed 191 pounds and consumed 146 watts. The GFO radar altimeter, under development by E-Systems Inc., will achieve the GEOSAT measurement capability, but at one-third the weight and one-half the power (48 pounds, excluding antenna, and 76 watts). The GFO altimeter uses the same proven linear FM waveform, pulse repetition frequency (PRF), pulse compression technique, and alpha-beta tracker design as the GEOSAT radar altimeter, but takes advantage of current RF and digital signal processing technologies to produce an instrument that is both light-weight and reliable. Also, thanks to a cooperative working relationship with JHU/APL, the GFO radar altimeter design encompasses "lessons learned" from both the GEOSAT and TOPEX programs. Analysis of the range, waveheight, and back-scattering cross section performance indicates that the GFO altimeter will achieve the GEOSAT performance in all areas. Finally, the GFO altimeter design encompasses features allowing economical expansion; including a C-band channel for improved range accuracy, and a 33% higher PRF for improved instrument noise performance. The GFO dual-channel altimeter would weigh 107 pounds and consume 156 watts.

Altimeter Measurement Requirements

The reader should consult reference [1] for a detailed discussion of radar altimeter operation. This paper includes a brief review only for completeness.

The GFO altimeter functions as a 13.5 GHz nadir looking radar. The altimeter operates in a pulse-limited mode, wherein the lateral extent of the intersection of the spherical pulse, representing the locus of all points equidistant from the radar, with the sea surface is small when compared with the antenna beamwidth.

Figure 1 depicts the mean ocean return waveform. The altimeter begins by transmitting a narrow pulse of microwave radiation toward the sea surface at nadir. The favorably oriented wave facets in the altimeter footprint reflect back the radiated pulse, with the early returns arriving from the wave crests. As the pulse continues to propagate, the circular illuminated area expands until the trailing edge of the pulse has passed through the wave troughs. As the pulse continues to propagate, the circular footprint becomes an annulus of constant area. The corresponding reflected power would also remain constant was it not for the exponential roll-off of the antenna. The 1/2 power point on the leading edge conforms closely to the reflected power when the pulse is at mean sea level. Therefore the two-way travel time of the pulse determines the range from the satellite to mean sea level. In addition, the slope of the leading edge and the peak amplitude determine the significant waveheight ($H_{1/3}$) and back-scattering cross section, respectively.
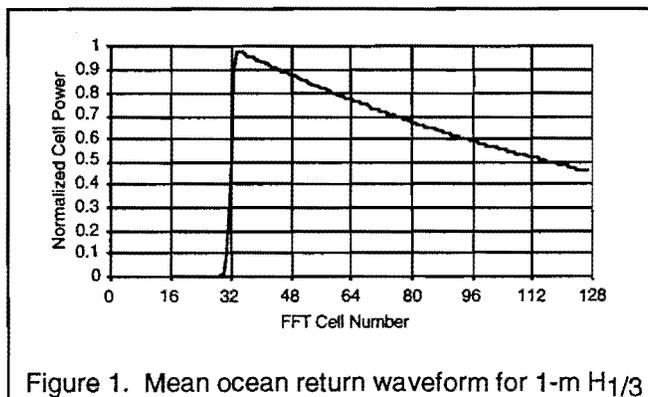

Figure 1. Mean ocean return waveform for 1-m $H_{1/3}$

The GFO altimeter provides 3 primary measurements:
1. The range from the radar antenna to mean sea level,
2. Significant waveheight ($H_{1/3}$), and
3. The normalized back-scattering cross section (σ°) of the ocean surface.

In addition, the GFO altimeter data will allow computation of the off-nadir pointing angle and ice index. The former being used in the ground processing corrections, and the latter to flag transitions between water and ice.

The GFO altimeter specific requirements are:
1. For 2-m $H_{1/3}$, the white noise standard deviation on the 1 second averaged range measurements, shall be less than or equal to 3.5 cm.
2. For 2-m $H_{1/3}$, the white noise standard deviation on the 1 second averaged $H_{1/3}$ measurements, shall be less than or equal to 15 cm.

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3. The $H_{1/3}$ measurement shall be made with a RMS. accuracy equal to or better than 0.5-m or 10% of $H_{1/3}$, whichever is greater.

4. The normalized back-scattering cross section ($\sigma°$) accuracy shall be better than or equal to 1 dB after ground calibration.

5. Achieve track acquisition within 5 seconds.

Analysis indicates that the GFO altimeter will acquire track within 2 seconds typical, achieve a 3 cm range precision, measure $\sigma°$ to an accuracy of 0.5 dB, and achieve an $H_{1/3}$ RMS. accuracy of 0.5-m or 10%.

GFO Altimeter Design

Altimeter Overview and System Design

Figure 2 depicts the GFO altimeter. The Digital Chirp Generator produces a 12.72 GHz, 102.4 μsec pulse, with a 320 MHz bandwidth. The pulse is upconverted to 13.495 GHz in the Upconverter/Frequency Multiplier, amplified in the solid state Power Amplifier, and routed to the 3 frequency feed antenna by the T/R Switch (the altimeter shares an antenna with a dual-frequency radiometer). The transmitted waveform is a 5.6 watt (after TX circuit losses), 102.4 μsec pulse, with a 320 MHz bandwidth.

The T/R Switch routes the return signal to the Receiver, where it is amplified and downconverted to a 775 MHz IF. The Receiver uses the 12.72 GHz linear FM chirp pulse from the Digital Chirp Generator as the local oscillator to the 1st mixer, transforming range separation into frequency separation. Thus allowing the ocean return waveform to be sampled using Fourier Transform techniques. Finally, The Receiver AGCs and downconverts the 775 MHz IF to baseband in-phase and quadrature-phase channels.
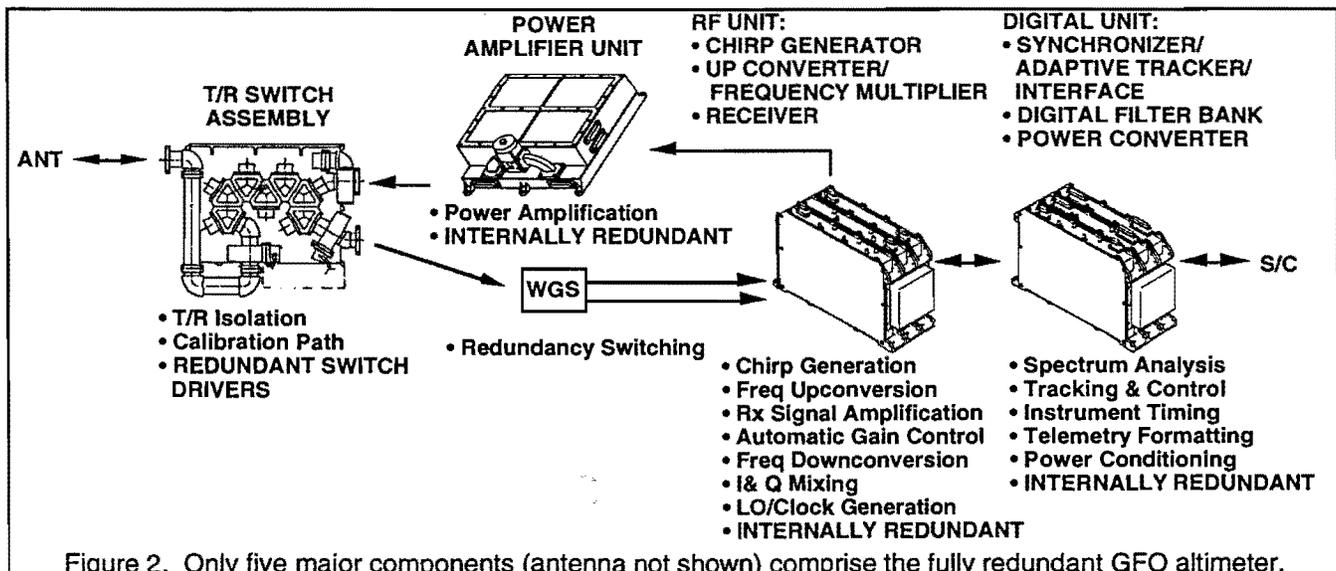
The Digital Filter Bank performs the Fast Fourier Transform (FFT), and accumulates 50 of the ocean return waveforms to produce the mean ocean return waveform. The Adaptive Tracker accepts the mean ocean return waveform and computes range, $H_{1/3}$, and AGC (automatic gain control, converted to back-scattering cross section in the ground processing). On a per pulse basis the Adaptive Tracker provides: a coarse timing adjustment (12.5 nsec LSB) to the Synchronizer gate array, a fine timing adjustment (48 psec LSB) to the Digital Filter Bank, and an AGC adjustment (1 dB LSB) to the Receiver. The adjustments ensure that the ocean return waveforms align within the FFT bandwidth, and that the receiver operates in its linear region.

The final components of the altimeter are: the Synchronizer, an ECL gate array that controls the altimeter transmit, receive, and telemetry operations; the Power Converter, which supplies secondary power to both the altimeter and radiometer; and the Interface module, which provides the altimeter and radiometer command and data telemetry interface to the spacecraft. The GFO altimeter system characteristics and the science telemetry content are listed in Tables I and II, respectively.

The major improvements achieved through the GFO altimeter development are:

1. A significant reduction in mass and power (Table III),

2. A major improvement in instrument reliability,

3. An improvement in radiation hardness, and

4. A highly integrated electronics design consisting of only four boxes, with overall dimensions of: T/R Switch -- 7.2 x 8.8 x 3.8 inches^3, Power Amplifier -- 3.0 x 9.0 x 8.75 inches^3, RF Unit -- 9.0 x 13.0 x 5.0 inches^3, and Digital Unit -- 9.0 x 13.0 x 5.0 inches^3.

Figure 2. Only five major components (antenna not shown) comprise the fully redundant GFO altimeter.

Current technology and sound engineering achieve a significant weight reduction. A solid state power amplifier replaces a heavy TWTA. The T/R Switch is an improved version of the highly integrated, light weight, ERS-1 design. GFO's digitally synthesized, direct IF, chirp approach requires only 1/2 the components of the previous baseband synthesis implementations. GFO's chirped acquisition approach requires no additional acquisition circuitry. In the RF modules, microstrip filter techniques reduce the number of active components. A single chip FFT processor samples the ocean return waveform. Finally, field programmable gate arrays (FPGAs) provide high density packaging for the low speed digital logic, while a mature ECL gate array process provides high density packaging for the high speed digital logic.

Redundancy cross-strapping provides an improved instrument reliability. Care must be taken, however, to balance reliability with altimeter calibration. Each RF cross strap doubles the number of calibration paths though the instrument, thereby doubling the pre-launch calibration time. GFO achieves an optimum balance between instrument reliability and instrument calibration. The GFO altimeter design attains a predicted reliability that exceeds 0.9 at 8 years, yet limits the number of calibration paths to 4.

The GFO design is highly resistant to single-event-upsets (SEUs). A space qualified 1750A silicon-on-sapphire (SOS) microprocessor implements the Adaptive Tracker. The altimeter program and data memory are radiation hardened read only memory (ROM) and static random access memory (SRAM). A space qualified, inherently hard, ECL process implements the critical Synchronizer and Digital Chirp Generator circuits. In the unlikely event an SEU should occur, the GFO altimeter autonomously resets without ground intervention.

GFO makes extensive use of gate array packaging and surface mount technology to achieve a high board-level packing density. In addition, the RF and Digital Unit circuit boards are packaged using our mature "slice" technology, that have both FLTSAT and MILSTAR heritage.

T/R Switch Design

The Transmit/Receive Switch (TRS) provides the transmit/receive duplex operation and receiver protection during transmit. The TRS design is an improved version of the ERS-1 design. Figure 3 shows the TRS block diagram. The TRS consists of six latching ferrite isolators; a fixed circulator; a precision height-bias calibration path; and an antenna power monitor. The TRS supports internally redundant switch drivers and power monitor for enhanced reliability.

Table I. GFO Altimeter Characteristics

WAVEFORM :	
• TYPE:	LINEAR FM SWEEP
• CENTER FREQUENCY:	13.495 GHz
• PULSE WIDTH:	102.4 µSEC
• BANDWIDTH:	320 MHz - TRACK
	5 MHz - ACQUISITION
• PRI:	980 µSEC
ANTENNA:	
• TYPE:	1 m OFFSET-FED
	PARABOLIC
• GAIN:	40 dB
• BEAMWIDTH:	1.6 deg
TRANSMIT/RECEIVE SWITCH:	
• SWITCH TECHNOLOGY:	LATCHING FERRITE
TRANSMITTER:	
• SOLID STATE TYPE:	GaAs FET
• PEAK OUTPUT POWER:	7 W
• AVG POWER CONSUMPTION:	11.4 W
RECEIVER:	
• TYPE:	DOUBLE-SUPER-
	HETERODYNE
	775 MHz (1st IF)
	0 Hz (2nd IF)
• NOISE FIGURE:	3 dB
• AGC:	0 - 63 dB IN 1 dB STEPS
SIGNAL PROCESSOR:	
• A/D CONVERTER (2):	7 BITS + SIGN
• WAVEFORM SAMPLES:	128
• WAVEFORM SAMPLE RESOLUTION:	47 CM
• ADAPTIVE TRACKER:	1750A SOS
• TRACKER TYPE:	ALPHA - BETA
• TRACKER HEIGHT ADJUSTMENT LSB:	0.7325 CM
OPERATING MODES:	
• STANDBY:	NON- TRANSMITTING
• TRACK 1:	IDENTICAL TO GEOSAT TRACK
	MODE, NO WAVEFORM DATA TLM
• TRACK 2:	USES GROUND SELECTABLE
	TRACKING PARAMETERS,
	NO WAVEFORM DATA TLM
• TRACK 3:	ADDS WAVEFORM DATA TLM TO
	EITHER TRACK 1 OR TRACK 2
• CALIBRATE:	2 CALIBRATE MODES
• TEST:	10 TEST MODES
• UPLINK PROGRAM:	PROVIDES FOR ON-ORBIT
	REPROGRAMMING
• MEMORY DUMP:	DUMPS ADAPTIVE TRACKER
	MEMORY CONTENTS
INPUTS:	
• POWER BUS:	24 - 34 V DC
• REFERENCE SIGNAL:	5 MHz
• COMMANDS:	RELAY (11)
	SERIAL DATA (16 BIT, 25.6 KBPS)
TLM OUTPUTS:	
• TRACK 1 & 2 SCIENCE DATA:	19 8-BIT WORDS
	AT 10/S RATE
• TRACK 3 & CAL SCIENCE DATA:	91 8-BIT WORDS
	AT 10/S RATE
• ENGINEERING TLM:	8 ANALOG
	16 THERMISTOR
	26 HEALTH/STATUS

Table II. Science Data Frame Contents

- CURRENT OPERATING MODE
- LAST COMMAND RECEIVED
- SATI STATUS
- TRACK PARAMETER CHANNEL/AT MODE
- HEIGHT
- HEIGHT RATE
- HEIGHT ERROR (DH)
- SIGNIFICANT WAVE HEIGHT
- AGC
- VOLTAGE PROPORTIONAL TO ATTITUDE (VATT)
- TRACKING GATE INDEX
- AGC GATE AMPLITUDE
- EARLY GATE AMPLITUDE
- LATE GATE AMPLITUDE
- MIDDLE GATE AMPLITUDE
- L6 - E6 AMPLITUDE
- ATTITUDE GATE AMPLITUDE
- NOISE GATE AMPLITUDE
- WAVEFORM DATA
- WAVEFORM SCALING FACTOR

Table III. Weight and Power Trends

ALTIMETER	LAUNCH DATE	WT (LB)	POWER (W)	REDUNDANCY
SEASAT [2]	1978	207*	165	NONE
GEOSAT-A [3]	1985	191*	146	PARTIAL
ERS-1 [4]	1990	220*	150	FULL
POSEIDON [5]	1992	55	50	NONE
GFO	1996	48	76	FULL

* Includes antenna and structure

The ferrite circulator provides approximately 25 dB of isolation between the transmit/receive ports and the antenna. The six latching ferrite isolators, configured as a ferrite switch matrix, provide the transmit/receive duplex operation, and supply a minimum of 100 dB isolation to the receiver port during transmit. The latching ferrite devices have extensive space heritage and offer high reliability, fast switching time, low switching energy, high RF power handling capability, and low insertion loss. A current pulse changes the circulation (magnetic state) of the switches, and the magnetic flux level in the ferrite is maintained without additional holding current. The TRS design incorporates fully redundant switch driver circuits for increased reliability.

The calibration path, between the transmit and receive ports of the TRS, has a fixed attenuation of 130 dB and a time delay of 25 nsec. The time delay provides a time separation between the calibrate signal and any leakage signals. The delay line is implemented using 16.9 feet of 0.070 inch (UT 70-LL) semi-rigid coaxial cable. The semi-rigid provides 22.3 nsec of delay; with the remaining 2.7 nsec provided by the waveguide components. The delay line coils to a 3.5 inch diameter, 0.5 inch high coil, and weighs approximately 200 grams.

The redundant power monitor measures the energy in the transmit pulse. A cross-guide coupler couples the output power to a diode detector. The detector provides an analog voltage proportional to the transmit power.

The receive path includes a low loss, waveguide preselection filter; with and out-of-band rejection of better than 50 dB. The total insertion loss for the receive path, including the filter and ferrite switches, is less than 1.1 dB.

The construction of the TRS design uses waveguide technology, measures 22.1 x 8.9 x 18.3 cm, has a mass of 2.0 kg, and consumes 1.5 watts.

Solid State Power Amplifier (SSPA) Design

The use of a solid-state power amplifier (SSPA) in spaceborne applications has increased significantly in recent years. The SSPA higher reliability, smaller size, and better performance, have resulted in an increased popularity over their traveling wave tube amplifier (TWTA) counterparts. The SSPA technology eliminates the need for high voltage power supplies, and has improved reliability, linearity and noise performance. SSPAs, using discrete field effect transistor devices that provide up to 10 Watts of output power, have accumulated thousands of hours of operational experience, with no on-orbit failures reported to date. The GFO RA uses an SSPA designed to provide 7 Watts (peak) of transmit power at Ku-band. Table IV summarizes the characteristics of the GFO SSPA. The GFO SSPA assembly houses both prime and redundant amplifiers.

Figure 4 is a functional block diagram of the SSPA. Three main functional sections make up the SSPA:

1. Amplifier section consisting of the:
   a. A low-power amplifier
   b. The driver amplifier
   c. The power amplifier

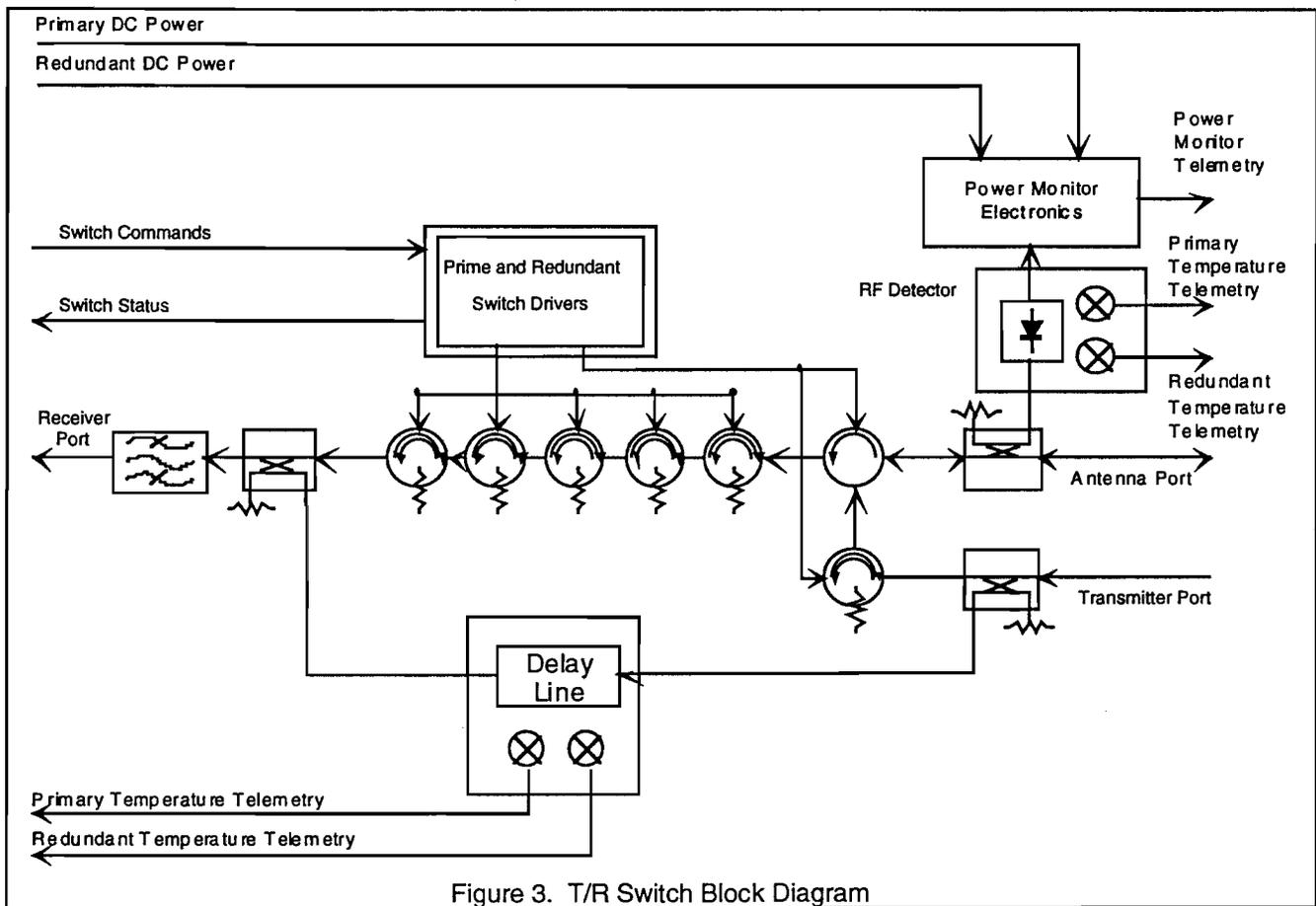2. DC-to-DC power converter
3. Control and telemetry circuits

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Figure 3. T/R Switch Block Diagram

Table IV. SSPA Characteristics.	
Frequency (GHz)	13.495
Bandwidth (MHz)	± 200
Input Power (dBm)	0 ± 2 dB
Output Power (dBm)	38.5
Pulsewidth (μs)	102.4
PRI (μs)	980
Volume (cm)	7.6 x 22.2 x 22.8
Weight (lb)	9.0
Average DC Power (watts)	14.8
Operational Life (yrs)	8 (min)

Amplifier Section

The Ku-band low-power amplifier section consists of three cascaded amplifiers using packaged gallium arsenide (GaAs) field effect transistor (FET) devices. These devices can provide up to 24 dBm of output power at the 1 dB gain compression point. The FETs were characterized by measuring their scattering parameters and DC characteristics. A commercial microwave computer-aided design (CAD) package designed the bias, input and output matching circuits. The low-power amplifier section also includes two isolators and two voltage variable PIN diode attenuators as shown in the block diagram. The

isolators minimize VSWR interactions that can cause excessive amplitude ripple and mismatch losses. The attenuators are part of an automatic level control (ALC) circuit, which maintains a constant output power over varying input and environmental conditions. The output power of the low-power amplifier section is a nominal 15.5 dBm. The amplifiers are constructed on alumina substrates, and mounted on Kovar carriers.

The driver amplifier consists of three FET amplifier gain stages. A single device was selected for both the driver amplifier and the power amplifier. The typical output power for this device is 1.8 Watts with a drain-to-source voltage (V_{ds}) of 10 Volts, and a drain-to-source current (I_{DS}) of 480 mA. Since the driver amplifier output requirement is only 26 dBm, the devices are biased at a V_{DS} of 9 Volts, and at a reduced I_{DS}. Cascaded amplifiers, with a design similar to the low-power amplifier section, comprise the first two driver amplifier stages. The output stage consists of two amplifiers, a two-way splitter at the input, and two two-way splitters at the outputs. The four outputs drive the individual power amplifier stages.

The power amplifier uses eight FETs. Realizing a higher output power than can be attained

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from individual devices, requires parallel combining techniques. The SSPA design parallel combines two individually designed power amplifiers, and uses stripline two-way quadrature-phase power dividers and combiners to achieve a balanced configuration. Each of the balanced amplifier pairs is capable of providing 34.5 dBm of output power at Ku-band. A parallel combination, using a four-way stripline combiner, of four balanced amplifier pairs, provides an output power of 10 watts. Finally, the power amplifier includes an output isolator, harmonic filter and power detector. The power detector provides a DC voltage proportional to the output power, which adjusts the ALC attenuator in the low-power amplifier.

Commonly used methods, for pulsed operation of microwave GaAs FET devices, are gate switching and drain switching. Gate switching involves changing the gate voltage from its normal operating voltage to pinch-off. This essentially shuts off the device except for the drain-to-source leakage current which can be 50 mA or higher for a power FET device. The method used for the GFO SSPA design relies on drain voltage switching. By switching the drain voltage off between transmit pulses there is no drain-to-source leakage current. The disadvantage of drain switching is the burden it places on the power converter and switching circuit designs. The power converter and switching circuits must be able to switch the high drain currents while maintaining the proper drain voltage. Locating the switching circuitry near the FET devices minimizes the switching inductance, and maintains a reasonable switching speed. In actual operation the amplifier is turned on approximately 20 μs before receiving the transmit pulse. This overcomes the effects of thermal transients, which degrade the amplitude and phase linearity of the amplifier.

DC-to-DC Power Converter (PC)

The PC converts primary spacecraft voltage to required secondary voltages. The PC is an efficient, high frequency, pulse-width modulated (PWM) design; that uses energy storage as the means for maintaining load regulation during pulsed operation. The design uses radiation hardened power MOSFETs, planar power transformers and high frequency multi-layer capacitors.

Control and Telemetry Circuits

The control circuit switches the amplifier sections on during the transmit pulse, and switches them off when there is no transmit pulse. Controlling the drain voltage, as previously discussed, accomplishes this on/off switching. The telemetry
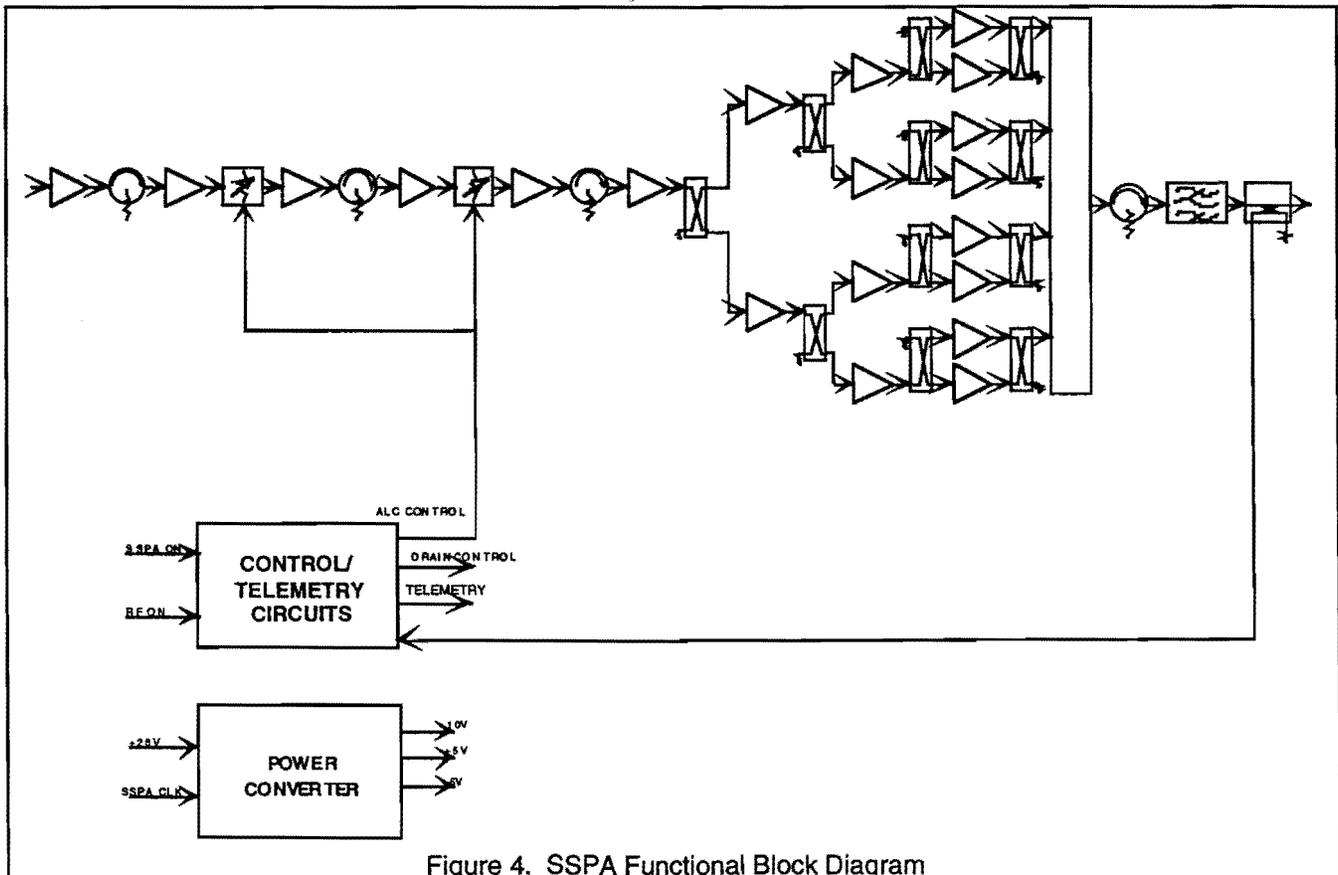

Figure 4. SSPA Functional Block Diagram

circuit provides analog telemetry on input current, secondary voltages, and temperature.

RF Unit Design

The RF Unit (RFU) consists of the hardware required to generate and receive the chirped signal waveform. It consists of three fully redundant assemblies. As depicted in figure 5, each assembly is housed in a light weight, aluminum slice. The RFU slices include the following:

> Digital Chirp Generator (DCG)
> UpConverter/Frequency Multiplier (UCFM)
> Receiver

The DCG uses a Direct Digital Synthesizer (DDS) design to generate a pulsed linear FM chirp at 12.72 GHz. The DCG provides the chirp signal to the UCFM for transmission. Later, as determined by the on-board tracker, the DCG generates an identical chirp and sends it to the Receiver; where it is used for pulse bandwidth compression.

The UCFM upconverts the DCG chirp to 13.495 GHz, and sends it to the SSPA for amplification and transmission. In addition, the UCFM generates the local oscillator (LO) signals and clock used by the altimeter sub-system. The Receiver, DCG and UCFM use the UCFM generated 775 MHz signal as the LO signal for frequency conversion. The DCG uses the UCFM generated 160 MHz signal to clock the DDS. The Digital Unit also uses the 160 MHz clock.

The Receiver amplifies and compresses the Ku-band return chirp. The Receiver mixes the return chirp with the DCG chirp signal to affect bandwidth compression. After compression, the Receiver performs gain control, and downconverts the IF chirp into in-phase (I) and quadrature-phase (Q) signals. These are sent to the Digital Unit for further processing.

Figure 6 shows the altimeter frequency plan for the 320 MHz bandwidth chirp. The DCG DDS generates a linear FM chirp, sweeping from 20 to 60 MHz in 102.4 μsec, which is upconverted to a 1570 to 1610 MHz chirp. The upconversion LO is a 775 MHz
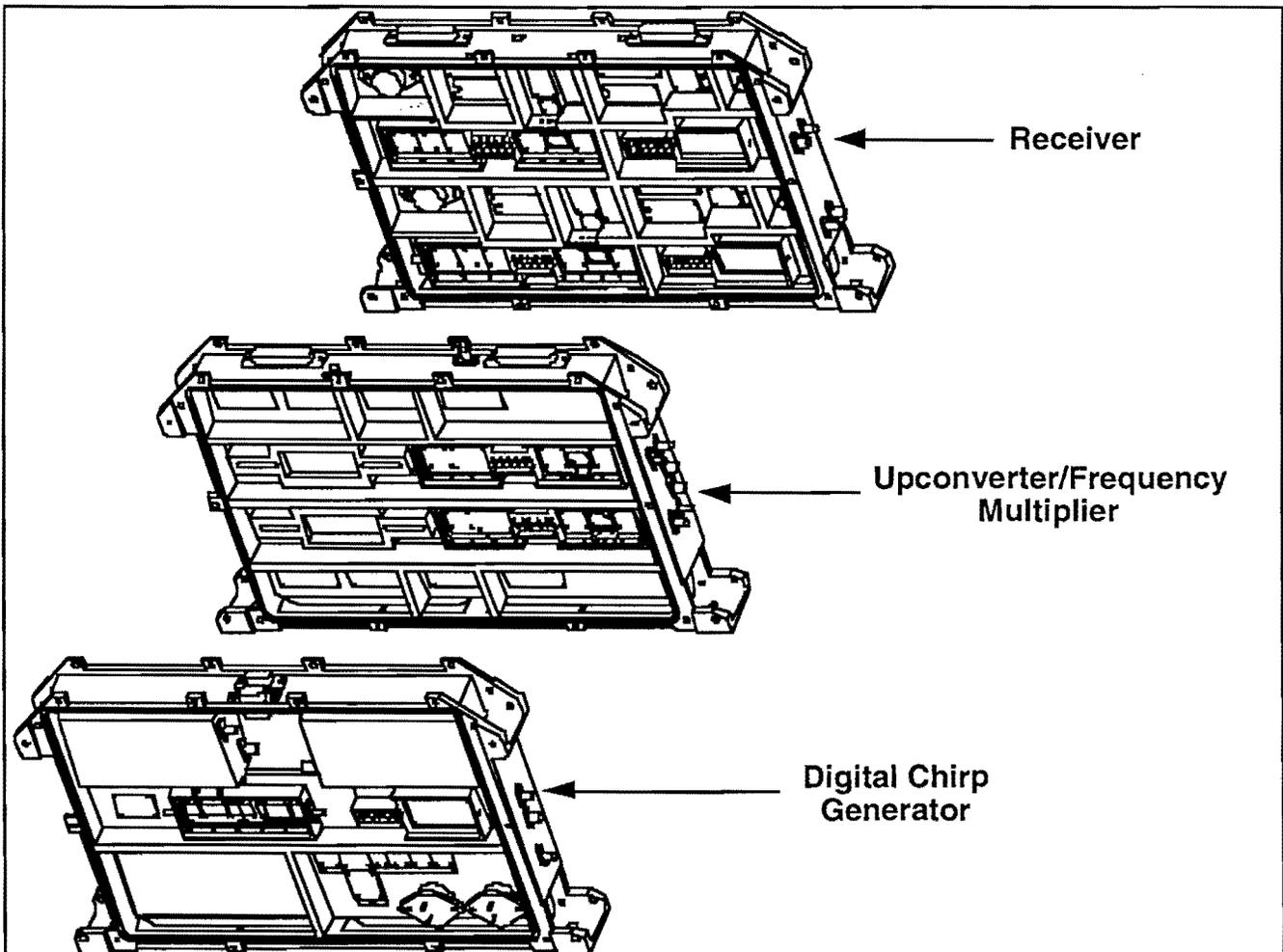

Figure 5. The RF Unit consists of three 9 x 13 x 1.7 inch slices; each containing a prime and redundant circuit.

signal, from the UCFM, that is multiplied by two. The 1570 to 1610 MHz chirp, is multiplied by 8 to a 12.560 to 12.880 GHz chirp, that is sent to both the UCFM and Receiver. The UCFM translates the signal to a 13.335 to 13.355 GHz chirp, using a 775 MHz LO signal, and then sends it to the SSPA for amplification and transmission. The 13.335 to 13.355 GHz return chirp signal is downconverted and compressed in the Receiver using the DCG 12.560 to 12.880 GHz chirp signal. The resulting 775 MHz IF signal is fed to an I/Q demodulator where it is converted to I and Q video signals using the 775 MHz LO signal from the UCFM.

Digital Chirp Generator (DCG)

The redundant Digital Chirp Generator (DCG) produces the linear FM chirp waveform. Depending on the altimeter state, the chirp bandwidth is either 5 MHz or 320 MHz. Low resolution acquisition uses the 5 MHz waveform, while high resolution acquisition and range tracking use the 320 MHz waveform. Figure 7 depicts the DCG functional block diagram.
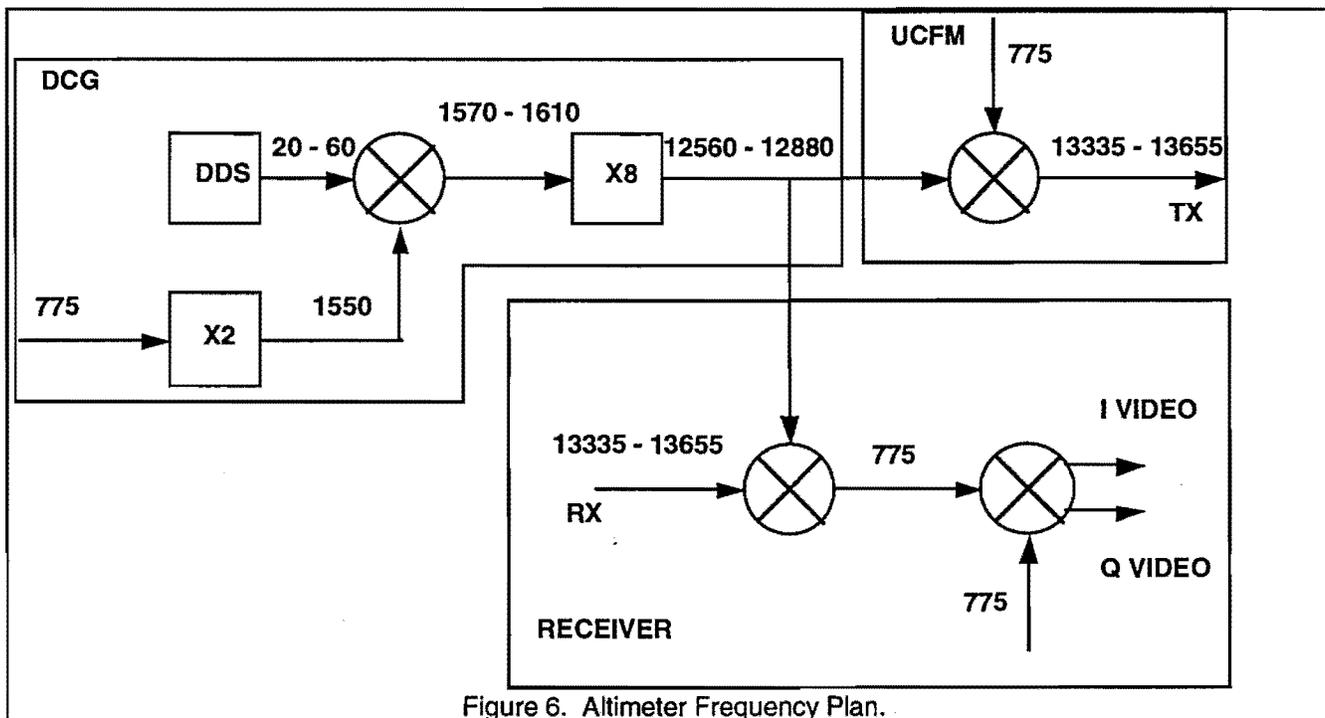

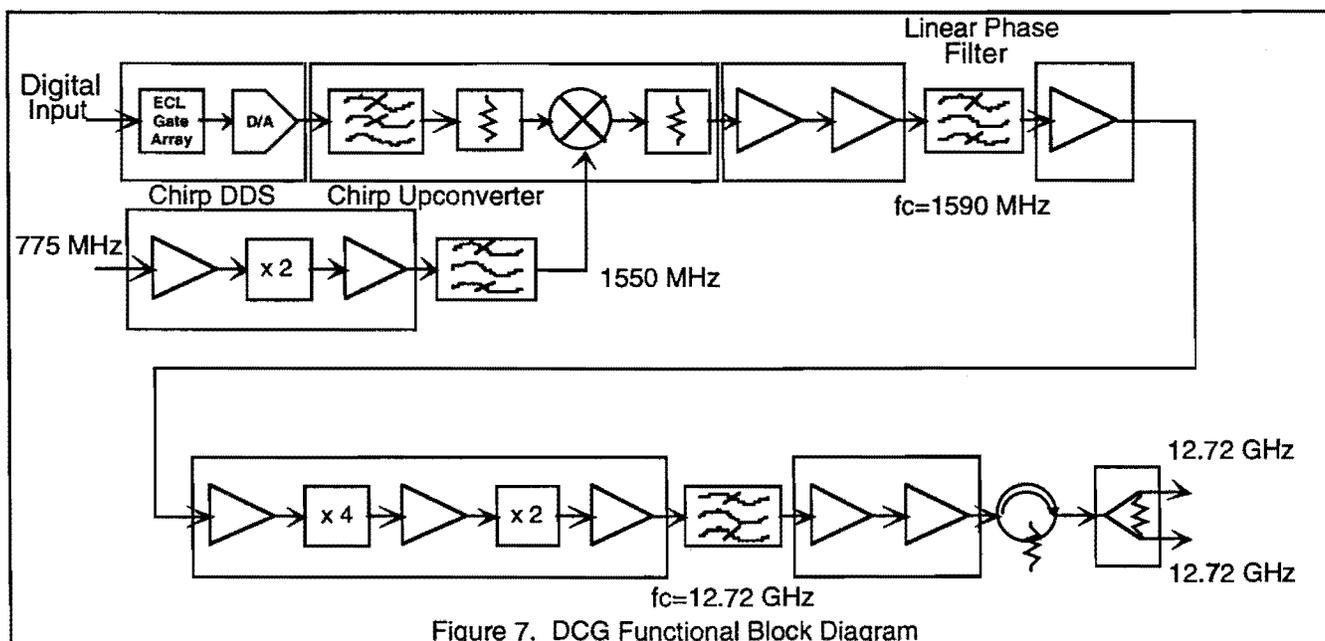Figure 6. Altimeter Frequency Plan.

Figure 7. DCG Functional Block Diagram

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A Direct Digital Synthesizer (DDS) design produces the chirp waveform. The DDS is a custom ECL gate array design clocked at 160 MHz. The DDS chirp output mixes with a 1550 MHz LO, and is then multiplied by a factor of eight to provide a chirp signal centered at 12.72 GHz; with either a 5 MHz or 320 MHz bandwidth. The 12.72 GHz signal is sent to both the UCFM and Receiver slices.

The DCG slice has a mass of 2.3 Kg, and an average power consumption of 9.9 watts.

UpConverter/Frequency Multiplier (UCFM)

Figure 8 depicts the UCFM functional block diagram. The UCFM upconverts the DCG's 12.72 GHz chirp signal to a chirp signal centered at 13.495 GHz. The UCFM then provides the 13.495 GHz chirp signal to the SSPA. The UCFM also generates a 775 MHz LO for the DCG and Receiver, and generates the 160 MHz clock used by the DDS.

The 775 MHz LO signal is derived from a phase-locked oscillator (PLO) with an output of 155 MHz. The PLO is locked to the 5 MHz spacecraft reference oscillator. A X5 multiplier, using an active multiplier circuit, multiplies the 155 MHz PLO output to produce the 775 MHz LO signal. A X32 multiplier multiplies the 5 MHz reference to generate the 160 MHz clock signal.

The UCFM houses both prime and redundant circuits. Switching between prime and redundant circuits is done by passive cross straps

The UCFM slice has a mass of 2.3 Kg, and an average power consumption of 5.2 watts.

Receiver

The receiver assembly compresses, downconverts, and processes the return waveform. The Receiver slice has a mass of 2.7 Kg, and an average power consumption of 5.6 watts. The receiver outputs I and Q video signals, which are processed by the Digital Unit. Figure 9 shows a functional block diagram of the receiver. A low noise amplifier (LNA), an automatic gain control (AGC) circuit, and an I/Q demodulator makes up the receiver.

The fully redundant receiver slice consists of two independent receivers. The receiver amplifies, filters, and then compresses, using the Digital Chirp Generator 12.72 GHz chirp signal as the 1st LO, the 13.495 GHz return signal. The resulting 775 MHz IF signal undergoes filtering, amplification and routing through the AGC circuitry. The AGC circuit provides a total of 63 dB of gain attenuation in 1 dB steps. The I/Q demodulator downconverts the 775 MHz IF into two equal-amplitude, phase-quadrature signals.
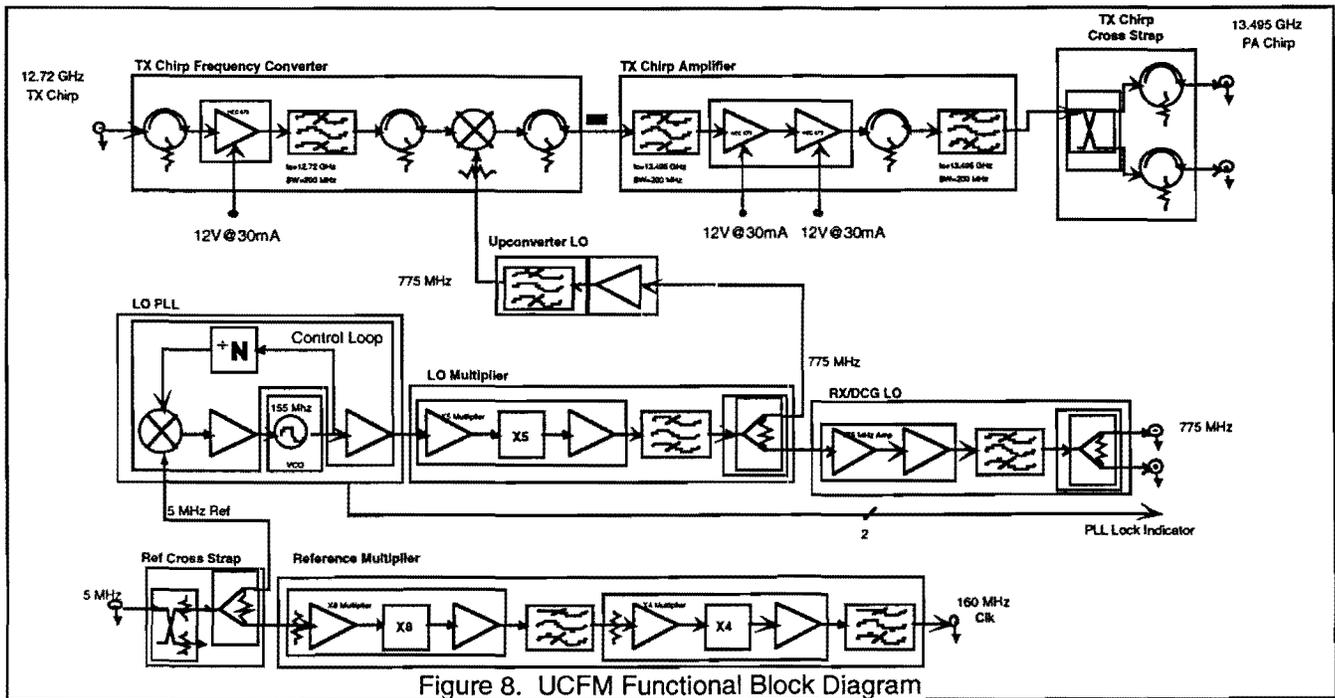

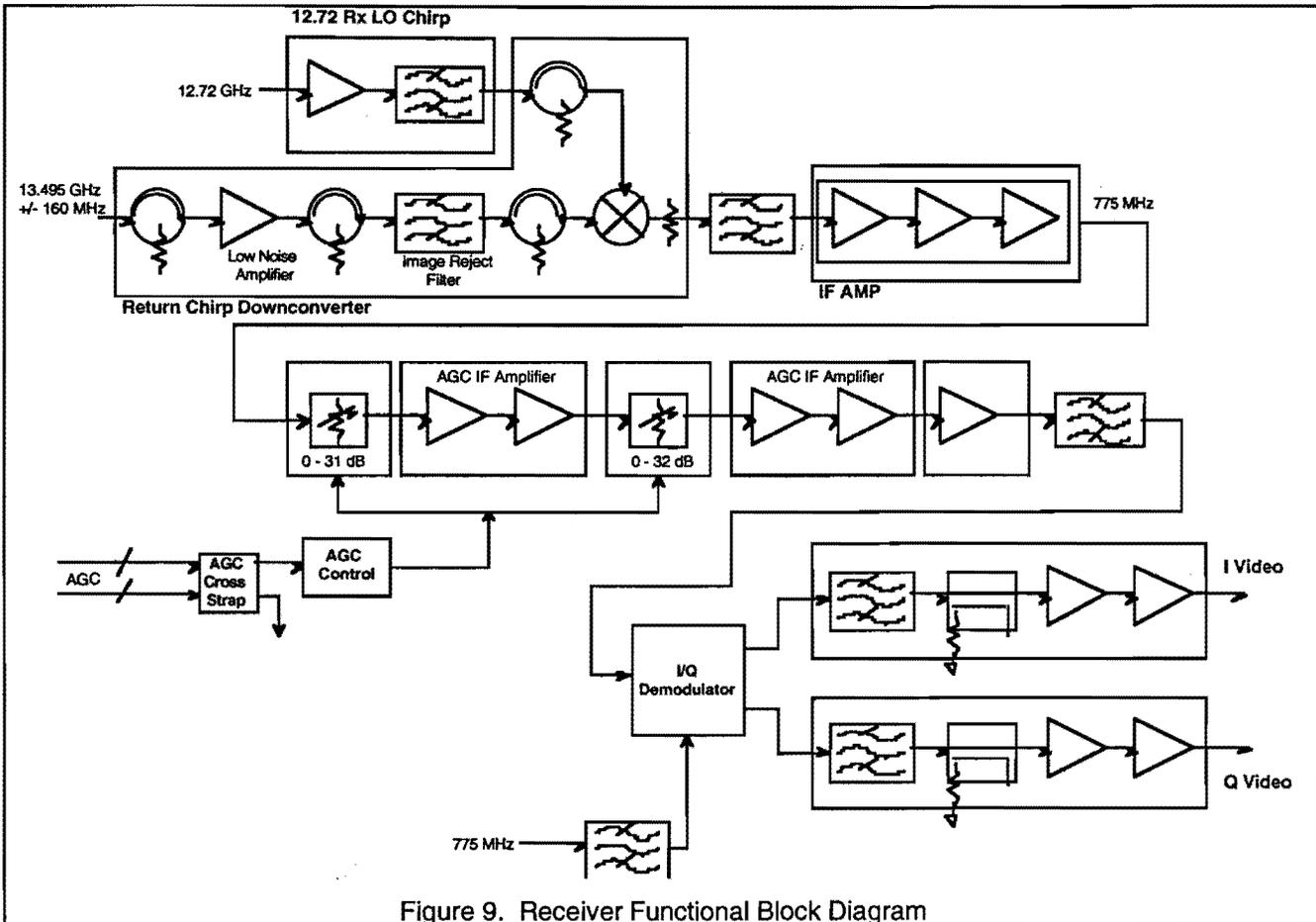Figure 8. UCFM Functional Block Diagram

Figure 9. Receiver Functional Block Diagram

Digital Unit Design

The Digital Unit (DU) is a highly integrated, space qualifiable hardware unit that performs the altimeter signal processing functions. Low power, radiation tolerant, surface mount, CMOS devices implement the design wherever possible. To ensure low component stress and mission longevity, part selection criterion uses conservative power and speed deratings. The DU design uses surface mount components, large gate array logic devices, and powerful microprocessors to conserve circuit board space.

Three slices comprise the DU. A slice is a mechanical shell that houses a prime and redundant circuit. Interfaces between units are through connectors on top of the slice, and inter-slice connections are on the side. The three Digital Unit slices are the Digital Filter Bank (DFB), the Synchronizer /Adaptive Tracker/Interface (SATI), and the Power Converter (PC).

Figure 10 depicts the altimeter signal processing flow. The DU signal processing function starts with in-phase and quadrature-phase video signals from the Receiver. Each signal is cross strapped, filtered, amplified, and converted to a sequence of 256, 8-bit digital complex samples. The

digital sequence undergoes a phase shift, and is then processed by a 256 point complex FFT. The frequency gates from the FFT are power detected through a magnitude square function. The DFB accumulates the power in the center 128 gates over 50 chirps. The 50 chirp average, which makes up the mean ocean return waveform data, is sent to the Adaptive Tracker processor. There it is processed by the range and AGC tracking software to generate tracking loop feedback. The telemetry data stream includes the waveform data.
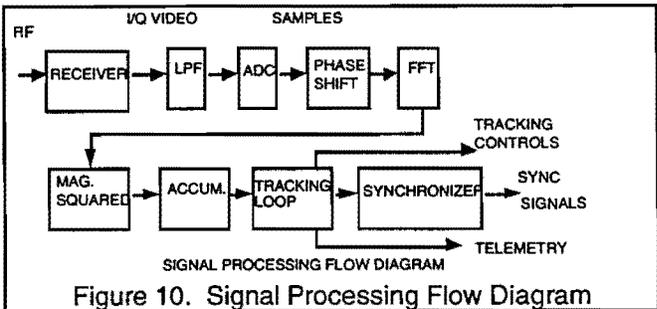

Figure 10. Signal Processing Flow Diagram

Along with the signal processing path, the DU also provides the Synchronization and digital Interface functions. The Synchronization function provides the radar pulse timing, along with the clocks and other control signals necessary for system operation. There

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are two types of interfaces, real time tracking and control. The synchronizer provides the real time tracking interfaces. The Interface function receives commands from the SC control function and configures the altimeter as commanded. This function also provides the telemetry back to the SC.

Digital Filter Bank (DFB)

Four printed circuit (PC) boards comprise the DFB slice. These are the four layer, Analog-to-Digital Converter (ADC) board, prime and redundant, and the ten layer, Fast Fourier Transform (FFT) board, prime and redundant. The DFB slice has a mass of 2.3 Kg and an average power consumption of 5.3 watts. The ADC card provides a passive cross strap for the incoming complex signal. The video input is buffered, and then passed through a lumped element lowpass filter. The I and Q filter paths are matched over the operational limits to within 5 degrees in phase and 0.3 dB in amplitude, from DC to 640 KHz, with a cutoff frequency of 1.25 MHz. The signal is AC coupled into a final amplifier that drives the A/D converter. The A/D converter is a CMOS, 8-bit, space qualified flash converter, which requires relatively low-power (400mW typical), and provides exceptional accuracy and very fast conversion times (sampling frequency = 20 MHz). The part is radiation hardened to a total dose of 330 KRAD. Due to design advances, this surface mount device provides accurate performance with the use of a single reference voltage. The ADC board takes 256 samples in 102.4 μsec, at a sample rate of 2.5 MHz, every 980 μsec.

Real and imaginary memory banks store the ADC samples on the FFT board. Surface mount SRAM (32Kx8) implements the FFT memory. This 40 nsec access time, low power, CMOS static RAM is latchup free, has a soft error rate of $<1 \times 10^{-10}$ upsets per bit-day, and has a total dose hardness of 1×10^6 RAD. Along with the SRAM, a surface mount,

CMOS ROM (8Kx8) is used. This device has a similar radiation performance, and an access time of 45 nsec. A space qualified FFT Processor chip performs the FFT processing. This CMOS, 68-pin device is latchup free, and preliminary SEU analysis predicts less than 5 upsets per day. The DFB design recovers from an upset within one chirp time, which translates into an FFT error rate of 5.7 x 10^{-8} FFT errors per day. Before computing a 256 point complex FFT, the FFT processor performs a fine timing adjustment by multiplying the sampled data with a ROM based complex sinusoid. After the complex FFT, a magnitude squared function is performed on the frequency domain data. The 20 MHz FFT processor clocks at 10 MHz, completing the previous functions in 330 μsec. A 172-pin, CMOS FPGA implements the FFT processor control and glue logic, as well as the 50 chirp accumulation. The radiation tolerant FPGA has 8000 equivalent gates (about 200 TTL packages), and clocks up to 48 MHz. The FFT board design clocks it at only 10 MHz. Figure 11 depicts the FFT board layout.

Synchronizer/Adaptive Tracker/Interface (SATI)

The SATI slice has ten layer, prime and redundant PC boards. The SATI slice has a mass of 2.3 Kg, and an average power consumption of 10.1 watts.

A 68-pin, SOS, 1750A processor, with on board floating point capability, implements the Adaptive Tracker function. The SOS design provides latch up free operation with excellent SEU performance. The processor uses a 64Kx16 memory bank, and an FPGA implements the processor glue logic. The Adaptive Tracker processor, which is the key element of the altimeter range and AGC tracking loops, computes and sends feedback to various interfaces. It also computes and formats the science
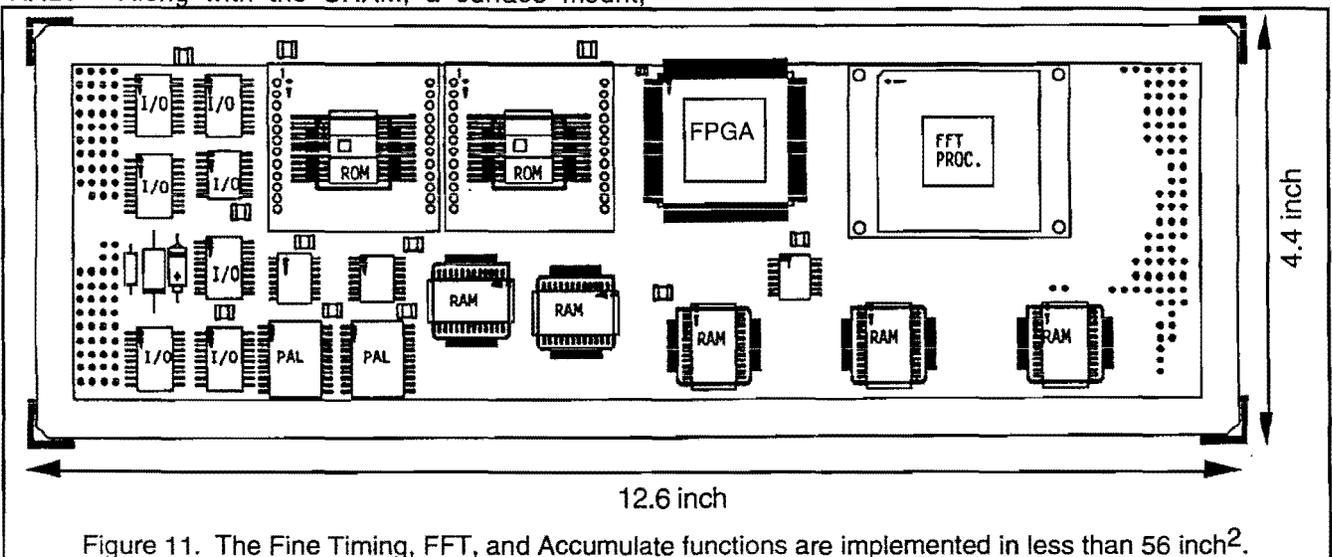

Figure 11. The Fine Timing, FFT, and Accumulate functions are implemented in less than 56 inch^2.

data telemetry, and decodes and processes' commands from the spacecraft. External interfaces are mostly RS-422 with AC coupled termination. To conserve power, the interfaces are active only during data transfers.

An ECL custom gate array (196-pin, 160 MHz) and a low speed FPGA implements the Synchronizer function. The ECL gate array provides the radar transmit timing pulse and clock necessary to drive the direct digital synthesizer (DDS), housed in the Digital Chirp Generator (DCG). A similar timing pulse and clock are generated at receive time, with the timing determined by the Adaptive Tracker software. The coarse timing adjustment is made with a resolution of 12.5 nsec. The Synchronizer provides control for the T/R switch, SSPA, telemetry function, and the WVR. A single ECL gate array implements the Synchronizer, and portions of the DDS function. The ECL gate array portion of the DDS function consists of a dual integrator, and sine lookup table. The DDS produces a 102.4 μsec, Linear FM chirp pulse, with either a bandwidth of 40 MHz or 625 KHz. The DDS sine output is updated at the 160 MHz clock rate. Figure 12 depicts the SATI board layout.

Power Converter(PC)

The PC slice, consisting of prime and redundant printed circuit boards, provides secondary DC power to the altimeter and WVR. The PC slice has a mass of 2.7 Kg and an average power consumption of 17.8 watts. The PC provides high efficiency by using a high frequency, switched-mode power supply (SMPS) design. The SMPS design uses a radiation tolerant power MOSFET. This device exhibits minimal characteristic changes to gamma, and gamma dot exposure. It has very fast switching speeds and low switching losses due to low on resistance. The PC design achieves high reliability by using conservative component derating for low component stress, controlled turn on and turn off, and good thermal management for low junction temperatures. Finally, the PC design uses flex circuitry and multi-layer ceramic capacitors, offering small size and ultra low equivalent series resistance and equivalent series inductance, to minimize size and weight.
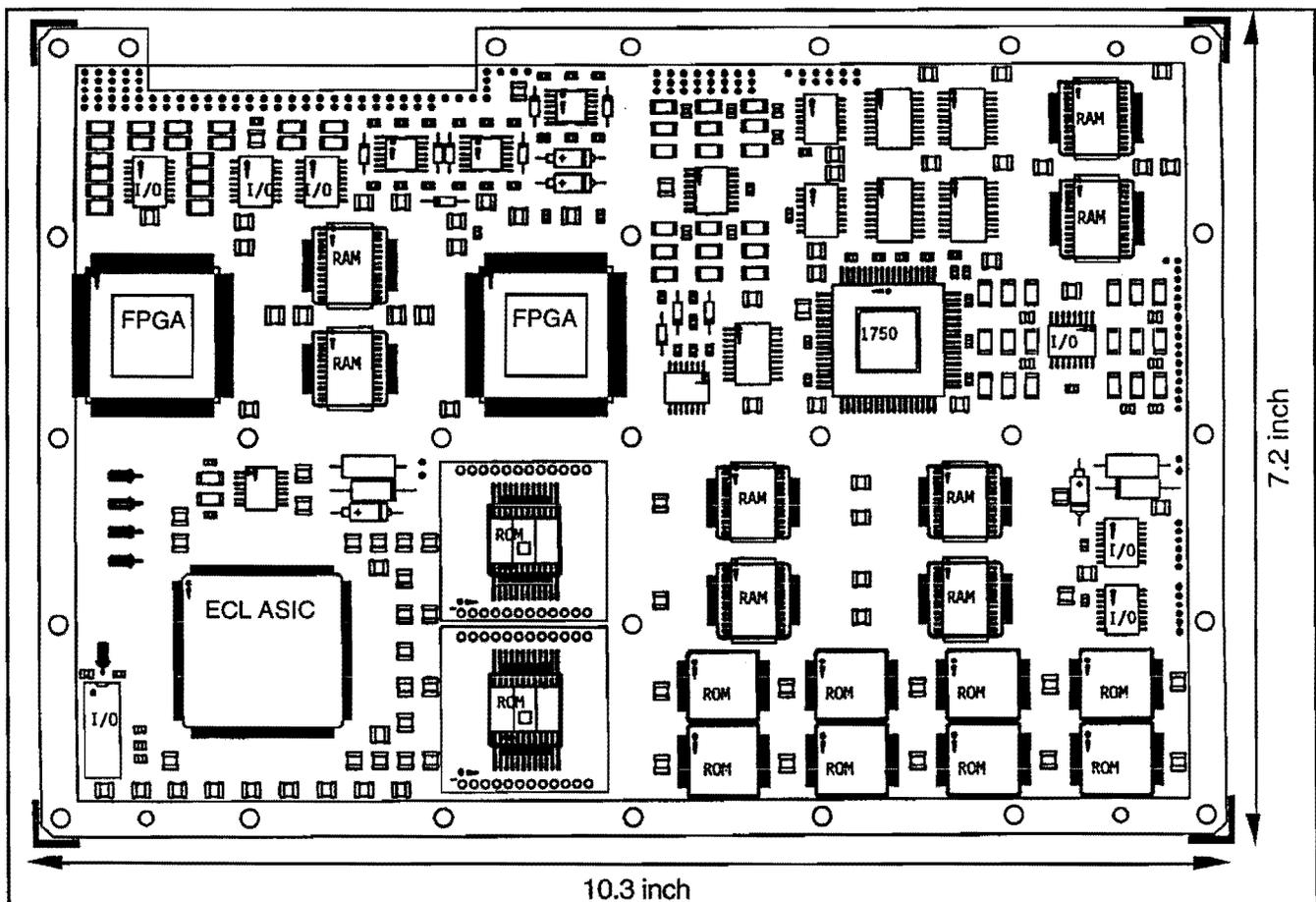

Figure 12. The Synchronizer, Adaptive Tracker, and Interface functions are implemented in less than 75 inch^2.

Looking Ahead - A Dual Frequency Altimeter

The altimeter range measurement is subject to various errors. These errors require correction to achieve the requisite accuracy for basin-scale and mesoscale circulation measurements. A major challenge will be the free electron ionospheric correction.

Free electrons in the ionosphere decrease the velocity of the radar pulse, thus causing the altimeter to overestimate its height. Typically, the electron content varies by an order of magnitude depending on: whether it's night or day, season of the year, and sunspot activity. This results in a 2 to 20 cm range error at 13 GHz. Basin-scale measurements require correction to ~2 cm[6]. As demonstrated on the TOPEX program, a dual-frequency altimeter appears to provide a near optimum solution.

The ionospheric correction is not without its price. Increases in height measurement noise, instrument mass, and power consumption accompany the dual-frequency altimeter solution. The mass and power reduction technologies used on GFO mitigates the latter. The former occurs from the combining of the C-band and Ku-band height measurements, and can be mitigated by increasing the number of independent waveforms available for averaging, i.e., decreasing the pulse repetition interval (PRI). Several PRI options, along with their associated impacts on existing design, size, weight, power, and height measurement noise were examined. A Ku-band PRI of 735 μsec (~1360 Hz PRF) and a C-band PRI on 1470 μsec (~680 Hz PRF) represents a near optimum solution. This combination maximized the use of unmodified GFO Ku-band hardware, and provided a predicted height measurement noise of 3 cm and 2 cm (at low waveheights) for the C and Ku bands, respectively. The predicted combined height noise approaches 2 cm for low waveheights.

Figure 13 depicts a candidate dual-frequency altimeter. An independent channel approach allows a simplified transmit and receive timing structure, provides excellent inter-channel isolation, and eliminates the necessity of modifications to the already designed RF hardware.

The Ku-band operation was previously described, and the C-band operation is very similar. The C-band channel uses the same Digital Chirp Generator, Digital Filter Bank, and Receiver IF and AGC design as the GFO Ku channel. The C-band solid state power amplifier is the TOPEX C-band power amplifier. The design of the T/R Switch will be functionally equivalent to the Ku-band design, but at C-band frequencies. The 3 frequency feed antenna will require modification to add the C-band capability, but the reflector diameter will remain the same. The only new design will be the Down Converter/Frequency Multiplier.

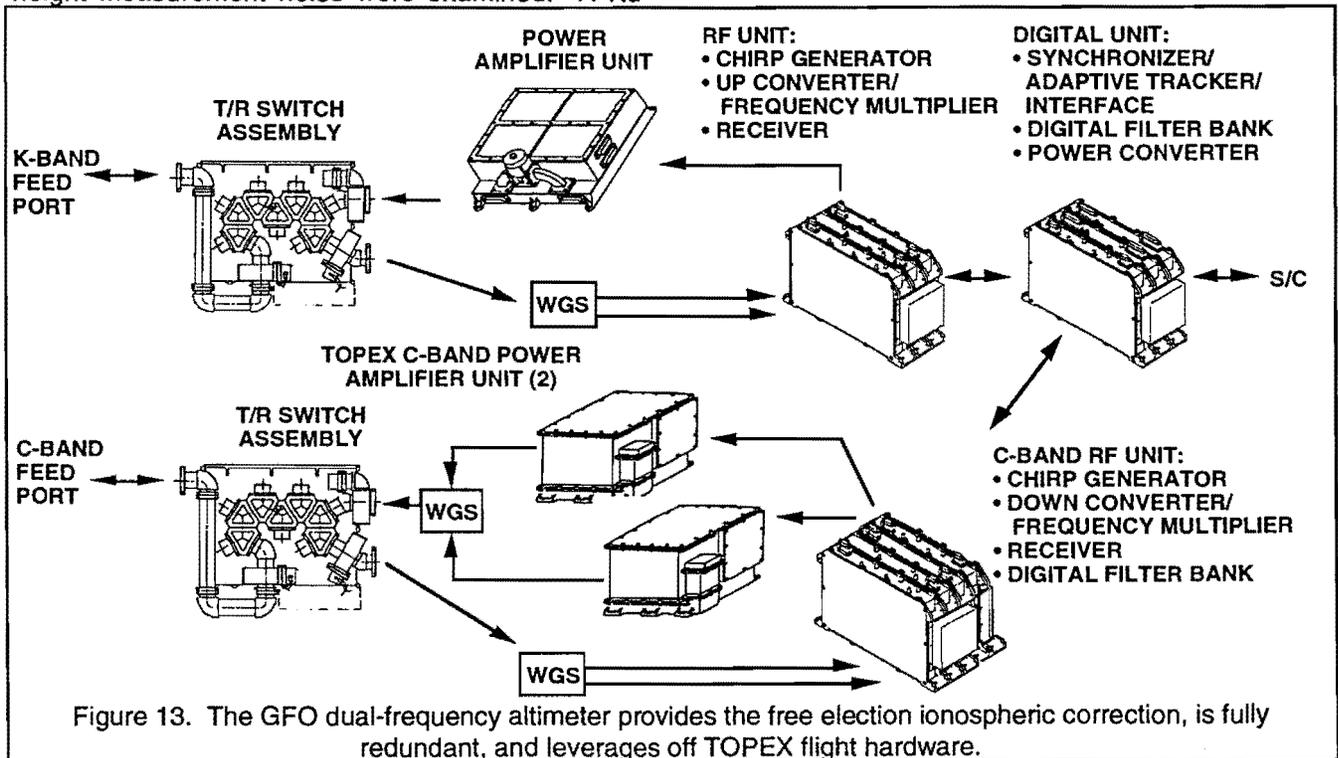The dual-frequency altimeter is estimated to weigh 107 pounds and consume 156 watts.

Figure 13. The GFO dual-frequency altimeter provides the free election ionospheric correction, is fully redundant, and leverages off TOPEX flight hardware.

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