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DESIGN OF THE U2 EXPERIMENT GROUND SUPPORT EQUIPMENT

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Small satellites and sensor payloads aboard larger spacecraft can
benefit from ground support equipment (GSE) which reduces the time
and cost of developing and flight qualifying space instruments. User-
friendly microcomputers and a comprehensive system design make
such GSE possible and, due to the availability of high speed process-
ors with real-time operating systems, even sophisticated instruments
can be accommodated. This was demonstrated by The Johns Hopkins
University/Applied Physics Laboratory (JHU/APL) during its work
with the U2 Experiment, part of the Strategic Defense Initiative
Office's Delta 181 Mission.

The U2 Experiment, an orbiting multi-sensor optical emissions
instrument, was designed, built, and tested by The JHU/APL. The
instrument required a high data rate and complex command capa-
bility. It also required a relatively short design-to-launch time of eight-
een months. GSE was built to facilitate the U2 Experiment's data
processing and instrument control subsystem development, sensor
subsystem integration, functional and environmental testing (both
independent of, and united with, the spacecraft intended to carry it
into orbit), and the U2 Experiment's flight data retrieval. Important
elements of a GSE system include:

1. Sensor stimulation and exact emulation of the experiment and
    spacecraft interfaces.

2. A compatible data acquisition and control unit.

3. A user-friendly, real-time computer system.

The GSE design for the U2 Experiment is described to show how it
satisfied these requirements.

INTRODUCTION

The Delta 180/181 Programs

The Space Department of The Johns Hopkins University/Applied Physics Laboratory
(JHU/APL) has been involved in two highly successful spacecraft missions for the Strategic
Defense Initiative Office (SDIO) during the three year period ending in February 1988. The
Delta 180 and Delta 181 missions have demonstrated concepts and provided data crucial
to the design of SDIO's planned space-based defense system. Each spacecraft contained a
sensor module of instruments designed to track and/or provide signature data for test objects
deployed from both the spacecraft and the ground. One instrument from each sensor module
was required to monitor the visible and ultraviolet emissions of these objects. APL built
the U1 Experiment for Delta 180, and the U2 Experiment for Delta 181, to perform these
functions.

The U1/U2 Experiments

The U1 and U2 Experiments each consisted of three main sections; the sensors, power conditioning, and instrument control and data processing system. The U1 and U2 sensing systems each included two imagers and four spectrometers while the U1 system had an additional four photometers. Power conditioning was accomplished with DC/DC converters. The Data, Control, and Interface System (DCIS) performed the central instrument control and data processing. The hardware and software development for the DCIS required test equipment capable of simulating the power, sensor, and spacecraft interfaces, and controlling, acquiring, reducing, and displaying the data processed by the DCIS. This ground support equipment (GSE) was designed to satisfy not only the DCIS requirements, but also those for the integration, environmental testing, and post-launch data retrieval for the entire instrument.

The U1/U2 GSE

The U1 GSE required only one desktop computer, reflecting relatively simple spacecraft and instrument interfaces and a data rate of only 16 kilobits per second (kbps). The U2 GSE, however, evolved to its present four computers due to three enhancements in the U2 Experiment; an increase in the U2 DCIS wideband data rate to 1056 kbps (in order to accommodate digital video), the addition of a narrowband downlink, and increased sophistication of the command and telemetry uplinks. Both GSE, however, utilized similar designs and also had to support ambitious 18 month instrument development schedules. Since the U2 GSE represents an increase in capability over the U1 GSE, and was actually built using hardware leftover from the Delta 180 program, the remainder of this paper will describe only the U2 GSE.

The U2 GSE Requirements

The U2 GSE required hardware and software which could support the following tasks, listed in chronological order:

1. Development of the DCIS hardware and software.

2. U2 Experiment integration and flight qualification.

3. Spacecraft level ground testing.

4. Mission data collection.

The GSE system had to be capable of acquiring and storing data collected from the instrument and its stimulus (such as test lamp light intensity). Prior to spacecraft integration, the data were collected directly from the instrument, requiring the GSE to employ a telemetry system simulator. After spacecraft integration the data were acquired from the spacecraft GSE.

The GSE system had to be able to display the command state of the instrument, including feedback status and housekeeping, and a summary of the sensor data in real time. It also had to be able to simultaneously display the video images and create any of several possible graphical outputs, especially line spectra. Hardcopy of any display screen had to be obtainable in near real time.

The test operator had to be able to use the computer keyboard to create a command state for the instrument (or the DCIS) by selecting control options from a menu displayed on the screen. The command state would then be converted, by the software, to the appropriate

set of digital words which would, through the use of digital actuators, control an interface simulator to exactly emulate the way the spacecraft would send the command. Any other spacecraft or experiment interfaces had to be simulated in the same manner, including those for telemetry uplink, power, and sensors. The interface simulator would be electronically indistinguishable from its flightworthy counterpart even to the extent that identical connectors, cables, and circuitry were used.

SYSTEM DESCRIPTION

The U2 Instrument

The main subsystems of the U2 Experiment perform sensing, instrument control and data processing, and power conditioning as depicted in Figure 1.
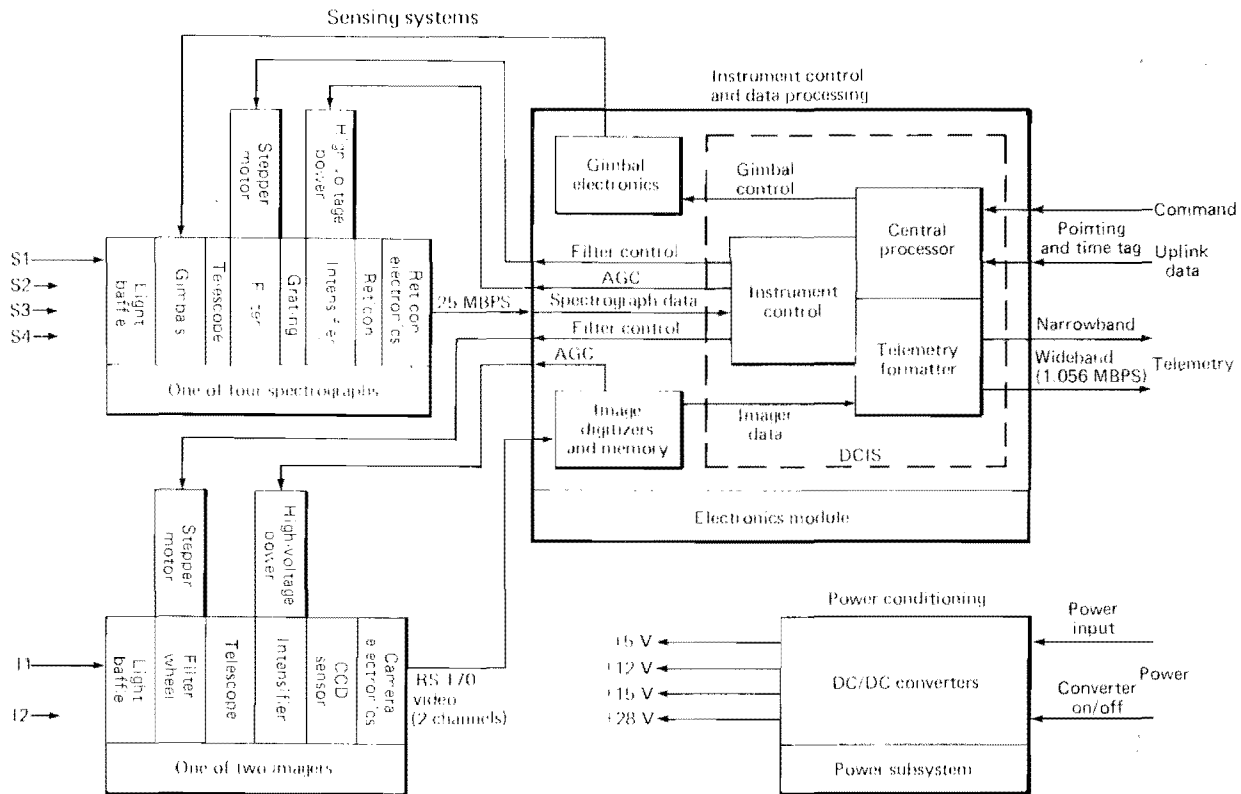

Fig. 1   Block diagram of the U2 experiment.

Each of the four spectrographs consists of a two-axis gimballed mirror assembly (which directs light through the baffles into the telescope), a four-position filter wheel, a diffraction grating, a gain-controllable intensifier, and a photodiode array (brand name Reticon) with digitizing electronics which produces 1.056 million six-bit words per second. Each of the two imagers is composed of a light baffle, a six-position filter wheel, a telescope, a gain-controllable intensifier, and a solid state camera containing a charge-coupled device (CCD) with electronics which produces RS-170 video output.

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The Electronics Module contains gimbal electronics for closed-loop control of the gimbal motors, image digitizing circuitry including automatic gain control (AGC) for the image intensifiers, and the DCIS. The three main parts of the DCIS perform instrument control, central processing, and telemetry formatting. The central processor accepts and executes spacecraft commands, performs a coordinate transformation on the pointing data to command the gimbals, and collects housekeeping and timetag data for integration into the telemetry stream. The instrument controller provides timing for the Reticon electronics, acquires the spectrograph data, and integrates it into smaller, manageable bins which it uses to automatically control the gain of the spectrograph intensifiers. The telemetry formatter combines video data from image digitizer memory, spectrograph data from the instrument controller, and housekeeping and status data from the central processor for downlink via the spacecraft wideband and narrowband telemetry.

The power subsystem consists of three DC/DC converters each with an unregulated 28 ±6 VDC input, a soft turn-on switch, and outputs which provide the regulated voltages shown in Figure 1.

The U2 GSE

An overview of the U2 Experiment GSE as it was used to support mission data collection and spacecraft ground test is shown in Figure 2. The spacecraft GSE receives the downlink wideband and narrowband data, distributing it to the U2 GSE, and to the GSE of the other six experimental payloads. The U2 GSE at this level consists of a data acquisition
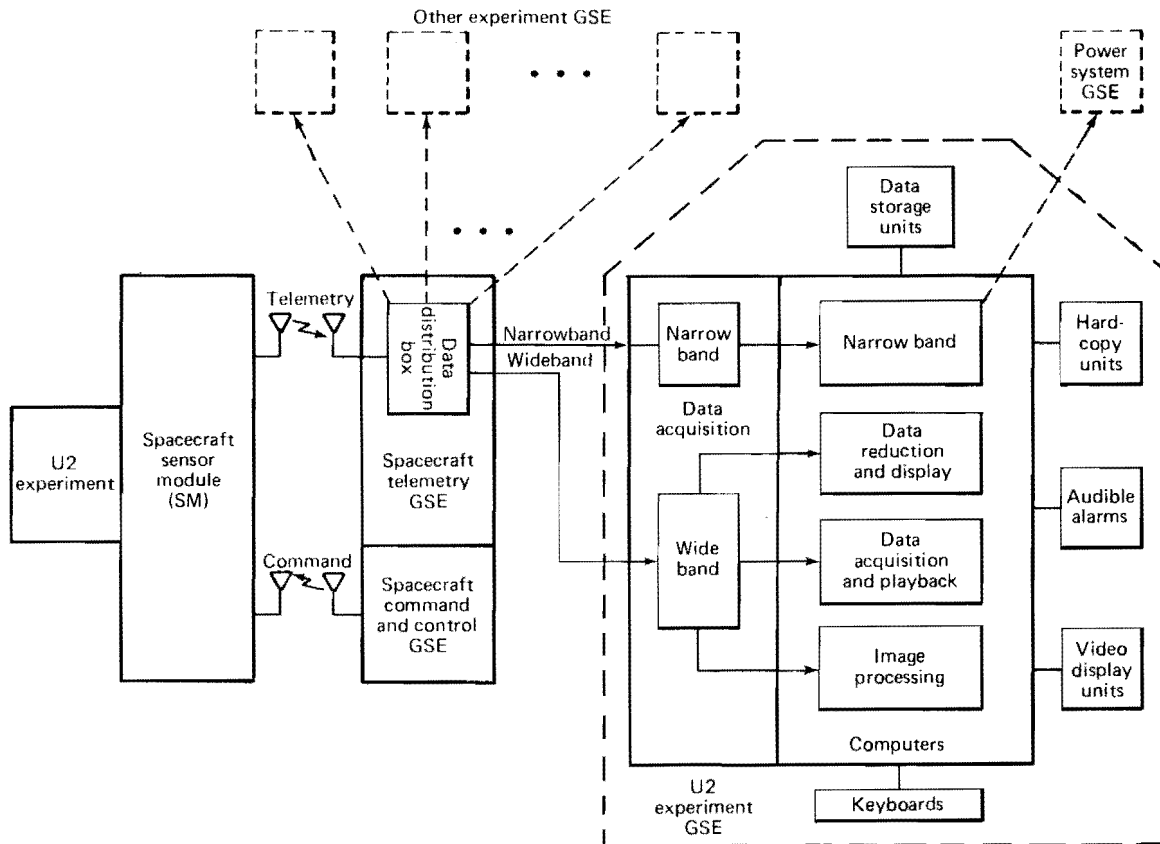

Fig. 2   Overview of U2 mission support.

section which performs frame synchronization, and a computer section. The computer section performs the basic tasks of data storage, display, and hardcopy, and has the special task of passing the spacecraft housekeeping data to the power system monitor computer.

For stand-alone testing of the U2 Experiment, the spacecraft sensor module with its associated command and control system is emulated by the U2 Experiment GSE as depicted in the simplified block diagram of Figure 3. Control is added to the data acquisition section at this level in order to exactly simulate the spacecraft uplink functions (pointing, command, and timetag) and the wideband and narrowband downlink interfaces. The computer section is implemented using four computers for: narrowband data reduction; wideband data reduction and control; data acquisition and playback; and image processing. Light sources simulating optical emissions expected to be encountered during the mission stimulate the U2 sensors during functional tests and can be used within the typical testing environments (thermal vacuum and vibration) required for U2 flight qualification.

Emulation of the DCIS interfaces allowed hardware and software verification to take place in parallel with sensor and power subsystem development. Figure 4, a block diagram of the test setup for the DCIS, shows the U2 GSE with a special test interface and a U2 simulator added. The DCIS was tested in this mode at both the breadboard and protoflight levels, and in each case the cardcage used to house the DCIS boards doubled as an Electronics Module simulator. The U2 simulator provided emulation of the four Reticon subsystems and the 48 temperature transducers and 32 analog voltages which reflected the health of the instrument. The image digitizer was simulated inside the Electronics Module, and gimbal control signals were monitored by the Data Acquisition and Control unit (DAC). The DCIS had a special test port for manually setting the spectrograph intensifier pulse width modulation. A special interface was developed for the test port which was used to check out the intensifier power supply interface and perform a cursory calibration of the spectrograph systems after they were integrated.

The computer workstation at the far left of Figure 5 was used for monitoring the narrowband downlink telemetry. The tall rack to its right housed the test lamp power supplies, data system and interface simulator cardcages, the system power supply, and the DAC. The computer workstation between the two racks was used for monitoring and recording the wideband downlink telemetry. Multiple displays provided fast updates and allowed simultaneous monitoring of text, graphics, and video. Menu driven software and automatic program startup eased system operations. Wheels underneath the racks and workstations minimized transport problems.

The following sections of this paper describe in detail the design of the three main parts of the U2 GSE, namely: the interface emulators; the data acquisition and control system; and the computer system.

INTERFACE EMULATORS

The Spacecraft Simulator

Figure 6 shows the interconnections between the U2 Experiment and the spacecraft, identifies each of the individual spacecraft interface simulators, and indicates where each simulator connects to the rest of the GSE.

The command simulator converts a 16-bit word strobed from the DAC into a 10 kbps digital stream which gates itself into the DCIS command port. The control computer activates the DAC in response to the test conductor's selection of a command via the keyboard. The
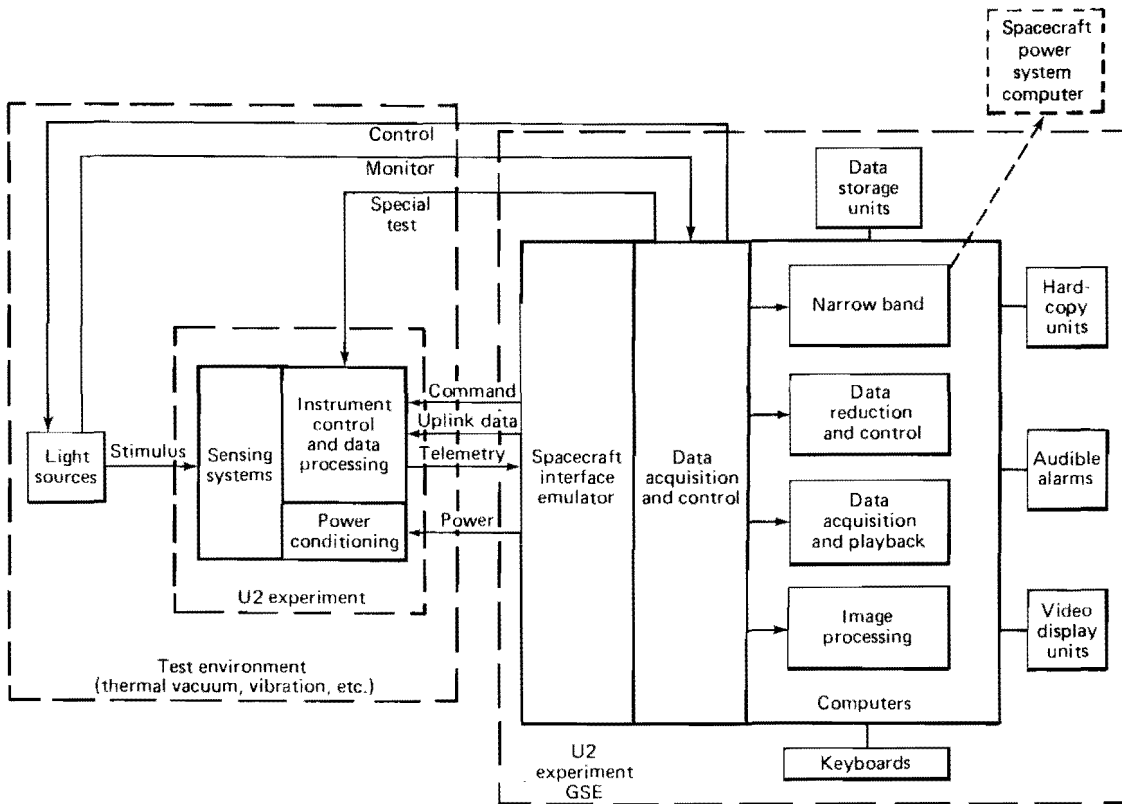
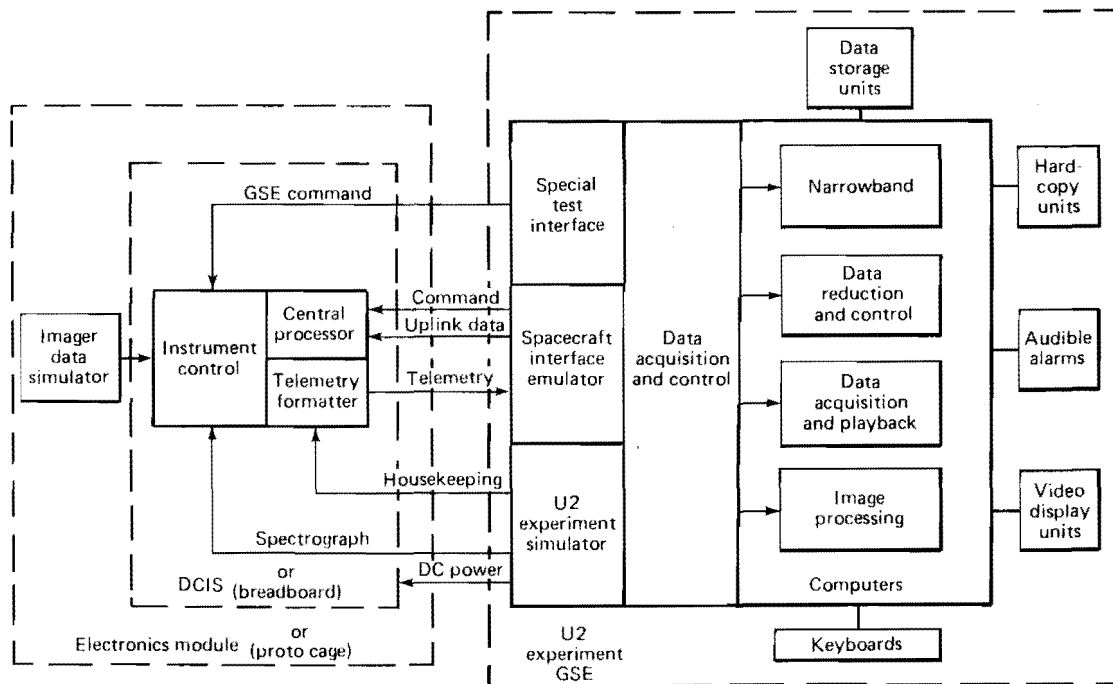**Fig. 3 Simplified block diagram of U2 experiment ground test.**

Fig. 4 Block diagram of data control and interface system (DCIS) test setup.

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Fig. 5   U2 GSE at Kennedy Space Center.

timetag simulator accumulates a 32-bit mission time count which is available to be periodically (every 49 milliseconds) clocked out by the DCIS at 33 kbps. The 125 microsecond resolution clock is free running, but can be reset to zero. The mapper simulator is driven by a 32 byte, 1200 baud RS-232 message which is sent by the control computer five times per second. The message simulates the output of the spacecraft's flight processor, which provides the U2 Experiment with the spacial coordinates of the test object under observation. Various patterns or trajectories can be created by the test conductor to simulate tracking. The simulator converts the message to RS-422 format and sends it to the DCIS central processor, which decodes the message and uses it to direct gimbal pointing and imager zoom field selection.

The U2 Experiment is allocated two bytes out of every narrowband minor frame to report its status. The narrowband telemetry simulator provides the gating and synchronization to clock those bytes from the DCIS output port and insert them into its simulated narrowband stream. The synchronization word and minor frame count are key elements of the simulator, which was used to debug and test the narrowband frame synchronizer. Since the U2 Experiment constructs all of its wideband data, the wideband telemetry simulator had to merely provide the 4.224 MHz and 1.056 MHz clocks to the DCIS, and accept the data that it returns.
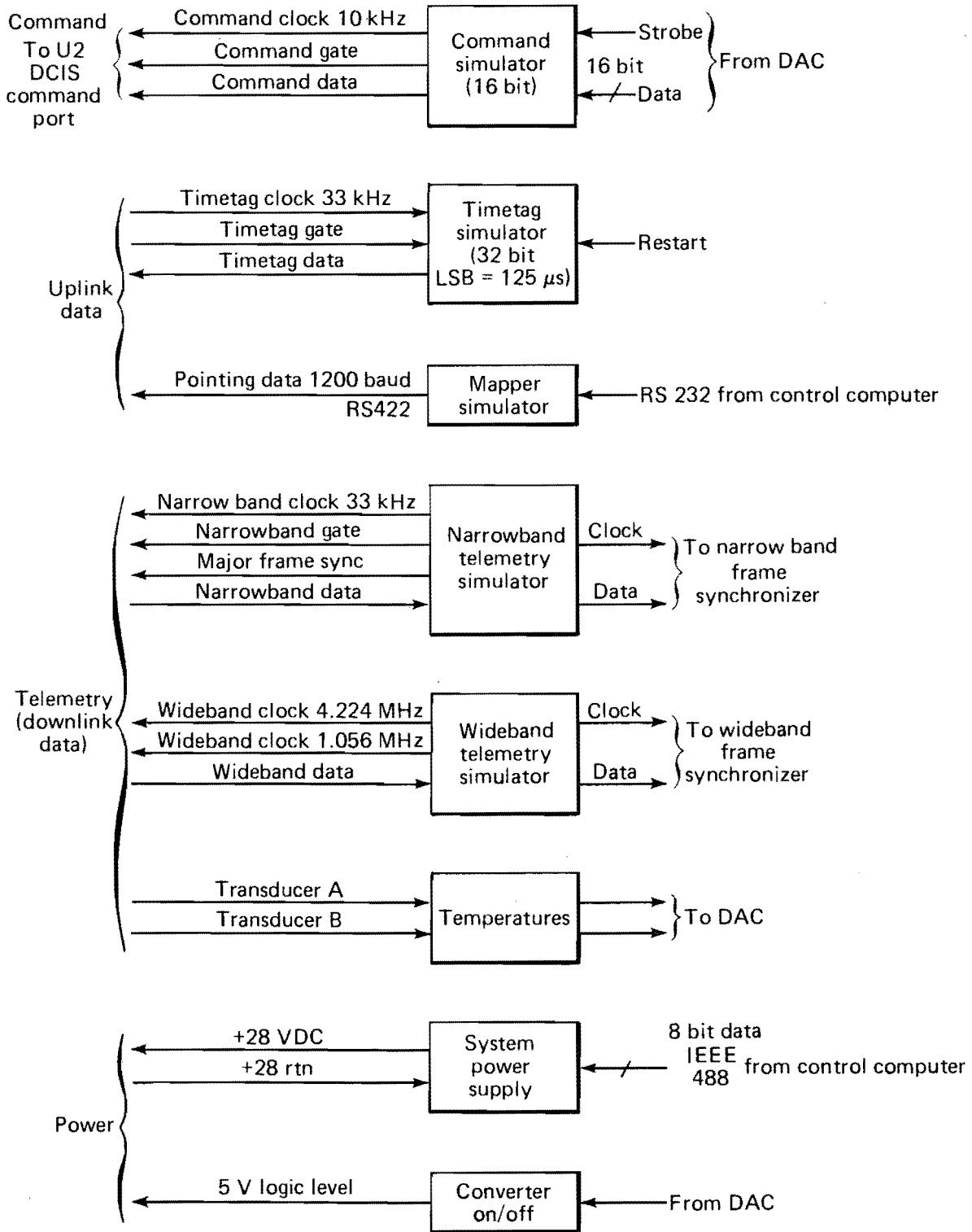
Command
To U2
DCIS
command
port

Command clock 10 kHz
Command gate
Command data

Command
simulator
(16 bit)

Strobe
16 bit
Data

From DAC

Uplink
data

Timetag clock 33 kHz
Timetag gate
Timetag data

Timetag
simulator
(32 bit
LSB = 125 μs)

Restart

Pointing data 1200 baud
RS422

Mapper
simulator

RS 232 from control computer

Telemetry
(downlink
data)

Narrow band clock 33 kHz
Narrowband gate
Major frame sync
Narrowband data

Narrowband
telemetry
simulator

Clock

Data

To narrow band
frame
synchronizer

Wideband clock 4.224 MHz
Wideband clock 1.056 MHz
Wideband data

Wideband
telemetry
simulator

Clock

Data

To wideband
frame
synchronizer

Transducer A
Transducer B

Temperatures

To DAC

Power

+28 VDC
+28 rtn

System
power
supply

8 bit data
IEEE
488 from control computer

5 V logic level

Converter
on/off

From DAC

Fig. 6   Block diagram of spacecraft interface emulator.

The spacecraft battery and power switching unit was simulated using a power supply programmed by the control computer. Voltage settings can be selected by the test operator at the command console and the voltage and current readings measured by the supply are returned to the computer and displayed on the screen. The power supply has both hard and soft programmable overvoltage and overcurrent limits and displays its status and power settings on the front panel. The DC/DC converters can also be commanded on and off via the control computer keyboard and through a buffered logic level output from the DAC.

The Optical Emissions Simulator

Simulation of light emissions was done with the test lamp units blocked out in Figure 7. The spectrograph test sources consisted of collimating optics which fit against the light baffles, a mercury vapor lamp, and a photodiode detector which was used to measure the relative brightness of the lamp in order to normalize fluctuations with temperature. Light entered the optics from a small pinhole in the casing around the lamp. A larger hole on the opposite side of the lamp allowed light to fall on the monitor. Identification of the spectral lines associated with mercury ensured that the system was operating properly. The imager test lamps were similarly configured except for the addition of a condenser lens, diffuser, and an Air Force test target in between the lamp and the collimating optics. The focus of the imager and its basic operation could be verified by observing the test pattern on the video display monitor.
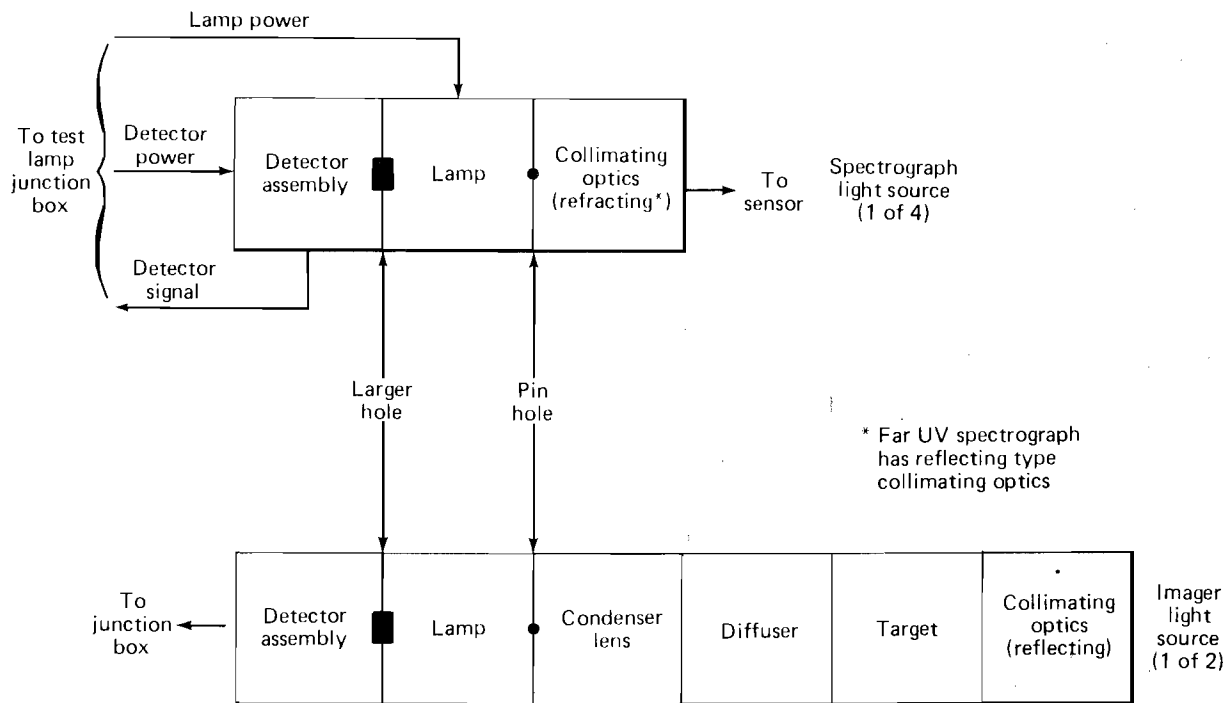

Fig. 7   Block diagram of light sources.

The Instrument Simulator

Interfaces internal to the experiment were simulated for the DCIS as shown in Figure 8. The DCIS clocks the data from the four Reticon simulators which can produce either constant values, or a staircase function, as selected by the test operator. The AGC output of the DCIS can then be verified by observing the pulse width modulation pattern which would be sent to the intensifier power supply. The imager digitizer memory is also simulated by simply shorting the DCIS address lines back onto its data bus in such a way as to produce a test pattern which easily verifies proper telemetry formatting. DCIS digital to analog (D/A) outputs to the gimbals are monitored by the DAC in order to verify that the software responds properly to different pointing coordinates. Each of the 48 temperature and 32 analog voltage telemetry channels are calibrated with the housekeeping simulator which uses the DAC's D/A outputs to allow the test operator to simulate different voltages and temperatures and then verify the DCIS' correct measurement in the telemetry stream. Finally, a multiple output power supply, protected from transients, overvoltage, and overcurrent, simulated the DC/DC converters for the DCIS.

Other important simulators are the breadboard and protoflight versions of the DCIS. Both of the cardcages used to house the DCIS boards were built to emulate the Electronics Module, and so the same set of GSE cables worked with all three DCIS systems, and preliminary sensor integration tests could be made with the protoflight cage before the Electronics Module wiring was complete. In addition, the DCIS protoflight boards fit into the Electronics Module and were used to debug its wiring harness and the experiment harness without endangering flight electronics. The protoflight boards were also used to allow sensor integration to proceed in the Electronics Module while the flight boards were being debugged in the protocage. Many convenient integration configurations were allowable by mixing the flight systems and fully compatible simulators.
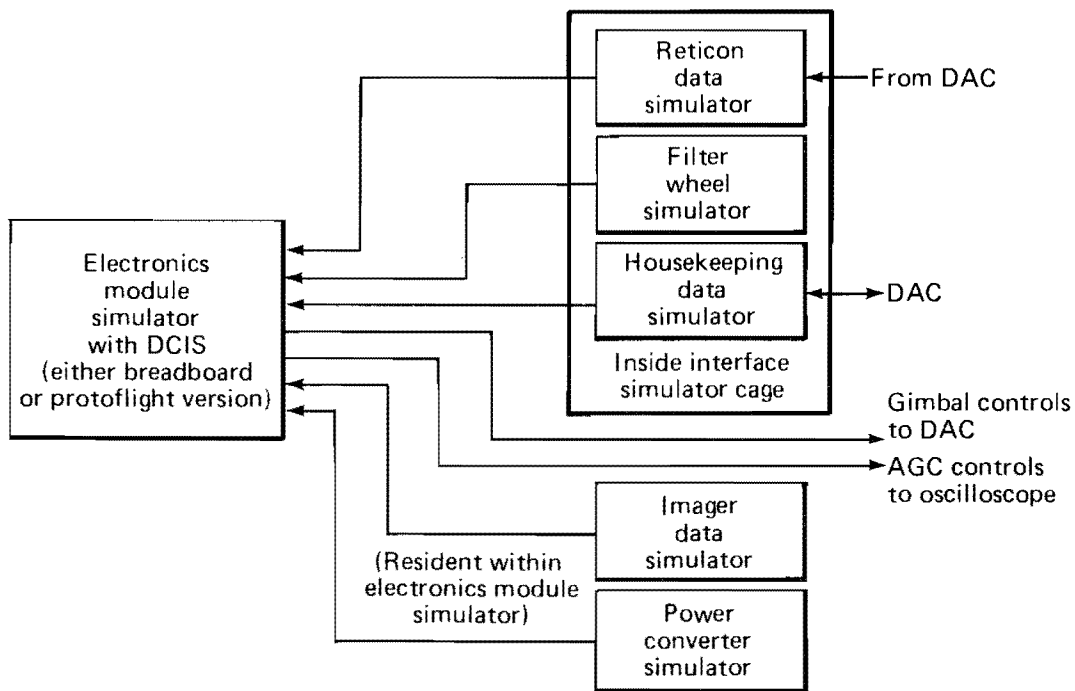

Fig. 8   Block diagram of U2 experiment simulator for DCIS testing.

The Simulator Hardware

With the exception of the system power supply, all of the interface simulators were fabricated on Augat wirewrap boards using a semiautomatic wirewrap machine. The machine was programmed by a net list extracted from hand drawn schematics and could complete the wiring of a full board in about three hours. These boards were housed in the Augat cardcage, the backplane of which was wired to a connector plate on the back of the cage. Every connection on the Electronics Module has a GSE cable associated with it which is built to the same specifications as the flight harness. Three of those cables simulate the spacecraft harness and the rest simulate the experiment harness. Additional connectors on the plate are used to input control signals from the DAC and control computer, and to output data to the Data System cage which houses the frame synchronizers and computer interfaces.

DATA ACQUISITION AND CONTROL

The data acquisition and control section of the U2 GSE provides the connection between the interface emulator and computer sections as shown in Figure 9. The test lamps are an exception due to the requirement that they must operate separately from the computer; for example during launch vehicle mating, spin tests, or final launch preparations on the pad. The lamps are individually turned on by a row of switches on the front panel of the chassis which contains the power supply for the lamps.

A standard component in this section is the Hewlett Packard 3852 DAC unit, which can be configured for many applications because of its variety of modular analog and digital input/output (I/O) cards. The DAC maintains exact control of each interface emulator through its transistor-transistor-logic (TTL) compatible (discrete logic level) and 12-bit D/A outputs. The DAC uses its TTL compatible inputs to monitor instrument and GSE telltales in order to verify the proper response to its commands. A relay multiplexer feeds an integrating digital voltmeter which monitors the health of the instrument (temperatures and voltages) as well as any analog test points in either the instrument or the GSE. While all the GSE command and housekeeping data is acquired through the DAC, there is no means for the DAC to receive the complex high speed wideband or narrowband telemetry or to perform the necessary synchronization or formatting which is required for the computer to be able to perform real-time telemetry decommutation and data reduction. The frame synchronizers and computer interfaces are customized components of the data acquisition section which perform these functions. In addition, the playback interface allows wideband data to be played back from the tape recorder through the wideband frame synchronizer so that the same video image reformatting hardware and data reduction and image processing software can be used just as it is in real-time data acquisition.

The HP3852A Data Acquisition and Control Unit

Figure 10 is a block diagram of the DAC along with two custom digital multiplexer circuits used to expand the number of digital inputs and outputs. The DAC is controlled by its own MC68000 microprocessor and is programmable in the same language as the computer: Real-time Measurement Basic (RMB, also known as HP Basic). The computer can send discrete commands to the DAC, or it can download programs which run automatically with or without computer intervention to send commands, acquire data, make decisions on the data, and send data to the computer.
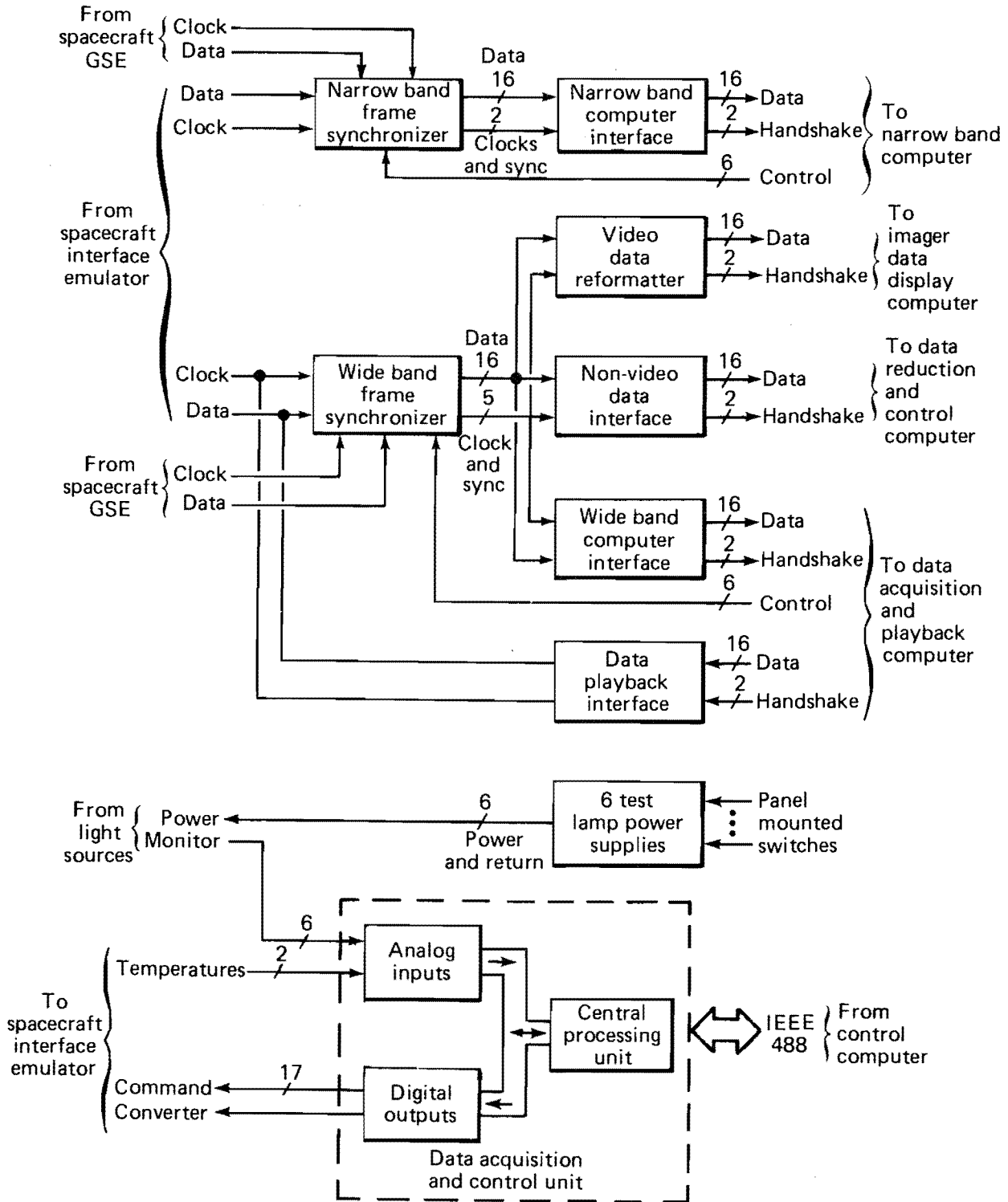
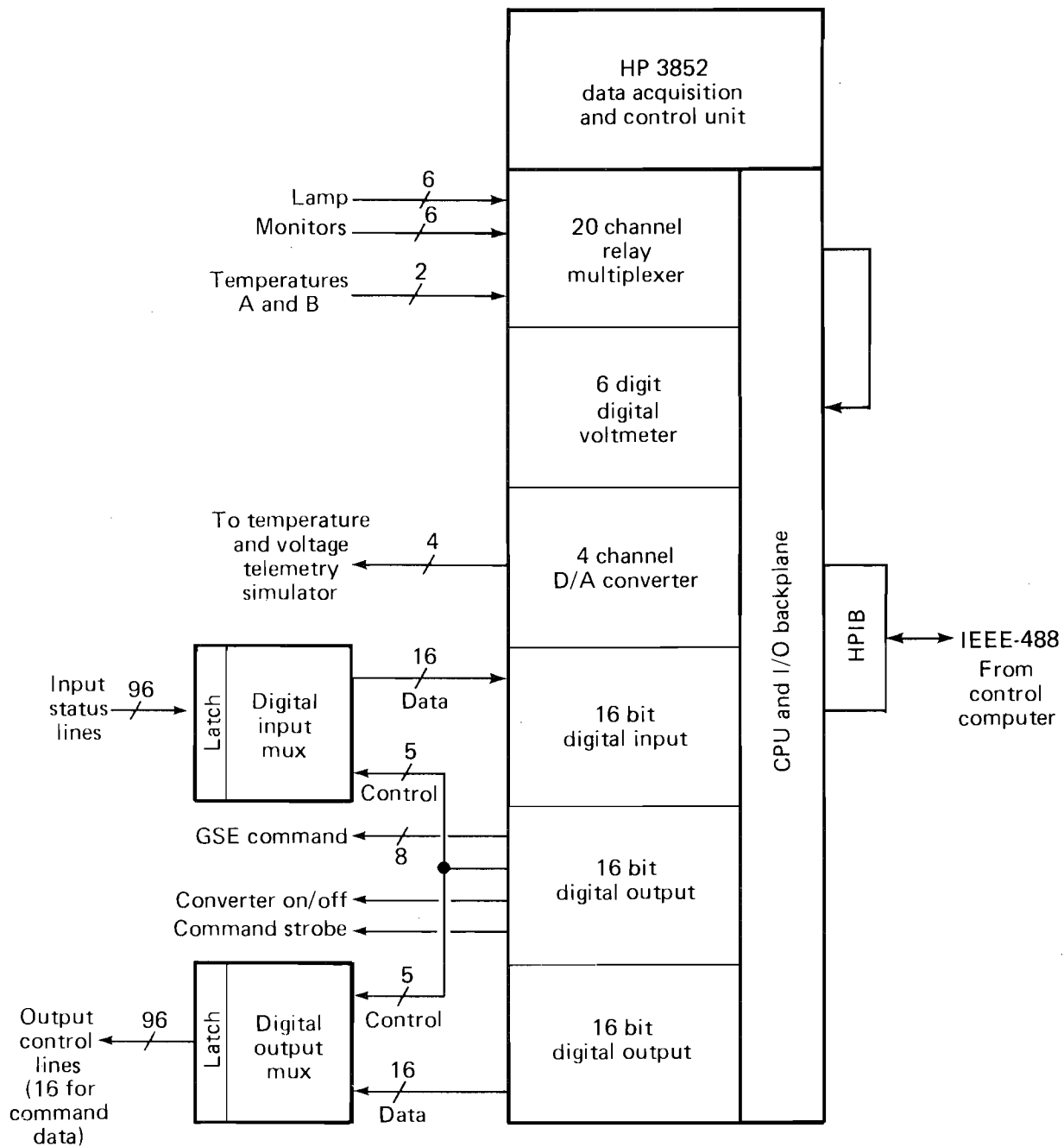**Fig. 9   Block diagram of data acquisition and control.**

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Fig. 10   Block diagram of data acquisition and control unit.

The Frame Synchronizers

The frame synchronizer's purpose is to identify the frame synchronization word and provide a timing mark to the computer interface. The computer interface distinguishes between valid and invalid frame timing marks, buffers the data, and provides a handshake for its transfer to the computer. The narrowband and wideband computer interfaces are designed to pass the entire frame to the computer, while the non-video computer interface and video data reformatter are designed to only pass that portion of the frame which is appropriate to its function. The video display computer, therefore, only receives image data, which is grouped in the latter 6144 bytes of each wideband minor frame, while the data reduction and control computer receives only the first 384 bytes, which is allocated to spectrograph, housekeeping, and status data.

A typical frame synchronizer-computer interface pair is depicted in Figure 11. Data and clock inputs from the telemetry interface simulator (or the playback interface) or the sensor module GSE are selected through a data switch which is controlled by the computer. The data is clocked serially into a shift register long enough to hold the frame synchronization word and the minor and major frame counts. A row of exclusive-or gates compares the data to the frame synchronization word as each bit is clocked. Any differences between bits are referred to as errors which are added using an "inverted pyramid" block of digital adders. The total number of errors is compared to the number which the computer selects as being tolerable, and if the number of errors is small enough, the candidate frame timing mark is produced.

The frame timing mark is sent to the computer interface board and input to the synchronization validator. This circuit consists of cascaded synchronous binary counters which count the number of bits clocked after the reception of the timing mark. The circuit will accept no further frame timing marks until it has counted the appropriate number of bits for a minor frame. If the previous timing mark was valid, the clock edge following the last bit expected in the minor frame will become coincident with a new minor frame timing mark and the circuit will produce a valid frame pulse. If the new frame mark is not detected as expected, then no valid frame pulse is generated and the circuit remains dormant until another candidate frame timing mark is received.

A first-in-first-out (FIFO) memory is used to buffer the data clocked out by the synchronization validator. The FIFO is configured to be 16 bits wide to match the width of the computer data port, and the depth of the FIFO is picked to allow enough data (about 15 milliseconds worth for wideband data, or $\frac{1}{3}$ of a minor frame) to be temporarily stored in the event that the computer processor or direct memory access (DMA) logic loses priority over the data collection process. Under normal operation the FIFO data are read out immediately after they have propagated to the output stage and so the FIFO is always kept empty by the computer.

The first piece of data which the computer interface is designed to provide to the computer is the first 16-bit word in the major frame (or major major frame for wideband data). To facilitate decommutation, computer memory is allocated via software such that the data flows into a structure which mimics the organization of one major frame. The computer will merely have to check those locations which it expects will hold the minor and major frame counts and frame synchronization words to validate and identify the data. Sometimes when the minor frame synchronization signal is not validated, minor frames will be dropped out and the software will automatically relocate the valid frames before attempting decommutation. This occurs when the instrument is commanded on and off, during real-time mission data acquisition near acquisition-of-signal (AOS) or loss-of-signal (LOS) points in the spacecraft pass, or during playback of data. It can be said, therefore, that minor frame synchronization is done in hardware, and major frame synchronization is done in software.
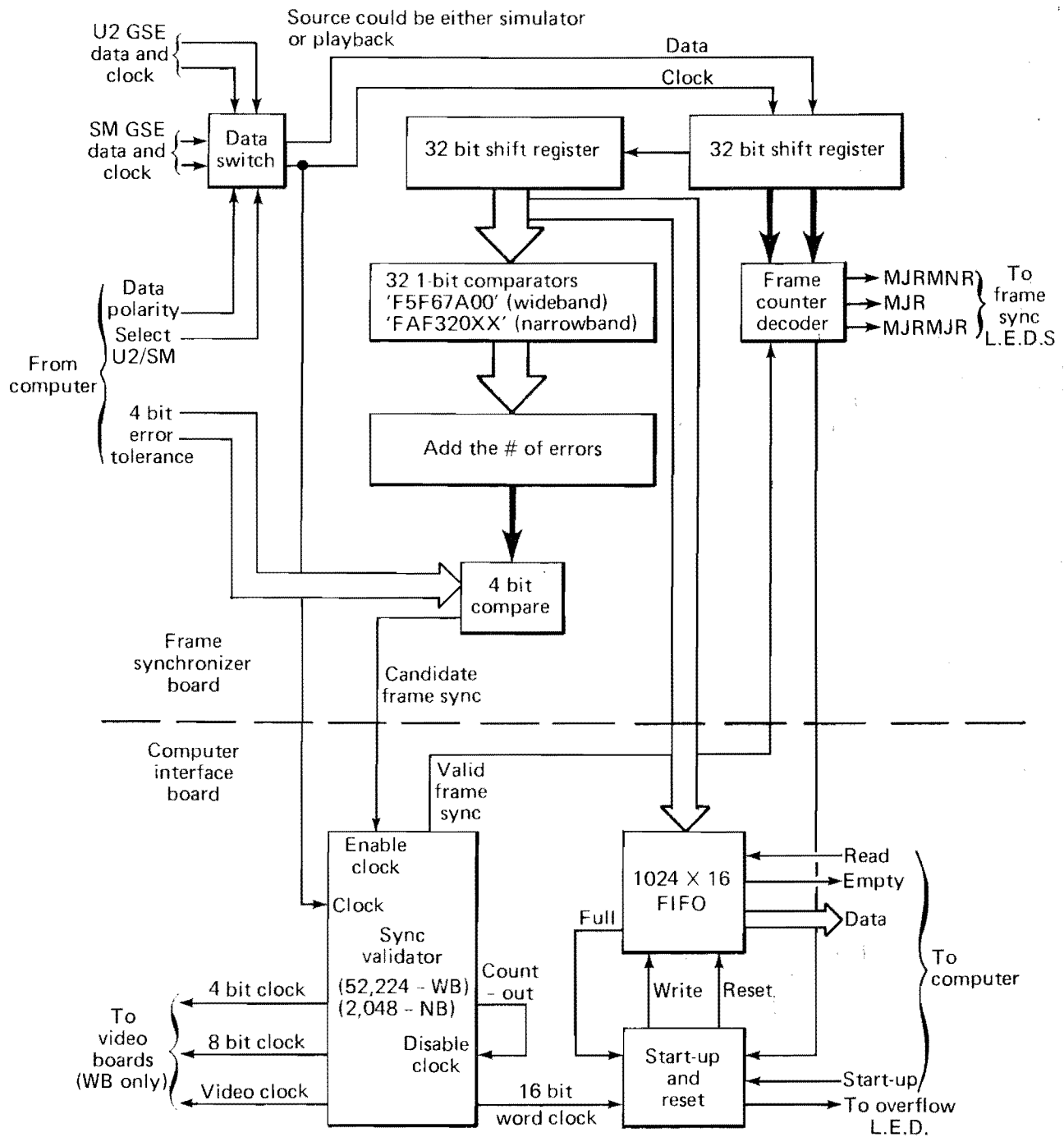
Fig. 11 Block diagram of frame synchronizer/computer interface.

COMPUTER SYSTEMS

System Configuration

The function of the computer system is to provide the test operator with the means to control and monitor the test without having to understand the details of the data acquisition, control, and interface emulation systems. The computer system keyboards' predefined user keys are designed to provide the test conductor with options for command, display, data storage, and hardcopy which satisfy the requirements specified in the test procedures. A block diagram of the U2 GSE computer system is shown in Figure 12. A combination of the U2 Experiment's complexity, high data rate, and ambitious development schedule warranted the use of several modular desktop computers as opposed to a central mainframe. Separating the GSE functions into modules such as: wideband data storage, instrument control and monitor; camera image display; and narrowband data storage and display, reduced the sophistication of the GSE software design which minimized development risk and the adverse effects of a single computer malfunction. At the same time, it ensured sufficient processing power for real-time monitoring during critical points in testing or in the mission. The selection of a particular brand of computer was based on: its response time to data interrupts, its ability to reduce and display the data (i.e. four 128 point spectra) with less than five seconds between updates, and its operation and programming ease.

The HP300 Series Computer

The Hewlett Packard 300 series (HP310 and HP320) computer system has many strong points which make it suitable for real-time data acquisition, control, and data reduction tasks. These include:

1. An asynchronous, eight MHz I/O backplane with a 16-bit data bus, 24-bit address bus, and bus arbiter, and which can support the following interfaces:

    a. A dual channel Direct Memory Access (DMA) board.

    b. Up to eight megabytes of Random Access Memory (RAM).

    c. RS-232 serial (19200 baud max double duplex).

    d. IEEE-488 8-bit (HPIB: 350/290 kbps I/O rate).

    e. Generic 16-bit (GPIO: 540/525 kilowords per second I/O rate).

2. HP Basic (Real-time Measurement Basic, RMB); a popular, user friendly operating system and interpretative language which specializes in prioritized interrupt handling and background data transfer, supports structured software constructs and graphics, and facilitates real-time user interaction.

3. A wide selection of compatible HP and third party peripherals, interfaces, and support software.

4. Powerful processor boards which include:

    a. MC68010 microprocessor running at 10 MHz (HP310), or MC68020 microprocessor with MC68881 Floating Point Coprocessor running at 16.6 MHz (HP 320).

    b. One megabyte of internal memory (HP310), or a 16-kilobyte instruction and data cache (HP320), and a memory management unit.
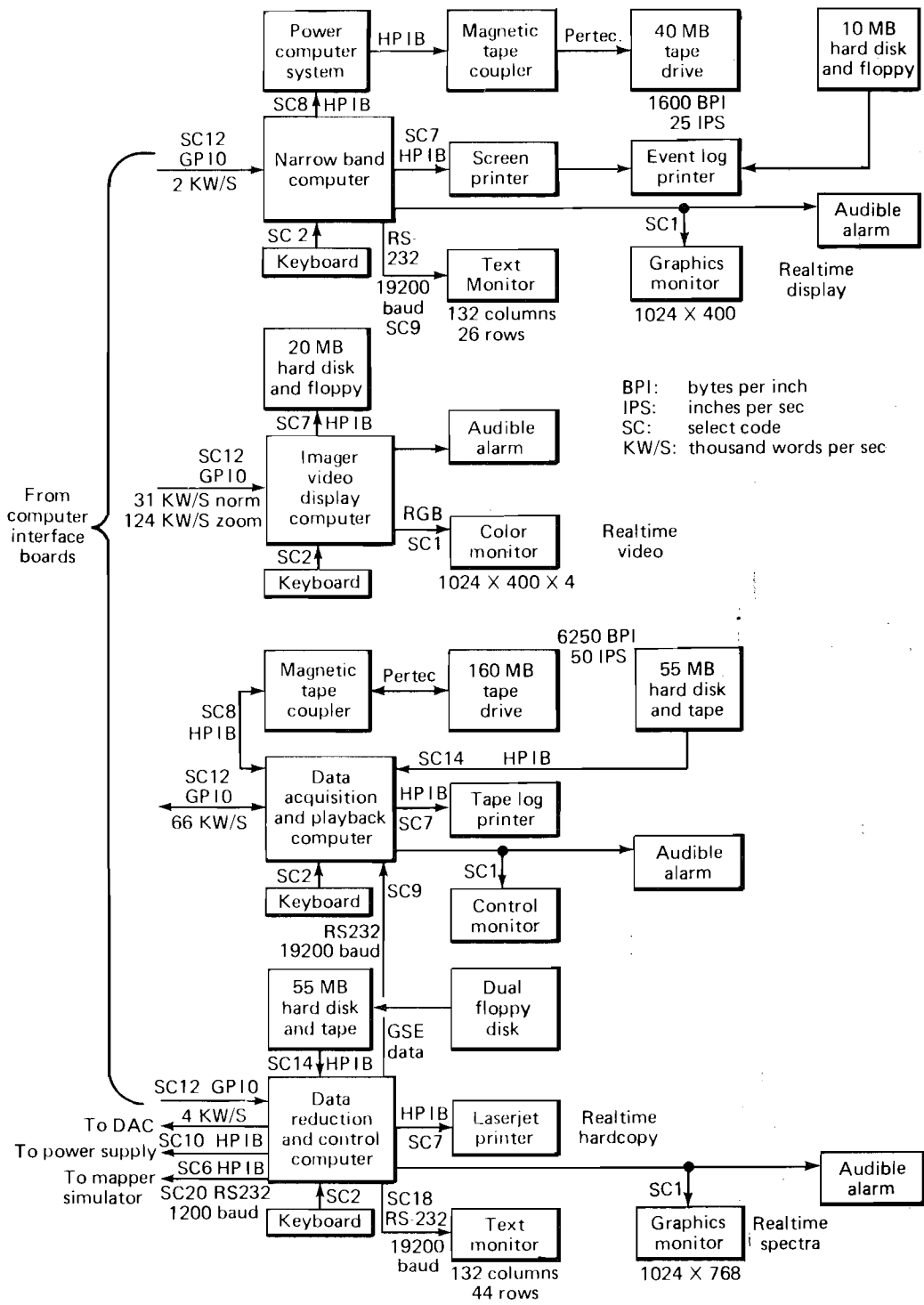
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Fig. 12   Block diagram of U2 GSE computers.

c. System timers with 4 millisecond resolution, user timers with 10 millisecond reso-
lution, and a battery backed real-time clock.

d. Keyboard, beeper, and video interfaces.

Figure 13 is a generalized block diagram of the series 300 computer. The bus on the left
side of the figure handles all of the high speed communication between the central process-
ing unit (CPU), internal memory, system timers, and video display interface while the I/O
backplane bus arbitrates the communication between the external interfaces. The CPU
fetches instructions and data from the eight MHz external memory while using its onboard
memory to allow processing at higher rates. The DMA card can control data I/O between
the external memory and peripheral interfaces without the processor's intervention.

Figure 14 is a block diagram depicting the service routines, or tasks, for the data reduc-
tion and control program. The symbol key at the bottom of the figure shows how the
diagram represents the relationship between each data set, interface, and service routine.
There are three data sets onto which the tasks operate; telemetry, command, and display.
Updating the telemetry data set with the latest wideband major frame has the highest priori-
ty for this program. GSE data collected from the DAC also updates the telemetry data set
and is then sent to the data acquisition computer. The decommutation and reduction of
the data and its display on the terminal occurs about every three seconds. The task to update
the video monitor or change graphics displays is selected by a keyboard softkey. The second
highest priority interrupt comes from a programmable timer which prompts the updat-
ing of the flight processor (mapper) simulator with the latest pointing information from
the command data base. Tasks which change the mapper message, issue new commands,
and control system power also update the command data base when interrupted by the
keyboard softkeys. The lowest priority tasks are those which copy the display screen
contents, maintained in the display data base, to the printer buffer. Examples of typical
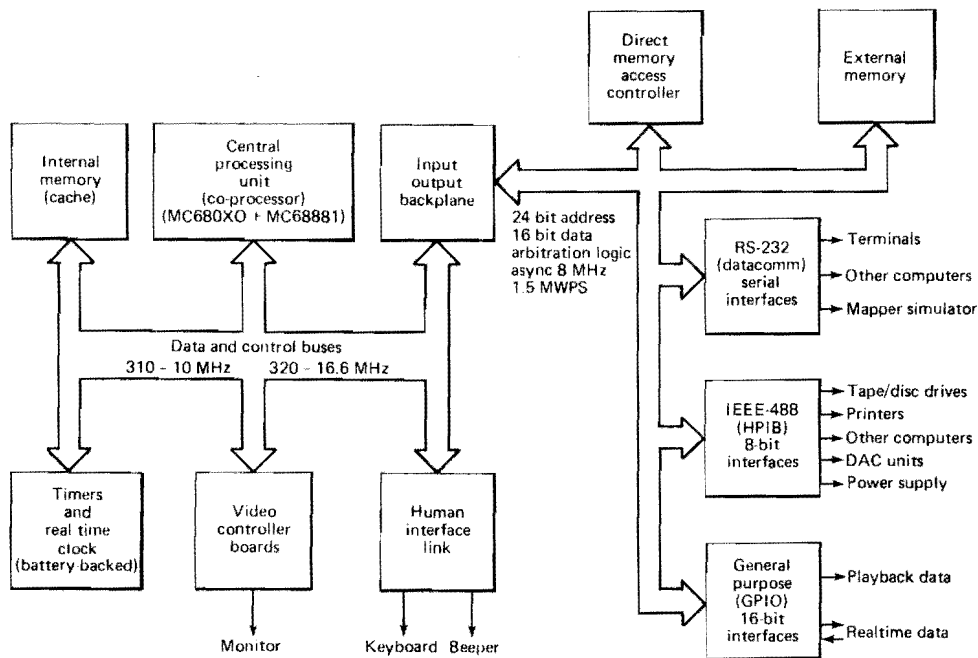printer output are included in Figure 15, and example command screens in Figure 16.

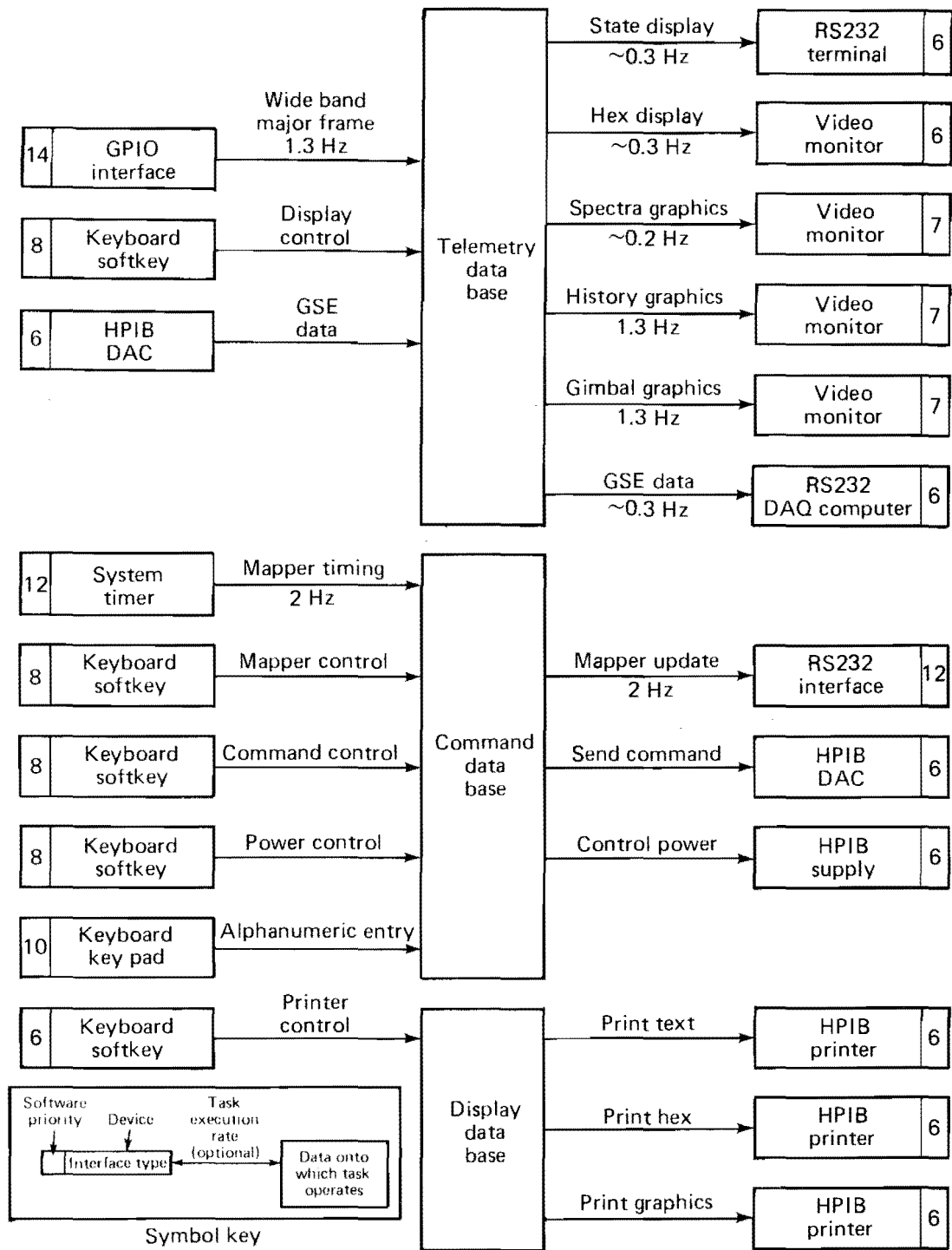**Fig. 13   Block diagram of computer hardware.**

Fig. 14 **Block diagram of relationship between data, tasks, interfaces, and priorities for data reduction and control program.**

U2 EXPERIMENT GSE STATE DISPLAY   17 Dec 1987

	SPECTROGRAPH 1			SPECTROGRAPH 2			SPECTROGRAPH 3			SPECTROGRAPH 4			SPECTROGRAPH SYSTEM	
COMMANDS	XMT	REC	STATE	XMT	REC	STATE	XMT	REC	STATE	XMT	REC	STATE	SDU AGC RESET COUNT		0
FIL POS	0	3	3 OPEN	0	3	3 OPEN	0	3	3 OPEN	0	3	3 OPEN			
LMP PWR	0	0	0 OFF	0	0	0 OFF	0	0	0 OFF	0	0	0 OFF	SPECTROGRAPH	EXTRNAL	
AGC MODE	0	3	3 AUTO	0	3	3 AUTO	0	3	3 AUTO	0	3	3 AUTO	DATA SUMMARY	LMP MON	
INT PWR	0	1	1 EN	0	1	1 EN	0	1	1 EN	0	1	1 EN	WD CT S1 7.129E+02	0.00	
AGC DTY CYCLE			050.1			000.5			000.5			001.7	WD CT S2 2.065E+03	0.00	
ACC SUM ERR			0 OK			0 OK			0 OK			0 OK	WD CT S3 1.620E+03	0.00	
FID ERR OR WHL MOV			0 OK			0 OK			0 OK			0 OK	WD CT S4 1.173E+03	0.00	
FIL WHL ERR			0 OK			0 OK			0 OK			0 OK	PK WL S1 7.319E+03	BIN 103	
FIL WHL DIR			1 FWD			1 FWD			1 FWD			1 FWD	PK WL S2 3.290E+04	BIN 61	
FIL WHL PWR			0 OFF			0 OFF			0 OFF			0 OFF	PK WL S3 1.674E+04	BIN 112	
INT CKT BREAKER			1 ON			1 ON			1 ON			1 ON	PK WL S4 1.782E+04	BIN 46	

	IMAGER 1			IMAGER 2			IMAGER SYSTEM			COMMAND STATUS		MISSION ELAPSED TIME	
COMMANDS	XMT	REC	STATE	XMT	REC	STATE	CMD	XMT	STATE	TLM MJR FRM	001498	009834.6266 SEC	
FIL POS	0	0	1 ND1 *	0	0	1 ND3 *	FIELD	0	0 FULL	CPU MJR FRM	001494	LOCAL TIME	
AGC OVER	0	0	0 USE AGC	0	0	0 USE AGC	GAIN	0	0 NORM	CMD CNT	005	12:44:05	
INT PWR	0	0	0 DIS	0	0	0 DIS	ZOOM ADDRESSES			CMD REJ CNT	000	+28V INPUT POWER	000.00 W
AGC DTY CYCLE			012.5			000.0	COLUMN		072	LST CMD REJ	0000	+28V INPUT VOLTAGE	00.00 V
AGC ACQ TIME			37.92			57.08	ROW		090	CMD MACRO	127	+28V INPUT CURRENT	0.00 A
AGC LVL			999			999	EXTERNAL CAL LAMPS			CONV 1	CONV 2	CONV 3	GIMBAL
FIL WHL ERR			0 OK			0 OK	IMAGR 1 LAMP		0.00	+15 +14.49	+12 +11.72	+28 +28.36	+28 +28.75
FIL WHL HI PWR ERR			0 OK			0 OK	IMAGR 2 LAMP		0.00	-15 -15.40	-12 -12.09	+15 +14.82	+15 +14.95
FIL WHL PWR			0 OFF			0 OFF				+5 +04.80	+5 +04.88	-15 -14.94	-15 -15.17
FIL WHL HI PWR			0 NORMAL			0 NORMAL							CUR +00.93 A
FIL WHL DIR			1 FWD			1 FWD				DCIS DAC 1,4 =	+00.98	Volts	
INT CKT BREAKER			0 OFF			0 OFF	CKT RESETS		0	DCIS DAC 2,4 =	+04.00	Volts	

	GIMBALS									TEMPERATURES			
COMMANDS	XMT	REC	STATE		COMPUTED	MEASURED	ERROR		S1 LAMP +23	S1 MOTOR +26	S1 HV PWR +22		
MAPP CMD	0	0	OFF	AZ 1	+0.00073	-0.00106	+0.00179	DEG	S2 LAMP +23	S2 MOTOR +25	S2 HV PWR +25		
BORE COR	0	0	OFF	AZ 2	+0.00073	-0.02210	+0.02283	DEG	S3 LAMP +26	S3 MOTOR +20	S3 HV PWR +25		
PATT REP	0	0	SINGLE	AZ 3	+0.00073	-0.00905	+0.00978	DEG	S4 LAMP +26	S4 MOTOR +22	S4 HV PWR +23		
PATT SEL	0	0	NONE	AZ 4	+0.00073	-0.01423	+0.01497	DEG	I1 HEAD 1 +23	I1 MOTOR +26	CONV 1 T1 +33		
PATT SIZ	0	0	0.00 DG	EL 1	+0.00073	+0.00630	-0.00557	DEG	I1 HEAD 2 +23	I2 MOTOR +24	CONV 1 T2 +35		
PATT INC	0	0	0.10 DG	EL 2	+0.00073	-0.02069	+0.02142	DEG	I2 HEAD 1 +24	GMBL MO 1 +21	CONV 2 T1 +35		
OFST AZI	+0.0000	+0.0000	DEGREES	EL 3	+0.00073	-0.01015	+0.01088	DEG	I2 HEAD 2 +23	GMBL MO 2 +20	CONV 2 T2 +37		
OFST ELE	+0.0000	+0.0000	DEGREES	EL 4	+0.00073	-0.00496	+0.00569	DEG	GMBL BD 1 +17	GMBL MO 3 +22	CONV 3 T1 +29		
UNIT XVT	+0.0000	+1.0000		PAT POS		000			GMBL BD 2 +16	GMBL MO 4 +19	CONV 3 T2 +29		
UNIT YVT	+0.0000	+0.0000		MAP MES LST CT		000	AZ/EL GRAPHICS		DCIS CPU +29		CAGE T1 +14		
UNIT ZVT	+0.0000	+0.0000		MAP PAR ERR CT		000	AZ/EL DISPLAY		DCIS ANA +33		CAGE T2 +22		
RANGE	000.0000	999.9999	KM	LST MSG MINOR		000							
TIME	000.0000	500.0000	MSEC	LST MSG MAJOR		000000							

Text display

Fig. 15   Spectra graphics.

Fig. 16 Command screens.

For data acquisition, tasks associated with the telemetry data set are responsible for transferring the wideband and GSE data to the tape drive, and displaying and printing the status of the drive. The control set includes the frame synchronizer error tolerance, input select, and data polarity settings, and the data acquisition mode. Softkey options allow the user to collect a predefined amount of data depending on which test is being run or put the program in automatic mode, where it will save the data as they become available. The playback program reads the data from the tape drive and sends them to the playback interface. Partial records caused by satellite data dropouts will generate errors with the tape coupler, so the program uses these to interrupt the program, correct the error, and resume playback.

The narrowband software tasks for the telemetry data set are similar to those of the data reduction and control software but involve only two different display screens which are much simpler in nature. Two additional tasks are to log U2 Experiment commands on the printer and to send the data to the power system monitor.

The imager video display software updates and sends the imager data set to the screen. Different color mappings can be selected via softkeys to enhance the appearance of the image, and the least or most significant bits can be specified for display. Images can be saved to the hard disk for quick recall later on when hardcopy is desired.

SUMMARY

GSE for spacecraft subsystems require three major elements: interface emulation; data acquisition and control; and computer systems. The development and integration of subsystems which contain embedded processors are enhanced by providing simulators for the processor's subsystem interfaces as well as those for spacecraft and other special test interfaces. The flight qualification of instrument subsystems is enhanced by providing a simulation of the environment to which the sensors will be exposed. The data acquisition and control section will typically require multiple channels of analog and digital I/O and a computer interface. If subsystem monitoring is to be continued at the spacecraft level and the data rate is sufficiently high, a hardware frame synchronizer will be required for the telemetry downlink. Computer system requirements include a keyboard, data display, hardcopy unit, data storage device, and real-time software. The GSE may also be required to collect data during the mission and support data recovery afterwards if remote ground stations were involved.

The U2 Experiment is an instrument subsystem containing embedded processors. The U2 GSE implementation was found to be appropriate for a multi-sensor optical emissions instrument with complex command capability, high data rate, and a design-to-launch development cycle of 18 months.

The design of the U2 Experiment GSE was inspired by the idea of having a single tool comprehensive enough to be usable not only for all phases of instrument development and testing, but employable beyond launch to enhance both mission and post-mission activities and data analyses. The trend for GSE, made possible by the continually increasing power available in microprocessor-based systems, will be to provide more of the real-time image processing, database management, and sophisticated data reduction now performed on a separate workstation long after the data are acquired. GSE will also be requiring higher data throughput rates as it supports the development of powerful embedded processors which provide instruments with more autonomy, while simultaneously reducing downlink transmitter requirements.

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