

A Study on Thermal Modeling and Heat Load Mitigation for Satellite Electronic Components

Young-Keun Chang*

Director, Space System Research Laboratory, Hankuk Aviation University
200-1 Hwajeon-dong, Deogyang-gu, Koyang, Kyonggi-do, 412-791, Korea
Phone (02) 300-0286 Fax (02) 3158-3189
E-mail; ykchang@mail.hau.ac.kr

Min-Young Kang, Jin-Han Park

Space System Research Laboratory, Hankuk Aviation University
200-1 Hwajeon-dong, Deogyang-gu, Koyang, Kyonggi-do, 412-791, Korea
Phone (02) 300-0147 Fax (02) 3158-3189
E-mail; ssrl@mail.hangkong.ac.kr

Young-Jin Choi

Space Development and Research Center, Korea Aerospace Industries
Yusung-gu, Taejon, Korea
E-mail; cyj65@koreaaero.com

Abstract. Since most of the satellite components are using various EEE (Electrical, Electronic and Electromechanical) parts, the reliability of EEE parts acts very important in the satellite system. There are many factors that influence the reliability of EEE parts in the satellite system. Excessively dissipated heat can cause the failure of EEE parts and consequently, leading to a failure of total satellite system. In this paper, the thermal modeling using nodal network was compared with that using plate modeling to find out which one is the most suitable methodology. For a comparison, KOMPSAT-1 SAR was modeled by two different modeling and the result was discussed. There was almost no difference in the numerical results between the two modeling methods. However, while it took much more time to perform thermal analysis using the nodal network modeling method, and the debugging was more difficult in the plate modeling method when the error is occurred. The computation time was considerably reduced by developing and implementing the input file format transfer code when using nodal network modeling method. It was found that the nodal network modeling method is suitable for the complicated components, such as SAR or transponder, because of its simple debugging ability. Excessive heat load was expected on some EEE parts of SAR such as high heat-dissipated diodes, transistors, and inductors due to increased power requirements of KOMPSAT-2 satellite system. The methods for the mitigation of heat load were studied through the design change of housing or the layout change of high power parts.

1. Introduction

Since it would be almost impossible to recover or repair the satellite in space once it has been launched, a detailed analysis and design, manufacturing using the high quality workmanship, and qualification and acceptance in space-simulation environments are necessarily accompanied for all satellite components prior to launch. In particular, the electronic boxes are occupying an important role in satellite. Some malfunction or fault occurred in the electronic box can make satellite useless or give catastrophic damage in the mission. Such a consideration of the thermal issues in satellite system and

components development becomes very important.

The most important element in the design of electronic boxes operated in space environments is to design the optimal circuits. The temperature, among various elements, can provide a considerable impact on the electronic boxes from the viewpoint of efficiency. In case the temperature of electronic parts increases, it might cause a malfunction or rather burning-up. This leads to satellite failure as well as the reduction of satellite life. Thermal control is recognized to be a major factor in the design, which requires the thermal analysis.

As well known, the convection heat transfer

mechanism does not exist in space. The overall thermal control of the satellite in orbit is accomplished through the balance between the energy dissipated from the internal electronic boxes and the energy obtained from satellite outside by conduction and radiation. The sources of internally dissipated heat in the satellite are communications system transponder, battery, electronic boxes, and, when the liquid apogee engine is implemented, including the heat radiated from the engine. The design of thermal control subsystem should maintain the temperature of electronic boxes within the operational limits based on suppliers' data.

2. Thermal Analysis Steps

The temperature of electronic box depends on heat dissipation from EEE (Electric, Electronics, Electro-mechanical) parts except heat input from the external environments. It is necessary to fully understand how much heat is generated from the EEE parts, and through which path the heat passes to the exterior of the electronic box.

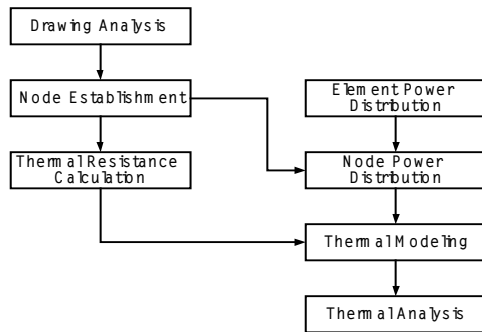


Figure 1. Thermal Analysis Flow Chart

The thermal analysis is performed as shown in Figure 1. In the first phase of drawing analysis, thermal path will be clarified by investigating mounting state between PCB (Printed Circuit Board) and frame configuration, and housing configuration in the design drawing. Constant number of nodes are established based on drawing analysis in the second phase of node establishment, in which nodes are divided by optimizing the configurations and junction locations of PCB, spacer, frame, and housing, etc. The elements dissipating higher power such as transistors and diodes are classified as special nodes. Thirdly, thermal resistance is computed between nodes. There are several thermal resistance such as heat conduction resistance considering material, distance, sectional area

between node and node, and junction resistance considering contact area and pressure in the thermal analysis of electronic boxes. The input values are those considering the worst case by simplifying complicated configuration. In the fourth phase, the parts location is identified and the power dissipation for corresponding parts and nodes are calculated, respectively. In the thermal modeling process, the following work is achieved; the definition of node coordinates in space, connection by thermal resistance between nodes, and heat allocation to nodes. Finally, the temperature is computed by defining boundary nodes and boundary temperature on the thermal model.

3. Calculation of Thermal Resistance

3.1 Thermal Resistance

The simple and relatively exact solution can be obtained using the concept of thermal resistance in the thermal analysis. Since thermal resistance represents similar characteristics to electric resistance, thermal circuit representation provides an efficient tool for both conceptualizing and quantifying thermal modeling.

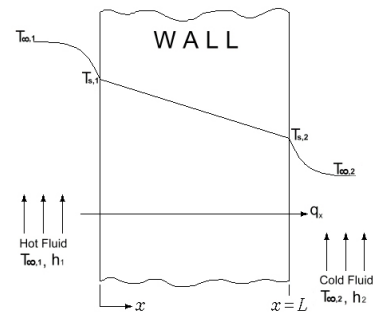


Figure 2. Heat Transfer Through a Plane Wall (Temperature Distribution)

For one-dimensional conduction in a plane wall, temperature is a function of x -coordinate only and heat is transferred exclusively in this direction. In Figure 2, a plane wall separates two fluids having different temperatures. Heat transfer is occurred by convection from the hot fluid at $T_{\infty,1}$ to one side of the wall at $T_{s,1}$, by conduction through the wall, and by convection from the other side of the wall at $T_{s,2}$ to the cold fluid at $T_{\infty,2}$. By considering conditions within the wall, we first determine the temperature distribution, from which we can obtain the conduction heat transfer rate. The temperature distribution in the wall can be determined by solving the heat equation with the proper boundary conditions. The Fourier's law

is used to determine the conduction heat rate from the temperature distribution.

$$q_x = -kA \frac{dT}{dA} = \frac{kA}{L}(T_{s,1} - T_{s,2}) \quad (1)$$

where A is the area of the wall perpendicular to the direction of heat transfer and it is constant without regard to x at the plane wall. There exists an analogy between heat diffusion and electrical charge. Just as an electrical resistance is associated with the conduction of electricity, a thermal resistance can be related to the conduction heat rate. Defining resistance as the ratio of a driving potential to the corresponding transfer rate, it follows from the equation (1) that the thermal resistance for conduction is shown as below[3].

$$R_{t,cond} \equiv \frac{T_{s,1} - T_{s,2}}{q_x} = \frac{L}{kA} \quad (2)$$

3.2 Contact Resistance

The contact resistance is generated by the junction pressure between the contact surface of any two bodies. The electronic equipment consists of various elements such as printed circuit board, frame or page frame, spacer, housing, cover, etc. These elements are fastened with screws each other, and the pressure exists between the contact surface. The contact resistance is represented as a function of the pressure applied to the surface as shown in equation (3).

$$R_{i(interface)} = \frac{50}{P^{2/3}} \quad [\square \cdot \text{in}^2 / W] \quad (3)$$

$$P = \frac{5nE}{Ad}$$

where, P = mounting pressure, psi
 n = number of screws
 E = torque/screw, in-lb
 A = mounting area, in²
 d = nominal diameter of screw, in

$R_i \sim P^{2/3}$ is roughly expected from elastic deformation theory[4]. The constant has been determined so that the curve approximates experimental data for vacuum conditions.

3.3 Printed Circuit Board Resistance

The satellite electronic equipment usually consist of several PCB (Printed Circuit Boards). Electric, electronic, and electromechanical parts are installed on PCB and the heat generated by

parts pass through PCB. Since PCB is composed of multiple copper layers, a thermal resistance per unit area for each layer can be determined and then added in parallel as shown in Figure 3. The exact circuit configuration should be known to get the theoretical thermal resistance per unit area, however, actually an approximate resistance per unit area is used here. The combined thermal resistance is then multiplied by a length/width shape factor to determine the total thermal resistance between nodes.

$$R_{SQ} = \left[\frac{1}{\frac{1}{R_{SQ1}} + \frac{1}{R_{SQ2}} + \frac{1}{R_{SQ3}} + K + \frac{1}{R_{SQm}}} \right] \quad (4)$$

$$R = \left(\frac{L}{W} \right) R_{SQ} \quad (5)$$

where, RSQ = thermal resistance of printed circuit board per unit square, \square/W
 m = number of copper layers
 L = distance between nodes, in
 W = width between nodes, in

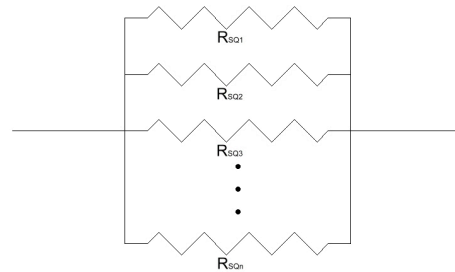


Figure 3. Schematic of Thermal Resistors for Multi Layer Printed Circuit Board

3.4 Page Frame Resistance

The page frame is a frame PCB is directly installed as shown in Figure 4. The left figure is representing a PCB attached to page frame, the right one is a page frame itself. In the x-y plane view (top view), the page frame is directly exposed in one part and the other part is covered with PCB. The resistances in the page frame are different depending on the interval: a corner section, a center, x and y directions, and a section which PCB and page frame are superposed. Both the resistance of the page frame and that of PCB should be applied to nodes existed on the surface located between the page frame and PCB. Consequently, the computation of thermal resistance in the page frame is relatively complex.

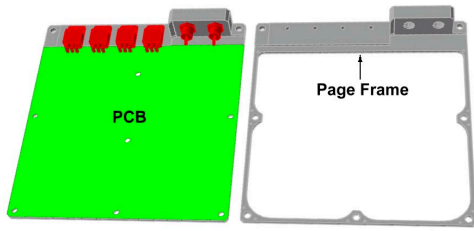


Figure 4. Configuration of Page Frame

3.5 Printed Circuit Board to Housing Thermal Resistance

The heat path from PCB to housing is different depending on the electronic equipment. The total thermal resistance can be calculated by summing all of the resistances in series between PCB and housing. As illustrated in Figure 5, some heat paths are composed of the page frame resistance and contact resistance and others are formed with PCB resistance, epoxy resistance connecting between PCB and page frame, and page frame resistance, and contact resistance.

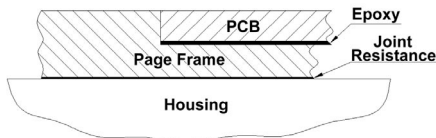


Figure 5. Printed Circuit Board to Housing Thermal Resistance

3.6 Spacer/Frame Standoff Resistance

As described in the previous section, several PCBs are located within an electronic box. It is the spacer that plays the role in the heat path maintaining the space among PCBs. The frame standoff provides the similar function as a spacer by being positioned between PCB and frame, and not among PCBs as shown in Figure 6. The KOMPSAT-1 (Korea Multi-Purpose Satellite) On-Board Computer (OBC) has three supporting frames inside the housing, and four to six PCBs are installed in the individual frames. In other words, the heat dissipated from the PCBs is transferred to frame via spacer and frame standoff, and consequently transferred to baseplate via housing.

The understanding for an exact configuration and the area and pressure of the surface contacted with boards are necessary to calculate the spacer resistance. The spacer thermal resistance consists of its own resistance and two joint resistances from both ends of the spacer. Since the one end is fixed with frame in case of the frame standoff, the total resistance can be calculated by adding contacting resistance (contacting with PCB) acting on other side on the original frame standoff

resistance.

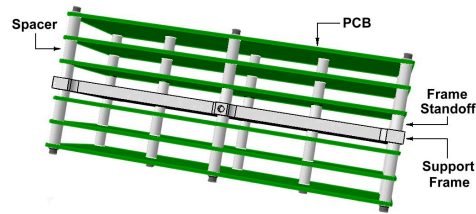


Figure 6. Configuration of Spacer and Frame Standoff Installed on Support Frame

3.7 Sponge Rubber Resistance

The sponge rubber thermal resistance means a resistance of silicon sponge. In some case, a sheet of silicon sponge rubber is sandwiched between PCB and housing or PCB and frame. It also has a contact resistance whose approximate value can be obtained from manufacturer's data. The heat path is summarized as follows; PCB, contact surface, sponge rubber, another contact surface, and housing or other PCB. Total thermal resistance can be simply calculated by adding the individual resistances in series.

3.8 Frame to Housing Resistance

The frame to housing resistance exists in all electronic boxes including frame. It is a contact resistance of contact area between the frame and housing. For example, three supporting frame of the KOMPSAT-1 OBC is fastened to the housing in the five places and to the cover in one place as shown in Figure 7. The frame to housing resistance is simply calculated by directly summing the frame resistance and the contact resistance.

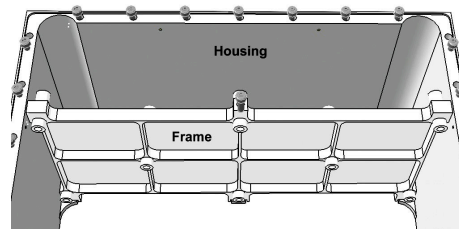


Figure 7. Frame Installed in Housing

3.9 Housing Resistance

A typical housing of electronic box has a shape of hexahedron including one cover side. The resistance for each side is separately calculated due to different size and thickness per sides. Since the cover and housing are fastened with screws, the contact resistance should be taken into consideration.

3.10 Housing to Mounting Surface Resistance

The mounting surface or baseplate is the place where the electronic equipment is directly installed on the satellite. This surface will be boundary condition for thermal analysis.

3.11 Transistors and Diodes

The most important element in the thermal analysis is the EEE parts having the high power dissipation. These elements will give a considerable impact on the numerical solution (or actual temperature on orbit) and be controlled separately. The representative ones are transistors and diodes. Those parts have its own heat path. When the overall thermal analysis is performed, the thermal resistance located on the heat path should be certainly considered.

3.12 Calculation of Radiation Factor

The thermal radiation is associated with the rate at which energy is emitted by matter as a result of its finite temperature. At this moment thermal radiation is being emitted by all the matter that surround us: by the furniture and walls of the room in the interior or by ground, buildings, atmosphere and the sun in the exterior. The mechanism of emission is related to energy released as a result of oscillations or translations of lots of electrons that constitute matter. These oscillations are, in turn, sustained by the internal energy, and consequently the temperature, of the matter. The emission of thermal radiation is associated with thermally excited conditions within the matter.

In a system of n surfaces, the exchange of energy between any two gray surface is

$$q_{ij} = A_i F_{i-j} (W_{bi} - W_{bj}) \quad (6)$$

where, $W_b = \sigma T^4 =$ emissive power of black body, W/in^2

$A =$ area, in^2

$F =$ exchange coefficient

$\sigma =$ Stefan-Boltzmann constant

The radiation factor is $RF = A_i F_{i-j}$,

$$F = \frac{1}{\frac{1}{\epsilon_i} + \frac{1}{\epsilon_j} - 1} \quad (7)$$

where, $\epsilon_i =$ emissivity of i node

$\epsilon_j =$ emissivity of j node

There are some cases which thermal radiation should be considered at thermal modeling. The

judgment whether thermal radiation is considered or not is not based on theoretical background and on empirical factors.

4. Thermal Modeling Methods

4.1 Nodal Network Modeling

The method of this modeling first divides the object for thermal analysis into a finite number of nodes and connects between node and node by using thermal resistance. This method has advantages of simplicity and fast calculation and disadvantage of requiring time-consuming manual work for modeling. It is the most popular modeling method for thermal analysis. In general, the analysis results are compared to thermal test data. However, the temperature measurement of the board is difficult in the case of Flight Model (FM) electronic equipment. Thermal test data obtained from Prototype Model (PM) can be used to compare with thermal analysis results, however, it may be difficult to utilize PM thermal test data as an initial value of FM thermal analysis. Most likely, FM will be built after design change based on PM thermal test data and thermal analysis results. The thermal analysis results are also used as input data of thermal test like selection of thermocouple location.

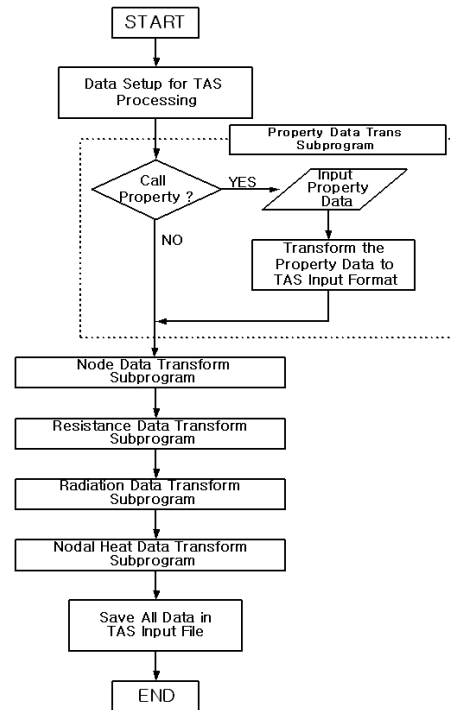


Figure 8. Input File Transformation Code

As described above, all data for thermal

modeling should be input manually in the nodal network modeling. In this study, the input file transformation code which automatically generates the input file, while meeting the format of the input data, has been developed to save time for thermal modeling. The flow chart of the code is shown in Figure 8.

4.2 Plate Modeling

The method of plate modeling is to conduct the modeling by assuming any equipment as two-dimensional plate. In this paper, the plate modeling was limitedly used for the printed circuit boards (including page frame) which the parts are located actually as heat sources, and other elements are analyzed by the nodal network modeling.

5. Thermal Analysis for KOMPSAT-1 SAR

In this paper, the thermal analysis at the component and board level has been performed using TAS (Thermal Analysis System) code. Prior to the calculation of temperature at each nodes, TAS converts the entire thermal modeling, consisting of thermal resistance, plate modeling, radiation, etc., into the form of nodal network. TAS is implementing the finite difference method to compute temperature distribution at steady state of energy balance.

5.1 SAR Characteristics

The KOMPSAT-1 Solar Array Regulator (SAR) consists of four PCBs and housing. Two PCBs are operating boards and other two PCBs are redundant boards. Thermal modeling should be performed only for two primary PCBs and housing. Two PCBs are ARM Converter board and ARM Control board; the ARM Converter board is directly attached to page frame, while the ARM Control board is mounted and supported by spacer in the upper side of the Converter board. The SAR thermal dissipation is relatively higher than other electronic components, whose parts layout is also complicated. In addition, the fact that the individual parts form multiple heat path is required to be considered for thermal modeling.

5.2 Node Division

The entire unit has been divided into 236 nodes; 91 nodes for ARM Converter board and ARM Control board, respectively, 4 nodes for OM6051 transistors, 1 node for 1N6306R diodes, 48 nodes for housing, and 1 node for the spacecraft mounting surface. Nodes divisions are shown in Figure 9 (a) and (b) for ARM Converter board and ARM Control board, respectively.

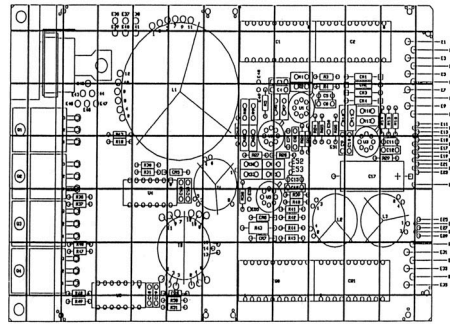


Figure 9 (a). Node Division of ARM Converter Board

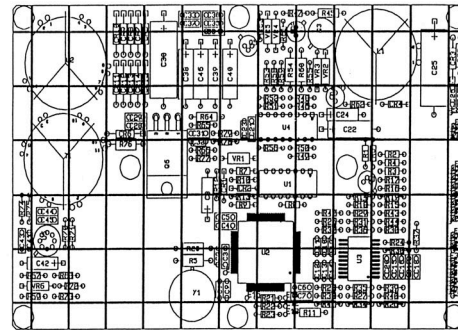


Figure 9 (b). Node Division of ARM Control Board

5.3 Nodal Network Modeling Results

From the analysis results of the nodal network modeling, it was obtained that the maximum temperature of ARM Converter board is 84.2 C at node 41 and that of ARM Control board is 81.1 C at node 145. The maximum temperature on the ARM Converter board appeared near the inductor coil. The temperature contour which resulted from the thermal analysis is shown in Figure 10. Figure 10(a) is a temperature contour for ARM Converter board which the temperatures of transistors and diodes are not included. Since transistors and diodes are defined as separate nodes in the thermal modeling, the temperature increases impact on temperature distribution and are not reflected in the temperature contour. Actually, the temperature of transistors and diodes is relatively high as illustrated in Table 1.

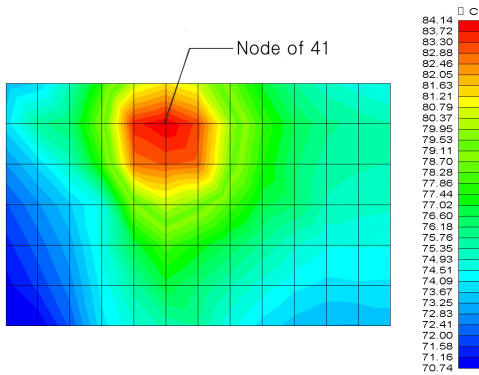


Figure 10 (a). Temperature Contour of ARM Converter Board (Nodal Network Modeling)

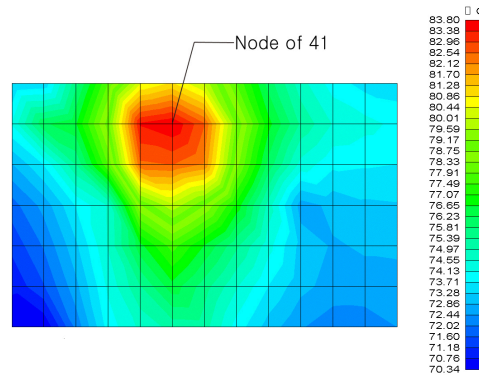


Figure 11 (a). Temperature Contour of ARM Converter Board (Plate Modeling)

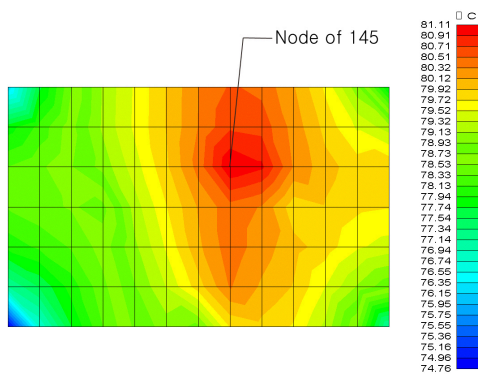


Figure 10 (b). Temperature Contour of ARM Control Board (Nodal Network Modeling)

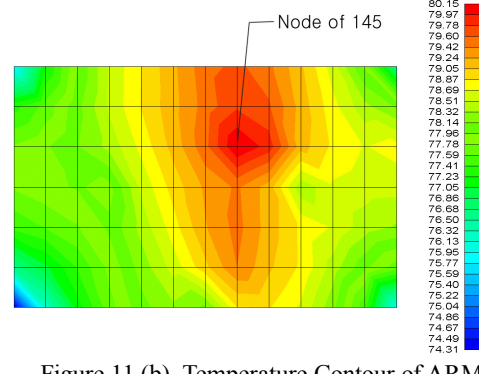


Figure 11 (b). Temperature Contour of ARM Control Board (Plate Modeling)

Table 1. Temperature of Diode and Transistors (Node Network Modeling)

Node	Temp. [°C]	Remark
231	103.44	Diode
232	77.61	Transistor
233	76.59	□
234	76.04	□
235	75.53	□

Table 2. Temperature of Diode and Transistors (Plate Modeling)

Node	Temp. [°C]	Remark
231	103.98	Diode
232	77.57	Transistor
233	76.45	□
234	75.91	□
235	75.41	□

5.4 Plate Modeling Results

From the analysis results of the plate modeling, the similar results were obtained as nodal network modeling, in which the maximum temperature of ARM Converter board is 83.8 C at node 41 and that of ARM Control board is 80.2 C at node 145. In the plate modeling, the maximum temperature on the ARM Converter board appeared near the inductor coil as well. The temperature contour which resulted from the thermal analysis is shown in Figure 11. Like nodal network modeling, the temperature of diodes and transistors is not included in this figure. The temperature at diodes and transistors is represented in Table 2.

5.5 Comparison of Thermal Analysis Results

Since there is no thermal test data of KOMPSAT-1 Solar Array Regulator at the board level, the current thermal analysis results were compared with the SAR's manufacturer's thermal data. Table 3 presents the comparison of thermal analysis results between nodal network modeling and plate modeling at several different nodes. It can be concluded that the difference of thermal analysis results between two modeling is almost negligible. Since thermal resistance is calculated after simplifying the heat path between node and node in the nodal network modeling, this modeling can be easily applicable to complex configuration. In this study, it is found that the computation time of nodal network modeling is shorter than that of plating modeling. Error

correction is much easier in nodal network modeling by just modifying the corresponding nodes or thermal resistance values when errors are occurred or the design of electronic equipment is changed. The problem that it takes long time to do thermal modeling, which is a unique defect of nodal network modeling, was resolved by using the input file format transformation code developed. The plate modeling can be easily applicable to the plane such as PCB or housing and it does not take long time to perform the modeling. However, since this method cannot be applicable to frame or contact area, the nodal network modeling should be implemented in this case. In the plate modeling, error correction is accomplished by converting the contents of modeling into the text form because it is very difficult to directly acknowledge those errors.

Table 3. Temperature of Principal Nodes

Node	Temp. when Nodal Network Modeling [□]	Temp. when Plate Modeling [□]
41	84.15	83.80
145	81.11	80.15
231	103.44	103.98
232	77.61	77.57
233	76.59	76.45
234	76.04	75.91
235	75.53	75.41

Table 4 represents the comparison of the difference between two modeling. The nodal network modeling is preferable to plate modeling from the viewpoint of debugging in the case of complicated electronic equipment like SAR. On the other hand, the plating modeling is estimated to be more effective in the form of plate like PCB.

Table 4. Comparison of Node Network Modeling and Plate Modeling

Nodal Network Modeling	Plate Modeling
Advantages : - can be used for complex configuration - reduced computation time - easier debugging	Advantages : - short modeling time - easily applicable to the plate
Disadvantages : - long modeling time	Disadvantages : - difficult to apply to complex configuration - difficult to debug

6. Thermal Analysis for KOMPSAT-2 SAR

6.1 Thermal Analyses

Since the power requirement for KOMPSAT-2 is increased over 850W, the capacity of SAR incorporated in KOMPSAT-1 is not enough for KOMPSAT-2. Korea Aerospace Industries (KAI) is currently developing high-capacity SAR. The power dissipation of SAR is increased from 26.5W to 56.9W. Excessive heat load was expected on some EEE parts of SAR such as high heat-dissipated diodes, transistors, and inductors. Therefore, the methods for the mitigation of heat load are required; design change of housing or layout change of high power parts.

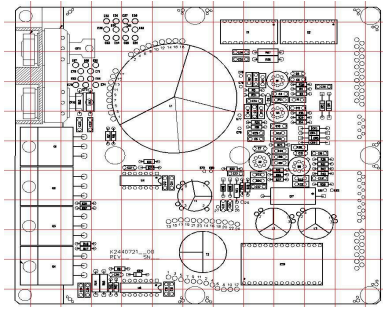


Figure 12 (a). Node Division of ARM Converter Board

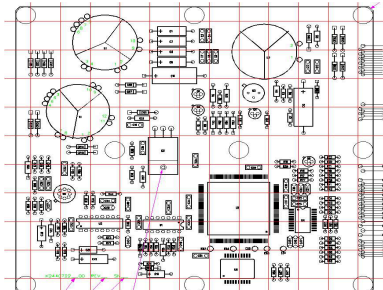


Figure 12 (b). Node Division of ARM Control Board

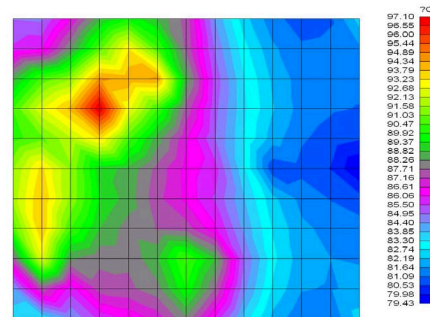


Figure 13 (a). Temperature Contour of ARM Converter Board

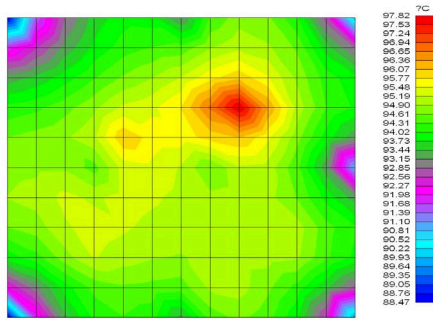


Figure 13 (b). Temperature Contour of ARM Control Board

Figure 12 (a) and (b) shows the boards layout being developed. Figure 13 (a) and (b) illustrates the thermal analysis results for individual boards, for which the nodal network modeling has been implemented.

In Figure 13, the temperature distribution was obtained between 80°C and 97°C in ARM Converter board and between 85°C and 97°C in ARM Control board. The number of power diode was increased from one for KOMPSAT-1 to two for KOMPSAT-2. The power dissipation of each of four power transistors has been increased from 2.4W to 6.3W, which caused high temperature. Table 5 presents thermal analysis results at diodes and transistors.

Table 5. Temperature of Diodes and Transistors

Node	Temp. [°C]	Remark
287	99.96	Transistor
288	103.17	
289	104.31	
290	103.87	
291	121.87	Diode
292	119.92	

6.2 Mitigation of Heat Load

Since high heat dissipation illustrated in Table 5 reduces the efficiencies of EEE parts and reliability, and leads to mission failure. It is necessary to mitigate the thermal loads. One of the methods is to increase the housing thickness, which is one of the heat paths, in order to increase the heat transfer rate. The other method is to increase the mounting surface area by extending the housing length. Figure 14 shows the relationship between housing thickness and temperature distribution. The relationship between temperature distribution and housing length is obtained in Figure 15.

In Figure 14, it was found that the temperature was decreased by 10°C when the housing thickness is increased from 0.15 inch to 0.3 inch. It is obtained that the housing thickness is more

sensitive to temperature variations than housing length. This kind of design change can impact on system level requirements.

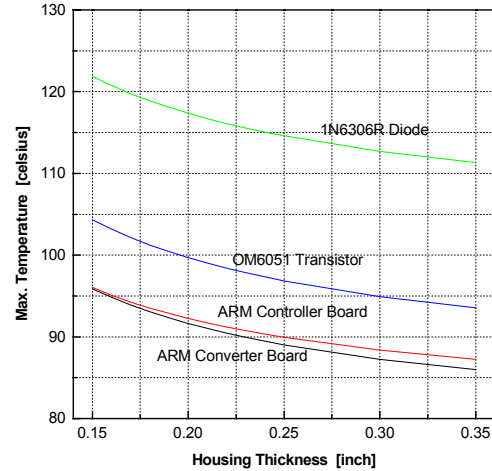


Figure 14. Housing Thickness vs. Temperature

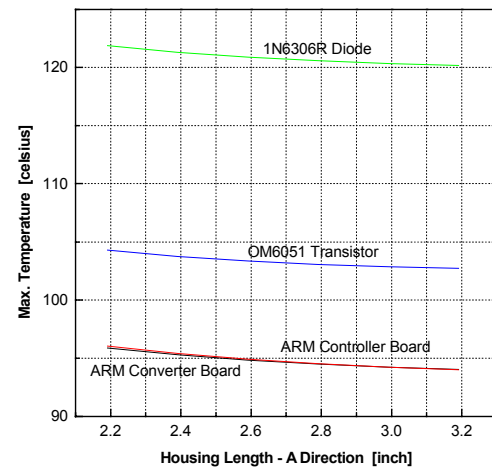


Figure 15. Housing Length (1-Direction) vs. Temperature

7. Conclusion

The numerical thermal analysis and thermal test are necessary for satellite thermal design. The thermal analysis should be verified through thermal test results. Also, thermal test should be conducted based on numerical thermal analyses.

It was found that the method of nodal network modeling is preferable to plate modeling from the viewpoint of debugging. The plating modeling is suitable to electronic equipment, which has a simple configuration and constitutes the form of plate, such as KOMPSAT On-Board Computer

and EPS Control Unit.

Excessive heat load was expected on some EEE parts of SAR such as high heat-dissipated diodes, transistors, and inductors due to increased power requirements of KOMPSAT-2 satellite system. The methods for the mitigation of heat load were studied through the design change of housing or the layout change of high power parts. It was obtained that the temperature was decreased by 10° when the housing thickness is increased from 0.15 inch to 0.3 inch. It is also found that the housing thickness is more sensitive to temperature variations than housing length. This kind of design change can impact on system level requirements.

References

1. Robert Lyle, Pericles Stabekis, Robert Stroud, "Spacecraft Thermal Control", NASA SP-8105, May 1973.
2. D. Baker, D. C. Koehler, W. O. Fleckenstein, C. E. Roden, R. Sabia, Physical Design of Electronic Systems, Prentice-Hall, 1970.
3. Frank P. Incropera, David P. DeWitt, Fundamentals of Heat and Mass Transfer, John Wiley and sons, 1996
4. "KOMPSAT SAR Thermal Analysis", GULTON Data Systems, March 1996.
5. Michael Pecht, Handbook of Electronic Package Design, Marcel Dekker, Inc., New York, 1991.
6. TAS(Thermal Analysis System) User's Manual, Harvard Thermal Inc. April 2000.
7. Dave S. Steinberg, Cooling techniques for Electronic Equipment, John Wiley and Sons Inc., 1980.
8. David G. Gilmore, Mel Bello, Satellite Thermal Control Handbook, The Aerospace Corporation Press, 1994.