SSC00-V-7

Minimizing Risk Associated with Imaging Payloads: Lessons Learned from a CCD Experiment Gone Awry^

^ Portions of this work were sponsored by the Space Vehicles Directorate, Air Force Research Laboratory, Kirtland Air Force Base, Albuquerque NM.

***Todd W. Goforth, +Scott R. Cannon**

*Maxwell Technologies, Alb., NM. goforthT@maxwell.com

+Utah State University, Logan, UT. scott@cannon.cs.usu.edu

ABSTRACT. The number of uses for imaging devices in space is rapidly increasing. To evaluate suitability for space-based surveillance and star tracker operation, an experimental payload was developed based on an experimental Charge Coupled imaging Device (CCD). This payload was to have flown on the small STRV-1d satellite (a joint US and British program) to collect data during 600+ minute highly elliptical orbits. These orbits were intended to expose the CCD to high radiation levels and possibly significant solar flare events. The main objective of the experiment was to measure the degradation of the Charge Transfer Efficiency (CTE) of the device, and to characterize its overall performance in an orbit that would provide a significant radiation threat. Due to the inherent complexities and fragility of experimental CCD devices, many hardware and software obstacles were encountered and many lessons were learned. Vibration and environmental testing issues were of particular significance. By underestimating the difficulty of mechanical mounting, cooling, software operation and clocking, and environmental stability, our project did not make satellite integration deadlines despite considerable effort.

Introduction

Designing hardware for application in space presents many challenges. These challenges include parts selection, meeting the project goals while observing power, mass, and volume constraints, and designing the hardware robustly enough to survive rigorous environmental qualification testing. Designing hardware to support an imaging payload for space presents not only the challenges mentioned above, but also an additional, unique set of challenges.

Experience facing many of these unique challenges was gained during the design and integration of an experimental imaging payload for the joint US/UK Space Test Research Vehicle satellite, STRV-1d[1]. The STRV-1d satellite, which will be launched with the STRV-1c companion spacecraft in autumn 2000, will be placed into highly elliptical orbits where they will pass in and out of the Van Allen radiation belts every 10.5 hours during their one-year mission. Aboard this satellite will be a palletized ensemble of experiments called the Electronics TestBed (ETB). In our effort to design this experimental imaging payload for the ETB many obstacles were encountered and most were overcome. But despite considerable effort the project did not meet the satellite integration deadline and it was subsequently de-manifested from the mission.

This paper addresses some of the challenges which our design team faced by relating first hand experience. It is our hope that these experiences will help other experimental imaging payload designers better prepare for these obstacles.

Experiment Goals

A continuing concern in the development of electronic designs for space is the effect of the synergistic radiation environment on new forms of electronics and sensor technologies. Experimental opportunities to evaluate on-orbit performance are rare, and few payloads have been assembled to respond to quick-turn investigative needs for combined radiation effects environments. The STRV series of satellites, however, created the opportunity for the demonstration of space

experiments in harsh radiation environments. The STRV-1d orbit profile, combined with BMDO (Ballistic Missile Defense Organization) involvement in the project, provided an excellent opportunity to evaluate a particular CCD device in an environment that was of interest.

The main goal of flying an imaging experiment on the STRV-1d satellite was to evaluate the operation of a particular 516 x 512 CCD in space in support of BMDO radiation hardened visible sensor/star-tracker needs. The CCD experiment parameters to be measured included power supply current draw, dark current, output offset voltage, output noise, optical responsivity, and charge transfer efficiency. The parametric data taken by the experiment while on orbit would be used to evaluate the usefulness of the CCD in future space applications.

Funding for the development of this payload was provided by the Space Vehicles Directorate of the Air Force Research Laboratory, and by Maxwell Technologies, Inc.

Experiment Description

This experiment is intended to operate as a sort of flying laboratory bench, with a charge coupled device as the central Device Under Test (DUT). The experiment board was designed to contain all of the hardware and software necessary to stimulate and exercise the DUT to produce enough data to properly characterize its performance. The flight circuit board is shown in figures 1 and 2, and each functional section of the board is described in the paragraphs that follow.

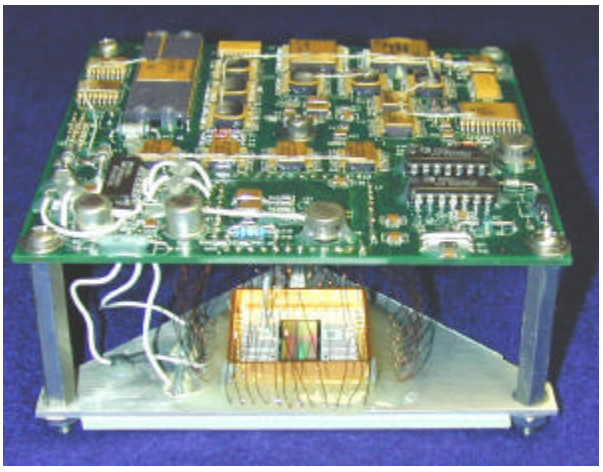

Figure 1. Top View of the CCD Experiment Board

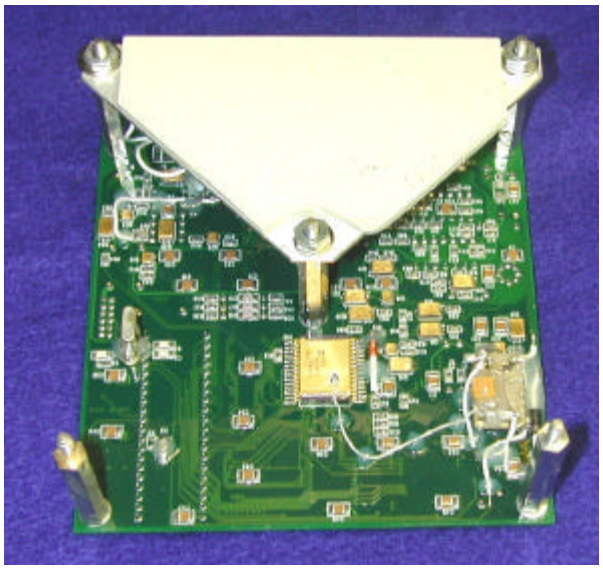

Figure 2. Bottom View of the CCD Experiment Board

Basic Operation of the Device Under Test

The DUT used on this experiment is the CCID-22. This device is manufactured by MIT Lincoln Labs. The CCID-22 is a 516x512 array containing both an imaging array and a frame store array. The block diagram for this part is shown in Figure 3. The CCID-22 that was used for the development of this experiment included a light shield that covered all of the pixels except for six small windows of 3 x 3 pixels.

In operation, the Input Array (IA) is clocked one line at a time into the Frame Store (FS), which is clocked to the serial output register. The serial output register is then clocked to transfer the data to the output. The CCID-22 has duplicated connections to facilitate operation of both a left (L) and right (R) side.

In addition to the right and left side inputs, there are also two outputs, one for each side. In normal operation, all of the pixel signals from one side of the array go out one output, while the other half go out the other. However, it is also possible to change the clocking scheme so that all of the pixel signals go out only one output. This is the operating mode that was selected for use on this experiment.

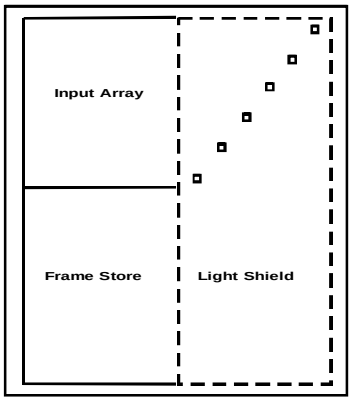

Figure 3. Block Diagram of the CCID-22

It is important to note that the CCID-22 is a "bare" CCD. This means that the part has a CCD array structure capable of transferring charge between pixels in an ordered fashion, but has no biases or clocks generated on-chip. For this reason all of the correct signals necessary for orderly transfer of charge were generated on the experiment board by using hardware dedicated to these tasks. The only non-CCD devices within the CCID-22 are an on-chip MOSFET voltage follower and an off-chip JFET voltage follower for each output. Because of the inherent complexities associated with the DUT a description is given of the major operational sections of the CCID-22 in the paragraphs that follow.

DC Biases

There are five distinct DC biases to the CCID-22. The voltage values chosen for each of the biases was determined through a series of bench tests. These bench tests evaluated the performance of the DUT using automated test equipment, while changing the combinations of bias voltages. Because changes in some bias voltage value produced changes in DUT performance, these trade-offs were weighed before final bias voltage values were selected [1].

The various substrate pins are all connected to ground. The RET-R and RET-L pins, which are the return lines for the output voltage followers, were also tied to ground.

[1] For more information concerning bench test data please contact the author

Clocking

The clocking to the DUT can be broken down into two distinct types: the parallel clocking which shifts one entire line of pixels in the input array or the frame store array, and the serial clocking which shifts single pixels towards the outputs.

Since the clocking for the input and frame store arrays are independent, the CCID-22 can be operated in several ways. The simplest, which is the clocking scheme used for the STRV-1d experiment board, is to use identical clocking for both arrays. This simultaneously shifts the entire array of pixels, both the input and frame store arrays, down by one line per clock cycle. Figure 4 depicts the relative timing of the three signals used for the parallel clocking of this part.

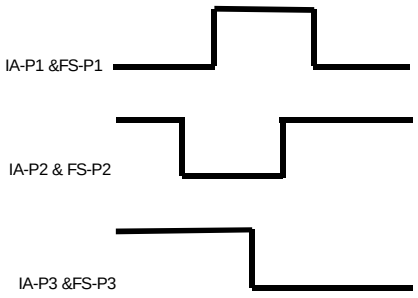

Figure 4. Diagram of Parallel Timing Waveforms

Bench testing showed that the clock levels required for the serial clocks were not especially sensitive. The low voltage rail needed to be less than 0.0V and the high voltage rail should be above the Output Gate (OG) voltage. Bench testing also showed that changing the high voltage from +4 to +6 volts and the low voltage from –7 to –5 volts appeared to have very little effect on the output signal.

Three clock sequences are required before the first signal associated with the first illuminated pixel appears at the output. In addition to the three clock sequences needed for a CCD transfer, the serial clocking also requires the Read Gate (RG) to be clocked. This clock is involved in transferring the charge between the CCD structure and the output stage. The relative timing of the various serial clocks is shown in Figure 5.

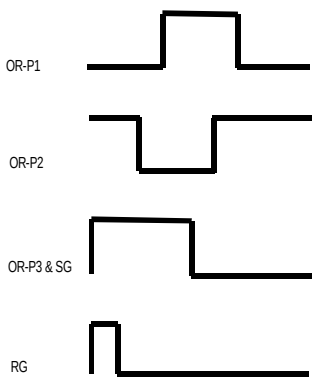

Figure 5. Diagram of Serial Timing Waveforms

Note that these clock patterns are what would be used if it were desired to clock data out through *two* outputs. In order to send all of the data out one output, as was done on this experiment board, the P1 and P2 clocks were switched. Therefore, to send all of the pixel data out of the left output, P1-OR-R was fed the OR-P2 signal shown above, and P2-OR-R was fed the OR-P1 signal shown above. The OR-P3 and RG signals remain the same for both inputs.

Although not found to be especially sensitive, the selection of the clock rails voltages for the serial clocks was found to be more critical than for the parallel clocks. Also, the low clock rail voltage appeared to be more critical than the high rail voltage. Changing the low rail voltage produced a significant effect on the well capacity, which controls the maximum output voltage swing of the device. Testing showed that the OG bias voltage must be between the serial clock high and low rail voltage. Setting the serial clocks to go between 0V and +10 volts and the OG voltage at about +2V seemed to give the largest well capacity and the best immunity to changes in any of the voltages.

The rail voltages of the RG clock did not seem to have much effect on the CCD performance as long as the low rail was less than +2 volts and the high rail greater than +8 volts. The rails of this clock were also set to go from 0V to +10 volts.

Integration time clocking and light source

When the DUT is integrating optical signal, it should be continuously given serial clocking and no parallel clocking. The reason for performing serial clocking is that the serial output array of the chip can also accumulate charge. Continuously applying serial clocks removes charge from the DUT, avoiding the possibility of this charge spilling over into another part of the chip if saturation occurs. Since no data is being read during this time, this clock rate is not critical.

Ideally, there should be no illumination of the DUT while performing any parallel clocking to transfer the pixel data off the chip. Since clocking the data out can take a significant amount of time (several seconds), if the DUT is illuminated, the later pixels can still be accumulating charge from the light source after the first pixels already have been read. This will cause an apparent slope in intensity across the chip even if the illumination is uniform.

Output Bias and Signal Characteristics

Using the biasing described above, the output signal from the DUT, without any optical signal input, was approximately +16 volts. Since the output transistor used on this device has a VGS(off) which can vary by as much as three volts, the output voltage from the DUT can also vary by as much as three volts.

The clock timing during DUT readout proved to be very critical. Testing showed that the DUT output voltage could change significantly with minor changes in clock rate. It is believed that the majority of this change is due to leakage currents, which are integrated at all times during the process. To compensate for this, the DUT pixels were read out as rapidly as possible. And even more importantly, the timing was kept as constant as possible.

Experiment Hardware

The experiment hardware can be divided into several sub-sections. Each sub-section performs a specific function and is necessary for the production of DUT characterization data. Each of the major hardware sub-sections is described below.

CCD Bias Voltage Generation Circuitry

As described in a previous section, the CCID-22 requires five separate bias voltages, including ground, for proper operation. The non-zero voltages, +18V, +12V, and +2V were generated from the +15V and +5V feeds that were provided to the experiment board. Using linear voltage regulators and some associated circuitry easily generated the +12V and +2V supplies. The +18V supply was generated from the +5V and +15V supplies by using a voltage multiplier circuit. The output of the voltage multiplier circuit was then feed into a linear voltage regulator circuit.

Each of the bias voltage generating circuits included a

current and a voltage monitoring circuit. The outputs of these circuits were fed to the main instrumentation circuitry in order to provide indications of the voltage stability and the CCD power consumption during operation.

Bench testing had shown that the stability of the +18V DUT bias supply was critical, and the design that was finally chosen worked out very well. Our tests indicated that the +18V supply circuit had a drift of less than 5mV, even while sourceing a load current 10X greater than would be drawn by the DUT.

CCD Clock Generation Circuitry

As was previously described, the CCID-22 requires clocks which shifts data in both a serial and parallel fashion. The experiment circuitry generates a total of six parallel clocks and five serial clocks. The parallel clocks range in voltage from –6V to +5V, while the serial clocks range in voltage from 0V to +10V. Generating the clock voltage rails did present somewhat of a challenge. Eventually, a suitable clock driver was found which was available in a radiation tolerant version, and would allow the use of non-symmetrical bipolar voltage supplies. This feature was essential for generating the clock voltage levels necessary to drive the DUT.

CCD Temperature Control Circuitry

In order to maintain the DUT within at an acceptable temperature range a temperature control circuit had to be designed. A scheme was eventually devised which used a Thermo-Electric Cooler (TEC) and several RTDs Resistive Temperature Detectors (RTDs) as the active and feedback elements of the circuit. A control circuit was used, roughly approximating a Proportional-Integrating (PI) controller, in order to drive the TEC to either the cooling or heating mode. One of the RTDs was used as a feedback sensor to drive the control loop. This RTD was bonded inside the DUT package, and provided a very accurate indication of DUT temperature.

Digital Control Circuitry

The experiment board is controlled by an 8-bit microcontroller, the SNL SA3865[2]. This microcontroller is a radiation tolerant version of the Intel 80C51BH. The microcontroller orchastrates all of the experiment board operations based on stored schedules, generates the raw clocks for the DUT, controls the instrumentation circuitry gains and offsets, and handles all of the data transfers to and from the experiment board. The SA3865 operates out of an 8K x 8 instruction memory, and uses a 32K x 8 data memory for characterization data storage.

CCD Stimulus Circuitry

In order to stimulate the DUT a light source had to be chosen. The source which was eventually selected was an incandescent bulb. Two bulbs were used on the experiment board. On one of the sources the glass envelope was removed. It was intended that the source with no envelope would be used as the stimulation source in orbit and also during vacuum testing, while the source with the envelope would be used during ground testing. This scheme was chosen because it was suspected that the glass envelope could create reflections which would lead to erroneous and unreproducable results in the DUT responsivity data. It was also our belief that the total ionizing dose associated with the STRV-1d orbit would likely cause some discoloration of the envelope which would change the bulb characteristics.

The light sources were mounted on the underside of the experiment board, directly above the DUT (refer to figure 2). Although the use of these light sources appeared to be very straight forward during the early stages of the design effort, they would later present various problems which are discussed in another section of this paper.

Instrumentation Circuitry

An on-board instrumentation system was developed which captured and digitized all of the experiment data. This circuitry consisted of various stages of signal conditioning electronics, a Digital to Analog Converter (DAC), and an Analog to Digital Converter (ADC). An 8-bit ADC was available for the design, but the measurements required 12-bit accuracy. The individual signal conditioning circuits consisted mainly of amplifiers and buffers. The DAC circuit was used to add a variable DC offset to the signals which are applied to the ADC, in order to bring these siganls into range of the measureing circuit and to increase its overall resolution. Using a variable offset scheme was necessary due to the large amount of variation in the amplitude of the signals being measured, but also presented several new challenges which had to be overcome. The most serious of these challenges was ensureing that DUT measurements were completed before the signal decayed to the point that it was no

[2] Sandia National Laboratories, P.O. Box 5800, Albuquerque, NM 87185 (505)844-4470
Point of Contact - Mr. Henry White.

longer valid.

Experiment Software

To minimize and simplify hardware design, all clocking signals, ADC sampling, and DAC bias were accomplished using digital output ports of the experiment microcontroller.

Challenges Faced during Development of the Experiment

The design and testing of this space experiment presented many challenges which had not been faced by the development team before. The majority of these challenges were directly related to the fact that the experiment was an *imaging* experiment and therefore required special attention in areas which weren't an issue on other projects. Although the AFRL/Maxwell/USU team has successfully designed and integrated many space experiment boards in the past, none of them can be classified as an imaging experiment, and none presented the kinds of challenges that were experienced during the development of this particular experiment.

The majority of the problems that the team faced can be put into one of five catagories. Each of these catagories is addressed in a separate sub-section below.

Making Software Timing Deterministic

Stable clocks and bias voltages for the DUT were essential. The DUT proved to be extremely sensitive to the stability and timing of the sequential and parallel clocks probably due to leakage and integration variations. A considerable effort was expended on this problem and satisfactory results were not obtained until the software functions responsible for these operations became completely deterministic.

All decisions had to be postponed and a single deterministic software execution path generated during sequential and parallel clocking. Image acquisition proved to be less sensitive, but we found that the time needed to find the correct bias voltage to bring pixel measurements within the 8-bit ADC range had to be padded so that each pixel measurement required the same time.

A consistent and stable time between images also proved necessary. To provide the level of accuracy needed for consistent image calibration testing, the software slack associated with a real-time scheduling monitor had to be eliminated. The final software had to be written without library or scheduler support. In all, this trial-and-test software development proved time consuming.

Providing Stable Clocks and Bias Voltages for the CCD

Bench testing of the DUT showed that a slight shift in clock rail voltage of a specific clock could produce a profound effect on the responsivity of the DUT. Yet, large variations of the voltage rails of other clocks produced very little change in responsivity.

A clock driver chip was eventually identified which would allow the use of separate voltage supplies to bias the chip inputs and the chip outputs, and was available in a radiation tolerant version. This allowed us to feed TTL level clocks into the part, clocks that were generated by the SA3865, while biasing the output to produce the necessary voltage rail levels.

Generating stable bias voltages for the DUT, for the most part, was simply an exercise of careful parts selection. The one exception to this was the generation of the +18V DUT supply. The value of this bias supply was critical because it determined the DC offset point of the DUT output voltage, and given the fact that the voltage feeds to the experiment board were +5V, and +/- 15V, a scheme needed to be devised which would produce the +18V bias supply from a combination of the voltage feeds to the experiment board.

Several schemes for generating this bias voltage were considered and rejected. The use of a standard switching converter was rejected because the project power budget would not allow it and it would likely create excursions on the power and ground planes which would disturb the measuring circuitry. A scheme in which the DUT power and ground rails were offset could not be employed because it complicated the clocking voltage levels, and produced a problem similar to the original one. The scheme which was eventually chosen to generate the +18V bias for the DUT involved the use of a voltage multiplier. The time varying source originally chosen for this circuit was the crystal feeding the SA3865, the frequency of which is 11.059MHz. After experiencing several multiplier circuit failures it was determined that this frequency source was not stable enough during its transition through the logic level crossover point. This instability was causing the circuit to oscillate and to eventually fail. The multiplier frequency source was replaced with a dedicated 2MHz oscillator that produced a very stable, reliable +18V DUT bias voltage.

Creating a Stable Thermal environment for the CCD

Creating a stable thermal environment for the DUT was critical for this experiment. The target temperature, based on future application goals and on the design of the CCID-22, was chosen to be 263K. Our design goals also called for maintaining this target temperature to +/-3K.

In order to heat and cool the DUT a thermo-electric cooler was chosen as the active element. Although theoretical calculations showed that a TEC would provide enough heating and cooling capacity to achieve our temperature control goals, there were other issues which needed to be verified empirically. Several of these issues are discussed in more detail in the paragraphs that follow.

Issues Associated With Providing an Adequate Thermal Sink

In order to stabilize the temperature of the DUT in as short a time period as possible, an adequate thermal sink was necessary. It was also very important that the thermal energy not be transferred to the experiment board in a manner that would affect the operation of the other experiment circuitry. For these reasons, as well as others, the decision was made to mount the DUT on a separate substrate below the main circuit board (refer to figure 1). In this configuration the bottom of the DUT was bonded to the top of the TEC using a thermally conductive epoxy. The bottom of the TEC was then bonded to an aluminum plate using the same epoxy. Sandwiched between the aluminum plate and the spacecraft chassis was a thin sheet of thermally conductive material that would be used to transfer the thermal energy away from the DUT. To help ensure that the DUT was thermally isolated from the rest of the experiment circuitry, 40 AWG manganin wire was used to electrically connect the DUT to the experiment board. Although this configuration initially appeared to be an acceptable solution for thermal issues, vibration testing (discussed below) proved it was not.

Issues Associated with the Selection of Critical Components

Selection of the components that controlled the DUT target temperature and which instrumented the monitoring of the actual DUT temperature turned out to be a more difficult task than was anticipated. Because RTDs were used for both functions, the circuit performance was directly proportional to the stability of the current sources that were used to drive them. Unfortunately, the original components chosen for this job did not perform as well as expected. In fact, these components had a pronounced negative temperature coefficient that caused the DUT target temperature to continuously change. The problem was eventually solved by replacing the original components with devices that exhibited a flat response over the temperature range that the experiment would be exposed to. Consequently, schedule slips were forced while the problem was investigated and the new components were identified, procured, and installed.

Selection of a Proper CCD Illumination Source

As mentioned in a previous section of this paper, incandescent bulbs were used as the DUT stimulus sources. The decision to use these bulbs was based on the fact that they would not degrade with total dose radiation, and would therefore, for the purposes of this experiment, not need to be calibrated. Although this is a valid argument, the use of these bulbs as DUT illumination sources presented enough problems that a more thorough search for a better source could have been justified. Some of the problems associated with the use of these bulbs are discussed in the paragraphs that follow.

Illumination Source Stability

In order for the DUT responsivity to be accurate and reproducible, the illumination sources needed to be as stable as possible. Unfortunately, several factors were at work that reduced the effectiveness of these bulbs.

The bulb circuitry was designed to use the +5V feed as the sole power source. This voltage source was also used to drive the TEC during DUT cooling phases. Because the cooling phase required approximately four times as much current from the supply as was needed for other phases of operation, and because the power and ground leads supplied to the experiment had resistances of approximately 0.50 Ohms, rather large IR drops were seen in the +5V supply lines. These IR drops caused the voltage at the illumination sources to sag, thereby causing the amount of signal felt by the DUT to fluctuate. It is now clear that this problem could have easily been remedied by supplying the bulbs with a regulated voltage source. This would have helped the illumination signal to remain stable regardless of fluctuations in the voltage or ground feeds to the board.

The incandescent bulbs, even though they were designed to be low power low illumination sources, were simply too bright for this application. This forced us to operate the bulbs in a non-linear portion of their operating curve. To compensate for this the circuits

driving the bulbs had to be very carefully adjusted in order to produce an amount of light that would put the DUT output into a usable region. Testing showed that the difference between the DUT not putting out a measurable amount of signal and being completely saturated was an adjustment of a particular current limiting resistor of less than 5%.

When properly adjusted, and in a controlled environment, the DUT response was very clear and very measurable. Figure 6 shows the response of a particular row of pixels in a particular window. The response of the pixels at either end of the window is weaker due to the edges of the light shield casting shadows on them.

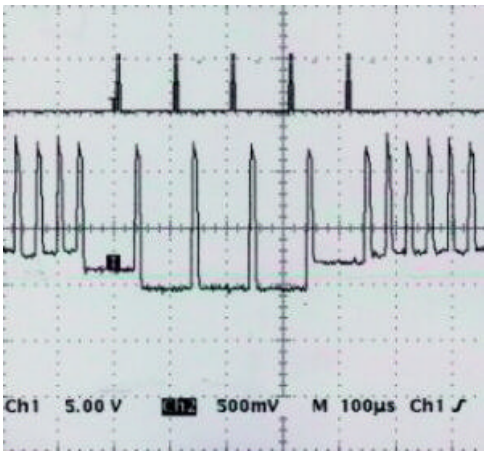

Figure 6. Oscilloscope Screen Image Showing a Typical Response for one Row of Pixels in one Window (Lower Trace) .

A three-dimensional plot of the relative response for an entire window that is properly illuminated is shown in figure 7.

Certainly more testing would have to be done before completely ruling out the use of incandescent bulbs as viable candidates for illumination sources in similar future experiments. But it is very clear that the use of these sources presents many problems that require special attention.

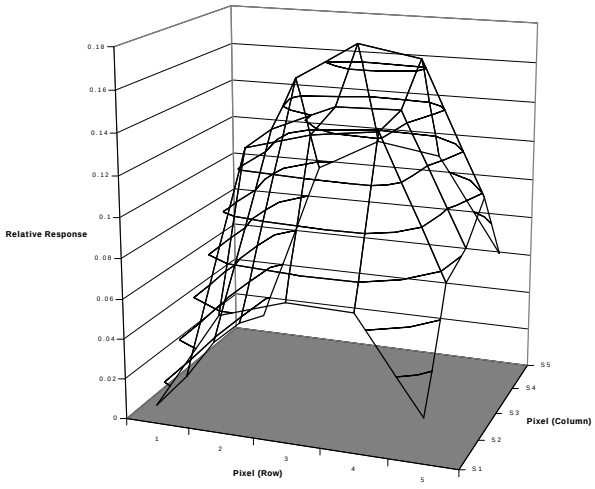

Figure 7. Relative Response for a typical Window of Pixels

Qualification Testing Challenges

The qualification-testing requirement for each of the ETB experiments was similar to that of other experimental payloads our team has designed in the past. It consisted of temperature cycling, vibration testing, bakeout, and thermal vacuum testing. Of all the challenges that contributed to the experiment missing the integration deadline, none had more impact than vibration testing. This testing exposed several major design flaws that caused slips in the delivery schedule, from which the experiment was never able to recover.

As discussed in a previous section of this paper, in order to thermally isolate the DUT from the rest of the thermal loads of the experiment it was located off of the board. The DUT electrical connections were made via 40 AWG manganin wire. It was understood that

using such fragile wire for these connections was a risk but it was believed that they would withstand the rigors of vibration testing. Unfortunately, they did not. The wires broke during the early stages of a vibration test and the testing was suspended pending board re-work.

In order to repair the DUT electrical connection wiring it was decided that the best option was to use a heavier gauge wire. Other options were considered, such as staking the wires at the board and at the DUT. This option did not appear to be attractive because it was feared that the staking compound would limit the transfer of thermal energy from the DUT. And because there wasn't enough margin left in our power budget to compensate for any new thermal resistances by simply driving the TEC harder, we settled for replacing the DUT connecting wire. Eventually we would learn that staking compound would be necessary, but at the time this solution seemed acceptable.

During the next attempt to vibration test the experiment more serious problems were encountered. During the random vibration portion of the testing the TEC structure failed. This failure caused the DUT to become completely detached from experiment. Figure 8 shows the bottom portion of the TEC still bonded to the aluminum heat sink, but the top of the TEC and the DUT have broken loose. This failure resulted in the complete destruction of the CCID-22. By the time a replacement part was procured the project had suffered a major slip in the delivery schedule.

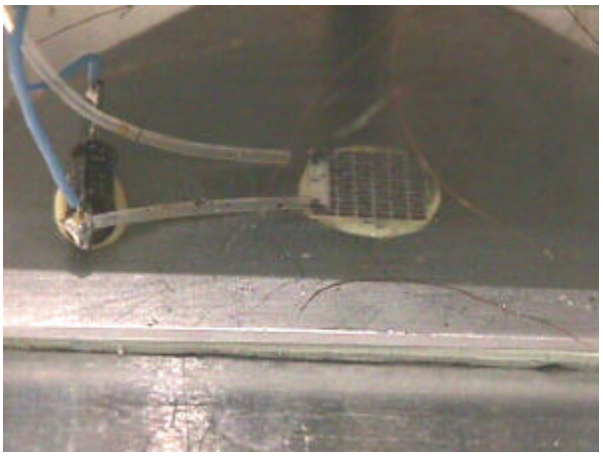

Figure 8. Image of Thermo-Electric Cooler Mechanical Failure

After the new DUT had been installed onto the experiment, preliminary testing was done to verify its proper operation (refer to figures 6 and 7), and the board was again readied for vibration testing. In order to prevent a repeat of the previous failure a bead of staking compound was used around the entire bottom edge of the DUT (this can be seen in figure 1). Although we had previously determined that using staking compound on the DUT would inhibit thermal transfer, at this point we had no choice but to use it. The ends of the manganin wires were also staked at the printed circuit board and at the DUT.

With the new staking in place the experiment passed the vibration testing, and all other environmental qualification tests that were required.
A conformal coating was then applied to the board. This coating was required of all ETB experiment boards, and its application had not caused any problems on any of the other boards. Once the conformal coating cured the board was tested again. The testing revealed that the DUT response was severely degraded. So much degradation had occurred that the DUT output was no longer in the usable range of the instrumentation circuitry. Over the course of a week or so testing was done to try to reveal the cause of the problem, yet none were found. With no clear indication as to the cause of the problem no new delivery date could be set. At this point in time the experiment's position on the ETB was forfeited to a back-up experiment that was ready to be integrated.

Although relatively little time was spent trying to determine the cause of the DUT degradation after the de-manifestation of the project, several possible causes have been considered. It is possible that during the conformal coating cure period a chemical film formed over the face of the DUT that prevented the illumination of the pixels. This could probably be confirmed by viewing the pixels under the light shield windows with an appropriate microscope. But because the DUT would have to be removed from the heat sink to do this, and because that would require the removal of the staking compound, this was never done.
Another possible cause of the problem could be that the conformal coating, which when cured became very shiny, was causing the light to be reflected back and forth between the DUT and the experiment board.
Another possibility is that bond wires on the DUT were broken during the application of the conformal coating. The coating was applied manually with a small brush similar to a common paintbrush. Although the DUT is located a few inches below the board it is possible that the brush made contact with the exposed bond wires and damaged them. This could also be confirmed by viewing the DUT under a microscope, but for the reasons mentioned above it was never removed from the experiment board.

While experiencing failures of space hardware during qualification testing is certainly not unique to imaging payloads, the failures that were experienced with this particular experiment were a direct result of the configuration and placement of the DUT. Decisions related to configuration and placement were made because of the special needs of the imaging device. These needs included strict temperature control, illumination issues, and the requirement for thermal isolation.

Summary

Designing hardware and software to support an imaging payload for space not only presents the traditional set of challenges, but it also presents a different, unique set of challenges. Of these unique challenges our project team found that issues of particular importance were the ones associated with software design and DUT timing, bias voltage and clock pulse generation, thermal stability and isolation, selection and control of the illumination source, and qualification testing.

Some of these issues, though not properly addressed at the conception of the program, were satisfactorly re-worked as they were discovered. These setbacks resulted in slips of the delivery schedule but were eventually corrected. Other issues, especially those associated with mechanical design, stress analysis, and vibration testing, were much more difficult to resolve. At the heart of these issues were decisions that were made early in the project concerning DUT configuration, DUT placement, and test methodology. Proper resolution of these problems would have required changes that could have only been successfully implemented during the conceptual stages of the project. It was these issues that eventually caused the experiment to miss the integration deadline.

If the opportunity to design and integrate a similar imaging experiment were to present itself in the future the experience that was gained from this evolution would be invaluable.

Acknowledgments

Acknowledgment is given to Mr. Jim Gregory, Mr. Michael Cooper, and Mr. Barry Burke (MIT Lincoln Laboratories), Mr. James Lyke, Mr. Franklin Roush, and Capt. Michael Dunn (U.S. Air Force Research Laboratory), Mr. Norman Anderson (Ball Aerospace), Dr. James Duffey, Mr. Thomas Bradley, Mr Charles Gilbert, and Mr. Michael Andersen (Maxwell Technologies, Inc.), and to Utah State University for providing technical support during the development of hardware and software related to this space experiment.

References

[i] Wells, Nigel. “STRV-1c & 1d Mission Definition Specification”, Phillips Laboratory technical report, July 1997.