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SCISAT-1 ACE Mission C&DH Unit Development

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Abstract. The SCISAT-1 Atmospheric Chemistry Experiment (ACE) Mission is a part of the Canadian Space Agency's (CSA's) space science program, to support ongoing research in the areas of solar-terrestrial relations, atmospheric sciences and space astronomy. Bristol Aerospace Limited is the CSA's Spacecraft Prime Contractor for the ACE Mission. The ACE spacecraft will be launched on a Pegasus XL vehicle in mid-2002, co-manifested with a NASA spacecraft.

A Control and Data Handling (C&DH) Unit is being developed by Bristol for the ACE Mission. This C&DH Unit will be responsible for all onboard command, control, monitoring and science data recording. This unit is being developed to support a range of Canadian small science missions, from Smallsats to Microsats. The unit is low power and light weight, and features a rad-tolerant core to assure reliable operation in a single string architecture. The C&DH Unit is comprised of a Controller Card (CC), Data Handling Card (DHC), Input/Output Card (IOC) and a Power Supply Card (PSC). Each card is housed in its own aluminum frame, and the frames are integrated into a vertical stack. The unit is expected to operate with 7 Watts orbit average power and uses a UTMC 80C196 16-bit processor running at 16 MHz to manage the satellite operations and perform attitude control. Mass storage of 1.5 Gbytes and CCSDS variable-rate telemetry up to 5 Mbits/sec are provided.

This paper will present an overview of the ACE Mission and a description of the C&DH Unit, describing its architecture, hardware/software partitioning, FPGA functionality and key performance specifications.

SCISAT Program Overview

The SCISAT-1 ACE Mission is being conducted under the auspices of the Canadian Space Agency's (CSA's) Space Science Program. The CSA provides opportunities for Canadian scientists to conduct experimentation from space in the fields of Earth Sciences, Space Astronomy, Space Exploration and Life Sciences. Selection of missions is done through an Announcement of Opportunity (AO) process, culminating in competitive selection of science teams through a peer review process. Preparation of the tools necessary to perform the research is accomplished through contracts to Canadian industry, including the science instrumentation, the spacecraft bus, and the associated ground control and data reception elements.

The SCISAT program is part of a collaboration between the CSA and the US National Aeronautics and Space Administration (NASA), consisting of two missions. Under the terms of the cooperative agreement, each agency will provide a spacecraft and instrumentation, to be co-launched on an expendable vehicle. Mass resources will be shared between the two spacecraft, and missions selected to be reasonably compatible in terms of orbit requirements and launch schedule. Following deployment of the spacecraft on-orbit, each agency will be responsible for their own flight operations.

Science Objectives

The principal goal of the ACE Mission is to measure and to understand the chemical and dynamical processes that control the distribution of ozone in the upper troposphere and stratosphere. Anthropogenic changes in atmospheric ozone are increasing the amount of ultraviolet radiation received at northern mid-latitudes and in the Arctic, and may affect the climate. A comprehensive set of simultaneous measurements of trace gases, thin clouds, aerosols and temperature will be made by solar occultation from low earth orbit (see Figure 1). The concentrations of more than 30 molecules will be measured as a function of altitude.

Measurements will be taken during solar occultation as the sun's light passes through the various layers of the atmosphere. As the satellite continues in its orbit the sun's light passes through an increasing number of layers until the earth eventually blocks the light. Measurement error must be low, because the concentrations measured for the outer layers must be used to quantify the concentrations of the inner layers.

Science Instruments
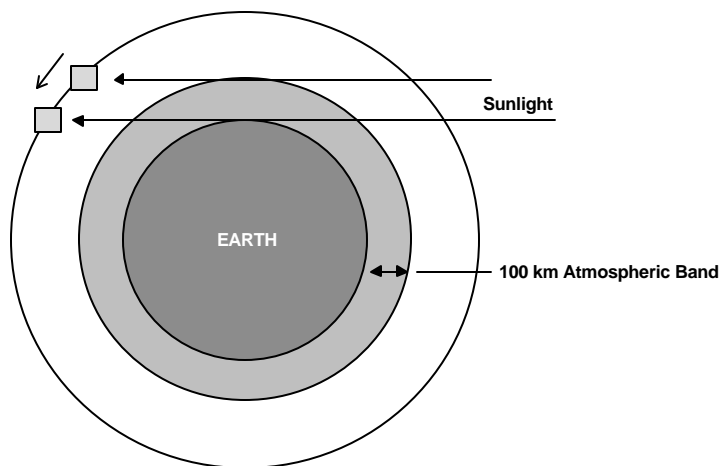
Figure 1 - Mission Operations Scenario

The ACE spacecraft will carry two scientific instruments; the Fourier Transform Spectrometer (ACE-FTS) instrument and the Measurements of Aerosol Extinction in the Stratosphere and Troposphere Retrieved by Occultation (MAESTRO) instrument.

ACE-FTS Instrument

A high resolution infrared Fourier Transform Spectrometer (FTS) operating from 2 to 14 microns will measure the vertical distribution of trace gases as well as the meteorological variables of pressure and temperature. During sunrise and sunset, the FTS measures infrared absorption spectra that contain information on different atmospheric layers. These spectra will be inverted on the ground to provide vertical profiles (3-4 km resolution) of atmospheric constituents. Temperature and pressure will be derived from the CO_2 lines. Aerosols and clouds will be monitored using the extinction of solar radiation at 1.02 and 0.525 microns as measured by two filtered CCD imagers and in the infrared by the FTS.

The FTS instrument is an infrared spectrometer with an auxiliary 2-channel visible / near infrared (IR) imager. The instrument includes a suntracker, which provides the sun radiance to both the infrared spectrometer and the visible / near IR imager during solar occultation of the earth's atmosphere. During sunrises and sunsets, the instrument measures the visible and infrared signals that contain information on different atmospheric layers, which provides the vertical profiles of atmospheric components.

MAESTRO Instrument

MAESTRO is a UV/Vis array detector spectrometer designed to measure the attenuation of the solar beam through the atmosphere as viewed from the spacecraft at sunrise and sunset and make measurements of solar radiation scattered back into space from the surface of the earth and the earth's atmosphere. From these measurements in the wavelength range of 285-1000 nm at a resolution of 1-2 nm, scientific information about the aerosol and ozone profiles of the atmosphere can be deduced.

The MEASTRO shares a common sun input with the FTS and operates by using the same suntracker.

Spacecraft Design

SCISAT-1 will be the upper spacecraft of a two spacecraft launch by a Pegasus XL. Key spacecraft specifications are shown in Table 1 and a line drawing of the spacecraft is shown in Figure 2 Spacecraft Layout. The spacecraft will be designed for a 5-year life with the reliability specified at 2 years.
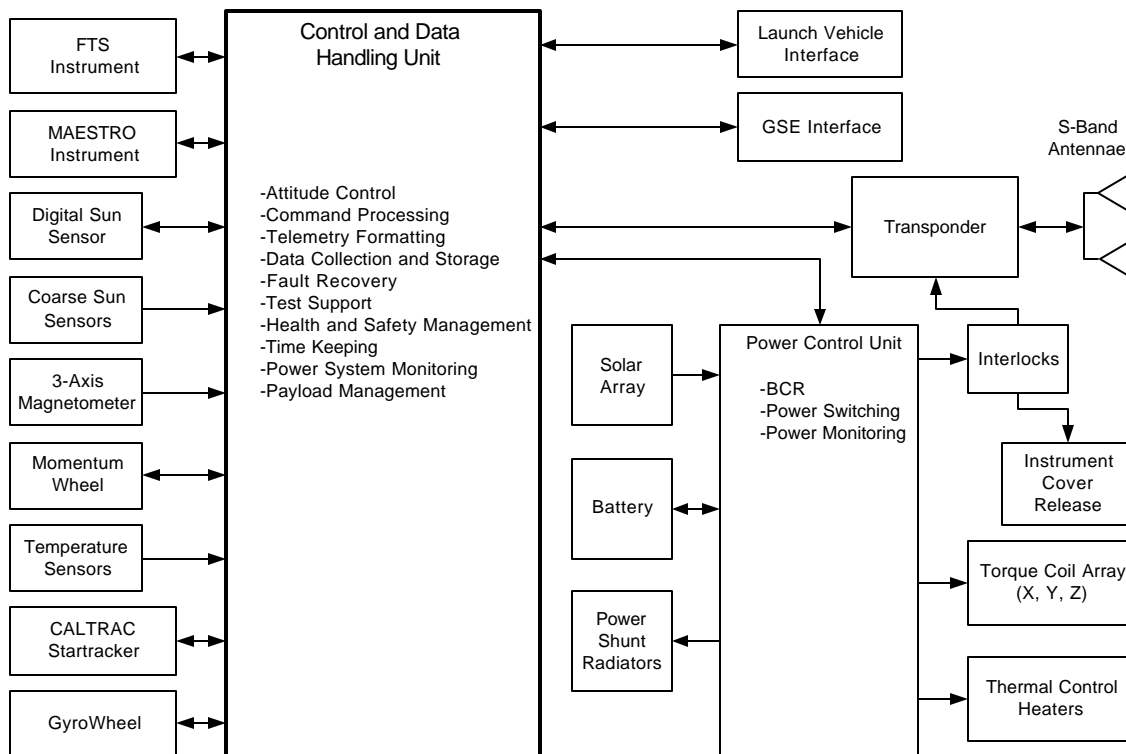
Spacecraft Architecture

The architecture of the spacecraft is shown in Figure 3 Spacecraft Architecture. To keep costs down, minimum equipment will be used. The system is essentially single-string with very few exceptions. Bristol's GyroWheel[TM] will be flown to validate this technology in the space environment. The GyroWheel[TM] has the ability to simultaneously provide the spacecraft with stored angular momentum, function as a 3-axis torque actuator, and measure the spacecraft's angular rates in two axes.

Table 1 Key Spacecraft Specifications

Parameter	Value	Units
Sun pointing accuracy	< 1	degrees
Orbit	circular	
Altitude	650	km
Inclination	74	degrees
Mass	< 140	kg
Satellite diameter	112	cm
Solar array power (orbit average)	80	Watts
Reliability goal (2-years)	80	%
Mass Memory (surviving after 2 years)	1	Gbyte
Total bit error rate	< 1E-9	
Telemetry (NASA STDN compatible)	S-Band	
Downlink data rate	5	Mbits/sec
Uplink data rates	2,4	kbits/sec
Telecommand format	CCSDS	
Telemetry format	CCSDS	
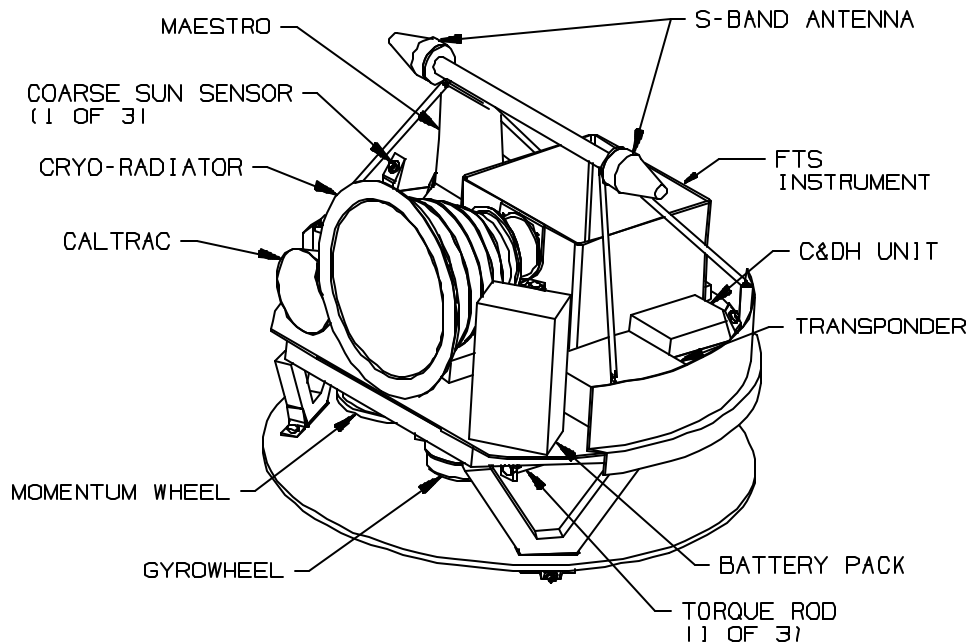
Figure 2 Spacecraft Layout

Figure 3 Spacecraft Architecture

C&DH Architecture

Key C&DH Performance Requirements

A key requirement of the ACE spacecraft C&DH Unit is the ability to handle high data rates from the science instruments (up to 9.6 Mbits/sec) and to provide 1.5Gbytes of on-board storage for science data. Key specifications are summarized in Table 2.

Design Philosophy

The design philosophy is to use a lower-speed, lower-power processor to perform all complex tasks. Higher speed, simpler tasks are performed in firmware. Power is minimized by making the software and firmware event-driven so that power is consumed only when required.

Card Functionality

The block diagram of the C&DH Unit is shown in Figure 4. The C&DH Unit processes all uplink commands and includes firmware critical command decoders for use in the event of processor/software anomalies. The C&DH Unit includes a two-stage watchdog process, with both a warm reboot to preserve operational states and a cold reboot with re-initialization of all parameters. The telemetry chain programmed into the C&DH Unit FPGAs includes functionality for CCSDS transfer frame formatting, Reed-Solomon Encoding, randomization, and convolution encoding.

The C&DH Unit is comprised of a Controller Card (CC), Data Handling Card (DHC), Input/Output Card (IOC) and Power Supply Card (PSC) as shown in Figure 4. Each card is housed in its own aluminum frame, and the frames are integrated in a vertical stack as shown in Figure 5.

Controller Card (CC)

The CC is responsible for control of all aspects of the spacecraft. A block diagram is shown in Figure 6. This includes attitude control, instrument control, power system control, thermal control, telemetry control and higher levels of data management. It also receives up-link

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commands/data from the receiver and sends formatted data to the ground via the transmitter.

The CC is built around the UTMC 80C196 which is a radiation-hardened 16-bit microprocessor. Two FPGAs are used on the CC to implement all

Table 2 Key C&DH Specifications

Parameter	Value	Units
Processor (16-bit)	80C196	
Operating frequency	16	MHz
SRAM (16-bit, no wait states)	256	kBytes
EEPROM (dual redundant)	256	kBytes
Mass Storage	1.5	Gbytes
FTS daily requirement	650	Mbytes
MAESTRO daily requirement	100	Mbytes
Error rate	1E-10	max
Transfer Rates		
FTS	9.6	Mbits/sec
FTS VNI and housekeeping	2	Mbits/sec
MAESTRO	3	Mbits/sec
CCSDS Telemetry		
Maximum rate	5	Mbits/sec
Rate adjustment step size	20	% max
Transfer frame data size	1016	bits
Reed Solomon Encoding	yes	
Convolutional Encoding	yes	
CCSDS Telecommand		
Rate	2, 4	kbits/sec
ADCS Processing		
Sun-pointing loop bandwidth	5	Hz
Wheel speed control loop	5	Hz
Roll control loop bandwidth	1	Hz
Wheel speed resolution	16	bits
Wheel torque resolution	12	bits
Torque rod pulse quantization	4	ms
Radiation		
Total dose (limited by SDRAM)	15	krads
Maximum upset rate	1	upset/month
Latchup	none	
Power	10	Watts max
Reliability for two year mission	0.95	
Mass	under 4	kg

the support logic functions i.e. reset and interrupt expansion, timers, address decoding, the critical command decoder and the Reed-Solomon encoding for the telemetry data.

The CC contains 256 kbytes of rad-hard SRAM and 256 kbytes of rad-tolerant EEPROM. The EEPROM is isolated from the address and data buses by a bus switch in the FPGA. This allows the EEPROM to be powered-down except when needed. Program code is copied from EEPROM at power-up and executed in SRAM with 0 wait states at 16 MHz.

The EEPROMs can be reprogrammed in orbit. Two EEPROMs are used and arranged so they can be accessed independently of each other. This allows the processor to be able to boot successfully even if one of the devices becomes corrupted during a write operation.

The CC has two external interface connectors and a backplane connector. Whenever possible, off-card communications are through Intersil rad-hard RS-422 transmitters and receivers. The RS-422 receivers can be powered down when not required in order to save power.

The CC has one high frequency temperature-compensated crystal oscillator which is used as a frequency reference for the entire C&DH Unit.

The CC also contains diagnostic monitoring circuitry to monitor the power to the various circuit blocks.

There is also a critical command decoder on the CC which operates independently of software running on the CC. The critical command decoder can upload software as well as generate a reset or perform a timed power down. Other critical commands such as pinging the transmitter are also supported.

Data Handling Card (DHC)

The DHC receives high-rate data from the instruments and stores it in on-board mass memory. A block diagram is shown in Figure 7. When over a ground station, the CC signals the DHC to output the stored data. The data is formatted into CCSDS transfer frames and transferred to the Reed Solomon encoder on the CC for final encoding before it is transferred to the ground.

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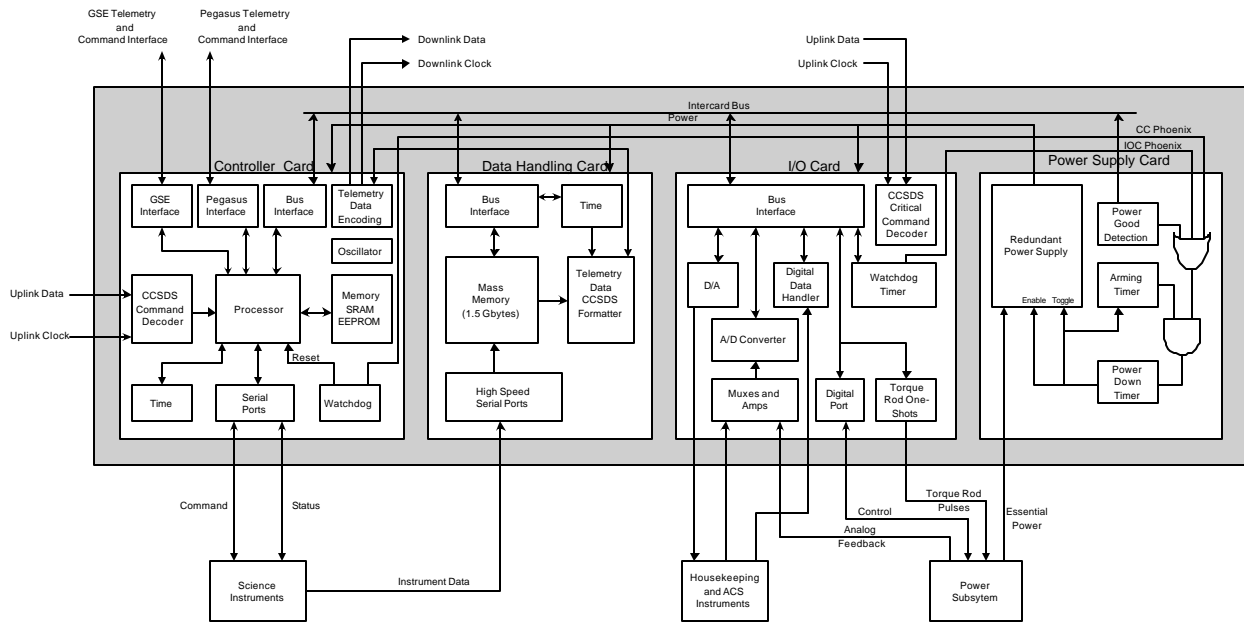
Figure 4 Block Diagram of the Control and Data Handling (C&DH) Unit

Figure 5 Development Model of C&DH

The CC controls the DHC and transfers housekeeping data and other low-rate data to the DHC via the backplane. The instruments transfer data though RS-422 synchronous serial ports. Data is transferred to mass memory as required in a prioritized fashion. No FIFOs are required.

The mass memory has 1.5 Gbyte capacity and has additional Error Detection and Correction (EDAC) circuitry to protect the memory from Single Event Upset (SEU) and failed bits. All single-bit errors can be detected and corrected and double-bit

errors can be detected and corrected using software in the ground station. The memory is organized with three redundant 512 Mbyte banks so that a failure affecting one of the banks does not cause the whole memory to fail. In addition, areas of 128 kbytes can be bypassed if failures are detected within them.

Two high-density FPGAs perform all aspects of the data handling function.

Input / Output Card (IOC)

The IOC is used to provide the analog interface for all analog sensors used in the spacecraft. 16-bits of digital input and 16-bits of digital output capability are also provided.

The IOC contains a 16-bit analog to digital converter. Signal conditioning is included for interface to thermistors (used to monitor various spacecraft temperatures) and level translation of low level and bipolar inputs. Buffer amplifiers are included on the output of the four D/A converters to provide drive capability and filtering. The IOC also includes monitoring circuitry to monitor the power to the various circuit blocks.
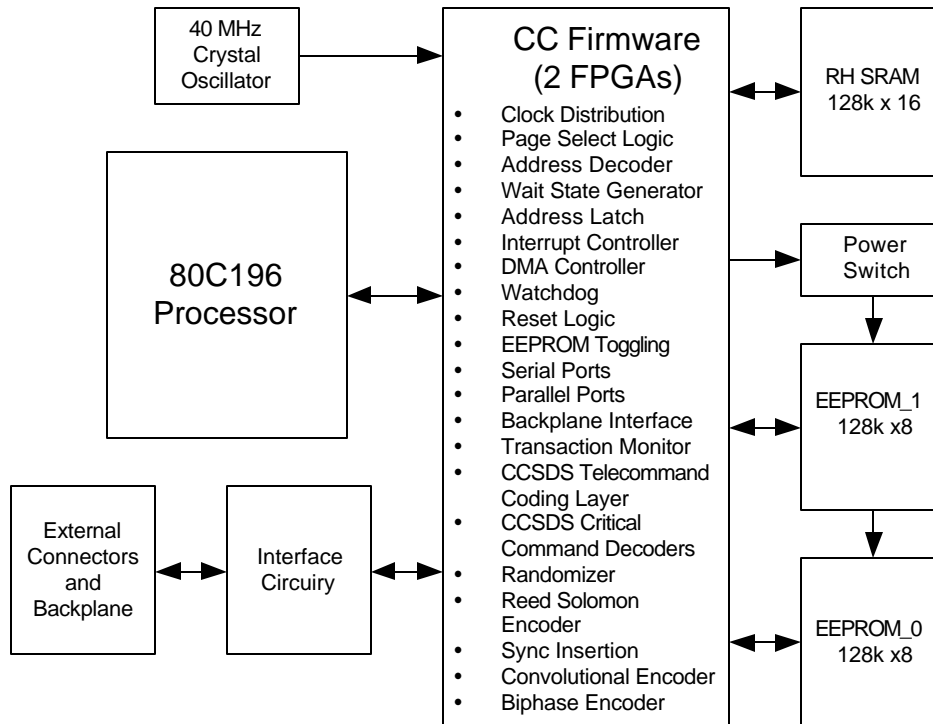
Figure 6 Block Diagram of the Controller Card (CC)

The FPGA on the IOC provides glue logic, the backplane interface and state-machine type sequencing. The FPGA performs signal averaging on critical signals. For the momentum wheel, the FPGA provides a custom high-resolution reciprocal counter for measuring wheel speed and a dual-modulus high resolution PWM controller for generating the torque command. The FPGA also provides a special interface to the digital sun sensor.

Power Supply Card (PSC)

The PSC provides the power to the various cards in the C&DH Unit. The PSC contains isolated DC-DC converters to provide the required DC isolation between the C&DH Unit and chassis ground. The PSC accepts the 28 Vdc bus voltage from the Power Control Unit (PCU) and generates the four voltages necessary to power the C&DH Unit. The output of the PSC is directed to the other cards in the C&DH Unit via the backplane.

The PSC contains dual-redundant converters and circuitry to monitor faults of low input or output voltages, or excessive input current. Each time a fault condition triggers a timed-shutdown, the active set of converters is switched off and the redundant set becomes active.

C&DH Mechanical Packaging Concept

The C&DH mechanical packaging concept is shown in an exploded view in Figure 8 - C&DH Packaging Concept. Instead of a traditional card cage design with a passive backplane, a card stack approach was taken. This packaging method provides almost unlimited flexibility in configuration, as any number of cards in any stacking sequence can be installed. Each printed circuit board is attached to an integral aluminum card frame with screws. These card frames "stack", with top and bottom frames, using quantity six #8 screws. Accurately located 70-pin backplane connectors on each circuit card provide intercard communication and power. The circuit boards are solidly clamped all around the perimeter between the aluminum card frames thereby providing efficient heat transfer from the cards. The bottom frame is

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bolted to the spacecraft deckplate with quantity six #10 screws.

The C&DH external surfaces are black anodized to enhance radiation heat transfer to internal spacecraft surfaces. Intercard interface surfaces, and the spacecraft interface surface of the bottom frame, are clear alodined to provide a low

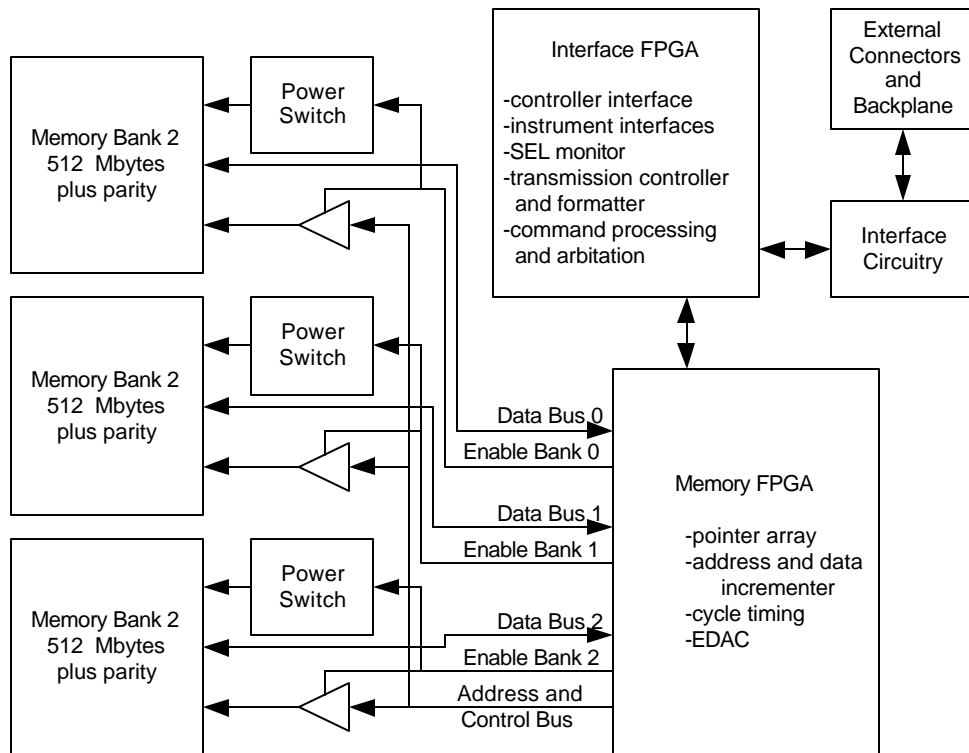impedance interface where electrical continuity/grounding is required.

Real Time Operating System

Originally the design concept was to use a simple foreground background executive, which for a
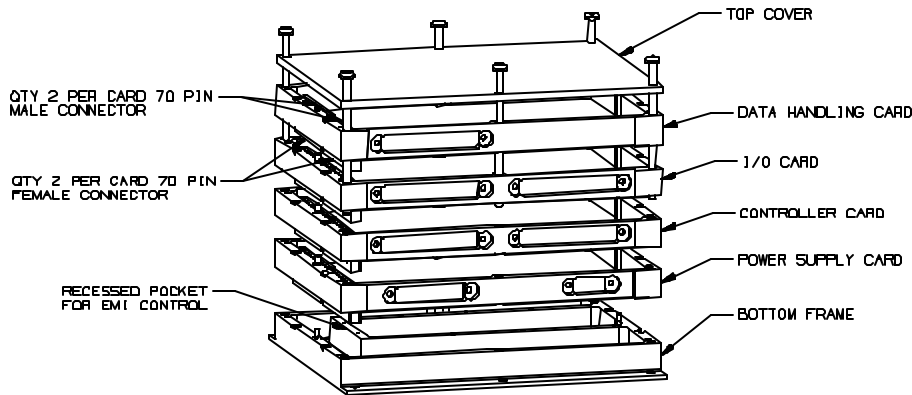
Figure 8 - C&DH Packaging Concept

Figure 7 Block Diagram of the Data Handling Card (DHC)

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simple system was a valid approach. As the requirements grew and the mission went from a single instrument, to the present configuration with two instruments, a Star Camera, and a Gyro wheel, it was determined that a COTS Real Time Operating System (RTOS) would be well suited to handle all of the asynchronous processes necessary to meet the mission requirements.

Three separate RTOS available for the 80C196 processor were evaluated. The CMX-RTOS by CMX Systems was selected. Key considerations in the selection were: small RAM footprint; excellent system response times for context switching; availability of a version specifically written for the Tasking Tool Set selected for development; availability of a test version of the RTOS that runs on a PC which can be used for prototyping and logic testing; and lower cost - there are no royalties or license fees and the source code is provided. The CMX RTOS is approved for use in medical systems, aviation systems, and is used to control a GPS clock.

The RTOS provides real-time multi-tasking, scheduling, intertask communication and synchronization, memory management and timer functions. Task execution will be event driven and based on task priority. Bristol will develop device I/O service routines specific to the architecture. An illustration of the top-level software architecture is shown in Figure 9 Software Architecture

The RTOS provides tested code to handle all the functions related to defining, initiating, coordinating and scheduling tasks and to provide inter-task messaging. With this approach the operations of the flight software will be implemented as a series of tasks, each with an assigned priority. This is a very common design approach.

Use of an RTOS enables the flight software to be easily expanded. Functions can be added without requiring major changes to the software structure - a key for incremental buildup and for achieving a reusable design. This approach simplifies the development process by splitting the code into separate tasks and minimizes the dependencies

between them. With support for task preemption - time critical events are handled quickly and efficiently. The RTOS provides control of resources through timers, semaphores, messaging and time-out monitoring. Overall this move to the RTOS will reduce our software development time.

Rapid development achieved by use of an RTOS has already been demonstrated for SCISAT-1 program. The RTOS was up and running early in the detail design phase - executing on both the UTMC 196 instruction set simulator and an Evaluation Board. Prototype timeline code - handling interrupts, mission elapsed time, and time specific events was implemented under the RTOS within in a matter of days.

Software Design

On power up, boot code runs directly from the boot EEPROM. Two copies of the software are kept on board, stored on different EEPROM devices. The C&DH unit alternates between these versions on sequential cold restarts. The boot code is responsible for performing a checksum on the boot and application code in EEPROM and will switch to the alternate copy if errors are found. If there are no errors the boot code will copy the application code to RAM, complete the hardware initialization, initialize tasks and variables and launch the RTOS.

After a restart the software will start its sun acquisition and will wait for ground commands.

Parameter Tables

A notable attribute of the flight software design is the use of ground-modifiable tables containing parameters instead of hard-coded values in the software. These tables group related parameters such as control gains, sensor and actuator scale factors and biases, fault detection and housekeeping limits and tolerances, and system enable flags. Tables may be modified temporarily by loading new values to RAM, or permanently by loading to EEPROM. This design approach simplifies on board processing and reduces the number of commands the software must support.

This capability is especially useful for ACS parameters such as sensor alignments and

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calibration measurements that remain undetermined until shortly before launch.

Autonomous Operations

The spacecraft will have multiple ground contacts each day. Between ground contacts the flight software provides autonomous control of the spacecraft by issuing pre-loaded commands from memory.

calculated on the ground and uploaded as time-tagged data, rather than performing on board computations and modeling.

The flight software performs continuous monitoring of spacecraft data for anomalies. A portion of the mass memory has been allocated to the flight software to store bus housekeeping data. Between ground contacts, data is stored for later playback to
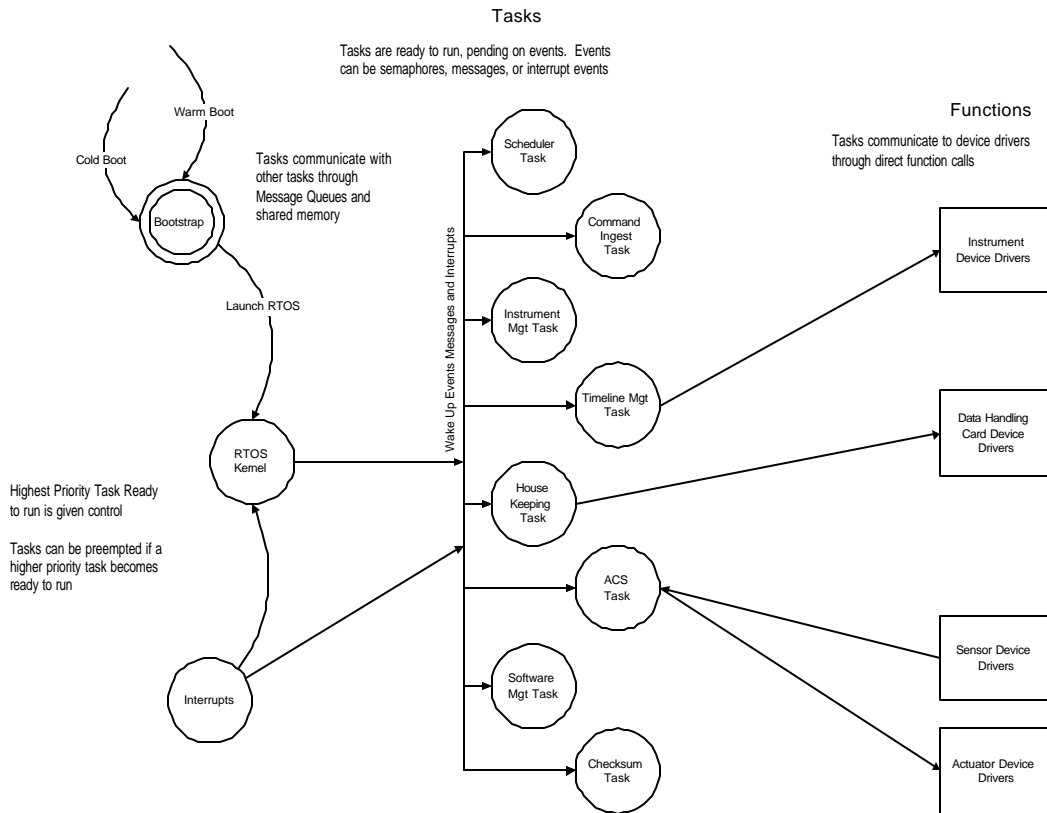
Figure 9 Software Architecture

On board buffers are available to store up to 7 days of normal operational timeline commands, magnetic field model data and star camera data. Nominally, these timeline data will be uploaded every three days. Due to the size of these data sets, they are stored in mass memory with the flight software maintaining small circular buffers of current data in RAM.

The design concept was to implement high speed data handling and formatting in FPGAs, reducing the processor load. Additionally to reduce the processor loading it was decided that magnetic field model and star tracker data would be

the ground. The bulk memory provides the storage for the engineering data, processor status, attitude control status, and science data.

Software Development Environment

The software tools for SCISAT-1 flight software provide an integrated platform for code development. The Tasking 80C196 Compiler Suite is integrated with the CodeWrite editor to provide syntax highlighting and enhanced code formatting. The Chipview x96 Instruction Set Simulator and Debugger provides a GUI-based source-level debugging environment integrated directly with the compiler. The compiler tools interface directly

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with Visual Source Safe for automated file sharing, version control and change tracking of source code across a local network.

One development workstation is configured with a UTMC-196 Evaluation board hardware with ROM monitor that is also controlled from the Chipview software. This provides a common debugging interface for the developers to run code either via the simulator or on evaluation hardware.

Key Design Issues

Parts Selection

The quality of most EEE parts is QML Q level (Class B). FPGAs are MIL-STD-883 B level. Upscreened commercial parts are acceptable for special parts such as the SDRAMs. Parts are derated per MIL-STD-975 or GSFC PPL-21.

All EEE parts have been selected to be latchup free and have a very low probability of SEU. The major exception is the 2Gbit SDRAM parts used on the DHC, where EDAC is used to achieve the required bit error rate of 1x10-10.

CCSDS Telemetry

CCSDS Telemetry is implemented in firmware. A block diagram is shown in Figure 10. The downlink data rate is programmable and can exceed 5 Mbits/sec. The rate can be adjusted with

reasonable granularity to allow a near optimum rate for channel conditions to be selected. Low data rates are also available to handle link anomalies.

Reed-Solomon and convolution encoding can be selectively used. Biphase encoding is also available for use at low bit rates in order to keep the spectral components of the data away from the carrier.

Data is organized and stored in mass memory based on the virtual channels that are used for downlinking. Firmware extracts data from memory and formats it into CCSDS compatible transfer frames. The priority of transmitting the data on each virtual channel can be adjusted by software to suit the operational requirements. During insertion of the sync word, the highest priority channel with data available is selected for transmitting. The idle channel is the lowest priority channel; if data is not available on other channels, idle data is inserted.

CCSDS Telecommand

The front end of the transfer layer for telecommand processing is done in firmware. This includes sync search, sync-inversion, de-randomization and CRC checking. 16-bit data is transferred to the processor as it is received. The
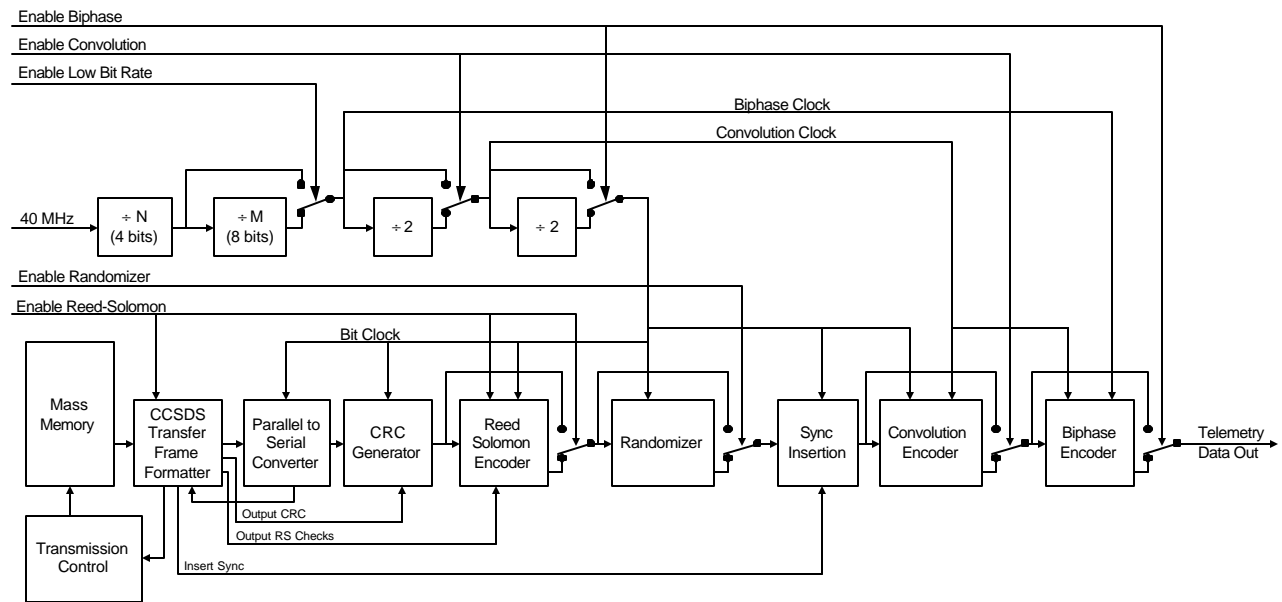

Figure 10 Block Diagram of Telemetry Chain

final word of the command codeblock transferred to the processor contains the result of the CRC check.

Several critical commands are decoded and executed by firmware. These commands do not require the processor to function in order to execute.

Power
Orbit-average power for the C&DH Unit is expected to be 7 Watts max. Peak power (instruments transferring data to memory and telemetry being output) is expected to be 10 Watts max.

Reliability
The memory on the DHC is organized as three separate banks which can be powered down independently of each other. Any failure that shorts out a bank can be isolated so that the remaining banks remain functional. In addition defective areas in mass memory (granulized to 128 kBytes) can be bypassed using a map table. This allows the reliability of the C&DH to be 0.95 for a minimum of 1 Gbyte operating for the two-year mission.

Summary

SCISAT-1 will be launched into a 650-km orbit in Q2 2002 to investigate processes that control the distribution of ozone in the upper atmosphere. The mission life is expected to be two years with a goal of extending operations to five years. The C&DH Unit being developed by Bristol to support the mission is low-power, light weight, and features a rad-tolerant core to assure reliable operation in a single-string architecture.

Ian Walkty   14th Annual/USU Conference on Small Satellites

Biography for Ian Walkty

Ian Walkty is currently employed with Bristol Aerospace Limited of Winnipeg, Manitoba, Canada. His present responsibility is Program Manager for the Canadian SCISAT-1 small satellite program, for which Bristol is the Prime Contractor to the Canadian Space Agency for the spacecraft bus. Mr. Walkty has been with Bristol for 20 years, holding various management and technical positions in the Space Systems Group. He has managed a wide range of sounding rocket and Space Shuttle payload projects over the last 11 years. Prior to this, he developed hardware and software for aviation weather systems that Bristol was designing for Environment Canada. Before joining Bristol, Mr. Walkty worked for the Department of National Defence in the areas of signal processing and underwater acoustics. Mr. Walkty holds a MSc degree in Electrical Engineering from the University of Manitoba.

Biography for Jim Petersen

Jim Petersen is employed with Landmark Electronics Inc. and has been contracted by Bristol Aerospace for the last 3 years in support of the SCISAT program. His current responsibility is lead C&DH hardware engineer. He has been involved in a number of successful projects over the years including a state-of-the-art contactless test system for which he was responsible for the patent. Mr Petersen was employed by Bristol Aerospace from 1982 to 1988 and was responsible for the RF design of synthesized transmitters. Mr. Petersen holds a BEng degree from McGill University in Montreal. He graduated in 1979 as a university scholar with distinction in electrical engineering.

Biography for Thom Doherty

Thom Doherty is currently employed with Bristol Aerospace Limited. His present responsibility is as the Software Lead for the Canadian SCISAT-1 small satellite program. Mr. Doherty has 16 years of experience developing real time mission critical software. During his ten years with Bristol, Mr. Doherty has served as the Software Lead for the development of airborne and ground systems software for a number of successful programs including: the Hokum-X Helicopter target drone the US Army Missile Command; the Heads Up Display software development for the Canadian F-5 fighter aircraft; Canadian F-5 - Flight Simulator; Inertial Navigation Unit ground support/test system; Digital Air Data Computer ground support software; Rooivalk Attack Helicopter rocket launcher controller concept design; CH135 Helicopter vibration and load analysis system. Prior to joining Bristol he worked for Unisys Defense Systems where he developed real time command and control system software for the Canadian Navy's Patrol Frigate Program and Tribal-Class Destroyer Upgrade Program.

Biography for Bill Whitehead

Bill Whitehead is employed with Bristol Aerospace Limited of Winnipeg, Manitoba, Canada. His current responsibility is Electrical Systems Lead for the Canadian SCISAT-1 small satellite. Mr. Whitehead has been with Bristol for 33 years, holding various technical positions in the Space Systems Group. During his career he designed and developed many products including: the Command Decoder for the CTS (Hermes) Satellite; instrumentation and RF products for sounding rockets; transmitters and microprocessor systems for automated weather stations; and robotics for the nuclear industry. Mr. Whitehead holds a BSc degree from the University of Manitoba and was awarded the Governor General's Gold Medal for Electrical Engineering when he graduated in 1967.