A Low power Command and Control Module for Small Satellites

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Abstract

Utah State University/Space Dynamics Laboratory has developed a low power computer system for command and control, attitude determination, and telemetry for small spacecraft. The system has been developed for the 15-kilogram class Ionospheric Observation Nanosatellite Formation (ION-F) satellites.

This constellation of three satellites is being built by Utah State University (USUSat), University of Washington/Cornell University (DawgStar), and Virginia Polytechnic Institute (HokieSat) and is part of the AFSOR/DARPA University Nanosatellite program with additional support from industry, NASA, the Air Force Research Labs, and the Air Force Space Test Program. The command and data handling (C&DH) system is based upon industrial-grade components, including a third generation Hitachi SuperH RISC processor and radiation tolerant ACTEL FPGAs. The memory subsystem is comprised of 256 Kbytes of EEPROM, 8 Mbytes of redundant flash memory, and 5 Mbytes of SRAM. The C&DH system also contains a 16 Mbyte telemetry buffer, digital and analog I/O interfaces, and a DMA-oriented CMOS camera system. The C&DH is radiation tolerant to approximately 5k Rad total dose. Single event upsets are dealt with at the hardware level by over current monitoring circuitry, redundant voting memory configurations, and multiple software watchdog timers. The entire computer system consumes less than 1.75 Watts peak, with an average of 1 Watt, and provides an 80-MIPS, 32-bit computation platform for a small spacecraft. An initial prototype satellite has successfully passed extensive environmental testing and demonstrated the advanced capabilities of the ION-F C&DH system.

Introduction

The Air Force Office of Scientific Research (AFOSR) and the Defense Advanced Research Projects Agency (DARPA), along with NASA, have jointly funded the Ionospheric Observation Nanosatellite Formation (ION-F) comprised of three ~15 kg class small satellites being built by Utah State University (USUSat), the University of Washington/Cornell University (DawgStar), and Viginia Polytechnic Institute (HokieSat). The objective of this program is to demonstrate the usefulness of nanosatellites in such areas as formation flying, attitude control, maneuvering, and communications. ION-F has been designed as a harbinger for innovative nanosatellite technologies. It is helping pioneer the development of low-cost distributed satellite clusters and will be the first such mission to attempt a global multi-satellite study of plasma density structures in the ionosphere.

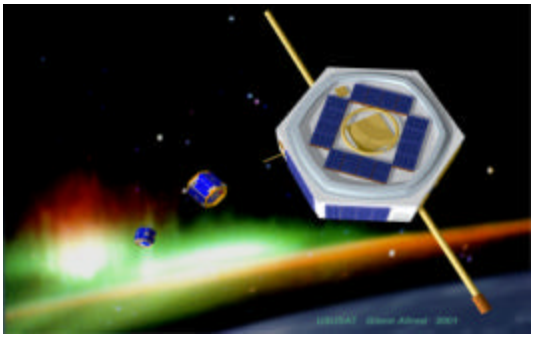

Figure 1.USUSat amongst the three satellites of the ION-F constellation

Principally, this paper will present the current stage of implementation of the IONF C&DH system. John Jensen[1] developed the requirements and the path-breaking design for the IONF C&DH approximately three

years ago. The C&DH system is common for all three ION-F satellites and is comprised of four individual C&DH sub-system modules; namely the CPU board, the Camera board, the Telemetry board, and the Input-Output (IO) board. All modules are plugged into the same motherboard (Backplane board) that furnishes power and a common address and data bus.

The CPU Board

The CPU board subsystem is based around the Hitachi SH7709 32-bit SuperH 3rd generation microprocessor. The on-board memory system comprises of 5 MBytes of SRAM, 8 MBytes of flash memory, and 256 kBytes of EEPROM.

The operating system being used is Wind River Systems' VxWorks Real-time Operating System (RTOS) version 5.4.1. The Boot Rom image occupies approximately 200 kBytes of EEPROM. The complete run-time OS occupies approximately 700 kBytes in flash memory. The board draws a peak power of 1.75 Watts during flash memory write and erase operations, and averages about 1 Watt of power usage. The processor has eight external A/D channels, each of which is used for over current monitoring on separate C&DH boards via the system motherboard. The processor supports two RS232 ports, one RS422 port, thirteen digital IO lines, and 10 digital input lines through a top external board connector. The processor also supports up to 32 additional digital IO lines for the rest of the satellite electronics modules via the motherboard. The CPU board communicates to the other C&DH modules with an address and data bus via the motherboard. One of the RS232 ports has been configured to allow external debugging and modification of the system software via an umbilical connection.

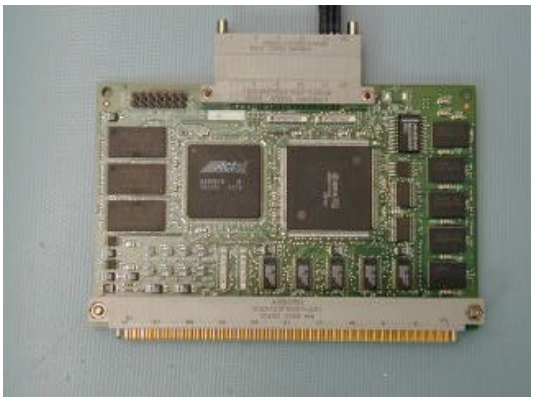

Figure 2. CPU Board

The SH7709 processor delivers 80 MIPS of performance for integer based calculations. The CPU board does not have a math coprocessor, but it simulates floating-point computations in double precision format using math libraries, delivering about 18 MIPS performance. As an example of the real-time computing power, the processor is able to compute a magnetic field vector in 270 msec using a 10th order spherical harmonic geomagnetic reference field model. Furthermore, the spacecraft attitude, based on a Kalman filter and calculation of the above mentioned magnetic field vector, sun vector, and the nadir vector, is computed in less than 1 sec. The algorithms are implemented in ANSI C++.

The Camera Board

The Camera board connects to 4 CMOS cameras and allows for DMA oriented simultaneous capture of four 512 x 512 pixel (8 bits per pixel) images. The images are transferred directly into a memory bank of 1 Mbyte SRAM and then retrieved by the CPU board processor for analysis at determined times. The CMOS camera data is transferred to the processor on the CPU board by utilizing the motherboard address and data bus.

The Camera board has external software gain control along with on board 8 Mbytes of flash memory for calibration images required for CMOS camera's fixed pixel noise correction. Out of the 8 MBytes of on-board flash memory, 6 MBytes are used for

calibration image storage and the remaining 2 MBytes are used for general-purpose non-volatile data storage.

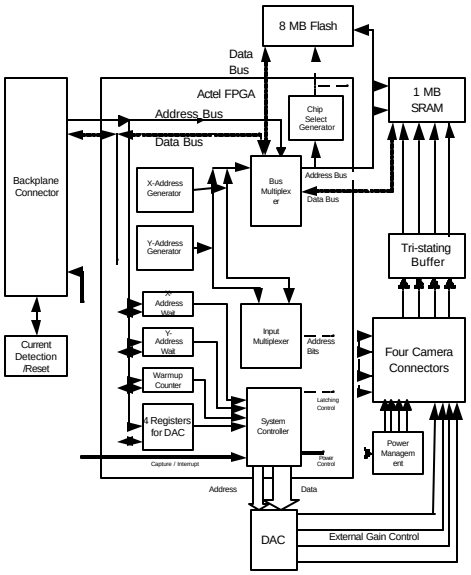

Figure 3. Camera Board Top Level

The Telemetry Board

The satellite's science mission collects a large amount of data that has to be stored on the satellite and then transmitted to a ground-station during an overpass. Hence the main function of the Telemetry board is to facilitate the downlink process and reduce the load on the microprocessor. The Telemetry board stores the data in PCM page format. The board is implemented using a DMA-oriented design. The CPU organizes data into PCM pages and stores them within 16 MByte of flash memory located on the Telemetry board. It then writes the starting and ending addresses of valid pages to registers on the telemetry FPGA. When a telemetry access begins, the Telemetry board FPGA digital logic disconnects the Telemetry board's flash memory data bus from the CPU board, reads mission data from the Telemetry board flash memory, and then serializes and streams it to the transmitter. At appropriate locations, frame synchronization words and real time data from the CPU board are also inserted into the stream. This process continues until all the valid data has been transmitted. If necessary, the telemetry process can be interrupted and restarted at an appropriate location. As errors in telemetry stream would not be fatal for mission continuity, bit-error detection and correction are not implemented on the Telemetry Board.

Figure 4. Telemetry Board

The Input-Output Board

The Input/Output (IO) board provides digital and analog interfaces to subsystems, both inside and outside the electronics enclosure. The IO board serves as an extension of the CPU board processor capabilities. The processor communicates with the IO board via the motherboard address and data bus.

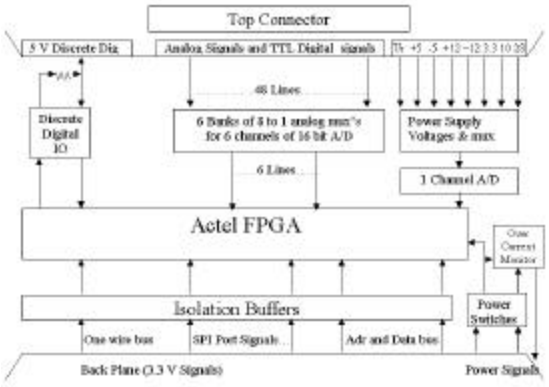

Figure 5. IO Board Top Level

The IO board has an external connector interface of 16 digital IO pins, 56 16-bit A/D channels, and a 1-Wire® data bus. A 1-Wire data bus also runs from the IO board to the remaining satellite electronic sub-systems

via the motherboard. In addition, the IO board supports a Motorola SPI data bus via the motherboard.

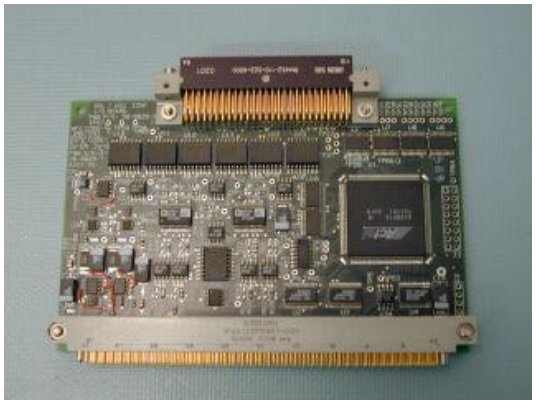

Figure 6. IO Board

Prototype Testing

Excluding the Telemetry board, the complete ION-F C&DH system has been tested in a thermal vacuum environment for over 250 hours of operation. Significant operating system loads were placed upon the CPU board processor throughout the hours of operation. Although a majority of the components used in the design are of industrial and commercial grade, they withstood continuous operation in a vacuum of at least 10^{-5} Torr and temperature ranges of –30 to +90 °C. The satellite C&DH system performed without any major flaws and proved the robustness and advanced capability of the C&DH design.

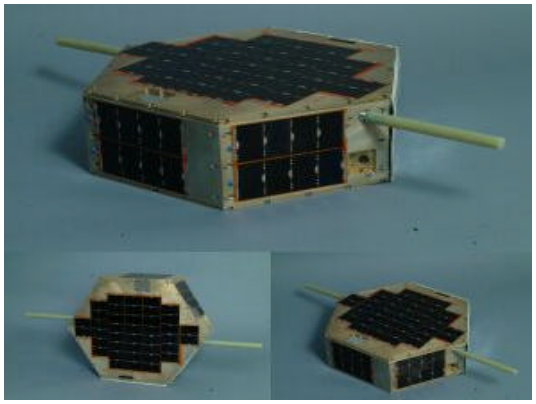

Figure 7. Prototype Satellite

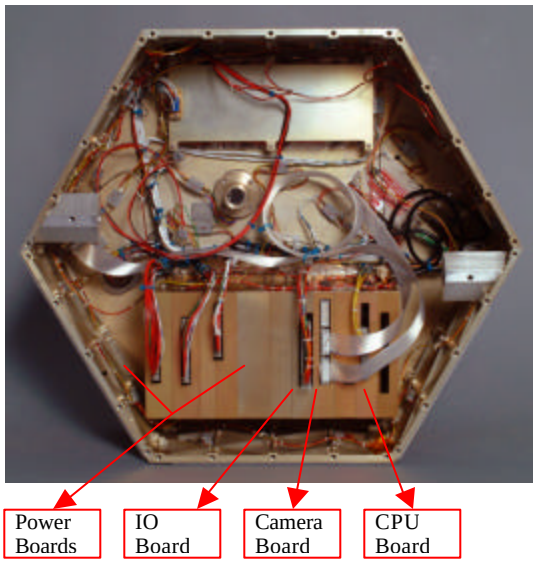

Figure 8. Prototype satellite electronics

SUMMARY

Though the C&DH system is built out of industrial and commercial grade components, the successful testing of the prototype satellite has increased confidence in the capability of the ION-F constellation. The usage of a 32-bit 80 MIPS microprocessor gives ION-F immense computational power, and the presence of redundant hardware and monitoring circuitry provides a significant amount of fault tolerance. Needless to say, ION-F is close to achieving one of its goals, that of being a harbinger in innovative small satellite design and technology.

ACKNOWLEDGEMENTS

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REFERENCES

1. Jensen, John. 2000 *The Design of the Command and Data handling subsystem used by ION-F*. MS Thesis, Utah State University