FPGA-based Coherent MSK Spread Spectrum Modem for Small Satellites TT&C Transponders

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ABSTRACT

In low earth orbit (LEO) satellite communication links it is required to employ modulation/demodulation techniques to achieve transmission with minimum power and efficient usage of spectrum (according to international telecommunication union (ITU) and consultative committee for space data systems (CCSDS) regulations and recommendations) with minimum bit error rate (BER) at the receiver. Minimum shift keying (MSK) meets all these requirements. It is required also to measure the varying distance between the satellite and the ground station (range) and the velocity of the satellite (range rate) to facilitate the tracking of the satellite by the ground station antenna tracking system and therefore, a direct sequence spread spectrum (DS-SS) technique is used. Thus, coherent MSK DS-SS modem is chosen in this paper for LEO communication links. This paper investigates design, implementation and testing of a FPGA-based coherent MSK DS-SS modem suitable for small satellites TT&C transponders. The modem includes a MSK modulator, an automatic gain control (AGC), and MSK DS-SS demodulator/synchronizer (where a proposed novel phase ambiguity solver algorithm is presented). Demodulator performance is evaluated by adding band-limited (nearly white within the signal bandwidth) Gaussian noise to the MSK DS-SS modulated signal (resulting in E_b/N_o near 0dB) and measuring the BER and the phase variances of the synchronized carrier and the clock with its operating E_b/N_o for the extracted chips, which show good performance.

INTRODUCTION

Digitally implemented coherent modems are typically used in LEO satellite communication links to convey information between space and ground segments in both directions with minimum BER. Coherent modems provide 3dB improvement in performance of the BER compared to non-coherent modems and allow use of DS-SS to track the satellite by the ground segment due to availability of locally generated carrier and clock references in coherence with the received ones even for low signal to noise ratios (SNR).

Digitally implemented coherent MSK DS-SS modem is presented in this paper. The modem contains synchronizer for both carrier and clock.

In the following, a qualitative analysis of the proposed digitally implemented coherent MSK DS-SS modem and its performance are presented. The modem includes: modulator, AGC and MSK DS-SS demodulator/synchronizer based on using squaring element, two linear phase-locked loops (LPLL) and correlators.

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The modulator produces type II MSK modulation, where the modulating bits alter the polarities of the absolute values of the positive half cycles of the sinusoidal weighting functions. Two low cross-correlation pseudo random sequences (PRS) of m-sequences (i.e. preferred pair of Gold codes) are used to modulate the in-phase (I) and the quadrature (Q) channels, respectively.

The demodulator is preceded by a high pass filter (HPF) followed by AGC (comprising demodulator front end). The HPF removes any attached DC component in the input signal. The AGC fixes, at the steady state, the input signal level at the input of the demodulator. Two types of AGC are presented; with linear (LAGC) and exponential (EAGC) gain characteristics of the controlled gain amplifier (CGA) which differ in the dependence of their attack times (time needed to compensate for a change in the input signal level) on the amplitude of the input signal. Signal level suppression at LAGC output is measured in the

presence of added band-limited Gaussian noise and the results are used in the design of LPLL and this method is also used to determine the E_b/N_o for BER measurement.

Carrier frequency acquisition is achieved by using complex fast Fourier transform (CFFT), while codes acquisitions are achieved using correlators. Coherent demodulation is employed by using squaring element technique for generating double the MSK symbols' frequencies from the received type II MSK modulated signal which are phase tracked by two LPLLs. Phase ambiguities due to doubling the symbols' frequencies are resolved.

Laplace transform analysis is used for the modeling and designing of HPF, AGC, and LPLL as a semi-continuous time systems and the results are used to obtain the discrete time circuits parameters assuming that the sampling frequency is much higher than the fastest transient in each circuit. Subsampling technique is used to downconvert the received IF signal with a rate satisfying Nyquist criterion for the chip rate.

Each of these circuits is designed and simulated using VHDL language and then implemented on FPGA. A real model for additive band-limited Gaussian noise is implemented to measure the demodulator performance while operating close to the real environment (i.e. low SNR and Doppler effect). The BER is the main measure for the modem performance with its operating E_b/N_o.

TYPE II MSK DS-SS MODULATOR

The proposed digitally implemented type II MSK modulator is shown in Fig.1. The modulated signal consisting of the sum of two quadrature carriers (I channel carrier $\cos(\omega_o t)$ and Q channel carrier $\sin(\omega_o t)$) each is modulated (independently) by baseband data multiplied by weighting functions. The weighting functions (positive half cosines, $|\cos(2\pi t/4T_s)|$, or sines, $|\sin(2\pi t/4T_s)|$, of periods $4T_s$, T_s is the symbol period) do not alter the polarities of the modulating baseband data streams in I or Q channels. This feature is beneficial in the demodulation because there is no more processing needed for proper extraction of the data if compared to alternating sign weighting functions of type I MSK modulation[1].

PRS are used to spread the baseband data in each channel thus, DS-SS modulation results. In this case, the chip rate, either in I or Q channel, equals to half the MSK signal symbol rate and the baseband data rate is chosen to be the chip rate divided by certain integer (equal to the processing gain (PG)). The employed PRSs, which are preferred pair of Gold codes, have low cross correlation and are aligned such that if one of the

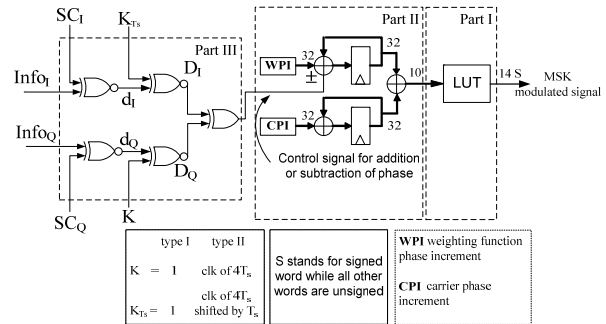preferred pairs is acquired and tracked correctly the other one can be generated automatically.

Figure 1: Digitally Implemented Type I/Type II MSK Spread Spectrum Modulator

TYPE II MSK DS-SS DEMODULATOR/SYNCHRONIZER

The proposed type II MSK DS-SS demodulator/synchronizer is shown in Fig.2 (including the demodulator front end, i.e. HPF and AGC) and consists mainly of: squarer (used to generate spectral lines), synchronizer (including: frequency detector, carrier and clock recovery, and phase ambiguities solver and PRS code acquisition), and demodulator.
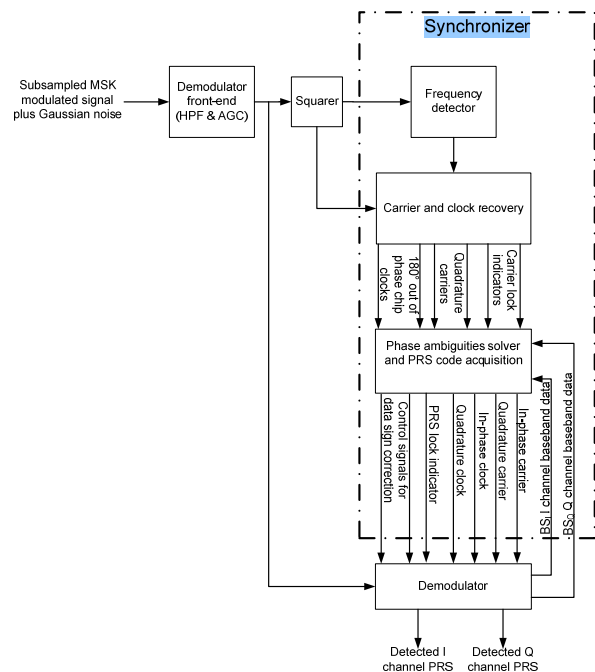

Figure 2: MSK Demodulator/Synchronizer

The used synchronizer employs aided frequency acquisition (frequency detector) which allows for using very narrow noise bandwidth LPLL and avoids the deep nonlinear behavior of LPLL (i.e. locking in very long

time) during frequency acquisition if the input frequency is outside the lock-in range of the LPLL, i.e. avoids occurrence of pull-in phenomenon. The carrier and clock phase recovery (tracking) block provides estimates for quadrature carriers and chip clocks for I and Q channels with phase ambiguities of multiples of 90° and 180°, respectively. These phase ambiguities are resolved in the phase ambiguities solver and PRS code acquisition block. This block exploits the autocorrelation feature of the PRS between the received and the locally generated codes (which gives a peak if they coincide) to resolve this phase ambiguities, and in addition the PRS code acquisition is implemented. This block provides I and Q carriers and chip clocks timing beside a control signal for correcting the sign of the extracted data (due to phase ambiguities).

The demodulator converts the received signal to the baseband and low pass filters it to get the modulating data (i.e. the information being transmitted), Fig.3.
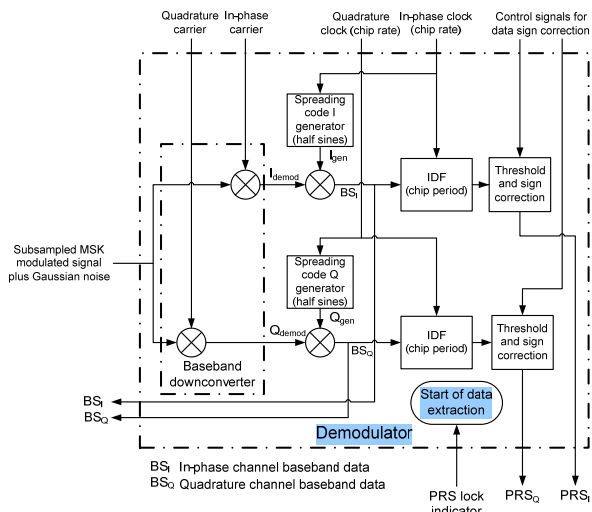

Figure 3: Digitally Implemented MSK Demodulator

The sequence of operations of the MSK synchronizer is controlled by internal state machine. This state machine monitors the results of each process and defines the next action to be performed. The MSK synchronizer acquisition/tracking state diagram is shown in Fig.4.

The first process is to high pass filter the incoming signal to remove any DC component which may be imposed in the signal. Second, the level stabilization is done by employing AGC. These two processes start after turning on the demodulator/synchronizer and they are active all the time.

Third, frequency detection begins and this process starts after the end of amplitude stabilization and it repeats until it finds a frequency component in the power

spectrum of the CFFT above a predefined threshold and if so, it is considered as the frequency component that corresponds to the Doppler shift and this process stops.
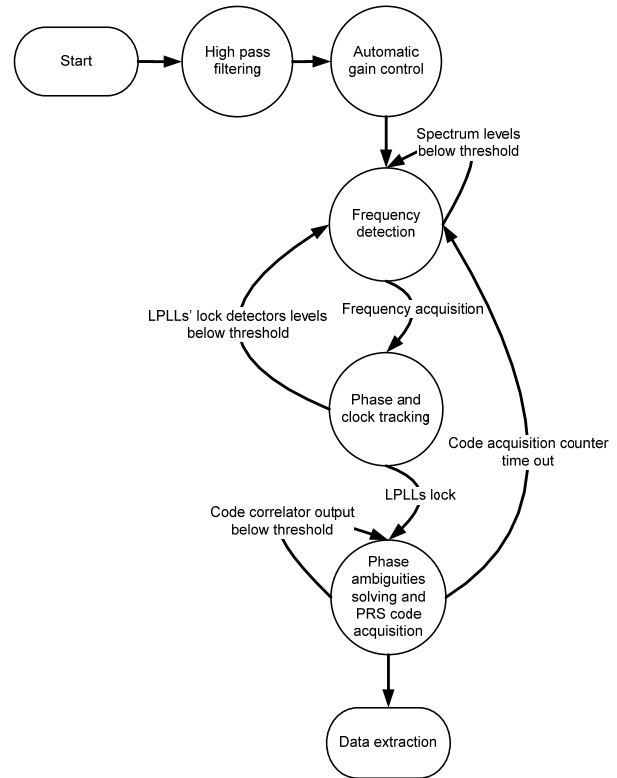

Figure 4: MSK Synchronizer Acquisition/Tracking State Diagram

Fourth, by the end of the frequency detection, the phase and clock tracking begins. This process ends if the LPLLs' lock detectors values are above a predefined threshold otherwise it goes back to the frequency detection mode.

Fifth, after carrier and clock tracking the process of phase ambiguities solving and code acquisition starts. This process operates until it finds the peak of the autocorrelation and then the process stops. If the code acquisition search is implemented for certain period of time (in the worst case, all possible phase ambiguities are scanned) and the correlation peak is not found the state machine goes back to the frequency detection mode.

Sixth, the demodulator is ready to extract the data.

Digital Demodulator Front-End

Operation of a number of receiver circuits requires a fixed input signal level. However, the received signal level may vary in a wide dynamic range (up to 100dB)[2]. Additionally, the analog front end may introduce significant variations in the signal level because of

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aging or temperature considerations[3]. The large dynamic range of signals must be handled by most receivers thus, gain adjustment is required to prevent overloading or inter-modulation in the receivers' stages[4]. In satellite communication links the received signal strength depends mainly on the antenna radiation pattern and the geometry between the transmitter and receiver.
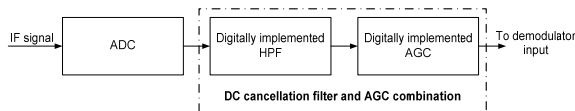

Figure 5: Digital Demodulator Front-End

For proper gain adjustment (e.g. AGC) operation, the input must be DC free signal. Thus, HPF is used at the AGC input.

HPF

A HPF is used first to remove any DC component from the input signal, which introduces bias at the AGC detector output due to this DC component. The HPF operates by accumulating the samples of the incoming signal for some long time (i.e. HPF time constant) and subtracting the value in the MSBs of the accumulator (which represents the long-term accumulated DC component superimposed on the AC signal) from the incoming signal, Fig.6.
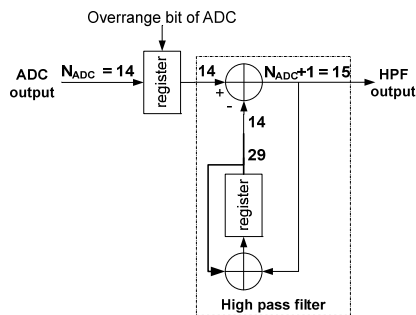

Figure 6: Digitally Implemented HPF

AGC

The use of AGC achieves fixing, at steady state, the signal level despite the variations of the received signal strength, where signal amplitude may be kept close to a desired value by appropriately controlling the gain of an amplifier (i.e. CGA)[2]. In addition, in coherent receivers (i.e. the receiver with a local oscillator (LO) that is phase locked to the incoming carrier) AGC provides the coarse gain correction necessary to help maintain the input signal to the PLL at a constant level. In PLL with multiplier type phase detector, the phase detector gain is proportional to the signal amplitude. Consequently, most of the PLL parameters depend on the input signal

level. To keep a PLL with multiplier type phase detector operating in the vicinity of its "design point" some kind of input amplitude control is inevitable[2]. Delay-locked loop (DLL), which uses multiplier(s) in the tracking discriminator, also requires AGC due to the dependence of the loop parameter on the input signal level[5]. AGC control is also important to provide the detection circuits in the digital receiver with a predefined signal level (e.g. PLL and DLL lock detectors)[2].

AGC stabilizes the total signal plus noise power. In case of receiving only noise (i.e. in the absence of the conveyed information signal), AGC stabilizes noise power and thus stabilizes the false alarm rate for PLL and DLL signal detection (i.e. it stabilizes the input signal level and in turn it stabilizes the power at the lock detectors of PLL and DLL because a lock detector contains integrator whose output is dependent on the input signal amplitude)[6,7,8, and 9].

The AGC should be fast enough to account for changing signal levels (possibly due to fast channel fading) without adjusting too quickly in a manner that would introduce AM distortion, particularly if the signal is a multi-level quadrature amplitude modulation (QAM) signal[3].

From digital point of view the AGC optimizes the bit resolution of the input signal levels (i.e. AGC decreases the output signal dynamic range) which permits to decrease the employed width of the digital words. This, in turn, decreases the capacity of the subsequent digital signal processing blocks in the digital receiver[10]. The AGC prevents loss of the LSBs although it reduces the number of the digital word bits. This is done by attenuating the large signals (represented in the whole input word length) so that it can be represented in the required reduced word length while it introduces gain for small signals (represented in the LSBs of the input word length) to fill the same required word length, thus preserves the small signal from being lost.

The AGC system (mostly used) is basically a feedback amplifier or servo system with a closed loop gain characteristic which is essentially low-pass[4]. In LAGC, the introduced gain in the feedback loop is directly proportional to the error signal and therefore, the loop dynamics is dependent on the input signal level[2 and 7]. However, some systems need nearly input-independent loop dynamics, which can be achieved using EAGC.

Signal Suppression Factor

For non coherent AGC with envelope detector, the signal suppression factor is introduced as a measure of how the detector estimates are near the actual level or

power of the scaled (by CGA) input signal. It is defined by the ratio of the signal amplitude estimated by the detector, Â, to the actual input signal amplitude A and has a minimum value of unity, at high SNR. As the signal suppression factor increases, it expresses more contribution for the input noise to the estimated signal amplitude, i.e. it increases as SNR decreases[2].

The signal suppression factor $\beta_{en}(\rho_i)$ of the envelope detector is given by[2]:

$$\beta_{en}(\rho_i) = \frac{\hat{A}(t)}{A(t)} = \left[\frac{\pi}{4\rho_i(t)}\right]^{1/2} \exp\left[-\frac{\rho_i(t)}{2}\right] \times$$
$$\left\{\left[1 + \rho_i(t)\right]I_o\left(\frac{\rho_i(t)}{2}\right) + \rho_i(t)I_1\left(\frac{\rho_i(t)}{2}\right)\right\} \quad (1)$$

where ρ_i is the input signal SNR.

The results from Equation (1) can exploited to give accurate value of the output signal level from LAGC at certain E_b/N_o, for proper design of the LPLL loop parameters.

Digital Implementation of LAGC and EAGC

Fig.7 and Fig.8 show LAGC and EAGC feedback loops with all the circuit parameters that govern the loop dynamics. The shown input and gain control signals ranges are used in deriving the loop performance parameters where K_F is the loop filter gain, T_F is the loop filter time constant, G_o is the amplifier constant, v_c is the controlling signal, K_G is the error scalar constant, A_{ss} is the required steady state output level, V_R is the reference signal and K_D is the detector gain.
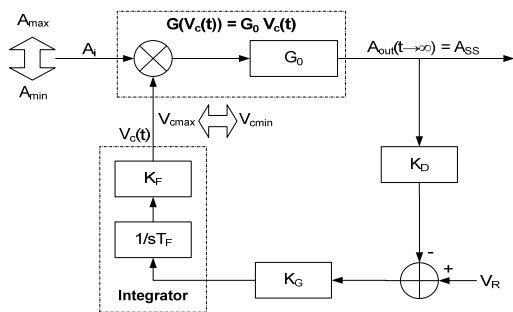

Figure 7: LAGC Feedback Loop

The attack time of the AGC loop is the time required for the resulting error (in the transient response to unit step function) to fall to a specified value, usually 0.37. LAGC attack time is equivalent to the LAGC loop time constant, τ_{LAGC}, and is given by[2]:

$$\tau_{LAGC} = \frac{T_F}{K_F K_D K_G G_o A_i} \quad (2)$$

It is to be noted that τ_{LAGC} depends inversely on the input signal level A_i, Equation (2), whereas the EAGC

loop time constant, τ_{EAGC}, is not and is given by[2]:

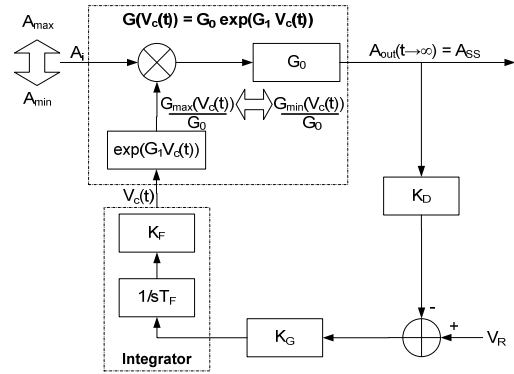$$\tau_{EAGC} = \frac{T_F}{K_F K_D K_G G_1 A_R} \quad (3)$$

Figure 8: EAGC Feedback Loop

Gaussian Noise Generation and Addition to the Signal

A 10MHz bandwidth (nearly white) Gaussian noise (drawn from noise generator, Agilent function generator model 33220A), Fig.9, is used as the input noise to the system.
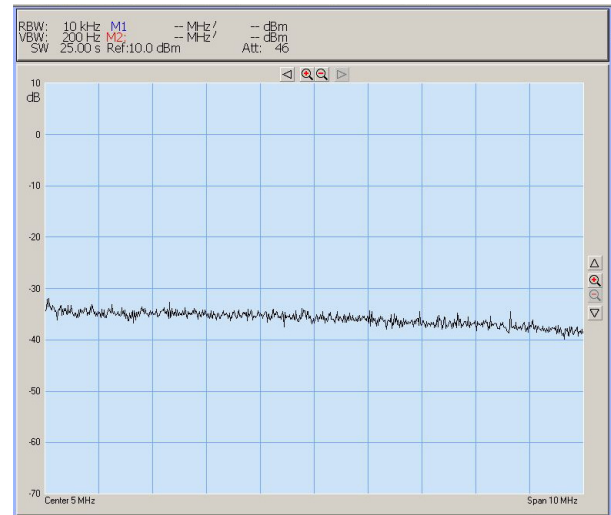

Figure 9: Gaussian Noise Spectrum in 10MHz Bandwidth

The noise is then filtered (band limited) by a FIR LPF with 2MHz bandwidth to avoid aliasing. The filter response is measured approximately by applying nearly white noise, Fig.9, to it and measuring the output, Fig.10.

Calculation of E_b/N_o

The ratio E_s/N_o (also equal to E_b/N_o for MSK modulation) can be calculated by measuring the signal

power P_s and noise power P_n (i.e. by squaring then averaging the sampled signal and noise) and using the values of the symbol rate f_s and the effective bandwidth of noise (EBW) as:

$$\frac{E_s}{N_o} = \frac{P_s}{f_s} \times \frac{EBW}{P_n} = \frac{P_s}{P_n} \times \frac{EBW}{f_s} \qquad (4)$$

EBW is obtained either by integrating the total noise power measured by the spectrum analyzer, Fig.10, and dividing it by the DC noise spectral density or by dividing the total noise power by the average value of the noise spectral density within 2MHz (the latter is larger than the former only by +0.2dB).
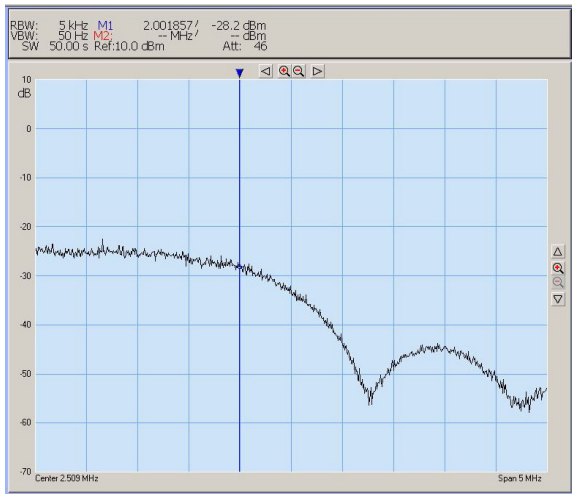
Figure 10: Approximate FIR LPF Response with 2MHz Bandwidth

MSK Carrier and Clock Recovery

In digital communication systems it is required to transmit information with minimum power and efficient use of the spectrum while achieving the lowest possible error rate at the receiver. The communications methods that have the lowest error rate are coherent or synchronous[11 and 12]. Coherency or synchronization means that the receiver can regenerate a local signal that is frequency, phase and clock coherent with the received signal. Transmitting the carrier is inefficient from power point of view, so most of the communications techniques suppress the carrier and locally recover the carrier and clock using the suppressed carrier signal. The receiver's circuit that generates the carrier and clock signals is called signal synchronizers. PRS sequence synchronization is also required in DS-SS.

We will consider here phase/frequency and PRS/symbol synchronization (usually implemented using some form of PLL and correlators, respectively). The

PLL automatically tunes its center frequency to (or to multiple of) that of the input signal.

A phase shift keying (PSK) coherent demodulator uses the locally recovered carrier to extract the baseband data. The recovered clock is used to determine the time of sampling the data. This may require over-sampling within the data bit to allow sampling at the appropriate time instant[6, 13, and 14]. The use of correlator or matched filter for the data bits leads to improved SNR when extracting the data[12].

In the following, demodulator/synchronizer design, digital implementation and performance evaluation are presented.

Aided Frequency Acquisition

For satellite communication links, aided frequency acquisition is employed by using separate carrier acquisition block which estimates the Doppler shift within a predetermined time. If the signal spectrum is analyzed by Fourier transform and the frequency of maximum power is selected, we can (almost) determine the instantaneous frequency deviation at this moment and feed it to the LPLL allowing it to operate initially within the lock-in range (i.e. phase error vanishes after one cycle of transient oscillation).

CCSDS states that for category A missions[15], the Doppler shift can usually be predicted to an accuracy of better than ±1 KHz. This estimation has to be delivered to the LPLL's VCO to force the frequency difference to be small, which in turn allows LPLL to avoid the long nonlinear pull-in process. Accordingly, this estimation of the Doppler frequency allows the selection of the lock-in range $\Delta\omega_L$ of the LPLL (should be slightly greater than the frequency resolution of the fast Fourier transform) and then verify B_n requirements. In this way, a good compromise is achieved between safe acquisition (actually done outside the LPLL) and the noise bandwidth.

MSK Frequency Detector

In aided frequency acquisition it is required to estimate the frequency of the received signal within a predefined frequency error (i.e. the frequency resolution of the frequency detector). By making CFFT for the square of the received MSK signal, the discrete frequency components of double the Doppler frequency shift can be determined. The resolution of the estimated frequencies depends on the sampling frequency and the number of waveform samples processed by the CFFT algorithm. The CFFT technique gives a snapshoot of the frequency components existing in a signal in a given period of time. Thus, this technique is used in the applications where the rate of variation of the signal

frequency is much less than the period of loading and processing of the samples. The proposed frequency detector is shown in Fig.11.
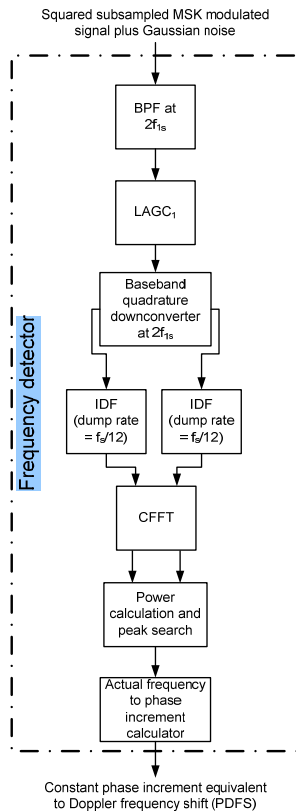

Figure 11: MSK Frequency Detector

After squaring the subsampled MSK modulated signal, the frequency component (i.e. single tone) with double the lower frequency symbol (i.e. $2f_{1s}$) plus double the Doppler frequency is selected by digital FIR BPF, Fig.12. This filtered frequency component is then downconverted to the baseband by a baseband quadrature downconverter (i.e. multiplies the input signal by quadrature sinusoidal signals with frequency $2f_{1s}$) thus a single tone complex signal with a frequency equal to double the Doppler shift is generated.

The outputs of the downconverter are low pass filtered by integrate and dump filter (IDF) (with bandwidth nearly equal to the maximum expected double the Doppler frequency) to remove the high frequency components and increase the SNR at the input of CFFT. The sampling frequency is reduced after the IDF by the dump rate (12) thus, the frequency step of the generated CFFT power spectrum is the sampling frequency after IDF divided by the number of CFFT points.

The power of the output spectrum from the CFFT block is calculated followed by search for the peak to detect the frequency component that is equivalent to double the Doppler shift. The normalized CFFT frequency is converted to actual frequency (by the actual frequency to phase increment calculator block) which is used to generate the phase increment equivalent to double the Doppler frequency shift (PDFS), which will be fed to the LPLLs. It is to be noted that the CFFT does not detect the sign of the Doppler frequency and this information is defined from the satellite motion whether approaching (+ve) or going away (-ve) from the ground station (e.g. can be obtained from the estimated satellite trajectory or through orbit propagator).
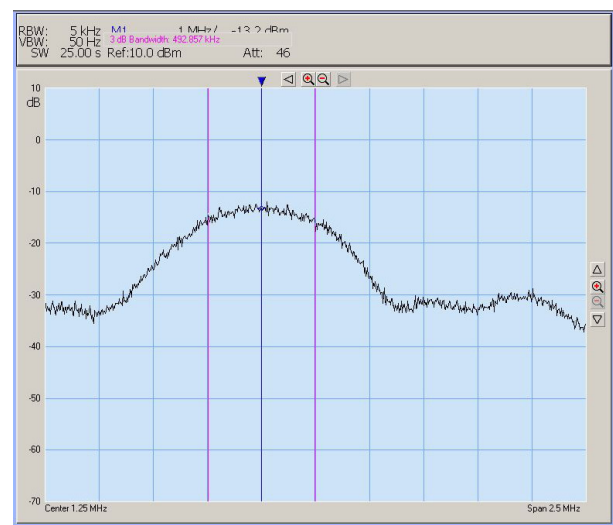

Figure 12: FIR BPF Approximate Frequency Response, Bandwidth ≈ 500KHz

LPLL

Conventional carrier and clock recovery use some forms of PLLs[12 and 16]. The data modulating the carrier should be first removed in order for the PLL to operate on a single tone continuous phase sinusoidal signal. Removal of the data can be implemented using training pattern or the extracted data by the demodulator or remove the data with other aids[6, 12, and 14].

MSK synchronizer uses squaring element to remove the data since the symbol frequencies assume only 2 states, which are f_1 and f_2[17 and 18]. The squaring element generates $2f_1$ and $2f_2$ at non-overlapping instants which are used to drive two LPLLs. The derived $2f_1$ and $2f_2$ can be added and subtracted to recover the synchronized carrier ($4f_o$) and clock (2 chip clock). The actual frequencies are obtained by dividing by 4 and 2, respectively.

The division of the frequency by 4 introduces phase ambiguity of multiple of ±90° between the locally generated carrier and the received one. This leads to

sign ambiguity (for phase ambiguity of $\pm180^o$) in the extracted data and phase ambiguity (for phase ambiguity of $\pm90^o$ and $\pm270^o$) in the locally generated carrier. These ambiguities can be removed by employing training pattern (e.g. PRS) to detect ambiguity[19].

Fig.13 illustrates all blocks of the proposed digitally implemented LPLL which are: phase detector PD, proportional and integral filter (PIF) with proportional and integral branches gains, and direct digital synthesizer (DDS) with phase increment M_{DDS}. IDF is added to average the PD output during the dump period since the generated double MSK symbols' frequencies does not exist in the received signal all the time (e.g. squared MSK signal). In addition, it accumulates the small phase errors from PD, which may be lost by shifts to right in PIF. It also reduces the processing rate in the PIF for the error signal which is basically a low frequency signal.
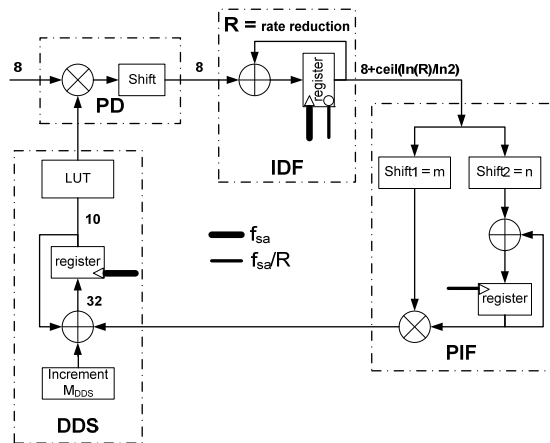
Figure 13: Digital Implemented LPLL

An equivalent analog carrier and clock recovery circuit compared to the proposed structure in this paper, shown in Fig.14, was first proposed by Buda[18] for the synchronization of fast frequency shift keying (FFSK, or equivalently MSK) signals. The proposed structure takes advantage of the fact that the spectrum of the square of binary CPM signals with index 1/2 contains two tones ($2f_1$ and $2f_2$) separated in frequency by the symbol rate ($1/T_s$). The phases corresponding to these two frequencies can be added and subtracted to obtain quadruple the phase of the carrier ($8\pi f_o t$) and the phase of the chip clock ($\pi t/T_s$), thus estimates of the phases of the carrier and chip clock can be obtained.

Some restrictions for Buda's analog approach were stated in[20]:

- The bandwidth of the two PLLs can't be made arbitrarily small (to account for Doppler shift).

- Difficulty of acquiring signals with a large Doppler uncertainty by comparison to the data rate.

However, these restrictions are overcome in the proposed structure as follows:

- By using aided frequency acquisition (as proposed), we can arbitrarily use very small loop noise bandwidths by employing high resolution CFFT. The noise bandwidth can be further reduced to a lower value after initial frequency acquisition.
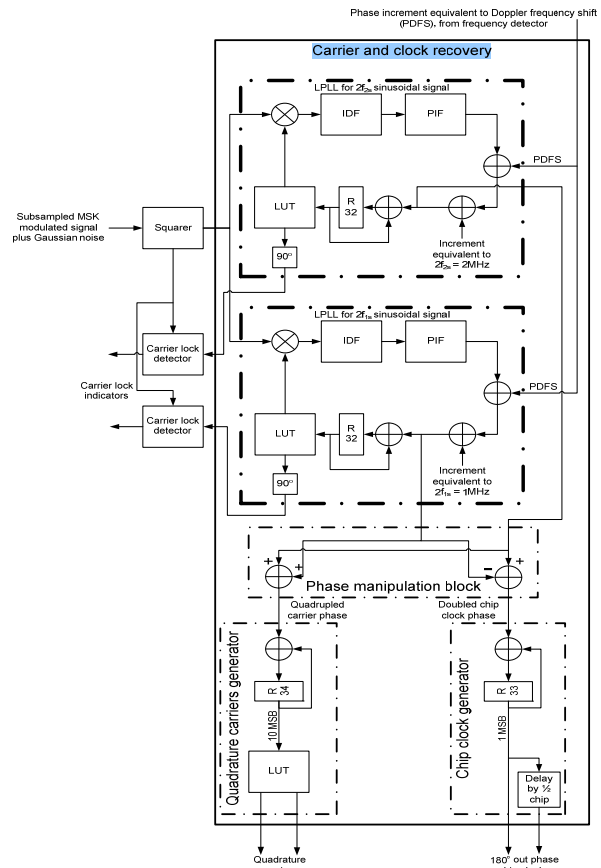- Large Doppler frequency can be estimated by using CFFT and compensating it in LPLL.

Figure 14: Carrier and Clock Recovery

Phase Ambiguities Solver and PRS Code Acquisition

To resolve phase ambiguities, two independent PRSs are used to modulate I and Q channels of the received signal, i.e. actually act as unique words for resolving of phase ambiguities[19]. These PRSs must possess low cross-correlation because the phase ambiguities solver exploits the results of correlation of the demodulated and locally generated PRS to identify the codes in I and

Q channels. The employed PRSs are preferred pair of Gold codes and have low cross-correlation.

Phase Ambiguity Solver

Two functions of phase ambiguities solving and PRS code acquisition are merged in one block. The PhA solver algorithm, Fig.15, is summarized as follows:

1. The received and locally generated PRSs are multiplied in the demodulator block, Fig.3, and the resulting signals (i.e. BS_I and BS_Q) are integrated over ten PRS patterns.
2. If correlation peak is detected, check its sign and correct if required (using control signals for the extracted data sign correction).
3. If correlation peak is not detected, check if step 1 is processed N_{PRS} times (code length) with one chip shift each time (in the demodulator block).
   3.1. If not, shift local PRSs (I_{gen} and Q_{gen}) by one chip period and repeat step 1.
   3.2. If yes, then correlation peak is not detected and phase ambiguities exist, thus:
      3.2.1. If the four alternatives phase ambiguities possibilities are scanned, go to frequency detection mode
      3.2.2. If the four alternatives are not scanned, change to a new combination of the router switches (one of the four possible phase ambiguities) and go to step 1.
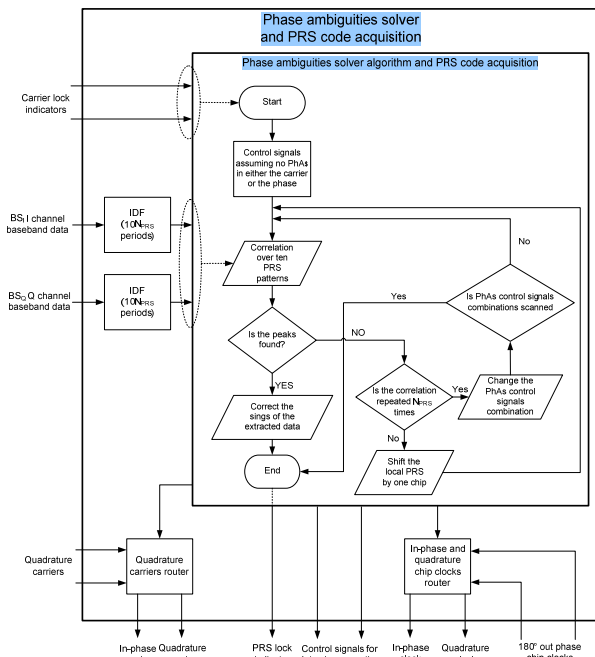
Figure 15: Phase Ambiguities Solver

FPGA IMPLEMENTATION

The digitally generated type II MSK modulated signal has 1MHz symbol rate (0.5MHz chip rate in the quadrature channels) and apparent nominal carrier frequency located at 5.75MHz, thus the two generated MSK symbols have frequencies $f_1 = 5.5$MHz and $f_2 = 6$MHz. The main lobe bandwidth for this signal is (1.5×1MHz = 1.5MHz) centered at the apparent carrier. For purpose of illustration, the shown spectrum of type II MSK modulated signal in Fig.16 is for very long PRSs (i.e. simulates random data) which have maximum length of 168.
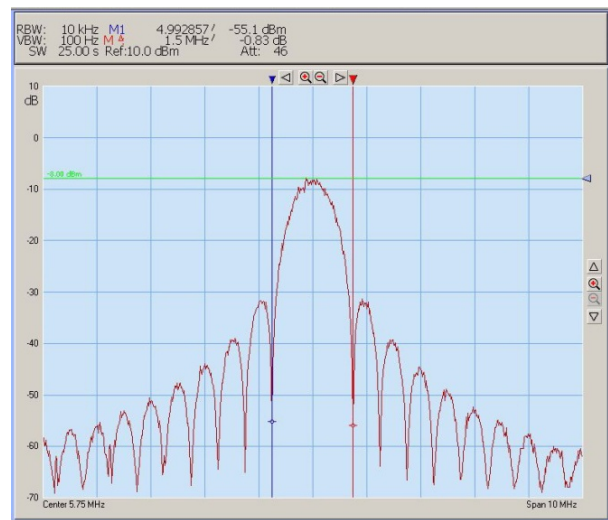

Figure 16: Spectrum of MSK Modulated Signal with Random Data

A 50KHz frequency shift is added to the apparent carrier to simulate the existence of Doppler shift, thus the MSK symbol frequencies become $f_{1D} = 5.55$MHz and $f_{2D} = 6.05$MHz and the apparent carrier frequency is located at 5.8MHz with the same main lobe bandwidth for the MSK modulated signal without Doppler shift, Fig.17. The non-smooth spectrum of the type II MSK modulated signal, Fig.4, with notches separated by 0.5MHz (compared to a smooth spectrum of the type II MSK modulated signal, Fig. 16, may be attributed to the existence of the repetitive pattern of the I and Q modulating data streams (i.e. the used preferred pair of m-sequences (Gold code)) rather than a random sequence. Properties of the employed preferred pairs of Gold codes can be found in[1].

HPF

To evaluate the digitally implemented HPF performance, the MSK modulated signal, Fig.16, is used as a test signal.
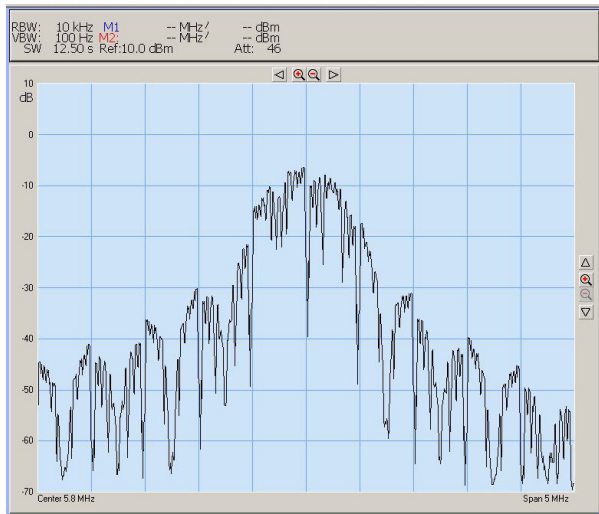
Figure 17: Spectrum of MSK Modulated Signal by I and Q Modulating PRSs

Fig.18 shows the input, output and DC component of HPF captured from FPGA with maximum digital levels of (+6383,-6661), (+6517,-6517) and 139 respectively. It is verified that the DC component is fully cancelled by averaging the sinusoidal signal. It is to be noted that the shown waveforms are subsampling of the 5.75MHz input sine wave by a 5MHz clock, and the cycles that are seen correspond to the first alias of 0.75MHz. The result shown in Fig.18 is taken after HPF operation for 314170 samples (equivalent to 314170 /5MHz = 62.834 ms) to achieve full cancellation of any DC component.
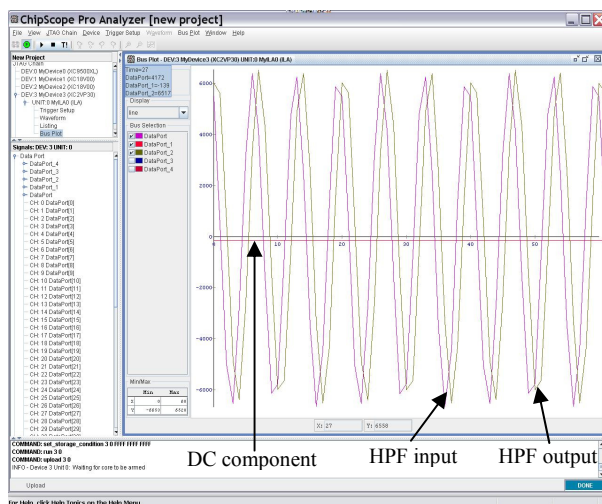
Figure 18: HPF DC Cancellation at Steady State

AGC

The output of the HPF (i.e. DC free MSK modulated signal) of maximum digital level of 6517 is fed to the LAGC and EAGC circuits. Since the sampled peak level is not the same in successive cycles, Fig.18, we

will take A_i as the average for the repetitive maximum sampled levels (6517, 6386, and 6007) which is equal to 6303.

Fig.19 shows the early time transient response of LAGC. The LAGC attack time is identified when the output reaches 63% of the difference between the initial value and the designed steady state value A_{ss} of digital level 106 (i.e. reaches a value $\approx$ 67) at the sample number 1018 (equivalent to 1018/5MHz = 203.6μs). This result agrees with the calculated attack time, Equation (2), which is equal to 209 μs.
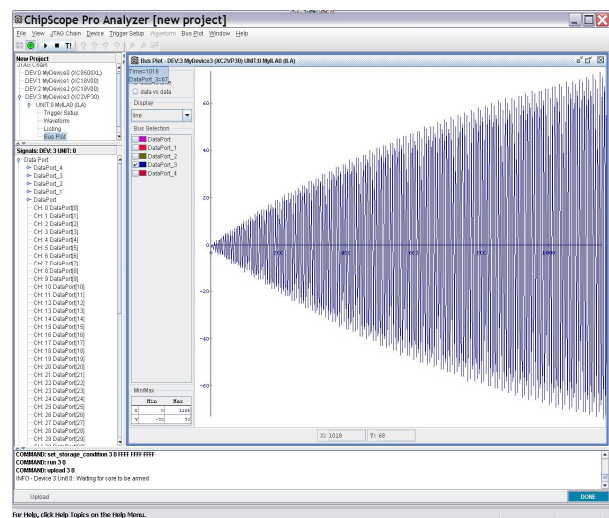

Figure 19: LAGC Output Captured from FPGA (Early Time)

Fig.20 shows the early time transient response of EAGC (with the same input for LAGC). The output reaches level 67 at sample number 6138 (equivalent to time 6138/5MHz = 1.228ms, representing the measured attack time). The designed attack time is given by[2]:

$$t_{exp} = 0.2242 \ln\left(\frac{\frac{106 \cdot 8192}{6303} - 1}{\left(\left[0.63 + 0.37(\frac{6303}{106 \cdot 8192}) \right]^{-1} - 1 \right)} \right) = 1.225 \text{ ms} \quad (5)$$

which agrees with the measured attack time for this design.

The late time (i.e. steady state response) is shown in Fig.21 for LAGC and EAGC where the stabilization of the output amplitude is achieved.

To test the response of the AGC to nonzero initial gain, a sinusoidal input signal of maximum level of 3260 is applied and after 3 ms, a step in amplitude with double the initial value (i.e. 6520) is applied, Fig.22, then a

step with maximum level of 3260 is applied again in a repetitive manner. The responses of LAGC and EAGC to this step in amplitude are shown in Fig.23 and Fig.24, respectively.
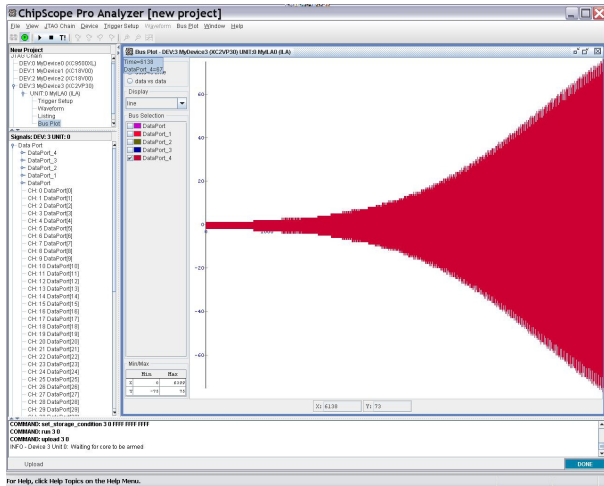

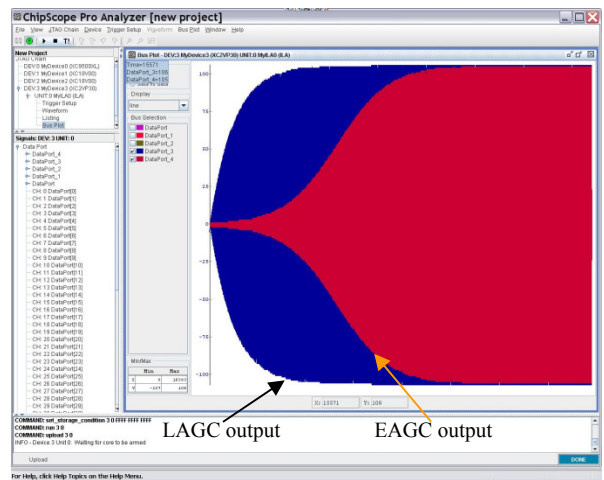**Figure 20: LAGC Output Captured from FPGA (Early Time)**

LAGC output   EAGC output
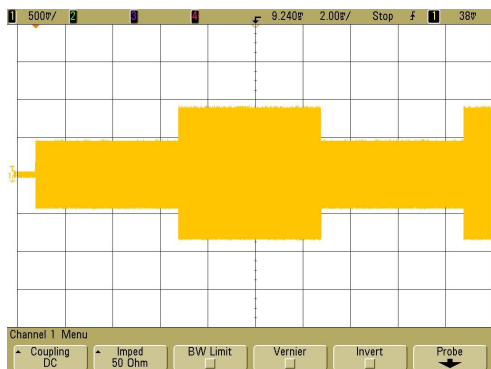
Figure 21: LAGC and EAGC Outputs Captured from FPGA (Late Time)

Figure 22: Step in Signal Amplitude Each 3 ms
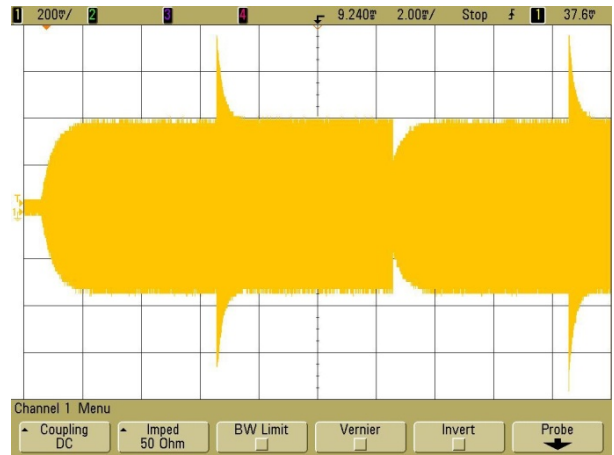

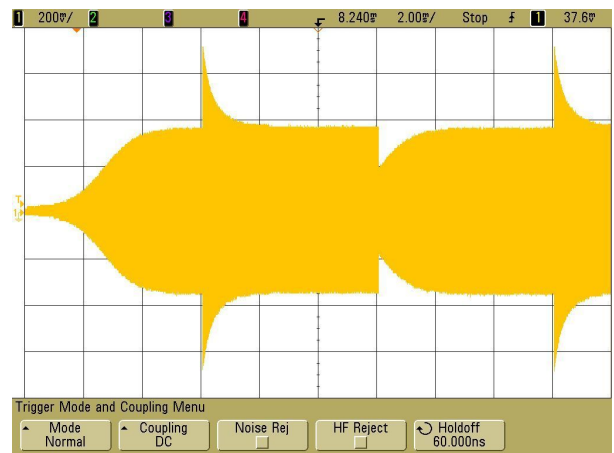**Figure 23: Response of LAGC to Step in Amplitude with Non-Zero Initial Conditions**

Figure 24: Response of EAGC to Step in Amplitude with Non-Zero Initial Conditions

Verification of Signal Suppression Factor Performance

The suppression factor of the tested LAGC with envelope detector, β_{en}, is the ratio of $\hat{A}$ in the presence of noise with the signal to its value without noise. Thus, β_{en} is measured though measuring the gain with the signal alone G_A and with the signal plus noise G_{A+N} and is given by:

$$\beta_{en} = \frac{\hat{A}_{A+N}}{\hat{A}_A} = \frac{G_A}{\hat{G}_{A+N}} \qquad (6)$$

The signal suppression factor can be determined by dividing the LAGC gain, at steady state, for only signal by that for a signal in presence of noise with certain SNR. The selected values for SNR start from 10.5dB and end with -5.5dB with 1dB step. Fig.25 shows the measured signal suppression factor curve for the digitally implemented LAGC with envelope detector.
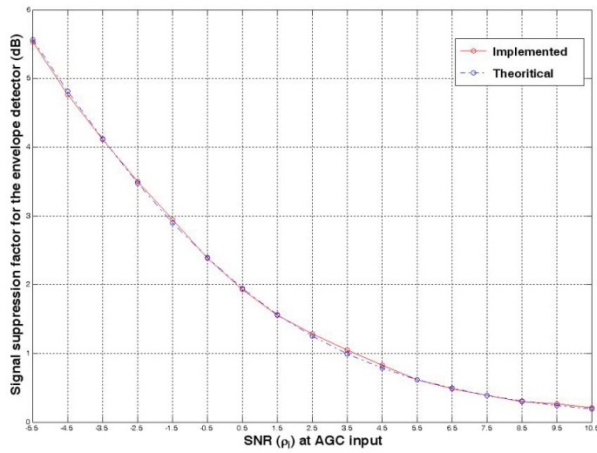
Figure 25: Measured vs. Theoretical β_{en} for LAGC with Envelope Detector

The estimated signal level Â in the presence of only noise at the input of LAGC with envelope detector is given by2:

$$\hat{A}(t) \approx \sqrt{\frac{\pi}{4}}\sigma_n \qquad (7)$$

In practice, the value of the input noise to the LAGC from the preceding stages should be known and can be verified, Equation (7), by measuring LAGC gain, at steady state, after turning on the receiver thus, Â (and in turn the noise variance σ^2_n) can be estimated.

Noise variance measurement is achieved using Equation (7) and is verified for the implemented LAGC as follows. An input noise signal with known σ^2_n is applied to the LAGC block and the transient response for the output signal and the gain build up are shown in Fig.26.
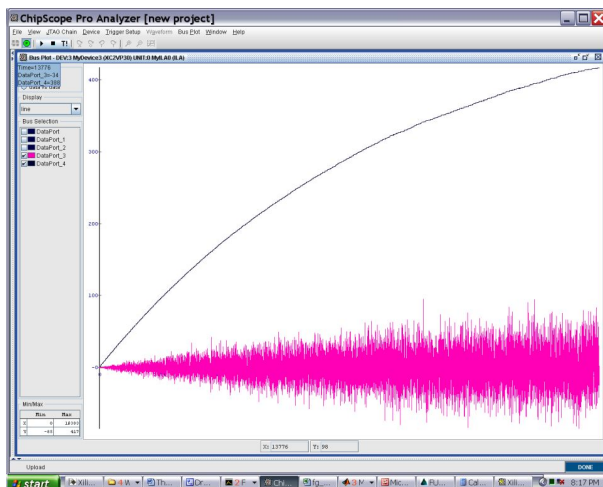

Figure 26: Gain Buildup for -10.5dBm Input Gaussian Noise

The corresponding steady state values are shown in Fig.27. The estimated signal level Â is obtained from the relation Â = A_{ss} / G, where the gain is found to be $v_c \times G_o$ = 507/8192.
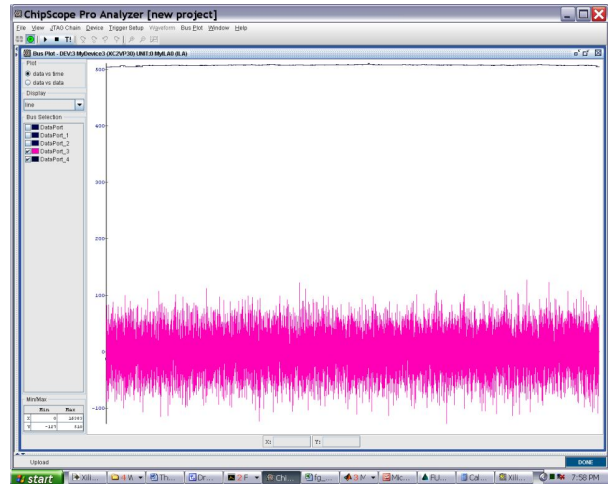

Figure 27: Stabilized Gain and LAGC Output for -10.5dBm, Gain = (507/213)

PLL

A digitally generated single carrier at 5.8MHz is fed to an ADC clocked at 5MHz thus, subsampling process is performed. This subsampled signal is then used as the input to the LPLL. Subsampling process generates spectrum of aliases of the subsampled carrier according to f_{alias} = ±f_{input} ±$pf_{sampling}$ (p = 0, 1, 2 …), Fig.28.
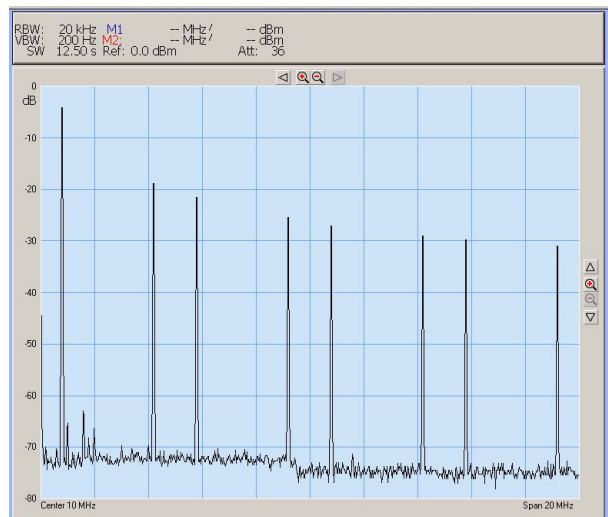

Figure 28: Spectrum of Aliases of the Sub-sampled 5.8MHz Sinusoidal Waveform

The nearest alias to DC is located 0.8MHz (5.8 – 5 = 0.8MHz) which has almost all the power of the subsampled signal.

The designed loop dynamics parameters for the digitally implemented LPLL, Fig.13, are: $\zeta=0.7$, $B_n=28.8$ Hz, and $\omega_n=54.6$ rad/sec.

The response to step in phase of the LPLL is shown in Fig.29. The measured transient oscillation period (≈ 160 ms) agrees with that calculated (IDF rate = 5 KHz).
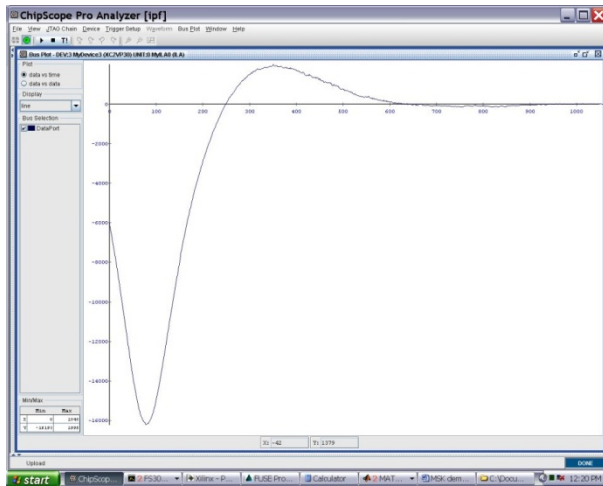

Figure 29: LPLL Transient Response ($\zeta = 0.7$)

Pull-in process is also verified by applying 50Hz frequency shift to the locally generated 0.8MHz carrier. The pull-in time is given by[2]:

$$T_p \approx \frac{\pi^2 (4\zeta^2 + 1)^3 \Delta f^2}{256 \zeta^4 B_n^3} \qquad (8)$$

which is equal to 435ms (equivalent to 2175 cycles of IDF, each cycle = 0.2ms), Fig.30.
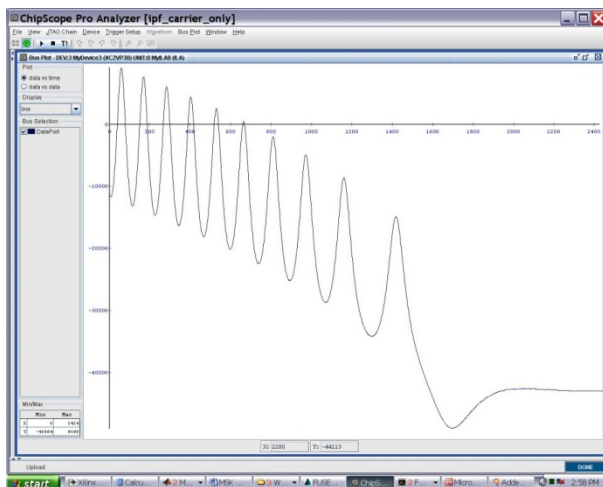

Figure 30: Pull-In Process for 50Hz Frequency Shift ($\zeta = 0.7$)

MSK Frequency Detector

Due to existence of 50 KHz frequency shift in the type II MSK modulated signal, Fig.17, (i.e. 100KHz after squaring) the CFFT frequency detector detects this shift, and its output is shown in Fig.31 for $E_b/N_o = 0$ dB. The peak power is found at the normalized frequency component number 778 where the actual value for this component is ≈ 100.09766 KHz.
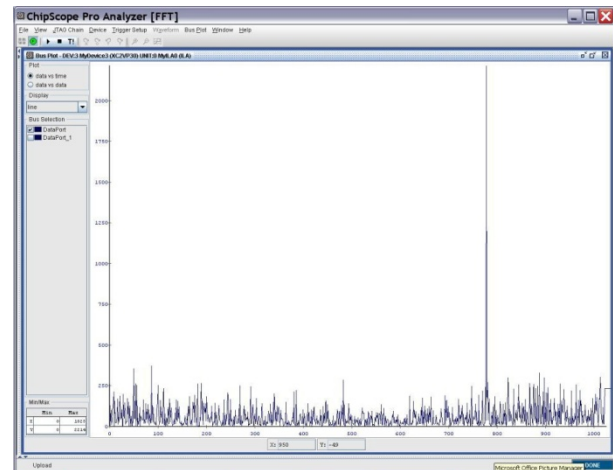

Figure 31: CFFT Spectrum for 100KHz Doppler Frequency Shift, $E_b/N_o = 0dB$

Extracted Carrier

Fig.32 shows the phase noise profile for the extracted I carrier by the MSK carrier and clock recovery, Fig.14, for $E_b/N_o = 0dB$.
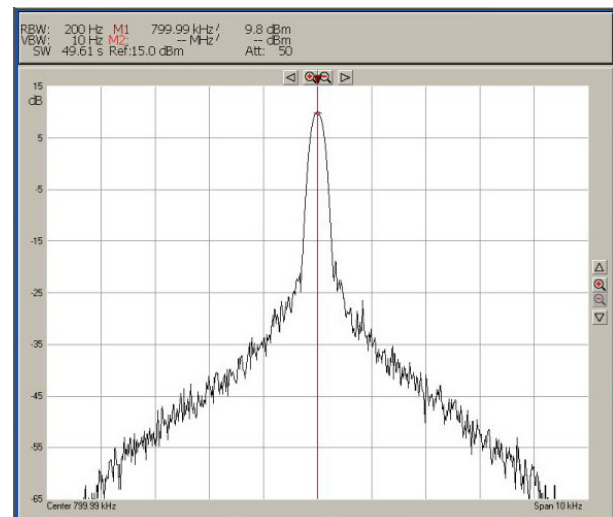

Figure 32: Phase Noise Profile for the Locally Generated Carrier, $E_b/N_o = 0dB$

The phase variances for the carrier and clock are calculated for different values of E_b/N_o starting from

0dB and ending with 40dB with step of 5dB. Fig.33 shows the measured phase variances for the carrier and chip clock and the Modified Cramer Rao bound (MCRB) of carrier phase. MCRB for the phase variance is given by[21]:

$$MCRB(\theta) = \frac{B_n T_S}{E_b / N_o} \qquad (9)$$

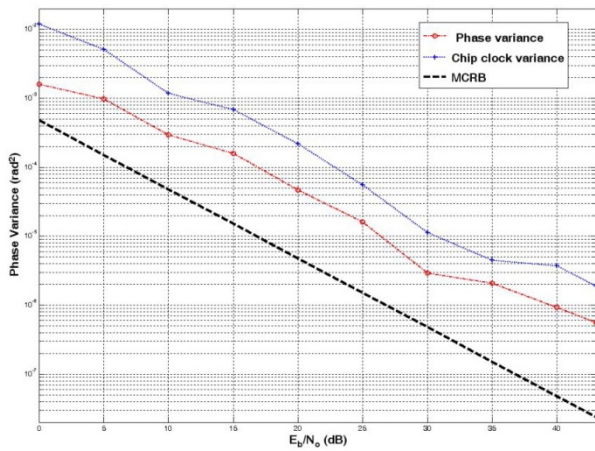In this design, MCRB $\approx 478 \times 10^{-6}$ where $B_n = 478$, and $E_b/N_o = 0$dB.

Figure 33: Measured Carrier and Chip Clock Phase Variances

PRS Acquisition

For purpose of illustration, Fig.34 shows correlation spectrum of the preferred pair of Gold codes during search for the peak but without stopping when acquiring the peak,.
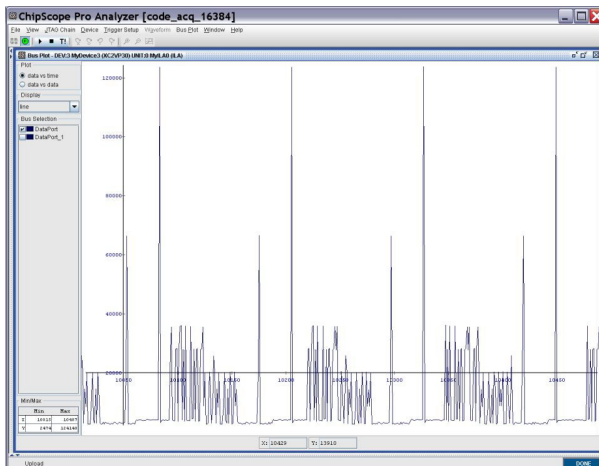

Figure 34: Preferred Pairs of Gold Codes Correlation Spectrum

The resulting absolute values of the correlation spectrum are: a peak if codes are coincident, 0.5×peak if the codes are shifted by half chip, 3 levels with maximum value of ≈ 0.3×peak if the codes are different (i.e. there is carrier phase ambiguity by 90° or 270°), or 5 levels with maximum value of ≈ 0.3×peak or less if the codes are different and shifted from each other by half chip.

Fig.35 shows the correlation spectrum during searching for the peak while $E_b/N_o = 0$dB and it shows stopping the search and in turn stopping to adjust the control signal, Fig.2, when it acquires the correlation peak.
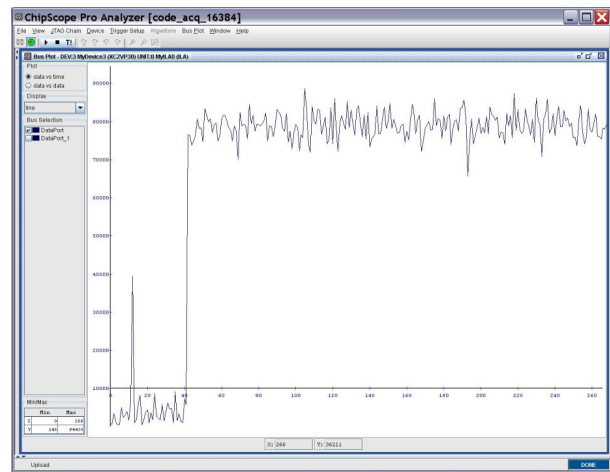

Figure 35: I Channel PRS Code Acquisition, $E_b/N_o=0$dB

Data Extraction and BER Performance

By the end of the phase ambiguities solver algorithm (i.e. when the PRSs lock indicator is equal to logic one) the I and Q carriers and the 180° out of phase chip clocks are routed correctly to the demodulator and thus the demodulated data represents the I and the Q baseband signals. Fig.36 shows the spectrum of the in-phase demodulated baseband signal I_{demod}, Fig.3, whose spectrum lies between 0Hz and 0.75MHz. This results due to folding of half the main lobe of the subsampled MSK modulated signal on itself at the centre after multiplication by the I carrier.

The errors in the extracted chips in either I or Q channels are equivalent to the symbol error probability (SEP). Thus, to measure the SEP, the signs of the extracted chips are compared with those generated locally in the demodulator and the numbers of erroneous chips are counted. The numbers of compared chips is 10^9 to obtain reliable values for SEP. SEP curve is calculated using different values for E_b/N_o stating from -0.2 dB and ending with 9.8dB with 1dB step, Fig.37.
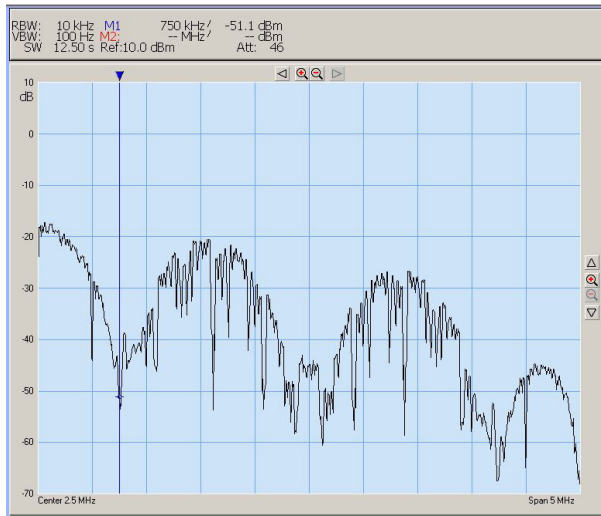
RBW: 10 kHz M1   750 kHz/ -51.1 dBm
VBW: 100 Hz M2;   -- MHz/   -- dBm
SW 12.50 s Ref:10.0 dBm   Att: 46

Figure 36: Spectrum of In-Phase Demodulated Baseband type II MSK Signal
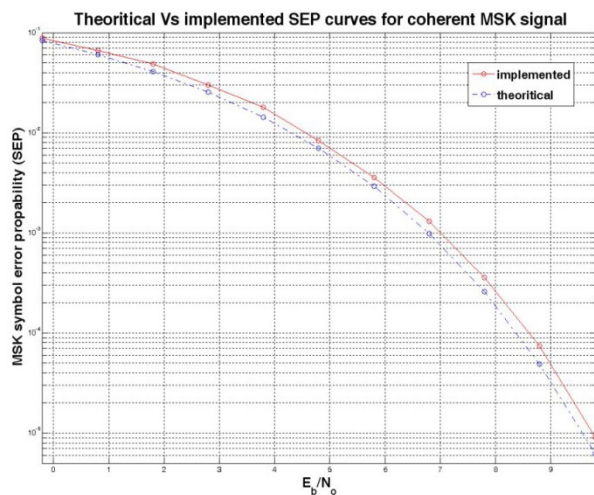

Figure 37: SEP for the Implemented Coherent Type II MSK DS-SS Modem

It is to be noted that there is less than 0.3dB difference between the theoretical and the implemented curves for SEP and it is due to implementation loss[14]. It is to be noted that the calculated values for E_b/N_o may be larger by +0.2dB than the value calculated here (depending on the way to define the EBW) thus there will be at most 0.5dB difference between the theoretical and the implemented curves for SEP.

RESULTS AND DISCUSSIONS

This thesis investigates the design, implementation and testing of a coherent MSK DS-SS modem, suitable for satellite communications. MSK has the advantage of being constant envelope modulation with relatively narrow bandwidth while DS-SS provides low power

spectral density and allows accurate ranging of satellites.

The modulator implements type II MSK modulation, in which the modulation is performed using sine and cosine weighting functions at a frequency equal to half the chip rate. For type II MSK modulation, positive half cycles of the sine and cosine functions are used. The I and Q spreading codes are implemented as a preferred pair of m-sequences (Gold code) with low cross correlation[1]. The spectrum of type II MSK modulated signal is verified, with good results.

Laplace transform analysis is used for the modeling and designing of HPF, AGC and LPLL as a semi-continuous time system and the results are used to obtain the discrete-time circuits parameters assuming that the sampling frequency is much higher than the fastest transients in each circuit.

The AGC is preceded by a HPF to remove any DC component which may be generated.

Two types of AGC are considered, with linear and exponential gain characteristics (the latter is employed in the digitally implemented modem). The response of LAGC to input step amplitude is exponential with a time constant that is inversely proportional to the input amplitude step. This is a drawback since the response to a small input step becomes slow. EAGC has a transient response which depends weakly on the input signal level. The transient behavior is tested and found to agree with the designed response.

Signal level suppression at LAGC output is measured in the presence of added band-limited (nearly white noise) and the results are used in the design of LPLL and the method is used to determine the E_b/N_o for BER measurement.

Input noise variance measurement at the input of the digitally implemented LAGC with envelope detector is achieved and verified. The gain value of LAGC, at steady state, in response to the input noise is proportional to the input noise power. This information could be used in receiver self-test and/or as a telemetry data for the receiver performance. The author suggests including in-flight noise power measurements at the demodulator input as a telemetry data in CCSDS TM/TC recommendations and/or reports.

The proposed type II MSK DS-SS synchronizer consisting mainly of a squaring element and two LPLLs. The squaring element removes the sign variation of the symbol signals due to the modulating bits. Two LPLLs operating at twice the MSK symbols' frequencies are used to recover these frequencies. By

adding and subtracting the phases of these frequencies, the quadruple of the carrier frequency and double the chip frequency are generated, from which the carrier and chip frequencies are generated. The generated carrier may have a phase shift w.r.t. the received signal of multiples of $\pm90^o$. The generated and received chip frequencies may have a phase shift of $\pm180^o$. Such ambiguities are resolved by using a circuit based on correlating the receiver code in either I or Q channels with the locally generated one.

The LPLL consists of multiplier phase detector, IDF, PIF and DDS. The IDF is mainly used to average phase error in the LPLL (since each symbol frequency does persist all the time) and to reduce the processing rate in the LPLL feedback loop. The use of the PIF allows the loop to respond to an input step in frequency with zero steady state phase error. The LPLL loop is designed to have a damping factor of 0.7 which leads to maximally flat frequency response, and accordingly a stable loop with relatively fast response. The loop natural frequency is chosen to provide a lock-in range greater than the uncertainties of the input frequency, which is determined using a CFFT function. The natural frequency leads also to a narrow loop noise bandwidth such that the loop SNR is high, i.e. loop unlocks are infrequent. The transient response of the error signal in the LPLL is tested and found to agree with the designed performance. The carrier and clock variances are measured versus E_b/N_o and the phase standard deviation is found to change from $10.4°$ to $4.45°$ for the carrier for E_b/N_o change from 0dB to 10dB, and the clock phase changes from $28.3°$ to $8.9°$ for the same range of E_b/N_o. The phase variances are nearly inversely proportional to E_b/N_o at low values of E_b/N_o, and contain self noise at high E_b/N_o.

A novel phase ambiguity solver algorithm is investigated and the data extraction is done using matched filters (implemented using correlators). The phase ambiguities solver and PRS code acquisition block performs correlation of the received and locally generated PRS codes. The combination of the carrier and chip clock phases leading to maximum correlation is the correct one thus, phase ambiguities are resolved.

The BER for the extracted PRS is measured and found to be nearly identical to the theoretical one with slight degradation due to the small phase variances and implementation losses. The BER for baseband data (rather than for PRS) can be determined by adding 10 $\log_{10}(PG)$ to SEP (dispreading process). Calibration to BER curve should be done to obtain a reference when modem verification is required or during receiver self-test.

Software and Hardware Setup

XtremeDSP development kit pro is used for the digital implementations. It contains:

- Xilinx VirtexII Pro (XC2VP30) main user FPGA
- Two ADCs (105 MSPS)
- Two DACs (160 MSPS)
- Xilinx VirtexII (XC2V80) user clock FPGA

Design, simulation, implementation and testing software from Xilinx and Nallatech are used in the development of the modem.

ISE software is used for FPGA development (design and implementation) and Fuse software (Nallatech) for FPGA configuration and interfacing with PC, ModelSimXE III for digital simulation and ChipScope Pro together with Xilinx parallel cable for FPGA debugging. FS300-K1 remote control/PC software is used to control and capture data from Rohde & Schwraz FS300 spectrum analyzer.

The used hardware testing instruments are:

- Rohde & Schwarz, spectrum analyzer FS300 (9KHz→3GHz)
- Agilent digital storage oscilloscope (DSO) model DSO06034A
- Agilent function/arbitrary waveform generator model 33220A, which is used as a noise source

Table 1 shows device utilization summary for the implemented coherent MSK DS-SS modem on Virtex-II Pro user FPGA XC2VP30.

Table 1: Implemented Coherent MSK DS-SS Modem FPGA Resources Utilization

Resources	Utilization	Percentage
Number of slices	2923 out of 13696	21%
Number of RAMB16s	11 out of 136	8%
Number of MULT18X18s	44 out of 136	32%
Number of BUFGMUXs	7 out of 16	43%
Number of external IOBs	86 out of 644	13%
Number of DCMs	1 out of 8	12%

Suggestions for Future Work

Future work may include the following:

a) To use alternative code acquisition and tracking methods.

b) Investigate employing of AGC with power detectors.

c) Implement exponential gain characteristics AGC with optimized use of resources.

d) To use realistically long and complex pseudo random sequences including nonlinear sequences and composite sequences.

e) To investigate employing coded modulation techniques.

f) To study cycle slip in the LPLL. To use a third order LPLL loop to achieve zero steady state error in the presence of a frequency ramp.

g) To model time varying Doppler shift and input signal level.

References

1. Maghawry, A. and E. Eldiwany, "FPGA-Based MSK DS-SS Modulator for Digital Satellite Communications," 23rd Annual AIAA/USU Conference on Small Satellites, SSC09-VI-11, August 2009.

2. Meyer, H. and G. Ascheid, Synchronization in Digital Communications, Volume I: Phase-, Frequency-Locked Loops, and Amplitude Control, John Wiley & Sons, 1990.

3. Reed, J. H., Software Radio: A Modern Approach to Radio Engineering, Pearson Education, 2002.

4. Rohde, U. L. et al, Communications Receivers: Principles and Design, McGraw-Hill, 1997.

5. Peterson, R. L. et al, Spread Spectrum Communications, Prentice Hall, 1995.

6. , Mengali U. and A. N. D'Andrea, Synchronization Techniques for Digital Receivers, Kluwer Academic/Plenum Publishers, 1997.

7. Bateman, A. and L. Paterson-Stephens, The DSP Handbook: Algorithms, Applications and Design Techniques, Prentice Hall, 2002.

8. Simon, M. K. et al, Spread Spectrum Communications Handbook, McGraw-Hill, 2002.

9. Parkinson, B. W. et al, Global Positioning System: Theory and Applications, Volume I, Chapter 8, American Institute of Aeronautics and Astronautics (AIAA) , 1996.

10. Intersil Co., Programmable Downconverter, HSP50214B, May 2000.

11. Razavi, B., RF Microelectronics, Prentice Hall PTR, 1998.

12. Proakis, J. G., Digital Communications, McGraw-Hill, 2001.

13. Intersil Co., Digital Costas loop, HSP50210, January 1999.

14. Meyr, H., M. Moeneclaey and S. A. Fechtel, Digital Communications Receivers: Synchronization, Channel Estimation, and Signal Processing, John Wiley & Sons, 1998.

15. Consultative Committee for Space Data System, Radio Frequency and Modulation Systems, Part 1 Earth Stations and Space Craft, May 1998.

16. Franks, L. E., Carrier and bit synchronization in data communication – A tutorial review., IEEE Trans. Com., pp. 1107-1120, Aug. 1980.

17. Spilker, J. J., Digital Communications by Satellite, Prentice Hall, 1977.

18. Buda, R., Coherent demodulation of frequency-shift keying with low deviation ratio, IEEE Trans. Com., pp.429-435, Jun. 1972.

19. Cacciamani, E. R. and C. J. Wolejsza, Phase-ambiguity resolution in a four-phase PSK communications system, IEEE Trans. Com. Tech., pp. 1200-1210, Dec. 1971.

20. El-Tanany, M. and S. A. Mahmoud, Analysis of two loops for carrier recovery in CPM with index ½, IEEE Trans. Com., pp. 164-176, Feb. 1989.

21. D'Andrea, A. N., U. Mengali and R. Reggiannini, The Modified Cramer-Rao bound and its application to synchronization problems, IEEE Trans. Com., pp. 1391-1399, Feb. 1994.