WIDE-BAND GAP DEVICES FOR DC BREAKER APPLICATIONS

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ABSTRACT

Wide-Band Gap Devices for DC Breaker Applications

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With the increasing interest in wide-band gap devices, their potential benefits in power applications have been studied and explored with numerous studies conducted for both SiC and GaN devices. This thesis investigates the use of wide-band gap devices as the switching element in a semiconductor DC breaker. It involves the design of an efficient semiconductor DC breaker, its simulation in SPICE, construction of a hardware prototype and the comparative study of SiC and Si versions of the aforementioned breaker. The results obtained from the experiments conducted in the process of concluding this thesis show that the SiC version of the breaker is a superior option for a semiconductor DC breaker.

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1 INTRODUCTION

In 2015, Information Handling Services (IHS) forecasts 53GW of solar installation globally [4]. An helralded NREL feasibility study in 2012 found that based on the current technology at the time, a more flexible electric grid could meet the entirety of U.S. energy needs with 80% of its power from renewable sources--45% from wind and solar; 35% from biomass, geothermal and hydro; and the rest from nuclear and fossil fuel power sources in the near future [1]. A little less than a century ago, the national grid consisted of one-way alternating current (AC) power flows from the utility companies to the consumer. However, recent technological advances, materials research, decreasing cost of renewable sources (solar power sources at grid parity for huge portions of the U.S. market), federal laws and global warming concerns, have led to increasing adaptation of renewable energy initiatives and distributed generation in most electric grids around the world. The increasingly complex connections between utility companies and customers require a grid with meshed power networks that can handle power flow in multiple directions and forms such as High Voltage AC to High Voltage Direct Current, HVDC to Medium Voltage AC, MVAC, etc. Unfortunately, the non-sinusoidal nature of DC current means it has no natural zero-crossing point. When this is combined with the vast majority of DC-coupling capacitors and significant transmission line inductance in such an interconnected power network, special considerations are needed to ensure grid protection from transmission line faults. A single line to ground fault leads to the application of large voltages across big line inductances plus the discharge of large coupling

capacitors in the grid and corresponding abnormally high current running through the entire power network. Traditionally, in order to prevent the destruction of huge swaths of the grid, AC breakers are used to separate the AC portion of the grid and help clear the fault. Since most AC breakers take five to six cycles prior to opening, this means the DC power network (DC transmission lines, converters) has to be able to withstand increasingly high current for approximately 83ms for a 60Hz system. As inductor current with large positive voltage across it plus a discharging capacitor's current increase very rapidly, a much faster response time is needed to halt the ramping current in order to reduce the amount of fault current and also the recovery time/capacitor recharge time for the grid after a fault. A faster DC breaker is thus needed as voltage-source converters with switches cannot stop the flow of DC fault current by gate block operation due to the presence of reverse conducting diodes parallel to the switch. Due to more DC systems becoming a part of the electric grid as increasingly grid-tied generating sources (as opposed to islanded generating sources), interfacing them with the mostly-AC grid network requires a setup where faults can be quickly diagnosed and surge currents swiftly arrested prior to reaching levels destructive to DC power network equipment.

Furthermore, as the world becomes progressively more interconnected and countries' economies become more intertwined, internet connectivity is becoming more of a need for business and individuals than a luxury. The United States Federal Communications Commission recently reclassified broadband internet access under the same common rules as utilities and currently regulates the

broadband internet networking sector with the same rules as utility companies [8]. As more users require internet access, providing that bandwidth and other internet services (like Storage-as-a-service, cloud computing, etc) means more computer servers, routers, datacenters and their support-infrastructure are needed to meet skyrocketing demand for network access. In 2013, data centers in the U.S. consumed 91 billion kilowatt-hours of electrical energy enough to power all the households in New York city twice, and are forecasted to consume 140 billion kilowatt-hours of electrical energy by 2020 [6]. Presently, only about half of the power supplied to a data center is actually used by the IT (Information Technology) load. The rest is used up by datacenter support-equipment like chillers, power distribution infrastructure to include switchgear, UPS, etc. In order to reduce the significant cost of powering datacenters, various DC topologies have been proposed and designed. These designs aim to help reduce the power consumption of the datacenter by shrinking the number of power conversion stages, therefore increasing power efficiency as each conversion stage contributes some finite power loss involved in the datacenter power distribution architecture. For these DC topologies, dependable DC breakers with low power consumption profiles are needed to maintain safety and maximize efficiency in the IT environments where these datacenters are deployed. This thesis aims to explore DC breaker technology and investigate how wideband-gap devices can improve the performance of a specific breaker topology.

2 BACKGROUND

DC circuit breakers are usually classified into two different categories; mechanical and solid-state DC circuit breakers. A mechanical DC breaker typically consists of three components in parallel; a traditional AC electromechanical breaker, an energy absorbing device and a parallel resonant circuit consisting of capacitor and inductor in series.

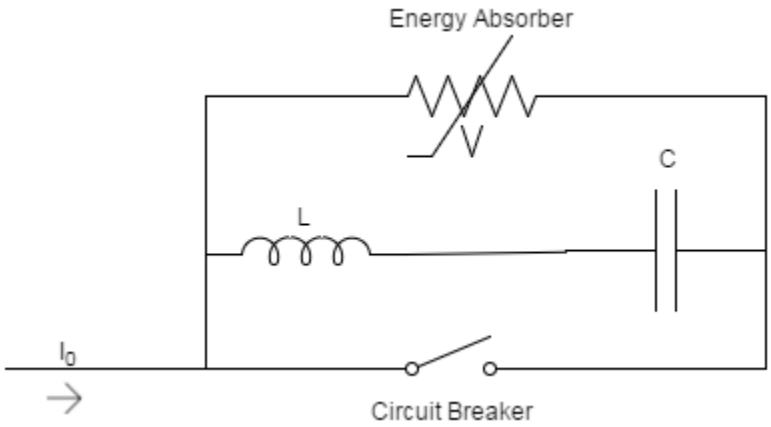

Figure 2-1. Mechanical DC Breaker [9]

The idea is to have the arc that forms when DC current is interrupted excite the resonant LC circuit with its voltage while using the sinuoidal current produced to bring the arc to zero and operate the breaker to isolate the circuit [9]. While the conduction losses of a mechanical DC breaker are almost zero since the metallic conductors the AC circuit breaker is made from have very little resistance, the time to current interruption is typically 30-100 ms. For a voltage-source converter (VSC) power network with low impedance and big DC coupling capacitors, that is too much time for the converter components to withstand a rapidly increasing current prior to the breaker finally opening. As such, a mechanical DC circuit

breaker is not really well suited for a VSC network. However, the method might be satisfactory for current-source converter network.

Conversely, solid-state DC circuit breakers are better suited for power system protection in a DC network due to their much higher speed of operation. The high speed is due to the relatively faster operation of enabling/disabling semiconductor devices when compared to the time required for an electromechanical coil to activate its breaker. This has a significant impact on the amount of down-time for the faulted section of the network as fault currents can be interrupted, cleared and power restored faster. Also, as opposed to taking out the entire DC portion of the network like when system protection involves using AC circuit breakers on the AC side of a mixed-power network, the specific fault sections can be targeted and isolated to increase power availabilty or reliability. However, despite the increased speed that solid-state DC breakers offer, they still possess several inherent properties which may make them still relatively big in physical size and degrade their efficiency. As for any solid state switch, during conduction time the switch will have a finite amount of power less due to its internal resistance. The size of solid-state breakers is also impacted by the operating voltage and current of the system they are connected to. For example, a solid-state breaker may consist of muliple switches/diodes connected in series to withstand the high transmission voltages and currents. This thesis aims to investigate the use of and compare performance of wide band gap power semiconductor devices in place of silicon devices as the solid-state switch component in a DC breaker. Wide band gap devices like Silicon Carbide (SiC) and Gallium Nitrate (GaN) devices have

lower conduction losses, higher thermal conductivity and higher blocking voltages than their silicon counterparts [10]. Incorporating this technology into a solid-state DC breaker could significantly reduce the power transmission losses, device size and increase the efficiency of DC power systems incorporating solid-state DC circuit breakers.

2.1 Traditional DC Breaker

Prior to the work done by Kenichiro Sano and Masahiro Takasaki [11], most of the solid-state DC circuit breaker designs involved a semiconductor switch device in parallel with a surge-absorption device and an inductor as shown in Figure 2-1 [11].

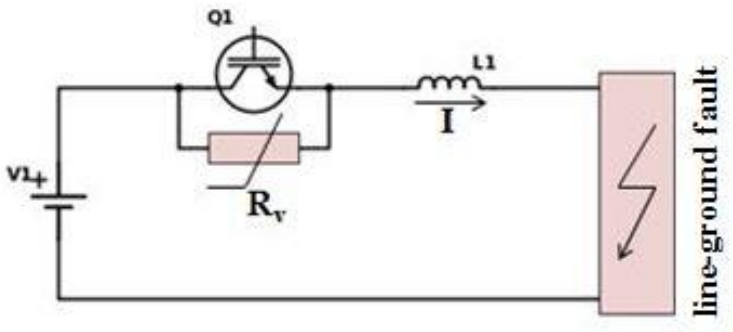

Figure 2-2. Traditional DC Breaker [11]

In this setup, a voltage source V_1 is connected in series with a semiconductor switch (Q_1), an inductor (L_1) and a load. The varistor (R_v) with a clamping voltage (V_{clamp}) is connected in parallel to Q1 and acts as an energy absorption device plus a path for the load current I to commutate to during breaker operation. A varistor allows very little current to flow through it when the voltage across its

ends is low, but when very high voltages are present, it naturally breaks down and very high reverse current flows through it due to very low resistance while maintaining its voltage drop at near-constant values or clamping voltage. This ability of the varistor to non-linearly vary its resistance dependent on voltage makes it attractive as an energy absorption and surge protection component. L_1 represents the overall inductance of the circuit—including the inductances of the DC breaker, the DC transmission line and load being powered.

If a fault occurs at time $t<t_0$, Q_1 is still conducting and has a negligible voltage drop across its terminals. Assuming the fault was detected quickly and Q_1 turned off at $t=t_0$, the increasing fault current in the same direction as I due to location of fault in system commutates to the varistor and the surge voltage across Q_1 is limited to V_{clamp}. As $V_{clamp}>V_1$. From KVL, the voltage across $L_1(V_L)$ is:

$$-V_1 + \mathrm{V_{clamp}} + V_L = 0$$

$$V_L = V_1 - \mathrm{V_{clamp}} = -(\mathrm{V_{clamp}} - V_1)$$

Hence, a negative voltage is applied across L_1 ($V_{clamp}>V_1$) and the fault current decreases from its value I_0 at time $t=t_0$ (assuming $t_0 = 0$) according to the following equation:

$$V_L = L_1 \times \frac{dI}{dt}$$

Equation 2.1;

$$I = \frac{1}{L_1} \times \int_0^t V_L dt = \frac{1}{L_1} \times t \times -\left(\mathrm{V_{clamp}} - V_1\right) + I_0$$

In order to find the time it takes to decrease the fault current to zero (t_f), set I = 0 and equation 2.1 becomes

$$I_0 = \frac{1}{L_1} \times t_f \times \left(\mathrm{V_{clamp}} - V_1\right)$$

Equation 2.2;

$$t_f = \frac{L_1 I_0}{\left(\mathrm{V_{clamp}} - V_1\right)}$$

Therefore, to make the fault current decay to zero faster, we have to make $V_{clamp} >> V_1$. This becomes a problem when we consider that the amount of energy absorbed in the varistor during breaker-opening operation with the total duration of t_f is dependent on the magnitudes of V_{clamp} and V_1.

Equation 2.3;

$$Energy, E_V = \int_0^{t_f} (\mathrm{V_{clamp}} \times I)dt$$

Substituting equations (1) and (2) into (3) yields:

$$E_V = \int_0^{\frac{L_1 I_0}{(\mathrm{V_{clamp}} - V_1)}} (\mathrm{V_{clamp}} \times (I_0 - \frac{\left(\mathrm{V_{clamp}} - V_1\right)t}{L_1}))dt$$

$$E_V = \mathrm{V_{clamp}} \times \left[I_0 t - \frac{\left(\mathrm{V_{clamp}} - V_1\right)t^2}{2L_1} \right]_0^{\frac{L_1 I_0}{(\mathrm{V_{clamp}} - V_1)}}$$

$$= \mathrm{V_{clamp}} \times \left(\frac{I_0^2 L_1}{\left(\mathrm{V_{clamp}} - V_1\right)} - \frac{I_0^2 L_1}{2\left(\mathrm{V_{clamp}} - V_1\right)} \right)$$

Equation 2.4;

$$E_V = \frac{I_0^2 L_1}{2(\mathrm{V_{clamp}} - V_1)} \times \mathrm{V_{clamp}} = \frac{I_0^2 L_1}{2\left(1 - \frac{V_1}{\mathrm{V_{clamp}}}\right)}$$

In other words, the higher varistor's clamping voltage, the smaller the ratio $\frac{V_1}{\mathrm{V_{clamp}}}$ (less than 1 as $V_{clamp} > V_1$) and the higher the energy dissipated in the varistor. Also, the higher V_{clamp}, the higher the voltage blocking rating (and cost) of the switching device Q_1 has to be to prevent device breakdown.

2.2 Freewheeling Diode-Variant DC Breaker

With an objective of addressing the concerns listed above and improving the efficiency of the traditional DC breaker, Kenichiro Sano and Masahiro Takasaki came up with a surgeless DC circuit breaker topology [11] with the varistor in a freewheeling diode path.

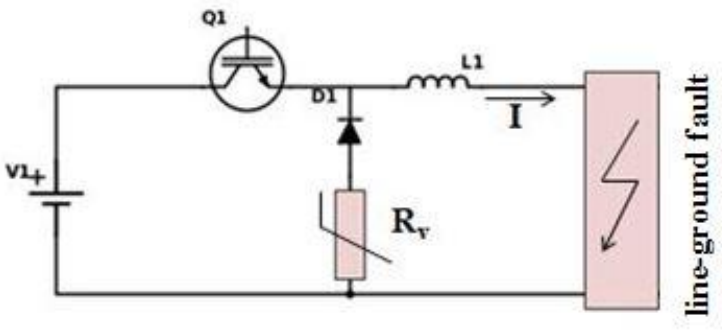

Figure 2-3. Freewheeling diode DC Breaker [11]

Here the voltage source V_1 is connected in series with the semiconductor switch, Q_1, the equivalent system inductance L_1 and load. The varistor R_v is connected

along the path of a freewheeling diode D_1 in the configuration shown in Figure 2-2. When a line fault occurs at time $t<t_0$ with Q_1 conducting, and the fault is detected/Q_1 opened at time $t=t_0$, the fault current I immediately commutates to the freewheeling diode and V_1 stops producing power, and thus quickly protects the VSC converter acting as a voltage source in a VSC-based power transmission application. From KVL on the rightmost loop, assuming an ideal diode with no voltage drop during conduction, the voltage across $L_1(V_L)$ is:

$$\mathrm{V_{clamp}} + V_L = 0$$

$$V_L = -\mathrm{V_{clamp}}$$

Therefore, the current through the inductor decreases with time as V_{clamp} is positive. If $t_0=0$ secs, then

$$V_L = L_1 \times \frac{dI}{dt} = -\mathrm{V_{clamp}}$$

Equation 2.5;

$$I = \frac{1}{L_1} \times \int_0^t V_L dt = \frac{1}{L_1} \times t \times -\left(\mathrm{V_{clamp}}\right) + I_0$$

When I reaches 0 Amps at t_f,

$$I_0 = \frac{1}{L_1} \times t_f \times \left(\mathrm{V_{clamp}}\right)$$

Equation 2.6;

$$t_f = \frac{L_1 I_0}{\left(\mathrm{V_{clamp}}\right)}$$

then, the power dissipated in the varistor becomes

$$E_V = \int_0^{t_f} (\mathrm{V_{clamp}} \times I)dt = \int_0^{\frac{L_1 I_0}{(\mathrm{V_{clamp}})}} (\mathrm{V_{clamp}} \times (I_0 - \frac{(\mathrm{V_{clamp}})t}{L_1}))dt$$

$$E_V = \mathrm{V_{clamp}} \times \left[I_0 t - \frac{(\mathrm{V_{clamp}})t^2}{2L_1} \right]_0^{\frac{L_1 I_0}{(\mathrm{V_{clamp}})}} = \mathrm{V_{clamp}} \times \left(\frac{I_0^2 L_1}{(\mathrm{V_{clamp}})} - \frac{I_0^2 L_1}{2(\mathrm{V_{clamp}})} \right)$$

Equation 2.7;

$$E_V = \frac{I_0^2 L_1}{2}$$

Essentially, all the energy dissipated in the varistor is equal to the energy previously stored in the inductor L_1 for a given line current I_0 at time $t = t_0 = 0$ secs. When compared with equation 2.4, the factor $\frac{1}{\left(1-\frac{V_1}{\mathrm{V_{clamp}}}\right)} > 1$ means less power is dissipated in the varistor for this configuration (note V_{clamp} has no effect on E_v). Although the voltage across the switch Q_1 is $V_{clamp}+ V_1$ when the freewheeling diode is conducting fault current, the actual voltage rating value of V_{clamp} can be set to a really low value as V_{clamp} does not have to be greater than V_1.

2.3 High Voltage Breaker Application and Operation

Using the freewheeling diode topology described in the previous section, two DC breakers A and B are connected between the sending and receiving ends of a typical DC transmission setup as shown in Figure 2-3. The system is configured to convert AC power to DC power then transfer from breaker A to breaker B through a transmission line before converting the received DC power back to AC

via the inverter at the receiving end. Each breaker element has a semiconductor device Q that is a series combination of multiple IGBT units so as to provide the necessary high blocking voltage required for HVDC applications. A similar series arrangement is implemented for the diode device D so as to prevent semiconductor device breakdown at high voltage. The IGBT unit consists of an IGBT (Q_1, Q_2, Q_3,…or Q_n), a parallel reverse-conducting diode (to aid bidirectional current flow), a snubber capacitor (C_{snub}) to help provide zero-voltage switching during breaker tripping operation and a resistor R_{snub} to assist with voltage balancing at breaker reclosing. The diode unit consists of a semiconductor diode (D_1, D_2, D_3,…or D_n), in parallel with a balancing resistor R_D while S_D represents a low-current mechanical switch in series with a diode forcing fault current to flow through the diode device D. This way S_D helps with line deionization and insulation recovery. The varistor device R_V is connected in the freewheeling diode path and the two symmetrical breakers are connected in a way to protect against a fault in the transmission line between them.

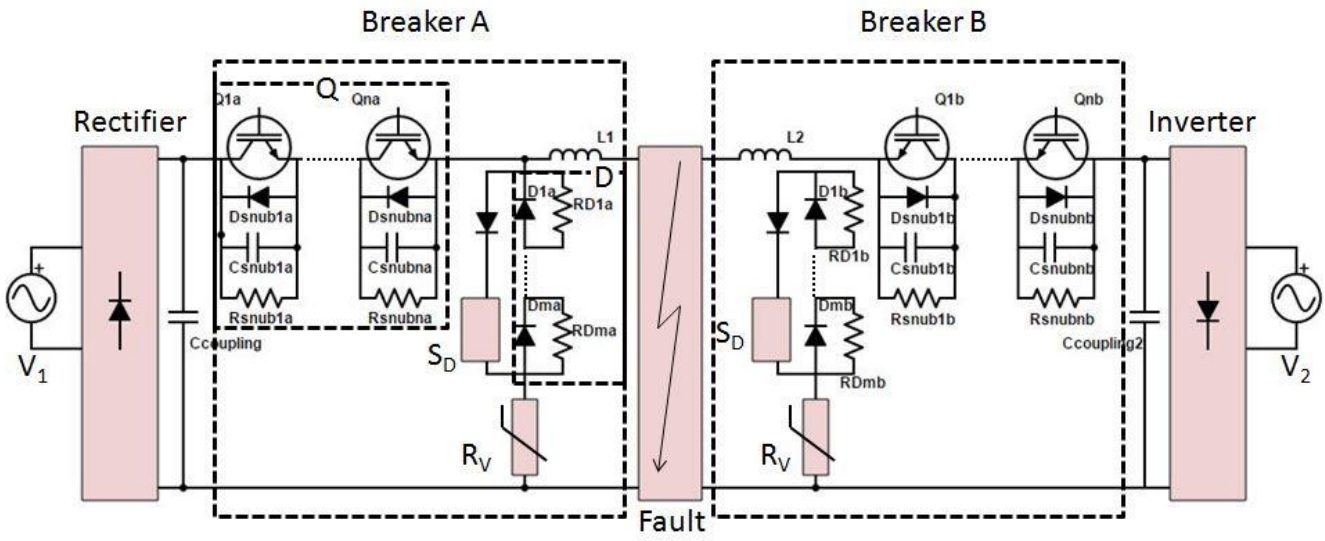

Figure 2-4. High Voltage Freewheeling Diode DC Breaker

2.3.1 High Voltage Breaker A Opening(Fault Current Interruption)

For the configuration described above, normal system operation has Q on with load current flowing from circuit breaker A to circuit breaker B, and no current through D. When a fault occurs on the transmission line as depicted in Figure 2-3, the coupling capacitors start discharging and this leads to a rapid increase in the current flow. When this rapidly increasing current is detected by the circuit breaker control circuit Q_1, Q is turned off. This makes the fault current flowing from the rectifier to the transmission line fault point commutate to the snubber capacitors C_{snub} and charge them until the total voltage across the series-connected capacitors is equal to rectifier's terminal voltage V_1 assuming ideal components. By KVL, the voltage at the cathode of the freewheeling diode device D then becomes zero and the fault current commutates to the now-conducting diodes. Finally, the varistor arrests the increasing fault current and brings it to zero by applying a negative voltage across the inductor.

2.3.2 Breaker B Opening

During normal operation, the load current flows through the reverse-conducting diodes of breaker B as current (and power) flows from breaker A to B. When a fault occurs on the transmission line, an increasing current flows from breaker A to the fault point and there is a quick reduction in the current flowing to breaker B and the inverter behind it that is detected by breaker B's control circuit. Thus, breaker B's IGBTs are opened to prevent power flow from the AC system on the other side of the inverter to the DC transmission line fault and the load current from breaker A to B eventually goes to zero due to the current flow into the line fault. At zero forward current, the snubber capacitors start charging due to the constant voltage at the inverter and a reverse current starts to flow from the inverter to the transmission line fault making the converter now acting as a rectifier. When the capacitors get charged to V_2, the freewheeling diode D comes on and the varistor applies a negative voltage across breaker B's inductor to bring the reverse current to zero over time.

2.3.3 Breaker Reclosing and Insulation Recovery

Upon total decay of fault current, current flow into fault point is kept minimal by choosing very large resistors Rsnub for Q device. In order to recover transmission line insulation, its voltage is reduced to a very low value by turning on switch S_D. This forces the voltage at the line to a maximum of V_{clamp} for fault current flow and creates a grounding path for the current flow through R_{snub}. After fault is cleared and sufficient time to recover insulation has passed, S_D is turned off. The minimal forward current through the resistors R_{snub} starts flowing from breaker A

to breaker B and also through the parallel balancing resistors R_D. As $R_D >> R_{snub}$, from voltage division, the voltage across diode device D is approximately V_1 with transmission live voltage at zero, and circuit breaker A can reclose its IGBTs at approximately zero voltage for minimal switching power loss. Note that if S_D is opened prior to fault being cleared, all of the minimal current through R_{snub} flows into the fault point and the voltage across D stays at zero. This feature can be used as a safety check for cleared faults prior to breaker reclosing.

3 DESIGN REQUIREMENTS AND PROTOTYPE

In order to verify the functionality of the solid-state DC breaker topology and compare the performances of the Si and SiC versions, a DC breaker prototype was designed for a 35V, 12A source with calculations shown below. The calculations are modeled after the high voltage example detailed in Sano and Takasaki's work [11].

3.1 High Voltage Design Example [11]

To protect a 300MVA HVDC power system with 250kV rated voltage, 4.5kV Si integrated gate-commutated thyristors (IGCT) are connected in series for the DC breaker design described previously to attain the required blocking voltage. In order to maintain a 100 failure-in-time (FIT) rating, i.e. one failure every 10^7 hours, the 4.5kV ABB IGCTs used in the design are intended to each handle 2.8kV while in operation. As the HVDC system is rated 250kV, 90 Si-IGCTs (n=90) are needed in series to form a single Q device.

$$\frac{250kV\ total\ required\ blocking\ voltage}{2.8kV\ IGCT\ blocking\ voltage} = 90\ IGCTs$$

$$\frac{300MVA}{250kV} = 1.2KA\ current\ rating\ per\ IGCT$$

With a forward/on-state voltage of 1.24V, the conduction power loss due to the IGCTs then becomes

$$P_{loss} = Voltage \times Current = 1.2kA \times 1.24V \times 90 = 133.92kW\ per\ breaker$$

Although the numerical amount of real power loss is high, it is significantly lower than the rated power of the system (approximately < 0.1%). If hundreds of the proposed DC breaker were implemented in the system as part of its protection circuitry, the conduction power loss could appreciably reduce the overall efficiency of the power system. When faults occur in a VSC DC system, V_1 is applied to the inductor coil, fault currents rise exponentially very quickly and to limit the rate of current rise to 10kA/ms, the inductor in the breaker is calculated as 25mH as shown below.

$$V_L = L_1 \times \frac{\Delta I}{\Delta t}$$

$$L_1 = V_L \div \frac{\Delta I}{\Delta t} = \frac{250kV}{10kA/ms} = 25mH$$

Note that for a lower inductor value and fixed V_L, $\frac{\Delta I}{\Delta t}$ increases. That is, the increase in current is quicker. To reduce the current's rate of ascent, we can use higher inductor values. Suppose it takes 39μs to detect the fault and 11μs for all IGCTs in the Q-device to turn-off, for a total delay 50μs. Then the current increase for the 50μs delay is

$$\Delta I_{delay} = \frac{V_L \times t_{delay}}{L_1} = \frac{250kV \times 50\mu s}{25mH} = 0.5kA$$

If the breaker pickup current is set at 150% of rated current (1.8kA), when the breaker actually opens, the current would be 1.8kA + 0.5kA (due to delay) = 2.3kA. For the ABB IGCTs used in this design example, variations in delay time of 0.3μs have been reported. Therefore for this application, the variation in turn-

off time was taken as 0.5μs. Upon opening of all 90 IGCTs, for the fault current to commutate to the the diode device, each of the 90 snubber capacitors for the Q device has to be charged to V_C = 2.8kV. As a result, the charging time of the snubber capacitors was set to ten times the turn-off variation (t_{charge} = 5μs) to reduce the effect of the varying turn-off on proper device operation.

$$C_{snub} \times V_C = Q_{charge} = I \times t_{charge}$$

$$C_{snub} = \frac{I \times t_{charge}}{V_C} = \frac{2.3kA \times 5\mu s}{2.8kV} = 4.1\mu F$$

From Chapter 2, the voltage across the Q device is V_{clamp} + V_1. In order to keep the blocking voltage requirement of the Q device as low as possible while still providing considerable reverse voltage to the inductor during fault current decay, V_{clamp} was set as 10% of V_1 = 25kV. Then Q device is expected to block 275kV in total during breaker operation which is well within IGCTs' capacity of 4.5kV*90 = 405kV. From Equation 2.6, the time for varistor to turn off fault current after commutating to freewheeling diode is calculated as follows.

$$t_f = \frac{L_1 \times I}{(\mathrm{V_{clamp}})} = \frac{25mH \times 2.3kA}{25kV} = 2.3ms.$$

Note $t_f >> t_{delay} > t_{charge}$. In order to obtain the energy absorbed by the varistor, use Equation 2.7.

$$E_V = \frac{I^2 \times L_1}{2} = \frac{25mH \times (2.3kA)^2}{2} = 66.125kJ$$

Unfortunately, this assumes there is zero inductance between the breaker and the fault location. For a more realistic scenario of a line to ground fault 100 miles from the DC breaker assuming DC transmission line with an inductance of 2.016mH/mile, total inductance from fault point to DC breaker(and return path) becomes L_{total} is:

$$L_{total} = L_1 + 2((2.016) \times 100) = 25mH + 403.2mH \cong 428.2mH$$

Then, the time to turn off the fault current which is approximately the time for relay to open becomes

$$t_{fnew} = \frac{L_{total} \times I}{(\mathrm{V_{clamp}})} = \frac{428.2mH \times 2.3kA}{25kV} = 39.39\ ms$$

Although the DC solid-state breaker opening time is similar to an electromechanical breaker's response time for a fault this far away, the fault current is still arrested very quickly within 50μs of fault occurrence, and does not go beyond 50% of rated current as shown above. Therefore, care must be taken to have the DC breakers staged at appropriate distances based on power system protection requirements. The energy absorbed in the varistor then becomes

$$E_{Vnew} = \frac{I^2 \times L_{total}}{2} = \frac{428.2mH \times (2.3kA)^2}{2} = 1.133MJ$$

The much larger required energy rating of the varistor relative to the original value of 66kJ, shows that the varistor must be sized for the fault furthest from the DC breaker.

3.2 Prototype Specifications

A 420VA (35V, 12A) system was designed to test the proposed DC breaker topology with a single breaker connected between a DC source and a resistive load. A knife switch S_{SLG} was connected between the DC coupling capacitors and the resistive load to help simulate possible line-ground faults. Two 1200V MOSFETs were used to implement the Q device with a 5V zener diode acting as a varistor.

When a fault occurs at t=0, V_1 is applied to the inductor coil, fault currents rise exponentially very quickly and to limit the rate of current rise to 175A/ms, the value of the breaker inductance was calculated as 200uH.

$$V_L = L_1 \times \frac{\Delta I}{\Delta t}$$

$$L_1 = V_L \div \frac{\Delta I}{\Delta t} = \frac{35V}{175A/ms} = 200uH$$

For an expected total delay 50μs when it takes 39μs to detect the fault and 11μs for IGBTs to turn-off [11], the current increase during the 50μs delay is given by

$$\Delta I_{delay} = \frac{V_L \times t_{delay}}{L_1} = \frac{35V \times 50\mu s}{200uH} = 8.75A$$

If the breaker pickup current is set at 125% of rated current at 10A, when the breaker actually opens, the current would be 10A + 8.75A (due to delay) = 18.75A. This means the breaker components should be able to handle ~18A. Variation in turn-off time was again taken as 0.5μs and the charging time of the

snubber capacitors set to four times the turn-off variation (t_{charge} = 2μs) to reduce the effect of the varying turn-off on proper device operation.

$$C_{snub} \times V_C = Q_{charge} = I \times t_{charge}$$

$$C_{snub} = \frac{I \times t_{charge}}{V_C} = \frac{18A \times 2\mu s}{35V} = 1.03\mu F$$

Here, the voltage across the Q device is V_{clamp} + V_1 and V_{clamp} was set as 14% of V_1, ~5V with the relatively low voltage of the prototype setup, V_{clamp} + V_1 is much smaller than the available IGBTs' rated blocking voltages. The Q device is expected to block 40V in total during breaker operation which is well within IGBTs' capacity of 1200V. From Equation 2.6, the time for varistor to turn off fault current after current is commutated to freewheeling diode is calculated as follows.

$$t_f = \frac{L_1 \times I}{(\mathrm{V_{clamp}})} = \frac{200uH \times 18A}{35V} = 0.103ms.$$

$$E_V = \frac{I^2 \times L_1}{2} = \frac{200uH \times (18A)^2}{2} = 28.512mJ$$

Note we are assuming there exists negligible inductance in DC line connections within test setup as opposed to the previous high-voltage example.

4 SIMULATION

4.1 Original Topology

With the expected behavior described in the Chapter 2 as a baseline, the following circuit setup for a DC source powering a resistive load was simulated in Orcad Capture/PSPICE to test the DC breaker's response and characteristics. In Figure 4-1, two Q devices (Sigbt1, Sigbt2) and two D devices (Dfwheel1, Dfwheel2) are used in series to provide the needed blocking voltage for the breaker. i.e. n=2=m. Just like Sano's prototype [11], simulation invloves a 360V source and lower power absorption requirements, a zener diode rated at 9.1 V is used instead of the varistor. A zener diode is a semiconductor designed to have specific breakdown voltages at which even when very large amounts of reverse current, the zener voltage stays constant. A zener diode in its breakdown region has a constant negative voltage, $-V_Z$ as current flows from its cathode to its anode. The semiconductor is carefully doped during fabrication to breakdown at a given voltage. As the circuit requires an energy-absorption device to provide a constant negative voltage regardless of amount of fault current across its inductor during a fault, a low-voltage zener diode was used to replace the varistor [11].

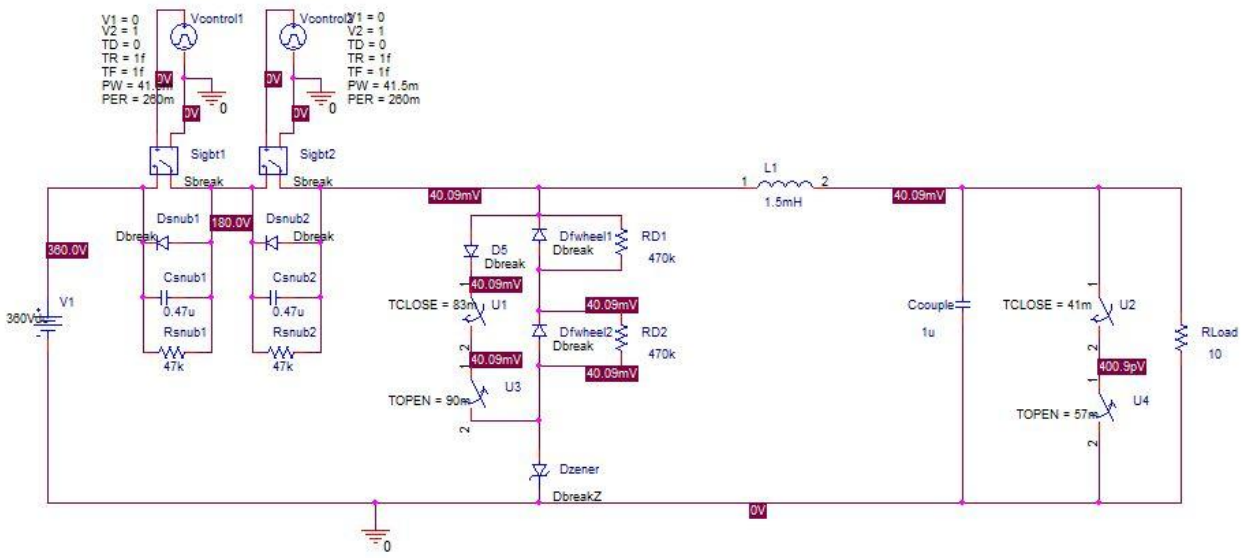

Figure 4-1. Original Freewheeling Diode DC Breaker Schematic - High Load

The circuit of Figure 4-1 is designed to simulate a line to ground fault at 41ms, with the Q devices detecting the fault and opening the IGBTs at 41.5 ms. The fault is then cleared at 57 ms and the electromechanical switch S_D is closed at 83 ms to begin the line reionization process. The IGBTs are reclosed at 260 ms with the results shown in Figure 4-2.

4.1.1 High Load

At high load, almost entire source voltage, V_1 is across switches after de-ionization (VRsnub2 ~ 180V). This is because there is very little resistance at the output compared to the balancing resistors parallel to the IGBTs and from voltage division for a series resistive circuit, most of V_1 is across the larger resistors. Therefore, when the switches are turned back on after fault clearing, it is done with significant switching loss as IGBT modules go from V_1 to 0 in a matter of microseconds. Also, the parallel capacitors across the switches have to discharge

in a hurry and this leads to the negative capacitor current spike (ICsnub2) as shown in Figure 4-3.

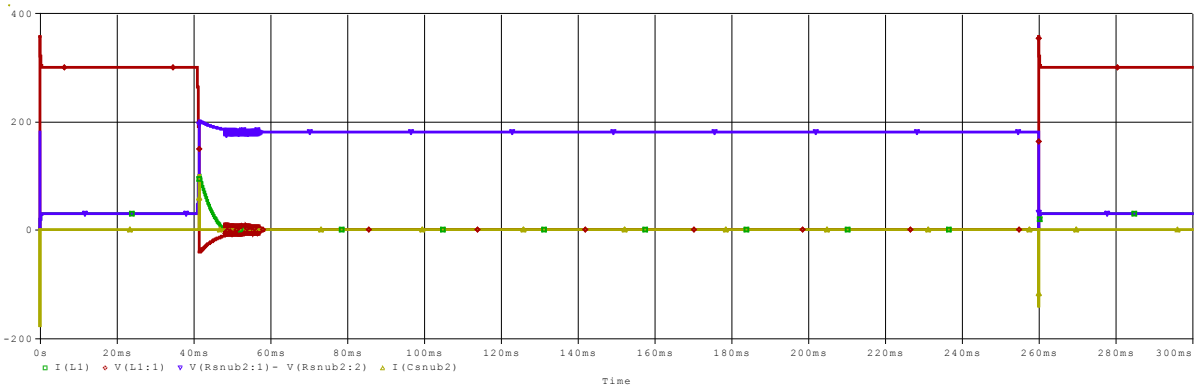

Figure 4-2. Original Topology Simulation Results - High Load

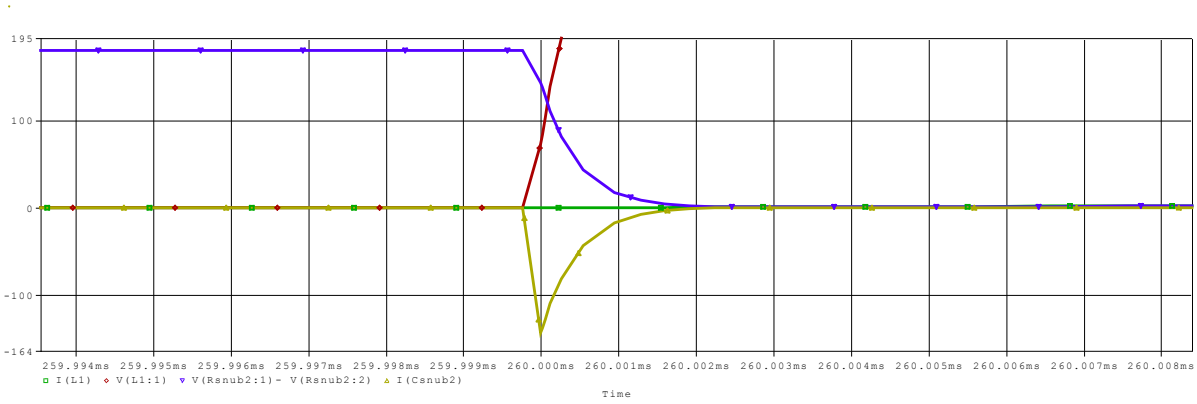

Figure 4-3. Original Topology Capacitor Discharge - High Load

Note that the line voltage (VL1:1) stays at approximately zero the entire time the IGBTs are off and fault current is zero amperes 7 ms after fault with 500us fault detection delay incorporated in the simulation.

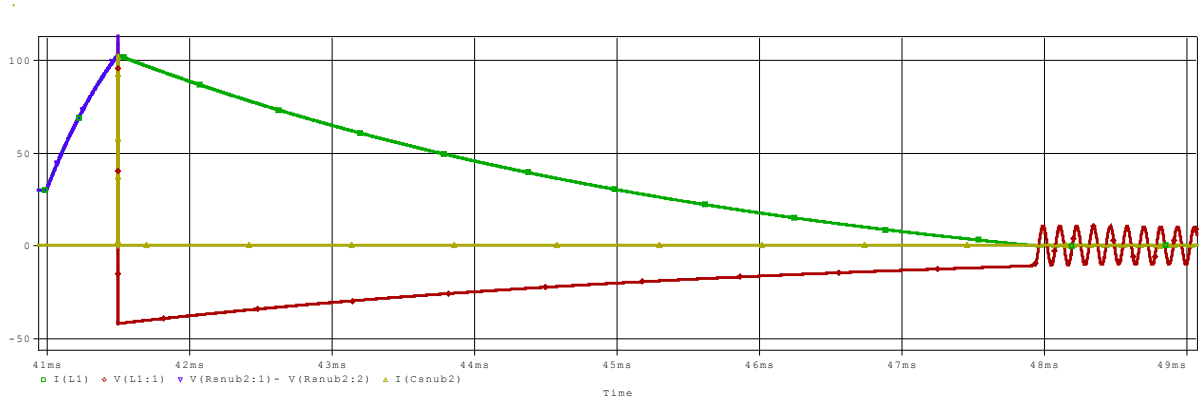

Figure 4-4. Original Topology Current Arrest and Decay - High Load

More importantly, noting there is a 500us detection delay, the fault current surge is arrested just 1us after IGBTs are turned off as capacitors are charged to V_1 and freewheeling diodes start conducting, and fault current commutates to freewheeling diodes as shown in Figure 4-5.

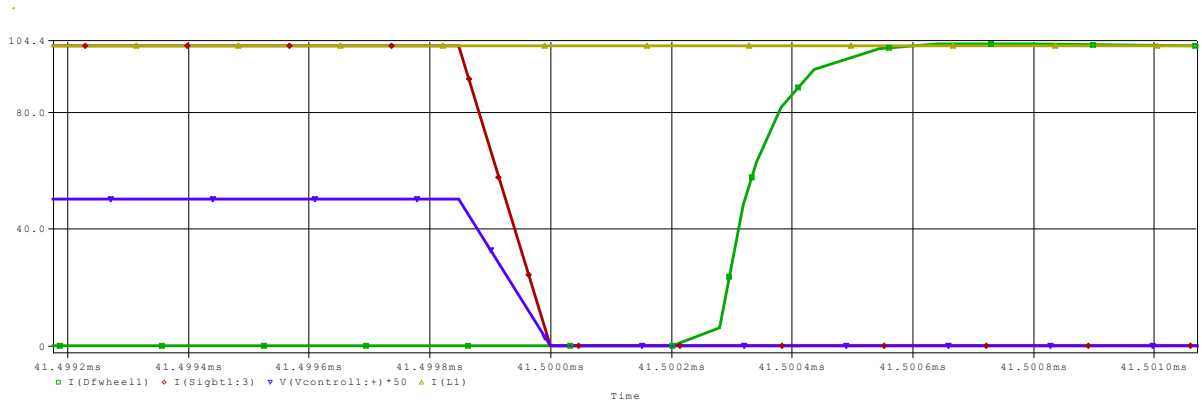

Figure 4-5. Original Topology Arrest Delay - High Load

4.1.2 Low Load

In order to simulate a low-loading situation, a much higher resistor value was set to represent the system load as shown in Figure 4-6.

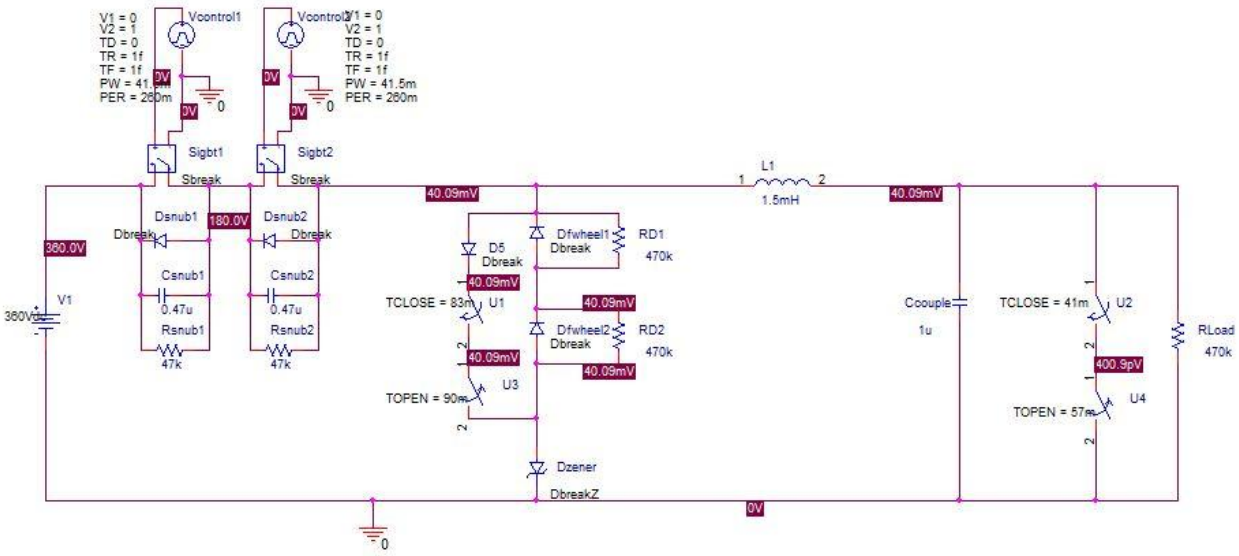

Figure 4-6. Original Freewheeling Diode DC Breaker Schematic - Low Load

At low load, and a higher overall load resistance, whenever the IGBTs and S_D are both off with no short circuit present, the source voltage V_1 is split between the load resistance and the IGBTs' balancing resistors due to voltage division for a series resistive circuit where Rsnub<<Rload. This leads to some transient voltage distribution behavior both after the short circuit fault is removed and after the electromechanical switch, S_D is turned off as shown in Figure 4-7.

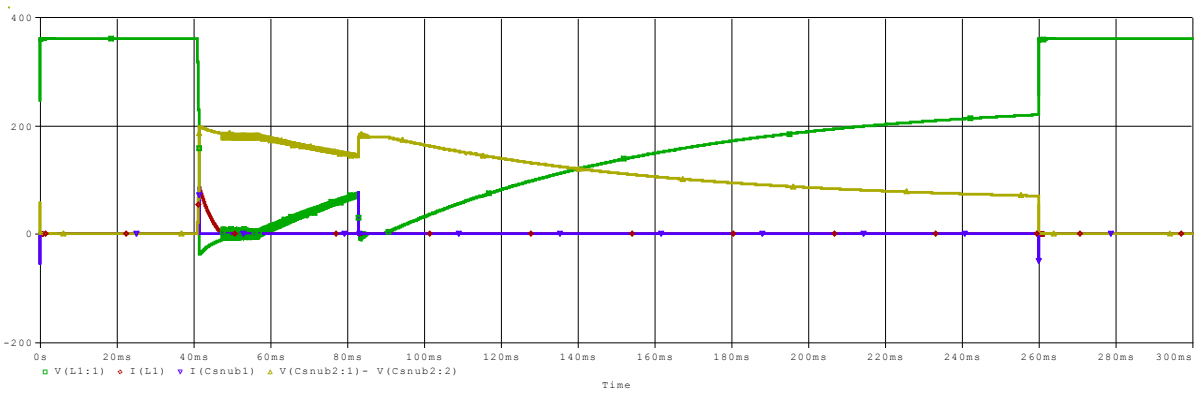

Figure 4-7. Original Topology Overall Simulation Results - Low Load

Inductor current rapidly goes to zero again on IGBT turn-off and breaker opening as expected. Since at low load, the load resistance here is larger than the Q device's balancing resistors, a larger portion of the source voltage V_1 is delivered to the load after SD is switched off making the line voltage much higher than zero. This higher line voltage (VL1:1) means lower voltage across IGBTs which further leads to lower switching power loss during reclosing of IGBTs and lower negative capacitor current with approximately 50A as opposed 150A for high load case. This result is shown in Figure 4-8.

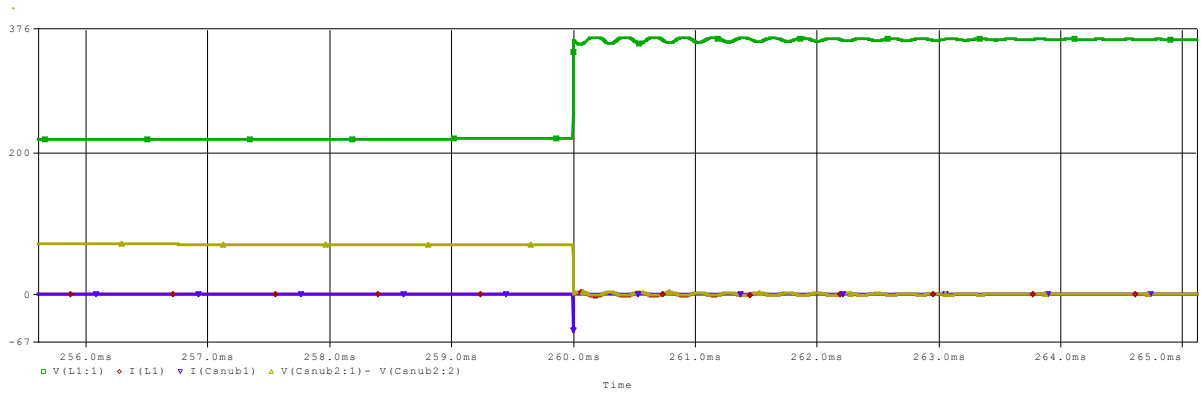

Figure 4-8. Original Topology IGBT Reclosing - Low Load

Unfortunately, this also means that the line voltage almost instantaneously drops to zero from a relatively high voltage when S_D comes on to help de-ionize the line and recover insulation. As such, the Sigbt capacitors have to rapidly increase voltage from a level significantly lower than V_1 to the source voltage, V_1--by KVL around the loop containing S_D switch and DC source. This leads to spiking positive capacitor current of almost 100A. Figure 4-9 illustrates this result.

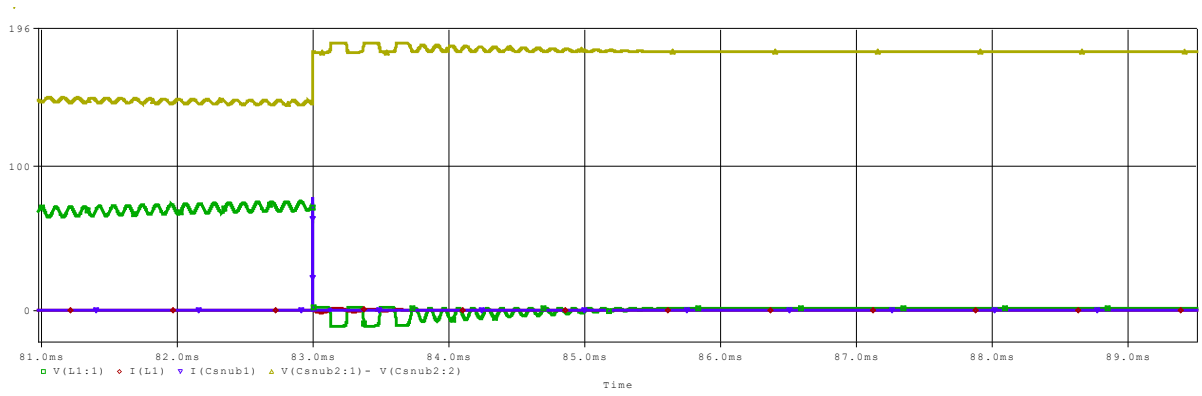

Figure 4-9. Original Topology Capacitor Current Spike- Low Load

4.2 Modified Topology

Further testing identified the lack of isolation in the previous configuration between the load resistance and circuit breaker's balancing resistors as the likely cause of the high voltage drop across the IGBT on turn-on/reclosing. i.e. when the IGBT is off, and Rsnub is much higher than the parallel combination of the load resistance at high load and freewheeling diode's balancing resistors. A simple voltage division leads to high voltage build-up across the IGBT. In order to combat this problem, a second IGBT that turns off after the re-ionization process when S_D goes off and turns on at the same time as the original IGBT was put in series as shown in Figure 4-10. The IGBTs' turn-on times were varied by 0.5us to account for disparities in semi-conductor characteristics/turn-on time [11]. Note that the isolating IGBT Sigbt2 is opened at the same time as S_D is opened with line still at zero voltage.

4.2.1 Sigbt1 Reclosed Faster than Sigbt2 - High Load

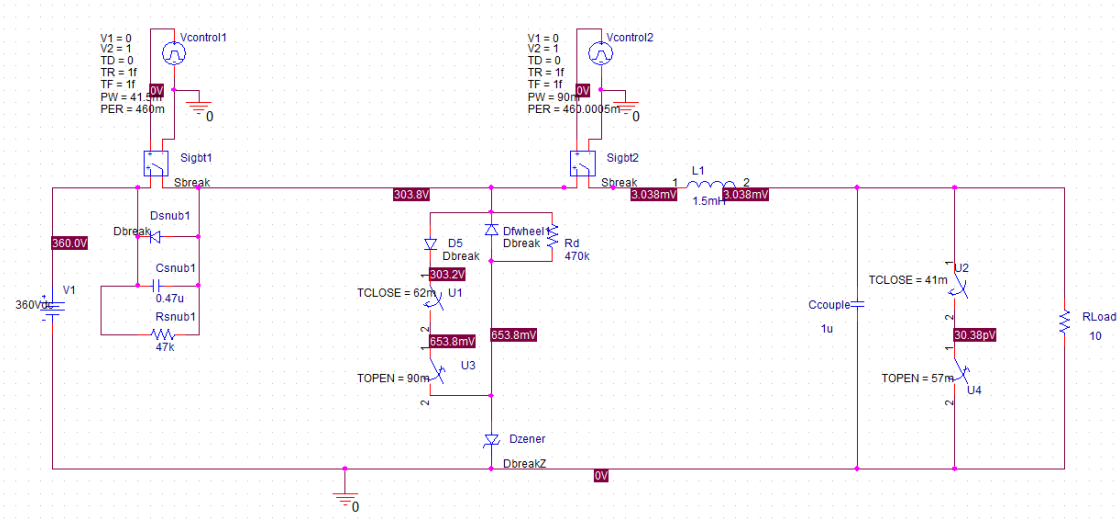

Figure 4-10. Modified Topology DC Breaker Schematic - High Load

In Figure 4-11, the high load simulation results with Sigbt2 slightly slower to turn-on than Sigbt1 are captured. The voltage at pin Rd:2 represents the line voltage--same voltage as VL1 for original topology. It shows how the voltage at the transmission line varies during the different phases of operation of the modified breaker in comparison to the original topology.

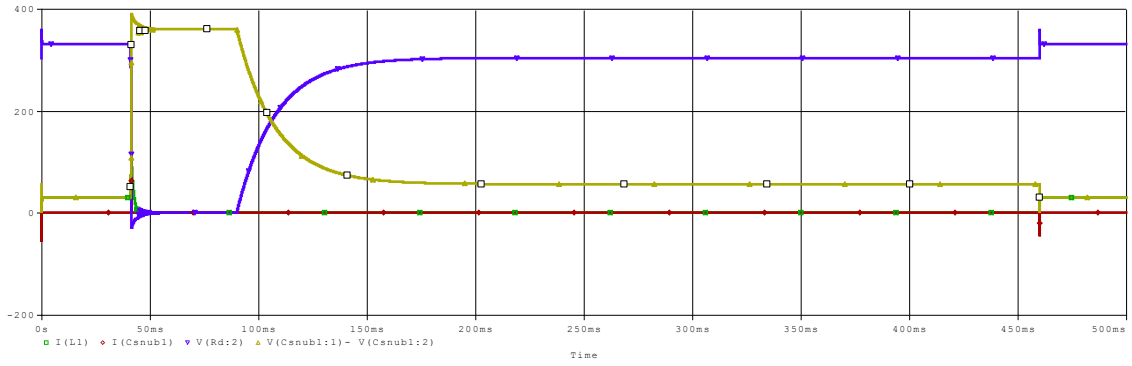

Figure 4-11. Modified Topology Overall Results - High Load and Si1 Faster

4.2.2 Sigbt1 Reclosed Faster than Sigbt2 - Low Load

At low load using 470kΩ load, the following behavior in Figure 4-12 is observed. Note that the problems of excessive positive and negative currents are mitigated with less than 50A in both high and low load cases. Also, S_D has to be turned-on as soon as the fault is cleared to prevent a rise in the line voltage by pulling line to ground with S_D when at high voltage can lead to spikes prior to de-ionization.

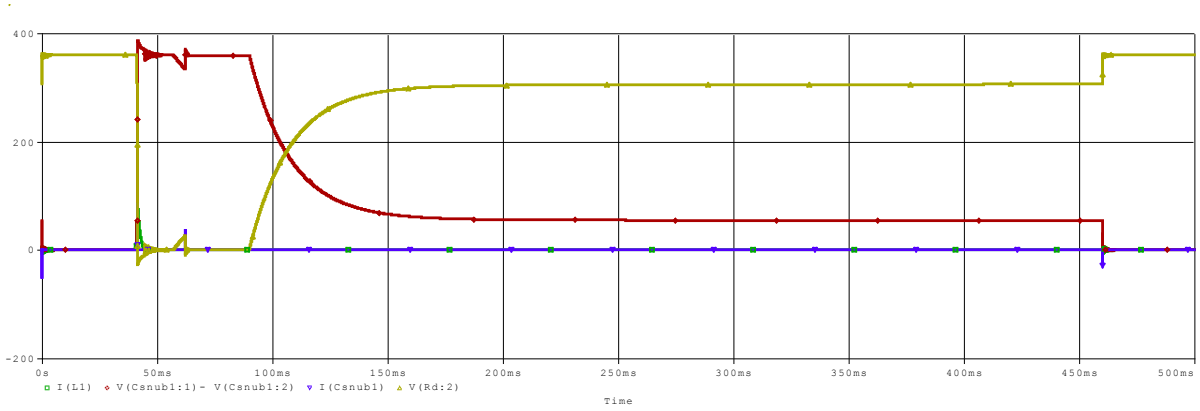

Figure 4-12. Modified Topology Overall Results - Low Load and Si1 Faster

4.2.3 Sigbt2 Reclosed Faster than Sigbt1 - Low and High Load

With IGBT1 slower (0.5us slower than IGBT2) to turn-on there were no differences in the observed waveforms for both high load (Figure 4-13) and low load (Figure 4-14).

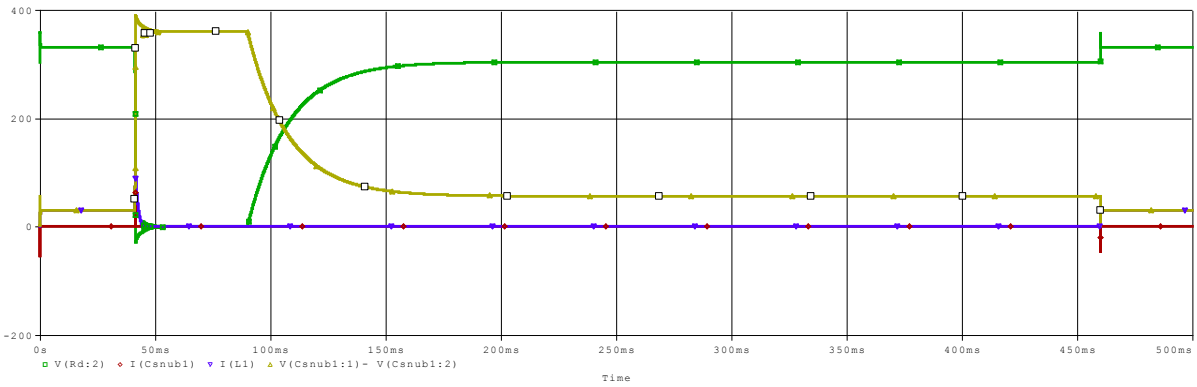

Figure 4-13. Modified Topology Overall Results - High Load and Si2 Faster

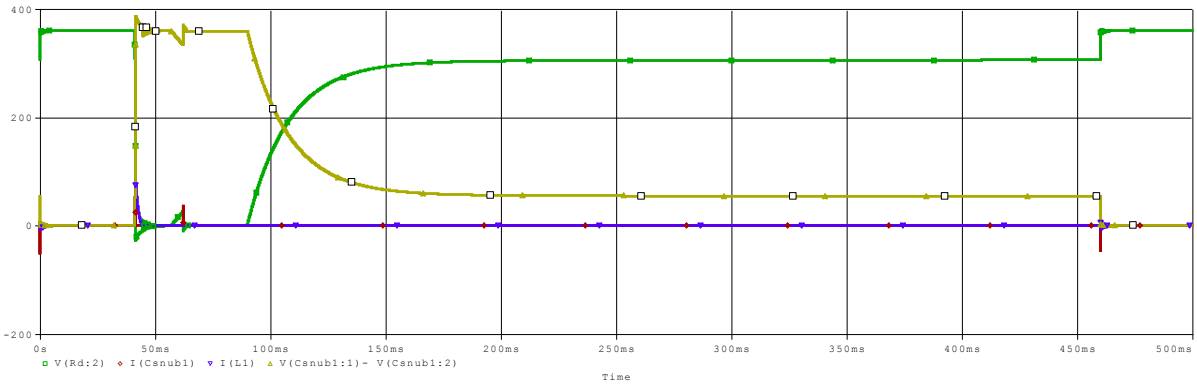

Figure 4-14. Modified Topology Overall Results - Low Load and Si2 Faster

4.3 DC Load Current Interruption (Modified Circuit)

The circuit was also tested for load current shut-off as opposed to fault clearing/circuit protection with Sigbt opening at 41 ms. In this configuration, upon Sigbt turn-off, the load current commutates to the capacitor until it fully charges to V_1 before commutating to the freewheeling diode and decaying due to the zener diode's reverse voltage. Figure 4-15 shows the setup for current interruption with no simulated faults in the system.

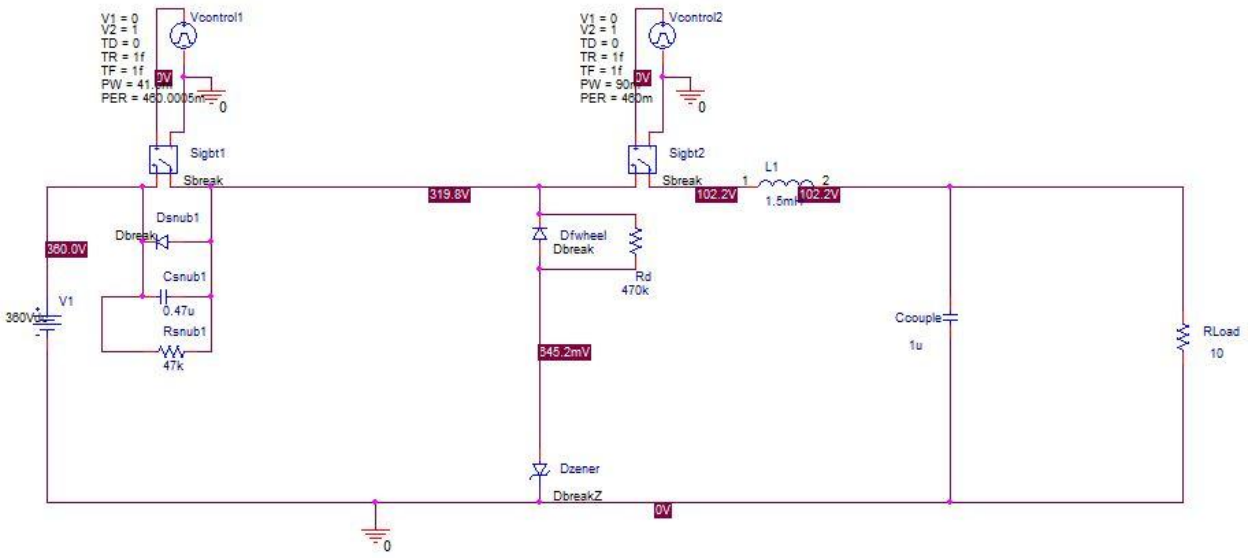

Figure 4-15. Modified Topology DC Load Current Interruption Schematic

4.3.1 High Load

Figure 4-16 shows the load current commutating to the freewheeling diode and then going to zero demonstrating successful load current interruption for a high load. The decay of the ~30A inductor current takes approximately 0.4ms with a similar exponential decay as observed for a fault condition.

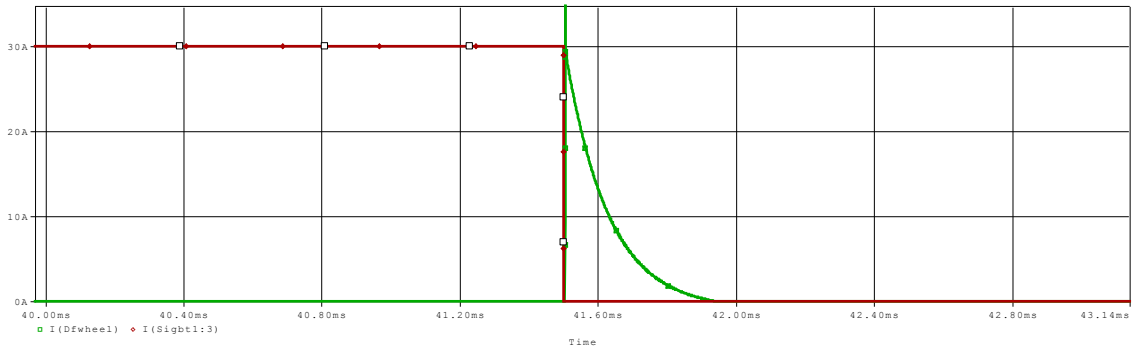

Figure 4-16. DC Load Current Interruption Decay - High Load

4.3.2 Low Load

At low load (470k) with no fault in the circuit, the load current is too small and does not commutate to the freewheeling diode-it instead dies out quickly when Sigbt1's opening disconnects it from its voltage source, V_1. This is depicted in Figure 4-17 where I(Dfwheel) is shown to stay at zero the entire time while I(Sigbt1:3) decays upon load current interruption at 41.5ms.

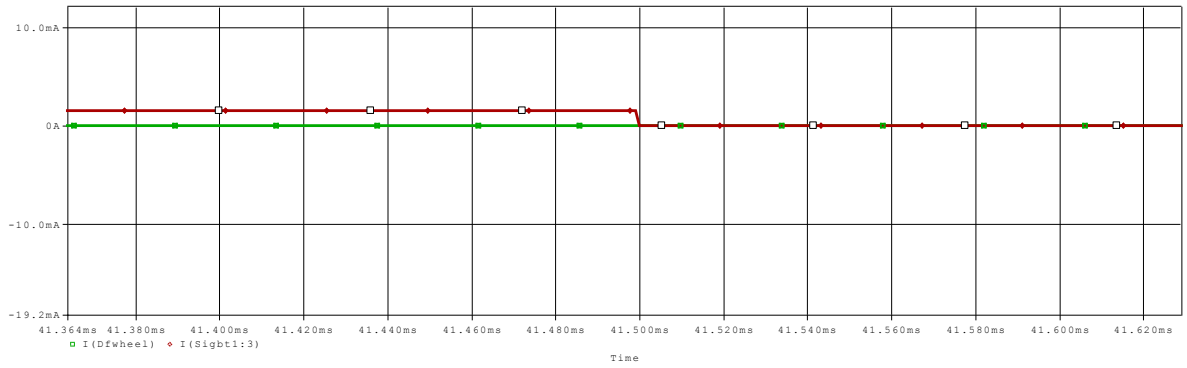

Figure 4-17. DC Load Current Interruption Decay - Low Load

For much lower values of Rload (100Ω), the load current begins to commutate to the diode with some ringing as shown in Figure 4-18. This ringing can be due to much lower resistance being present in the circuit to balance out the large inductor present in the design.

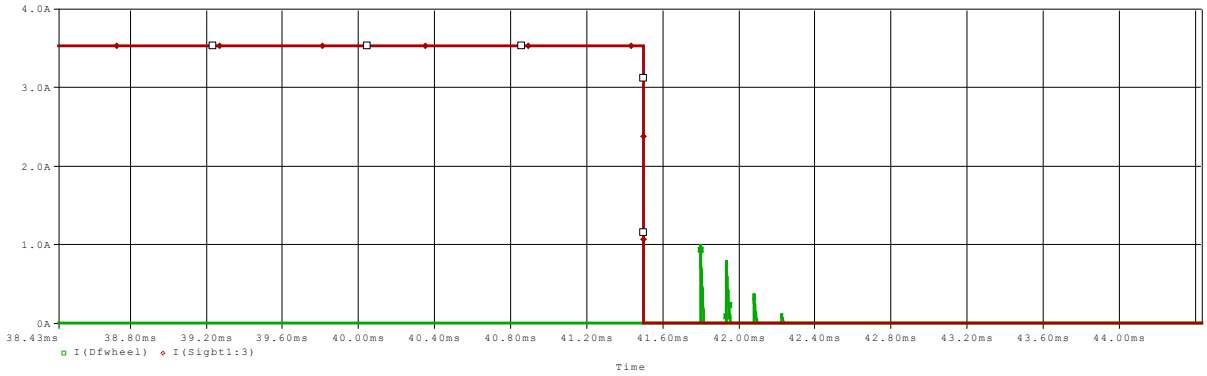

Figure 4-18. DC Load Current Interruption Decay - Ringing

4.4 Prototype Simulation

Based on available laboratory equipment and in order to keep costs low, the DC Breaker prorotype specified in Figure 3-1 was built and tested as a proof-of-concept and the results displayed in Chapter 5. Prior to constructing the protoype, the design was simulated in OrCad Capture/PSPICE in order to gain an insight into expected behavior and potentially preempt any problems in the real-world performance of the breaker.

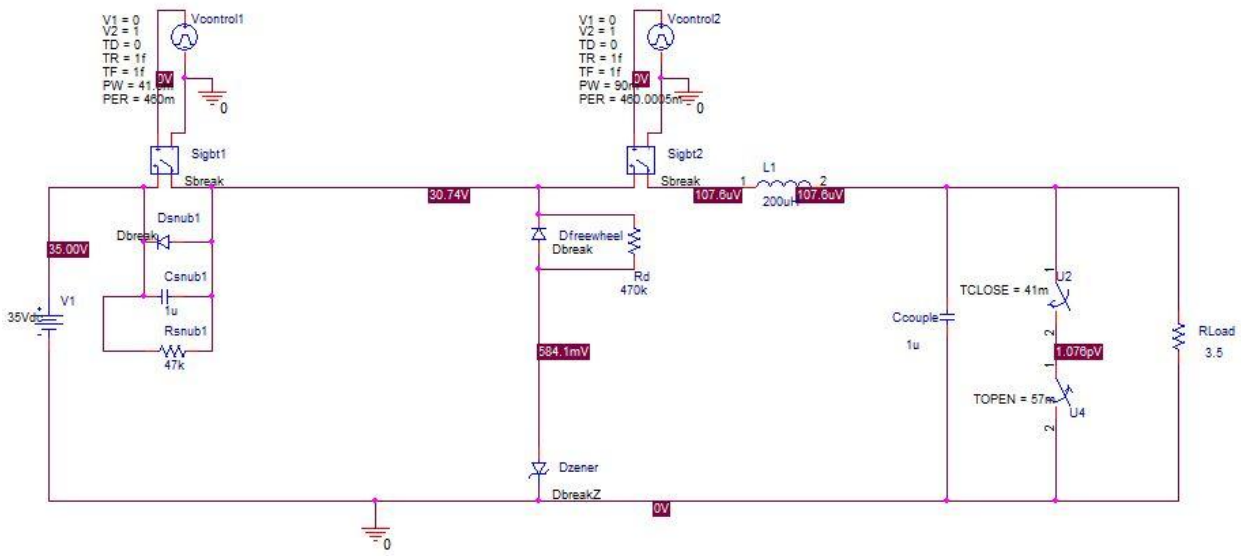

Figure 4-19. Prototype Circuit High Load

4.4.1 High Load

The results are as expected with the current decaying quickly once the negative 5V zener voltage is applied across the inductor. Here Sigbt1 is faster than Sigbt2 by 0.5us.

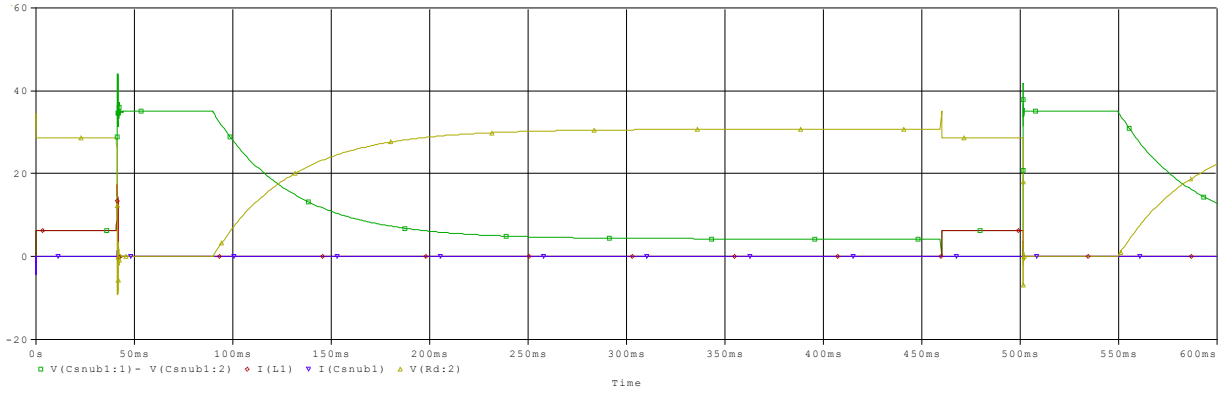

Figure 4-20. Prototype Circuit Overall High Load Results

On reclosing when Sigbt1 comes on 0.5us after Sigbt2, the source voltage is momentarily applied across the snubber capacitor(charging and discharging it

rapidly) and leads to the large positive capacitor voltage spike and negative capacitor current spike shown at 460ms in Figure 4-21 below.

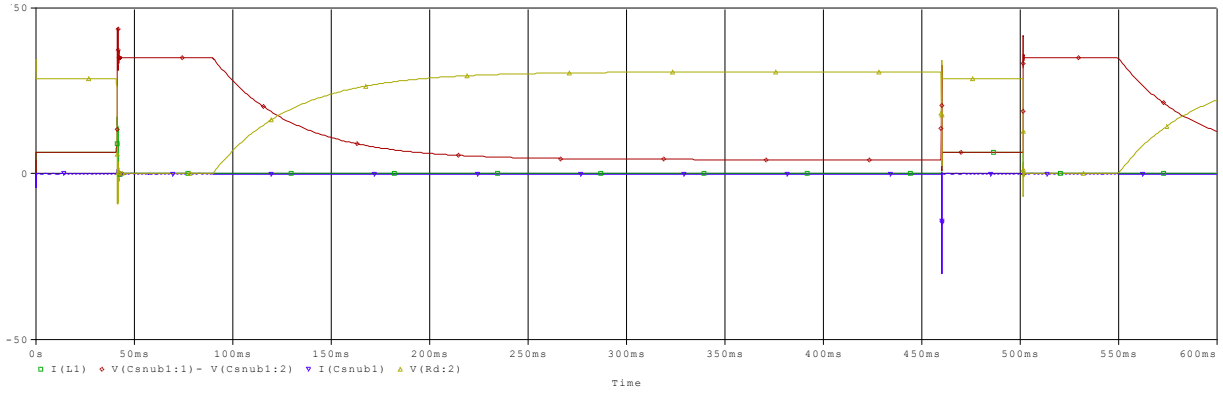

Figure 4-21. High Load Capacitor Current Spike Reclosing – Sigbt2 Faster

4.4.2 Low Load

At low load, similar behavior is observed when Sigbt2 is faster than Sigbt1 on reclosing.

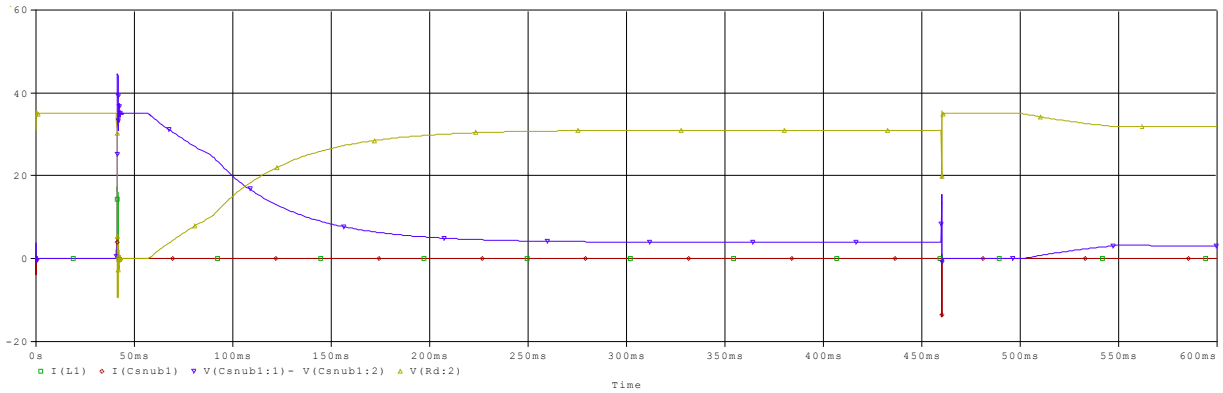

Figure 4-22. Low Load Capacitor Current Spike Reclosing – Sigbt2 Faster

When Sigbt1 is 0.5us faster than Sigbt2, the spikes at 460ms disappear as there is no rapid capacitive voltage buildup or discharge on reclosing.

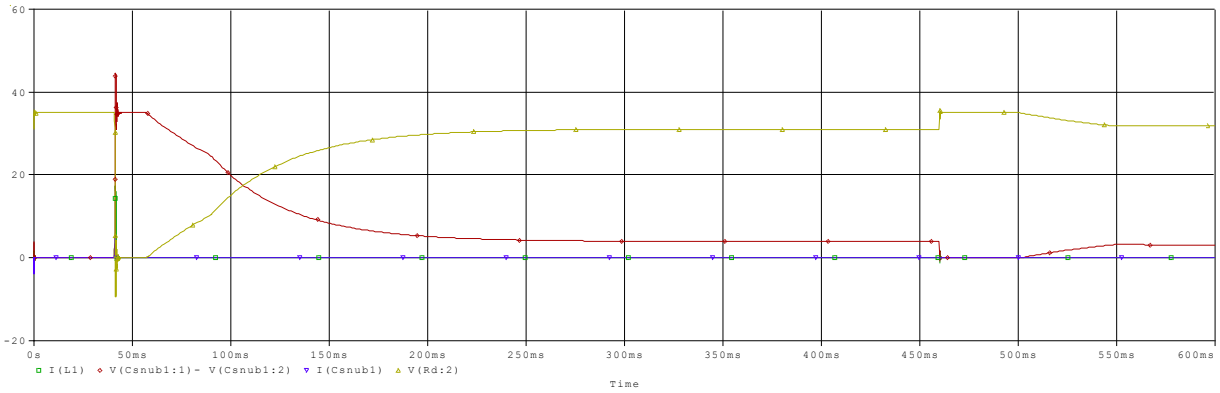

Figure 4-23. Low Load Capacitor Current Spike Reclosing – Sigbt1 Faster

5 HARDWARE AND TEST RESULTS

Based on the simulation results from Chapter 4 and available laboratory equipment in the Electrical Engineering Department at Calpoly, a DC breaker prototype was built with the specifications from Chapter 3.

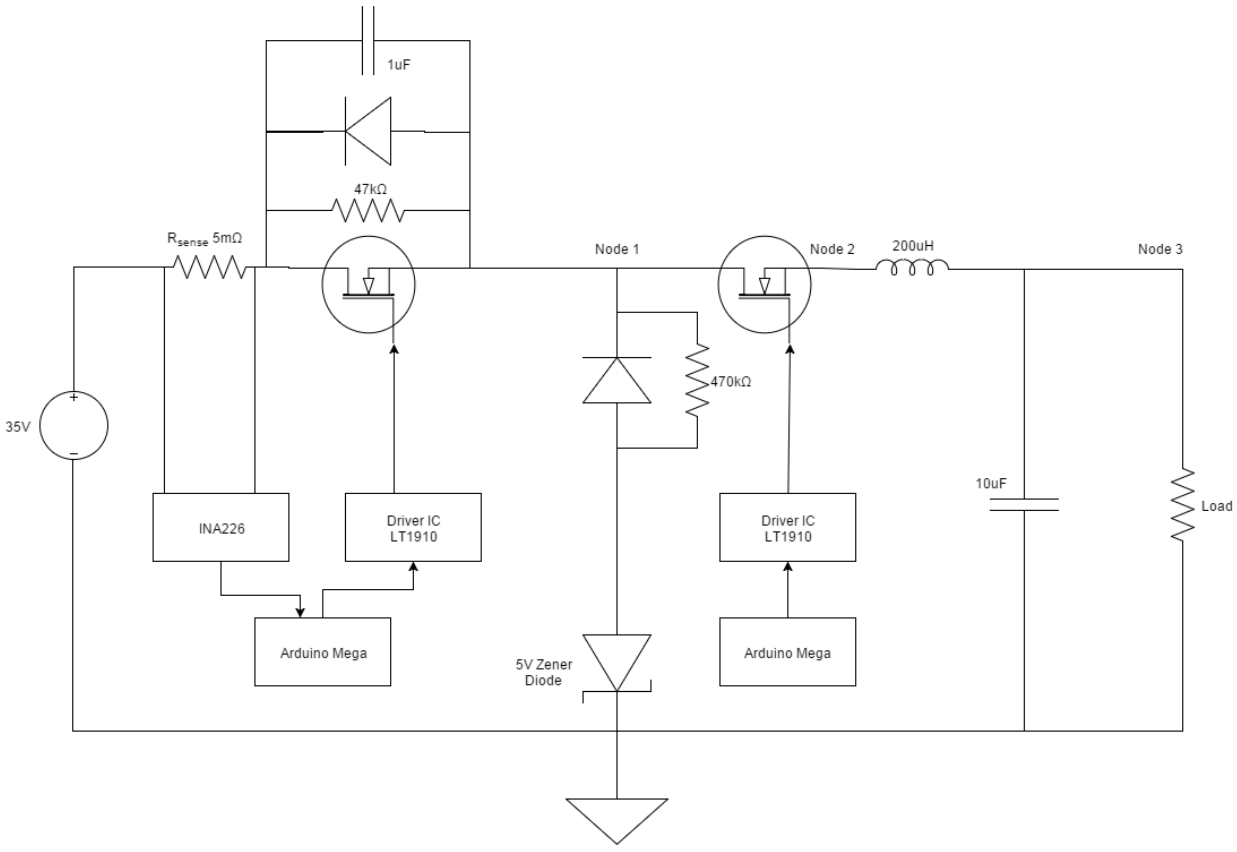

Figure 5-1. Prototype Control and Power Circuit

The prototype module is divided into two main parts:

1. Power circuit
2. Control circuit

5.1 Power Circuit

This includes the IGBTs/FETs, inductors, capacitors and diodes used in the design. The circuit of Figure 3-1 shows the voltage source in series with the modified Q device, inductor and an electronic load. DC coupling capacitors are also included to provide an insight into what happens in a real-world circuit when a line fault occurs between the load and the source.

International Rectifier's G4PH30KD IGBT was selected as the Silicon switching device due to an IGBT's intrinsic low power dissipation properties. Its 1200V/20A voltage and current rating at 25degC make it a good fit for implementing the 35V/15A DC breaker prototype.

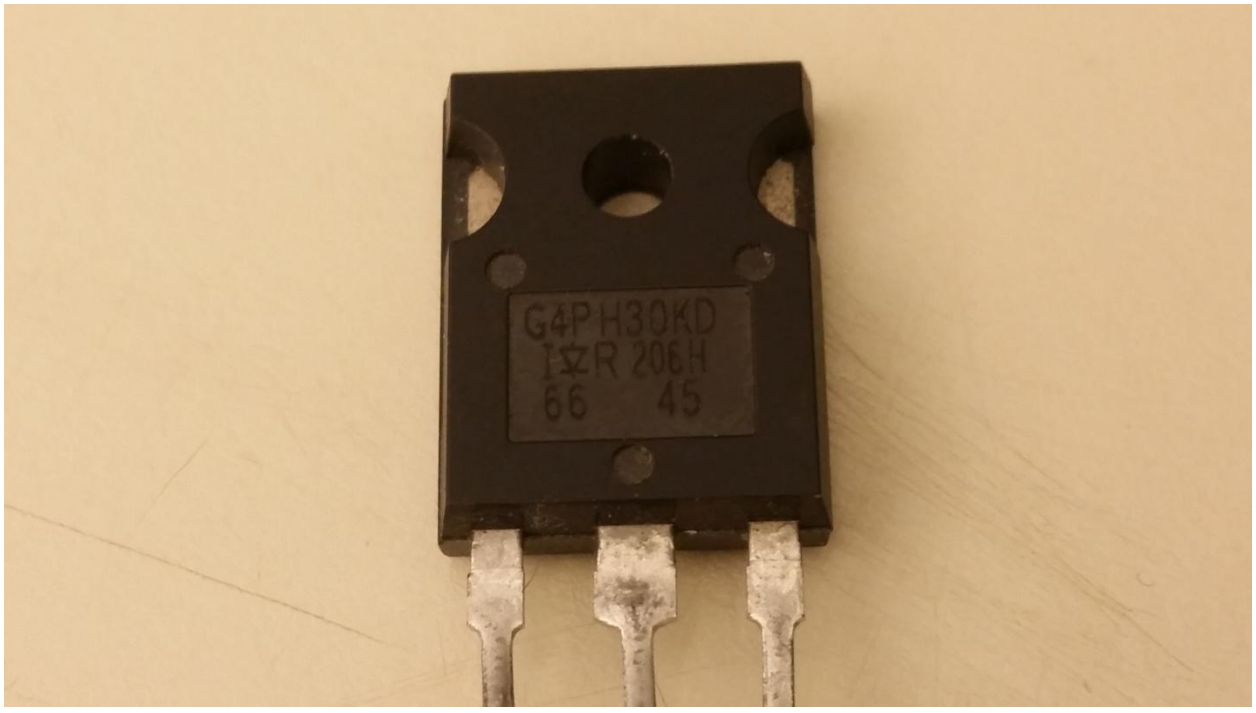

Figure 5-2. IRF G4PH30KD Si IGBT

In order to slow down the rise of the fault current whenever a line fault occurs, two toroidal core 100uH inductors rated 17A each are connected in series to provide a total of 200uH of inductance as calculated in Chapter 3.

Figure 5-3. Two 100uH Toroidal Inductors

On semiconductor's B60H100G 100V/60A Schottky Barrier Rectifier diodes were used in the RCD snubber and freewheeling diode portions of the prototype circuit.

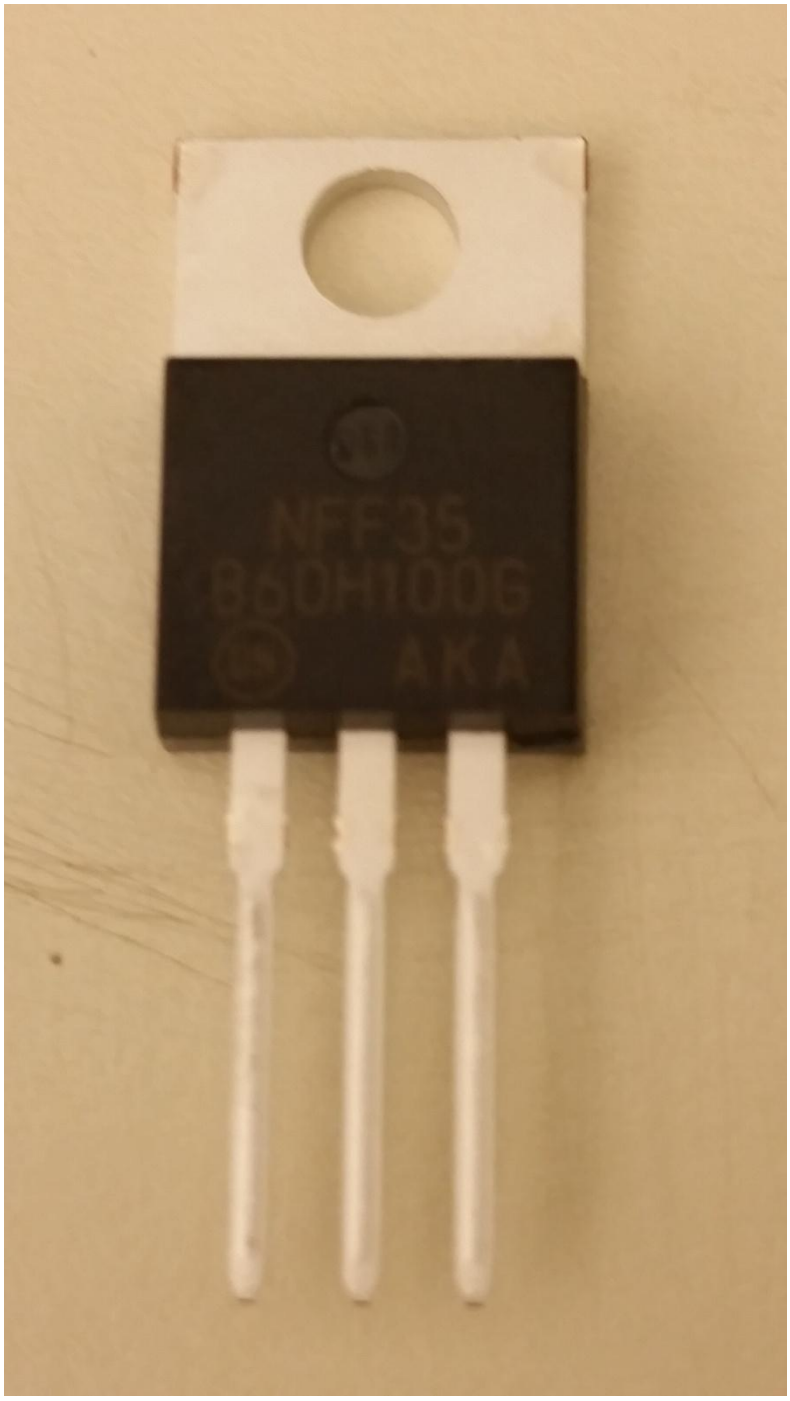

Figure 5-4. ON B60H100G Schottky Barrier Rectifier Diode

Finally, CREE's C2M0040120D Silicon Carbide(SiC) FET was used as the replacement wideband gap device to generate comparison data for DC breaker

prototype performance. Similarly rated at 1200V but with a higher 60A current rating, CREE's SiC FET is comparable in ratings to the Si IGBT used to generate the initial performance data.

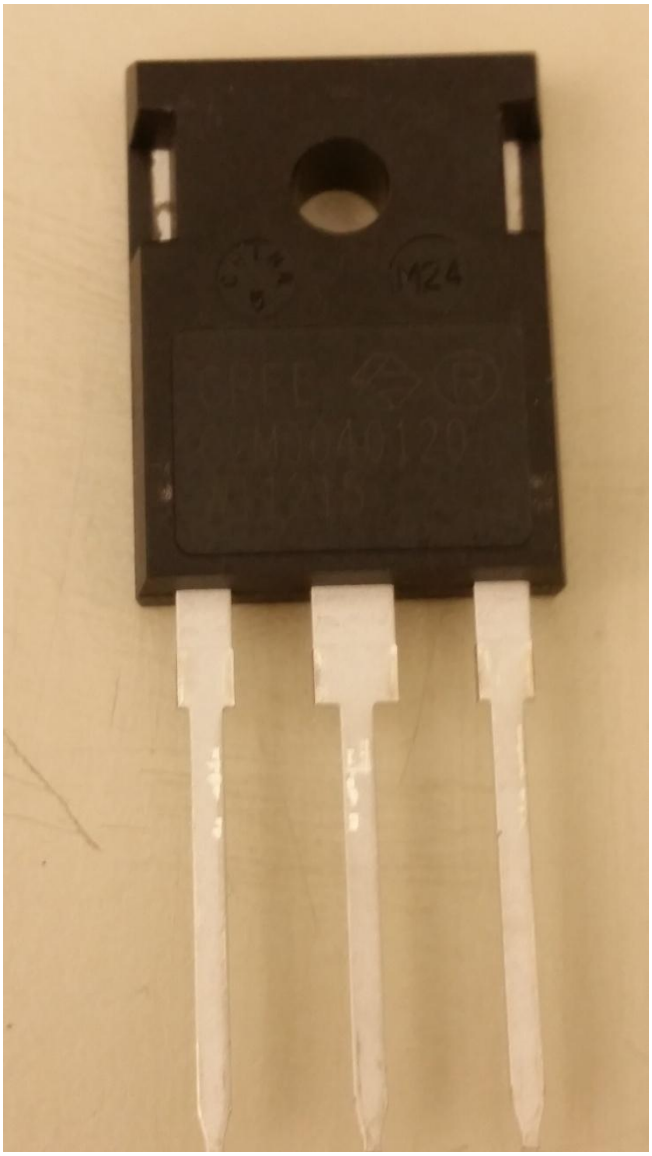

Figure 5-5. CREE's SiC MOSFET C2M0040120D

5.2 Control Circuit

For the breaker to know exactly when to trip, it needs to know when the current running through it exceeds a set threshold. In order to monitor the current passing through the breaker, Texas Instrument's INA226 current shunt monitor was used to acquire the current measurements. The INA226 consists of an integrated differential amplifier in series with an Analog-to-Digital converter(ADC) connected to an Inter-Integrated Circuit (I^2C) serial interface for digital current, voltage or power readings. The IC reads the current by measuring the voltage drop across a 5mΩ sensing resistor R_{sense} and storing the value in an internal register. The INA226 comes in a 10-pin VSSOP package made for surface-mount applications and had to be attached to a DIP adapter to enable soldering to DC breaker prototype board.

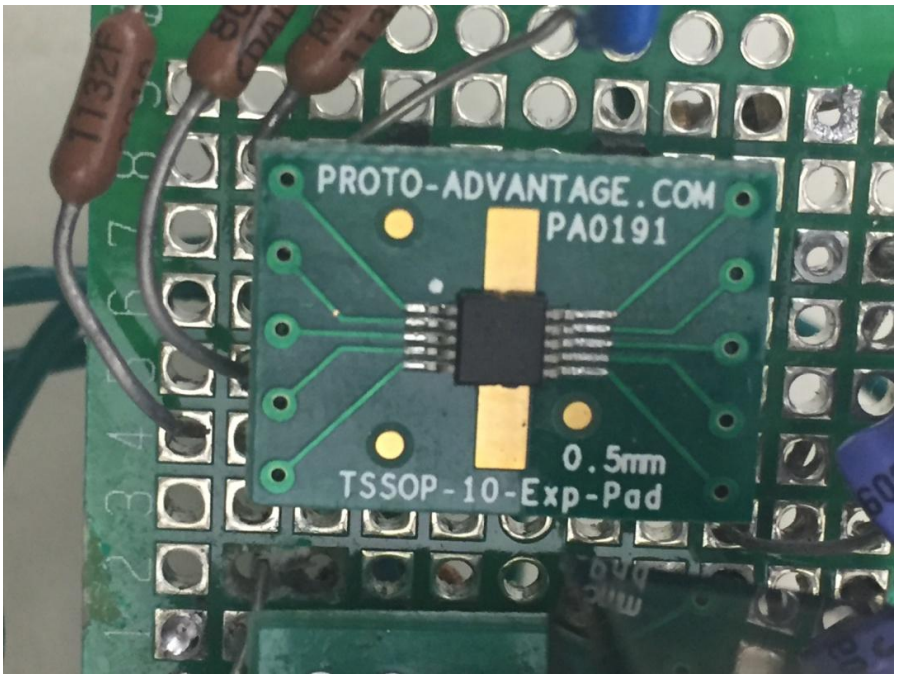

Figure 5-6. INA226 on 10-pin DIP adapter board

The digitized current reading is then sent to an Arduino Mega microcontroller where the voltage value is converted to its equivalent value in Amperes and a decision is made whether or not to open the FET based on the set current threshold. Furthermore, the digital readings can be remotely communicated or the breaker remotely controlled via the internet.

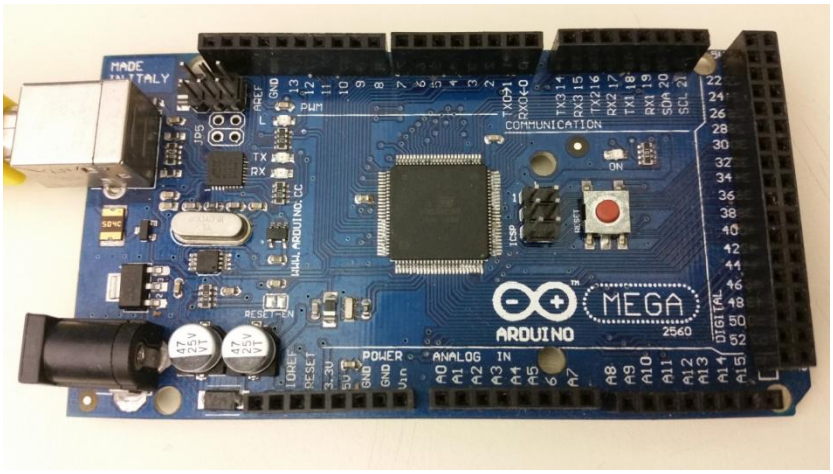

Figure 5-7. Arduino Mega

5.2.1 Configuring the INA226 and Arduino Mega

Texas Instrument's INA226 uses the I^2C protocol to communicate with the Arduino Mega in this setup. I^2C is a serial communication protocol with a serial data line (SDA) and a serial clock line (SCL). On the Arduino Mega, Pin 20 is setup as the SDA pin while Pin 21 is the SCL pin.

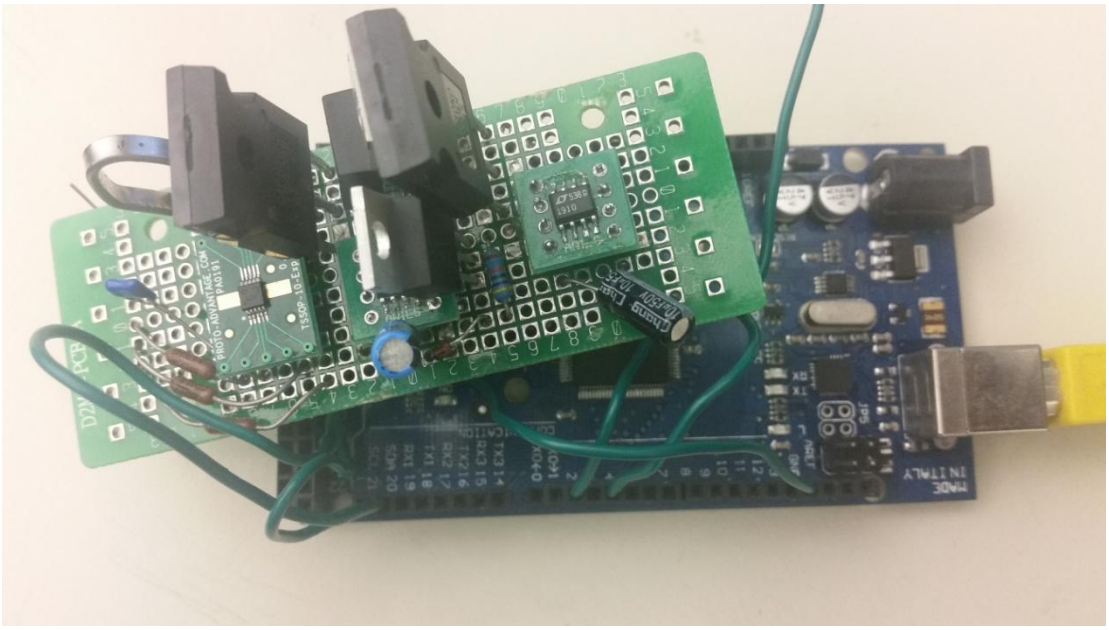

Figure 5-8. Breaker Coupled to Arduino Mega for I2C and Trigger

The Arduino Mega using the Wire library is setup as the master device while the INA226 is the slave device in this setup. In order to initiate I^2C communications, the I^2C master pulls the SDA line from high to low while holding the SCL line high as shown in Figure 3-2. The master then sends the 8-bit word specifying the slave address (first 7-bits) the communcation is intended for and whether a read (high) or write (low) operation is required (eighth bit). As multiple slaves can be connected to the same master, this ensures the right slave device receives the appropriate commands and sends a receipt acknowledgement. The INA226 address is configured as 0100100_2 (A1=VS, A0=GND) which translates to 68_{10}.

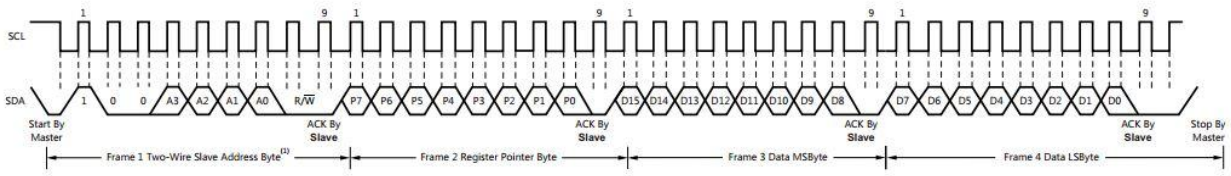

Figure 5-9. Configuring the INA226 [12]

Prior to acquiring current readings from the INA226, the IC needs to be configured for the right type of readings and the number of samples averaged per reading. Based on the need for low latency, the configuration register is programmed as x4005 and sent to the INA226 from the Arduino during setup as shown in Figure 3-3. Note the configuration setting is sent a byte at a time and to stop I^2C communication, the Arduino master pulls up SDA from low-to-high while holding SCL high.

```
#include <Wire.h>

void setup() {
  // put your setup code here, to run once:
  pinMode(2, OUTPUT);
  pinMode(4, OUTPUT);
  Wire.begin();
  Serial.begin(9600);          //open serial comms

  Wire.beginTransmission(68);   //open I2C comms with INA219
  Wire.write(byte(0x00));      //sets pointer to configuration register
  Wire.write(byte(0x40));      //sending MSByte for config register
  Wire.write(byte(0x05));      //sending LSByte for config register

  Wire.endTransmission();      //stop I2C comms might be able to do without

  Wire.beginTransmission(68);
  Wire.write(byte(0x01));      //sets pointer to current shunt voltage register
  Wire.endTransmission();      //stop I2C comms

  digitalWrite(2, HIGH);
  digitalWrite(4, HIGH);
}
```

Figure 5-10. Programming the Arduino as an I2C Master

The signals from the SDA and SCL lines from the INA226 were captured on the Teledyne Lecroy HDO4104 1GHz High Definition oscilloscope (Figure 5-11) during configuration with the results displayed in Figure 5-12.

Figure 5-11. Teledyne Lecroy HDO4104

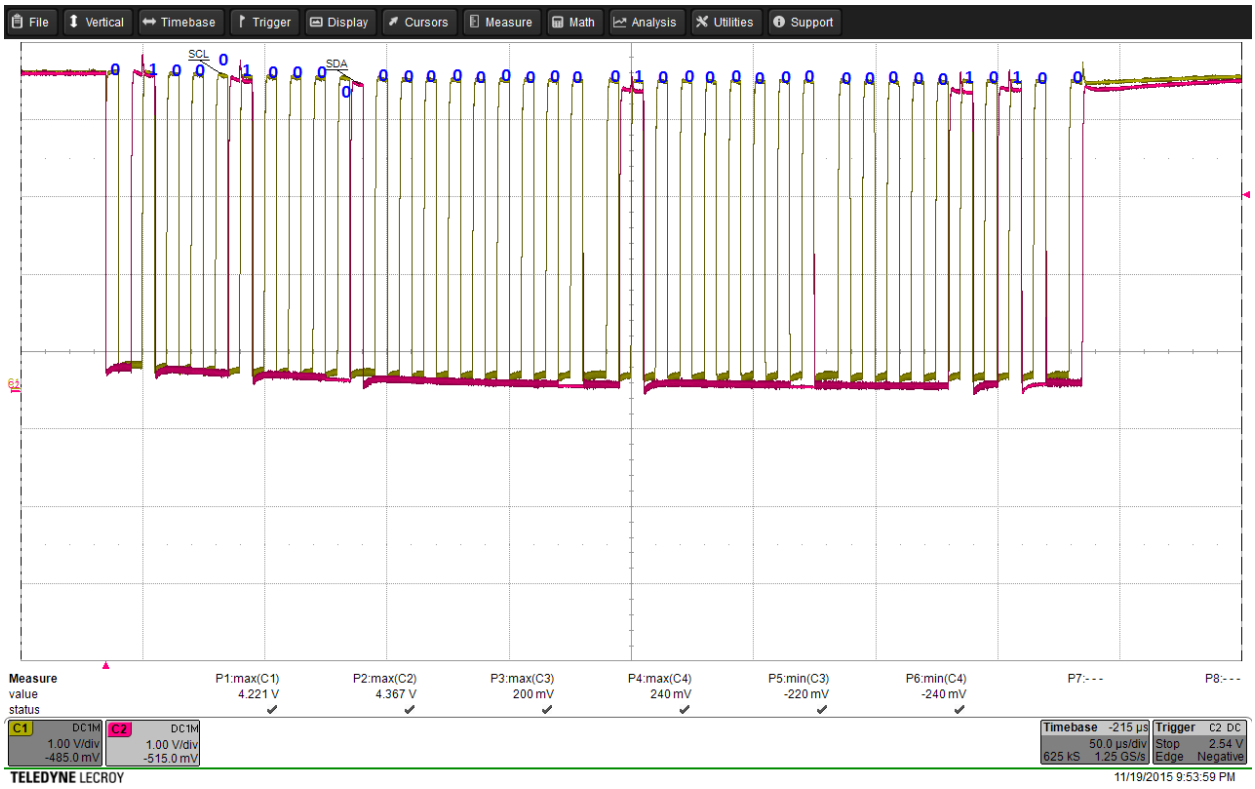

Figure 5-12. Oscilloscope Capture of INA226 Configuration

Here the transmission begins with a START signal being sent--depicted by the Channel 1 SCL signal held high while the Channel 2 SDA signal is pulled low. Thereafter, 10001000_2 is sent identifying the INA226 slave address and a low R/W signal for a write operation. Following the '0' acknowledgement (ACK) sent by the INA226, the pointer is set to the configuration register "x00" represented on the oscilloscope capture as the "00000000_2" byte and acknowledged by the INA226 with another '0' bit. Finally, the configuration register within the INA226 is set to "01000000_2"(x40) and "00000101_2"(x05) with two byte transfers so that the fastest continuous shunt voltage measurements are sent to the Arduino Mega. Acknowledge bits are sent confirming every byte transfer before a STOP signal is sent by the Arduino Mega with SCL held high while SDA is pulled high.

Once the configuration of the INA226 is complete, the pointer which determines the register to be read is set to the current shunt voltage register so that the Mega can continuously receive converted shunt voltage values as they become available.

To read the shunt voltage values in the shunt register, the Arduino is setup to follow the read timing diagram shown in Figure 5-13.

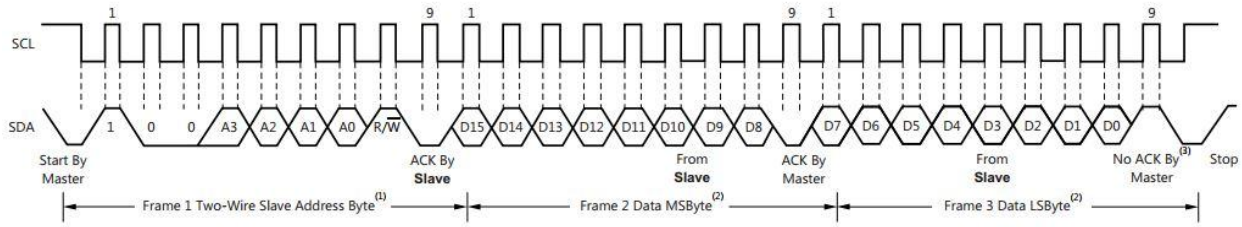

Figure 5-13. Reading Current Shunt Voltage from the INA226 [12]

The differential shunt voltage value read by the INA226's sense pins ranges from 0 to 80mV. Therefore for a 5mohm sense resistor, ~16A of current can be represented over 15-bits (~32000) saved in the shunt voltage register and transferred to the Arduino for monitoring. With just the Arduino and INA226 connected, the shunt voltage through the sense resistor was measured for 1A (Figure 5-13) current with the oscilloscope reading across SDA (Channel 2) and SCL (Channel 1) wires captured as shown below.

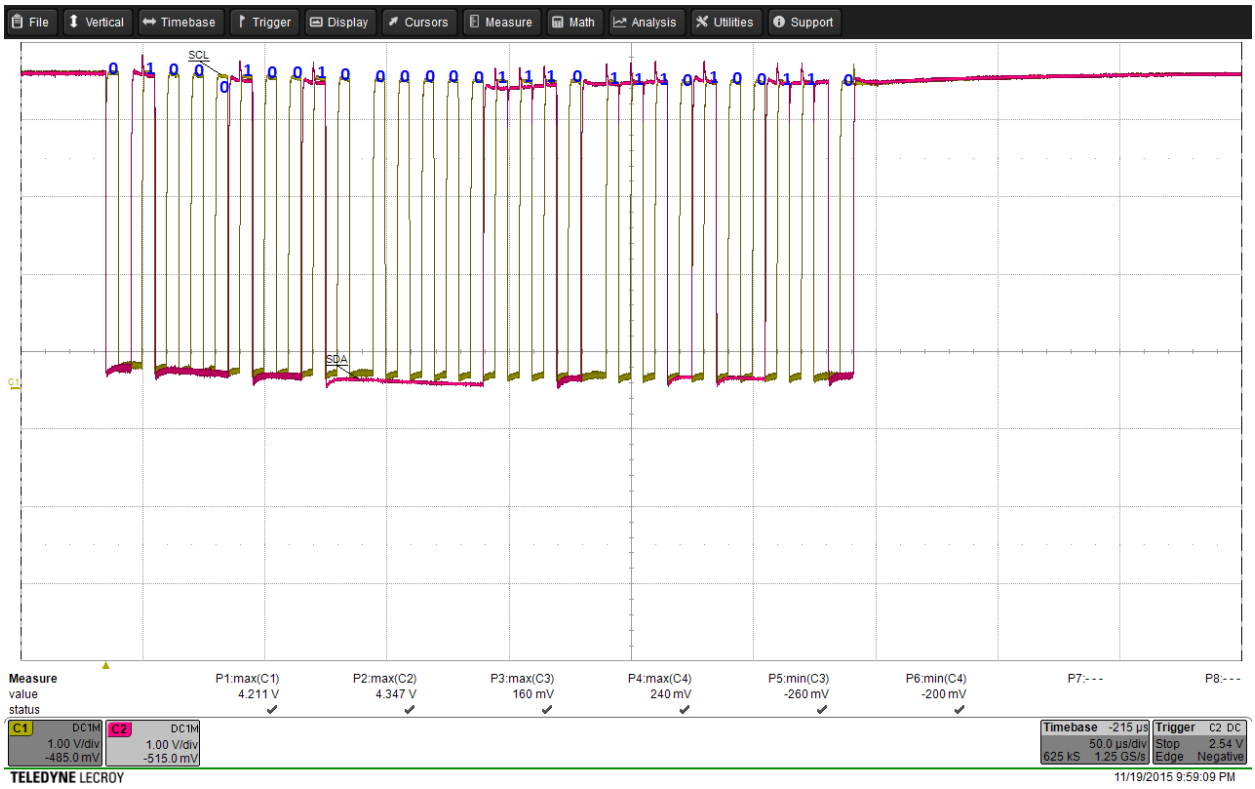

Figure 5-14. 1A reading I2C no Externals

In Figure 5-14, after the START signal is sent by the Arduino, the INA226 slave address is sent to the IC with the R/W bit set high to signify a read operation and the '0' acknowledgement leading to the "100010010_2" signal. Then the shunt voltage value saved in the 'x01' register is sent to the Arduino in two 8-bit (byte) data transfer operations. Here, "00000111_2" (Most Significant Byte, MSB) and "11101001_2" (Least Significant Byte, LSB) are concatenated to form "0000011111101001_2" = 'x07E9' = 2025_{10}. Assuming a linear scale,

$$16A \sim 32000 \; then \; 2025 \; corresponds \; to \; \frac{2025 * 16}{32000} = 1.0125A$$

The calculated current value is reasonably close to the 1A actual current flow through the circuit.

5.2.2 Switch Driver Requirements and Selection

If the current through the breaker exceeds the set threshold, a trip signal is sent from the Arduino to Linear Technologies' LT1910 High Side MOSFET Driver IC to open the FET and hereby commence the breaker opening process. In choosing the LT1910 as the driver for this breaker prototype, the input voltage of the breaker, on-time requirements, gate current drive and gate-to-source differential voltage needed to fully enhance an N-channel FET were all put into consideration. As the breaker will need to be in continuous on mode when there is no fault present plus the FET source is not grounded, a high side driver with an integrated charge pump that can provide ~12V gate-to-source voltage continuously was selected—LT1910. The LT1910 rated 48V comes in an 8-pin SOIC surface-mount package and needs a DIP adapter to be mounted on the protoboard as shown in Figure 5-15 below.

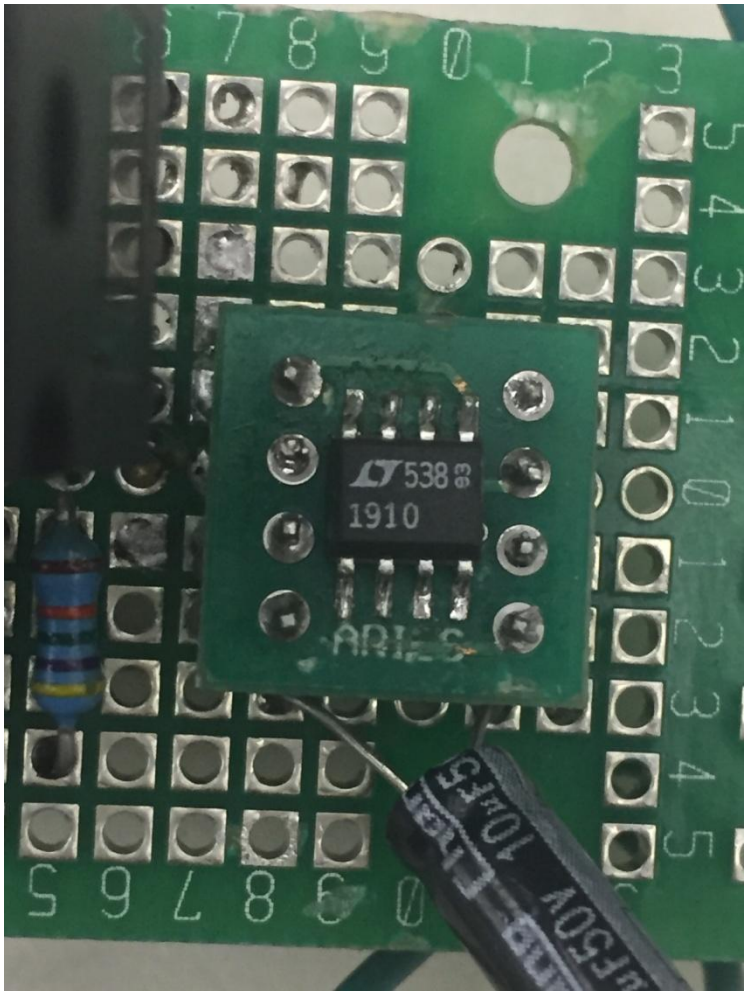

Figure 5-15. LT1910 High Side Driver

5.3 Breaker Assembly and Operation

The entire breaker was then assembled, soldered and built on a protoboard as shown in Figure 5-16.

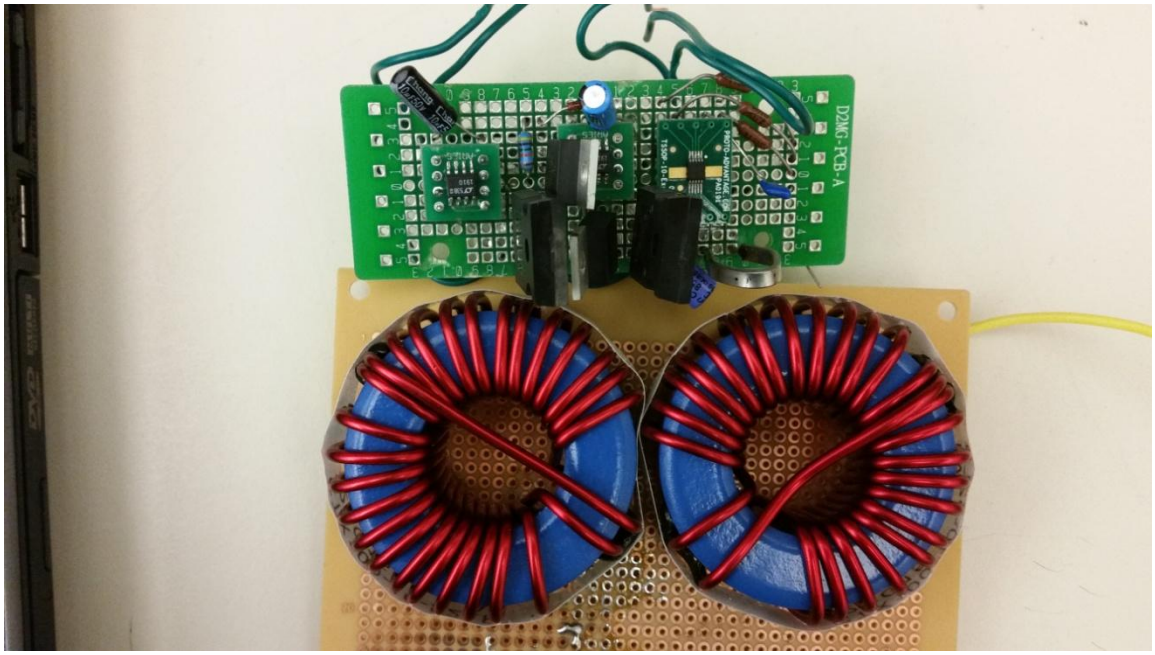

Figure 5-16. Assembled DC Breaker

Upon assembly, the shunt voltage across the sense pins of the INA226 was again measured with 1A flowing through the prototype and the results captured in Figure 5-17. Care should be taken to connect the Arduino ground pin to the same ground potential as the rest of the circuit so it can accurately detect voltages from interfaced components and correctly drive the input of the high side driver at 5V.

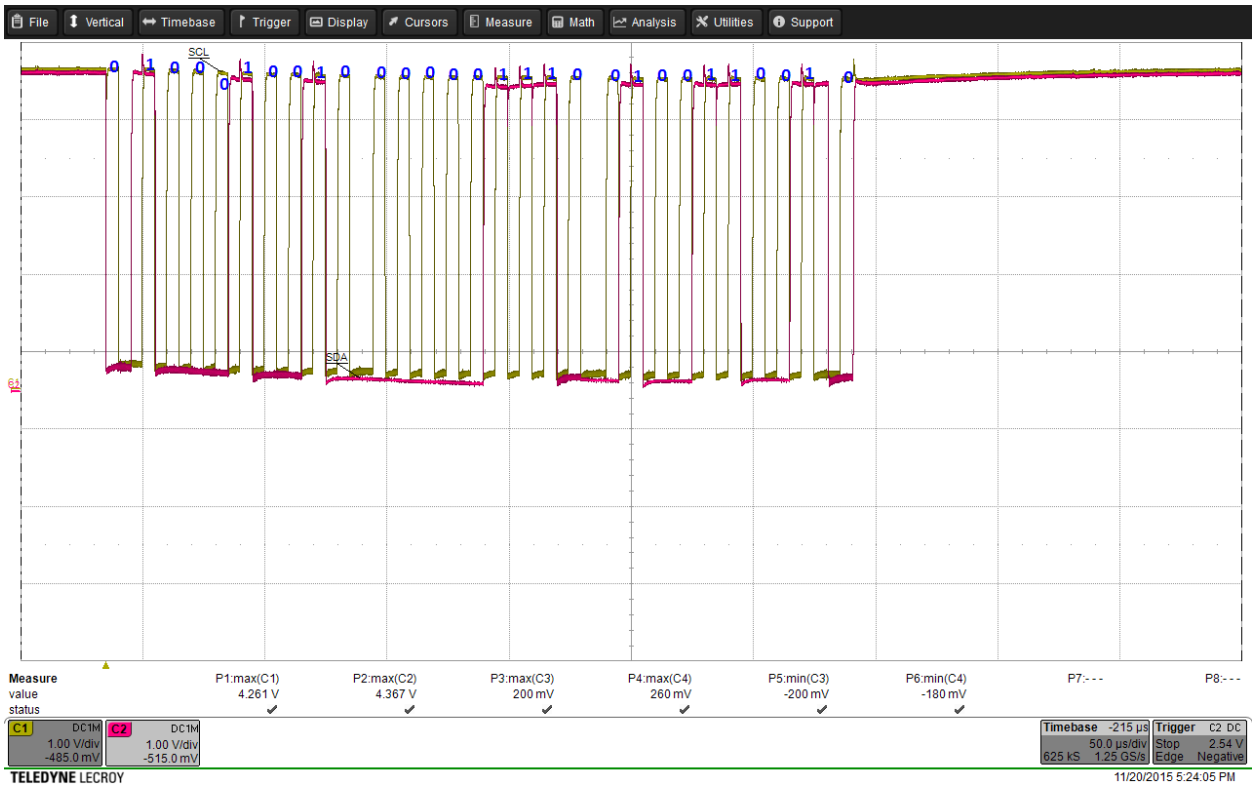

Figure 5-17. Full Breaker Module Calibration 1A

Again, there is the START signal then the "100010010_2" is sent by the Arduino to specify the slave address intended for I^2C read operation followed by the INA226 (slave device) transferring its shunt voltage register values in two 8-bit transfers followed by ACKs/NACKs and the STOP signal to end communications. "00000111_2" (MSB) and "01001100_2" (LSB) are combined to form "0000011101001100_2" = 'x074C' = 1868_{10}. Therefore, the control system would be reading a value of

$$16A \sim 32000 \; then \; 1868 \; corresponds \; to \; \frac{1868 * 16}{32000} = 0.934A$$

In order to compensate for this error, multiple readings were acquired with different current values drawn by the electronic load through the breaker. At 0A, the oscilloscope plot in Figure 5-18 was recorded.

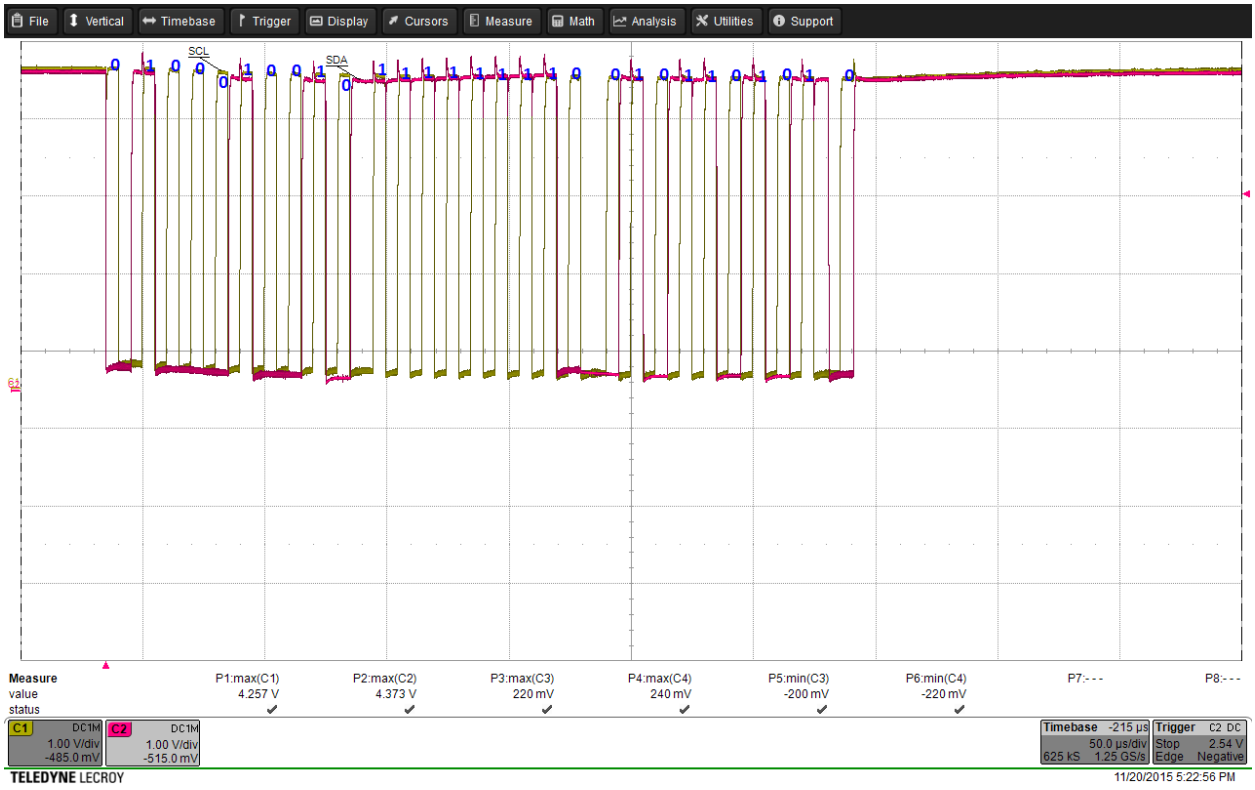

Figure 5-18. Full Breaker Module Calibration 0A

The value read here by the current shunt monitor with 0A flowing through the circuit when the MSB and LSB are combined is 1111111101011010_2. As the sign bit (16^{th} bit) is '1', this is a negative number and the INA226 shunt monitor represents negative numbers in a 2's complement format. The equivalent number then becomes $–(0000000010100101 + 1)_2$ or –(x00A6) equal to -166_{10}. This translates to approximately -0.083A leakage current likely through the body diode of the IGBTs. To account for this negative offset and increase device accuracy,

the formula used by the Arduino to estimate current flow from the voltage drop seen across the sense resistor was changed to the equation of a line with a negative intercept. After some curve fitting at different current levels, the modified equation then becomes;

Equation 5.1;

$$Current(Amps) = \frac{readValue + 250}{2100}$$

5.4 Measuring Breaker Performance

Once the breaker components were soldered together as shown above, the prototype breaker was tested with Si and SiC switching devices for different criteria.

i. Functionality: These tests were performed to ensure the breaker was working properly and to compare breaker response times and voltage/current decay speeds for Si, SiC devices.
    a. Electronic load test – This tests breaker functionality when slowly increasing load current passes a set threshold.
    b. Line fault test – This examines breaker behavior when a rapidly increasing fault current is present in the system.

ii. Power Dissipation: This test was conducted to contrast the efficiency, performance of both Si and SiC semiconductor devices during conduction.

iii. Temperature: This test aims to investigate the temperature rise of Si versus SiC devices.

5.4.1 Functionality: Si Electronic Load Test

For the electronic load test, the resistor in Figure 5-1 was replaced by the KIKUSUI PLZ303W electronic load as shown in Figure 5-19.

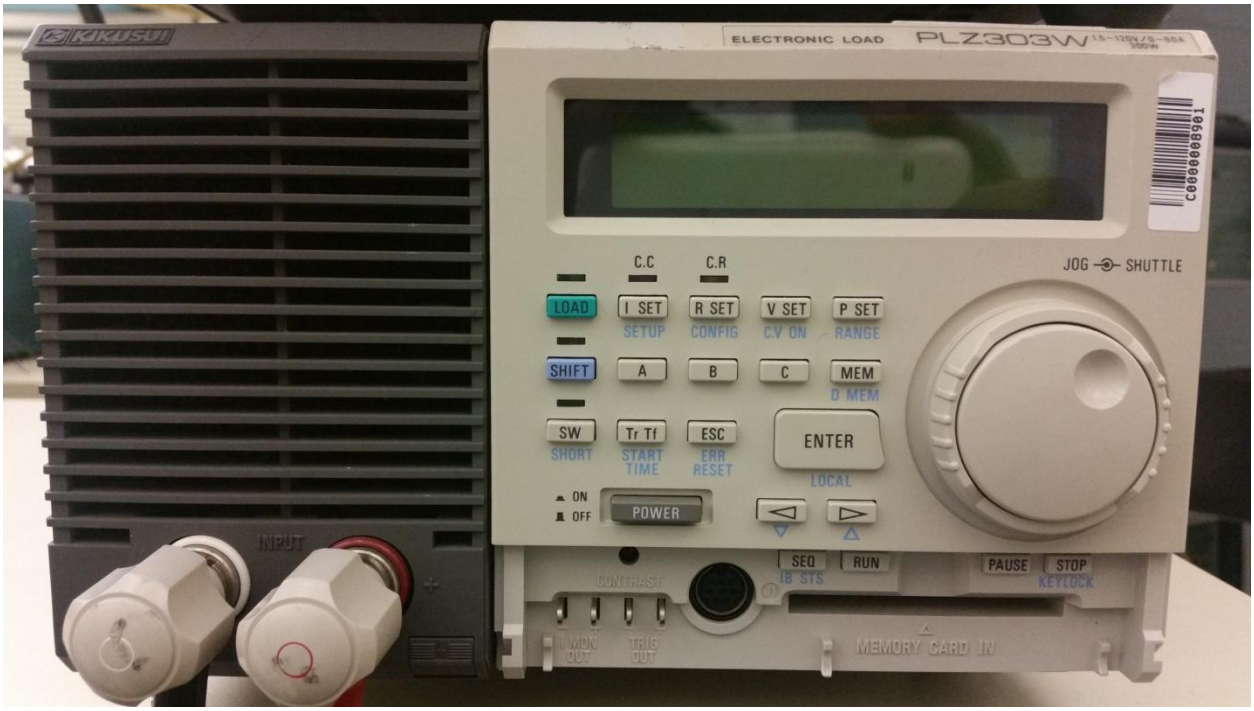

Figure 5-19. Electronic Load used in Functionality Test

The Arduino code was set to trigger the breaker and interrupt the current when the currentValue measurement from the INA226 exceeded 12000 as shown in Figure 5-16. This translates to approximately 5.83A. Figure 5-20 shows the original Arduino code used to operate the breaker with Equation 5.1 implemented to calculate the current in Amperes from the INA226 readings. The INA226 readings and estimated current in Amperes are then displayed on the UART screen every time the Arduino code in the loop is accessed.

```
void loop() {
  // put your main code here, to run repeatedly:
  int lowerShunt = 0;
  int upperShunt = 0;
  int currentValue;
  float CalculatedAmps;
  Serial.println("Starting current read");
  Wire.requestFrom(68, 2);     //request 2 bytes for shunt voltage from INA226

  if (2 <= Wire.available()){  //if two bytes were received
    upperShunt = Wire.read();      //high or upper byte
    lowerShunt |= Wire.read();     //low byte
    currentValue = (upperShunt << 8) + lowerShunt;  //left shift upper byte by 8bits
    Serial.println(currentValue);  //display value on new line in serial window
    CalculatedAmps = (currentValue+250.0)/2100.0;
    Serial.println(CalculatedAmps);
  }

  if (currentValue > 12000) {
  digitalWrite(2, LOW);
  digitalWrite(4, HIGH);
  delay(1);
  digitalWrite(4, LOW);
  }
```

Figure 5-20. Arduino Original Code

As the breaker prototype does not have any heat sinks or cooling fans attached, the IGBTs can only sustain higher current values for a short period of time before overheating and melting internally. In order to get around this problem, the electronic load was set to 5.6A with the current manually increased until the breaker sensed that the current threshold of ~5.83A had been exceeded and duly interrupted the current. The Lecroy oscilloscope was set to trigger and capture current and voltage readings when the voltage at node 1 in Figure 5-1 dropped below 700mV. The test was run for both zero output capacitance (Figure 5-21) and 10uF (Figure 5-22) output capacitance with the results captured on the Lecroy.

Figure 5-21. Si Breaker Electronic Load Test Results for Zero Output Cap

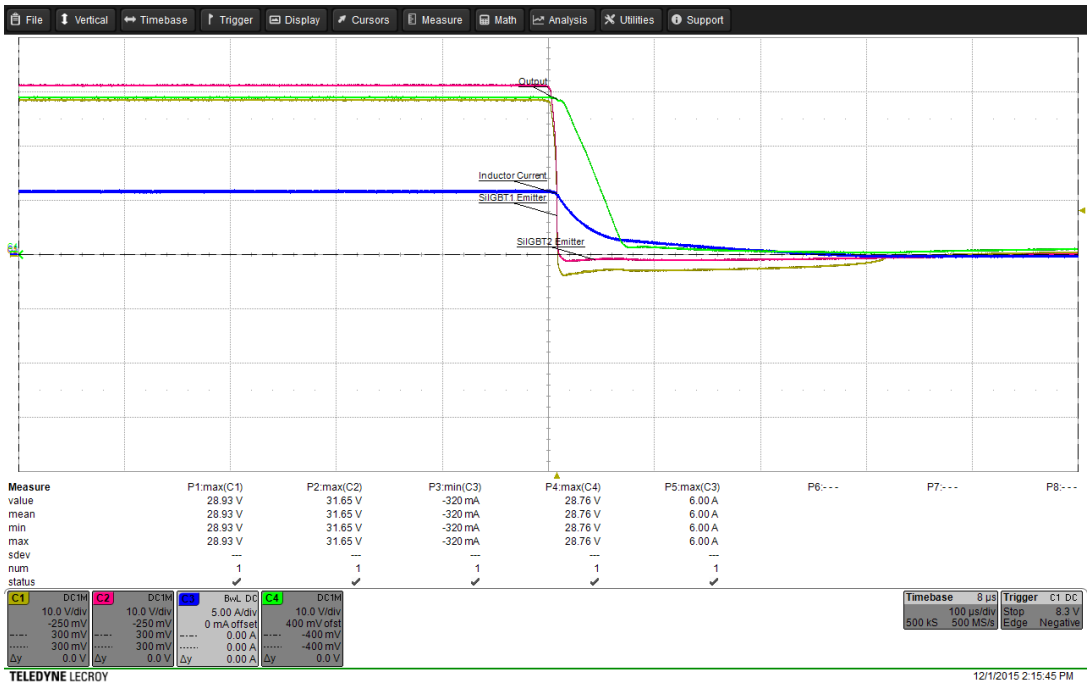

Figure 5-22. Si Breaker Electronic Load Test Results for 10uF Output Cap

Here the blue waveform represents the current through the inductor while the yellow waveform is the voltage at node 1 (IGBT1 Emitter) of Figure 5-1. The pink waveform measures the voltage at node 2 (IGBT2 Emitter) and the green waveform depicts the voltage at node 3 (Output Voltage). As shown, when the inductor current gets just under 6A, the breaker commences opening with node 1 and node 2 voltages rapidly dropping as the inductor current commutates to the freewheeling diode. The yellow waveform goes negative until the inductor current completes its decay due to the commutated current breaking down the 5V zener diode and applying approximately -5V potential across the inductor. The main difference between the captured waveforms in Figures 5-21 and 5-22 is the output voltage now takes about 66us to discharge when the output capacitor is present as opposed to ~6us with no output capacitor. This can largely be attributed to the discharge time of the capacitor. The IGBT emitter voltages also take slightly longer to get back to zero. Using the 10uF result, the Si IGBT emitter voltages at node 1 and node 2 have a decay-to-zero time of ~310us as shown in the red triangle of Figure 5-23.

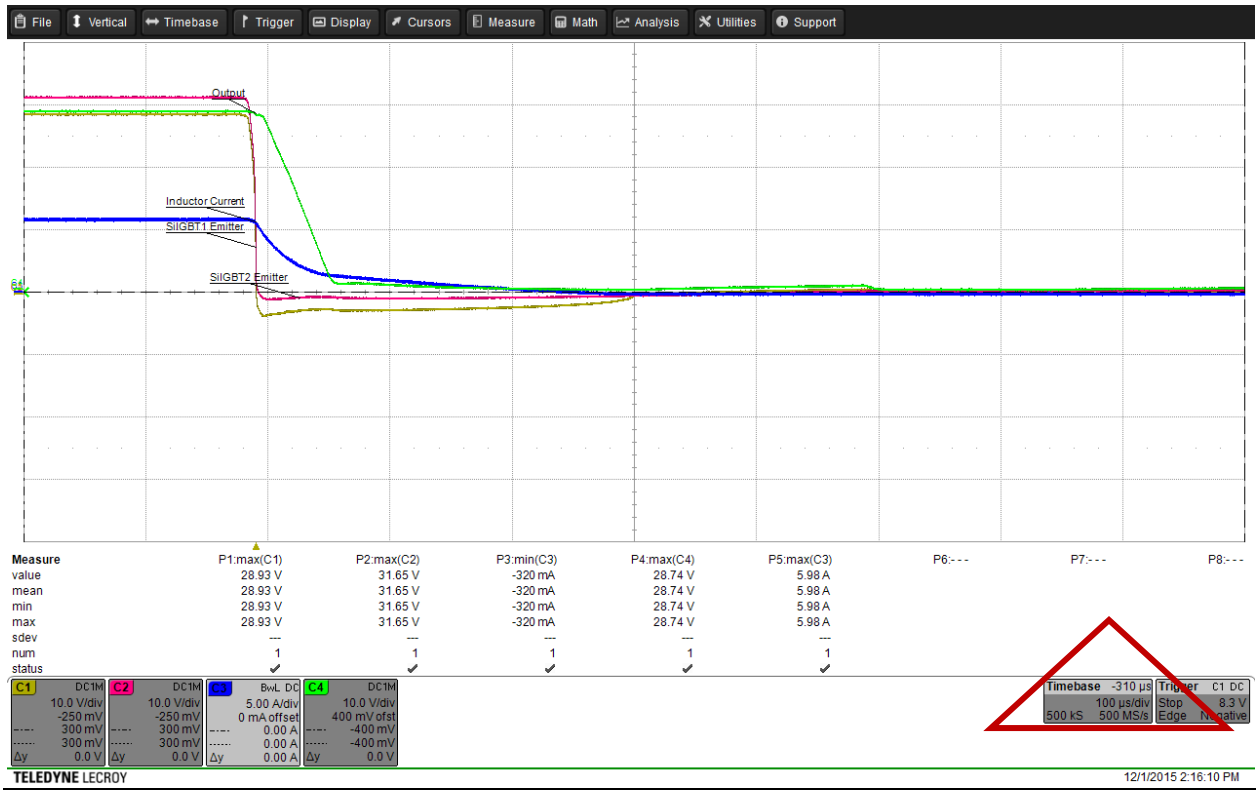

Figure 5-23. Si IGBT Emitter voltage decay

The current decay to 0A took slightly less time at ~220us. Unexpectedly, the voltage at node 1 does not rise to ~35V to signify an opportunity to reclose the breaker at zero voltage but stays at 0V before rising to ~4V after ~1.25ms. This peculiar behavior is shown in Figure 5-24.

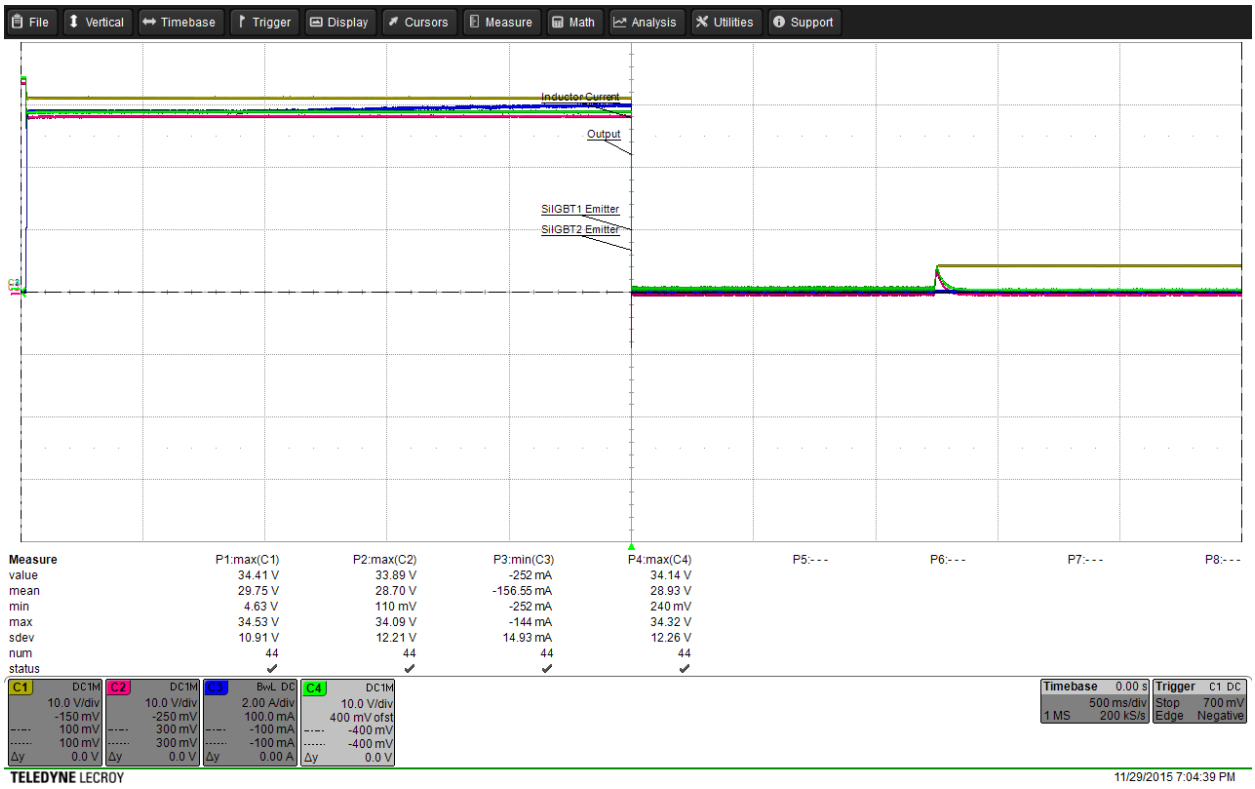

Figure 5-24. DC Breaker Reclosing Behavior

5.4.2 Functionality: Si Line Fault Test

The breaker prototype was then tested for its response to a line fault with a similar setup as the electronic load test. The major change to the test setup included adding the knife switch shown in Figure 5-25 in parallel to the grounded electronic load to simulate a line-to-ground fault in the system between some substantial system inductance and a load.

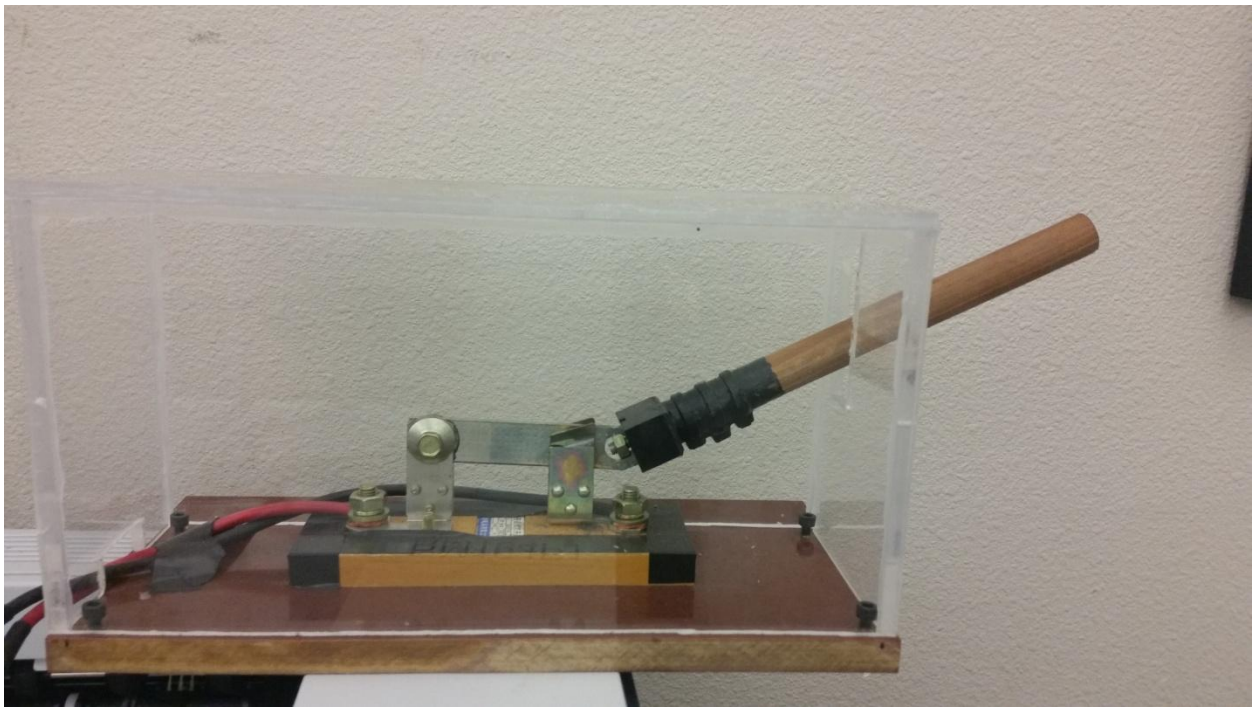

Figure 5-25. Knife Switch

The electronic load was set at 3A and shortly after, the knife switch was closed, simulating a line-to-ground fault in the system. The breaker was set to interrupt the current in the circuit when the threshold of ~5.83A was crossed with the test result captured in Figure 5-26.

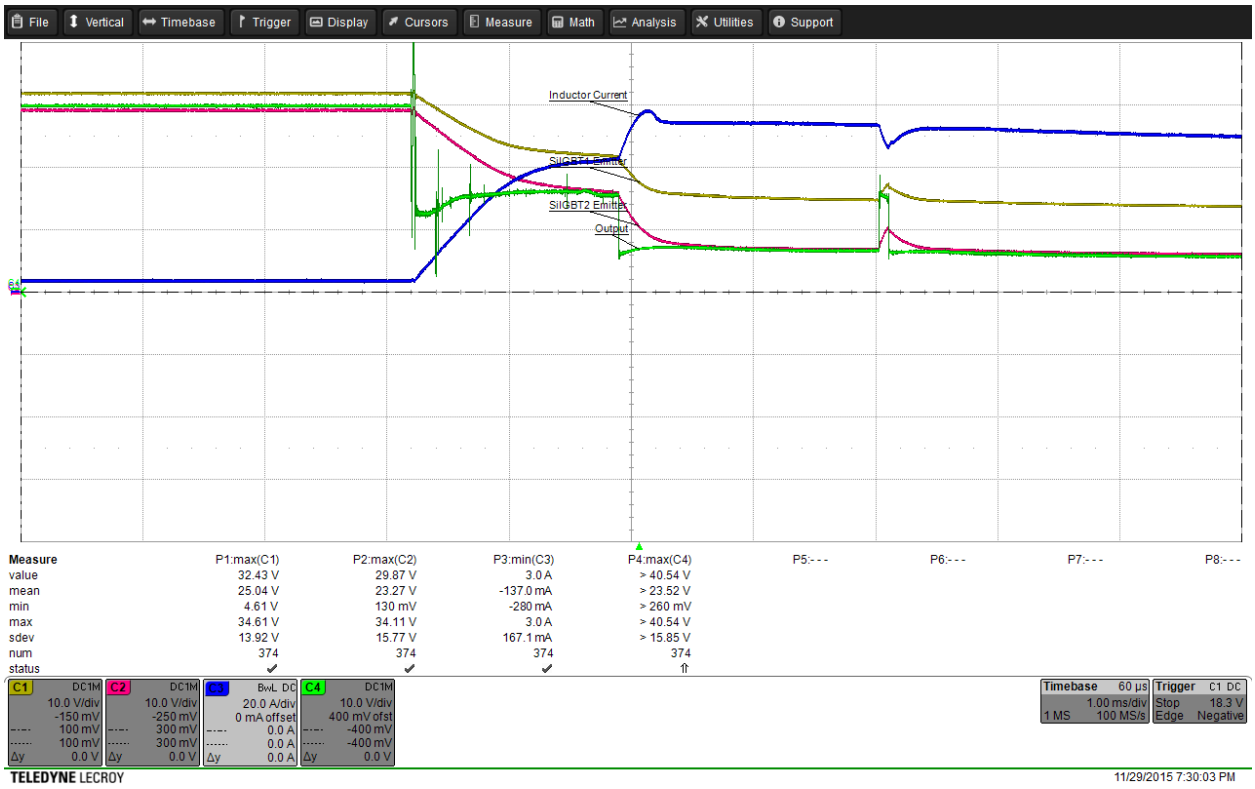

Figure 5-26. Si Breaker Line Fault Results

Unexpectedly, the current flowing through the inductor peaked at ~60A and crashed the power supply before the DC breaker prototype could arrest plus interrupt the rising fault current. Although the breaker eventually interrupted the fault current after about 43ms, the performance was unacceptably poor. As the INA226 sends readings of the shunt voltage measured across the sense resistor to the Arduino Mega every 140us (from the datasheet), and the Arduino Mega has a system clock running at a frequency of 16MHz (or period of 0.0625us), the culprit for the slow breaker reaction was likely the code implemented on the Mega. The code was slightly modified to omit the steps opening a UART channel/displaying current and shunt voltage readings as shown in Figure 5-27.

```
void loop() {
  // put your main code here, to run repeatedly:
  int lowerShunt = 0;
  int upperShunt = 0;
  int currentValue;
  float CalculatedAmps;
  //Serial.println("Starting current read");
  Wire.requestFrom(68, 2);     //request 2 bytes for shunt voltage from INA226

  if (2 <= Wire.available()){  //if two bytes were received
    upperShunt = Wire.read();      //high or upper byte
    lowerShunt |= Wire.read();     //low byte
    currentValue = (upperShunt << 8) + lowerShunt;  //left shift upper byte by 8bits
    //Serial.println(currentValue);  //display value on new line in serial window
    CalculatedAmps = (currentValue+250.0)/2100.0;
    //Serial.println(CalculatedAmps);
  }

  if (currentValue > 12000) {
  digitalWrite(2, LOW);
  digitalWrite(4, HIGH);
  //delay(1);
  //digitalWrite(4, LOW);
  }
```

Figure 5-27. Modified Breaker Arduino Code

The short circuit test was then rerun with the results in Figure 5-28. The breaker now takes about 500us (as much as 700us) to detect the current rise—this relatively small amount of time was enough to allow the inductor current to rise from 3A to ~30A before current surge arrest could start. The main reason for the rapid current rise is that the entire ~30V being passed by the IGBTs was applied across the inductor due to the ground short.

Figure 5-28. Si Breaker Updated Line Fault Test Result

The output voltage, IGBT emitter voltages and the inductor current all decay to zero after about 870us as shown in the red triangle on the bottom right portion of Figure 5-29. This value is significantly higher than the ~220us current decay time for the electronic load test but is expected due to the much higher initial current being interrupted.

Figure 5-29. Si Breaker Updated Line Fault Test Result for Decay

5.4.3 Power Dissipation Si

The performance of the breaker during conduction was also tested and documented with different load currents being supplied to the electronic load as displayed in Table 5-1.

I_{in}(A)	V_{in}(V)	I_{out}(A)	V_{out}(V)	Efficiency(%)
12	32.83	12	26.1	79.50
8	33.56	8	27.54	82.06
4	34.27	4	28.96	84.51
1	34.8	1	30.52	87.70
0.1	34.98	0.1	33.92	96.97

Table 5-1. Si Breaker Prototype Efficiency

The decreasing values for V_{in} at higher currents is due to the voltage drop across the long wires used to connect the 35V source to the breaker prototype. The power dissipation tests could only be run to 12A due to the 300W power limitation of the electronic load in the laboratory.

5.4.4 Temperature: Si IGBT Thermal Analysis

The thermal properties of the IRF G4PH30KD IGBT was then captured by measuring the temperature of IGBT1 with different current loads passing through the DC breaker. A thermocouple connected to a digital multimeter was affixed to the metal body of IGBT1 to get the temperature readings. As the IGBTs do not have a heat sink attached and cannot sustain heightened current levels for a long time, they were only loaded for 30secs. Three measurements were taken per current load over 50secs to account for post-turnoff heating and displayed in Table 5-2, then plotted in Figure 5-30.

Current(A)	Time Interval(s)	Avg Device Temp(°C)
2	0	22.7
2	10	27.2
2	15	31.05
2	20	33.77
2	25	38.2
2	30	41.93
2	35	45.1
2	40	45.7
2	45	45.9
2	50	45.75
4	0	22.57
4	10	30.37
4	15	38.83
4	20	46.05
4	25	53.17
4	30	61.63
4	35	69.6
4	40	72.03
4	45	72.47
4	50	72.2
6	0	22.6
6	10	34.13
6	15	46.47
6	20	62.1
6	25	76.65
6	30	91.35
6	35	100.65
6	40	104.05
6	45	103.8
6	50	102.05

Table 5-2. Si IGBT Thermal Data

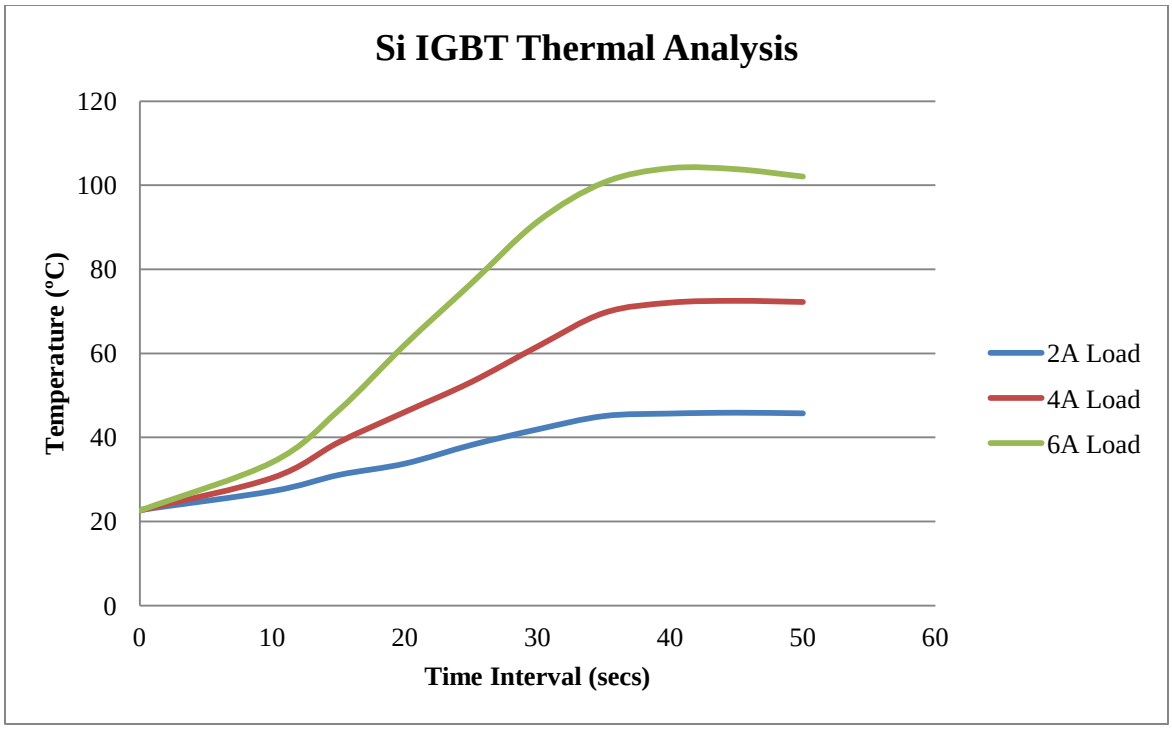

Figure 5-30. Si IGBT Thermal Performance

5.4.5 Functionality: SiC Electronic Load Test

The Si IGBTs soldered on the DC breaker prototype were replaced by CREE's C2M0040120D SiC MOFETs and run through the same electronic load test as used for the Si to get a comparison in performance. The test conditions and the breaker prototype components were exactly the same as the Si IGBTs' with a 10uF load capacitance and the breaker interrupting current whenever the 5.83A threshold was exceeded. The result was captured in Figure 5-31 below.

Figure 5-31. SiC Electronic Load Test Result

Here the SiC source terminal goes to zero briefly at 12us before staying slightly below zero until the inductor current decays to zero at ~480us as shown in Figure 5-32. There is a small voltage bump as the inductor current finally reaches zero. Also, the SiC MOSFET source voltages very closely track each other unlike the Si IGBT emitter voltages from Figure 5-23. This is due to a smaller voltage drop across each individual SiC switching device.

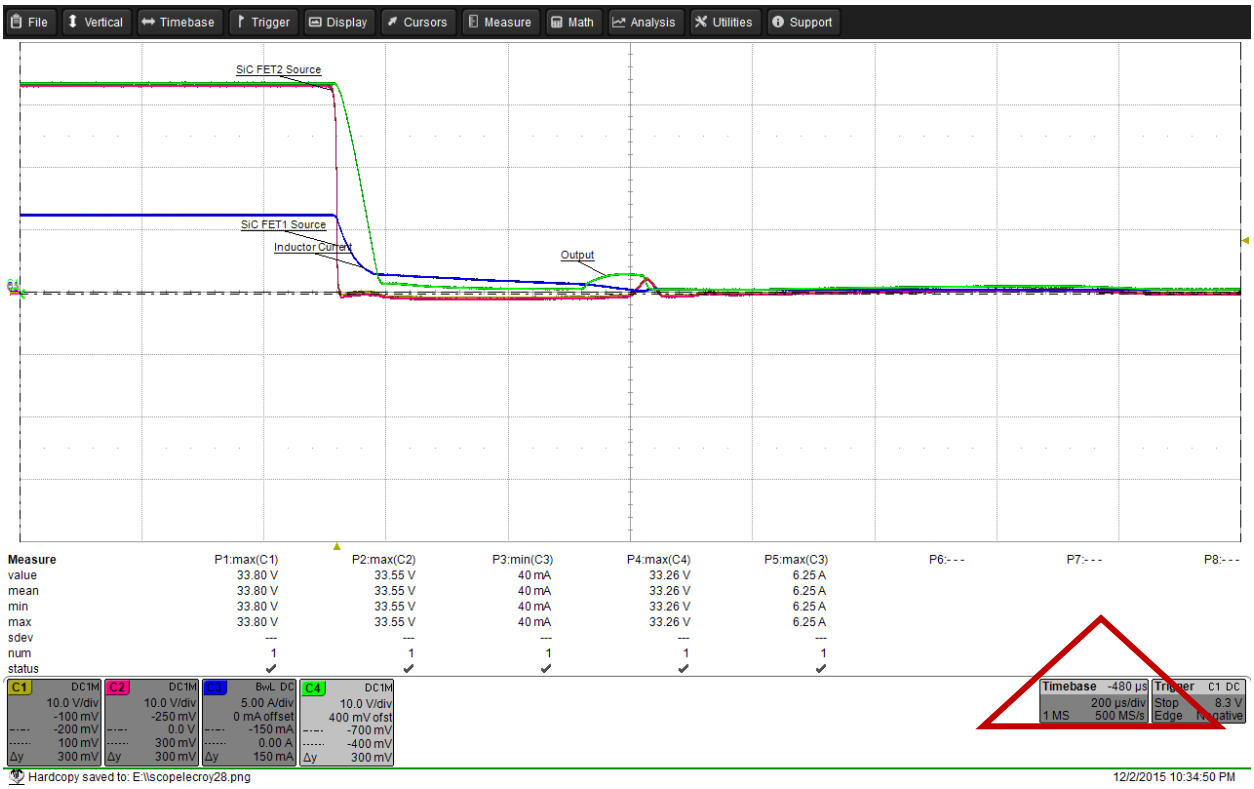

Figure 5-32. SiC MOSFET Source Voltage Decay

5.4.6 Functionality: SiC Line Fault Test

The SiC breaker was then put through a line fault test to document the difference in behavior. Just like the fault test with the Si IGBTs, the electronic load was programmed for 3A current and the DC breaker coded to interrupt when the current exceeded ~5.83A. The knife switch was again put in parallel with the electronic load and closed at time t=0 secs to simulate a line-to-ground fault in the system with the results recorded in Figure 5-33.

Figure 5-33. SiC Breaker Line Fault Test Result

The response time of the DC breaker to the current increase is ~530us with a current decay time of 930us. The current also rises from 3A to ~30A as was the case for the Si IGBTs.

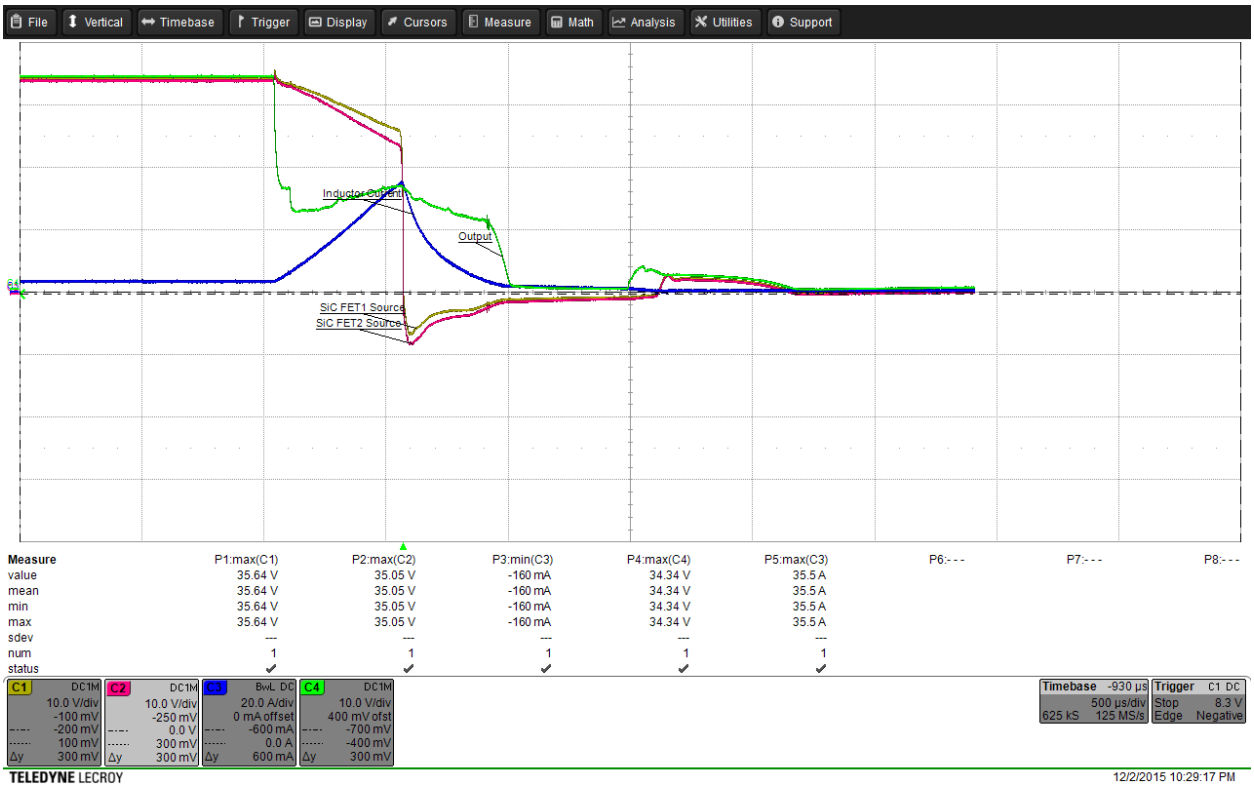

Figure 5-34. SiC Breaker Line Fault Current Decay

5.4.7 Power Dissipation SiC

The SiC breaker was then tested for power dissipation during conduction. The input and output voltages were measured at the breaker terminals to mitigate the effect of the voltage drop across the connecting wires as current through the breaker increased. The results were tabulated in Table 5-3.

I_{in}(A)	V_{in}(V)	I_{out}(A)	V_{out}(V)	Efficiency(%)
9	33.31	9	32.107	96.39
8	33.58	8	32.425	96.56
4	34.28	4	33.709	98.33
1	34.795	1	34.653	99.59
0.1	34.949	0.1	34.935	99.96

Table 5-3. SiC Breaker Prototype Efficiency

5.4.8 Temperature: SiC MOSFET Thermal Analysis

Just like the Si IGBT, the SiC MOSFET's thermal performance was captured by running the breaker at different loads for 30secs and capturing the average temperature readings in Table 5-4 and Figure 5-35.

Current(A)	Time Interval(s)	Avg Device Temp(°C)
2	0	24.3
2	10	24.47
2	15	24.6
2	20	24.73
2	25	24.87
2	30	25.07
2	35	25.17
2	40	25.27
2	45	25.3
2	50	25.23
4	0	24.3
4	10	24.6
4	15	25.35
4	20	25.73
4	25	26.55
4	30	27.23
4	35	27.77
4	40	28.07
4	45	28.17
4	50	28.2
6	0	24.2
6	10	25.1
6	15	26.13
6	20	27.9
6	25	29.83
6	30	31.3
6	35	32.3
6	40	33.07
6	45	33.57
6	50	33.67

Table 5-4. SiC MOSFET Thermal Data

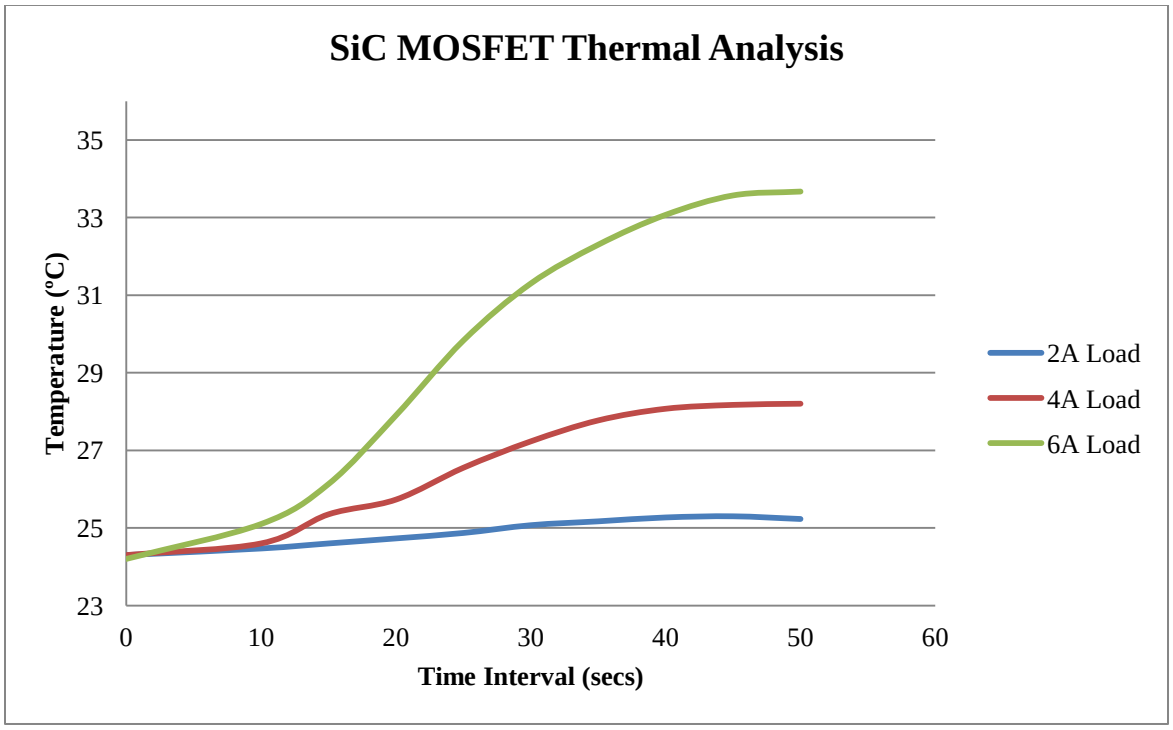

Figure 5-35. SiC MOSFET Thermal Performance

As shown in the figure and table above, the SiC MOSFET runs significantly cooler than the Si IGBT for the similar current load and conditions.

5.5 Switch N-channel Full- Enhancement and Efficient Reclosing

The peculiar behavior shown by the breaker prior to reclosing in Figure 5-24 was consistent regardless of switching device and was traced down to the driver's V+ power supply as depicted in Figure 5-36. Note the bypass capacitors are not included in the LT1910 IC configuration diagram for simplicity.

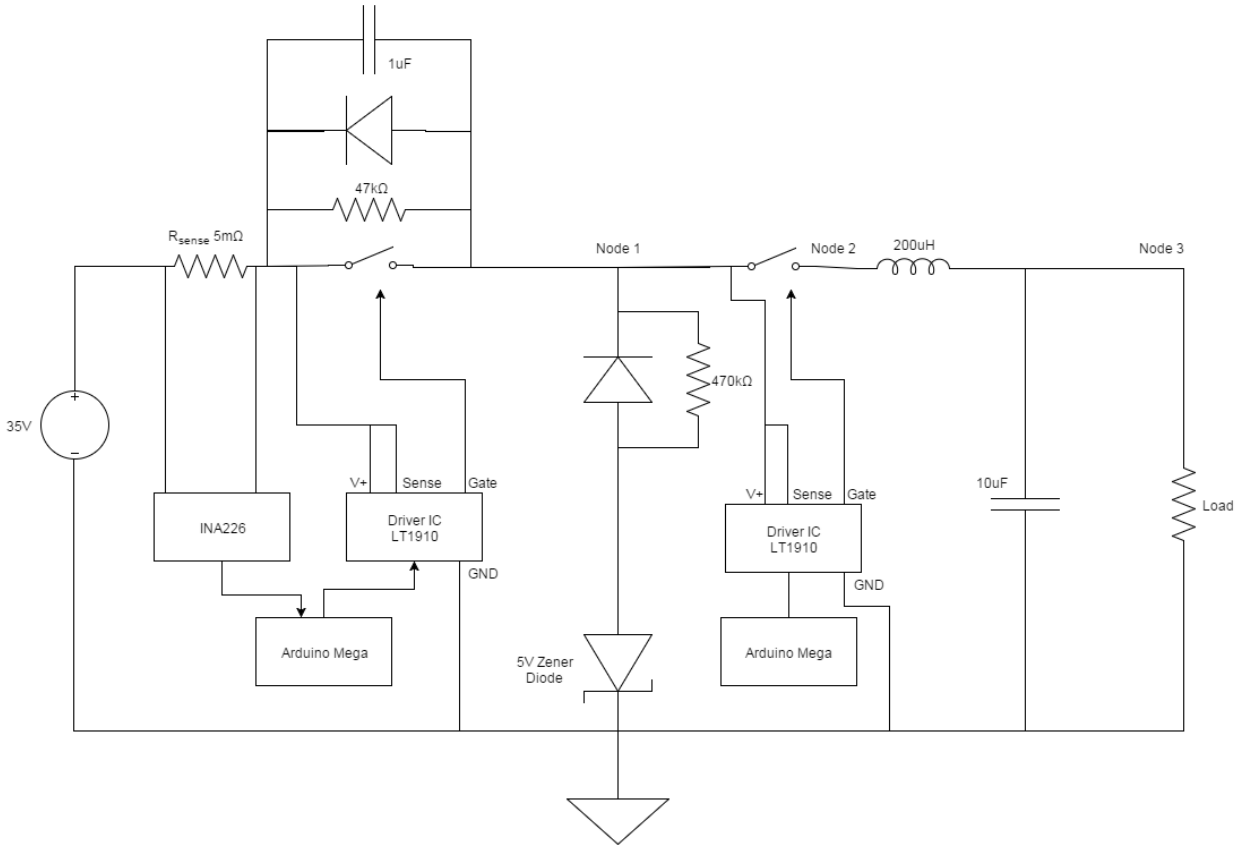

Figure 5-36. Switch Driver Loading Node 1

When both switching devices are off, the circuit reduces to that shown in Figure 5-36. The 470kΩ resistor in series with the 47kΩ essentially has the input impedance of the LT1910 driver IC in parallel with it. This combined with the other elements connected at Node 1 drastically reduces the effective resistance from 470kΩ to ~6.06kΩ leading to the 4V voltage seen at the node (voltage division of 35V between 47kΩ resistor and 6kΩ resistor).

Furthermore, the power dissipation performance between the two devices is not a wholly accurate comparison due to the relatively low V_{GS} voltage of ~12V maintained by the charge pump in the LT1910 configuration recommended by Linear Technologies [13]. In order to fully enhance both the IGBT (15V

recommended V_{GE}) and the MOSFET (20V recommended V_{GS}), modifications were made to the recommended driver configuration as shown in Figure 5-37. These modifications were made based on the "Low Side Driver" configurations of the LT1910 IC detailed in the datasheet [13] that allows the current-limited gate terminal of the IC to directly drive a clamp zener diode protecting the switching device.

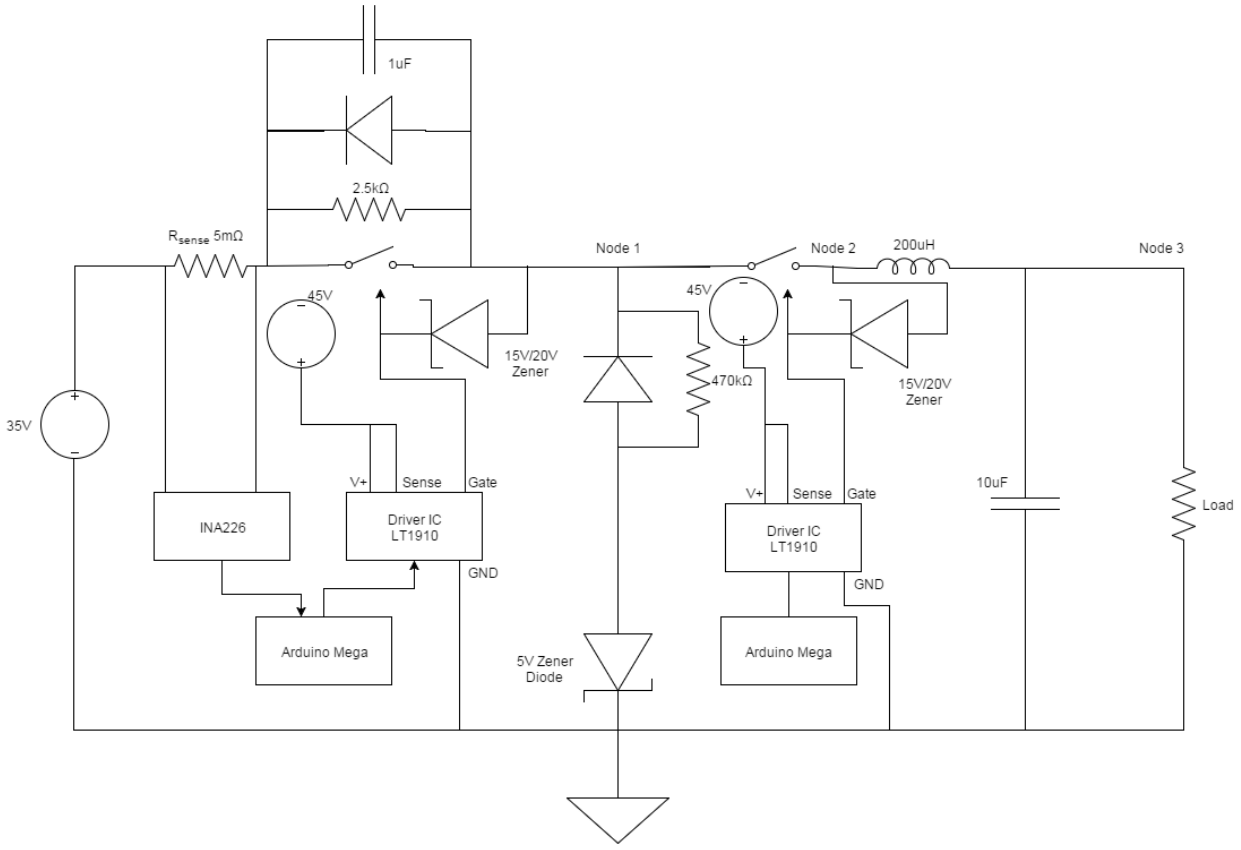

Figure 5-37. Modified LT1910 Driver Configuration

The LT1910 power supply was split from the 35V source V_{in} while limiting the gate-source/emitter voltages with the proper zener diodes—15V zener for Si IGBT and 20V zener for SiC FET. For example in the case of the SiC FET, the zener diodes ensure the gate voltage is never more than 20V above the source

voltage. The resulting breaker configuration provides full N-channel enhancement at device-recommended voltage levels for both the Si IGBT and the SiC FET. This modification also solves the problem of the LT1910's V+ terminal loading the 470kΩ resistor as the V+ terminal is now powered by a separate power supply instead of Node 1. Unfortunately, even with the IC's input impedance removed, other circuit elements connected to Node 1 still affect the effective resistance seen by the voltage divider. Therefore the snubber resistor was changed from 47kΩ to ~2.5kΩ to compensate for the lower balancing resistance.

5.5.1 Si Performance for Modified Driver

The electronic load test was repeated for both the Si IGBTs and the SiC FETs with the results displayed as shown in Figures 5-38 to 5-41.

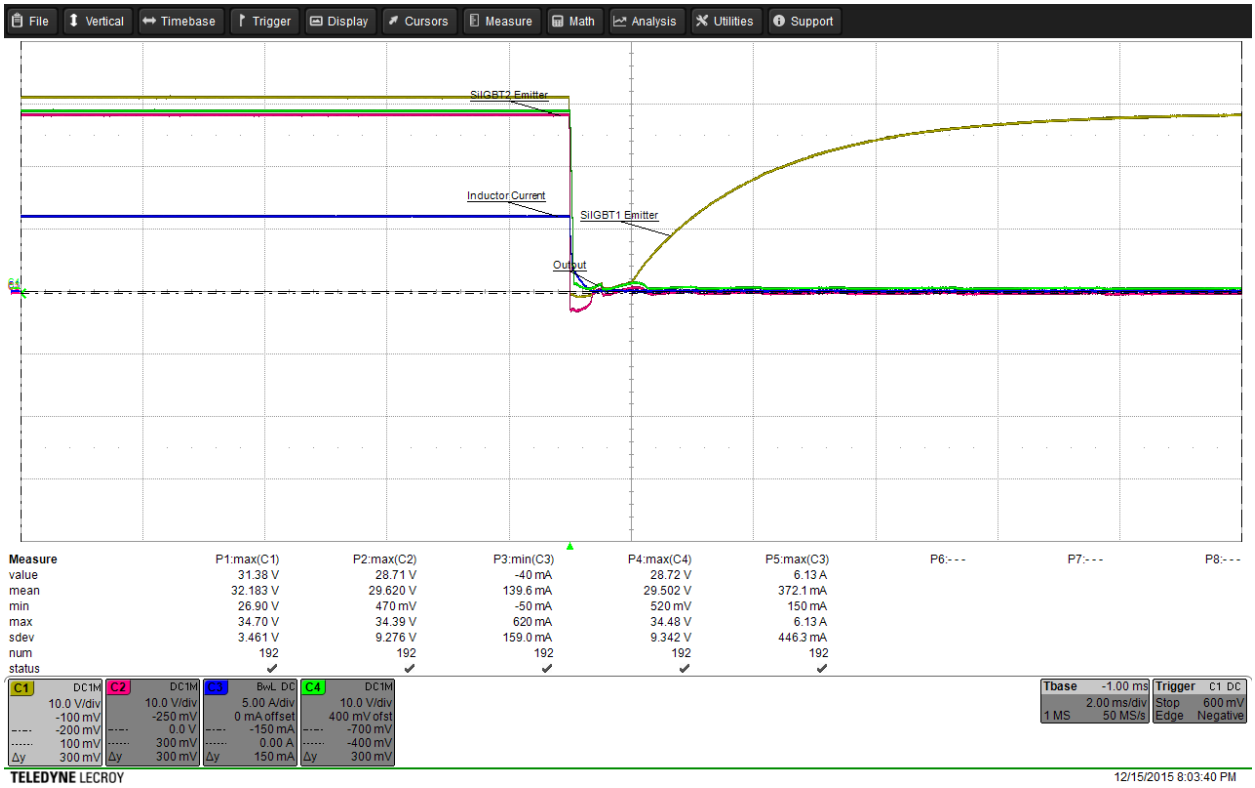

Figure 5-38. Si IGBT Electronic Load Test for Modified Driver

The inductor current decay took about 280us and the emitter voltages decayed after ~350us. The line fault test was also redone with the updated driver topology as shown in Figure 5-39.

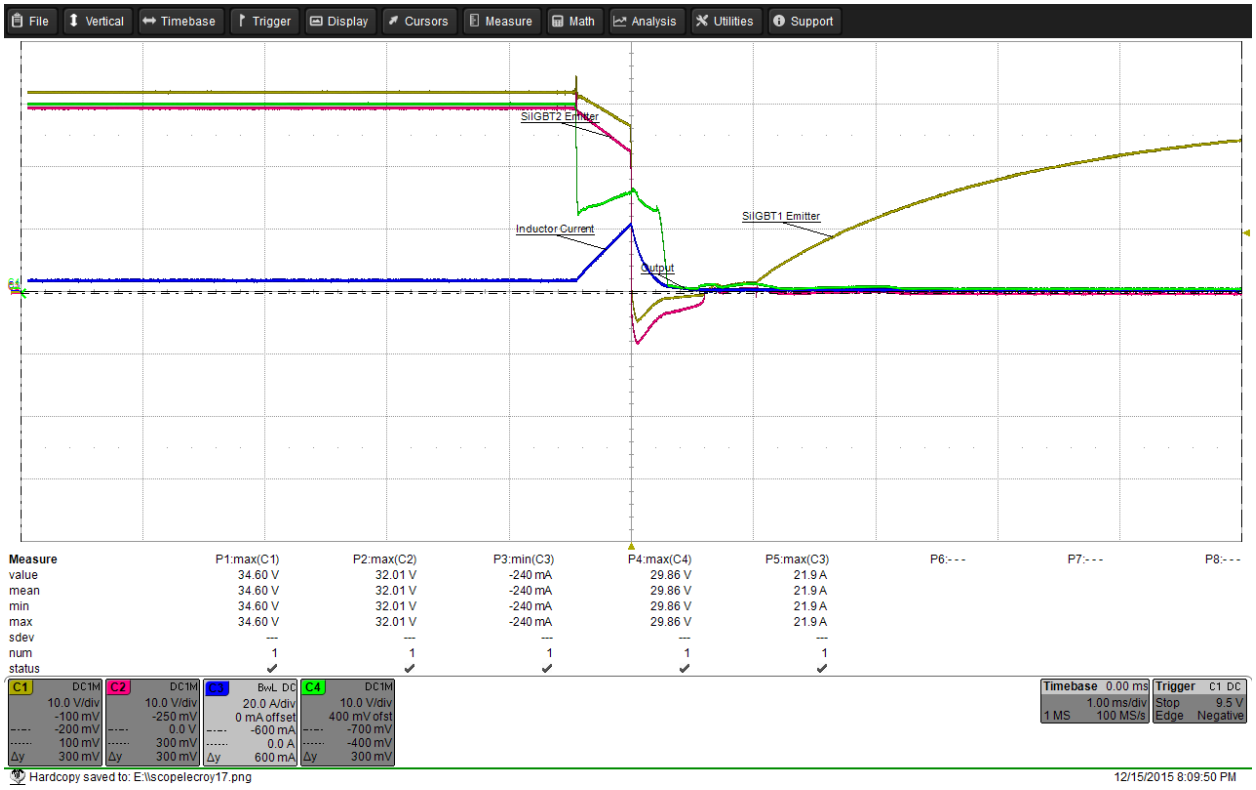

Figure 5-39. Si IGBT Line Fault Test for Modified Driver

The DC breaker's response was faster at 460us this instance and was captured in Figure 5-40. The current decay time was also significantly faster at 540us as the fast response time led to a lower peak current of ~22A.

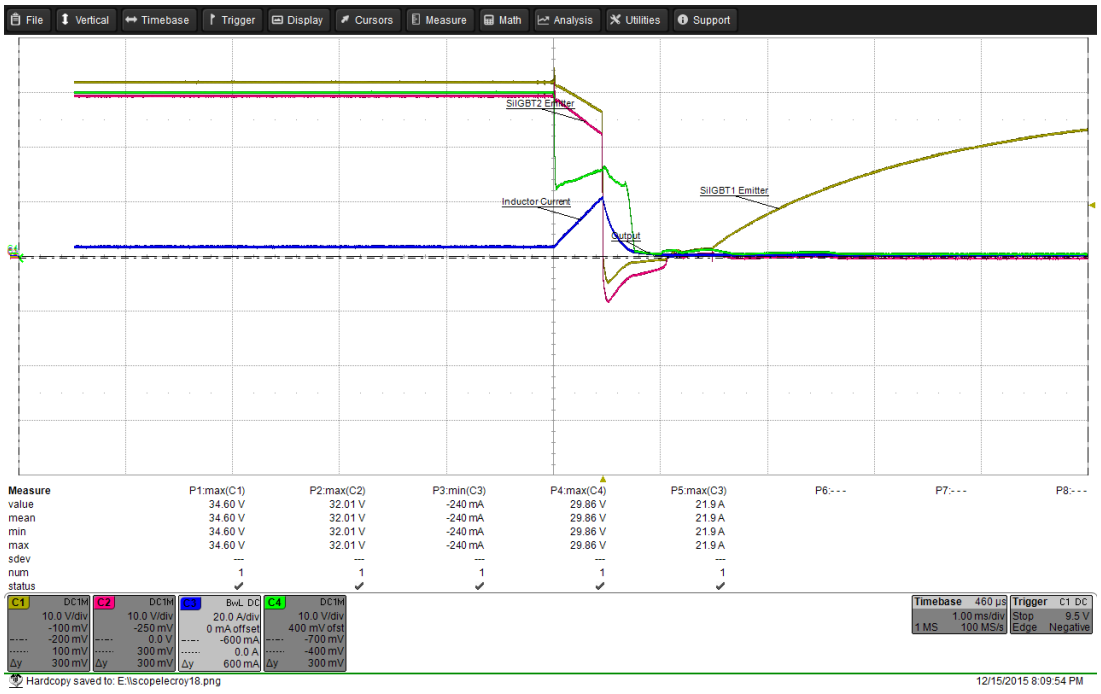

Figure 5-40. Si IGBT Line Fault Test for Modified Driver-Response Delay

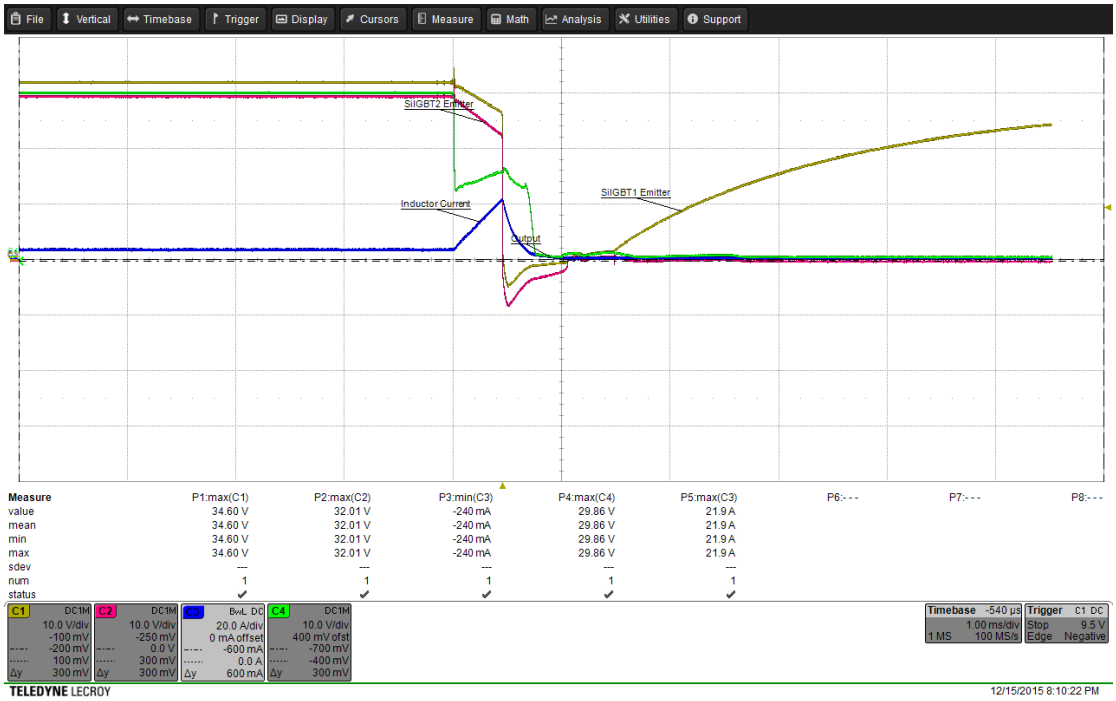

Figure 5-41. Si IGBT Line Fault Test for Modified Driver-Current Decay

Note that Node 1's voltage (SIGBT1's Emitter) in both instances starts rising after 1ms. This is due to the Arduino code controlling the breaker as shown in Figure 5-42. Specifically, IGBT2 is opened only after IGBT1 has been opened for 1ms. The rationale for the timing is to give the breaker's freewheeling zener path enough time to decay the inductor current before forcing all input current through the 470kΩ resistor.

```
void loop() {
  // put your main code here, to run repeatedly:
  int lowerShunt = 0;
  int upperShunt = 0;
  int currentValue;
  float CalculatedAmps;
  //Serial.println("Starting current read");
  Wire.requestFrom(68, 2);     //request 2 bytes for shunt voltage from INA226

  if (2 <= Wire.available()){  //if two bytes were received
    upperShunt = Wire.read();      //high or upper byte
    lowerShunt |= Wire.read();     //low byte
    currentValue = (upperShunt << 8) + lowerShunt;  //left shift upper byte by 8bits
    //Serial.println(currentValue);  //display value on new line in serial window
    CalculatedAmps = (currentValue+250.0)/2100.0;
    //Serial.println(CalculatedAmps);
  }

  if (currentValue > 12000) {
  digitalWrite(2, LOW);
  digitalWrite(4, HIGH);
  delay(1);
  digitalWrite(4, LOW);
  }
```

Figure 5-42. Breaker Arduino Code 1ms Delay

The power dissipation performance test was again repeated with the results in Table 5-5 below. Note that with a 300W limit, the electronic load can only handle ~12.5A at 23V Vout.

Iin	Vin	Iout	Vout	Efficiency
12	32.83	12	26.14	79.62
8	33.56	8	27.682	82.49
4	34.27	4	29.076	84.84
1	34.8	1	30.579	87.87
0.1	34.98	0.1	32.569	93.11

Table 5-5. Si Breaker Modified Driver Efficiency

When compared to the results of Table 5-1 obtained with the original driver configuration, there is very little efficiency gained from fully enhancing the Si IGBTs by having a V_{GE} of 15V as opposed to 12V.

5.5.2 SiC Performance for Modified Driver

The driver was again modified by replacing the 15V zener with a 20V zener and the breaker's Si IGBTs swapped out for the SiC MOSFET. The electronic load test, line fault test and power dissipation tests were then carried out for the SiC breaker with the results displayed in Figures 5-43 to 5-48.

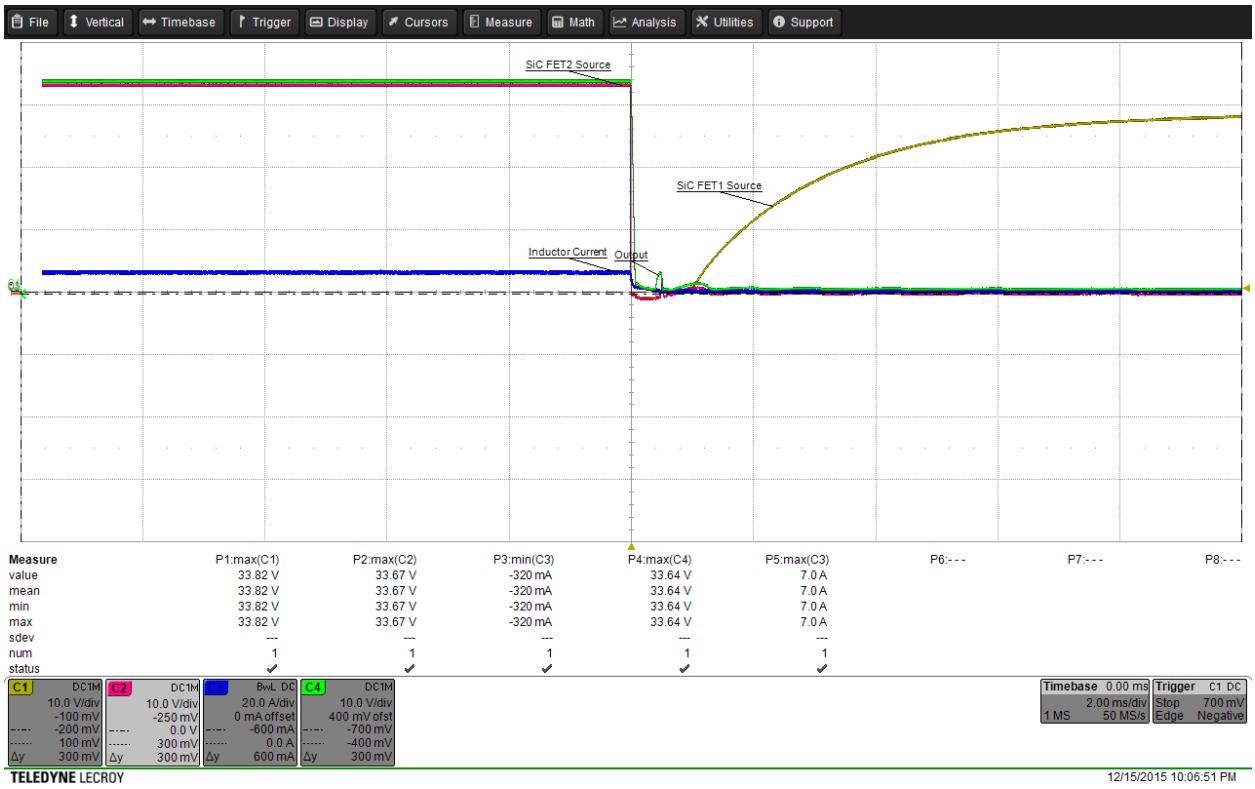

Figure 5-43. SiC FET Electronic Load Test for Modified Driver

Note that Node 1's voltage starts ramping up at 1ms (once FET2 is opened) and get to its maximum value at ~10.32ms. i.e. ~9.5ms wait needed to reclose breaker at low voltage levels to minimize power loss. The current and voltage decay again take ~480us. The results of the line fault test are also similar to those obtained using the original driver configuration.

Figure 5-44. SiC FET Line Fault Test for Modified Driver

The response time of the breaker was captured as ~590us as shown in Figure 5-45. Also the current had a peak of just under 40A with the current and voltage decay again taking about 920us.

Figure 5-45. SiC FET Line Fault Test for Modified Driver – Response Time

Lastly, the power dissipation performance of the SiC breaker was evaluated for fully enhanced FETs with a V_{GS} of 20V. The results captured are provided in Table 5-6.

Iin	Vin	Iout	Vout	Efficiency
9	33.31	9	32.451	97.42
8	33.58	8	32.743	97.51
4	34.28	4	33.863	98.78
1	34.795	1	34.692	99.70
0.1	34.949	0.1	34.939	99.97

Table 5-6. SiC Breaker Modified Driver Efficiency

At lower loads, the efficiency of the SiC breaker is not too different when compared to the original driver configuration's results from Table 5-3 but at higher loads, there appears a widening improvement in performance for the fully enhanced SiC. This relationship could not be explored further due to the 300W limitation of the electronic load used in the laboratory.

5.6 Comparative Analysis of Si & SiC

Collating the Si and SiC results obtained from the electronic load tests run on the breaker, for the Si IGBTs, the voltage decayed at 350us, the inductor current decayed to zero at 280us while in the case of the SiC FETs, both the voltage and inductor current decayed completely to zero at 480us.

For the line fault test with Si IGBTs, the breaker responded by interrupting the current surge after 460us and the inductor current decayed to zero in 540us. When conducted with SiC FETs, the current totally decayed to zero after 920us and the breaker response time was recorded as 590us.

As expected, the SiC FETs clearly outperformed the Si IGBTs during the power efficiency tests as shown in Figure 5-46. This lower conduction loss of the SiC breaker is significant as DC breakers are designed to be on most of the time.

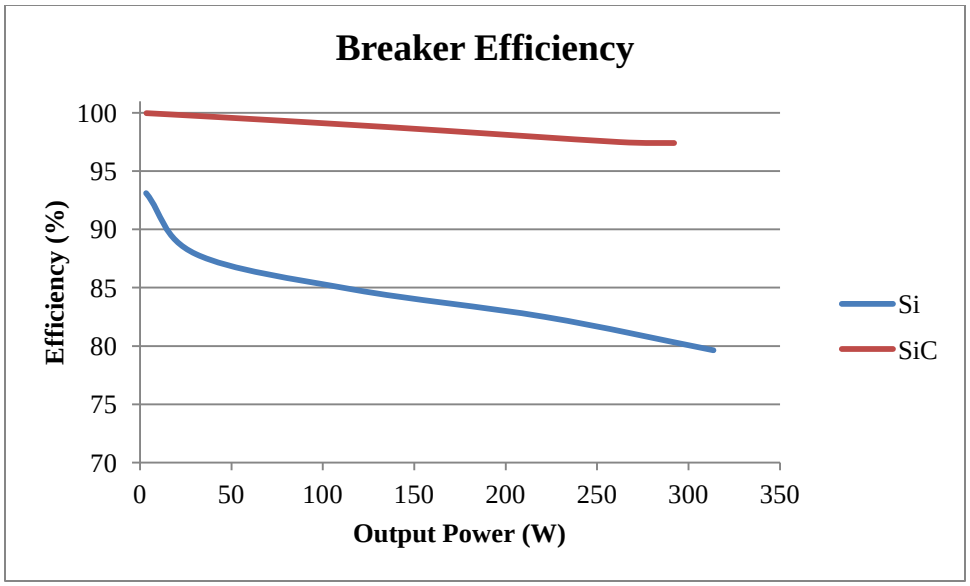

Figure 5-46. SiC and Si Breaker Efficiency Comparison

Lastly, the thermal performance of the Si and SiC devices at different current loads were overlaid in Figures 5-47 to 5-49 as shown.

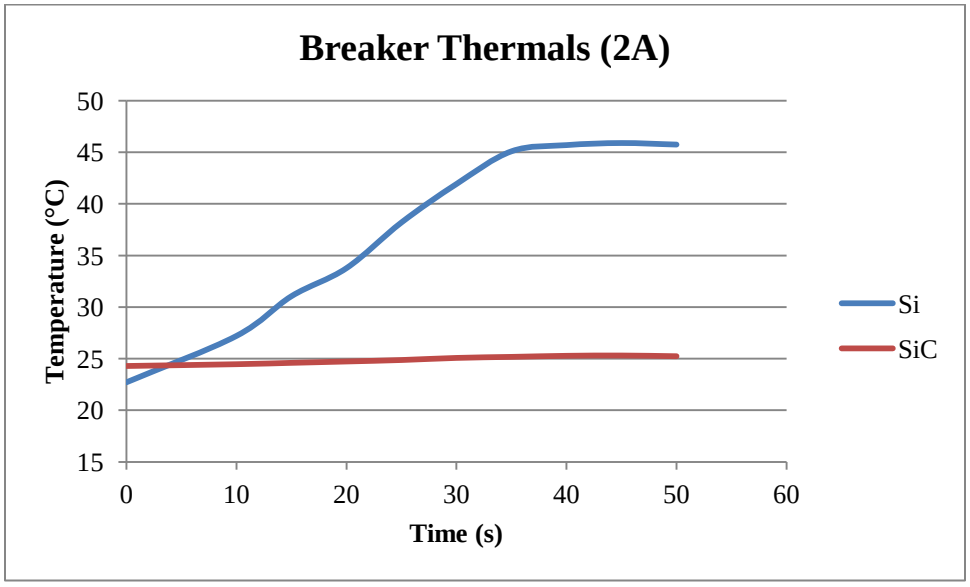

Figure 5-47. SiC and Si Breaker Thermals Comparison – 2A

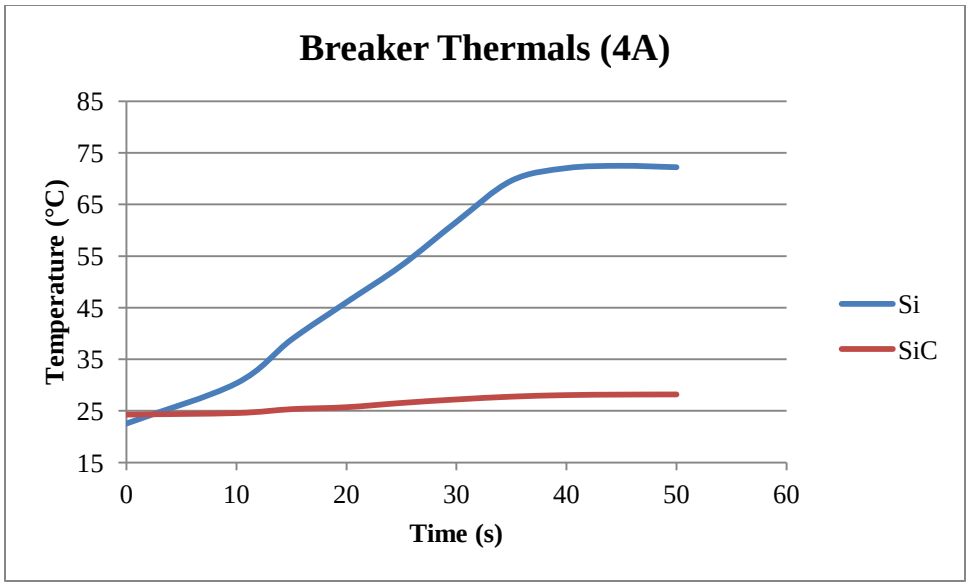

Figure 5-48. SiC and Si Breaker Thermals Comparison – 4A

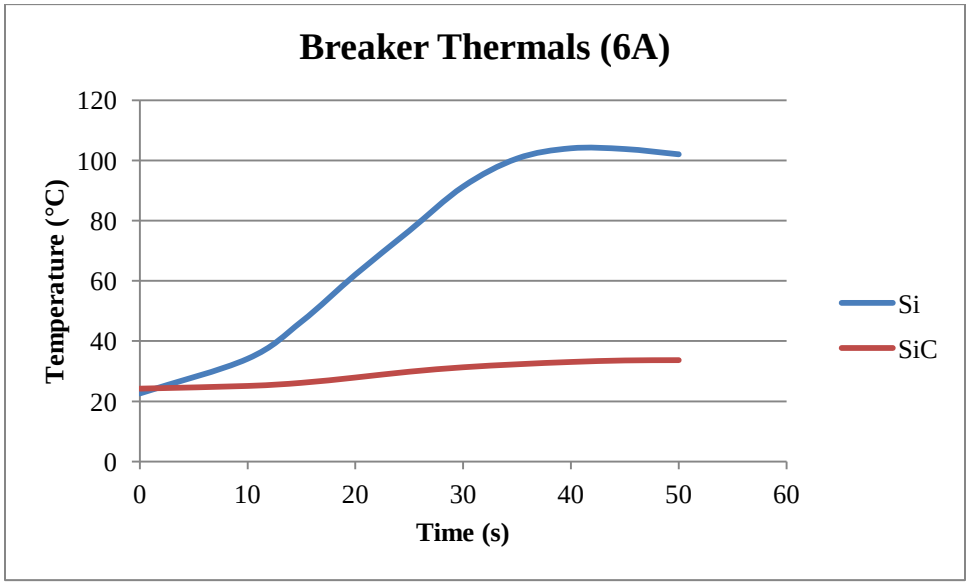

Figure 5-49. SiC and Si Breaker Thermals Comparison – 6A

The SiC breaker clearly outperforms the Si in thermals and runs significantly cooler that the Si IGBTs.

6 CONCLUSION AND FUTURE WORK

This thesis originally aimed to compare the performance of Si and SiC semiconductor breakers based on a known topology proposed by Ko Sano and Masahiro Takasaki [11] but due to the unexpected results obtained during simulation, the breaker topology was modified for passive loads. The proposed breaker interrupts the fault current within 2.3% of the time taken by an electromechanical breaker. Also, while both the SiC and Si breakers interrupt current as expected, the SiC MOSFET clearly outperforms the Si IGBT only when it comes to power dissipation and thermal performance. It slightly lags the IGBT when comparing speed of emitter/source decay and current decay. The SiC breaker has 15-20% higher efficiency than its Si counterpart between 150W and 300W and as much as 60°C ΔT advantage after running 6A for 30secs.

Future work would involve replacing the SiC MOSFET and LT1910 driver with GaN devices and their specialized drivers in order to get a full spectrum of wideband-gap device performance versus Si switching devices in a DC breaker. Furthermore, the power dissipation of the fully enhanced Si/SiC breaker needs further evaluation at higher loads with a larger capacity electronic load. Another possibility is to run both the Si and SiC breakers at max load for an extended period of time to get an idea of performance over time and failure rates—this would need appropriate heat sinks to cool down the switching devices. Finally, the DC breaker's current response time of ~700us can be improved further by reducing the processing overhead of the monitoring device—FPGA instead of

Arduino, or simpler current-monitoring/switch-operating technique instead of the INA226.

Lastly, since the DC breaker is likely to conduct during most of its operation and only trip when a few unexpected events occur, the higher conduction efficiency of the SiC FET makes it a much better choice for a DC breaker.

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