EMBEDDED POWER ACTIVE CONTACT LENS

A Thesis

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Master of Science in Engineering

by

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ABSTRACT

Embedded Power Active Contact Lens

This thesis designed and fabricated an active contact lens that notifies the user during the detection of an external wireless signal. The lens contained a printed antenna to communicate with a 2.4GHz system and provide inductive charging operating at 13.56 MHz. The lens utilizes a CBC005 5μAh thin film battery by Cymbet as a power source. A custom IC was designed using the On Semiconductor CMOS C5 0.6 μm process to manage the battery and drive the display. A printed single element display using electrochromic ink was chosen as it is able to indicate the user when activated while staying transparent. Lastly, this thesis analyzes the material properties of the chosen substrate for it clearness, flexibility, and biocompatibility to determine its suitability as a contact lens material.

Keywords: contact lens, IC, chip, antenna, printing, screen, loop, inductive, charging, electrochromic, wirebonding

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TABLE OF CONTENTS

LIST OF TABLES

Table   Page

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

Transparent circuits are still a new research area at Cal Poly and have only gained popularity with industry in the past 3 or 4 years. Only a few schools have been participating in this area of research and Cal Poly is aiming to be one of those schools. Researching transparent circuits provides us with a pathway to devices that we previously thought to be unfeasible – one of them being a circuit on a contact lens. These technological advancements allows for an improved way of life by providing a real-time heads-up-display (HUD) for use on contact lenses. Integrating an easily viewable display with an external wireless biomedical sensing system allows for an immediate notification during a potentially health threatening event. In many situations, factors that attribute to those events are not immediately detectable by our senses (e.g. external sources such as radiation and odorless fumes or internal such as glucose levels and cardiac behavior). Thus the individual must rely on external equipment as a safety measure. Such equipment should be unobtrusive such that it does not hinder one's ability to perform his or her task while also readily viewable to the user. Much research has been done on implementing sensors to be located on a contact lens. Huang *et al*. presented a ring-shaped microcapacitor as a pressure sensor to measure intraocular pressure. Kim *et al*. measured ocular movement by embedding magnets in a contact lens and measured eye movements using external magnetoresistive sensors. However, not all proposed contact lens sensors were active systems that required electrical power. Yan fabricated a contact lens pressure sensor that utilizes a microfluidic network as the sensor and information relay [1]. Various papers have investigated energy scavenging methods on a contact lens. Pandey *et al*. fabricated a contact lens with a single LED display powered by 2.4GHz [2]. Cheng *et al* presented a 5.8GHz rectenna design focusing on increasing efficiency by using high Q passive components to impedance match the antenna to the rectifier [3]. The drawback of RF scavenging is that the levels of energy present in the environment are small. In addition, the free space path loss causes the end-to-end efficiency of an RF scavenging system to

suffer. The advancements over these systems that our system provides is 1) The on-lens battery allows for operation even when an external supply is not being applied and 2) the coupled antenna and battery charger provides for more efficient power management.

This device is manufactured by screen printing conductive layers on top of a transparent substrate. The method of screen printing circuits is preferred because of its versatility. Printed electronics allows us to print using a wide variety of transparent and flexible substrates – ideal for this application. This technique of screen printing circuit board layouts can be miniaturized, when following stricter process controls, such that designs can be printed in areas as small as a contact lens. With these layouts in place, discrete components can be wirebonded on for a functional system. In addition, printed electronics provide a more sustainable alternative to the current printed circuit board fabrication process. The byproducts that result from the fabrication process, such as pollution and air emissions, are harmful to the health of the surrounding environment. Printed electronics promote a more sustainable process as it is an additive process - the conductive ink is deposited directly on top of the substrate thereby eliminating the use of harmful etchants.

Printed electronics is emerging as a major specialization in the Graphics Communications department here at Cal Poly. Currently, the MS program in printed electronics and functional imaging is pending approval by the CSU chancellor. This project will help promote this new area in graphic communications and connect engineering students with the GRC department where their engineering knowledge will greatly contribute to future research projects.

The interdisciplinary nature of this project required the expertise of multiple fields and would not have been possible with only electrical engineers. Paul Heckler (BMED) assisted us in researching biocompatible materials for the substrate and the dielectric materials. His role was vital in determining viable substrates that are harmless to the eye. In addition, he helped us with the encapsulation process to ensure proper isolation between electrical components and the eye. Philip Azar (BMED) characterized the operational safety of the contact lens. His roles included modeling heat transfer of the contact lens substrate in COMSOL as well as performed mechanical strength tests. Alex Do (EE) aided us in the antenna's design. Errol Leon's (EE) helped us implement the thin film battery in our design. Dr. Keif's (GrC) aid in printing

electronics has been invaluable with our previous attempt at this device. In a previous project, he provided the material for the clear PET substrate and the silver ink for the trace. In addition, he gave us access to his screen-printing press. Dr. Keif has agreed to continue providing his guidance and assistance in the field of printed electronics. Dr. Tina Smilkstein's guidance in IC design made it possible for me to successfully send a design out to MOSIS for fabrication.

In addition to being the main electrical engineer, I also had to fulfill the role of a system engineering lead because this project had many engineers that spanned multiple majors. One hour long Bi-weekly integration meetings were essential in helping everyone stay on track. We used this time to cover tasks that were completed, their results, and next steps that needs to be completed. Occasionally, we would have working meetings. Working meetings took up larger time slots but were not regular meetings. Their purpose was to get members together whenever a teammate encountered a problem that they needed assistance on. This was a more informal type of meeting where attendance was not required and we often met in a lab. These meetings were the most beneficial to me because it helped me learn the technical knowledge that did not pertain to electrical engineering. I was able to get hands-on experience with tasks such as screen printing, working on CAD models, and helping out Errol in the Microfabrication lab.

This thesis encompasses the total UV sensing and notification system design. Chapter 1 provides an overview of the entire system describing the functionality of its subcomponents. Chapter 2 details the design and testing of the individual electrical components such as the external UV sensor, antenna, and custom IC. After all the components are individually tested, they have to be integrated into a complete system. Chapter 3 discusses the assembly process and the setbacks encountered during this project. Chapter 4 discusses the encapsulation process as well as curving the lens. Lastly, chapter 5 presents the conclusions.

SYSTEM ARCHITECTURE

The main work in this thesis involved powering the contact lens and activating a display when triggered off a wireless signal. A UV warning application was selected in order to test the power management system and display but could be used with any type of sensor as long as it provides a signal over the required threshold. Fig. 2.1 shows the overall system of the active contact lens.
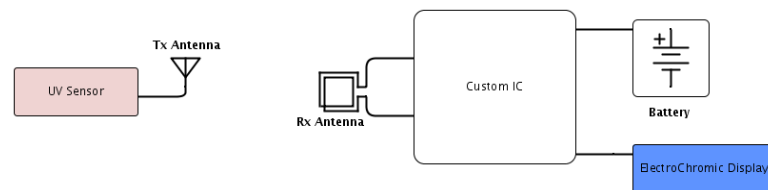
Figure 2.1: Active Contact Lens System Diagram

UV threshold detection will be handled in the external sensor circuit. The benefits of an external sensor over an integrated one include extending the utility of the contact lens by allowing the option to implement other types of sensors and reducing the area required for the circuitry on the lens itself. The possibility of a modular system is the motivation for having the sensor external to the contact lens. The UV sensor can be easily swapped out to situate another type of sensor depending on the needs of the work environment. For example, a person working in a oil refinery may need to be wary of harmful fumes while on the other hand, a laboratory worker may be concerned with exposure to certain radiation. A modular design for this system will allow the contact lens to function as an indicator in both those scenarios - the only requirement is that different sensors will need to be used.

Usable area for circuitry is very limited for a contact lens. Having components placed side by side may cause areas that overlap with the pupil, especially with the utilization of the thin film battery. Therefore, the approach taken in this thesis was to stack components on top of each other. This strategy increases of the overall thickness of the lens which compromises the comfortability of the contact lens. In addition, a contact lens that is too thick may shift around

when the user blinks. However, a thicker contact lens may still be more comfortable as they can fit the eye's curvature better than one that has components laid side-by-side.

The external sensor will transmit a 2.4GHz signal out from the antenna where it will be picked up by the printed receive antenna located on the contact lens. The printed antenna serves two purposes - it receives the 2.4GHz signal and acts as an inductive charging coil operating at 13.56 MHz. The antenna's outer diameter must under 1.5cm to fit the size of a contact lens and larger than 8mm for the inner diameter to avoid obstructing the pupil as shown in fig. 2.2. The antenna needs to be efficient enough to allow the IC on the contact lens to detect a signal at a distance of 32cm.
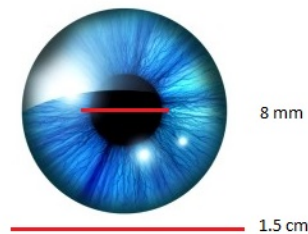
Figure 2.2: Eye Dimensions

The next stage of the system is the integrated circuit. The IC is fabricated by an external foundry using the On Semiconductor CMOS C5 0.6μm process. The custom IC serves two purposes: 1) The chip manages the battery power by handling inductive charging and protects the battery via low voltage cutoff and 2) it drives the display once the signal is received by the antenna. Fig. 2.3 shows the basic functionality of the IC.
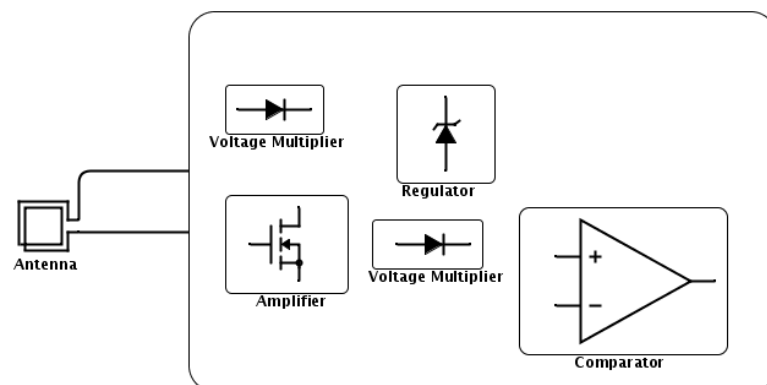
Figure 2.3: IC Block Diagram

The 13.56MHz charging signal is fed straight into a 3 stage voltage multiplier for rectification and DC voltage boosting. The DC voltage enters the voltage regulator which clamps it to 4.1V in order to meet the specified recharging voltage of the thin film battery. The 2.4GHz signal from the UV sensor, on the other hand, first becomes amplified in order to increase the range of operation. The amplified signal then goes through a 3-stage voltage multiplier to further bump up the signal level. Lastly, the comparator takes the DC voltage and compares it to an internal voltage reference. The IC drives the electrochromic (EC) display once the rectified voltage exceeds the internal reference level of 1V.

We chose a single pixel electrochromic display as the display technology due to it's low current consumption and optical properties. Unlike an LED where a constant current drive is necessary for illumination, the electrochromic ink acts similar to a capacitor where it becomes an open circuit during transient state and lowering the draw. When a voltage is applied across the ink, it turns from clear to a transparent blue while the illumination of an LED may be distracting to the user. Thus, the electrochromic ink is a novel way of implementing a display that does not impede on the user's vision.

An addition of an onboard power source differentiates this design from ones in previous works. The active contact lens implements a Cymbet CBC005 5 μAh thin film battery from the manufacturer Cymbet. Its size, rechargeability, and biocompatibility makes it a viable candidate for our design. The battery is small - the bare die chip only measures to be 1.7mm by 2.25mm and has a thickness of 200 microns. Its small footprint allows it to sit on the edge of the contact lens out of view of the user's vision. The battery has a simple recharging mechanism. All that is needed is a 4.1V constant voltage applied across its terminal and does not require a current limiting resistor as the internal resistance of the battery is sufficient. Lastly, in vitro testing of the battery showed no signs of cytotoxicity [4].

The printed elements of the system include the receive antenna and the electrochromic display while the battery and IC are discrete attached components. Fig. 2.4 below shows the stack up of the active contact lens.
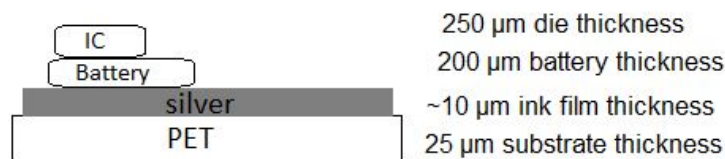
Figure 2.4: Stack Up of Components on Contact Lens

The substrate used for printing is a 25 μm PET film as PET is a standard in screen printing. However, PET is categorized as an eye irritant. A PDMS encapsulation process is introduced at the end of fabrication to ensure biocompatiblity of the device. PDMS was a foundational substrate during the early iterations of soft contact lens development. The flexible polymer allows us to mold the substrate to fit the curvature of the eye. In addition, the softness of PDMS compared to PET enhances user comfortability during use.

2.1 Biocompatibility

In order for our device to function as a contact lens, the material must be biologically suitable for our application. The material must not harm the body and vice-versa [5]. This analysis can be performed by conducting tests and studying the material's effects on cells, living systems, and live animals. Results from these tests are analyzed and reactions such as the amount of inflammation, toxicity, and rejection are all noted. The biomedical industry has already characterized and documented the biocompability of many materials, i.e. Material Safety Data Sheets. However, much of this information only applies to generalized effects and may lack data for a specific region of interest such as the surface of the eye. This limits the selection of suitable materials if we only look for materials that have already been characterized for the eye itself. Thus, performing studies with resources that are currently available is difficult and we had to determine the device's biocompability by relying on available data pertaining to more general biological reactions of the materials.

Designing for biocompatibility is one of the more difficult tasks in this project, and on-going research should be continued to improve on current materials. Both PET and PDMS are characterized as relatively biocompatible. However, PET may cause eye irritation as it is a not a

soft substrate. We decided to incorporate PDMS into our contact lens as it is soft, transparent, and utilized in many modern contact lenses. If this device was visioned for actual market release, the usage of PDMS would greatly strengthen the pursuit of 510(k) clearance with the FDA. The analysis of these properties on the fabricated lens is detailed in Chapter 5.

CHAPTER 3
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ELECTRICAL DESIGN
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The purpose of the contact lens is to act as a wirelessly triggered display for the user. The lens's

functionality relies on 3 main components onboard the lens: a printed antenna for signal

reception, integrated circuit for display drive, and a battery as the power source. While the

contact lens was the main focus of this project, a test system utilizing an external UV sensor was

implemented to demonstrate the intended use of the lens. This chapter lays out the design of

those 3 individual components and discusses experimental results.

 3.1 UV sensor

3.1.1 Design

An external circuit handles detection of ultraviolet energy. This external system consists of a

sensor and wireless transmission circuitry which signifies the user during a trigger event. We

will refer to the UV index (UVI) to determine the threshold of the trigger event. The World

Health Organization recommends the use of sun protection at an index level of 3 [6] – this

corresponds to $75mW/m^2$ of radiation. When the sensor detects $75mW/m^2$ of radiation, it will

communicate to the contact lens by activating the VCO and transmitting the 2.4GHz signal. The

system block diagram is shown in fig. 3.1 below.

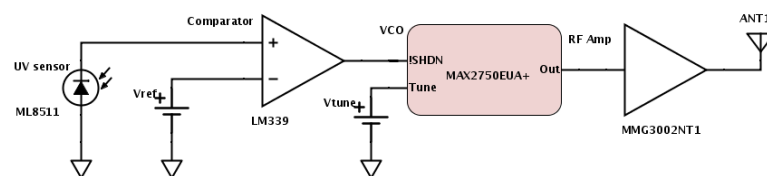**Figure 3.1:** External UV Sensor System Diagram

We used the ML8511 UV sensor by Rohm Semiconductor because of its simplicity. The sensor

outputs a voltage ranging from 1V to 2.2V. The output voltage of the ML5811 corresponds to

the sum of the UVA and UVB energies. Rohm Semiconductor previously performed field

testing in Santa Clara, CA, and the resulting equation was determined to approximate the UVI

with the output voltage with an UVI error $+\backslash-$.

$$UVI = 12.49Vout - 14.735 \quad (for \ Vout \geq 1.23V \ and \ UVI \geq 1) \tag{3.1}$$

Therefore, we would like the trigger event to occur when the UV sensor outputs about 1.4V. A basic non-inverting comparator design is implemented after the UV sensor that will output a high value when it detects 1.4V on the non-inverting input pin. A reference voltage of 1.3V on the inverting input pin is used to account for tolerances and this is realized using a resistor divider.
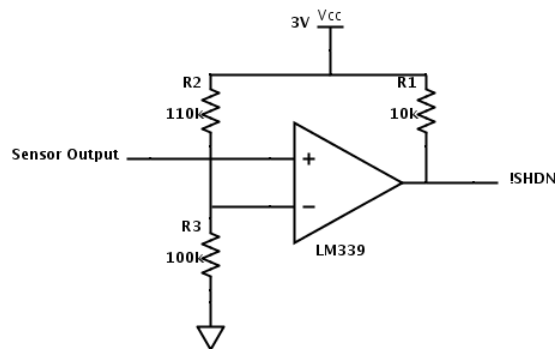
Figure 3.2: Comparator

The output of the comparator drives the $\overline{SHDN}$ input pin of the VCO. A high value on the $\overline{SHDN}$ pin puts the VCO out of low-power shutdown mode. Therefore, when $75mW/m^2$ of radiation hits the sensor, the output of the comparator swings high and the VCO outputs a -3dBm 2.4GHz signal. The last stage involves amplifying the output signal in order to fulfill the 32cm operational distance as stated in Chapter 2. We chose the MMG3002NT1 by Freescale Semiconductor because of its high 1dB compression point of 21dBm and the amplifier is already internally matched to 50Ω. The amplifier has a $|S_{21}|$ of 16dB at 2.4GHz as listed in the datasheet, which should boost the output signal of the VCO to 13dBm maximum.
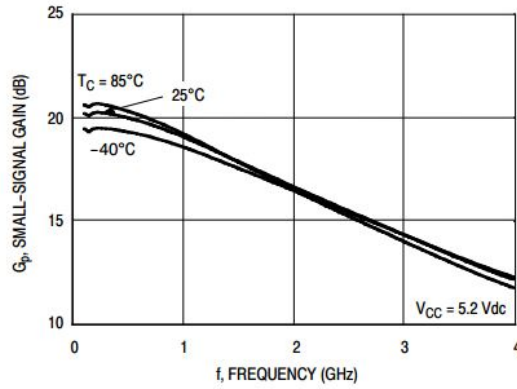
Figure 3.3: S21 of Amplifier vs. Frequency

3.1.2 Results

The first portion of the testing confirms the operation of the UV sensor. A multimeter was used to obtain the output voltage with the sensor in the sun.

Figure 3.4: UV Sensor Reading

Fig. 3.4 shows an output voltage of 1.4V while the sensor was placed in the sun. Using eq. 3.1, the UV sensor detects a UVI of 3 while online weather forecasts showed a UVI of 4 during the

time of the measurement. Therefore, this measurement confirms that the output of sensor is within the $+\backslash-$ 1 UVI error specification.

Next, the comparator operation was confirmed by obtaining the output when a ramp function was applied to the non-inverting input.
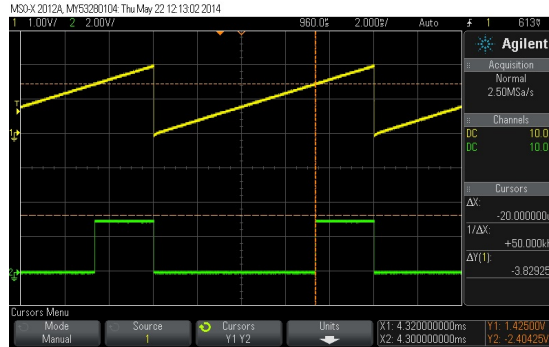
Figure 3.5: Oscilloscope Screenshot of Input Waveform and Output Waveform

The output of the comparator swings high right when the input sees 1.425V. Thus, the comparator will turn the VCO on when the sensor detects around 3.4 UVI which is higher than our original UVI level of 3 trigger point. Resistor tolerances caused the increased threshold point of the comparator. In addition, a trigger point error of 0.4 UVI can be negligible as the UVI calculated from eq. 3.1 produces an UVI error of $+\backslash-$ 1.

The output of the comparator turns on the VCO as stated in Chapter 2. The VCO we used was the MAX2750 which has a tunable frequency range of 2.4GHz to 2.5GHz even though operation only requires a single frequency. The desirable features of MAX2750 as opposed to using an oscillator are: 1) The VCO is already internally matched to 50Ω. 2) When $\overline{SHDN}$ is low, the VCO saves power by switching to shutdown mode which lowers it's current draw to 1μA. 3) A VCO can support a frequency modulation communication scheme during future reiterations of the device. The VCO was tested with the MMG3002NT1 RF amplifier in the output stage. The voltage for VTUNE must first be obtained such that the output of the VCO is 2.4GHz. A 0 to 1V ramp function was applied to the VTUNE pin in order to determine the VCO's exact response.
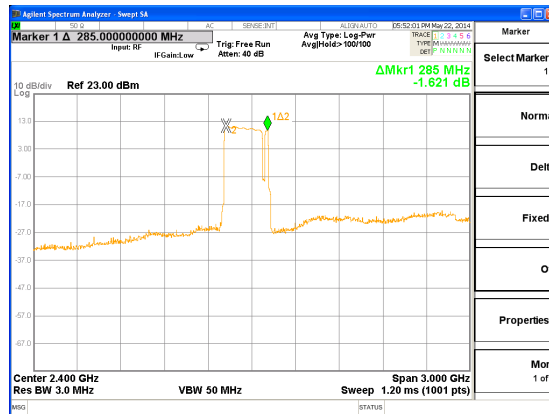
Figure 3.6: VCO output with Ramp Function Input

While the VCO has a flat output response throughout its frequency range, the output of RF amplifier has a decreasing response in relation to frequency which explains the negative slope in fig. 3.6. Since the VCO's output frequency is linearly proportional to VTUNE and the output frequency when 0V is applied to VTUNE is 22.5GHz, the voltage needed for 2.4GHz operation can be calculated to be 0.53V.
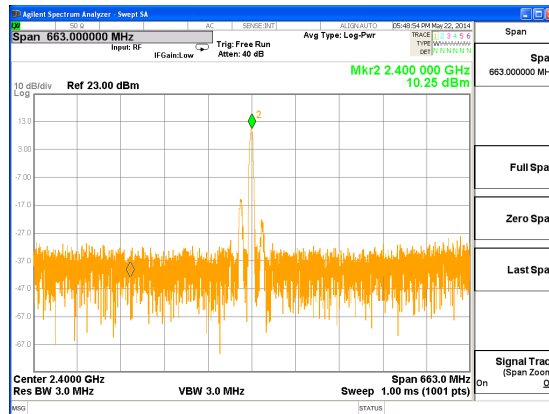
Figure 3.7: VCO output with 0.53V at VTUNE

Fig. 3.7 shows 2.4GHz operation when 0.53V was applied to Vtune. The spectrum analyzer shows a output power of 10.25dBm which is about 3dB lower than the estimated maximum of 13dBm. The power loss is because the estimated 13dBm maximum output is assuming a no load condition while the input to the spectrum analyzer is 50Ω. The input resistance of the spectrum analyzer creates a voltage divider with the 50Ω of the RF amplifier which drops the output of the RF amplifier by -6dB.Therefore, the expected output power should be roughly 7dBm which

is lower than the measured result in fig. 3.7. The 10dBm output power from the antenna should be high enough for the contact lens to detect the signal 32cm away.

3.2 Antenna

The main function of our contact lens is to warn the wearer when a signal caused by a trigger event is received by the contact lens from an external sensor – we implemented an external UV sensor as a test application. To support its functionality, the contact lens must be able to: receive incoming signals from the sensor, manage the battery's power, and activate a display as a warning stimulus. Reception of the wireless signal and inductive charging is handled by the printed antenna. There will be two modes of operation for the antenna; it will act as a receive antenna for a 2.4GHz wireless signal and perform as the tag coil for a 13.56MHz charging voltage. 2.4GHz was chosen to be the operating frequency because of its small wavelength which results in smaller antenna. A higher operating frequency such as 5GHz would allow the antenna size to decrease further. However, the higher frequencies experience higher attenuation when propagating in free space resulting in a shorter operating range. In addition, communicating at 5GHz is more difficult as that frequency band has higher noise than that of 2.4GHz. The size of the antenna was limited to a maximum diameter of 13mm to stay within the size of a contact lens and a minimum inner diameter of 6mm to avoid overlapping the pupil. Screen printing was selected as fabrication technique because of its support for flexible, transparent, and thin substrates.

3.2.1 Design

The antenna and battery charging coil were combined into a single device such that the coil will be inductive at our charging frequency of 13.54MHz and will be resonant at 2.4GHz. The magnetic field generated by a circular loop is give by [7]

$$B_Z = \frac{\mu_0 I N a^2}{2(a^2 + r^2)^{3/2}} \qquad (3.2)$$

where μ_0 is the permeability of free space, I is the current, N is the number of turns, a is the

radius of the loop, and r is the distance from the center of the loop. Fig. 3.8 below illustrates these parameters.
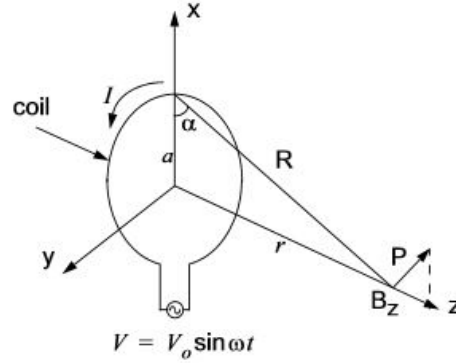
Figure 3.8: Magnetic Field Generated by Single Loop

Eq. 3.7 states that the magnetic field generated by the coil is increase by either having more turns or increasing loop area. We must also consider the efficiency of the antenna when receiving a 2.4GHz signal which is determined by its radiation resistance and Ohmic resistance. The radiation resistance Rr of an electrically small antenna is [8]

$$R_r = 20(\beta^2 NS)^2 \approx 31{,}200(\frac{NS}{\lambda^2})^2 \Omega \tag{3.3}$$

where N is the number of turns, S is the loop area, and λ is the wavelength. The ohmic resistance of a loop constructed with wire s given by [8]

$$R_W = N^2 \frac{2\pi b}{wt} Rs \tag{3.4}$$

where b is the mean loop radius, w is the trace width, and t is the ink film thickness. Rs is the

surface resistance given by

$$R_S = \sqrt{\frac{\omega\mu}{2\sigma}} \tag{3.5}$$

where σ is the conductivity of the silver conductive paste. The antenna efficiency is give by

$$e_r = \frac{R_r}{R_A} \tag{3.6}$$

where R_A is the sum of R_W and R_r. Having a large radiation resistance will improve the efficiency of our antenna. Therefore, increasing inductance by having a larger inner diameter is a better choice than having more turns because a larger diameter increase the area of the loop and consequently its radiation resistance. Our main focus was to optimize the dimensions of the coil such that it has a purely real impedance of 50Ω (input impedance of the chip) as we would like to avoid using lumped passive components for impedance matching. We expect a very low efficiency for our antenna because of its inherent design. First, the loop encompasses a small area which results in a low radiation resistance. Second, the silver conductive paste used for the traces has a high resistivity of $2.33\text{x}10^6$ S/m resulting in high ohmic losses. Antenna parameters such as trace width and number of turns were determined using simulations done on Agilent's Advance Design System (ADS). The table below shows the antenna design optimized for size, efficiency, and S11 reflection coefficient.

Table 3.1: Printed Coil Parameters

Outer Diameter (cm)	1.3
Inner Diameter(cm)	8
Trace Width(μm)	250
Trace Thickness (μm)	250
Number of Turns	4

(a) Simulated Coil

(b) S11 of Coil

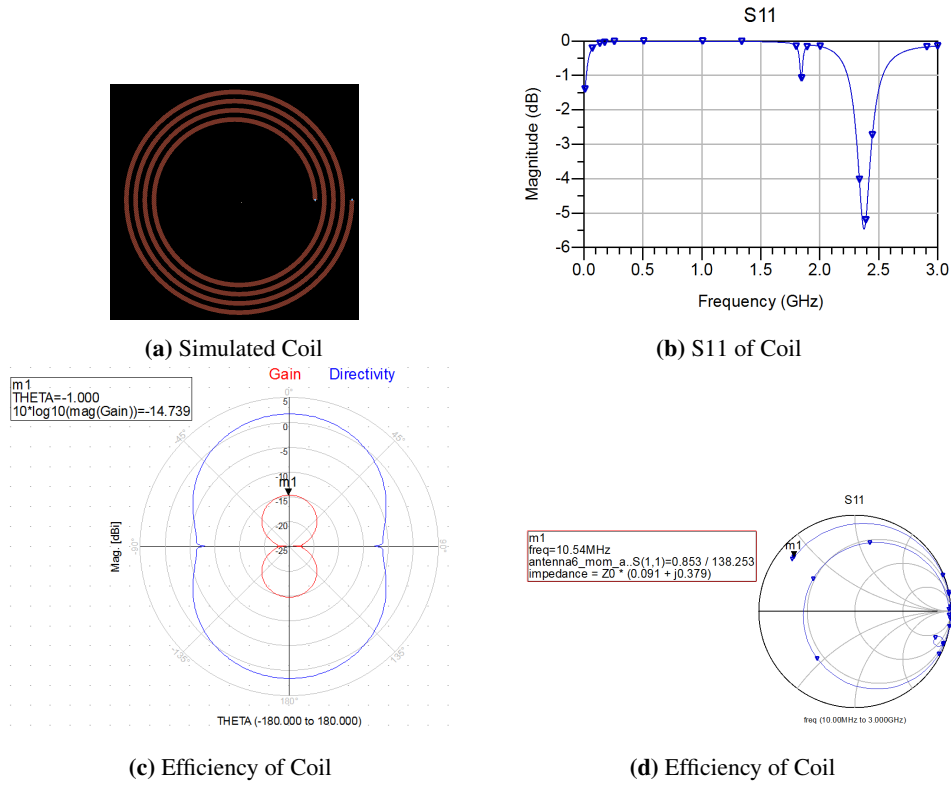**(c)** Efficiency of Coil

(d) Efficiency of Coil

Figure 3.9: Response of Coil Design

Fig. 3.9(a) shows the antenna layout in ADS. Fig. 3.9(b) shows the simulated reflection coefficient at 2.375GHz. Fig. 3.9(c) shows the simulated gain of the antenna. Fig. 3.9(d) shows a coil inductance of 286.6nH. As expected, this antenna design has a low gain (-14.74 dB) because the extra turns needed to produce inductance provides a high series resistance.

An alternative antenna design with higher gain was needed if we wanted to achieve detection at a distance of 32cm. The motivation for the final design of the antenna was the inverted F antenna (IFA). The advantages of the IFA for this design is its large ground plane and that its operating frequency is only determined by the length of a single stub. Fig. 3.10 below shows a 2.4GHz (for signal detection) IFA with a 31.25mm stub length and a large ground plane.

Figure 3.10: Inverted F Antenna

(a) S11 of IFA
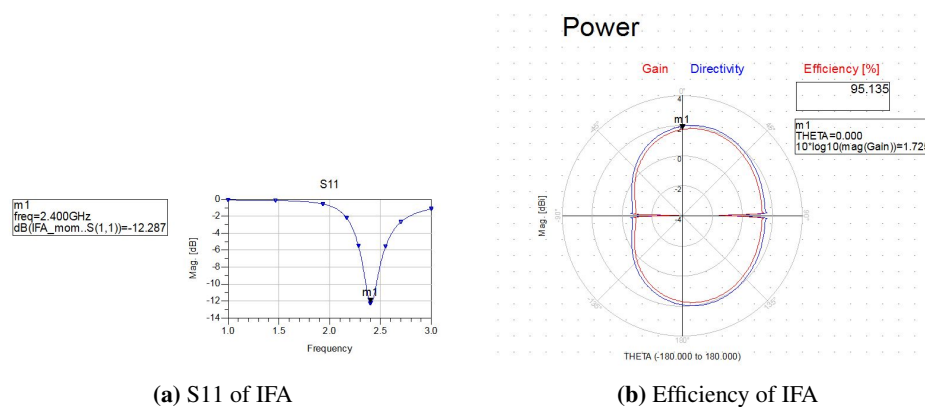

(b) Efficiency of IFA

Figure 3.11: Response of 2.4GHz IFA

Fig. 3.11(a) confirms the proper 2.4GHz operation of the IFA with a reflection coefficient of -12.287dB. The large ground plane allows the IFA to achieve an efficiency of 95%. Ideally, the height of the ground plane and the length of the stub should be quarter-wavelength - in the case of fig. 3.11, those dimensions were both 31.25mm. When adding these lengths together, the antenna has a similar structure to that of a half-wave dipole antenna. Unlike the dipole, the size of the IFA's ground plane does not affect the resonant frequency of the antenna. Therefore, the ground plane could be altered to fit a desired shape (i.e. cut a hole in it to let the eye see through). However, lower efficiencies and smaller bandwidths would result in a ground plane distortion.

In order to fit the IFA into a contact lens, its shape was adjusted such that it was circular and would allow the eye to see through. The first requirement was achieved by changing the ground plane to be circular instead of a square. The stub was then curved and wrapped around the ground plane while keeping the same length. To address the visibility issue, a hole was created in the ground plane to situate the eye. Fig. 3.12 shows the resulting antenna structure.
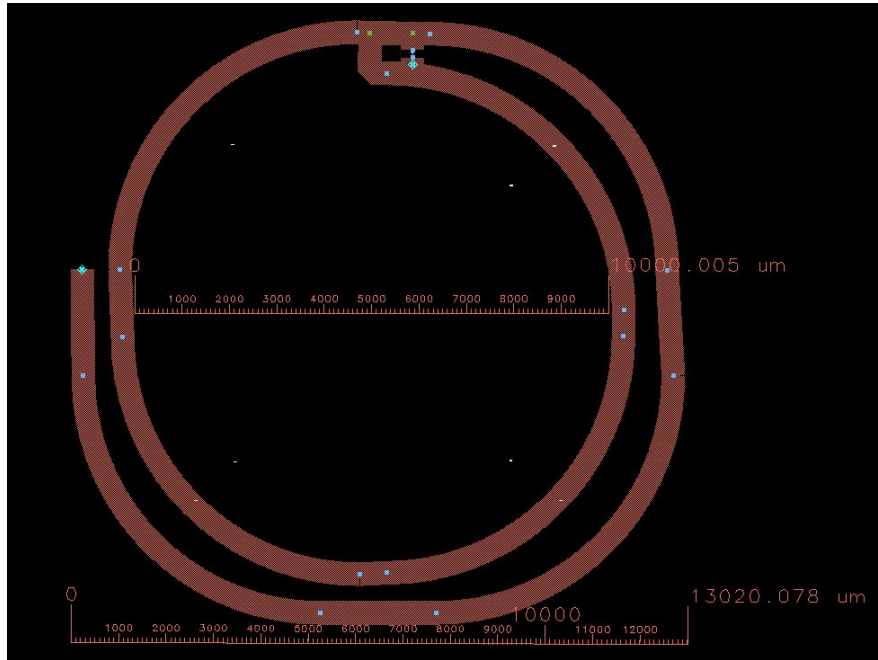

Figure 3.12: Curved IFA with Opened Ground Plane (top view)

The IFA was curved in such a way to fit within the 1.3cm maximum outer diameter while allowing plenty of room inside the ground plane for the iris.
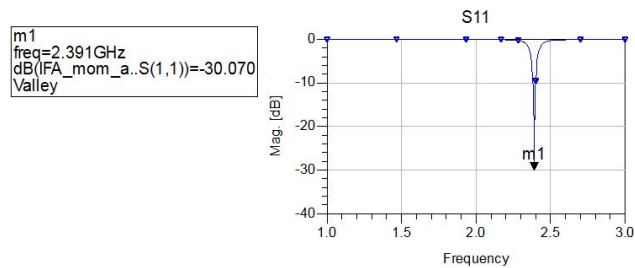

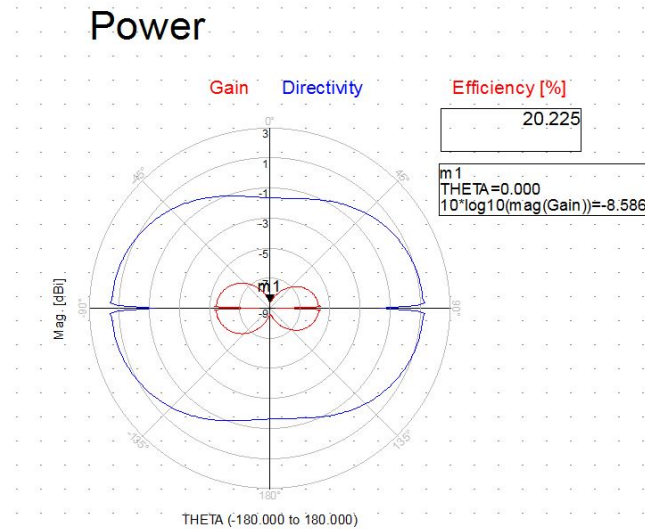**Figure 3.13:** S11 of Curved IFA Design

Figure 3.14: Efficiency of Curved IFA Design

Fig. 3.13 shows a small shift in the antennas resonant frequency and a lower bandwidth while the efficiency of the antenna dropped to 20% as shown in fig. 3.14. These changes the antenna's characteristics were caused by the change from a ground plane to a ground loop [9]. The lowered bandwidth was caused by added parasitic capacitance and inductance of the loop with the curved stub and the lowered efficiency was caused by higher ohmic losses due to a smaller ground plane. With a large open area present inside the ground plane of the IFA, a coil was inserted to be used for inductive charging.

Inductive charging is accomplished by applying a time-varying current through a coil. The AC current generates a time-varying magnetic field and that magnetic field induces an AC voltage at a receive coil. The amplitude of the induced voltage at the receive coil is proportional to the magnetic field created by the transmit coil. Therefore, a large magnetic field at the transmit side is desirable and can be calculated using the equation[7]:

$$B_Z = \frac{\mu_0 I N a^2}{2(a^2 + r^2)^{3/2}} \tag{3.7}$$

where μ_0 is the permeability of free space, I is the current, N is the number of turns, a is the radius of the loop, and r is the distance from the center of the loop. Eq. 3.7 states that the

magnetic field generated by the coil is increased by either having more turns or increasing the loop area. The inner diameter of the coil is limited by the average pupil diameter which is about 7mm in low light conditions. The smallest feature size achievable by the screen printing process on campus are 100μm trace widths as the mesh sizes of the screens on campus are too large to achieve thinner traces. Additionally, the outer diameter of the coil should not completely occupy the 10mm diameter available inside the ground loop as the small gap between the ground loop and the coil may cause shorts in the printing process. Therefore, the designed coil has an inner diameter of 7mm and an outer diameter of 9.6mm. These dimensions allow a maximum number of 6 turns with 100μm trace widths and spacing and fig. 3.15 shows the final antenna design.

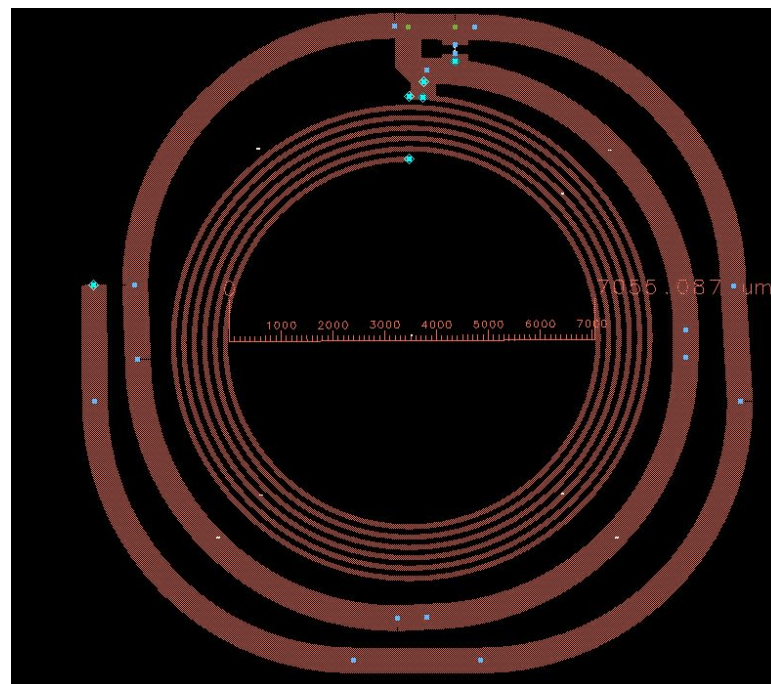**Figure 3.15:** Final Antenna Design

Fig. 3.16 shows the impedance of the coil. The coil was simulated using a 15 Ω/sq/mil sheet resistivity for the conductor to account for the resistance of the conductive ink used for screen printing.

Figure 3.16: Smith Chart of Coil
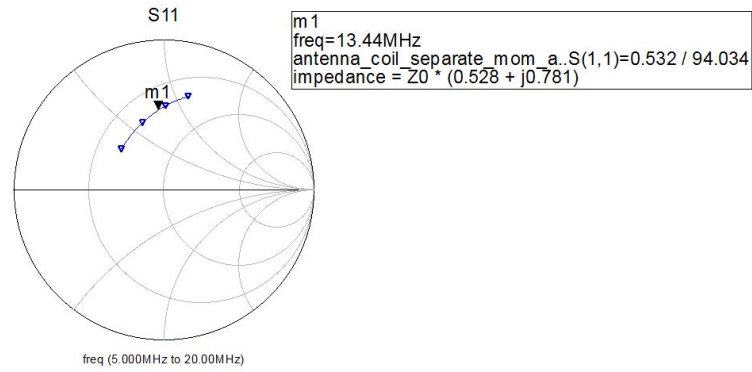
Simulations produce a resistance of 26.4Ω and inductance of 0.46μH in a 50Ω system resulting in a Q factor of 1.479. If a 10Vp sinusoid is applied to the coil (the transmit coil will be the same as the receive coil), the resulting 100mAp AC current produces a flux density of 107.66 $\frac{\mu Wb}{m^2}$ when calculated using eq. 3.7. The induced voltage at the receive coil can be calculated using [7]:

$$V_0 = 2\pi f NSQB_0 cos(\alpha) \tag{3.8}$$

where f is the 13.56MHz operating frequency, S is the area of the coil, Q is the Q-factor, B_0 is the arriving magnetic field, and α is an arrival angle of $90°$. Therefore, a 10V peak 13.56MHz sinusoid at the transmit coil should produce a peak voltage of 3.11V at the receive coil when the two coils are placed directly on top of each other (r=0).

Fig. 3.17 shows a decrease about 0.8 dB in gain and 3% in efficiency with the coil inserted. The added coil increased the resistivity of the ground plane resulting in a higher ohmic loss.
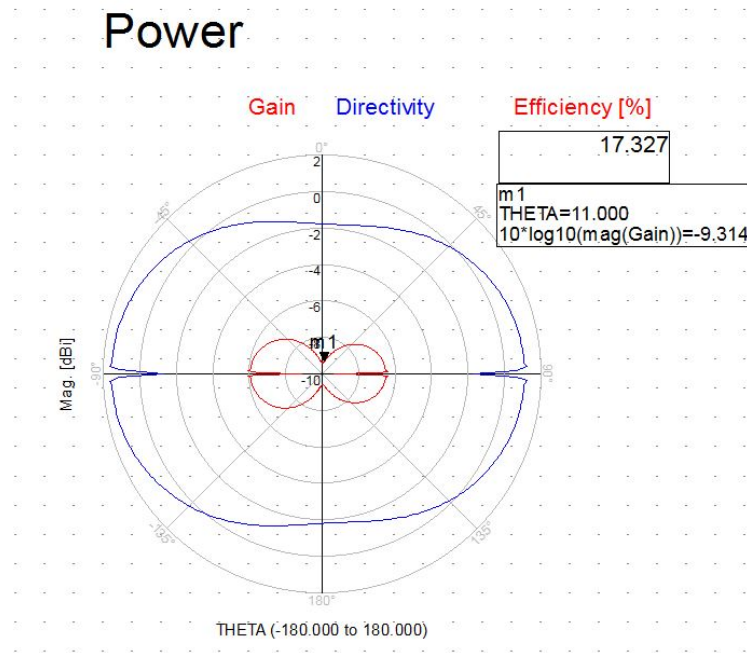
Figure 3.17: Gain of IFA Design

3.2.2 Fabrication

While the antenna was designed such that it was small enough to fit on a contact lens, a large portion of this work consisted of determining a suitable fabrication process. With the help of Dr. Malcolm Keif and the Graphic Communications (GRC) department, the technique of screen printing was utilized to fabricate the antenna. Screen printing allows us to rapidly prototype, test, and make necessary revisions all while supporting the use of transparent and flexible substrates. Therefore, we could print both antenna designs for testing with no extra work required. Screen printing is also an additive process eliminating the need for harmful etchants during fabrication. Screen printing works by having a screen where the design is patterned as gaps allowing ink to be pushed through the screen onto a substrate.
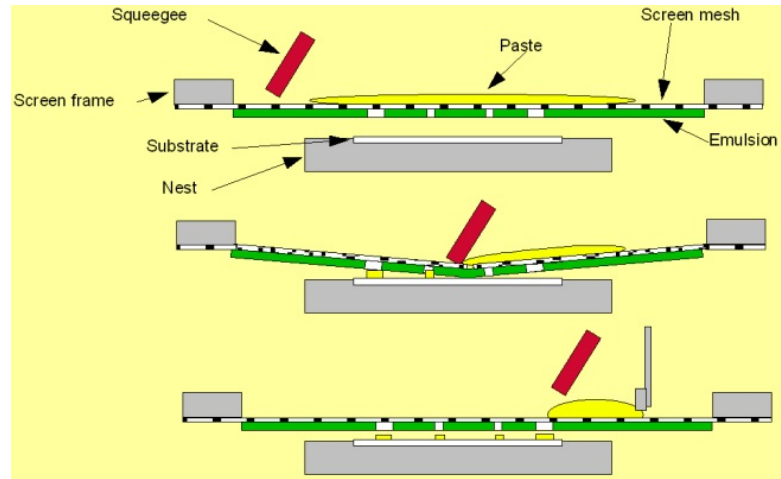
Figure 3.18: Screen Printing Illustration

While screen printing has been used to fabricated printed circuit boards on campus in the past, their features sizes were not as small as the ones required by our antenna. Therefore, strict process controls had to be followed. Screen printing consists of 3 major steps:

1. Create mask

2. Expose design onto screen

3. Print

3.2.2.1 Mask Creation

First, the design mask was created. The mask acts as a film positive that allows the design to be transferred on a mesh screen. It starts off as a sheet of black carbon as shown in fig. 3.19.

Figure 3.19: Roll of Carbon Sheets

The carbon sheet was then cut and fed into an Esko CDI where the imager's fiber laser removes excess carbon leaving just the design.

Figure 3.20: Feeding Carbon Sheet into Esko CDI

Figure 3.21: Resulting Mask

Once the mask is made, the design must then be transferred onto a screen.
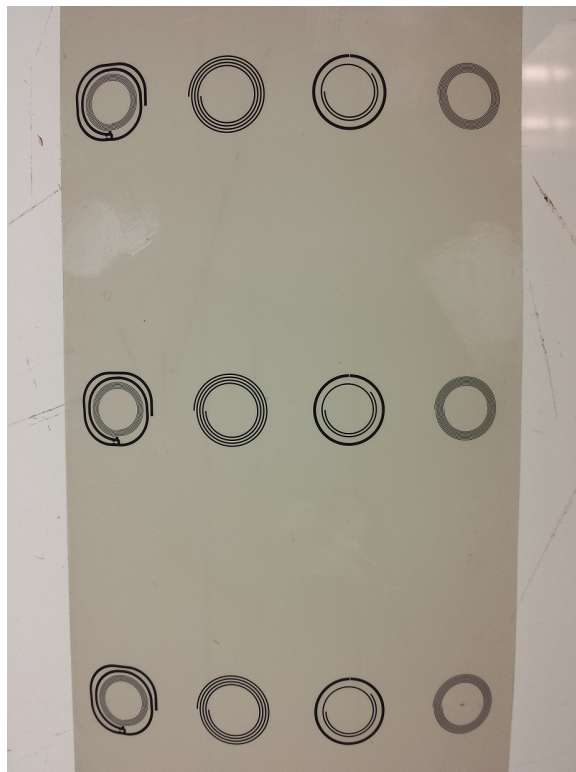
3.2.2.2 Screen Making

From fig. 3.18, the screen is the stencil that determines the ink pattern deposited on the substrate. It consists of hundreds of fine, intersecting polyester fibers stretched across a metal frame.
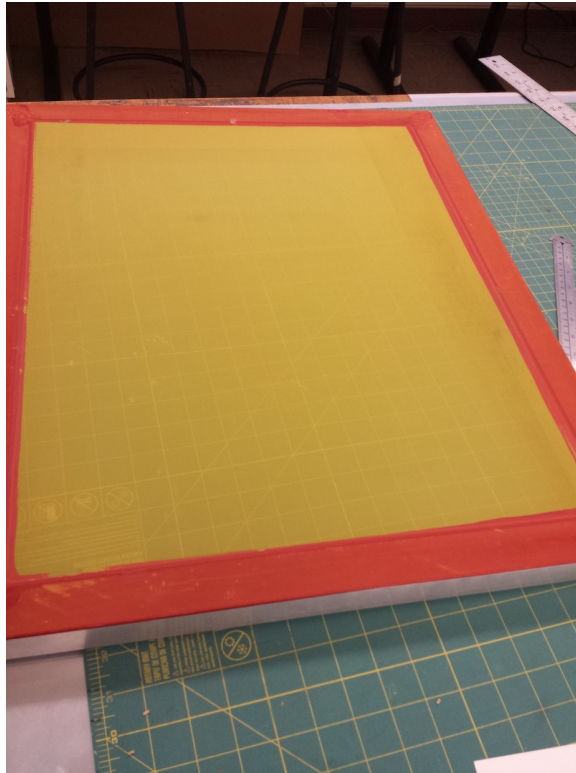
Figure 3.22: Screen

Image quality of the print is largely determined by the mesh number of the screen. The mesh number describes the number of fibers per linear inch. Thus, large mesh number means smaller threads which allows for finer details in the print. We used a 460 size mesh in order to flow ink into openings that are tens of microns wide. In order to create the stencil in mesh, emulsion was adhered to screen. The emulsion is UV-sensitive polymer such that exposed areas will harden. Therefore, the purpose of the mask is to block UV light which creates a negative stencil on the screen. We used a capillary film emulsion instead of regular liquid emulsion. Applying liquid emulsion requires us to manually coat the emulsion on the screen which causes variations in thickness. Capillary emulsion provides a more consistent ink film thickness as it is a sheet that

can just be laid on the screen.

Once the emulsion has been applied on the screen, the design was then transferred onto the emulsion to create the stencil. First, mask was laid on top of the emulsion.

Figure 3.23: Mask Laid On Top of Emulsion

The screen and the mask was then placed into a UV curing machine to expose the emulsion. The UV intensity was critical in preserving the 100μm trace widths: intensities that were not high enough would cause the features to blow out during the washing process and intensities that are too high causes the UV light to undercut the parts blocked by the mask resulting in thinner lines. After much trial and error, we determined that emulsion should be exposed with an intensity of 120LTU in order to preserve the fine features.

Figure 3.24: Screen in UV Curing Machine

Once the emulsion has been exposed, we gently wash out emulsion where the water removes the unexposed regions of the emulsion underneath the mask. We first apply a light spray on the screen and let it soak for a minute with the backlight off. Then, we turn on the backlight and lightly spray the areas that require additional washing.

Figure 3.25: Washing Screen

Figure 3.26: Blown Out Design
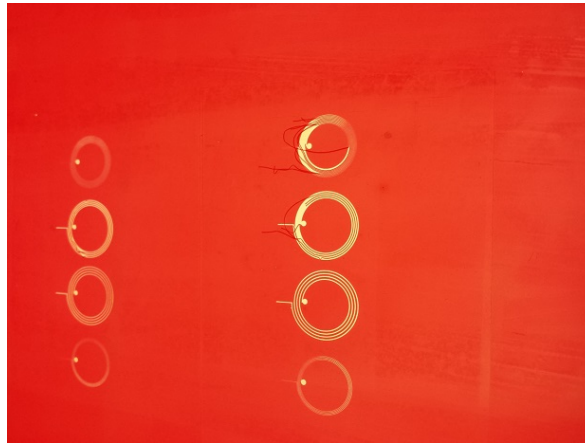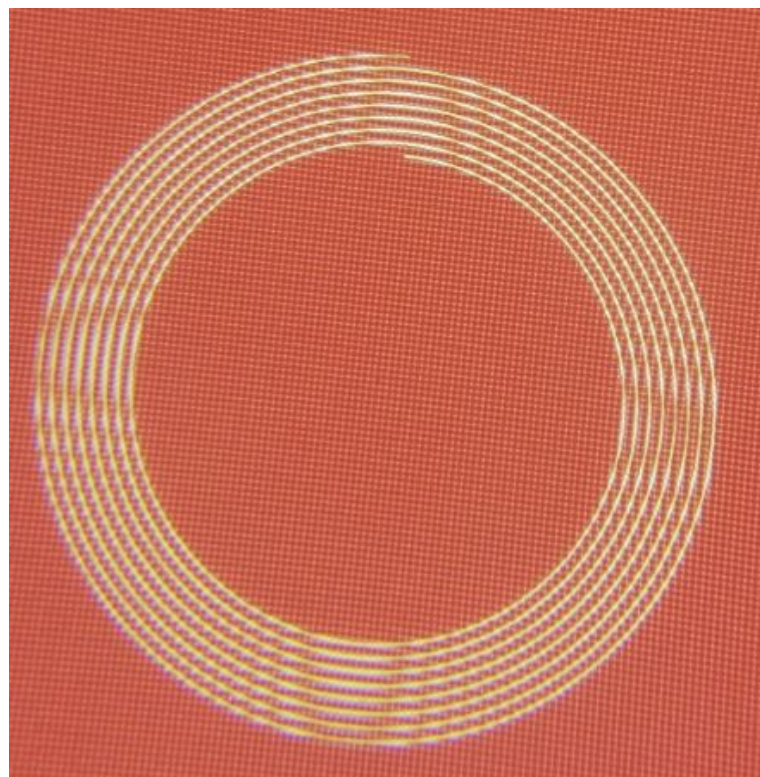

Figure 3.27: Undercutting

Fig. 3.26 shows a blown out design when the intensity was set to 90LTU. The areas between traces were not hardened completely and was washed out. In addition, improper emulsion adhesion may cause this issue too. If the emulsion was not applied with enough force on the screen, the emulsion may not adhere completely and tended to easily wash out. Fig. 3.27 shows

an example of overexposure at 140LTU. The test design was a coil with 100μm trace widths and spacing. An intensity level that is too high will cause the areas underneath the black areas of the mask to become partially exposed. Thus, the traces on the screen becomes thinner than traces on the mask resulting in thinner traces during the print. Fig. 3.28 shows the screen that has been exposed correctly using 120LTU. We see that the trace widths were slightly thinner than the spacings which indicates slight undercutting. However, this was unavoidable as preserving the feature sizes was more important than having thinner trace widths. Once the screen has been washed and dried, a second post-exposure at 120LTU was performed to harden the emulsion and increase durability.
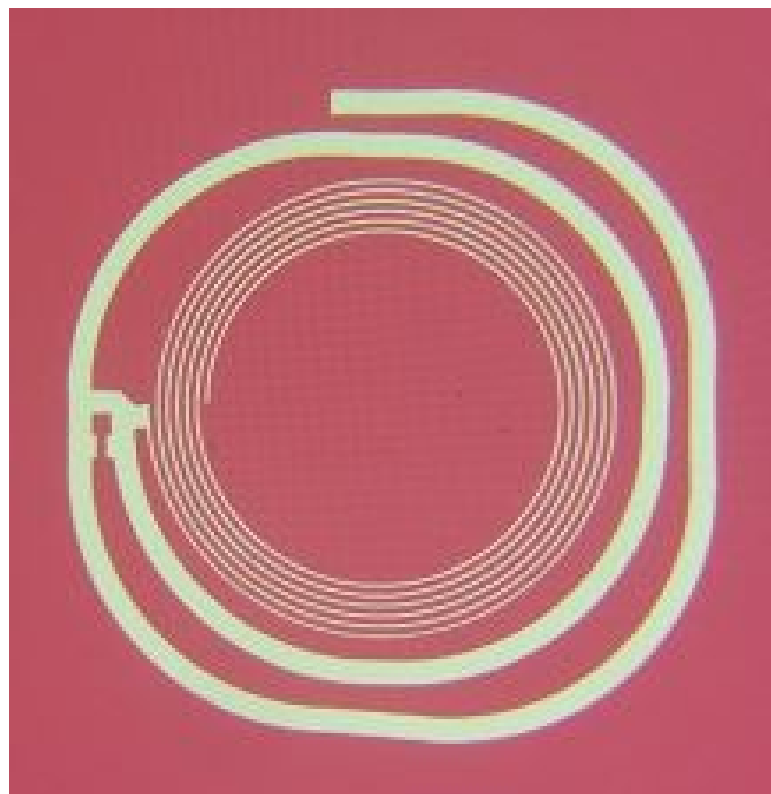

Figure 3.28: Resultant Stencil

3.2.2.3 Printing

With the screen finished, the next step was to print the design on the substrate. The substrate chosen was a 25μm Mylar PET film by DuPont. PET was chosen because it is a standard in printed electronics. The machine used to print the antenna was the ATMA AT-45FA Pneumatic

Screen Printer. The printing process is composed of two steps. First, the screen is flooded with ink. This step involves coating entire area with a film of ink without applying pressure. The purpose of the initial flooding stage is to present the design with an even layer of ink for a consistent deposition across the print.
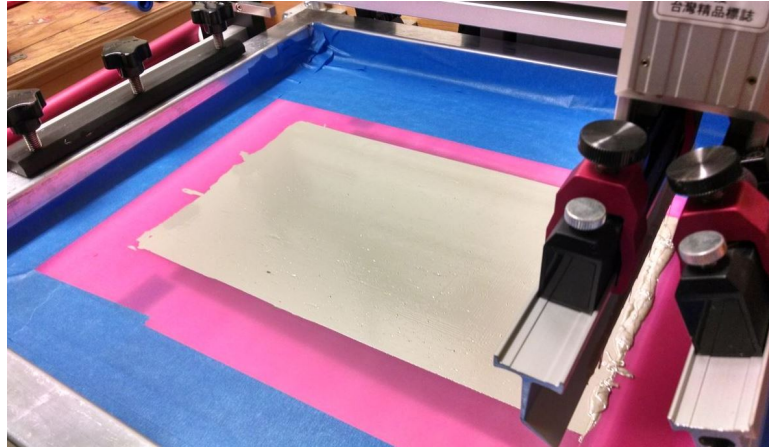
Figure 3.29: Flooding the Screen

Once the screen has been flooded, we apply the squeegee and push the ink onto the substrate going the opposite direction of the flooding step. Finally, the screen is re-flooded to prevent the ink from drying and clogging the mesh. Printing required many trial and error runs as adjustments to the squeegee level (how parallel the squeegee is in relation to the screen) and squeegee pressure were needed to prevent breaks in the coil.
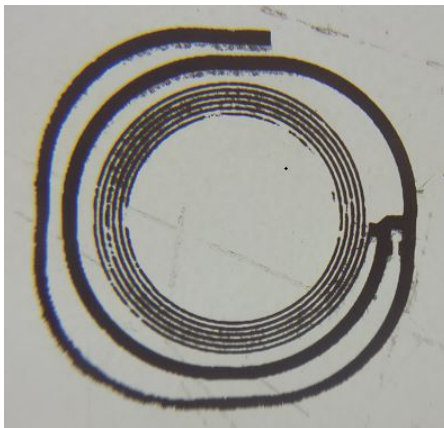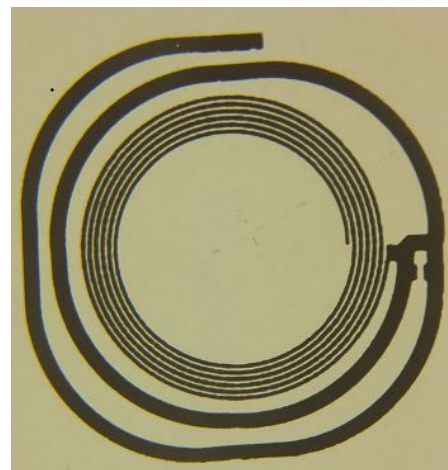
(a) Bad Print   **(b)** Good Print

Figure 3.30: Printed Results

Even though the screen in fig. 3.28 showed some undercutting, we do not see that effect in the final print. Fig. 3.31 shows that the traces were thicker than the spacings in between.
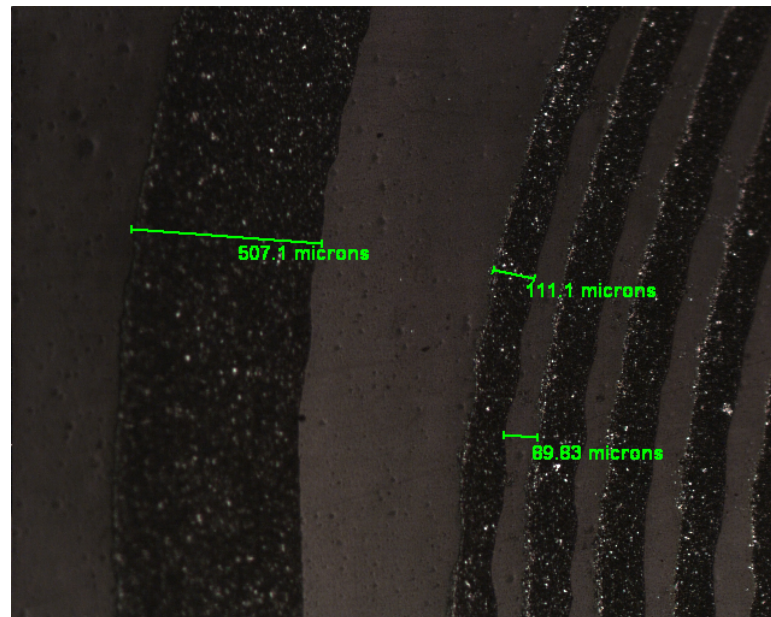
Figure 3.31: Microscope Image of Traces

3.2.3 Results

Fig. 3.32 below shows the reflection coefficient of the printed antennas. The frequency was shifted to 2.2GHz instead of the designed 2.4GHz. Additionally, the actual S_{11} was higher than simulated results by 4dB. These discrepancies may be caused by parasitic capacitances between the ink and PET substrate. In addition, cured ink may have been more resistive than anticipated in simulations.
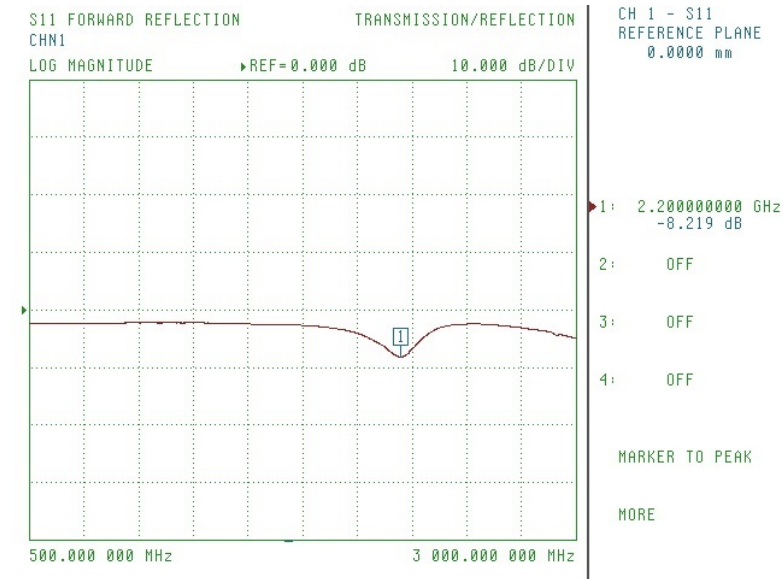
Figure 3.32: S11 of Printed IFA

Since the arm of the antenna determines its operating frequency (the length of the arm should be the wavelength of the antenna's operation), the lowered S_{11} frequency indicates that the length of the antenna was too long. Therefore, antenna was tuned by scraping off the ink at the tip of the stub while having it connected to a Vector Network Analyzer (VNA). The frequency shift was closely monitored as the stub was carefully shortened until it reach 2.4GHz as shown in fig. 3.33. Fig. 3.34 shows a reflection coefficient of -4.446 dB at 2.38GHz.
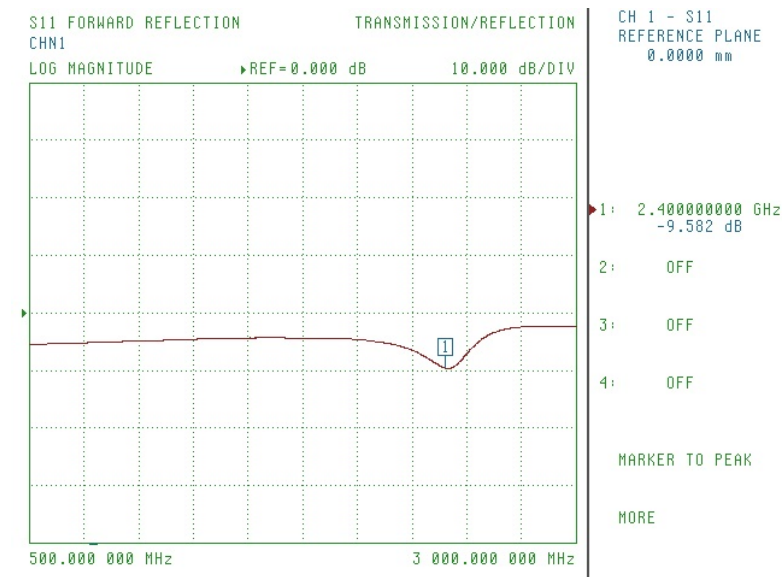
Figure 3.33: S11 of Printed IFA after Tuning
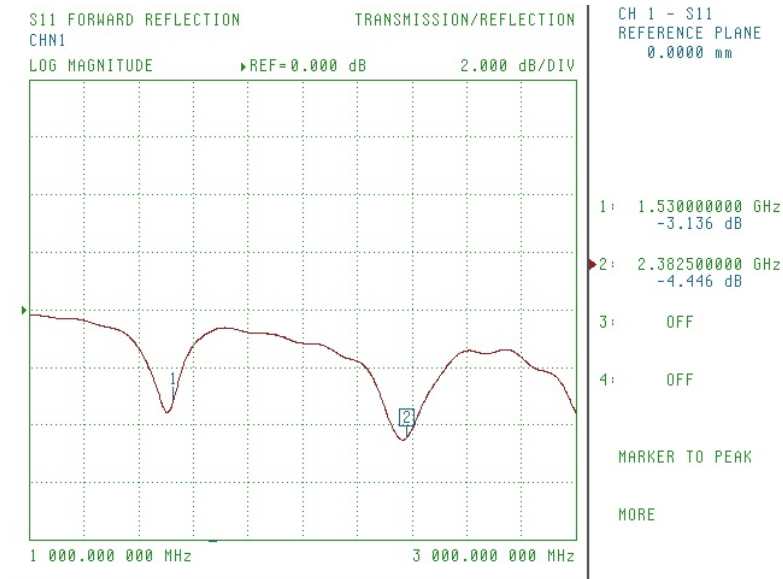
Figure 3.34: S11 of Printed Coil Design

The antenna gain was test by transmitting a 2.4GHz 10dBm signal using a 1.7dB gain antenna at a distance of 42 cm. Fig. 3.35 and 3.36 show the detected signal powers for the printed antennas.
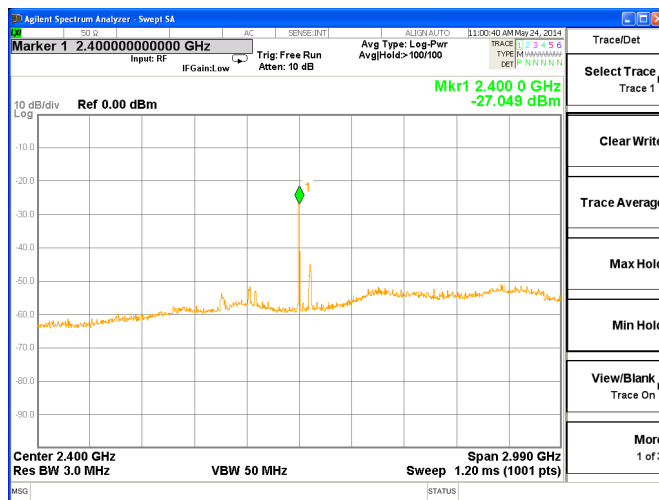
Figure 3.35: Recieved Signal Power at Spectrum Analyzer (IFA)
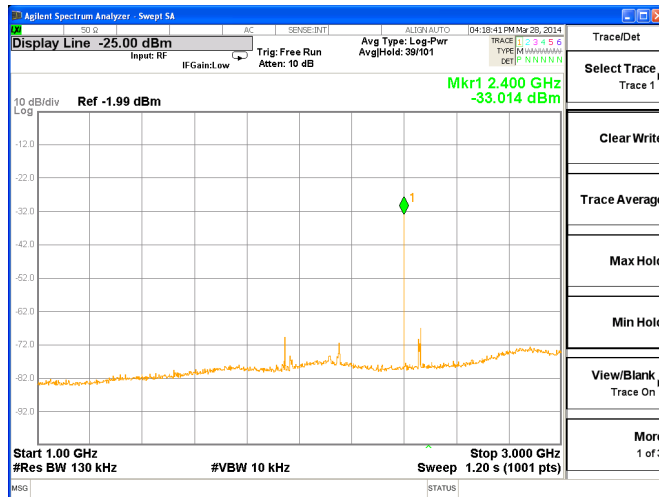
Figure 3.36: Received Signal Power at Spectrum Analyzer (Coil)

Friis transmission equation tells us that the power received is equal to the sum (in dB) of antenna gains and signal power subtracted from the path loss [8].

$$P_R(dBm) = P_T(dBm) + G_T(dB) + G_R(dB) - 20logR(km) - 20logf(MHz) - 32.44 \quad (3.9)$$

A distance of 42cm attenuates the signal by 32.7dB which means the signal right at the antenna has a power level of -21dBm or 7.95μW. |S$_{11}$| of -9.5dB means that 67% of the power is accepted by the antenna resulting in 6.7μW or -21.7dBm of accepted power. Therefore, the efficiency of the IFA can be calculated to be 33.5% resulting in a total antenna gain of -5.3dB which is 3.3dB higher than simulation. Similarly, the total gain of the printed coil design was calculated to be -13 dB. Fig. 3.37 and 3.38 shows an inductance of 273.4nH (Q factor of 0.269) and 268.2nH (Q factor of 0.98) for the IFA and Coil designs respectively. The trace resistances were higher than expected which explains the low Q factors.
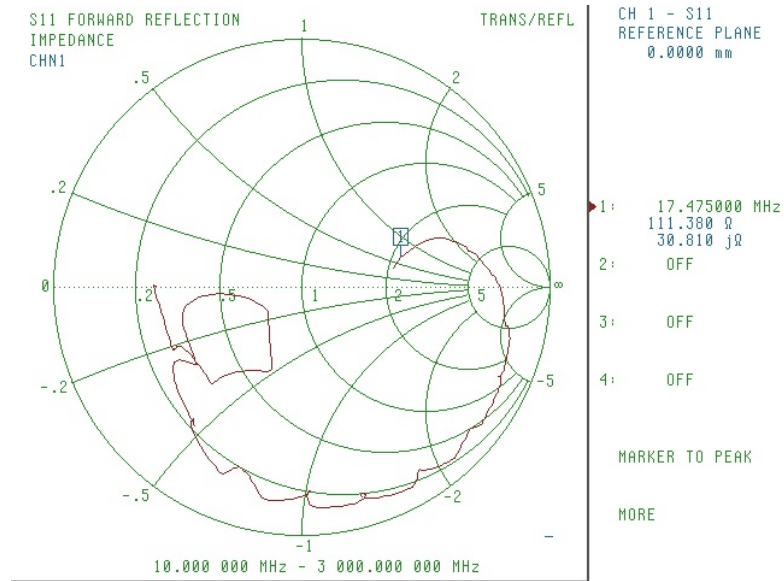
Figure 3.37: IFA Coil Inductance
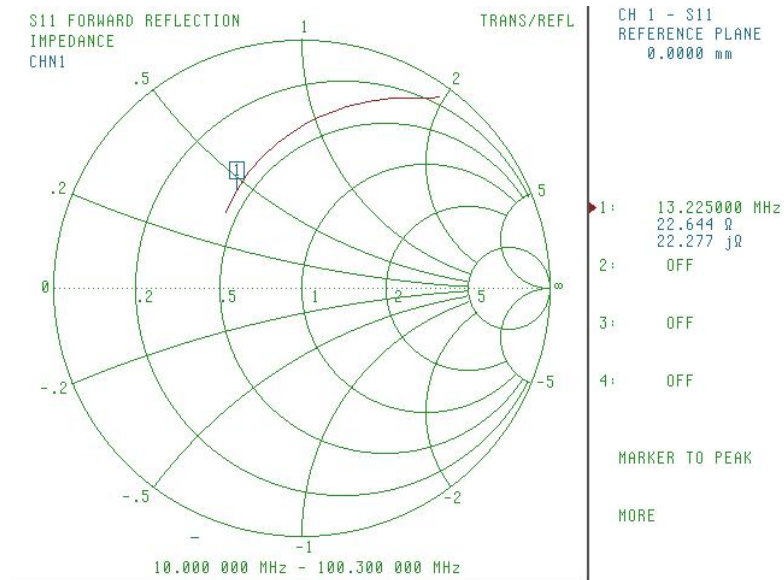
Figure 3.38: 250μm Coil Design Inductance

Unfortunately, we were not able to obtain the necessary 4V peak signal at the receive coil due to the high coil resistance from the thin traces. We had to opt back to the 250μm coil design. Fig. 3.39 shows a 4.7V peak signal at the receive end when a 10V peak, 20MHz signal was applied to the transmit coil.
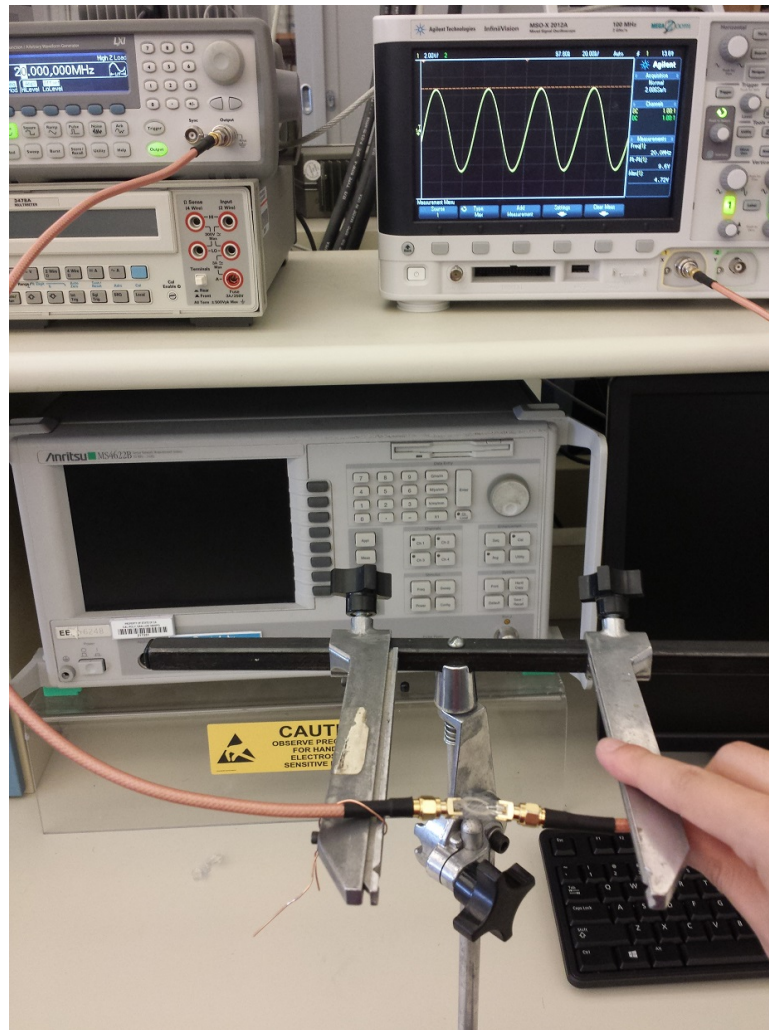
Figure 3.39: 250μm Coil Design Inductance

3.3 Electrochromic Display

The display technology chosen for our application was an electrochromic display (ECD). The ECD has several advantageous characteristics. First, it is screen printed so fabrication is not difficult. Second, the ECD is clear in its normal state. When 3V is applied, the ECD transitions into a transparent blue. The ECD is composed of two layers, electrode and electrolyte, as shown in fig. 3.40.
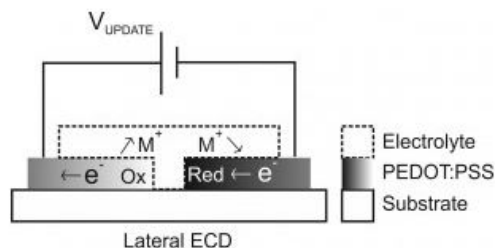
Figure 3.40: Electrochromic Display Stackup

The electrodes are made from an organic conductive polymer called PEDOT:PSS. This polymer acts as the electrochromic material as well as the electrical conductor. The electrolyte is then printed on top of the two electrodes, bridging them together. When a voltage is applied at the terminals, the potential causes a REDOX reaction to occur between the PEDOT:PSS and electrolyte; the transition from clear to blue occurs at the negative electrode where reduction occurs.

Since the ECD is a 2 layer configuration, it must be printed in 2 steps. First, we print the electrode layer. The conductive polymer used was the Clevios™ PEDOT:PSS by Heraeus. After the PEDOT:PSS was printed, it was cured in the oven at 80 degrees C for 10 minutes. Once cured, we printed the electrolyte layer. The electrolyte was created with the help of Errol Leon and consisted of 15 wt% of polymethyl methacrylate (PMMA) and 84.5 wt% of propylene carbonate are mixed with 0.5 wt% of $LiClO_4$. Fig. 3.41 and 3.42 shows the fabricated ECD in its off state and on state respectively.
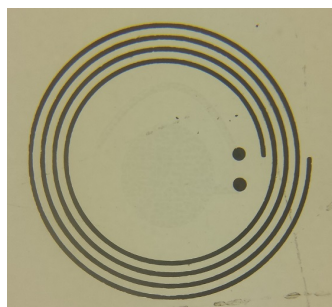
Figure 3.41: Electrochromic Display Off
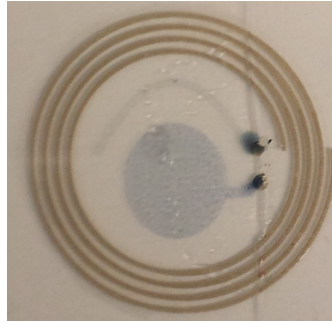
Figure 3.42: Electrochromic Display On With 3V Applied Across Electrodes

3.4 Integrated Circuit

3.4.1 Design

The main functionalities of the contact lens are handled by the custom designed integrated circuit. These functions include: 1) detect incoming signal from the external sensor circuit, 2) handle inductive recharging, 3) manage battery voltage level, and 4) drive the display. Additionally, the IC must have a total current draw of 5 μa in order to achieve an operation time of an hour running off the 5μAh battery. The IC was designed through Cadence Virtuoso and fabricated using the ON Semiconductor CMOS C5 0.6um process.

3.4.1.1 Voltage Reference

The first important component in the circuit is a stable voltage reference that will maintain its voltage as the battery drains. Most voltage references used today are band-gap voltage references which require the use of BJTs. Unfortunately, the fabrication process provided by this project only provides MOS transistors. Borggreve [10] lays out a voltage reference design that only requires MOSFETs as it utilizes a pair of current mirrors. This design lacks the temperature stability provided by band-gap references. However, the contact lens is not expected to operate over a large temperature range as the eye's surface temperature is regulated by the body.

The basic design of the current mirror is shown in Fig. 3.43 below. It is composed of an unmatched PMOS current mirror on top and a matched NMOS current mirror on the bottom.
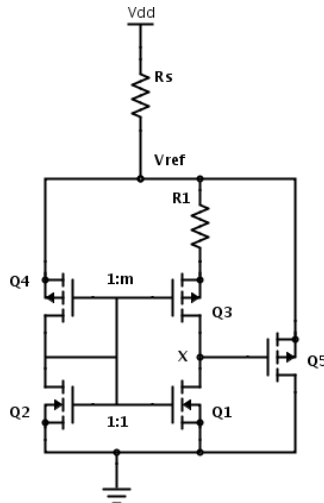
Figure 3.43: Voltage Reference

Even though the current mirrors are mismatched, the circuit maintains equal current through Q2 and Q4 through negative feedback. The mismatch between the NMOS and PMOS current mirrors produces a difference current out of node X. This difference current modulates the Vgs and Ids of Q5. The change in the current through Q5 changes the voltage Vref as well as the current through the current mirrors. So if the PMOS mirror has an effective mirror ratio higher than the NMOS mirror, I_{Q3} is larger than I_{Q1} which increases the V_{SG} of Q5. As the gate to source voltage of Q5 increases, it conducts more current which increases the current into the input of the mirrors Q4 and Q2. This causes a negative feedback response because it increases the amount of degeneration seen by Q3 due to resistor R_1 and lowers the effective mirror ratio. When the effective mirror ratio of the PMOS mirror is lower than the NMOS, I_{Q3} becomes lower than I_{Q1}. The circuit is then steered into the opposite direction and the response of circuit settles when there is a constant current through Q4 and Q2 and a constant voltage Vref. The reference voltage can be calculated as the voltage drops across Q2 and Q4 using the equation:

$$V_{REF} = V_{GS4} + V_{GS2} \tag{3.10}$$

40

Since the two MOSFETs are diode-connected, eq. 3.10 can be expanded to [10]:

$$V_{REF} = \sqrt{\frac{1}{k_p\prime(W/L)_4}}\sqrt{I_{REF}} + V_{TP} + \sqrt{\frac{1}{k_n\prime(W/L)_2}}\sqrt{I_{REF}} + V_{TN} \qquad (3.11)$$

The voltage reference was designed with the low capacity (in μAh) of the battery in mind. Also, the desired reference voltage will be chosen. Vref needs to be low enough to keep the transistors operating in saturation mode. Vref can be approximated by the added VT drops of the NMOS and PMOS transistor, about 1V each, which totals to 2V. Vref will be chosen to be 2.5V to give it extra headroom. In order to simplify the design and calculations, Q4 and Q2 will have the same aspect ratios.

Therefore, setting V_{REF} to 2.5V, I_{REF} to 1μA, and 1V as V_{TP} and V_{TN} turns eq. 3.11 to:

$$2.5V = \sqrt{\frac{1}{k_p\prime(W/L)}}\sqrt{1\mu A} + 1V + \sqrt{\frac{1}{k_n\prime(W/L)}}\sqrt{1\mu A} + 1V \qquad (3.12)$$

Solving for $\frac{W}{L}$ gives us 0.525 or 1.5μm/2.85μm for Q4 and Q2.

Next, the degenerating resistor R_1 will have to be determined. We can find this resistance by using the equation for the reference current I_{REF} [10]:

$$I_{REF} = \frac{1}{k_p\prime\frac{W}{L}R_1^2}(1 - \sqrt{\frac{1}{m}})^2 \qquad (3.13)$$

Since physical size is a major constraint of the integrated circuit, a low value resistor was desired. m refers to the aspect ratio mismatch between the PMOS Q4 and Q3, i.e. if m is 2 and the aspect ratio of Q4 of 1μm/1μm results in an aspect ratio of 2μm/1μm for Q3. m will be chosen to be a large value, 10, in order to lower the required resistance R_1. Therefore, substituting I_{REF} with 1μA, $\frac{W}{L}$ with 0.525, and m with 10 gives a resistance of 158kΩ.
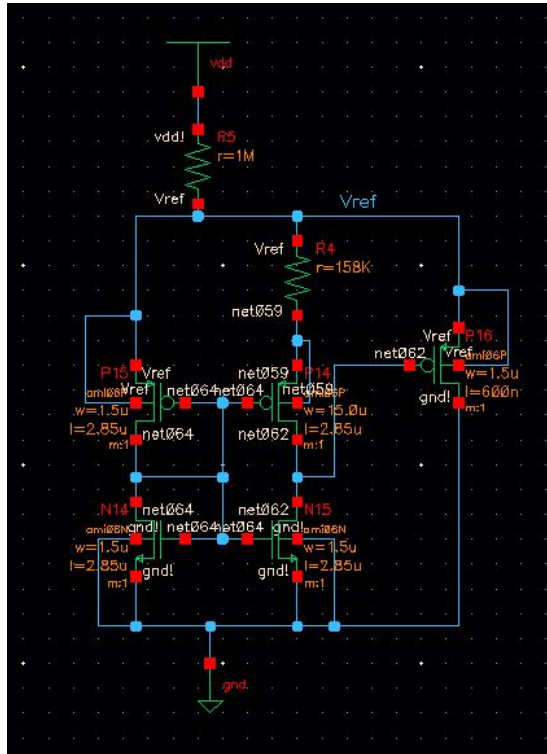
Figure 3.44: Voltage Reference Schematic

Lastly, the series resistance Rs which limits the current into the voltage reference, must be determined. Since the 1 μA reference current only accounts for the current going through 1 out of the 3 branches in the reference, the total sink current of the voltage reference will be greater than 1 μA. I chose a resistance of 1MΩ which results in a total current sink of $\frac{3.8V - 2.5V}{1M\Omega} =$ 1.3μA.

Fig. 3.44 shows simulated schematic of the voltage reference.
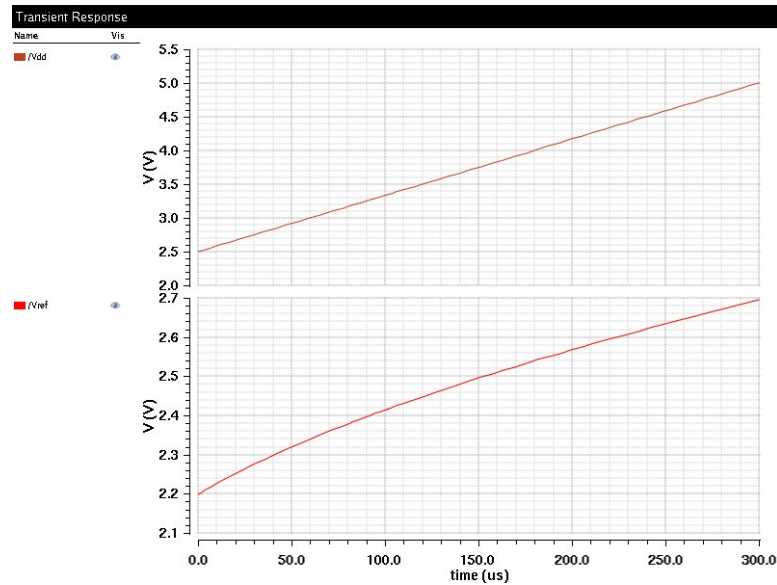
Figure 3.45: Voltage Reference Waveform

Fig. 3.45 shows the output voltage of the reference when Vdd was increased from 2.5 to 5V. Because the IC is operating off a battery that will discharge over time, it is important that the reference is stable. The line regulation, which is the reference's ability to hold a constant output value while varying the input voltage, was calculated to be 0.198V/V. Therefore, the voltage reference was expected to drop by 0.158V or about 6% during the operational range of the battery (3.8V to 3V). This 6% drop is acceptable for our application as comparators are the only circuits using this reference - the comparators will transition with an input voltage that is about 0.158V lower than expected. The comparators can be adjusted in future designs to account for this voltage reference deviation.

3.4.1.2 Comparator

With a voltage reference established, a comparator was designed to output a high value when the input is high. The comparator was realized using a simple differential pair.
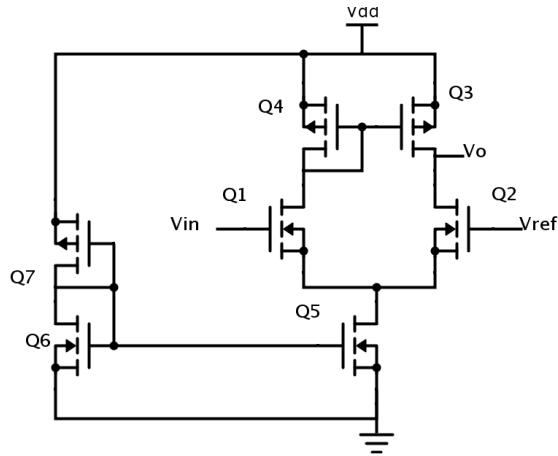
Figure 3.46: Comparator

First, the current mirror (Q5, Q6, and Q7) must be designed in order to bias the tail current of the differential pair determined by Q5. The current produced by the mirror was set to be 100nA in order to keep the current consumption of the battery low. Q6 and Q7 are the biasing components of the current mirror with Q7 being a current limiting transistor. A transistor was used as the current limiting element instead of a resistor was because of the size needed to realize a resistor of equivalent resistance to Q7. The resistance needed to limit the current through current mirror bias circuit was in the order of tens of MΩ which would require a physically large resistor. In addition, a PMOS transistor was chosen over an NMOS transistor was because its lower k/ meant higher effective resistance at shorter channel lengths. In order to keep V_{DS} of Q5 low, the gate voltage of Q5 and Q6 should be kept low also while keeping the transistor on. The NMOS and PMOS transistors have turn on voltages V_{TN} and V_{TP}, respectively, of around 1V. Therefore, the gate voltage was chosen to be 1.2V to give extra headroom. The aspect ratio of Q6 and Q7 was solved to be 1.5μm/21.6μm and 1.5μm/339.4μm using the standard MOSFET equation eq. 3.14 when operating in saturation region.

$$I_{DS} = k\prime(W/L)(V_{GS} - V_T)^2 \tag{3.14}$$

Q1, Q2, Q3, and Q4 were 1.5μm/0.6μm. The simulated design is shown below in fig. 3.47.
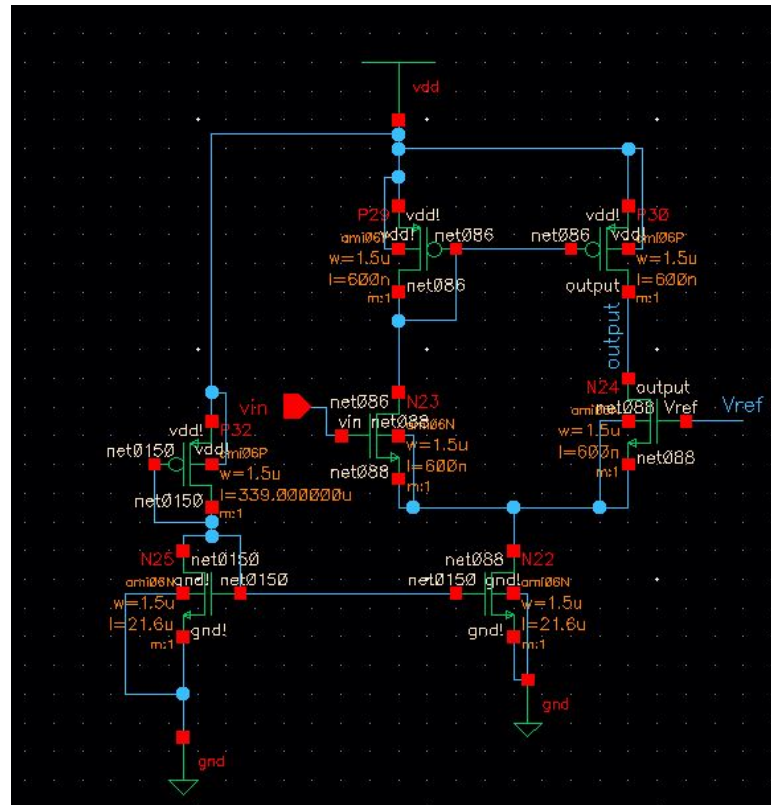
Figure 3.47: Schematic of Comparator

Fig. 3.48 shows the operation of the comparator. The top two waveforms display the current flow through the differential pair. The tail current generated by N22 only turns on when the input voltage is high and sinks 99nA. When Vin is low, the tail current does not sink any current because of the active load generated by the PMOS transistors P29 and P30. When Vin is low, net086 swings high turning off P29 and P30. Therefore, the right side of the differential pair does not conduct during a low input. The middle two waveforms show the operation of the current mirror. The current mirror was biased to 96nA instead of the designed 100nA. A differential pair usually has constant current flowing through the tail transistor N22. The comparator here only has current conducting when Vin is high which may negatively affect the speed of the comparator. Since the response time is not critical in our design, a tradeoff between lower speed but lower current draw is desirable. V_{GS} for N25 was simulated to be 1.18V instead of 1.2V which explains the lowered current. Additionally, the turn on voltage of the PMOS may be higher than 1V because of the lowered V_{GS} of N25. The bottom two waveforms show output

of the comparator with a pulsed input.
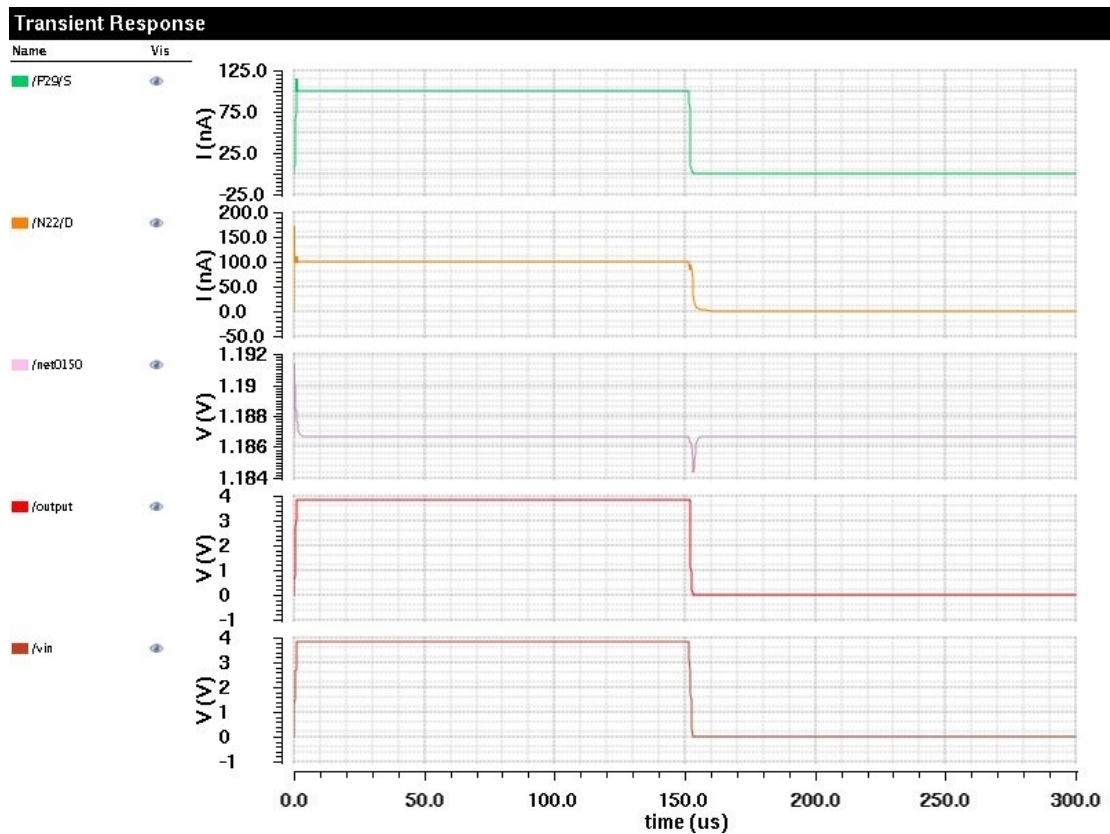
Figure 3.48: Comparator Waveforms

3.4.1.3 Rectifier

The comparator designed in the previous section only accepts positive DC voltages as its input while the signal sent from the sensor was a 2.4GHz sinusoid. Therefore, the incoming signal must be rectified before the comparator can accept it. The rectifier was implemented using a voltage multiplier shown in Fig. 3.49. The benefit of having a voltage multiplier is its ability to boost the amplitude of the incoming signal by cascading stages on top of each other [11].
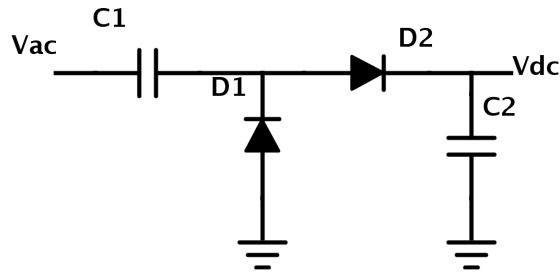
Figure 3.49: 2-Stage Voltage Multiplier

As more stages are stacked on, the output voltage increases given by:

$$V_{DC} = 2N(V_{in} - V_{th}) \tag{3.15}$$

Eq. 3.15 shows that the output voltage increases linearly with the the number of stages. Also, the output voltage is affected by the turn on voltage, V_{th}, of the device. Thus, there is a limit on how many stages the voltage multiplier has because of the body effect which increases the transistor's turn on voltage. Also, the size of the transistors affects the performance of the rectifier. A larger width lowers the resistance of the channel, but it also lowers the speed of performance of the transistor [11]. Therefore, the width of the transistor can not be set to just a very large value. According to the MOSIS SPICE parameters in appendix A, a wide transistor has an aspect ratio of 20μm/0.6μm - this was considered the upper bound of the transistor width. Fig. 3.50 shows the design of the 13MHz rectifier with transistor widths of 20μm and the bulk of the transistor was tied to the source in order to eliminate body effects. Capacitors were sized using trial and error simulations to determine smallest capacitance while obtaining a DC output. Since capacitors are the largest physical elements in the circuit, they were sized to be as small as possible while maintaining circuit functionality.

Figure 3.50: 3-Stage Voltage Multiplier

The DC voltage source with resistor R15 represents the battery and its internal resistance. 3.1V was chosen as the battery voltage as that is the lowest allowed battery voltage before cell damage occurs. Fig. 3.51 shows the output voltage when a 2V sinusoid was applied to its input. The output is a 3.3V DC with 0.3V peak to peak ripple.

Figure 3.51: 3-Stage Voltage Multiplier Output

A 2V sinusoidal signal at the receive coil will be barely enough to charge the battery when the battery is depleted. The reason for the poor AC to DC amplitude conversion was mainly due to the low output capacitance. A larger output capacitor will allow for a larger charge build up resulting in a higher DC voltage. However, larger capacitors require more surface area. In order to obtain a higher output voltage, the amplitude of the sinusoid will have to be increased.
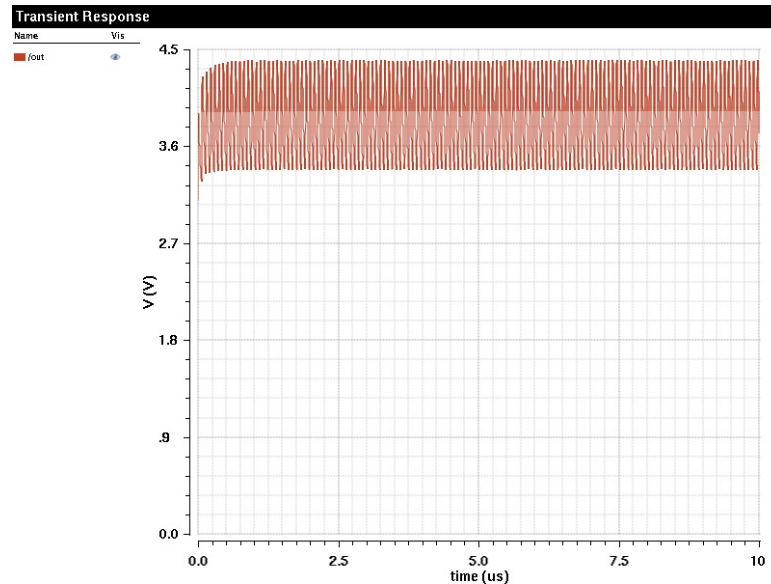
Figure 3.52: 3-Stage Voltage Multiplier Output with 4.5Vp Input

Fig. 3.52 shows a DC voltage of 3.8V with a 4.5V peak input signal. The reason for the lower AC to DC conversion as compared to fig. 3.51 is because as the DC voltage increases, the battery draws more current which begins loading the rectifier due to its low output capacitance - the capacitor is not able to both maintain the high output voltage and source the higher current at the same time. However, the battery's voltage will increase as the time elapses which lowers the current draw of the battery allowing the voltage across the output capacitor to build up resulting in a concurrent increase in the rectified voltage. Therefore, a 2Vp to 4.5Vp signal will be required at the input of the rectifier to properly charge the battery.

Similarly, a voltage multiplier is needed for the 2.4GHz signal from the external UV sensor. Again, the rectifier was realized by a 3-stage voltage multiplier with transistor dimensions 20μm/6μm to keep channel resistances low. Since this rectifier is for a higher frequency signal, the capacitor sizes can be reduced - capacitors were sized to be 500fF and an output storage

capacitor of 1pF through trial and error from simulations. Fig. 3.53 shows the rectifier for the 2.4GHz signal. The 1MΩ output resistance simulates the high input gate resistance of the comparator.
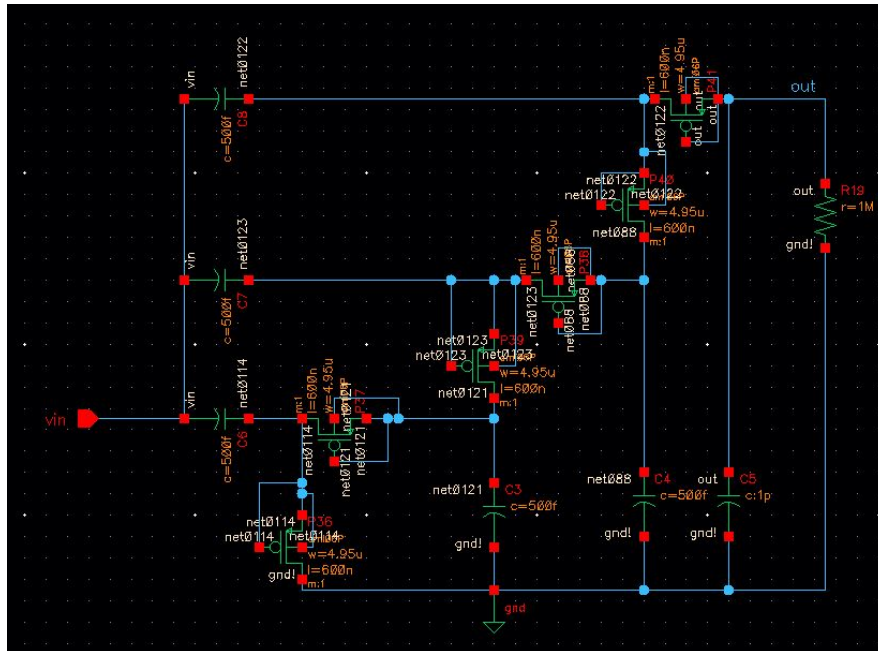
Figure 3.53: 2.4GHz 3-Stage Voltage Multiplier

The large MOSFET turn on voltages are a significant disadvantage of ON SEMICONDUCTOR's fabrication process. As a result, the rectifiers need a large amplitude signal for the circuit to operate. Fig: 3.54(a) shows a $2.2V_{DC}$ output voltage with a 1V peak input. Using eq. 3.15, the turn on voltage of the transistors were calculated to be 0.6V. Fig.3.54(b) shows the output of the rectifier when the input is right at the threshold level of the rectifier's operation. In order for the rectifier to work, the antenna has to output around 8dBm. Assuming the antenna has a total efficiency of around 10%, the signal received by the antenna must be at least 64mW or 18dBm. In order to achieve this high of a power at the output of the antenna, the operational distance of the sensor and contact lens link must be significantly decreased or the sensor's output power must be increased. Additionally, an amplifying stage could be introduced before the rectifier in order to boost the incoming signal to a high enough level for the rectifier.

(a) 1Vp Input

(b) 0.6Vp Input
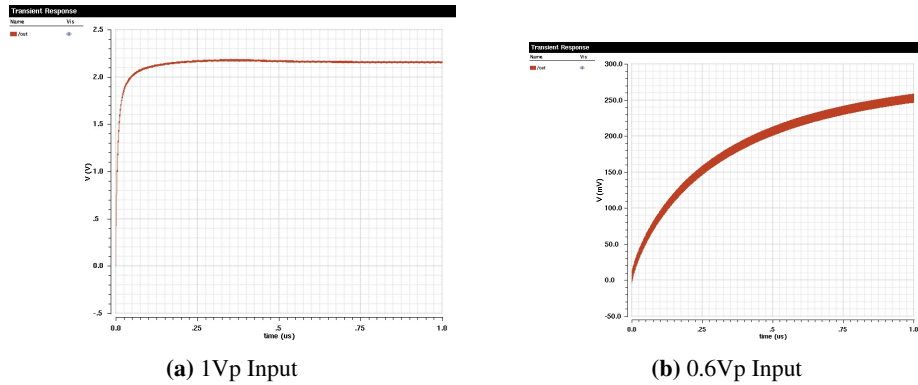
Figure 3.54: Output Voltage of 2.4GHz rectifier

3.4.1.4 Common Source Amplifier

As stated in the previous section, a 18dBm signal power level must be present at the chip's input in order for the rectifier to operate. Since the original specification called for an operational distance of 30cm, the output power from the external sensor with a 2dBi antenna must be at least 45dBm. That is a extremely large power so in order to lessen the output power requirement of the sensor, an amplifier was introduced at the input of the chip. The amplifier must be: 1. input matched to 50Ω at 2.4GHz and 2. have a low quiescent current. The amplifier was realized with a common-source amplifier with inductor degeneration for power matching.

Figure 3.55: Common Source Amplifier with Inductor Degeneration

Q1 is the main amplifying transistor with L1 as the degenerating inductor for input matching. L2 resonates out the gate-source capacitance C1 to allow for 2.4GHz operation [12]. Another important capacitance inherent of MOSFETs is the gate to drain capacitance (C_{GD}) which is not shown in the figure. In low frequency operations, C_{GD} prov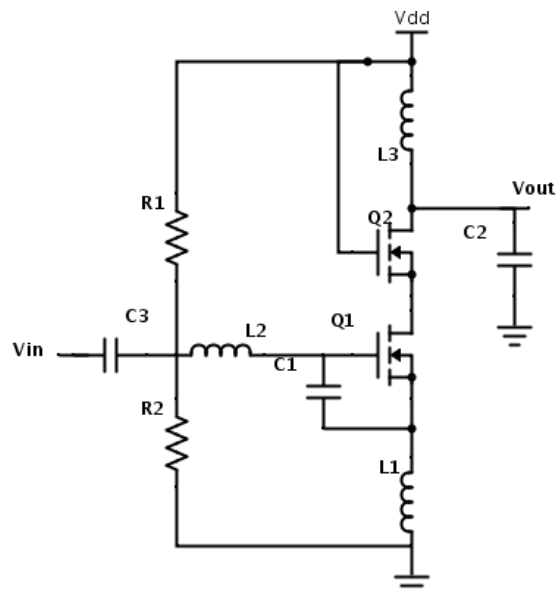ides a high impedance which isolates the output from the input. However, that impedance decreases as the frequency increases and feedback occurs between the output and input of the amplifier [13]. The type of feedback depends on the load that the amplifier is driving; negative feedback occurs when the load is mainly capacitive while positive feedback is caused by inductive loads. Adding a cascoding transistor Q2 isolates the output from the input reducing the amount of feedback. However, the cascode introduces parasitic capacitances to the output of the amplifier which lowers the gain of the amplifier as the capacitances provide a path to ground for the signal. To mitigate the parasitic capacitances of Q2, an inductive load L3 is applied to resonate out those capacitances. Since all passive components must be on-chip, inductor sizes were the limiting factors of the amplifier design. Therefore, the first step was to set an inductance value and design the amplifier around it. The operational frequency of the amplifier is determined by the equation [13]:

$$\omega_o = \frac{1}{\sqrt{L_{tot}C_{GS}}} \tag{3.16}$$

L_{tot} is the total inductance from L1 and L2. Eq. 3.16 shows the tradeoff between inductor and transistor sizing. A smaller inductor results requires a higher gate source capacitance which is achieved by larger transistors. A total inductance of 5nH was set and the required C_{GS} was calculated to be 880fF. The gate source capacitance is determined by [12]:

$$C_{GS} = \frac{2}{3}C_{OX}WL \tag{3.17}$$

C_{OX} is determined by the fabrication process and can be calculated using:

$$C_{OX} = \frac{\varepsilon_o \varepsilon_r}{t_{OX}} \tag{3.18}$$

t_{OX} can be found in the spice model and ε_r is the relative permittivity of SiO_2. C_{OX} was calculated to be 2.44mF. Therefore, the transistor will require a width of about 0.9mm in order to produce the required 880fF C_{GS}. The size of the transistor can be lowered by introducing a discrete capacitor in parallel with the gate-source of the transistor where the sum of the those capacitances add up to 880fF. If the width of the transistor is lowered by about a third, C_{GS} becomes 264fF and a parallel capacitance of 616fF can be added which only requires an area of $25\mu m^2$. The input impedance is determined by inductor L1 and can be calculated using [13]:

$$R_S = g_m \frac{L_S}{C_{GS}} \tag{3.19}$$

If L1 is set to 1nH, g_m can be calculated to be 44mS for an input impedance of 50Ω. Voltage divider R1 and R2 biases the gate of the transistor to obtain the proper g_m. The gate-source voltage can be calculated using:

$$V_{GS} = \frac{g_m L}{k\prime W} + V_T \tag{3.20}$$

Therefore, a gate voltage of 1V will bias the transistor in the desired operation. Lastly, L2 needs to be 4nH such that the total inductance is 5nH as specified earlier in the design. L3 and C2 were found by simulating the circuit and observing that 2.4GHz was within the passband of that filter. Q2 was chosen to have the same dimensions as Q1.

Figure 3.56: Initial Common Source Amplifier Design
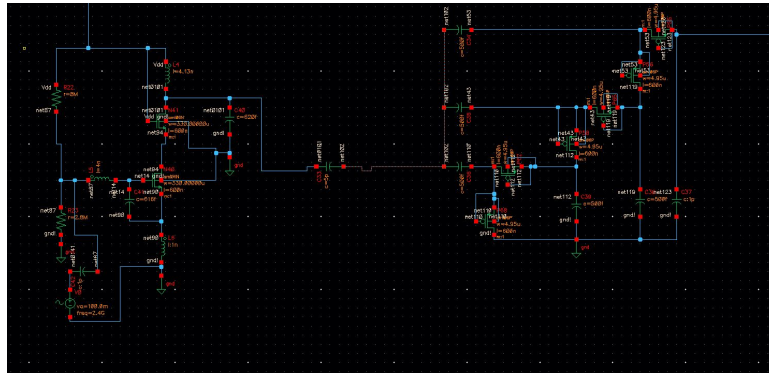
Fig. 3.56 shows the common-source amplifier with the designed parameters and the rectifier load. The series capacitors at the input and output are for DC block.
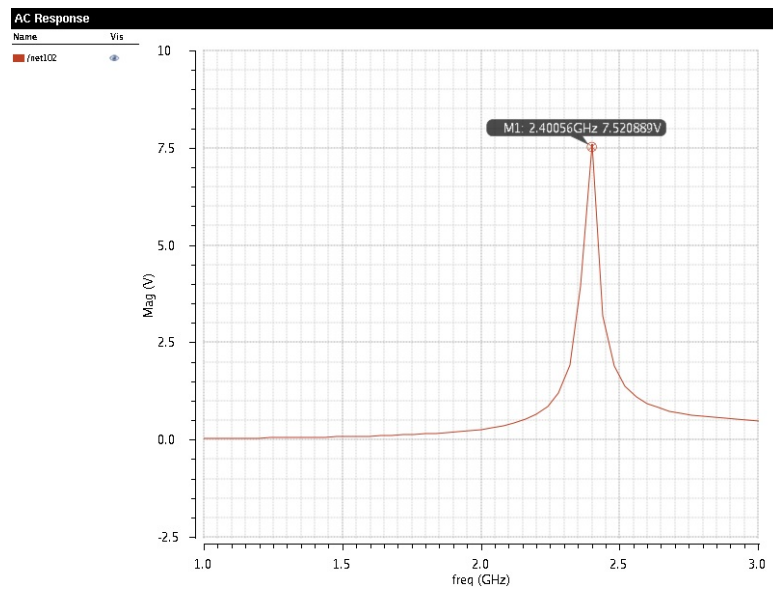

Figure 3.57: AC Response of Amplifier

Fig. 3.57 shows the AC response of the amplifier with an input waveform magnitude of 0.1V. The amplifier is correctly tuned to 2.4GHz operation and has a max gain of 38.5dB.
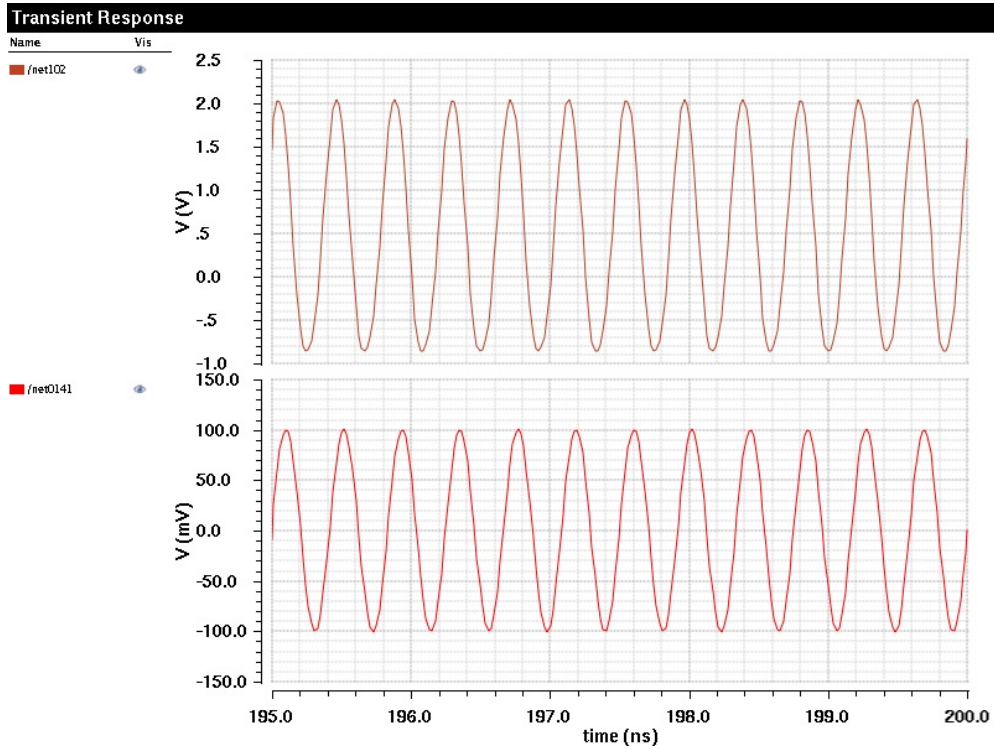
Figure 3.58: Output (top) and Input(bottom) Waveforms of Amplifier

Fig. 3.58 shows a 2.8Vp waveform with a 100mVp input signal. The output has slight DC offset as the output DC blocking capacitor may not be large enough. The common source amplifier seems to have sufficient gain while substantially lowering the required input signal from the antenna to 100mVp. However, the tradeoff to such high gain is a high current draw. The bias current can be calculated using the equation [12]:

$$I_D = (V_{GS} - V_T)\frac{g_m}{2} \tag{3.21}$$

Using eq. 3.21, the bias current can be calculated to be about 7mA. This current is confirmed in the figure below.
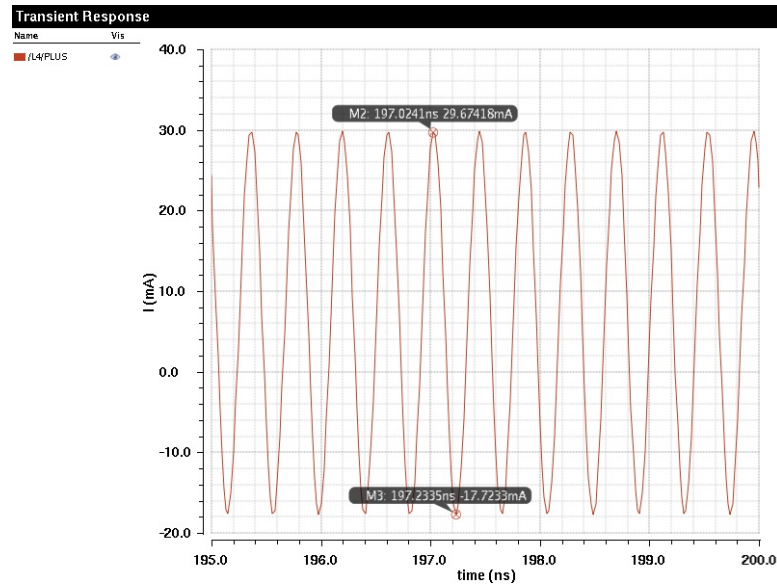
Figure 3.59: Source Current of CS Amplifier

Fig. 3.59 shows a DC current of about 6.5mA. This poses a large issue as the thin film battery can not provide that high of a current. Thus, the design of the amplifier must be adjusted to lower its bias current. The tradeoff to lowering the bias current would be a decrease in g_m which affects the gain of the amplifier and also the input impedance. However, this tradeoff is necessary if the amplifier is to operate using the thin film battery. The resistor divider into the gate of the transistor was altered such that a lower voltage was sent to the gate. The bias current was specified to be 1μA and the values for the resistive divider was found through simulating the circuit.

Figure 3.60: Lower Current CS Amplifier

Fig. 3.60 shows the adjusted design to support a lower current draw. The gate bias resistive divider was changed in order to lower the gate to source voltage of the transistor. Fig. 3.61 shows the lowered current draw.
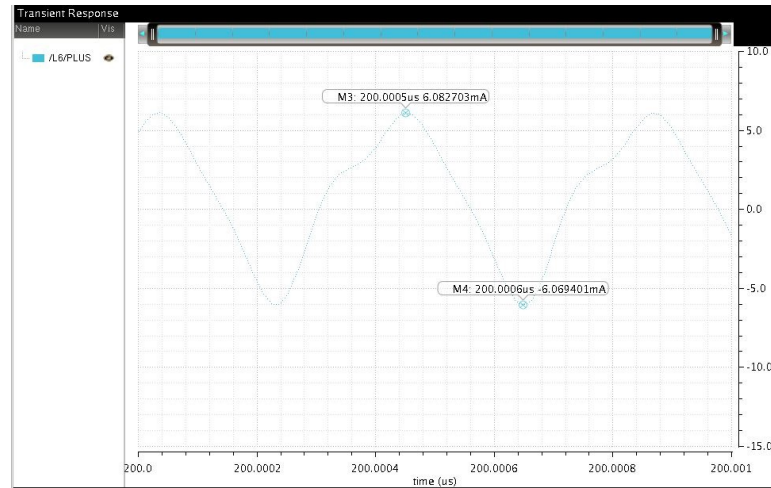
Figure 3.61: Current Through Source Inductor
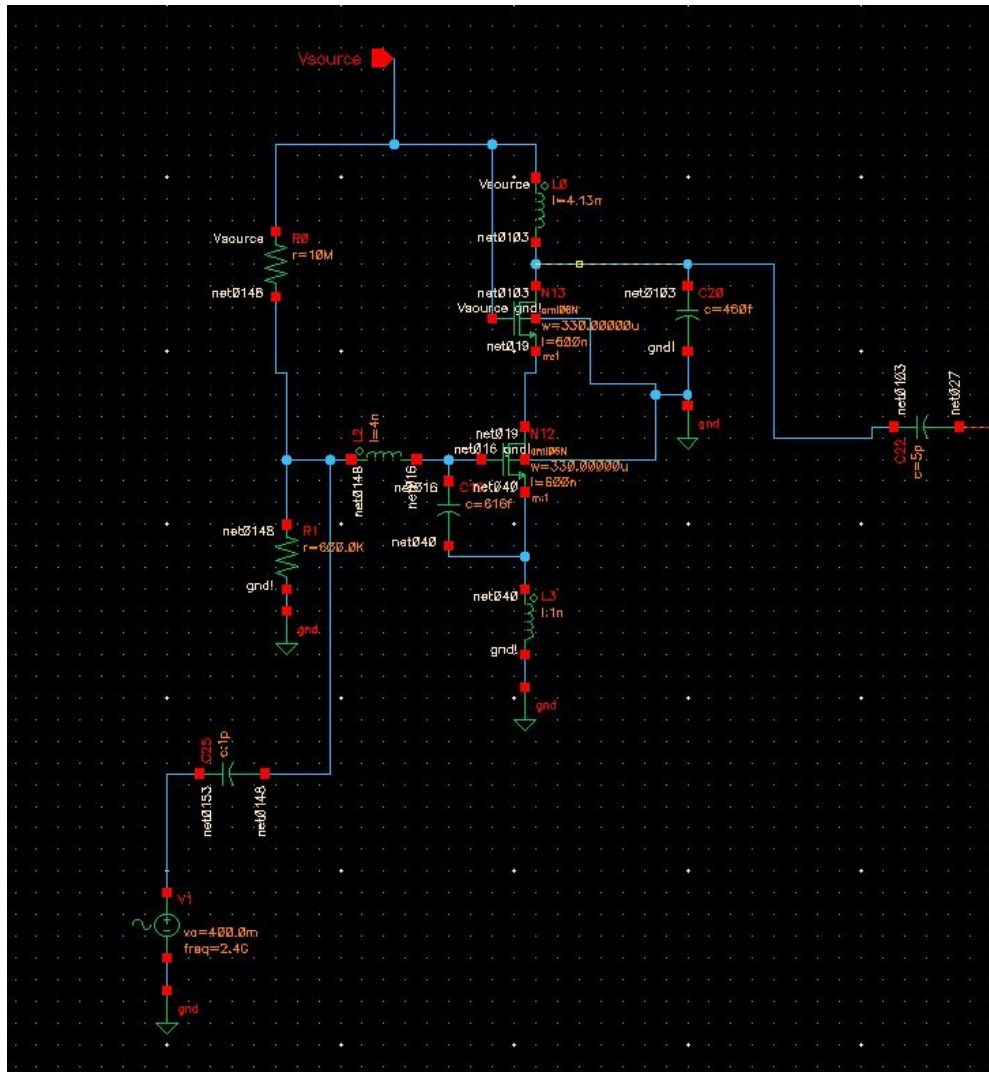
The tail current draws an average of 5μA which is higher than desired. In order for the transistor to consume less current, the gate voltage would have to be lowered even more. The transistor in Fig. 3.60 is already biased to its threshold of conduction as shown in the non-linearity of the current waveform. Therefore, this was the lowest bias current that could be achieved while still allowing for signal amplification.
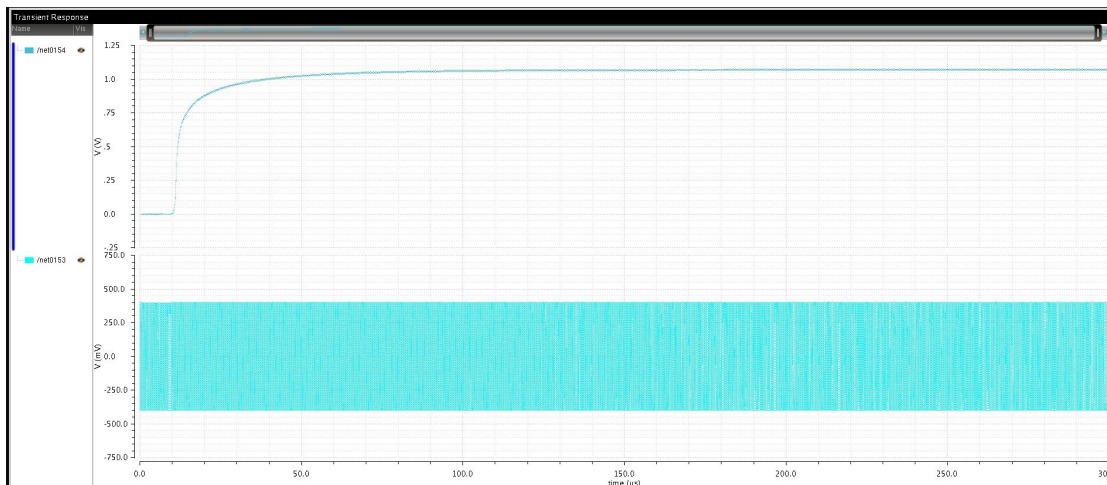
Figure 3.62: Output of Rectifier with 350mVp Input Signal to Amplifier

Fig. 3.62 shows the output DC level from rectifier with a 0.35V peak input. While the amplifier was biased at the edge of conduction, the gain was high enough to reduce the required input signal level as compared to Fig. 3.54(b). However, the output voltage of the rectifier is not high

enough to set the output of the comparator high - the input signal level has to be increased
further. Fig. 3.62 shows that a 0.5Vp signal is more than enough to provide a DC voltage larger
than the 2.5V threshold voltage.
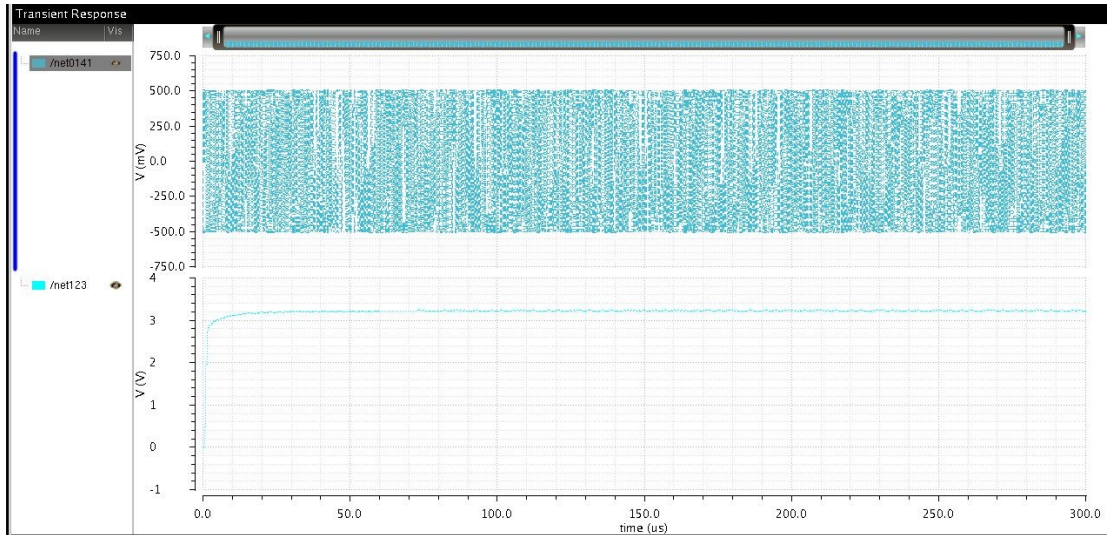
Figure 3.63: Output of Rectifier with 350mVp Input Signal to Amplifier

3.4.1.5 Voltage Regulator

One of the major advantages of using the CBC005 battery from Cymbet is its charging
simplicity. The only charging requirement is that a constant voltage between 4V and 4.3V is
applied to its terminals while the internal resistance of the battery will limit the current to
protect the cells as shown.
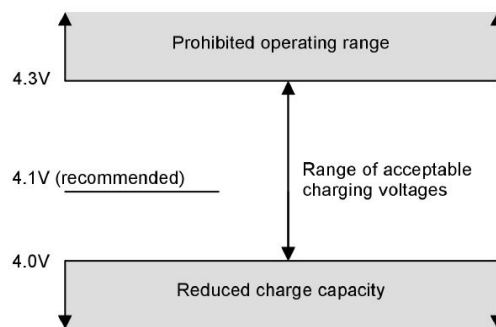
Figure 3.64: Allowed Voltage Range for Battery Recharge

Since wireless charging was employed to recharge the battery, the simplest method to charge the

battery would be to apply maximum power at the transmit coil. By applying the maximum amount of power on the transmit side, the charging voltage at the receive side will be less sensitive to coil misalignment while also meeting the lower bound of the recommended charging voltage. However, the issue of exceeding the maximum rated 4.3V charging voltage will occur when maximum power is applied by the charger. To address this problem, the IC implements a low dropout (LDO) voltage regulator such that the rectified voltage does not exceed the maximum rating.
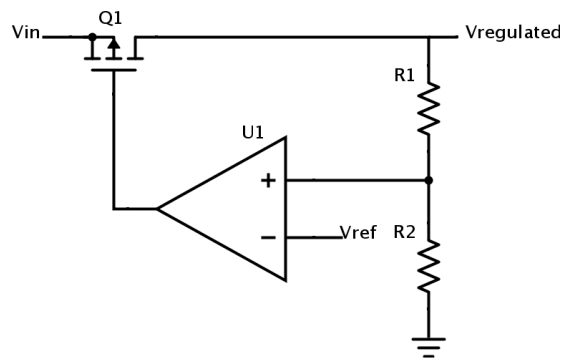
Figure 3.65: Voltage Regulator

As shown in Fig. 3.65, an LDO consists of a comparator, a PMOS pass transistor, and a feedback loop for the output [14]. As the voltage seen by the non-inverting input increases towards Vref, the output of the comparator is low and turns on the pass transistor. Once the voltage at the output of the divider reaches the level of Vref, the comparator outputs a high value turning off the PMOS transistor which in turn lowers the regulated voltage. Therefore, the regulated output voltage stabilizes when the voltage at the non-inverting input of the comparator equals the reference voltage. Since the comparator was already designed in section 3.4.1.2, the LDO will incorporate the same design.
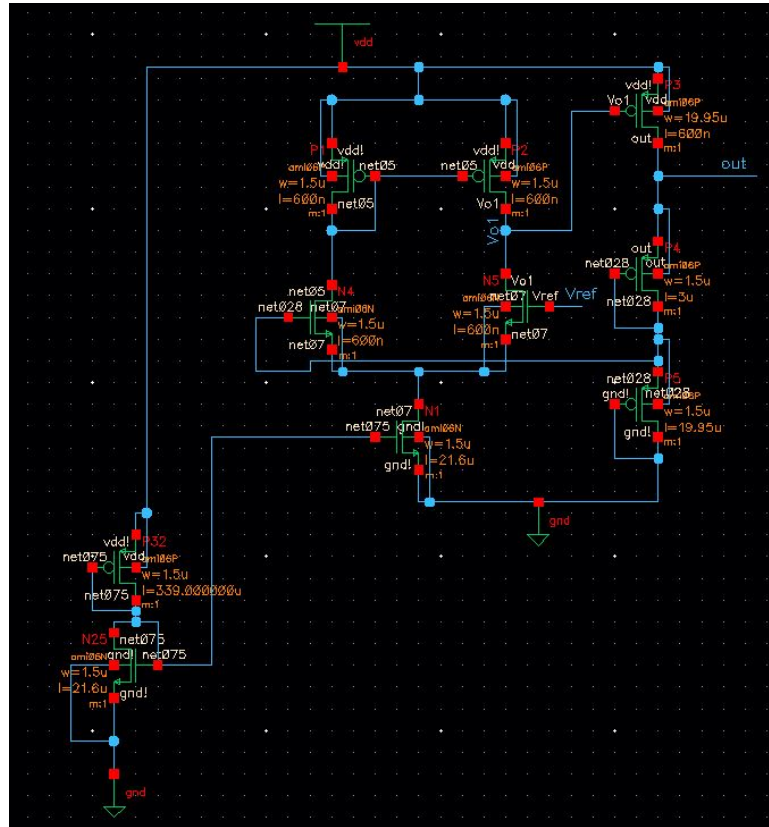
Figure 3.66: Voltage Regulator Schematic

The resistor divider was replaced by a PMOS voltage divider as large value resistors occupy a large area. The aspect ratios of the PMOS voltage divider can be calculated by setting the two currents equal to each other:

$$\frac{(W/L)_4}{(W/L)_5} = \frac{(V_X - V_{TP})^2}{(V_{DD} - V_X - V_{TP})^2} \tag{3.22}$$

where V_X is the voltage at the non-inverting input of the comparator. The aspect ratios of P4 and P5 must produce a V_X of 2.5V (when operating in saturation mode) which is the value of the reference voltage. Therefore, the resulting ratio between the two PMOS transistors calculates to 6.67 using eq. 3.22.

The aspect ratio of P4 was found by setting a current value of 1μA flowing through the branch

and using the equation [15]:

$$I_{SD} = k_p' \frac{W}{L}(V_X - V_{TP})^2 \tag{3.23}$$

By setting V_X to the 2.5V reference voltage, the aspect ratio of P5 was calculated to be 0.05. Once the width and length of P5 was determined, the aspect ratio for P4 can be calculated by multiplying 0.05 by 6.667 which results in 0.333. The aspect ratios had to be tweaked to 0.075 and 0.5 for P5 and P4 to get an exact regulated voltage for 4.1V.

Figure 3.67: Voltage Regulator Output Response

Fig. 3.67 shows the output response of the voltage regulator (bottom) with a ramp voltage as the input (top). The output follows the input until V_{DD} reaches 4.1V. When the input voltage rises past 4.1V, the regulator holds the output voltage and prevents it from increasing.
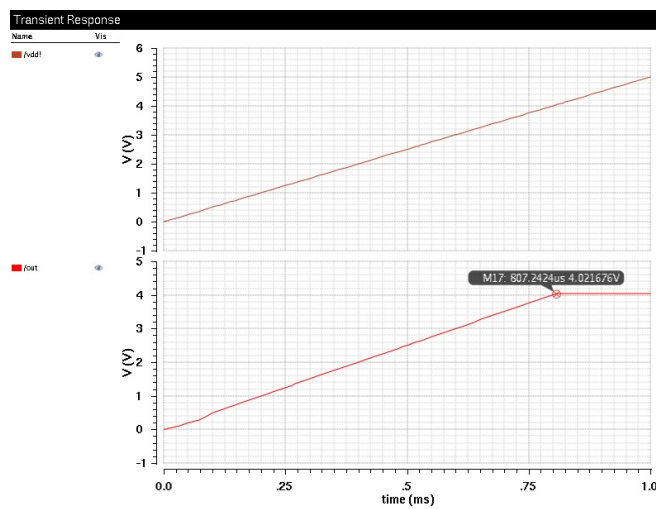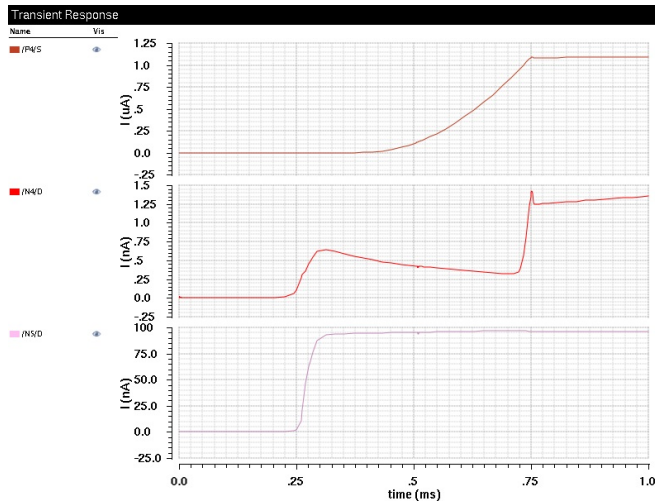
Figure 3.68: Voltage Regulator Current Draw

Fig. 3.68 shows the current draw of the voltage regulator. The altered P4 and P5 aspect ratios increased the current draw from the desired 1μA to 1.5μA. The next two waveforms show the current draw of the comparator. Unlike the design of the comparator in section 3.4.1.2, the current draw of the comparator is not crucial as the current drawn is from the wireless charger instead of the battery. However, since the comparator was a low power design taken from an earlier section, the LDO still draws low amounts of current (in the low μ range).

3.4.1.6 Battery Low Voltage Cutoff

Deep discharge of the battery must also be prevented to maximize the lifetime of the battery. In accordance to CBC005 datasheet specifications, the battery must stop discharging when the voltage drops to 3V or else the cells will become degraded. Therefore, a low battery cutoff switch was required to prevent the battery from entering that deep discharge state. The design of the cutoff circuitry is very similar to that of the voltage regulator - it is implemented by a comparator and a pass transistor. The only difference is the unneeded feedback loop for a stable output voltage as the output either needs to be high or low. The figure below shows the design of the cutoff circuit.
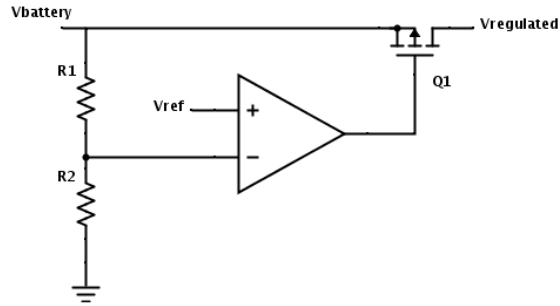
Figure 3.69: Low Battery Cutoff

The inverting input of the comparator monitors the voltage level of the battery. As the voltage seen on that input drops below the reference voltage, the output of the comparator swings high and turns off the PMOS pass transistor. With the pass transistor off, the battery becomes disconnected from the rest of the battery.
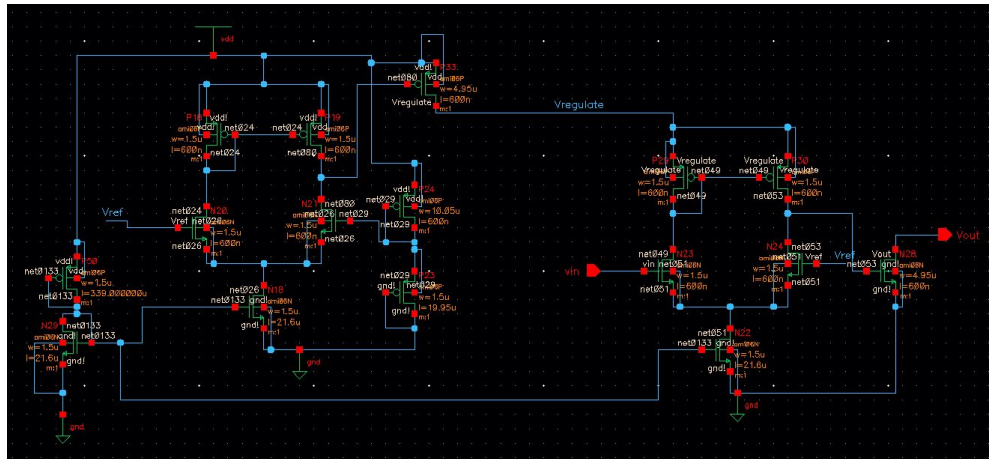
Figure 3.70: Low Voltage Cutoff Schematic

Fig. 3.70 shows the schematic of the low voltage cutoff circuitry. Similar to the voltage regulator design, the resistive divider was replaced by MOSFETs that simulate a high resistance value in order to save space. The aspect ratios of P24 and P25 were calculated using eq. 3.23 such that the voltage at the inverting input of the comparator sees a voltage of 2.5V when the battery voltage drops to 3V.
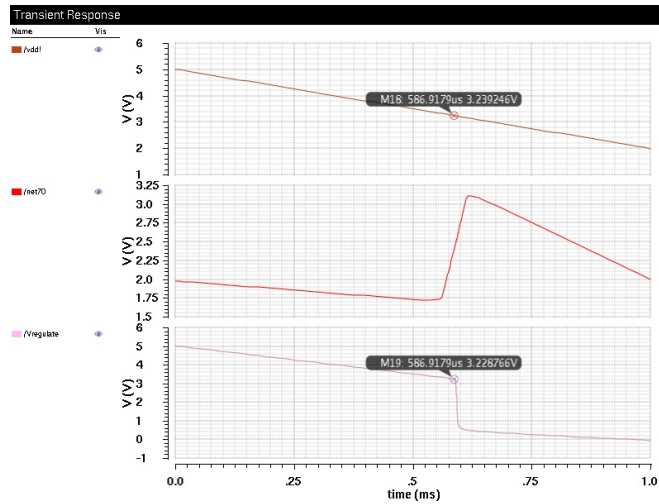
Figure 3.71: Response of Low Voltage Cutoff

Fig. 3.71 shows the waveforms of the voltage cutoff circuitry. The input (top) is the ramp waveform dropping from 3.8V to 2V. When the input drops to 3.2V, the comparator's output (middle) swings high and turns off the the PMOS pass transistor. Thus, the PMOS cuts off the voltage path for the battery (bottom).

3.4.2 Complete Design

Fig. 3.73 below shows the schematic of the whole IC. Currently, the only circuit that will be disconnected from the battery by cutoff circuitry is the output transistor for the display and the comparator to drive that transistor. As future work increases the functionality of the IC, the added components should be placed after the battery cutoff circuit.
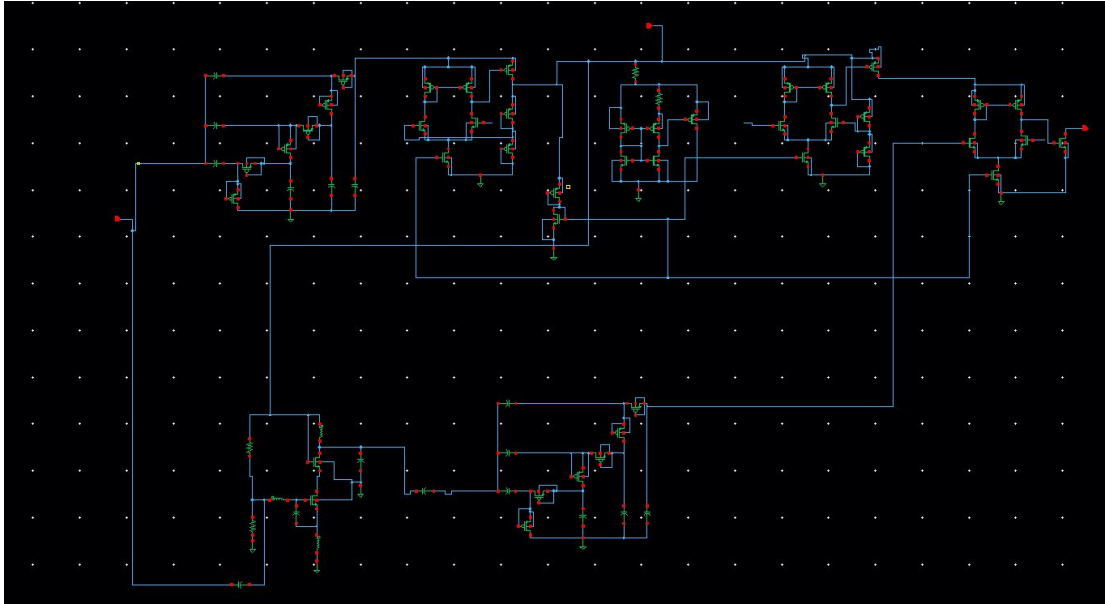
Figure 3.72: Complete IC Schematic
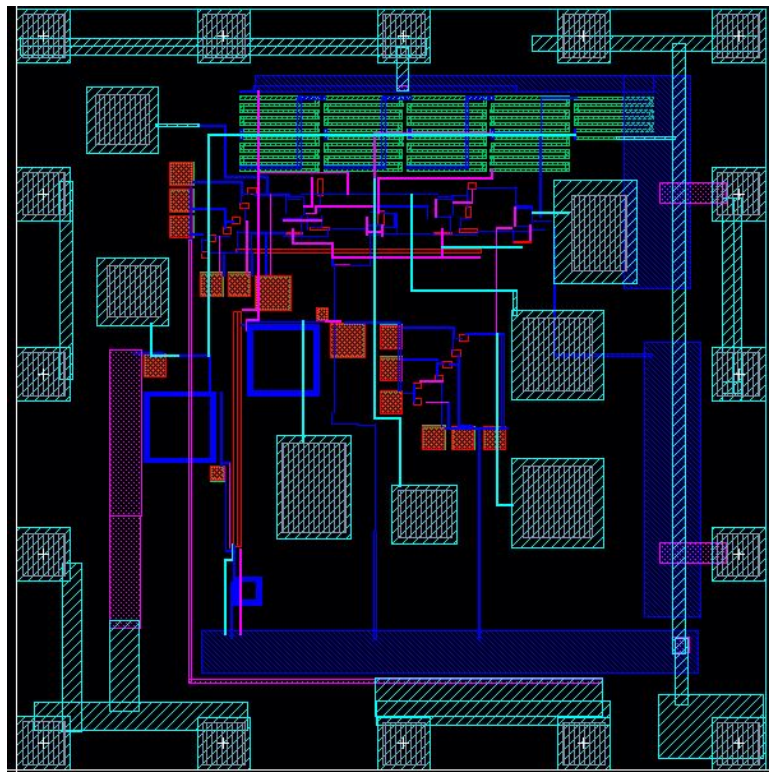
Figure 3.73: Circuit Layout

Fig. 3.73 shows the layout of the IC. The bare die has dimensions of 1mm by 1mm thus it is

small enough to be situated right on top of the battery. Unfortunately, a significant error occurred during the layout process of the IC. In the design of the common-source amplifier, the output capacitor should be tied to ground.
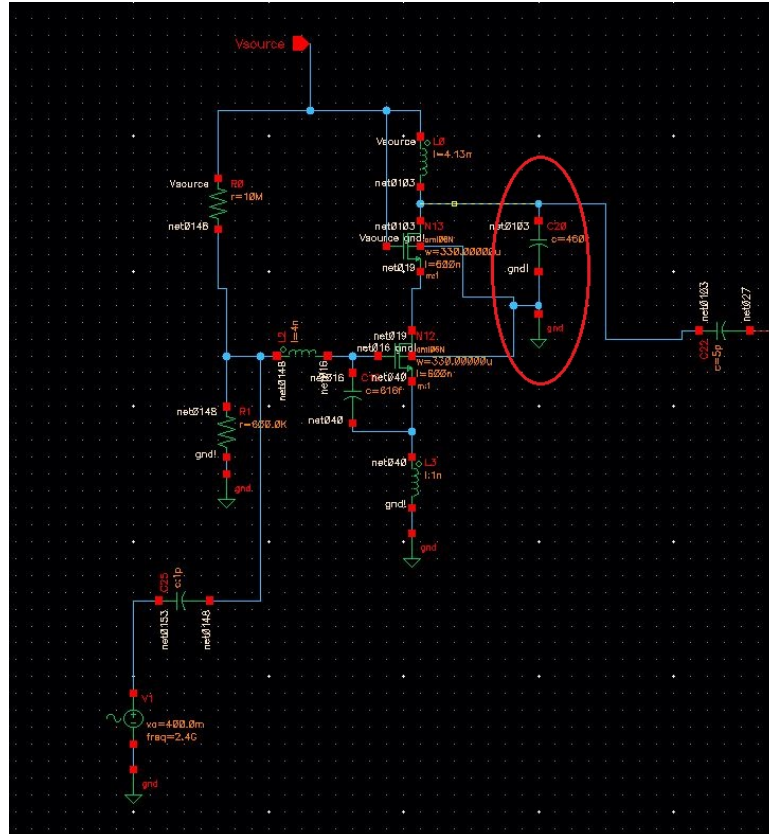
Figure 3.74: Correct Output Capacitor Placement of CS Amplifier
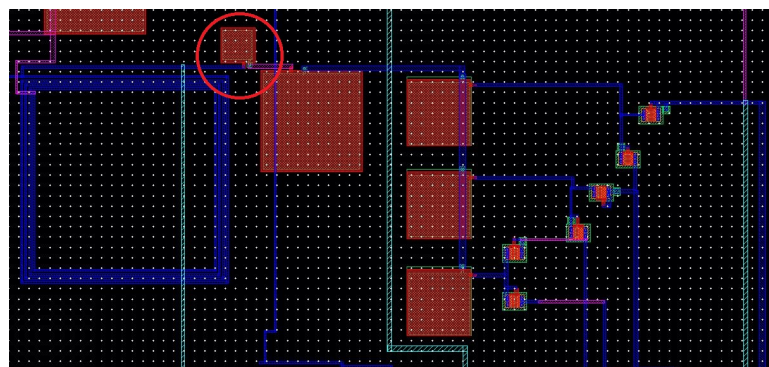
Figure 3.75: Incorrect Series Connection of Capacitor

The error occurred in the circled portion of fig. 3.75 where the 460fF capacitor to ground was

mistakenly connected in series. Unfortunately, the LVS (layout vs. schematic) feature of Cadence was not working properly during the layout of the circuit. The function of LVS was to notify the designer of any netlist anomalies between the schematic and layout. Without the aid of LVS, this error was overlooked and was not caught before the design was sent out to the fabricator. The figure below shows the simulated results with the capacitor in series as occurred in the layout. The series capacitance causes the output of the rectifier to be negative instead of a positive DC value.
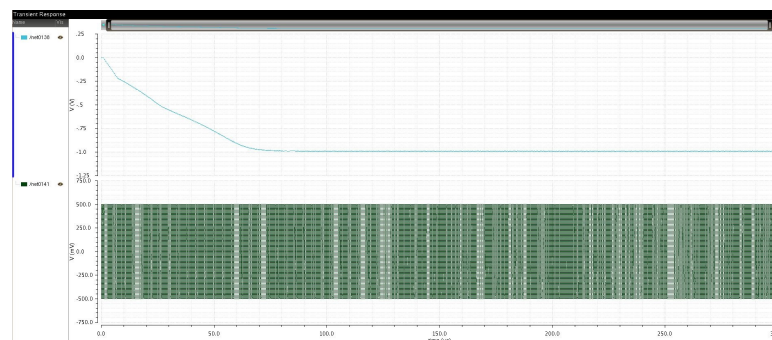
Figure 3.76: Output Waveform with Series Connected Output Capacitor

3.4.3 Results

MOSIS was kind enough to provide us with 5 IC's in bare die form and 1 in packaged form for free. While the design of the circuit only occupied a 1mm by 1mm area, MOSIS adds on additional space for the 30μM overhead containing the fabrication ID. If size was critical, this overhead could be eliminated by using other processes such as IBM's. In addition to the overhead, MOSIS adds an additional buffer to separate the many designs that were fabricated on the single wafer.
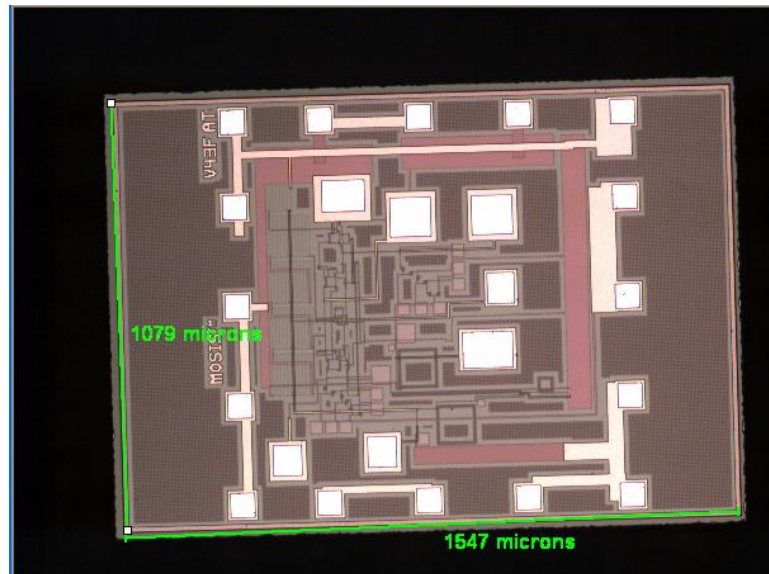
Figure 3.77: Microscope Capture of IC

IC functionality testing was done using the probe station located in the microfabrication lab on campus. The probe station consists of probing needles for pad contact, microscope, and basic testing equipment such as supplies and digital multimeter
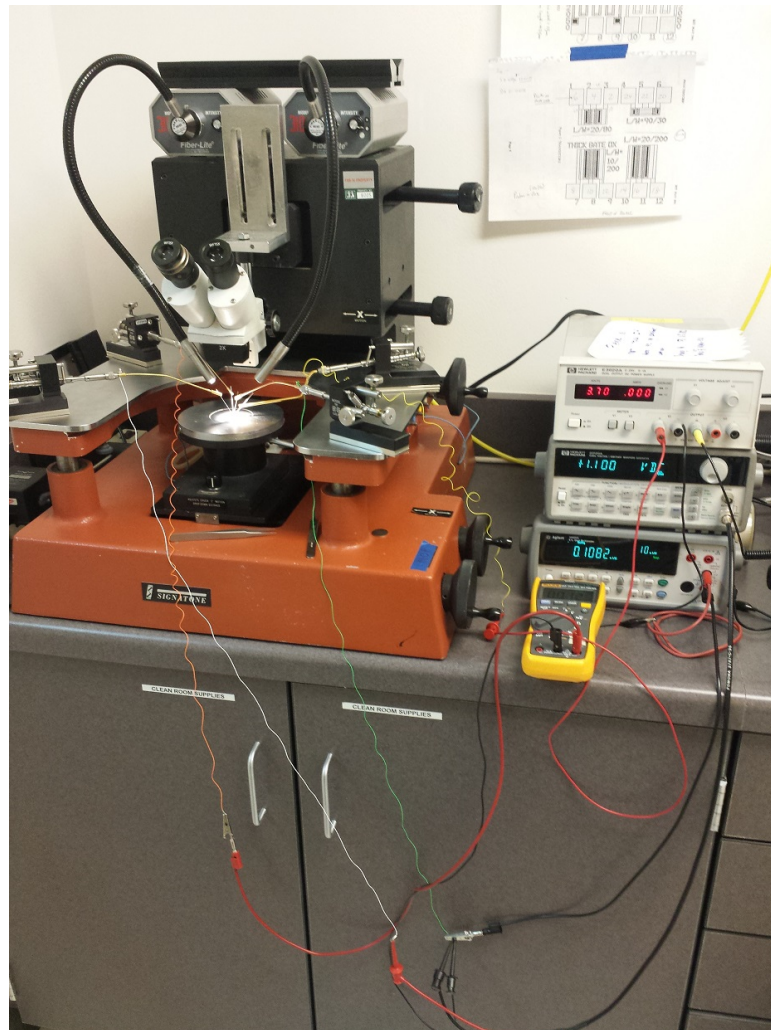
Figure 3.78: Probe Station Setup

Connection from the test equipment and the IC pad was achieved using the micromanipulators as show in fig. 3.79 below. At the end of the micromanipulators are probing needles that provide contact to the pad. Three dials - for the X,Y, and Z axis - are used to place the needle on the IC contacts. The needles are very sharp in order to make contact with the small IC pads; my inexperience with the micromanipulators caused me to damage some of the pads. Probing the IC was difficult and time consuming because I had a hard time determining if the needle was actually touching the pad or not as you risk damaging the pads if the sharp needle puts too much pressure on the pad.
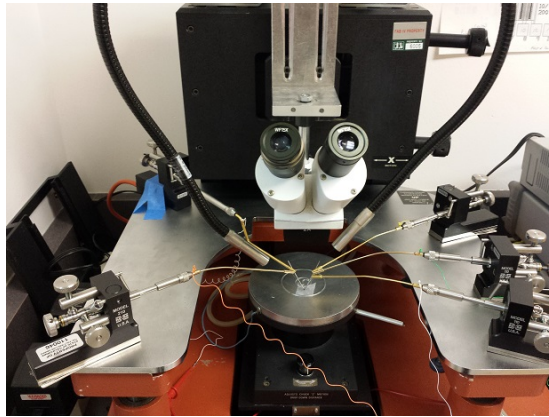
Figure 3.79: IC Pad Probing
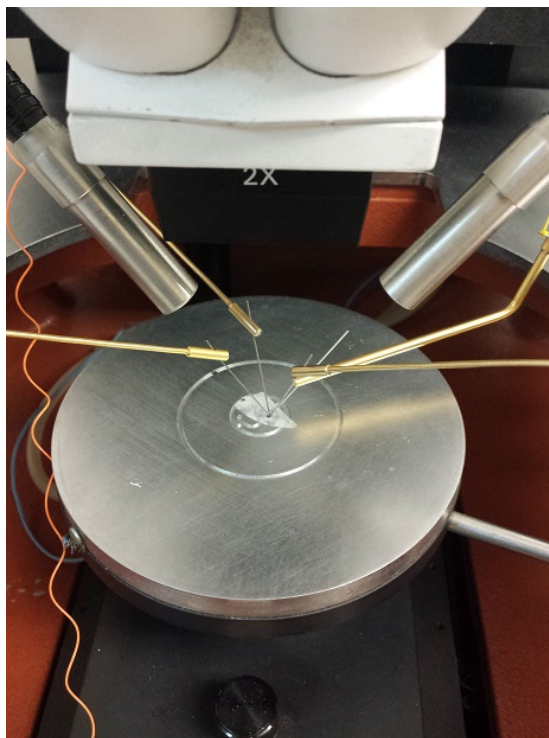
Figure 3.80: Close Up of Probes

The IC contains 5 IO pins - VDD, IN1, IN2, OUT, and GND and each IO has been connected to multiple pads in case I damaged some in the testing process. In addition to the IO pads, I have 6 accessible test points: TP1-TP6. Fig. 3.81 below shows a schematic view of the test point locations.
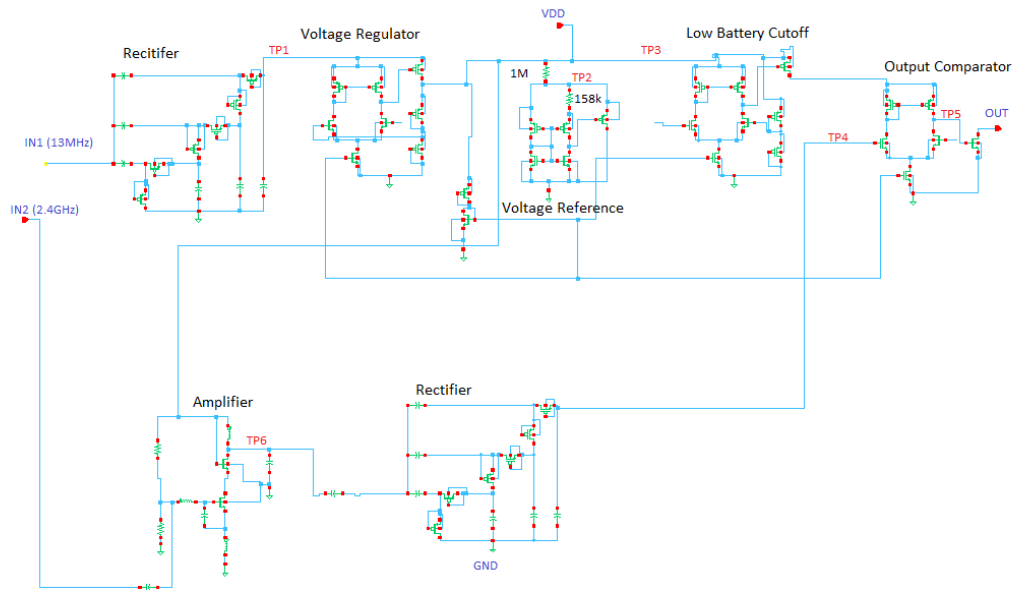
Figure 3.81: Probe Points

I first measured the output of the voltage reference, TP2. The voltage reference did not produce a voltage at TP2 when it was designed to output about 2.25V and sink around 1.5μA due to the 1MΩ resistor. If 2V is applied to TP2 and left VDD open, the voltage reference sinks 20 μA. The measured resistance between TP2 and VDD was 170kΩ instead of the designed 1MΩ resistance; that may explain the non-functioning voltage reference. In addition, the resistance between TP2 and ground was measured to be 500kΩ which eliminates the possibility of a short. Next, I tested the operation of the output comparator. I applied 3.8V to VDD and measured the output voltage at TP5 while stepping a DC voltage at the input TP4. The reference voltage was left unaltered. Fig. 3.82 shows the voltage transfer characteristic of the comparator.
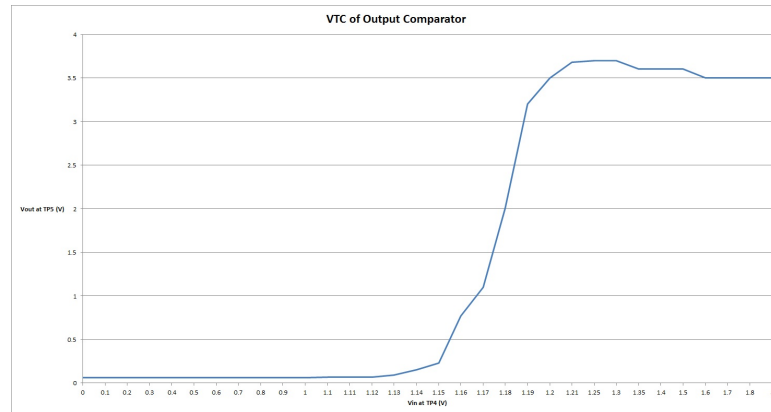
Figure 3.82: Output Comparator VTC

The transition point of the comparator can be approximated to be 1.18V. As previously stated, the VTC was obtained with an unaltered voltage reference of 0V. Thus, the output of the comparator should swing high when the input voltage is high enough to turn on the non-inverting transistor. Fig. 3.82 shows this effect as the input needs to be at least 1V to turn on the gate of the transistor. We can also use the VTC to confirm the current mirror's operation. Since the NMOS turns on with a 1.18V input even though V_{TH} is 1V, we can then say that V_{DS} of the NMOS for the tail current is 0.18V. Using the standard mosfet equation eq. 3.24:

$$I_{DS} = k\prime(W/L)(V_{DS})^2 \tag{3.24}$$

we can calculate the mirror bias current to be about 130nA which is slightly higher than the desired 100nA. This is just an approximation since V_{TH} may differ slightly between fabrication runs. I would suggest that a probe point be added at the gate of the tail NMOS transistor in order to obtain a more accurate measurement of the currrent mirror.

Next, I tested the operation of the voltage regulator. The purpose of the voltage regulator is to limit the charging voltage to 4.1V as specified by the datasheet. The output of the voltage regulator follows the input voltage until it reaches the desired maximum and then holds it at that value. To properly test the functionality of the regulator, a proper reference voltage must be established by applying 2V to TP2 in order to bias the regulator. Then, I stepped a voltage at

TP1 and measured the voltage at TP3.
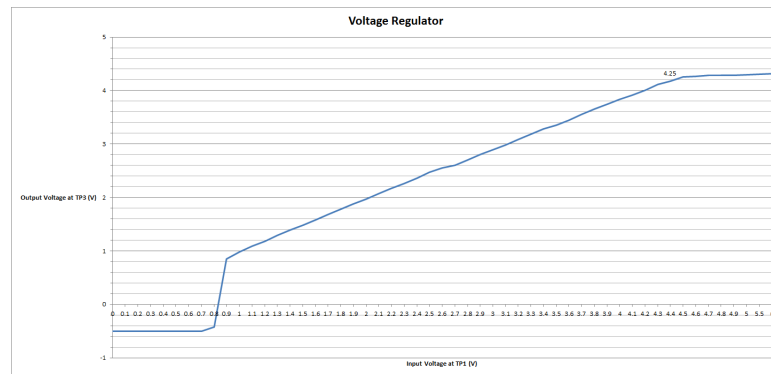
Figure 3.83: Voltage Regulator Waveform

Fig. 3.83 confirms that the voltage regulator operates correctly. The voltage regulator clamps the voltage at 4.2V which is slightly higher than the desired 4.1V.

Measuring the low battery cutoff was not as simple as the two previous components because I could not fit a test point right at the output of the battery cutoff circuitry. Instead, I applied 2V at TP4 in order to turn on the output comparator and measured TP5 as the output of the low battery cutoff. This was the best solution because if the comparator is on, then its output should follow the output of the low battery cutoff. The input of the low battery cutoff was applied at TP3. To test this component, I stepped the voltage at 3.8V down to 2V and measured the output voltage. Fig. 3.84 shows the obtained waveform.
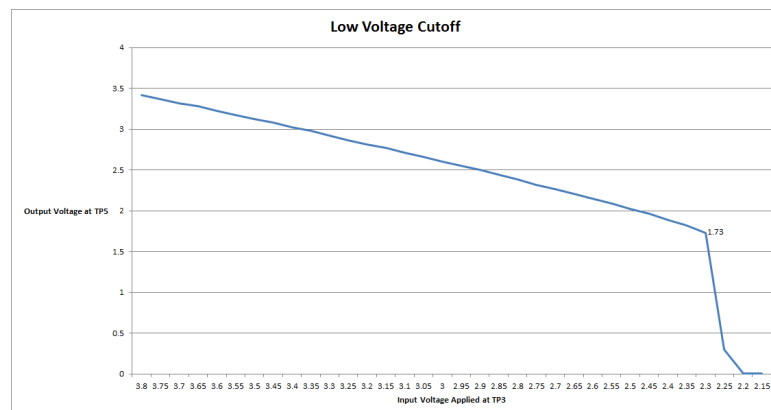
Figure 3.84: Low Battery Cutoff Waveform

The circuit did not cutoff the voltage until 2.3V when the specifications state 3.1V minimum.

The cause of this discrepancy is hard to pinpoint as I was not able to test the cutoff circuitry by itself. One explanation could be that the bias point created by the PMOS voltage divider may have shifted due to the fabrication - adding a test point there would have made debugging easier. However, the small IC area prevented me from fitting sufficient test points.

The 13MHz input rectifier was tested by inserting a sine wave to IN1 and measuring output at TP1. The rectifier did not perform as well as simulations. A 3-stage charge pump should produce a DC output that is 3 times larger than the amplitude of the input signal. However, the charge pump was barely able to rectifier the input to a useable DC voltage as shown in fig. 3.85 below.
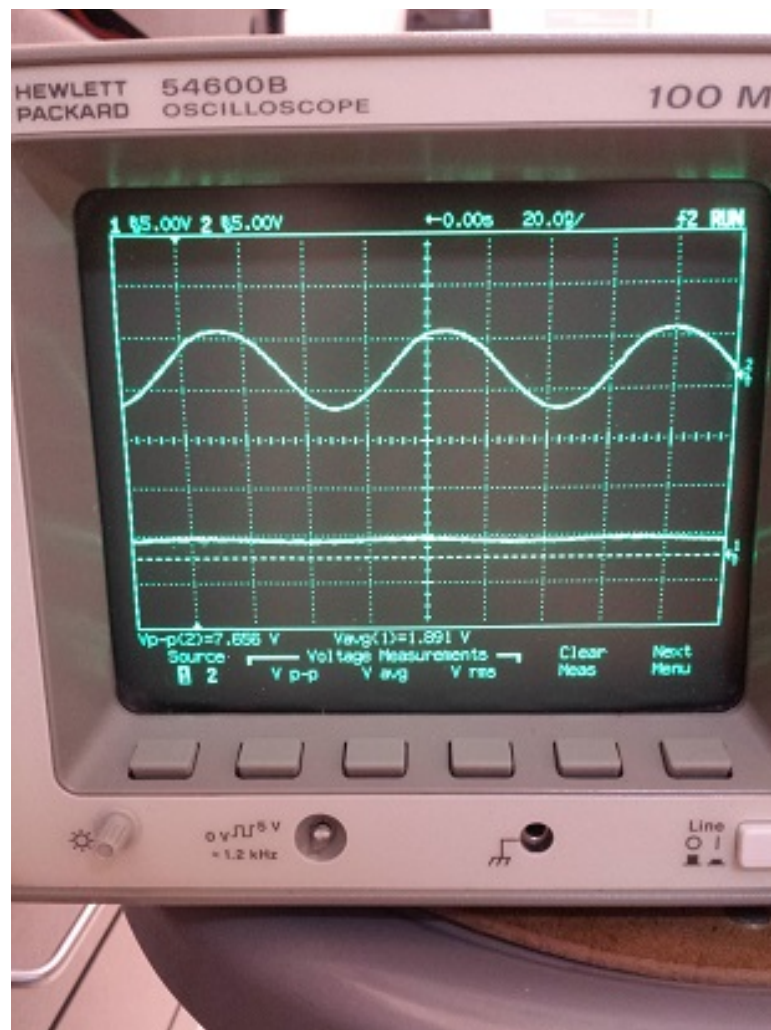
Figure 3.85: 10Vp Sinewave Input

The rectifier only produces a 1.89V DC value with 7.8Vpp, 13MHz sinusoidal source. The reason for this may be explained by the capacitors in each of the stages. In most processes, libraries for passive components such as resistors, capacitors, and inductors are usually provided by the fabricator. However, the C5 process did not provide layout libraries for the passive components. Thus, the capacitors were manually drawn in layout and the capacitance was estimated using the area of the overlapping layers. I believe that the actual capacitance was much lower than the desired capacitance which results in a lower output DC value. The transistors seem to be working properly as there are no visible waveform distortion at the output. However, the output waveforms must be acquired at different input frequencies in order to determine if the transistors are operating correctly.

THe 2.4GHz rectifier did have failed transistors which distorted both the input and output waveforms. To test the 2.4GHz rectifier, I sent the input signal at TP6 and probed the output at TP4. Fig. 3.86 below shows the distorted waveforms.
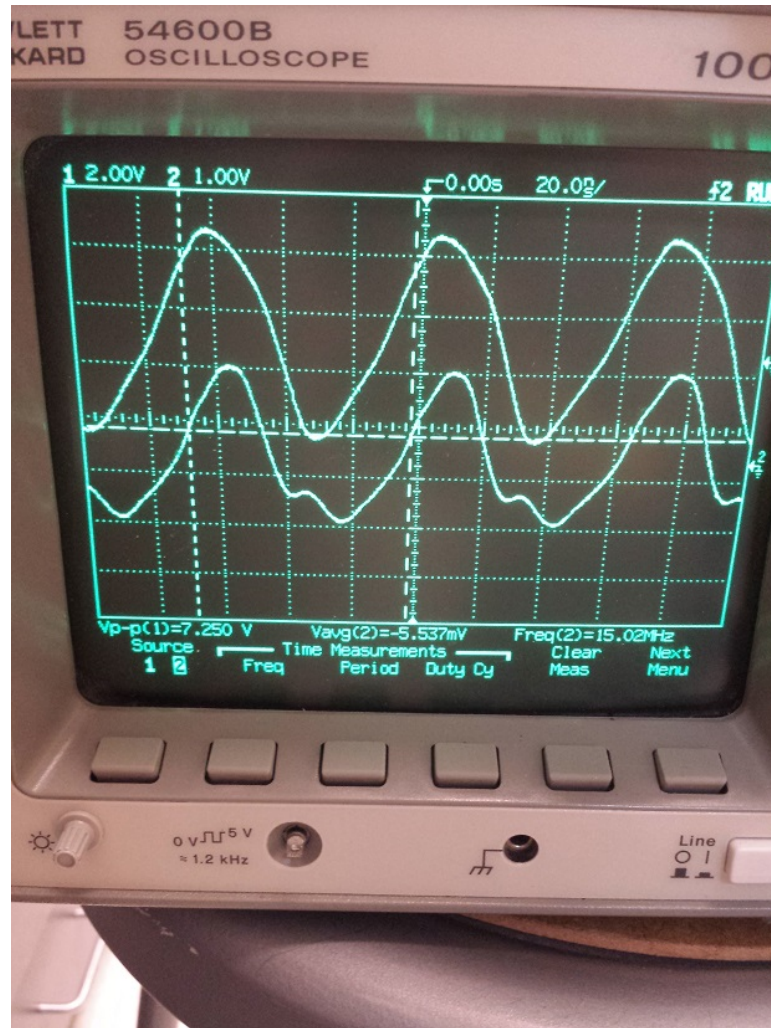
Figure 3.86: 10Vp 15MHz Sinusoid Input

The input signal is distorted because the rectifier loses the 50Ω input impedance due to the failed transistors. Also, the distortion may be caused by the series capacitor that was originally designed to be connected to ground. Another possibility could be that 15MHz exceeded the specifications of the transistors. To test this, I obtained the output waveform with a 1MHz input sinusoid and a 100KHz input sinusoid.
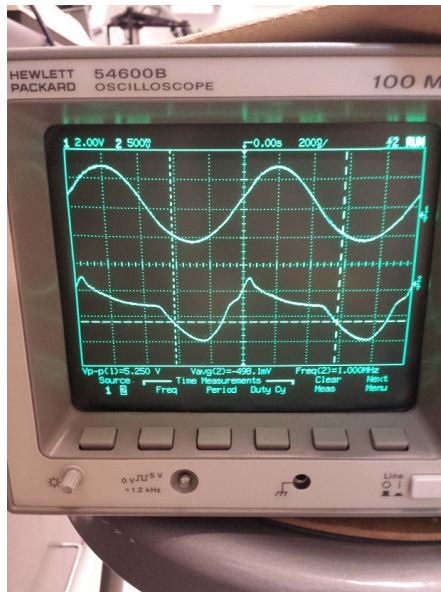
Figure 3.87: 10Vp 1MHz Sinusoid Input
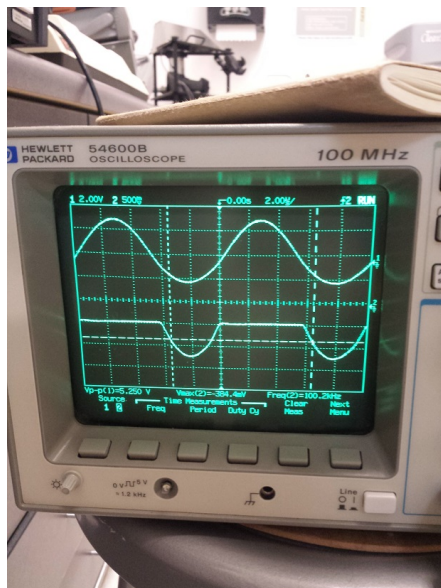
Figure 3.88: 10Vp 100KHz Sinusoid Input

As the frequency lowers, a negative DC value starts to appear. The DC voltage is negative because of amplifier's output capacitor which was mistakenly connected in series instead of to ground. Fig. 3.87 and 3.88 show that the rectifier had issues operating above 100KHz even though this issue did not surface during simulations at the schematic level. I believe that the reason the two rectifiers are not performing correctly are because of the capacitors.

The last component in the IC to be tested was the common-source amplifier. The microfabrication lab lacked a synthesizer and spectrum analyzer which was needed to test the amplifier's functionality. Therefore, future students planning to test high frequency ICs must transport those necessary equipment to the microfabrication lab. Also, the lab lacked proper SMA connections to the micromanipulators so connections to the test equipment were made using regular BNC to grabber connectors as shown in Fig. 3.89.
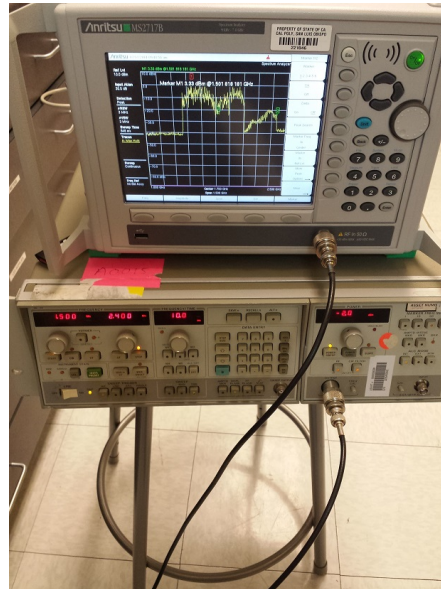
Figure 3.89: Test Equipment Setup for Amplifier Testing

Fig. 3.90 below shows the frequency response of the common source amplifier. The input signal was a -2dBm source with its frequency swept from 1.5GHz to 2.4GHz.

Figure 3.90: Frequency Response of Common Source Amplifier

The maximum gain of the amplifier seems to have been shifted to 1.59GHz. At 2.4GHz, the signal exceeds the bandwidth of the amplifier and becomes attenuated. These measurements may not show the true functionality of the amplifier as the long BNC to grabber cables contain large amounts of parasitics and loss at high frequencies. The shift in the actual frequency response from simulation may also be caused by the inductors and capacitors in the IC as their dimensions had to be manually drawn in layout to achieve their desired values. Therefore, the current setup shows a maximum gain of 6.65dB at 1.594 GHz.

ASSEMBLY

Originally, my plan was to wirebond the IC, battery, and antenna together in order to have a functional system. Dr. Smilkstein informed me that the IME department on campus had a wirebonding machine and she connected me with Dr. Pan for access. Dr. Pan was not able to help me bond the components nor provide training such that I could operate the machine myself. He was able to refer an external company named F&K Delvotec for additional assistance. They quoted me for $230 per hour and agreed to bond it in their facilities if I mail them the components. They also required CAD drawings of my bonding configuration when my IC arrived. Fig. 4.1 and 4.2 shows the bonding configurations for the coil antenna and the IFA.
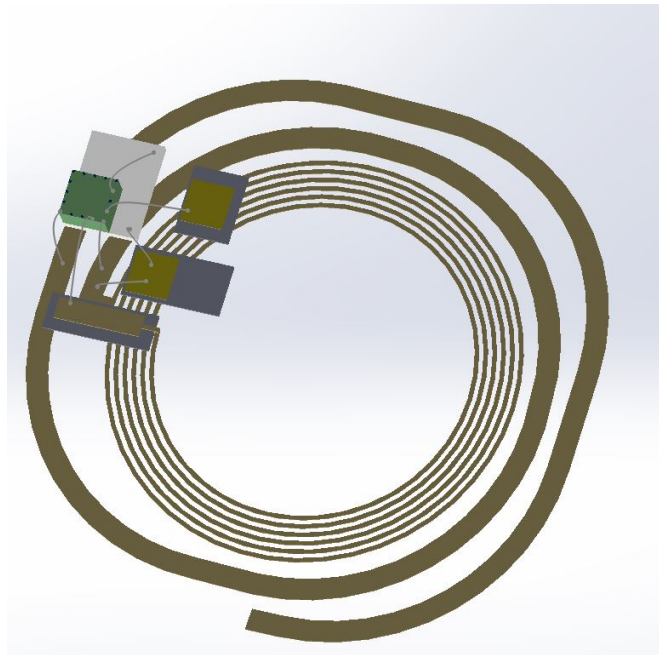
Figure 4.1: Bonding Configuration for Coil Antenna
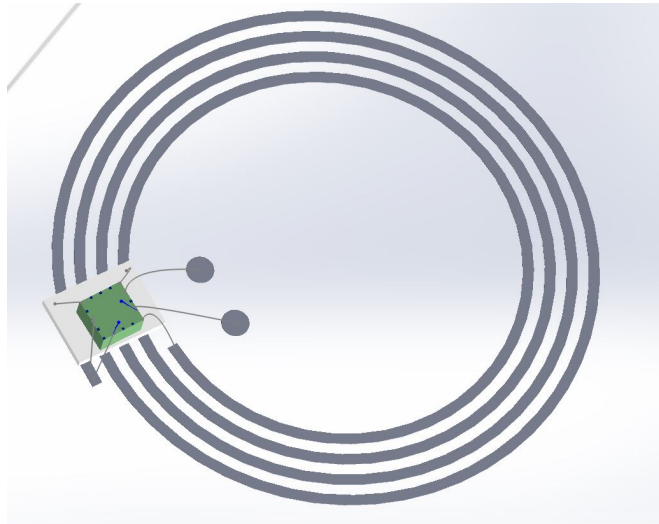
Figure 4.2: Bonding Configuration for IFA Antenna

I was not able to send them the components to be wirebonded due to unexpected delays with my IC. MOSIS originally estimated a 4-6 week fabrication time for my IC but they encountered a 1 month delay on their side. Therefore, I did not receive my IC and submit the CAD drawing to F&K Delvotec until July instead of June. F&K Delvotec reviewed the CAD drawings and concluded that they did not have the proper tip to bond at the required dimensions. They referred me to a company named Small Precision Tools to have the bonding capillary fabricated. SPT quoted me $250 for the part (part number CSA-33ES-CM-1/16-16mm). Unfortunately, the part required a 6 to 8 week lead time which meant that wirebonding would not occur until September. Therefore, the electrical assembly was not able to fit into the project's timeline due to these unexpected delays.

CHAPTER 5

ENCAPSULATION

The last step in the fabrication process was curving the lens to fit the eye's curvature and then encapsulating the PET substrate and circuitry for biocompatibility. With the help of Paul Heckler, we were able to adapt and apply the injection molding process to our contact lens. This process required several steps. First, we designed and fabricated a mold to curve the PET substrate. Since the PET film is a thermoplastic substrate, we could heat up the mold and press the PET into the desired curvature. We then placed the curved PET into a second mold in which we poured liquid PDMS. Once the PDMS cured, the entire lens was encapsulated.

5.1 Mold Design and Fabrication

The purpose of the mold, designed by Paul Heckler using SolidWorks, was to control the shape and thickness of the PDMS during its curing process. The lens fabrication process is a 3 step process and each step requires two molds, resulting in a total of 6 molds needed. Appendix B contains these mold drawings. The drawings were needed by the CNC machine in the machine shop on campus in order to mill out the design on a solid block of metal. The choice of metal for our mold was dictated by its thermal conductivity because the metal must be able to heat up in order to curve the PET and cure the PDMS. Ideally, we would use brass but our budget restricted us to use aluminum instead.

5.2 PET Curving

With the mold fabricated, we can now curve the PET substrate. The antenna must first be manually centered on the male side of the mold (Male Mold 1) and taped down in place. We then took the female mold 1 and placed it on top of the male mold. These two molds were then placed in the oven at 80 degrees C for 10 minutes. The oven used was the Jeio Tech ON-01E located in the specialty printing lab in the GRC building. The mold was then removed from the oven and left out for 15 minutes to cool. Once the mold was cool to the touch, we separated the

two molds and retrieved the curved PET.
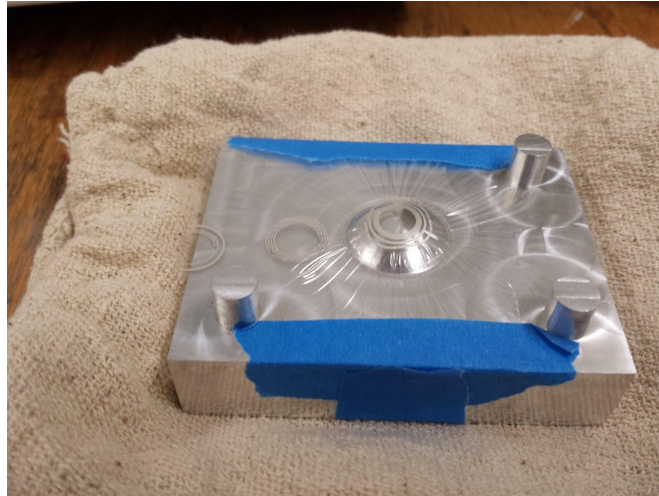
Figure 5.1: Curved PET

5.3 Encapsulation

The encapsulation process requires the use of 2 molds - 1 for each side of the lens. First, we pour PDMS into the female part of the second mold. In order to prevent bubbles from forming, the mold was placed in a degassing chamber after the PDMS had been poured.
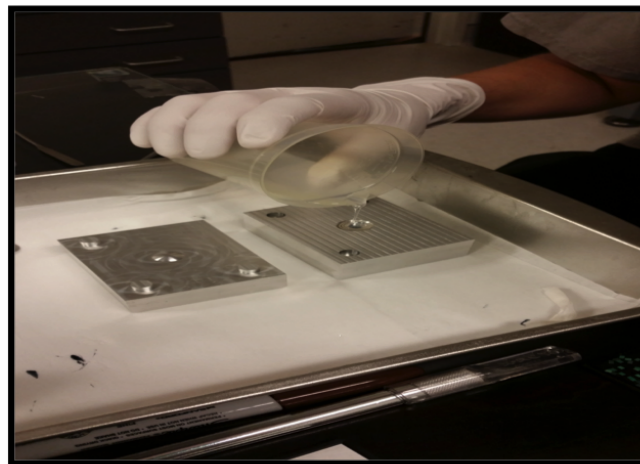
Figure 5.2: Pouring PDMS into Mold

The curved PET lens was then attached to the male part of the second mold and then placed onto the female mold which contained PDMS. The two molds were baked at 70 degrees C for 4 hours in order to cure the PDMS which created the convex PDMS layer. Then, we placed the

lens PDMS side down into the third female mold and poured PDMS on top of the exposed PET - forming a pool of PDMS. The male portion of the third mold is then inserted and the cavity between the male mold and lens creates a 50μm layer of PDMS on top. Again, the molds were placed back in the oven at 70 degrees C for 4 hours to let the PDMS cure and form the concave layer of the lens.
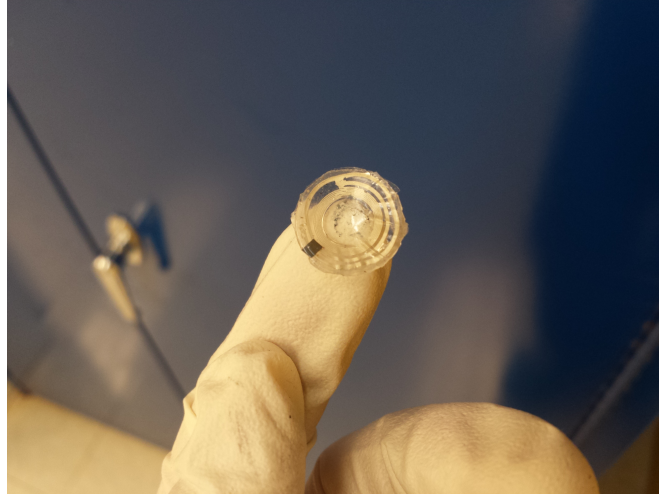
Figure 5.3: Encapsulated Contact Lens

5.4 Results

The curving process was not difficult as the substrate was moldable when heat was applied. However, the PET formed wrinkles because the mold was stretching the PET as it curved. Fortunately, the wrinkles were located towards the edge of the lens leaving the center smooth. We were able to trim the edges of the wrinkled PET without having to destroy the antenna. To prevent this in the future, the male mold should be larger such that the wrinkles would be pushed further away from the antenna.

The main challenge in the PDMS encapsulation process was separating the female and male molds after curing in the oven. We were not able to separate the molds by hand and had to pry them apart using a razor blade and hammer. When they were separated, we discovered that the excess PDMS was pushed out of the cavity where the lens was sitting and dried in between the male and female mold faces. After more research, we found that overflow was not uncommon in injection molding and could be solved by including an overflow chamber for the excess material.

Unfortunately, we did not have the funds or time to manufacture a new mold. In addition, the excess overflowed PDMS had to be removed from the lens. Our method of removal was to manually trim the excess PDMS using an exacto knife. This method is not precise and left rough edges. In the future, a separator that functions much like a cookie cutter should be manufactured to trim the excess PDMS. The resulting thickness of the contact lens was measured with calipers accurate to 3/1000th's of an inch. 15 points around the lens was measured to account for variance and a thickness of 800 μm was measured with a standard error of 71.12 μm (n = 15). When we calculated the thickness due to the stackup shown in fig. 2.4, we determined that the two PDMS layers contribute a total of about 300 μm of thickness. The reason for the thick PDMS layer could be caused by our mold design. The mold did not allow excess PDMS to funnel out of the cavity formed by the male and female counterparts. Therefore, when the two molds are placed together, the excess PDMS does not allow the two molds to fit tightly on top of each other leaving a gap between them. This gap caused by the excess PDMS could be the reason for the thick contact lens.

Phil Azar helped us test the comfortability of the contact lens. Since we could not conduct any animal testing with this device, we were not able to test the comfortability of the contact lens directly. We decided on an indirect method by measuring the wettability of the contact lens via contact angle testing. Contact lenses rely on the surface tension created by the eye's tear layer to keep it in place. A material with insufficient wettability will cause tears to improperly coat the contact lens and leave gaps of exposed PDMS causing irritation and blurry vision. Contact lenses require a contact angle of 65 degrees maximum for proper wettability. To test the contact angle of the PDMS contact lens, a VCA Optima contact angle system, saline, and DI water was used.
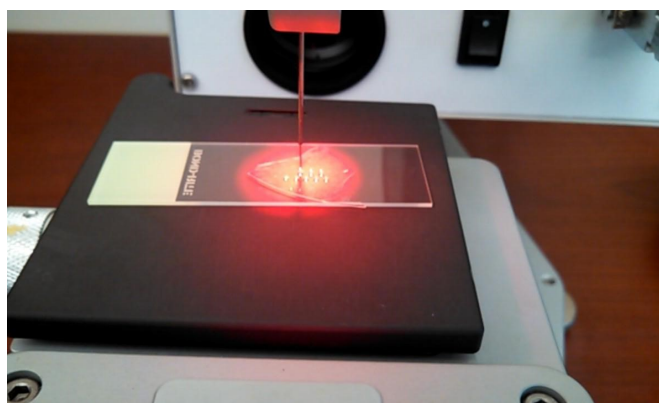
Figure 5.4: Contact Angle Testing using VCA Optima System

Figure 5.5 shows a contact angle of 105 degrees produced by the VCA Optima system.
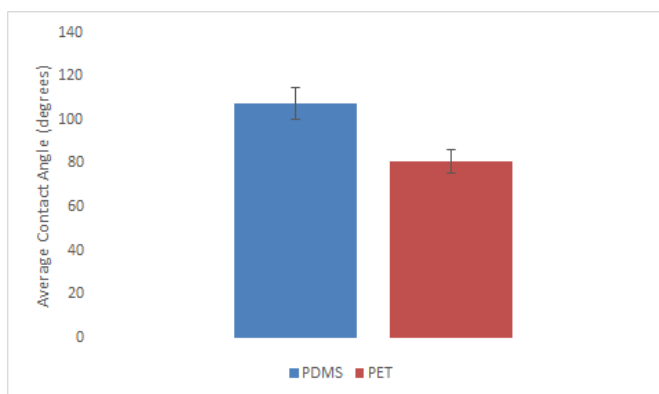
Figure 5.5: Bar Chart of Average Contact Angles for PET and PDMS, including standard error bars. (n = 15)

We can conclude from the results that while the PDMS contact lens is safe to wear, it would not be very comfortable for the user. The reason is that PDMS, while soft and biocompatible, is not very hydrophillic. A future remedy to this problem would be to switch to a silicon hydrogel material. Traditional silicon hydrogel contact lenses are cut from a solid block material which makes it difficult to apply to the surface of our PET lens. However, a patent was filed recently under the number WO2009073401 A2 which proposes a silicon hydrogel spray application. This type of application would allow us to spray this coating onto our contact lens and increase its comfortability.

We did not have proper resources on campus to test the lens's biocompatibility and breathability. While PET displays biocompatible qualities through both *in vivo* and *in vitro* tests [16][17],

longer *in vitro* tests to determine cell adhesion and cell toxicity properties would strengthen this conclusion. Cell adhesion tests involve colonizing the surface of the lens with cells and then washing them off a various time intervals. Cell toxicity tests involve placing the PDMS lens over a colony of living cells and bacterial. After allowing the PDMS to diffuse into the cell layer, we would observe any signs of cell death and use that as a metric for toxicity *in vitro*.

CHAPTER 6

CONCLUSION

Advancements in printing techniques allows us to adapt this technology for other fields, such as circuit board fabrication. The ability to screen print circuits on flexible and transparent substrates enables us to advance electronics in certain areas such as the biomedical industry. In this thesis, I undertook the fabrication of a circuit on a contact lens with the help of the screen printing from the Graphic Communications department. We printed two different types of antennas, a coil and IFA variation, that would provide inductive charging and also communicate at the 2.4GHz ISM band. The antennas were printed on 25 μm PET substrate with a silver conductive ink by Dupont. The coil antenna produced a S_{11} of -4.45 dB, a coil inductance of 268.2nH with a Q-factor of 0.98 and a gain of -13 dB. The IFA-based design produced a S_{11} of -9.582 dB, a coil inductance of 273.4 nH with a Q-factor of 0.269 and a gain of -5.3 dB. The battery chosen for our application was the CBC005 3.8V, 5μAh thin film battery by Cymbet. A custom IC was designed and fabricated by MOSIS using the On Semiconductor CMOS C5 0.6 μm process. The IC was designed to detect the incoming 2.4GHz signal, handle inductive charging via rectification and voltage limiting, and cutoff the IC from the battery when the battery voltage dropped below 3.1V. The display technology chosen was a single element printed display using electrochromic ink. The ink is originally clear but turns transparent blue when 3V was applied to it. Unfortunately, all the components could not be assembled together due to unforeseen delays in the wirebonding process due to their long lead times and from delays in the IC fabrication schedule from MOSIS.

There were many unforeseen setbacks during the course of this thesis. The first major setback was the lack of layout libraries for the passive (capacitor, resistor, and inductor) components. This should be kept in mind if future projects are done using ON SEMICONDUCTOR's C5 process. The wirebonding process also had its own setbacks. The wirebonding facility did not inform us that they needed a custom capillary tip until very late in the project. That that point,

we did not have the funds or timeline to obtain a new tip. I would advise that if future projects were to have FK Delvotech wirebond their ICs, then a 3D model should be provided to them early in the project to check if the dimensions are within their tolerances.

CHAPTER 7

FUTURE WORKS

Many design aspects of this thesis can be improved on in future projects continued at Cal Poly.

Since this project encompasses multiple fabrication techniques and disciplines, there was not

enough time to build and test different revisions past our first prototypes. Improvements to each

subsystem can be investigated individually, but one should be mindful of how change may affect

the rest of the system. For example, switching to a higher capacity battery may increase the

wireless communication distance of the device, but may risk the device running hotter than it

should. This chapter discusses improvements this project that either we briefly test and warrants

further investigation, or ideas that spawned from our lessons learned.

7.1 Electrical

The design of my common source amplifier could be improved to consume less power and make

the battery last longer. Since the addition of the amplifier was made late into the project, I did

not have time to build and simulate a more complex design. One technique that I briefly

investigated was a subthreshold amplifier design. Lee *et al.* [18] utilizes a typology that closely

resembled the current LNA design in this thesis. Circuit designs that bias MOSFETS in the

subthreshold region require tight process tolerances as well as accurate biasing. However, if

ultra-low power design could be achieved, then we could deviate away from battery powered

systems and possibly use other energy harvesting techniques.

7.2 Printing and Materials

I briefly tested multiple different fabrication techniques in parallel with the screen printing. One

of those was microfluidics. The theory behind using microfluidics is that screen printing requires

printing on a substrate that has good ink adhesion - which many biocompatible substrates are

not. Using microfluidics, the antenna design could be etched out in the form of channels and

flow the ink through. We tried this technique on a PDMS substrate and was able to flow in a

channel that was 100um wide and 25um thick. The viscosity of the ink poses a problem when trying to flow the ink through more narrow channels. This concern can be addressed two ways: 1. We could alter the ink, such as adding alcohols, to lower it viscosity or 2. Add more vias for the microfluidics nozzle such that more force could be applied to push the ink through. Future projects could also employ different types of ink other than silver. At the beginning of the project, I ordered a clear conductive ink, Henkel ECI-5001, to be used for the antenna design - unfortunately, the ink did not arrive in time. Having a clear conductive ink allows us to alter the antenna design such that its features can run across the users vision. For example, we would not have to open up the ground plane in the IFA design in Ch. 3 which will increase the efficiency of the antenna. The transparent ink may also allow future coil designs to incorporate more turns to achieve a higher inductance.

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A   Datasheets

CYMBET™ CORPORATION

Preliminary

EnerChip™ CBC005

Rechargeable Energy Storage Device: 5µAh, 3.8V

Features
- All Solid State Construction
- Designed for Wirebond Attachment
- Lead-Free Reflow Tolerant
- Thousands of Recharge Cycles
- Low Self-Discharge
- Fast Recharge
- Eco-Friendly, RoHS-Compliant
- Smallest Commercially Available Rechargeable Energy Storage Device
- Flat Output Voltage Profile
- Wire Bond or Solder Bump attachment

Electrical Properties
Output voltage (nominal): 3.8V
Capacity (nominal):   5µAh
Charging source: 4.1V
Recharge time to 80%:   15 minutes
Charge/discharge cycles: >5000 at 10% discharge

Physical Properties
Die size (mm):   1.7 x 2.25 x 0.175
Operating temperature: -20°C to 70°C
Storage temperature: -40°C to 125°C

Applications
- **Standby supply** for non-volatile SRAM, real-time clocks, controllers, supply supervisors, and other system-critical components.
- **Portable devices** requiring ultra-slim profile and small footprint backup power source.
- **Localized power source** to keep microcontrollers and other devices alert in standby mode.
- **Power bridging** to provide backup power to system during exchange of main battery.

Bare die CBC005 suitable for wirebonding.
Dimensions: 1.7mm x 2.25mm x 0.175mm.
[Not to scale.]

The EnerChip™ CBC005 is a solid state, thin film, rechargeable energy storage device rated at 5µAh at 3.8V. It is ideal as a localized on-board power source to retain memory or maintain real-time clock function in mobile systems when main power is interrupted. The CBC005 is the smallest rechargeable energy storage device available to Original Equipment Manufacturers (OEMs) and is a superior alternative to button and coin cell batteries and super-capacitors in handheld devices.

Board mounting area of the CBC005 is less than 1/2 the area of a 1210 (3225 metric) surface mount device and less than 1/4 the thickness. Such dimensions make the CBC005 ideal for space-constrained applications.

Because of their solid state design, EnerChip™ energy storage devices are able to withstand solder reflow temperatures and can be processed in high-volume manufacturing lines similar to conventional semiconductor devices. In contrast to traditional rechargeable batteries and super-capacitors, there are no harmful gases, liquids or special handling procedures associated with the EnerChip™.

The CBC005 is based on a patented, all solid state, rechargeable lithium cell with a nominal 3.8V output. Recharge is fast and simple with a direct connection to a 4.1V voltage source and no current limiting components required. Recharge time is 15 minutes to 80% capacity. A robust design offers thousands of charge/discharge cycles. The CBC005 is delivered as a 1.7mm x 2.25mm x 0.175mm bare die with two wirebondable pads for co-packaging with other components or chip-on-board mounting. Die are shipped in tape-and-reel, waffle packs, and trays.

Preliminary

EnerChip™ CBC005 Energy Storage Device

Operating Characteristics

| Parameter		Condition	Min	Typical	Max	Units
Discharge Cutoff Voltage		25°C	3.0[1]	-	-	V
Charge Voltage		25°C	4.0[2]	4.1	4.2	V
Self-Discharge (average; 25°C)		Non-recoverable	-	2.5	-	% per year
		Recoverable	-	1.5[3]	-	% per year
Operating Temperature		-	-20	-	+70	°C
Storage Temperature		-	-40	-	+125[4]	°C
Cell Resistance (25°C)		Charge cycle 2	-	7	11	KΩ
		Charge cycle 1000	-	31	48	
Recharge Cycles (to 80% of rated capacity; 4.1V charge voltage)	25°C	10% depth-of-discharge	5000	-	-	cycles
		50% depth-of-discharge	1000	-	-	cycles
	40°C	10% depth-of-discharge	2500	-	-	cycles
		50% depth-of-discharge	500	-	-	cycles
Recharge Time (to 80% of rated capacity; 4.1V charge voltage)		Charge cycle 2	-	11	22	minutes
		Charge cycle 1000	-	45	70	
Discharge Capacity		400nA discharge; 25°C	5.0	-	-	µAh

[1] *Failure to cutoff the discharge voltage at 3.0V will result in cell performance degradation.*

[2] *Charging at 4.0V will charge the cell to approximately 70% of its rated capacity.*

[3] *First month recoverable self-discharge is 5% average.*

[4] *Storage temperature is specified for uncharged EnerChip.*

Note: All specifications contained within this document are subject to change without notice.
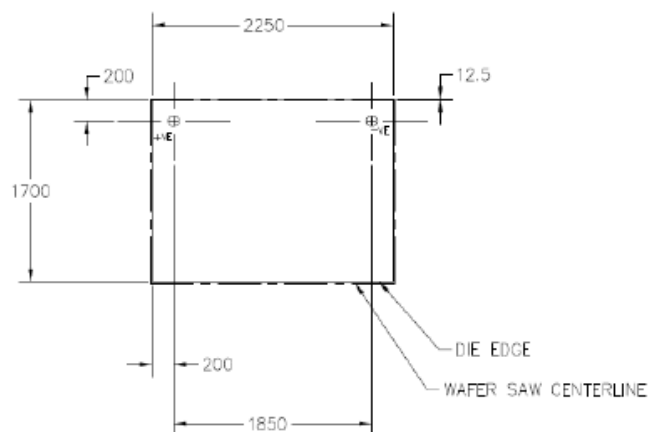

Typical CBC005 EnerChip Discharge Characteristics
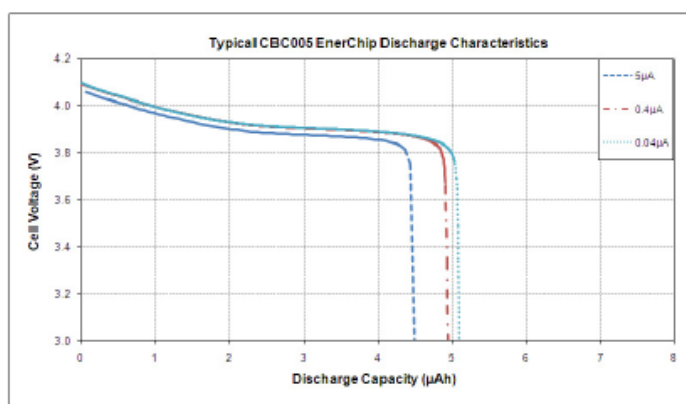
Preliminary **EnerChip™ CBC005 Energy Storage Device**

CBC005 Bare Die Dimensions

NOTES:
1. ALL DIMENSIONS IN MICRONS

DETAIL OF PAD OPENING

Ordering Information

EnerChip Part Number	Description	Notes
CBC005-BDC-WP	5µAh EnerChip Bare Die, Waffle Pack	Contact Cymbet
CBC005-BUC-WP	5µAh EnerChip Bare Die Solder Bumped, Waffle Pack	Contact Cymbet

Appendix A: Datasheets

DuPont 5025
SILVER CONDUCTOR

Technical Data Sheet

Product Description
DuPont 5025 silver conductor is used to fabricate low voltage circuitry, especially on flexible substrates. It can be used with manual, semi-automatic, and reel-to-reel equipment.

Product Benefits
- Best general purpose Ag for higher temperature operations

Processing
- **Screen Printing Equipment**
  Reel-to-reel, Semiautomatic, manual

- **Substrates**
  Polyester, polyimide, paper, epoxy glass

- **Ink Residence Time on Screen**
  > 2 hours

- **Screen Types**
  Stainless steel, Polyester

- **Typical Cure Conditions**
  Box Oven: 120°C for 5 - 6 minutes
  Reel-to-reel: 140°C for 1 minute

- **Typical Circuit Line Thickness Printed with 325-mesh stainless steel screen**
  12 - 15 microns

- **Clean-up Solvent**
  Ethylene diacetate or methyl propasol acetate

Table 1
Typical Physical Properties on 5-mil Polyester Film

Test	Properties
Sheet Resistivity (mΩ/sq/mil)*	12 - 15
Resistivity after Flex (mΩ/sq/mil) 15 sec after test Crease (180°, 1 cycle)	≤ 50
Adhesion/Tape Pull (3M Scotch Tape #600)	No Ag Transfer
Abrasion Resistance, Pencil Hardness (ASTM D3363-74) [H]	≥1
Operating Use Temperature (°C)	≤ 110
Solderability	Not Recommended
Change is Physical Properties after Environment Test *	Insignificant
Change is Physical Properties after Environment Test * (%)	<10

* Environmental Tests
- Thermal Shock (+85°C to -40°C, 30 min. each, 5 cycles)
- Dry Heat (+85°C, 20 days)
- Humidity (+60°C, 95% RH, 10 days) [MIL Std 202E, method 103, cond. A]
- Salt Spray (+35°C, 5% salt, 10 days) [ASTM B117]
- Silver Migration (1 V DC/mil gap, +40°, 90% RH, 500 hr, tested on 40 and 70-mil gaps)
- Sulfate Dioxide (+45°C, 90% RH, 500 hrs in a 9-liter chamber containing 500 mg of flowers of sulfur)

Table 1 & 2 show anticipated typical physical properties for DuPont 5025 based on specific controlled experiments in our labs and are not intended to represent the product specifications, details of which are available upon request.

Appendix A: Datasheets

Test	Properties
Table 2 **Composition Properties**	
Viscosity (Pa.S) [Brookfield 0.5RVT, 5rpm #14, 25°C]	20 - 30
Solids (150°C) [%]	68 - 72
Coverage (cm²/g) [Dependent on print thickness]	230 - 320
Thinner	DuPont 8210

Dry
Dry and cure in a well ventilated oven or conveyor dryer where the exhaust meets environmental regulations.

Storage and Shelf Life
Containers should be stored, tightly sealed, in a clean, stable environment at room temperature (<25°C). Shelf life of material in unopened containers is six months from date of shipment. Some settling of solids may occur and compositions should be thoroughly mixed prior to use.

Safety and Handling
For Safety and Handling information pertaining to this product, read the Material Safety Data Sheet (MSDS).

For more information on DuPont 5025 or other DuPont Microcircuit Materials products, please contact your local representative:

Americas
DuPont Microcircuit Materials
14 T.W. Alexander Drive
Research Triangle Park, NC 27709
Tel.: 800-284-3382

Europe
Du Pont (U.K.) Limited
Coldharbour Lane
Bristol BS16 1QD
U.K.
Tel.: 44-117-931-3191

Asia
DuPont Kabushiki Kaisha
Sanno Park Tower, 11-1
Nagata-cho 2-chome
Chiyoda-ku, Tokyo 100-611
Japan
Tel.: 81-3-5521-8650

DuPont Taiwan Ltd
45, Hsing-Pont Road,
Taoyuan, Taiwan 330
Tel.: 886-3-377-3616

DuPont China Holding Co. Ltd
Bldg 11, 399 Keyuan Rd., Zhangji Hi-Tech Park,
Pudong New District, Shanghai 201203, China
Tel.: 86-21-6386-6366 ext.2202

DuPont Korea Inc.
3~5th Floor, Asia tower #726,
Yeoksam-dong, Gangnam-gu
Seoul 135-719, Korea
Tel.: 82-10-6385-5399

E. I. DuPont India Private Limited
7th Floor, Tower C, DLF Cyber Greens,
Sector-25A, DLF City, Phase-III,
Gurgaon 122 002 Haryana, India
Tel.: 91-124-4091818

Du Pont Company (Singapore) Pte Ltd
1 HarbourFront Place, #11-01
HarbourFrong Tower One,
Singapore 098633
Tel.: 65-6586-3022
http://mcm.dupont.com

MCM5025 (09/2014)

DUPONT®

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Appendix A: Datasheets

```
                        MOSIS WAFER ELECTRICAL TESTS

            RUN: V37P                              VENDOR: AMIS (ON-SEMI)
      TECHNOLOGY: SCN05                        FEATURE SIZE: 0.5 microns
                           Run type: SHR


INTRODUCTION: This report contains the lot average results obtained by MOSIS
              from measurements of MOSIS test structures on each wafer of
              this fabrication lot. SPICE parameters obtained from similar
              measurements on a selected wafer are also attached.

COMMENTS: SMSCN3ME06_ON-SEMI


TRANSISTOR PARAMETERS      W/L      N-CHANNEL P-CHANNEL  UNITS

 MINIMUM                  3.0/0.6
  Vth                                  0.76      -0.90  volts

 SHORT                   20.0/0.6
  Idss                                 466       -255   uA/um
  Vth                                  0.65      -0.88  volts
  Vpt                                  13.1      -12.2  volts

 WIDE                    20.0/0.6
  Ids0                               < 2.5     < 2.5    pA/um

 LARGE                    50/50
  Vth                                  0.67      -0.94  volts
  Vjbkd                                10.9      -11.8  volts
  Ijlk                                 242.7    <50.0   pA
  Gamma                                0.49       0.56  V^0.5

 K' (Uo*Cox/2)                         57.8      -18.9  uA/V^2
 Low-field Mobility                   472.03    154.35  cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask
          bias use the appropriate value for the parameter XL in your
          SPICE model card.
                      Design Technology              XL (um)  XW (um)
                      -----------------              -------  ------
                      SCMOS_SUBM (lambda=0.30)         0.10     0.00
                      SCMOS  (lambda=0.35)             0.00     0.20


FOX TRANSISTORS           GATE     N+ACTIVE  P+ACTIVE  UNITS
  Vth                     Poly       >15.0    <-15.0   volts
```

```
COMMENTS:


PROCESS PARAMETERS      N+     P+    N_W    _U  POLY PLY2_HR   POLY2    M1   UNITS
  Sheet Resistance      82.4 106.7  814.1  23.2 1076          40.8    0.09  ohms/sq
  Contact Resistance    59.6 152.5         16.0              26.0          ohms
  Gate Oxide Thickness 141                                                 angstrom


PROCESS PARAMETERS             M2       M3    N_W       UNITS
  Sheet Resistance            0.09     0.05   808       ohms/sq
  Contact Resistance          0.84     0.82             ohms


CAPACITANCE PARAMETERS  N+    P+    POLY   POLY2    M1   M2   M3   N_W   UNITS
  Area (substrate)      416   710    86            29   12    8    91   aF/um^2
  Area (N+active)                  2456            37   17   12         aF/um^2
  Area (P+active)                  2362                                 aF/um^2
  Area (poly)                              922     64   16    9         aF/um^2
  Area (poly2)                                     58                   aF/um^2
  Area (metal1)                                         32   12         aF/um^2
  Area (metal2)                                              32         aF/um^2
  Fringe (substrate)    345   236                  51   34   26         aF/um
  Fringe (poly)                                    70   39   28         aF/um
  Fringe (metal1)                                       49   33         aF/um
  Fringe (metal2)                                            55         aF/um
  Overlap (N+active)                191                                 aF/um
  Overlap (P+active)                234                                 aF/um


CIRCUIT PARAMETERS                       UNITS
  Inverters                   K
   Vinv                      1.0     2.02  volts
   Vinv                      1.5     2.29  volts
   Vol (100 uA)              2.0     0.47  volts
   Voh (100 uA)              2.0     4.48  volts
   Vinv                      2.0     2.47  volts
   Gain                      2.0    -17.59
  Ring Oscillator Freq.
   DIV256 (31-stg,5.0V)            103.03  MHz
   D256_WIDE (31-stg,5.0V)         158.86  MHz
  Ring Oscillator Power
   DIV256 (31-stg,5.0V)              0.48  uW/MHz/gate
   D256_WIDE (31-stg,5.0V)           0.99  uW/MHz/gate

COMMENTS: SUBMICRON
```

```
V37P SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Oct 17/13
* LOT: v37p                    WAF: 1003
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                               LEVEL    = 49
+VERSION = 3.1          TNOM    = 27             TOX      = 1.41E-8
+XJ       = 1.5E-7      NCH     = 1.7E17         VTH0     = 0.6176544
+K1       = 0.9137986   K2      = -0.1071877     K3       = 22.288867
+K3B      = -9.7485086  W0      = 2.658488E-8    NLX      = 1E-9
+DVT0W    = 0           DVT1W   = 0              DVT2W    = 0
+DVT0     = 0.8309419   DVT1    = 0.3317542      DVT2     = -0.5
+U0       = 460.0124125 UA      = 2.759471E-13   UB       = 1.603084E-18
+UC       = 3.089014E-12 VSAT   = 1.840576E5     A0       = 0.5615191
+AGS      = 0.1204319   B0      = 1.941274E-6    B1       = 5E-6
+KETA     = -2.797385E-3 A1     = 2.420581E-5    A2       = 0.3164714
+RDSW     = 1.115544E3  PRWG    = 0.0828351      PRWB     = 0.0311852
+WR       = 1           WINT    = 2.526685E-7    LINT     = 7.469087E-8
+XL       = 1E-7        XW      = 0              DWG      = -1.032244E-8
+DWB      = 1.914595E-8 VOFF    = -6.986376E-5   NFACTOR  = 0.8533219
+CIT      = 0           CDSC    = 2.4E-4         CDSCD    = 0
+CDSCB    = 0           ETA0    = 2.045973E-3    ETAB     = -3.21453E-4
+DSUB     = 0.0833302   PCLM    = 2.3615569      PDIBLC1  = 9.500103E-5
+PDIBLC2  = 1.863456E-3 PDIBLCB = 0.0644698      DROUT    = 1.39184E-3
+PSCBE1   = 3.853855E8  PSCBE2  = 4.115782E-6    PVAG     = 0
+DELTA    = 0.01        RSH     = 82.4           MOBMOD   = 1
+PRT      = 0           UTE     = -1.5           KT1      = -0.11
+KT1L     = 0           KT2     = 0.022          UA1      = 4.31E-9
+UB1      = -7.61E-18   UC1     = -5.6E-11       AT       = 3.3E4
+WL       = 0           WLN     = 1              WW       = 0
+WWN      = 1           WWL     = 0              LL       = 0
+LLN      = 1           LW      = 0              LWN      = 1
+LWL      = 0           CAPMOD  = 2              XPART    = 0.5
+CGDO     = 1.91E-10    CGSO    = 1.91E-10       CGBO     = 1E-9
+CJ       = 4.131634E-4 PB      = 0.8399766      MJ       = 0.4305505
+CJSW     = 3.400072E-10 PBSW   = 0.809471       MJSW     = 0.1977865
+CJSWG    = 1.64E-10    PBSWG   = 0.8            MJSWG    = 0.2019414
+CF       = 0           PVTH0   = -0.028514      PRDSW    = 114.6437024
+PK2      = -0.0768747  WKETA   = -0.0138828     LKETA    = 1.62687E-3        )
*
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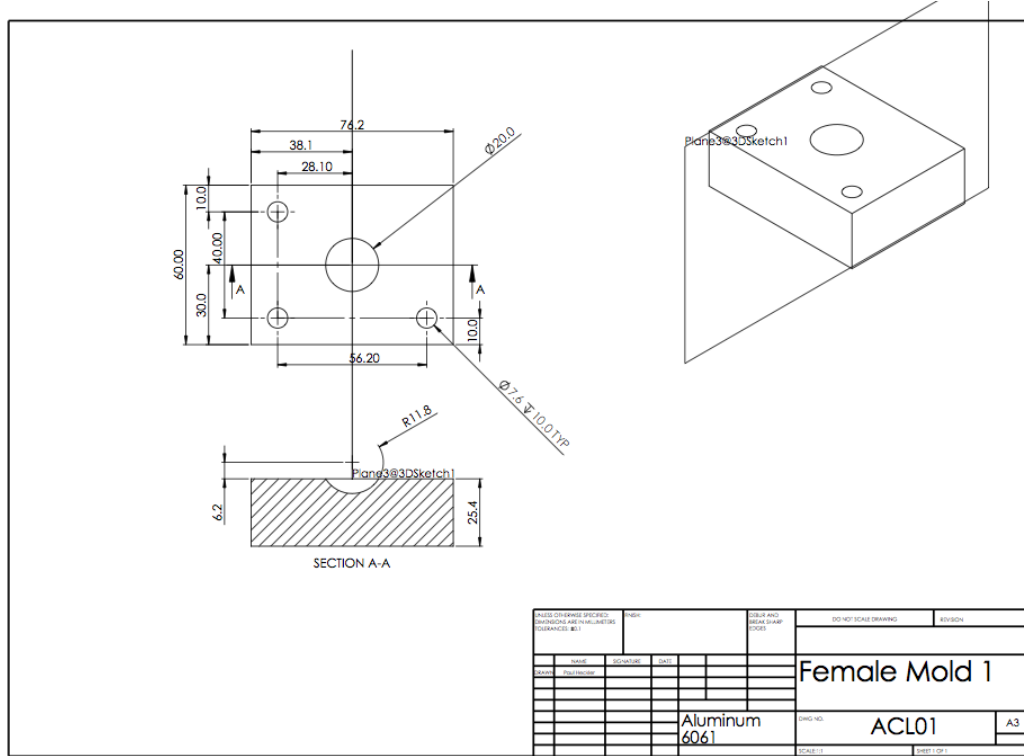
Appendix A: Datasheets

```
.MODEL CMOSP PMOS (                                              LEVEL    = 49
+VERSION = 3.1            TNOM    = 27              TOX      = 1.41E-8
+XJ      = 1.5E-7         NCH     = 1.7E17          VTH0     = -0.9152268
+K1      = 0.553472       K2      = 7.871921E-3     K3       = 8.5645893
+K3B     = 0.5506188      W0      = 1E-8            NLX      = 1.006451E-9
+DVT0W   = 0              DVT1W   = 0               DVT2W    = 0
+DVT0    = 0.4716221      DVT1    = 0.1854949       DVT2     = -0.3
+U0      = 201.3603195    UA      = 2.48572E-9      UB       = 1.005454E-21
+UC      = -1E-10         VSAT    = 1.578444E5      A0       = 0.8192884
+AGS     = 0.1111278      B0      = 5.743519E-7     B1       = 6.088988E-8
+KETA    = -4.865785E-3   A1      = 5.800723E-4     A2       = 0.3229711
+RDSW    = 3E3            PRWG    = -0.0219603      PRWB     = -0.0910566
+WR      = 1.01           WINT    = 2.247043E-7     LINT     = 9.979797E-8
+XL      = 1E-7           XW      = 0               DWG      = 2.080226E-9
+DWB     = -1.38669E-8    VOFF    = -0.0295318      NFACTOR  = 0.5872216
+CIT     = 0              CDSC    = 2.4E-4          CDSCD    = 0
+CDSCB   = 0              ETA0    = 4.979072E-4     ETAB     = -0.2
+DSUB    = 1              PCLM    = 2.3970968       PDIBLC1  = 0.0961044
+PDIBLC2 = 4.073922E-3    PDIBLCB = -0.0315594      DROUT    = 0.2897615
+PSCBE1  = 8E10           PSCBE2  = 8.966681E-8     PVAG     = 0.0149129
+DELTA   = 0.01           RSH     = 106.7           MOBMOD   = 1
+PRT     = 0              UTE     = -1.5            KT1      = -0.11
+KT1L    = 0              KT2     = 0.022           UA1      = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11        AT       = 3.3E4
+WL      = 0              WLN     = 1               WW       = 0
+WWN     = 1              WWL     = 0               LL       = 0
+LLN     = 1              LW      = 0               LWN      = 1
+LWL     = 0              CAPMOD  = 2               XPART    = 0.5
+CGDO    = 2.34E-10       CGSO    = 2.34E-10        CGBO     = 1E-9
+CJ      = 7.086018E-4    PB      = 0.8698912       MJ       = 0.4856488
+CJSW    = 2.340641E-10   PBSW    = 0.8329387       MJSW     = 0.2034305
+CJSWG   = 6.4E-11        PBSWG   = 0.8             MJSWG    = 0.2261452
+CF      = 0              PVTH0   = 5.98016E-3      PRDSW    = 14.8598424
+PK2     = 3.73981E-3     WKETA   = 0.0120657       LKETA    = -0.0104163    )
*
```

B Drawings

SECTION A-A

Female Mold 2
Aluminum
ACL02
A3

SECTION A-A

Female Part 3
Aluminum
ACL03
A3

Appendix B: Drawings

Male Part 1

ACL04

A3

Male Part 2

Aluminum 6061

ACL05

A3

Appendix B: Drawings

76.2
38.1
28.1
28.1
10
60
10
Ø6.0 TYP
Ø11.4
Plane3@3DSketch1

Plane3@3DSketch1
5
17.4
17.4
5
Ø20.8
Plane3@3DSketch1

	NAME	SIGNATURE	DATE			Male Part 3		
DRAWN								
CHK'D								
APPV'D								
MFG								
Q.A				Aluminum 6061		DWG. NO. ACL06		A3

DO NOT SCALE DRAWING   REVISION

WEIGHT   SCALE:1:1   SHEET 1 OF 1