

THE DEVELOPMENT OF A HIGH-PERFORMANCE DISTRIBUTED BATTERY
MANAGEMENT SYSTEM FOR LARGE LITHIUM ION PACKS

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by
Christopher Grasberger
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COMMITTEE MEMBERSHIP

TITLE: The Development of a High-Performance Distributed
Battery Management System for Large Lithium Ion Packs

AUTHOR: Christopher Grasberger

DATE SUBMITTED: June 2015

COMMITTEE CHAIR: Dr. Dale Dolan, Ph.D
Associate Professor
Dept. of Electrical Engineering

COMMITTEE MEMBER: Dr. Taufik, Ph.D
Professor, Director of Electric Power Institute
Dept. of Electrical Engineering

COMMITTEE MEMBER: Dr. Ali Shaban, Ph.D
Professor
Dept. of Electrical Engineering

ABSTRACT

The Development of a High-Performance Distributed Battery Management System for Large Lithium Ion Packs

Christopher Grasberger

A high performance battery management system (BMS) for large capacity cells was designed, built, and tested in a cycle of three revisions. The BMS was designed for use in applications where the battery pack configuration is unknown: parallel, series, or any combination. Each of the cells is equipped with its own battery management system to allow a peer-to-peer mesh network to monitor the safety of the cell. The BMS attached to each cell also is equipped with a 25A DC/DC converter to perform active balancing between cells in a string. This converter can transfer charge to (or from) a cell of higher potential and a cell of lower potential at the same time. The balancing circuit has a peak efficiency of 85.3%. The system draws only 53mA while balancing at 25A helping to increase low current performance. The system draws just under 5mA over all while active. Each BMS is equipped with one current sensor, which can measure $\pm 800\text{A}$ with a second $\pm 120\text{A}$ current range. Additionally, the board is equipped with coulomb counting to provide a better understanding of each cell.

While this design has many great features, lack of full software support makes many of the subsystems dependent on user interaction to use. As a result, the design is not fully complete. Additionally, last minute design changes on the final revision resulted in detrimental effects to the accuracy of many of the analog circuits including the current sensing features.

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Chapter 1 - Introduction

Batteries are used in everything from inexpensive toys to high performance cars. While an inexpensive toy most likely will use a non-rechargeable (primary) battery and a car will use some sort of rechargeable (secondary) battery, both devices would be of little use without a battery. Though batteries have evolved over the years, from the “Baghdad Batteries”¹ to Alessandro Volta 1800’s first battery to modern day cells using carbon nano-tubes^[1], the technology remains fundamentally the same.

In both primary and secondary batteries, chemical potential energy is converted into electrical energy. However, secondary batteries are capable of reversing this process by applying current to the cell. Primary batteries are typically used in low drain or intermittent use products^[2]. Primary cells typically have a higher energy density than secondary cells. Secondary cells on the other hand can output more current, which is required when starting a car or accelerating in an electric car. While secondary cells can be recharged, there usually is a limit to the number of recharges because not 100% of the chemical process is reversible

In a low cost application, a simple circuit that connects a battery to a motor is all that needed: for example a toy car. However, in a more expensive or sensitive product, a warning of low battery may be required. How obnoxious would it be to have a cell phone just simply turn off without a warning of low battery? What if a pacemaker gave no warning of low battery? In both of these cases, some sort of battery management system is needed to monitor of the remaining charge.

¹ Baghdad batteries are speculated to be an ancient cell.

1.1 Battery Management

A battery management system can be used to estimate remaining capacity in a cell. This capability is just one of the many tasks battery management systems (BMS) perform. The most important job for a BMS is to ensure the safety of the cell and the users. For example in Boston in 2013, a Boeing Dreamliner's auxiliary battery overheated and caught fire ^[3]. Fortunately no one was onboard the plane. Had this occurred in the air instead of on land, the results could have been much worse. While the source of the exact failure is not known at the time of writing, potentially a better battery management system could have prevented this failure.

Battery management systems come in a variety of forms and typically change from application to application. A common measurement for a BMS to take is voltage measurements. The voltage of the cell is one of the critical measurements as it can monitor if the cell is within a safe operating region (SOR). Over discharging or over charging, can cause damage. Damaging the cell could potentially lead to damage to the device the cell is powering. Attempting to charge a primary cell could cause it to overheat and catch fire. Similarly, secondary cells are sensitive to abuse; their capacity can be degraded or they may be destroyed. A battery management system is able to monitor if an unsafe condition is occurring and potentially disable the device to protect the cell.

Another common thing for a battery management system to do is to monitor the current into and/or out of the cell. This measurement may be of the entire battery pack (multiple cells). Measuring the current, especially of each individual cell, will allow the system to watch for any situations that may cause the device to be damaged. For example,

a 100Ah may be able to source 1000A for a short period ^[4], but extended period may cause the cell to overheat and become damaged. Accelerating from a stop in an electric car may require 1000A for a few seconds. Similarly, charging the same 100Ah cell with 100A is not recommended as it will decrease the capacity or, again, overheat it.

Using a combination of data collected from current measurements and voltage measurements, other aspects of the cell can be estimated. For example, the internal resistance of the cell can be estimated. As a cell ages, the internal resistance tends to increase ^[5]. As the cell ages, it decreases its capacity ^[6]. The capacity can be estimated by tracking the amount of charge that leaves and enters the cell, also referred to as coulomb counting. Other things like state-of-health or depth-of-discharge can be calculated from these measurements as well ^[7].

Many of the examples listed are concerns about overheating. Using the same cell as in the previous example, with only $100\mu\Omega$ of internal resistance, continuous sourcing at 100A will result in only 1W of self-heating. This is not a big concern assuming the cell can dissipate heat somehow. At 400A, the cell is dissipating 16W. At 1000A, it is dissipating 100W. These wattages are relatively low compared to the total output of the cell. However consider the case of an electric car with 16 cells performing time trials in the Mohave Desert. The ambient air is warm and the cells are all being utilized very heavily. Internal heat generation could be several hundred watts to further heat up the battery compartment. Since the voltage and current do not tell the BMS how warm the cell is, the BMS may also need to measure the temperature of individual cells or packs to remain in the SOR.

Another task that may be part of a BMS is charge management. In some cases, a separate controller handles this. Each cell's chemistry has a different preferred charge profile. For example, lithium ion typically uses a constant current charge until a certain point near maximum charge then a constant voltage charge ^[8]. Even if there is a separate charge module, the BMS may be required to perform balancing.

Balancing is used in systems with more than one cell. As the pack charges and discharges many times, differences in cells (even with the same model or same manufacturing lot) cause one cell to be more charged than another. This results in an unbalanced state that can reduce the effective capacity. Balancing can be as simple as using a resistor to discharge a cell or utilize a more complicated method of balancing.

There are many things a BMS may do, and some may not do. Typically this results in each system being tailor for a specific application. Many commercial systems are available, especially for handheld devices where an IC can handle the management without having to deal with significant current loads. Figure 1.1, shows a very basic BMS system attached to a battery pack consisting of four 100Ah cells. Figure 1.2, shows the cell without the BMS.

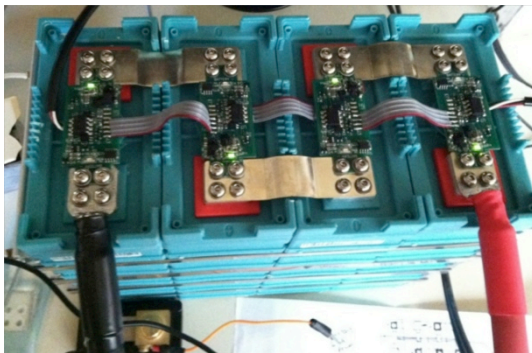


Figure 1.1 – Pictures of a rudimentary battery management system attached to large capacity cells.



Figure 1.2 – A battery pack with four 100Ah cells.

1.2 Goals

This project is more product development than a research project. Also the goals are somewhat general because the customer did not have a desired solution to solve the problem. The goal of the project from the customer (thesis advisor) was that the system was to handle battery management for multiple large capacity lithium ion cells. Each cell is to be at least 60Ah or larger. Additionally there was no predetermined cell configuration of the cells in the pack: all in series, all in parallel, or a combination of both.

Further discussion of the project indicated the direction of using a microcontroller to control the system. An additional requirement was to use an Atmel AVR processor was requested. This requirement was added so future work could be accomplished on the design since many students are familiar with this family of chips. Additionally, there was one more obvious goal: the design must be safe.

After determining the four primary goals: safety, unknown number of cells, 60Ah or larger capacity per cell, and the use of an AVR processor, secondary goals were added. The author added six secondary goals to make a better product instead of making the easiest to design and build. First, the product should be durable since it is designed to go into somewhat harsh environments: a car for example. Second, the design should fit within the outline of the cell so that the pack density is not affected by the addition of the board. Third, the design should be low profile so that it does not protrude from the top of the cell so far that the compartment where the batteries are stored must be retrofitted. Fourth, there should be minimal hardware setup required to install the system. There are many designs that require running hundreds (possibly thousands) of sense wires to a

central measurement system. Fifth, the system should be high performance so that its measurements and capabilities can be trusted. Finally, the system should be low cost.

Primary Goals

1. Safe
2. Unknown number of cells in pack
3. 60Ah or more per cell
4. Use AVR MCU

Secondary Goals

1. Durable design
2. Fits within cell outline
3. Low profile
4. Minimal setup
5. High performance
6. Low cost

Chapter 2 - Literature Review

This project is more product-oriented so a significant amount of literature review that is covered in the design sections as research was done to resolve or fix problems. Describing all of the research before explaining the design might result in confusion. To assist with clarity in the research and design, this section will cover the preliminary research that builds up to the basic design of the system.

Battery management systems come in a variety of forms. Ideally the solution is low cost yet high performance. However, most of the time these are mutually exclusive. Typically buying off-the-shelf systems is less expensive than the ground up design ^[7]. Many prefabricated designs exist which could be utilized. A quick search on Digikey reveals that nearly 9,788 (1,892 stocked) BMS related products were available. For example, a full-featured integrated circuit that includes charging controls, capacity, state of health, and many other great tools is available for \$3.88/ea in volumes of 2K ^[9]. However, nearly every one of these prefabricated ICs is aimed at one market: mobile electronics. Unfortunately, mobile electronics typically have 1-40Wh packs while the design for this project has 1200Wh battery pack.

While Digikey and its competitors focus on small capacity cells, large cells are not without prefabricated battery management systems. For example, Orion BMS and Elithion are two companies making battery management systems for large capacity packs. Orion's design is a centralized BMS, where Elithion is distributed BMS. There is a litany of other designs including a variety of custom circuit boards made by no-name companies and hobbyist available for purchase online.

Centralized or distributed BMS: which is better? Like many choices, there is not one correct answer. Centralized systems work by connecting all cells (or possibly only packs of cells) to one large processor to monitor the voltage of the cells (or pack). These systems tend to be less expensive than distributed designs because typically only one controller box is required. Centralized designs tend to be limiting in that each box can only handle a specific amount of units. An additional down side is that each cell has to be connected to the central box, which can result in very large bundles of sense wires to manage and maintain. Also, a centralized system tends to be physically further away from the cells and passive cell balancing is typically used. This may result in longer charge times. Finally, a possibly larger cooling system may be required to cool the passive balancing circuit.

Distributed BMS come in a variety of forms. Some have one BMS per cell, while others use one BMS per several cells. The latter has some similarities to a centralized system as it monitors multiple cells. Distributed systems tend to have many more control units, and as a result there is a much higher cost associated with this design since there are more controllers. Each controller also tends to be smaller because it does not have hundreds of wires connected to the board. Since each controller is closer (or on) each cell, active or passive balancing can be used.

Cell balancing is critical to utilizing the maximum capacity of all cells in the pack. Unbalanced packs will be unable to fully discharge or fully charge. Figure 2.1 shows an example of a battery pack with balanced cells. In this scenario, both cells charge and discharge at the same rate and will reach the empty point at the exact same time leaving no unused charge. Similarly when charged, they will reach their maximum capacity at the

same time. Figure 2.1 also shows a battery pack with unbalanced cells. While both of the cells are the same capacity, the pack's capacity is reduced. When charging, one cell reaches its maximum voltage and cannot be charged anymore preventing the partially charged cell (2.8V cell in Figure 2.1) from being fully charged. A similar thing happens when the cells discharge. The partially charged cell reaches an empty state before the fully charged cell which prevents the previously fully charged cell from completely discharging because further discharge would cause damage to the now empty cell.

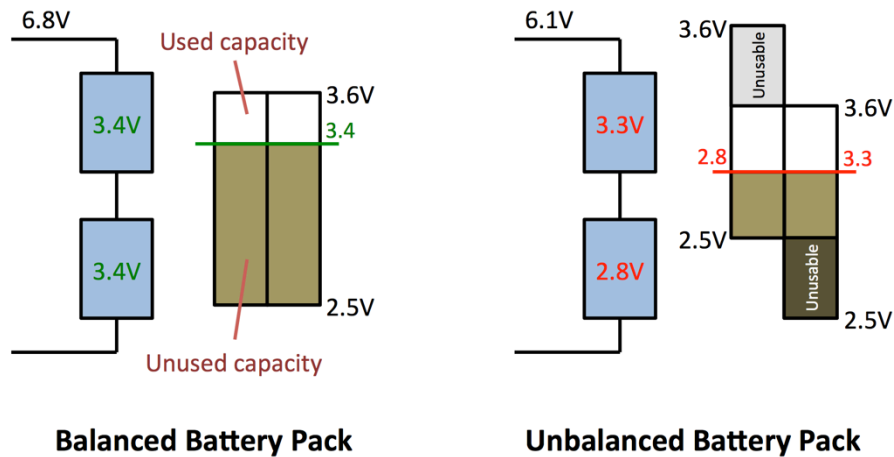


Figure 2.1 – Image showing the useable capacity of a balanced and unbalanced battery packed, both of the same capacity.

Cells with different capacities further exacerbate the problems from an unbalanced pack. While using a 60Ah cell with a 100Ah cell would make this problem very noticeable, fabrication of two identical cells will result in different capacities and internal properties. These slight differences will cause the cells to become unbalanced over a few charge cycles. Figure 2.2 shows two cells of different capacities in both unbalanced and balanced states. In the case of balanced cells, there is still an unusable region. The smaller cell is fully used and the larger cell is used as much as possible. In the case of unbalanced cells, there is limited usage because of charge and discharge limits.

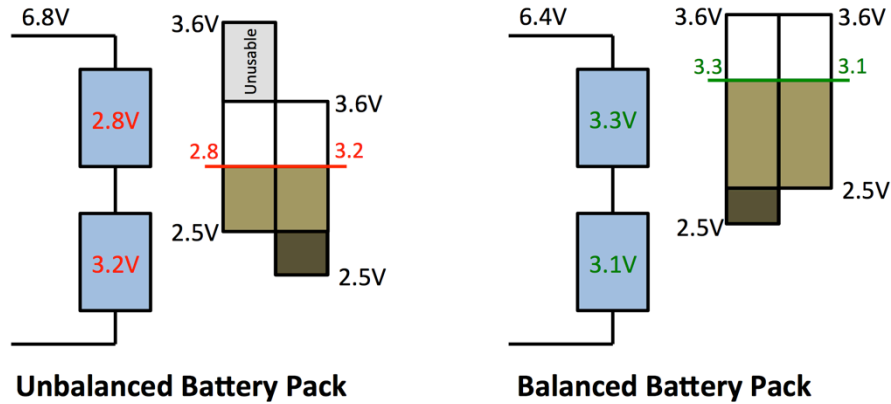


Figure 2.2 – Image showing the useable capacity of a balanced and unbalanced battery packed, both of different capacities.

To balance unbalanced cells, passive or active balancing techniques are typically used. Passive balancing is an excellent choice as it is very simple to implement and exceptionally inexpensive. Typically implementations of a passive balancing system are a power resistor or MOSFET across the terminals of the cell to discharge the most charged cell. Doing this permits the rest of the pack to charge more. Unfortunately, this solution has two large drawbacks. First, since it is dissipating the stored charge into heat, the power resistor or MOSFET will heat up. Depending on how the solution is implemented, there may be little or no room available to add a heat sink or a fan. As a result, the current through the dissipative element most likely will be fairly small which may result in extremely long balancing periods. Depending on capacity and how unbalanced the pack is, balancing may take anywhere from a few minutes to several hours. This can easily add a large amount of extra charge time. The second problem is that the charged capacity is being wasted. If efficiency is important, wasting energy is not an acceptable solution.

In contrast to passive systems, there are active balancing systems. These systems come in a variety of forms. A simple but improved method from the passive system is to continuously discharge the most charged cell (as in the passive system) as the pack is

being charged. This requires a better voltage monitoring system than a simple passive method, however it decreases charge and balance time. A significantly more complicated and expensive, but efficient, faster balancing, and charge, is to use a DC/DC converter. Using a DC/DC converter can potentially allow the system to transfer charge from the most charged cell to the least charged cell.

There are four basic varieties of a DC/DC converter based balancers. Each has multiple implementations. There is cell-to-cell, cell-to-battery, battery-to-cell, and bidirectional. See Figure 2.3. Each design has its own benefits but many of them require a very large storage element, typically an inductor or transformer, which would potentially require the system to be designed around a set cell configuration.

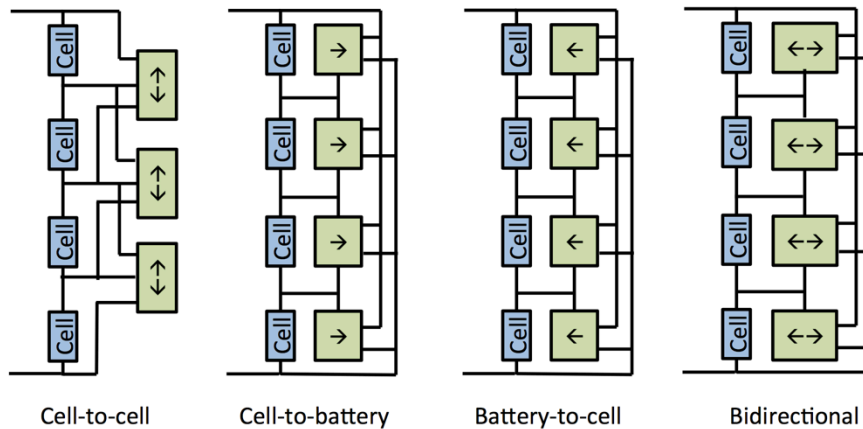


Figure 2.3 – This figure shows how the current flows to-and-from the cells in order to balance the battery pack.

Chapter 3 - Design

This part of the project was the longest phase of the project. A lot of early design was spent trying to optimize every aspect as much as possible before the first revision of hardware was fabricated. In total three revisions of the hardware were fabricated. For each the first two revisions, there were only two boards fabricated to test features. The final, revision had four boards fabricated to permit testing on a pack of four cells. This section will only discuss the final design, however earlier designs can be reviewed in the appendices.

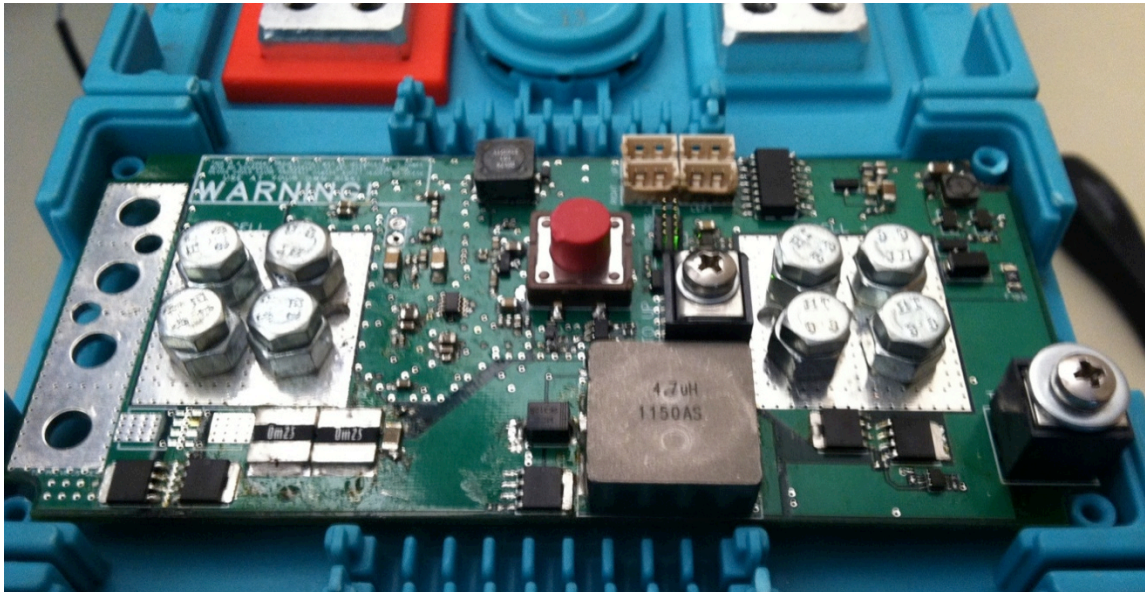


Figure 3.1 – Picture of the topside of the designed BMS mounted to a cell.

3.1 Electrical Hardware

Most of the goals relate to the electrical hardware. Unlike software, a simple change in the hardware design requires that a new PCB (printed circuit board) be fabricated. To prevent fabricating too many boards, the design started with a high-level

block diagram to achieve the goals. An overview of the system is shown in Figure 3.2. The image details the major features of the PCB. The image also includes connections to circuit boards of higher and lower potentials via communication and DC/DC connections. A circuit to greatly increase the current momentarily, shown in red, shorts the terminals across a small resistor to generate a measurable change in current. A sense resistor is connected to the negative terminal of the cell to measure. Connected to the sense resistor is a disconnect switch to break the connection to the outside world to protect the cell. Operational amplifier circuits to measure cell voltage and current are shown in blue. DC/DC related components for transferring charge from one cell to the next are shown highlighted in orange. Finally, things that are associated with the microcontroller (MCU) are in green. Finally, communication connections from board-to-board are shown in purple.

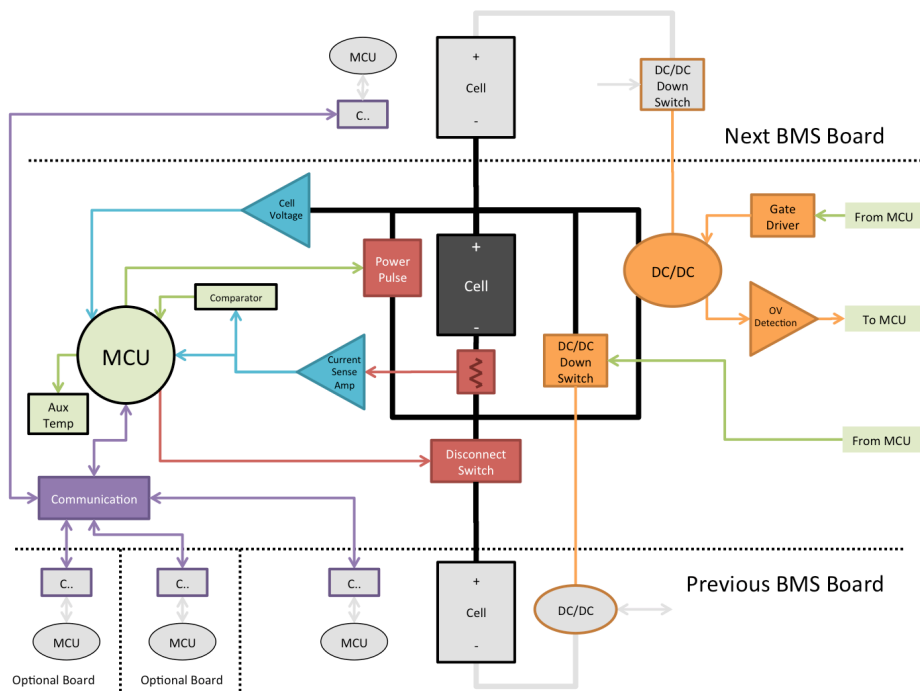


Figure 3.2 - Electrical System Overview

3.1.1 System voltage and power

With all battery-operated systems, the system voltage can be low. 1V or less is common for computer processors these days. Other circuit components, such as operational amplifiers, are difficult to find in these voltage ranges. Additionally, using nearly any LED would be difficult. As a result, some time was put into what the voltage the logic of the circuit should operate from.

Knowing that lithium ion batteries can vary in safe operating region (more on this covered in a later section), a logic level of 2.2V was selected. More common logic voltage of 3.3V was rejected as the cell voltage can operate below 3V in many cases. Utilizing a boost or SEPIC DC/DC converter would reduce the challenges associated with component selection; but these solutions create a larger, more expensive, more complicated solution, and a less efficient one. Additionally, there are exceptionally sensitive analog components within the design. By using a DC/DC converter supply voltage would be potentially too noisy and a second stage linear-drop-out regulator (LDO) would be required to clean up the signal. This means that the voltage would have to be boosted even higher meaning additional losses beyond the DC/DC converter's own losses. These losses are further exacerbated by the quiescent current required to drive the DC/DC converter as the target set for total system current is less than 1mA. However, the biggest motivation was noise on the analog system. Using another common voltage of 1.8V was also rejected because of lack of operational amplifiers selection and gate drivers for MOSFETs. As a result, 2.2V was selected using adjustable LDOs. This allowed for a 200mV drop out from the LDO (with a 2.4V cell). None of

the LDOs should ever see a high enough current load to incur a 200mV drop. 2.2V also gave an acceptable selection of components to use on the system.

The board was designed for batteries that can output very large currents (100-1000A). A fuse alone would not sufficiently ensure the battery remains at a safe operating point so MOSFETs were used to protect the cell. However, losses in the MOSFET could reduce the output performance of the cell, over-heat, or cause damage to the board. To prevent losses, very low R_{SD-on} MOSFETs were selected: NXP's PSMN0R9-25YLC ^[10]. Unfortunately to benefit from the low R_{SD-on} , the gate voltage needs to be 5 volts higher than the drain to ensure the MOSFET was completely on. The cell voltage alone could not supply this. As a result, a boost DC/DC converter had to be used.

As pointed out before using a boost converter adds more current draw. However, most of the MOSFETs in this design are simply in an on or off state and not driven hard with the exception of the balancing circuit which is covered later. Holding a MOSFET gate in an on state does not require much current: therefore a very low output current boost could be used, provided it does not have high losses or high quiescent current. A boost was found that required only 400 μ A quiescent current and had conversion efficiency at near no-load of approximately 50%. While increasing the load does improve efficiency, this boost typically only holds MOSFET gates high or low, thus it does not see higher loads often.

Figure 3.3 shows an outline of all of the voltages and supplies in the design. PP2V2 means 2.2 volts. Any label with MCU is for the microcontroller and anything with VA is an analog supply. PP2V2_ALWAYS is a legacy name from early in the

project indicating it was always on. In revision A, some of the power supplies would be disabled to conserve power. All power supplies stay on in revisions B and C.

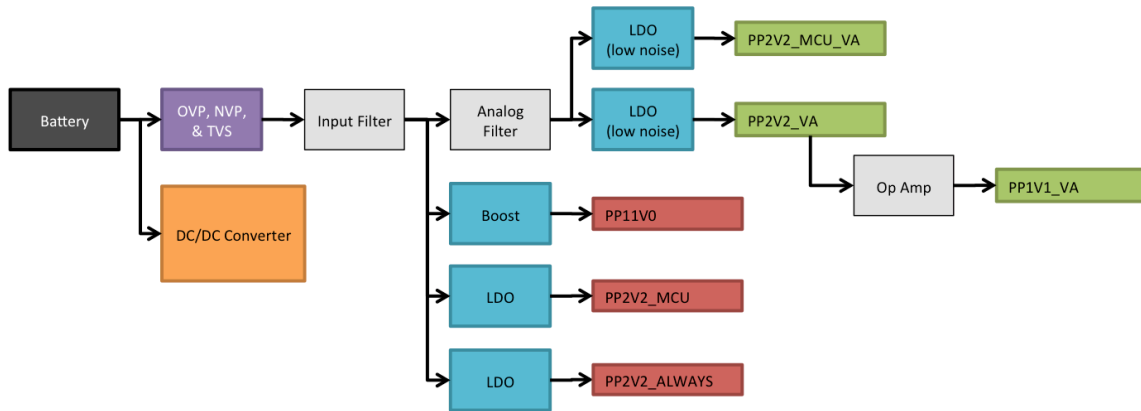


Figure 3.3 - Overview of system supply voltages.

3.1.2 Analog supplies

Separating analog supplies from the digital supply is a common and necessary practice because digital components tend to inject noise back onto the power lines supplying them. In revision A, both the digital and analog supplies were identical common LDOs. Unfortunately, as mentioned previously, the analog components are susceptible to noise. The analog circuitry was exceptionally sensitive as it attempted to amplify a signal that could be as small as $15\mu\text{V}$. Despite careful layout and selection of amplifiers, revision A suffered from noise on the analog supplies resulting in an unreliable amplifier output.

Some debugging of the circuit uncovered that the linear regulators (LDOs) used in the design were taking in a clean signal and outputting a signal with more noise than the input. To resolve this issue, revision B of the hardware used ultra-low noise LDOs. This

particular kind of LDO was very hard to find. The design required low input voltage, very low quiescent current, and a package that could be hand soldered with a reasonable yield. One IC was found that was a triple output ultra-low noise LDO: the Analog Device's ADP323ACPZ. There were a few other ICs available, however the cost to get the same number outputs was more than 2 times the cost.

The next step to noise suppression was to add a very wide range of input capacitors. Revision A used 0.01 μ F and 1 μ F capacitors in parallel to suppress noise. Both of these caps were rated for 25V so capacitor de-rating was not the problem. Revision B used 1pF, 100pF, 0.01 μ F, 1 μ F, and 10 μ F. Using a wide range suppresses a wider range of frequencies, but it added the risk of self-oscillation between the larger and smaller capacitors. Fortunately, testing showed no oscillations during operation.

The noise on the output was no longer detectable and the amplifiers generated a usable signal after adding nearly fifty more capacitors, using better capacitors (X5R vs. X7R and Y5R), and changing to a more expensive regulator. This improvement came at an expense more than just the cost. Adding more capacitors required more space. Revision A used 0603 capacitors and resistors. However, adding fifty more capacitors to a small area required that the design use 0402 whenever possible. To be consistent the whole design moved to 0402 components. Some 0603s and 0805s remained as the capacitance values reached higher values. There was another difficulty added by the design change. Since the quantity of boards being fabricated was very small, paying for a factory to assemble 2-6 boards was cost prohibitive. As a result all boards were hand soldered. As expected, some packages were more challenging to solder than others. The DFN package for the triple regulator was more challenging than any of the other DFNs

on the board. In fact, of the five attempts to solder the IC to a board, only one succeeded. This meant that only one of the two prototype boards could measure analog signals. For reference, the other DFNs could be soldered down with no issues.

In the final revision, revision C, the circuit was modified one more time to make assembly slightly easier since four complete boards were desired. The regulator was changed. This was a high-risk action as the new regulator was untested, however with such a low yield in assembly it was necessary. The new LDO selected was Micrel's MIC5209YM. This is an adjustable LDO with an ultra-low noise option by changing the feedback circuit ^[11]. Another change to the circuit was to reduce the number of capacitors to a more reasonable quantity. All of the 1pF caps in the analog section were removed and several of the 10 μ F capacitors were removed as well. This was done for three reasons.

First, the filter between the unregulated digital main and the unregulated analog main was improved from a simple RC filter to an LC filter damped with an RC filter. This filter used 100 μ H inductor and a 1 μ F capacitor resulting in a cut off at 16kHz. At such a low frequency, linear regulators are able to suppress any noise and output a clean supply. Second, 1pF capacitors filter out extremely high frequencies. It is possible for a high frequency to get into the circuit, however the PCB design should shield against external noise. Third, having more capacitors around reduces the options of how to route all of the signals. Less components makes routing easier and having a clean routing will most likely have more of an impact on signal integrity than a 1pF in this design. Unfortunately, the new regulator was significantly noisier than the previous regulator. The impact of the noise is covered in Chapter 4.

Finally, there is a high precision voltage reference IC. This regulator outputs a 2.048V $\pm 0.2\%$ reference. Another option would have been to connect the ADC reference to one of the analog supplies. While the LDOs regulate the output to less than $\pm 1\%$, the tolerance of the resistors and the internal reference can vary the output's set point by several hundred millivolts. Accounting for this variability in software is not too challenging, but if the voltage drifts or dips at all, any calibration is useless. Additionally the reference IC is nearly insensitive to temperature and aging effects unlike the LDOs. By using a 2.048V reference, each least significant bit (LSB), of the 12-bit ADC, is equivalent to 0.5mV.

3.1.3 Measurement

One of the primary tasks for the battery management system is to monitor the cell. The following sections describe the design for measuring battery voltage, current, and cell capacity as well as measuring other important values.

3.1.3.A Battery voltage

One of the first things designed was a way to measure the battery voltage. Since the cell voltage is direct indication of remaining capacity and health, it is very important to monitor this voltage accurately. The lithium iron phosphate (LiFePO_4) cells were selected for testing the BMS. These cells have a working voltage between 3.1 to 3.3V, and an absolute max range of 2.8V to 3.6V. Since the system voltage is 2.2V, a

simple voltage divider would be an exceptionally inexpensive and reasonably accurate solution. However, the lowest part of the Analog-to-Digital Converter's (ADC) range is unreachable and this reduces the usefulness of the divider². Also, since the divider would probably need a voltage follower to buffer the divider from an ADC, a better circuit was added for nearly no additional cost.

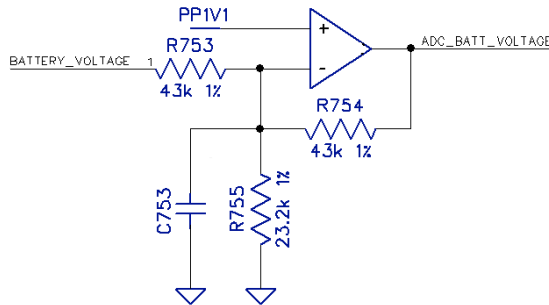


Figure 3.4 - Battery voltage measurement circuit

$$V_{out} = (1.1V) \left(1 + \frac{R_{754}}{R_{755}} + \frac{R_{754}}{R_{753}} \right) - V_{Battery} \left(\frac{R_{754}}{R_{753}} \right)$$

$$V_{out} = 4.239V - V_{Battery}$$

Equation 3.1 – Design equation for battery voltage scaling and shifting.

The circuit shown in Figure 3.4 was designed. This circuit scales and shifts the battery voltage to fit the ADC measurement range. To make the design useful on more than LiFePO₄ batteries, an input voltage range of 2.4 to 4.2V was used. This range was shifted and scaled to fit within the range of just slightly above 0V and slightly below 2.048V. The circuit is an inverting summing amplifier using 1.1V as the reference instead of ground. This means 4.2V would be nearly 0V at the ADC and 2.2V would be 2.048V. Since 1.1V is “ground” in this circuit, tying one of the summed inputs to real ground results in a -1.1V being summed. The resulting equation is shown as Equation 3.1. Adjusting R₇₅₅ will scale how large the voltage shift down affects the input and adjusting R₇₅₃ will adjust the scaling of the input. The current design includes a -1

² A voltage divider could be designed so that the divided voltage is just at the top of the ADC's range at full charge. However, there is no way that the voltage divider's divided voltage can ever reach zero, thus wasting a section of the ADC's measurement range.

scaling factor and a voltage shift down of 4.2V. C_{753} was added as an optional low-pass filter.

3.1.3.B Battery current

Measuring the battery current is one of the most important features and also one of the most challenging to design. Accurately measuring the current is important for the system to count coulombs, log usage, and detect abnormal operation. One challenge associated with accurately measuring the current is that the selected 100Ah batteries can source peak currents of 1000A for 10 seconds. Measuring $\pm 1000\text{A}$ (for over-current detection) is possible to do accurately, but also measuring a more typical range of $\pm 30\text{A}$ accurately is a challenge using the same hardware.

Initial research indicated that the best way to measure a $\pm 1000\text{A}$ current range is to use a magnetic sensor to minimize power loss.^[12] There were a number of problems with this design. Nearly every commercially available design using a magnetic sensor used one single current sensor on the output of the entire array of battery packs. This yielded a lower cost solution, however it gave very little insight into the charge in an individual cell. The design proposed in this paper uses a current sensor for each cell.

Another option was to use a current loop sensor. Several of the current loop sensors were rated for the required range: for example, a $\pm 200\text{A}$ current sensor could measure 800A for short duration. However this current loop sensor was accurate to $\pm 2\text{A}$ near 0A through sensor and $\pm 10\text{A}$ closer to 200A ^[13]. Using these values to coulomb count would possibly result in an unacceptable error in cell capacity estimations.

Another issue this device presented was that its bandwidth was limited to 50kHz. In addition to the inaccuracies, most of the current loop systems needed 5-12V with currents ranging from 15-30mA. A current of 15mA exceeds the entire budget for current before considering the current required to boost from 2.2V up to 5-12V. Finally, these devices required that typically a wire or bus bar be placed through the sensor. While a solution could have been designed, this posed a problem when considering two of the goals of the project: low profile and durable. Regardless of the bulkiness of this design, the power consumption was enough to completely remove it from consideration.

A lower cost system that does not directly require contact with the trace is to use a giant magnetoresistance (GMR) IC. These ICs are essentially resistors that are sensitive to magnetic fields^[14]. These devices need to be in near proximity to the current carrying trace. Unfortunately these sensors also could be thrown off by other magnetic sources such as an electric motor. Since these sensors would be unreliable in this application, they were rejected.

Overall, the magnetic solutions posed too many problems for high accuracy measurement. Many commercial designs use one large magnetic sensor to determine the output current but this limits feedback for the BMS. The design used in this thesis measures the current for each individual battery to better control and monitor battery usage. Ultimately, the final solution was to use a current sensing resistor.

Research into the resistive sensors indicated that there are two options: use power resistors or calibrate a small copper trace length. Using a copper trace length is appealing because it is an inexpensive solution. The major issue with using a copper trace is the temperature dependence of copper's resistance is very significant ($\sim 3930\text{ppm/K}$ ^[15]),

which would add an error into the measurement. The change in the resistance can be accounted for by using a temperature sensor. The second option is to use power sense resistors, which typically have much lower thermal coefficient ($<20\text{ppm}/\text{C}^{[15]}$).

To minimize the effect of temperature dependence, this project uses four power sense resistors in parallel. Each resistor is $4\text{W } 250\mu\Omega \pm 1\%$. Four power resistors were chosen since it was easier to purchase four resistors than a single $16\text{W } 62.5\mu\Omega$ resistor. The resistor network allows for 506A to continuously go through the sensor. This would require external cooling because the board cannot dissipate 16W on its own. A more typical continuous operating current of 100A will only dissipate 5/8W. Additionally, the resistors can only handle short transients above 500A.

One of the many design problems was that a 1A measurement would only output a $62.5\mu\text{V}$ signal. Another problem was that a failsafe feature (this is covered in a later section) required that the sense resistors be connected to ground. This is a problem because the signal to measure is potentially outside the range of operation for most ICs. A set of voltage dividers was used to remedy this problem. The voltage dividers are connected from the analog supply of 2.2V to both terminals of the sensor resistor. The signal is shifted up to a more optimal operating condition for the amplifiers, however it reduced the amplitude of the signal to $3/4^{\text{th}}$ of what it was before. So now a 1A signal results in a $46.875\mu\text{V}$ output signal. An additional problem that was caused by using voltage dividers was the tolerance of the resistors.

Initially the voltage divider used $10\text{k}\Omega \pm 1\%$ and $30\text{k}\Omega \pm 1\%$ resistors. However, when two circuits are connected in parallel (to exactly the same supply and ground) the difference between the two center nodes can be as large as 16.5mV with a 2.2V source.

This is an exceptionally large error. It can be removed in calibration (covered in a later section) but this adds a large offset to the signal that will be multiplied by 120 possibly causing saturation at a very low current measurement. To resolve this problem, more expensive $\pm 0.1\%$ resistors were used for the voltage divider. Using 0.1% resistors, the maximum difference became only 1.65mV , which is still a significant error. The total offset after amplification is 198mV instead of 1.98V with 1% tolerance resistors.

The next step to processing the differential signal was to amplify it. A logical choice would be to use an instrumentation amplifier (IA). Three problems immediately arose. The first problem was that most IA ICs require too large of a quiescent current: typically 1mA or more. The second problem was that many of the IA ICs bandwidth was low. Some of the better commercial IA's bandwidth was in the range of 50kHz with a gain of 1 (the final design of this circuit uses a gain of 120). Finally, the input voltage offset of many IAs are anywhere from 1mV to 500mV . An input offset of $\pm 1\text{mV}$ would be seen as $\pm 1.33\text{mV}$ more on the current sense resistor, adding the equivalent of $\pm 21\text{A}$ to the measured value. While 1mV is less than the error of the voltage divider, the voltage divider is a worst-case scenario where the input offset is the best case. Additionally, the resistors are much less dependent on temperature and age than the input offset of an amplifier. When combining all of these problems, commercially available IA ICs were not sufficient for the design. As a result, a discrete IA circuit was designed.

The selected operational amplifiers were LTC6256, which is a dual chopper OA. A chopper op-amp was selected because they constantly calibrate themselves to minimize the input voltage offset. The LTC6256 has a typical input voltage offset of $\pm 9\mu\text{V}$ (with a maximum of $\pm 100\mu\text{V}$). The circuit that was designed is a basic three OA instrumentation

amplifier. The first stage (two OAs, U700.1 and U700.2) had a gain of 4 and the second stage (one OA, U730.1) also has a gain of 4. By splitting the gain into two stages of 4, the bandwidth of the OAs was maximized. The total gain of the IA from input to output was a gain of 16 with a bandwidth of more than 200kHz. Additionally, the circuit has an optional low-pass filter on the output using R₇₁₀ and C₇₀₁ to attenuate undesirable signals.

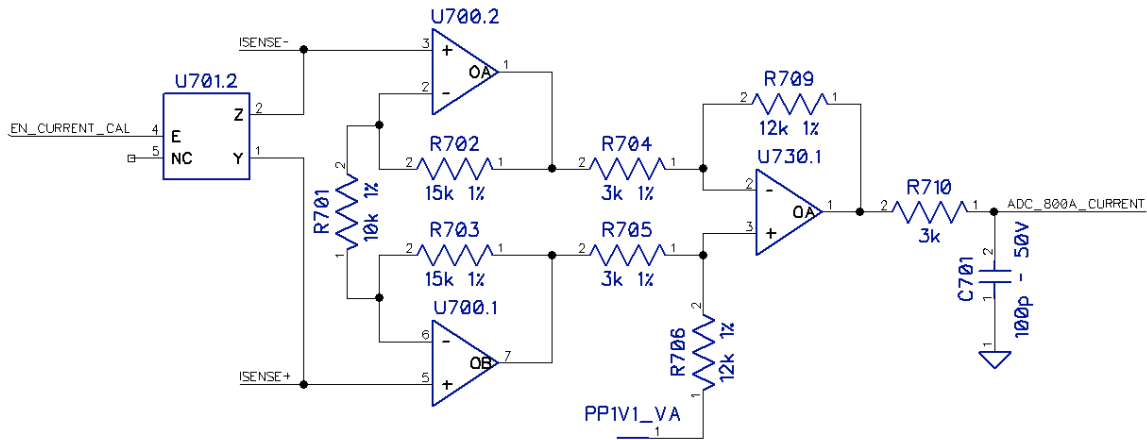


Figure 3.5 – Instrumentation amplifier circuit used to amplify voltage from sense resistor.

$$V_{ADC_800A_CURRENT} = (V_{ISENSE+} - V_{ISENSE-}) \left(1 + 2 \frac{R_{702}}{R_{701}} \right) \left(\frac{R_{709}}{R_{704}} \right) \quad \text{Equation 3.2 – Design equation to calculated desired output from an instrumentation amplifier made from three op-amps.}$$

The output of the IA is used to measure the current through the sense resistors for a range of $\pm 800A$ with a sensitivity of $187.5\mu V/A$. A second measurement range of $\pm 120A$, with a sensitivity of $1.5mV/A$, was added by adding a third amplification stage. The third amplification stage is a simple non-inverting op-amplifier circuit (U730.2) with a gain of 8. The circuit also has an optional low-pass filter R₇₁₁ and C₇₀₂.

As mentioned before, there was an accumulation of errors that are part of the signal. To remedy this, two calibrations were used to mitigate most of the error. First, there is an analog switch that shorts the inputs of the IA. Shorting the inputs allows for

the errors from the input of the op-amps to the input of the ADC to be measured. Some of the errors are temperature dependent such as the input offset. As a result, the analog switch is used before every measurement to calibrate out many of the variable errors. To sample the current, the inputs of the IA are shorted first. After shorting the inputs, a measurement is made on the ADC. This measurement is all of the accumulated errors in the IA circuit. After that measurement is completed, the inputs are no longer shorted and a second sample is taken. The first measurement is subtracted from the second measurement to remove the offsets and errors. This does not account for the tolerance of the sense resistor or the errors associated with the voltage dividers since they are before the analog switch.

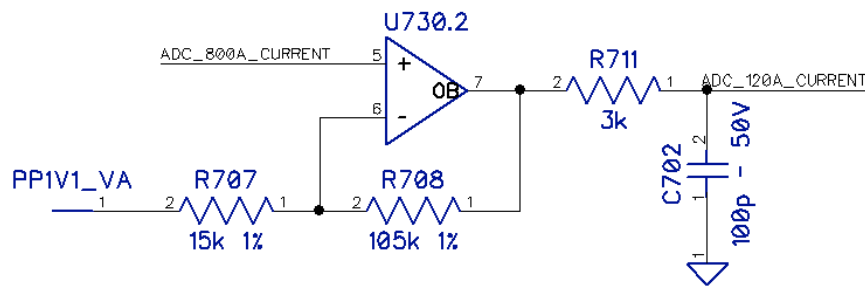


Figure 3.6 - Amplifier stage to archive ±120A current range.

$$V_{ADC_120A_CURRENT} = -V_{ADC_800A_CURRENT} \left(1 + \frac{R_{708}}{R_{707}} \right) \quad \text{Equation 3.3 – Design equation for } \pm 120A \text{ current measurement gain stage.}$$

To adjust for the errors not covered by shorting the inputs, a calibration is done using software tools. The software measures multiple known currents and fits a line using linear regression. This removes most of the errors, however some of the parameters may have a weak relationship with temperature and aging that is only corrected by recalibration using software. This calibration would be done at the “factory,” however it is possible for the user to do it as well.

Software Steps to Sample:

1. Enable analog switch (short inputs)
2. Sample ADC channel desired (120A or 800A range signal)
3. Disable analog switch (no longer shorting inputs)
4. Sample same ADC channel as in step 2
5. Subtract the first sample (step 2) from the second sample (step 4)
6. Apply gains and offsets determined by software calibration

Ignoring all of the offsets and errors associated with this measurement circuit, there are two additional sources of error that are not directly associated with the circuit. The first one is the noise from the power supplies. The initial linear regulators (LDO) used on revision A added about 20mV_{pp} of noise on to the input signal of the amplifier. This caused unpredictable errors at the output of the amplifier. The impact of the power supply noise was reduced by using ultra-low noise regulators, a large range of input capacitors to suppress a wide range of frequencies, and a low-pass filter to isolate digital power from analog power.

The second problem was that this highly sensitive amplifier is unavoidably close to the active balancing circuit, which may be switching up to 25A. This problem was one of the most challenging and mitigated in multiple ways. First the analog signals were buried as much as possible to protect against electronic noise. A magnetically shielded inductor was used to protect the circuit from magnetic noise. The balancing circuit was pushed as far away as possible from the analog circuit. Finally, the layout of the ground planes was designated to prevent currents from circulating through the analog area.

3.1.3.C Coulomb Counting

Measuring the capacity of the cell is an important feature of a battery management system. A very inexpensive way to estimate the capacity of the cell is to use the cell voltage. This can be an accurate measurement if the profile of the cell charge to voltage is well known. However, age, usage, temperature, discharge rate, and other parameters affect the profile of the voltage vs. charge ^[16]. Additionally, the internal resistance of the cell is required parameter to accurately estimate the cell's voltage. Ignoring the internal resistance may make the cell appear to be at a higher voltage, which would give a higher estimation of remaining charge.

A more accurate measurement of the remaining capacity is to count the charge that enter and leave the cell. This can be achieved by first carefully discharging the cell down to a state of near zero capacity. Then charge the cell back to full capacity and integrate the current going into the cell. ^[17]

Two ways to count coulombs are: to perform a digital integration of measurements or use an analog integrator circuit. Digital integration is easier to implement than analog integration. Using digital integration requires only that the microcontroller can sample the current measurement. Increasing the sample speed will improve the accuracy by capturing transients better. Unfortunately the same thing that makes it accurate also makes it less accurate. Since the measurement relies on individual conversions from analog to digital, each conversion has an associated error. The more samples used, the more the error accumulates. Using a higher resolution ADC can reduce this, however this typically comes at the cost of power consumption. Another problem with digital integration is that, depending on implementation, it may need to be running continuously which means the

controller cannot utilize sleep which will result in more power consumption. In some BMS applications, power consumption may not be an issue.

Another option is to use an analog integrator circuit. An inverting operational amplifier circuit with the feedback resistor replaced with a capacitor can integrate the input signal. This allows for continuous analog measurement and does not rely on rapidly sampling the current. It should be noted that an analog integrator is not without problems. The primary drawback to this circuit is that the input offset of the integrator causes the integrated voltage to slowly grow until it saturates the output. Also the circuit has limited bandwidth and can be affected by noise.

This design uses an analog integrator since it allows for much lower power consumption. The power consumption per integrator is approximately $60\mu\text{A}$ instead of the $800\mu\text{A}$ or more current required to keep the selected microcontroller in an active state. Additionally, with special care, the input and output signals can have minimal noise. To further improve noise rejection, the microcontroller can average multiple samples.

In Figure 3.7, U750 is one amplifier in a dual operational amplifier IC package (LTC76256 – low offset, voltage, and quiescent current). The second one is used for the 800A range coulomb counting. One might note that C757 is significantly smaller than C756 and would have no impact on the circuit. The goal of this is to improve higher frequency response. The larger cap may not be able to capture frequencies higher frequencies. The combination of $470\text{k}\Omega$ resistor and $47\mu\text{F}$ will allow the microcontroller to sleep for twenty to thirty seconds before the output saturates with a maximum voltage input. U751 is a dual analog switch used to reset the capacitors, thus removing the

accumulation of error from the input offset. The added 470Ω resistor is to prevent exceeding the maximum ratings of the switch.

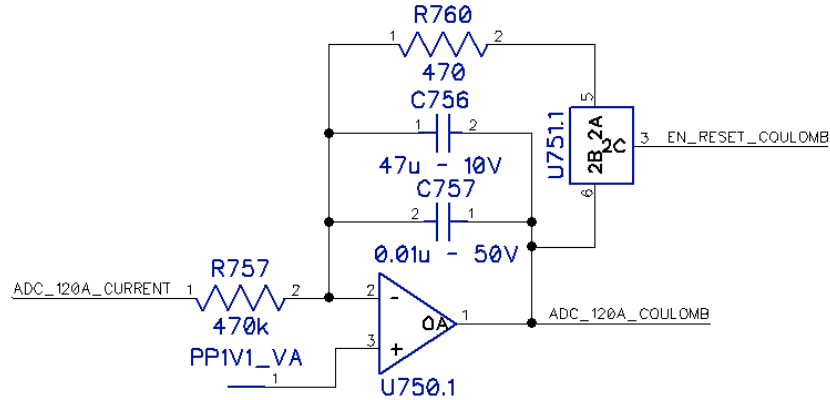


Figure 3.7 - Circuit diagram of the ±120A current range's coulomb counter. There is a similar circuit for the ±800A range.

In most cases, the 120A integrator should not saturate and would be the primary choice for coulomb counting. The 800A range is there for the cases where large surges have been detected and the 120A input may have saturated which would result in an inaccurate count. As mentioned before in the previous section, there is a significant accumulation of error as the very small current signal goes through multiple amplifier stages. As a result, the coulomb counting circuits are also calibrated with software in the “factory.”

Software steps to sample:

1. Measure ADC on 800A channel and then measure ADC on 120A channel. This order is important as the 120A channel changes quicker than the 800A channel.
2. Enable the “reset” switch to short and reset the integrating capacitors.
3. Enable the analog switch to short the input of the instrumentation amplifier circuit.
4. Measure ADC both 120A and 800A channels.
5. Disable both analog switches.

6. Using “factory” software calibrations, the time since last sample, the samples taken in step 1, and the calibration samples taken in step 4 the error from the offsets can be removed.

3.1.3.D Over-charge and over discharge detection

Charging the battery too rapidly or discharging the battery too rapidly can cause permanent damage or even destruction of the cell. To prevent this, a simple window detector was designed to capture any excursions beyond a safe operating point. This design utilizes the two digital-to-analog converters (DACs) built into the microcontroller. One sets the charge limit and the other sets the discharge limit. The 800A current measurement range is then sent to the window detector. See Figure 3.8.

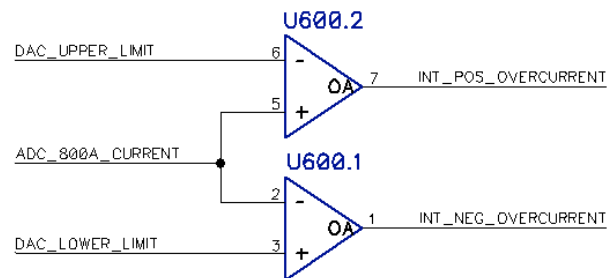


Figure 3.8 – Over discharge and over charge current detection circuit.

When the $\pm 800\text{A}$ range output (ADC_800A_CURRENT) exceeds the threshold for over-current (DAC_UPPER_LIMIT), an interrupt is triggered indicating an overcurrent state. Similarly if the over-discharge limit (DAC_LOWER_LIMIT) is passed by the ADC_800A_CURRENT, an interrupt triggering over-discharge state is also triggered. Each interrupt goes to its own dedicated GPIO on the microcontroller for software flexibility.

3.1.3.E Current pulse

This system has a power resistor, which shorts the terminals of the cell to momentarily increase current. This is used to help estimate the DC resistance (DCR) of the battery cell. This resistor is not intended for passive balancing system³. The DCR is used to estimate cell voltage (versus terminal voltage) and health of the cell. The cell DCR is also an indicator of age as the DCR increases.

Figure 3.9 shows a simplified circuit of a battery cell. When measuring the voltage of a cell, the terminal voltage is what is actually measured. To measure the cell voltage, the current and the internal resistance are required. Unfortunately measuring the internal resistance is challenging, which is why a current pulse is used. Since the cell capacity is very large, increasing by 30A will not cause a significant drop in V_{CELL} , but there is a measurable rise in voltage on $V_{TERMINAL}$ ^[18]. Using the change in current and voltage will result in the DCR of the cell. See Equation 3.4.

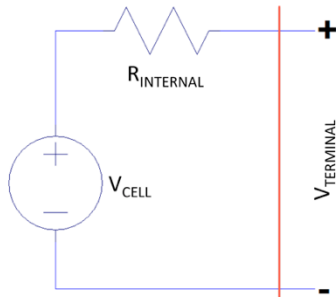


Figure 3.9 – Simplified diagram showing internal cell voltage versus terminal voltage.

$$R_{INTERNAL} = \frac{\Delta V}{\Delta I} = \frac{V_2 - V_1}{I_2 - I_1}$$

Equation 3.4 – Equation to determine the internal cell resistance.

Since operating this circuit for too long of a period of time could cause damage, protection was added. This circuit is connected to the PP_DCDC_FUSED net, which is

³ While this resistor could be used to discharge the battery, a much larger resistor value is required. The system cannot thermally sustain discharge through this resistor.

used on the DCDC converter. This net was used because, as the name suggests, it is fused. Therefore, using the DC/DC and the power pulse at the same time will trip the fuse. This is a good thing because otherwise the DC/DC converter may add undesirable noise to any current measurement. The fuse that protects this circuit is a medium blow fuse rated for 30A. If the cell voltage is less than 3V, the fuse will not blow (in a reasonable time frame). A hardware timeout circuit is used to prevent damage from this case.

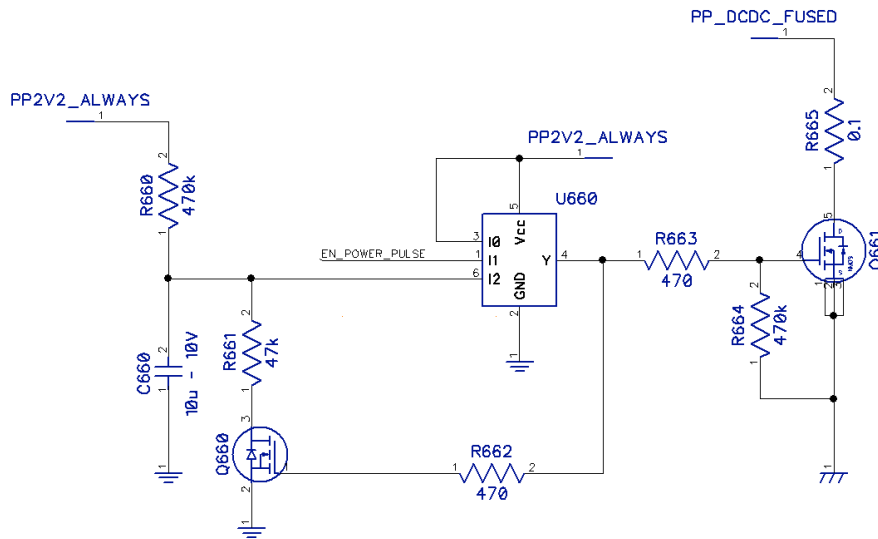


Figure 3.10 – Power pulse circuit with timeout to prevent damage to power resistor.

The timeout circuit is based around U660, which is a universal logic IC with Schmitt trigger inputs. This IC is wired as a 2-input logic AND. When the power pulse is not being used, C660 is charged to 2.2 volts: setting a logic 1 to an input of the AND. When the microcontroller sets the EN_POWER_PULSE net high, the AND outputs a high signal. This enables the power MOSFET Q661 to starting the power pulse. This also enables Q660, which discharges C660 much more quickly than it charged up. When it

reaches the low threshold of the Schmitt trigger, the AND outputs a low state and disables the power pulse. If the input signal is not disabled, it will pulse on for 55ms and turn off for about 4.5 seconds, which is just over a 1% duty cycle. This circuit was chosen over a 555 timer IC because a 555 timer was more expensive, requires nearly the same components, and many of the 555 timers consumed more power than the universal logic IC.

3.1.3.F External Temperature Sensor

The design incorporates a set of solder points to add a thermistor (NTC resistor). This component is optional as the microcontroller has an imbedded temperature sensor, which can be polled. Additionally, there are two over-temperature sensors placed on the board, which is covered in a later section.

The external temperature sensor was designed to use a 470k NTC (Panasonic ERT-J0EV474J): however, software or other component values can easily be adjusted to accommodate any NTC. Using the suggested NTC resistor results in a fairly linear output from the circuit between 10 and 90°C see Figure 3.12. A third order approximation of the curve will reasonably fit the data from -40 to 120°C. Using a probe with leads can be attached to the cell to detect thermal transients. However, since this is an optional feature, no software is available other than to test the output of the operational amplifier.

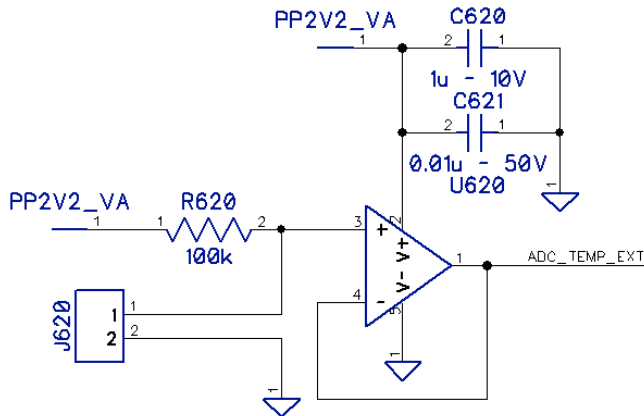


Figure 3.11 – Schematic voltage follower used to buffer voltage divider with thermistor.

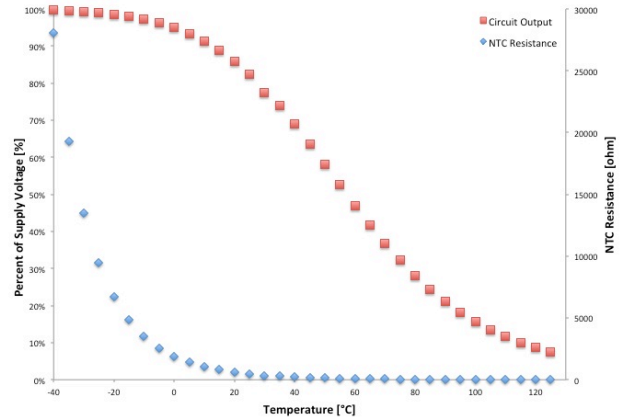


Figure 3.12 – Plot of Thermistor (NTC resistor) versus temperature and percent of voltage supply from divided voltage.

3.1.4 Active Balancer DC/DC Design

To achieve one of the goals of this project, the design needs to be flexible to handle any configuration of cells in the battery pack. As a result, this design uses a cell-to-cell based balancer because it allows all of the circuitry be attached to each cell without exceptionally large inductors or capacitors for mass storage. In addition, it allowed for a minimalistic set of power connections. One draw back to this design is that it requires repetition of many parts.

It should be noted that an active balancing system was the only practical solution for a cell pack of this capacity being used in an unknown environment. If the application was purely long-term storage, then possibly a passive system may be acceptable. However, if the application is an electric car, adding possibly several hours to the charge

time for balancing may be prohibitive. There is also an argument to be made for the size and expense of adding a cooling system depending on application.

This design uses a synchronous buck-boost circuit to transfer from cell-to-cell in series. In Figure 3.13, a typical buck-boost (non-synchronous) circuit is shown. Figure 3.14 shows a simplified circuit used in this design. By changing R1 to a voltage source (positive side connected to the inductor) and changing the diode to a switch, a bi-directional circuit with minimal parts is formed.

Unfortunately, this design was patented in 1995 by G. Brainard ^[19]. It does serve the purpose of a simple circuit to transfer large amounts of current from cell-to-cell. In 2008, a doctoral student presented a 100kW version of this circuit using a 450V input to 280V output and achieved 98% efficient at full load ^[20]. The 100kW version used a four-phase system with thyristors. The student's design transferred charge between two supplies at the same potential instead of different potentials, however the operation of the two circuits is very similar.

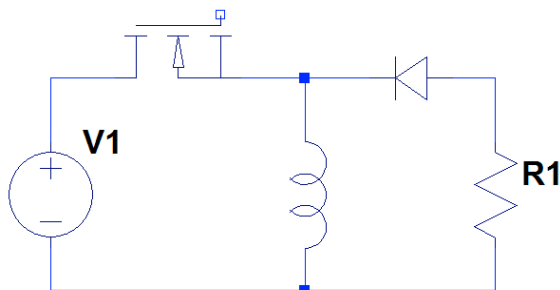


Figure 3.13 – Schematic of a basic buck-boost DC/DC converter.

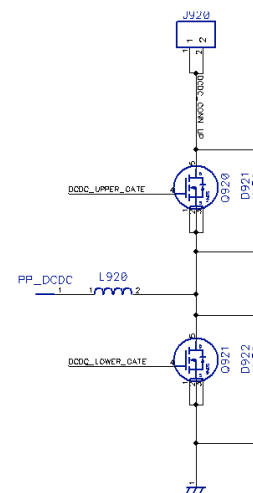


Figure 3.14 – Basic schematic of synchronous buck-boost used to transfer charge from cell to cell.

While a successful version of this circuit was fabricated with thyristors, this version will use n-channel MOSFETs. Reason for this design change is that thyristors typically have a voltage drop of at least 1V. In a 450V system, 1V is a trivial loss. In a 3V system, a thyristor results in a significant loss. Additionally, the designed proposed in this paper has a peak current of 25A instead of 250A as in the 100kW design. Unfortunately MOSFET's power loss is a function of current squared instead of the approximately linear relationship with current for a thyristor. To reduce the power loss associated with the MOSFET, an extremely low on-state resistance (R_{SD-ON}) was used. In this case, the selected MOSFET is a PSMN0R9-25YLC (25V, 100A continuous) from NXP with an R_{SD-ON} of 0.75m Ω . This MOSFET will dissipate 0.47W with 25A continuous current through it, which this circuit should never see.

While the selected MOSFET boasts a very low R_{SD-ON} , it requires a minimum V_{GS} of 10V. Since the battery has a maximum of 3.6V, a boost was required. The boost used in this design supplies 11.5 volts to ensure the MOSFET is fully on⁴. The boost circuit is covered in a later section.

Another source of loss associated with a switching circuit, like this one, is the turning on and off of the MOSFET. To reduce this loss, a very fast on and off transition is required. Two low-side drivers were initially used because 11.5V was high enough to turn on the high side switch with an acceptable R_{SD-ON} . However, this design caused a significant amount more ringing than using a single half-bridge gate driver with a bootstrapped high side. The selected IC is the LM5109MA, which can output a peak of $\pm 1A$ into the gate of the MOSFET. One problem with this IC is that the high level input

⁴ The MOSFET turns on at a much lower voltage ($\sim 4.5V$), but does not achieve the desired low resistance until closer to 10V.

voltage threshold (V_{IH}). Typically the V_{IH} is 1.8V, which is not a problem; however it can be as high as 2.2V in a corner part. To prevent possible problems with the logic not being detected in a corner case, the voltage regulators in the system were set to be nominally 2.25V.

One other possible loss due to this switching circuit is the power consumption associated with rapidly charging and discharging the MOSFET gate. In some cases, the power required to charge and discharge the gate of a MOSFET will exceed the power losses associated with the MOSFET's R_{sd-on} . Figure 3.15 shows a plot of several MOSFETs ranging from 0.45m Ω to 10.5m Ω R_{sd-on} . MOSFETs for this plot have comparable voltage rating to keep the gate capacitance comparable.

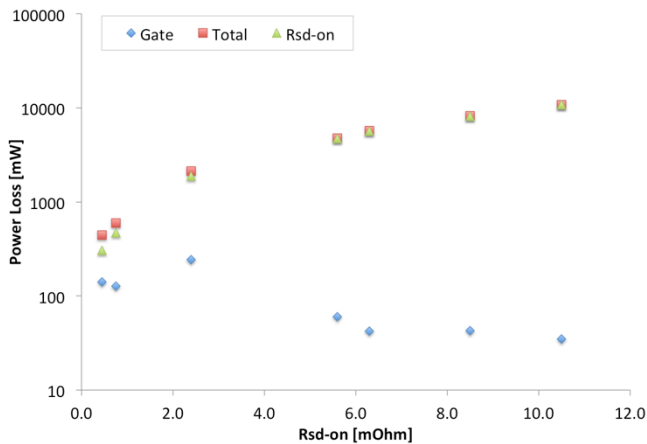


Figure 3.15 – Plot of power loss versus R_{sd-on} at 30A continuous for a selection of commercially available MOSFETs. The plot also includes losses associated with driving the gate using a LM5109.

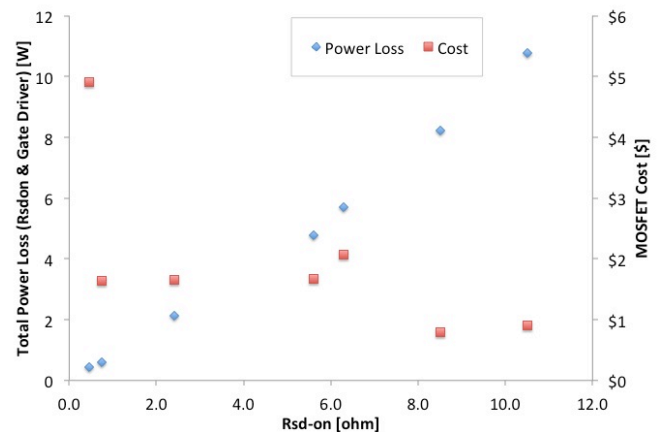


Figure 3.16 – Plot of power loss and MOSFET cost versus R_{sd-on} for the same MOSFETs selected in Figure 3.15

The analysis showed that lower R_{sd-on} would reduce power loss despite having exceptionally large gate capacitance. A second analysis, shown in Figure 3.16, showed that the cost of the selected MOSFET (R_{sd-on} of 0.75m Ω) would yield the best balance between losses and cost.

One challenge associated with all synchronous DC/DC converters is the control signals. Two complimentary signals are required. Both MOSFETS cannot be on at the same time and keeping both switches off too long increases losses. To prevent problems, dead time is always inserted into the circuit. Many commercial gate drivers have built in dead time to alleviate this problem, but the selected gate driver was specifically chosen because it does not have a dead time insertion circuit. This was done to allow software to be tuned to optimize the converter.

The selected microcontroller (XMEGA128A3) has a built in pulse-width modulation (PWM) generator. It also has a built in module to improve the PWM called the advanced waveform extension (AWEX), which is specifically designed for this application. The AWEX is capable of handling four synchronous circuits, each with its own dead time, duty cycle, and phase. This design only utilizes one channel of the four. Using more channels could be used to interleave additional separate DC/DC converters to increase charge transfer.

One limitation, which will be covered more in a later section, is that the low system voltage of 2.2V. This low voltage reduces the maximum operating frequency of the microcontroller. While the microcontroller can operate at 12MHz at 2.2V, an 8MHz clock frequency was used to add a safety factor. This lower clock frequency limits the resolution that the duty cycle can be adjusted with fewer clock cycles in each period. The microcontroller has an additional module, which increases the clock resolution, not surprisingly called a high-resolution timer (HIRES). This module achieves a higher resolution by counting both rising and falling edge transitions instead of just one edge. The combination of the microcontroller's PWM module, AWEX module, and HIRES

module allowed the duty cycle, frequency, and dead time to be controlled reasonably precisely.

As shown before, a simplified version of the converter is shown in Figure 3.14. In contrast, Figure 3.17 shows the switching node on the left side and the enable/disable switch on the right side. The center figure shows how the two circuits are integrated. Each board has a switching node and an enable/disconnect switch. The enable/disconnect switch connects to a board of lower potential's switching node circuit. This is achieved by connecting a jumper between two screw terminals. The enable/disable switch is composed of two n-channel MOSFETs that are connected in anti-series: see Figure 3.17.

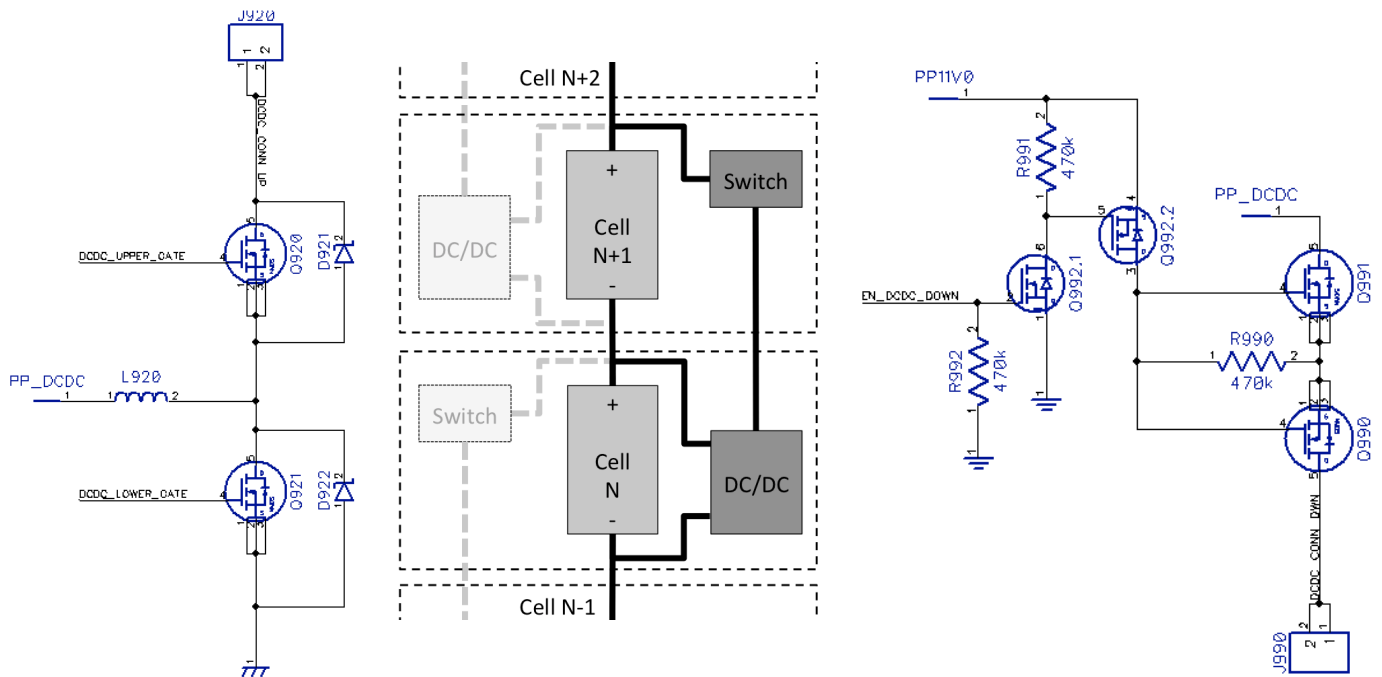


Figure 3.17 – This figure shows the sub circuits that connect together to make the active balancing DC/DC converter.

The image on the left shows the switches that make the synchronous buck-boost converter. Connector J920 connects to J990 on the far right image. The schematic on the right side shows the switch to enable or disable charge transfer. The middle diagram shows each board has a buck-boost circuit and a switch circuit and how they connect to cells of different potentials.

The switch circuit shown in Figure 3.17 is designed to block the DC/DC converter on the other board from operating in an unsafe condition. This circuit uses the same MOSFET as the rest of the converter circuit to minimize series resistance. The PP_DCDC net is connected to the positive terminal of cell N+1 in Figure 3.17. J990 is also a screw terminal (similar to J920) so that a very low resistance and low inductance connection can be connected between the two boards.

One problem associated with using a disconnect switch is that if the DC/DC does attempt to operate there may possibly be a voltage spike caused by the inductor. This voltage spike could damage the MOSFETs and other connected circuitry. Software communication between the two cells should prevent this from occurring, however a hardware backup was added. The hardware protection consists of a bidirectional voltage suppression diode added in parallel to inductor L920. This diode activates when the voltage exceeds 8 volts. When the cell is at a maximum voltage of 4V, this means that the peak voltage should not exceed 12V. The blocking MOSFETs breakdown voltage is 25V.

The voltage suppression diode should prevent the circuit from failing but continuous usage of the diode may cause it to fail. To alert the microcontroller of a failure condition, a comparator with a voltage threshold around 11V will detect an over voltage case. Under normal operation, the circuit should only reach a peak of 8V.

One final problem arose from this circuit: there was a significant amount of ringing. While this ringing was substantially reduced from previous revisions, it still could potentially over-voltage the MOSFETs. Most of the circuit components are placed as close as possible together and connected with as short of traces as possible, but

parasitic capacitance and inductances arise from numerous sources. Significant sources include the drain-to-source on the switching MOSFETs, the wire and bus bar connecting two boards, and the power resistors on the N+1 board. Also, the current goes through two different fuses also add some inductance. As a result, the circuit rings heavily when the low side MOSFET is disabled. To reduce this problem, simple RC snubbers were placed parallel to both the low-side and high-side switches ^{[21][22]}. Most snubber solutions only require a snubber on the low side switch. Since these were added in the final revision of the hardware, the high side switch also had a snubber in case it was required. By default these two snubbers were not populated with components. Thee snubbers are intended to be tuned after the initial characterization. The complete circuit is shown in Figure 3.18.

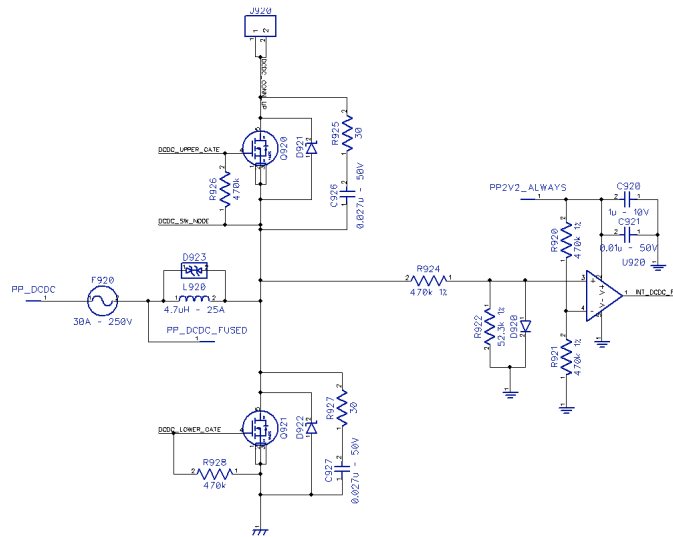


Figure 3.18 – Complete schematic of the buck-boost switches, snubbers, and disconnect protection.

3.1.4.A DC/DC Design Equation Development

One of the questions for this circuit was how to control it. While component ratings could be estimated and the circuit looks like a synchronous buck-boost, it has an added twist. This twist changed much of the math for a buck-boost. A typical buck-boost does not have a source on the output so Equation 3.5 does not provide much help since V_{in} and V_{out} are fixed and the duty cycle is user adjustable. As a result, the basic ideal equation typically used for a buck-boost is of little assistance and using a slightly more complicated model is required.

$$V_{out} = -\frac{D}{1-D}V_{in} \quad \text{Equation 3.5 - Buck-boost output function.}$$

As a starting point, the most ideal case was analyzed where both R_1 and R_2 are zero (see Figure 3.19) and the switches turn on and off perfectly so that the diodes do not conduct. With no losses, Equation 3.5 determines the duty cycle that will result in zero net charge transfer from cell to cell. Later it will be shown that this calculated duty cycle will approach 100% efficiency ideally.

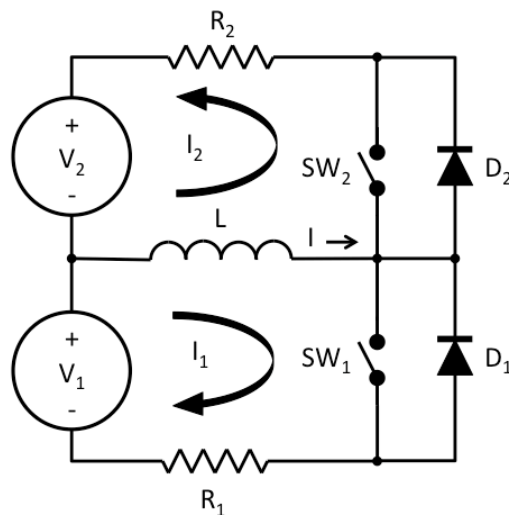


Figure 3.19 - Circuit of synchronous buck-boost.

The ideal case reveals no information about the current through the sources, inductor, or the switches. To generate a more useful set of equations the next case included adding series resistance into each loop. Both R_1 and R_2 are the lumped series resistance of the current loop from the source, inductor, switch, and any other sources of resistance. Equation 3.7 and Equation 3.8 calculate the current through source 1 and source 2 respectively.

$$D = \frac{V_2}{V_1 + V_2} \quad \text{Equation 3.6 – Duty cycle}$$

$$i_1 = \frac{V_1 - V_2 \left(\frac{1-D}{D}\right)}{R_1 + R_2 \left(\frac{1-D}{D}\right)^2} \quad \text{Equation 3.7 – Current through switch 1.}$$

$$i_2 = \frac{V_1 \left(\frac{D}{1-D}\right) - V_2}{R_1 \left(\frac{D}{1-D}\right)^2 + R_2} \quad \text{Equation 3.8 – Current through switch 2.}$$

$$\eta = \frac{P_o}{P_o + P_{loss}} = \frac{V_2 i_2}{V_2 i_2 + i_2^2 R_2 + i_1^2 R_1} \quad \text{Equation 3.9 – Equation to determine efficiency}$$

Equation 3.7 and Equation 3.8 were developed by setting the change in current through the inductor as a result of switch 1 to the change in inductor current of switch 2 equal to each other. Using Equation 3.7 and Equation 3.8, it is possible to estimate the efficiency of this circuit by starting with Equation 3.9. This case assumes charge is being transferred from source 1 to 2, but this can be done for the reverse as well. The resulting equation is shown in Equation 3.10. In the case that charge is being transferred from source 2 to 1, see Equation 3.11.

$$\eta = \frac{V_2}{V_1} \left(\frac{1-D}{D} \right)$$

Equation 3.10 – Equation for converter efficiency when transfer is from source 1 to 2. This is for the case of no dead time.

$$\eta = \frac{V_1}{V_2} \left(\frac{D}{1-D} \right)$$

Equation 3.11 – Equation for converter efficiency when transfer is from source 2 to 1. This is for the case of no dead time.

Despite starting with the resistive losses (diode losses were not included), the efficiency is purely a function of voltage and duty cycle. This could be more simply found by looking at output power over input power as a function of source voltage and current. Figure 3.20 plots the efficiencies and currents based on the presented equations. All values are plotted as the absolute value. Figure 3.20 also shows that the duty cycle with maximum efficiency is 0.5 which Equation 3.5 estimated for $V_1 = V_2 = 3.3V$. As previously noted, the efficiency is theoretically 100% at this point.

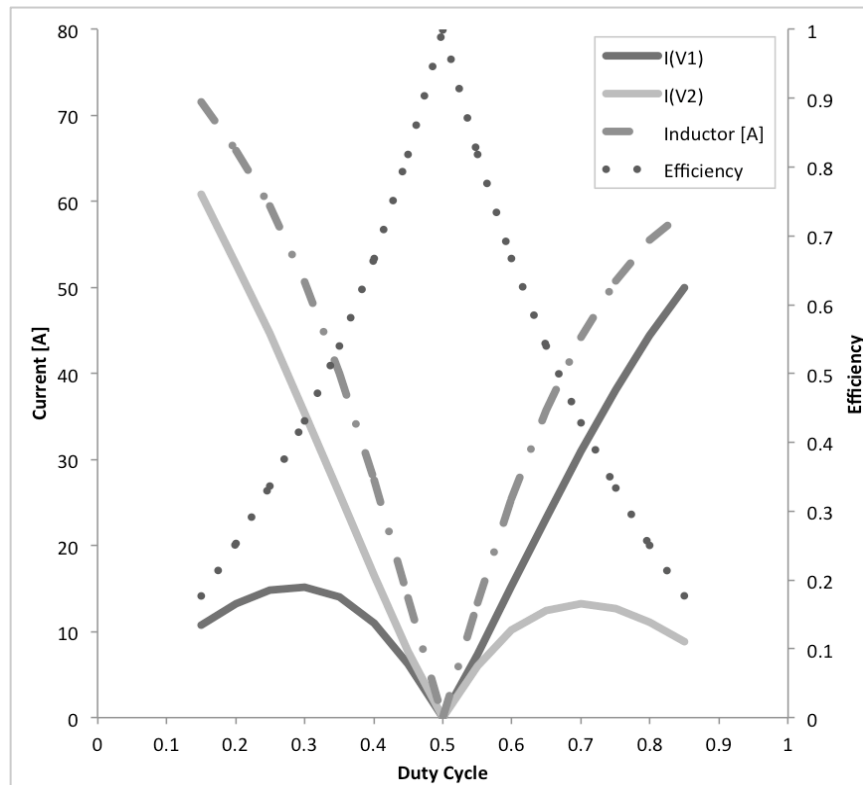


Figure 3.20 – Plot of inductor current, V1 and V2 current, and efficiency versus duty cycle. All values are absolute values. $V_1 = V_2 = 3.3V$. $R_1 = 53 \text{ m}\Omega$, $R_2 = 43 \text{ m}\Omega$.

The previously shown equations are interesting, however, they are highly academic because any real synchronous system requires dead time between high and low side switches. When dead time is introduced, the equations become significantly more complicated. In fact adding dead time causes the solution to require seven piece-wise functions to model the average inductor current. Figure 3.21 shows all 7 modes that the DC/DC can operate in. As the duty cycle decreases the waveform goes from a positive CCM state, to DCM, then to a second DCM state. Following the second DCM state it enters a CCM state (where the net current transfer is near zero). It then leaves the CCM state, goes through to two negative DCM states and finally to a negative CCM state.

The four DCM states all result in very complicated solutions. As a result, reducing the complexity was a goal. Simulations (and measurements) showed very little difference in duty cycle versus average current between the two DCM states between CCM states. As a result, the equations were simplified to a set of 5 equations. Positive CCM, positive DCM, neutral CCM, negative DCM, and negative CCM. The DCM state originally between the first DCM state and the neutral CCM state was removed (DCM 2 in the plot). Figure 3.22 shows the five states that the converter can operate in.

The duty cycle at the transitions from DCM to CCM or CCM to DCM can be calculated, however the closed form of the solution is incredibly long and impractical to use. As a result, performing a binary search on the intercept is the best method. In all of the following derived equations, both dead times (transition from switch 1 to 2 and switch 2 to 1) are identical and total dead time in a period is 2α . Dead time is modeled in terms of duty cycle rather than actual time. Additionally V_D is the diode voltage during dead time, L is inductor value, and f is frequency.

All of the equations were derived from a volt-second-balance across the inductor to determine the current. The equations for the CCM states were solved for the minimum inductor current for positive and negative CCM, and for maximum current for negative CCM. These equations can be easily converted to average current, however the equation is longer and difficult to clearly present. For DCM states the solutions use average inductor current because minimum inductor current is zero, which reveals no information about the inductor. The DCM equations were solved for the time that the diode current was zero and uses this to find the average inductor current. For derivations of all five states see the appendix.

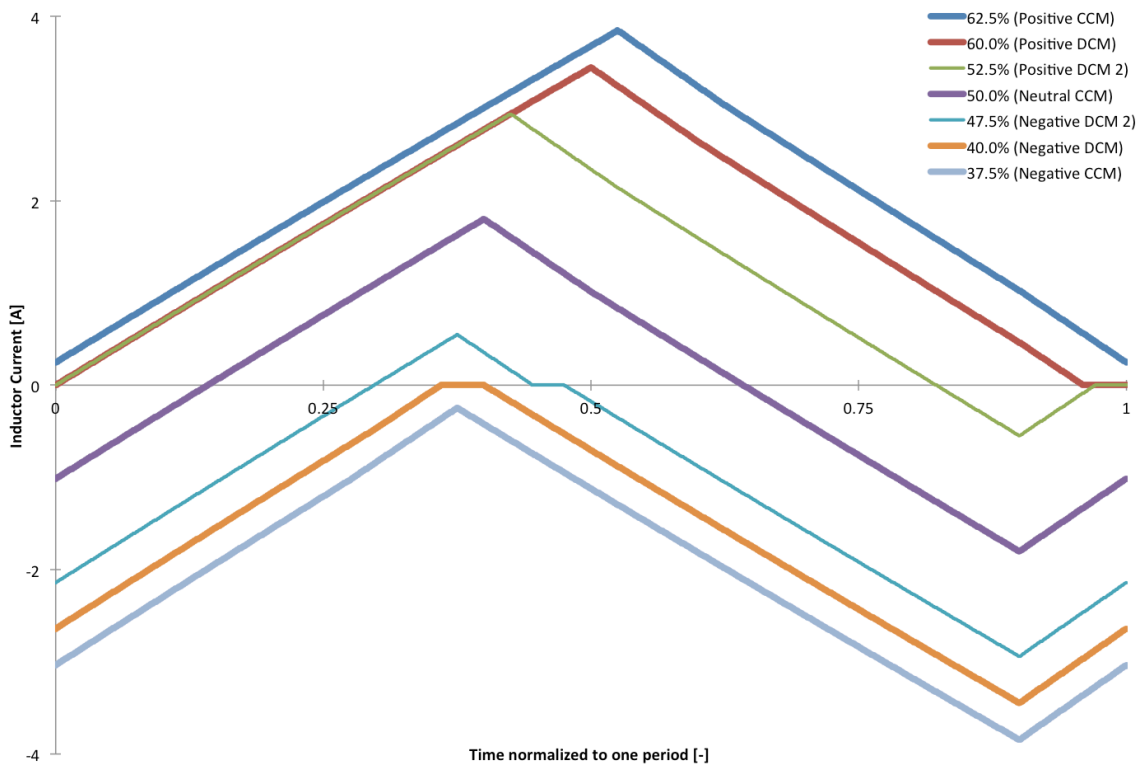
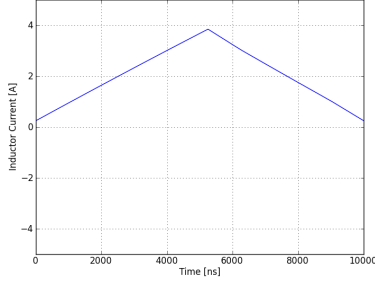
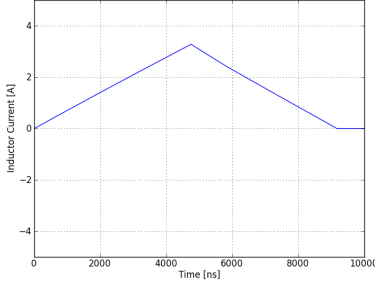


Figure 3.21 – Plot of all seven modes of operation of the DC/DC converter.



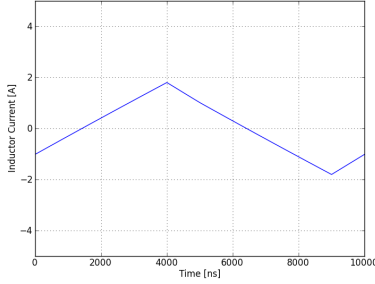
Positive CCM

$$i_{posCCM} \approx \frac{DV_1 - (1-D)V_2 - \alpha V_d}{DR_1 + (1-D)R_2}$$



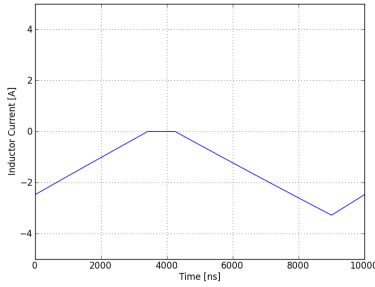
Positive DCM

$$I_{posDCM} \approx \left(\frac{1}{2}\right) \frac{D^2 T(V_1^2 + V_1 V_2) + D T V_1 V_d (1 - 2\alpha)}{D T R_2 (V_1 + V_2) + T R_2 (V_2 (\alpha - 1) - V_d \alpha) + L (V_d + V_2)}$$



Neutral CCM

$$i_{neuCCM} \approx \frac{(D+1)V_1 - (D+\alpha-1)V_2}{(D+\alpha)R_1 + (1-D-\alpha)R_2}$$

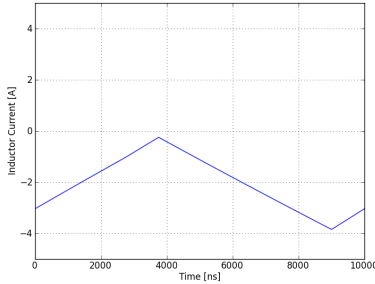


Negative DCM

$$I_{negDCM} \approx \frac{(V_2 T)^2 R_1 D^3 - \left\{ \begin{array}{l} V_1 [L - \psi(2\alpha - 1)] \\ + V_2 [L - 3\psi(2\alpha - 1)] \\ - \psi \alpha V_d \end{array} \right\} V_2 T D^2 - \left\{ \begin{array}{l} V_1 [2\beta - \psi(5\alpha^2 - 5\alpha + 1)] \\ + V_2 [2\beta - 3\psi(4\alpha^2 - 4\alpha + 1)] \\ + V_d [\beta - \psi(3\alpha^2 - 2\alpha)] \end{array} \right\} V_2 T D - \left\{ \begin{array}{l} V_2 [\beta - \psi(4\alpha^2 - 4\alpha + 1)] \\ + (V_1 + V_d) [\beta - \psi(\alpha^2 - \alpha)] \end{array} \right\} (2\alpha - 1) V_1}{2(T R_1)^2 V_2 D^2 - \left\{ \begin{array}{l} V_1 [L - \psi \alpha] \\ + V_2 [L - \psi(3\alpha - 1)] \\ - \psi \alpha V_d \end{array} \right\} 2\psi D - \left\{ \begin{array}{l} L V_1 \\ - V_2 \psi [2\alpha - 1] \\ + L V_d \end{array} \right\} 2(\psi \alpha - L)}$$

$$\beta = (2\alpha - 1)L$$

$$\psi = T R_1$$



Negative CCM

$$i_{negCCM} \approx \frac{(D+2\alpha)V_1 + (D+2\alpha-1)V_2 + 2\alpha V_2}{(D+2\alpha)R_1 + (1-D-2\alpha)R_2}$$

Figure 3.22 – Five modes that the synchronous bi-directional buck-boost can operate in.

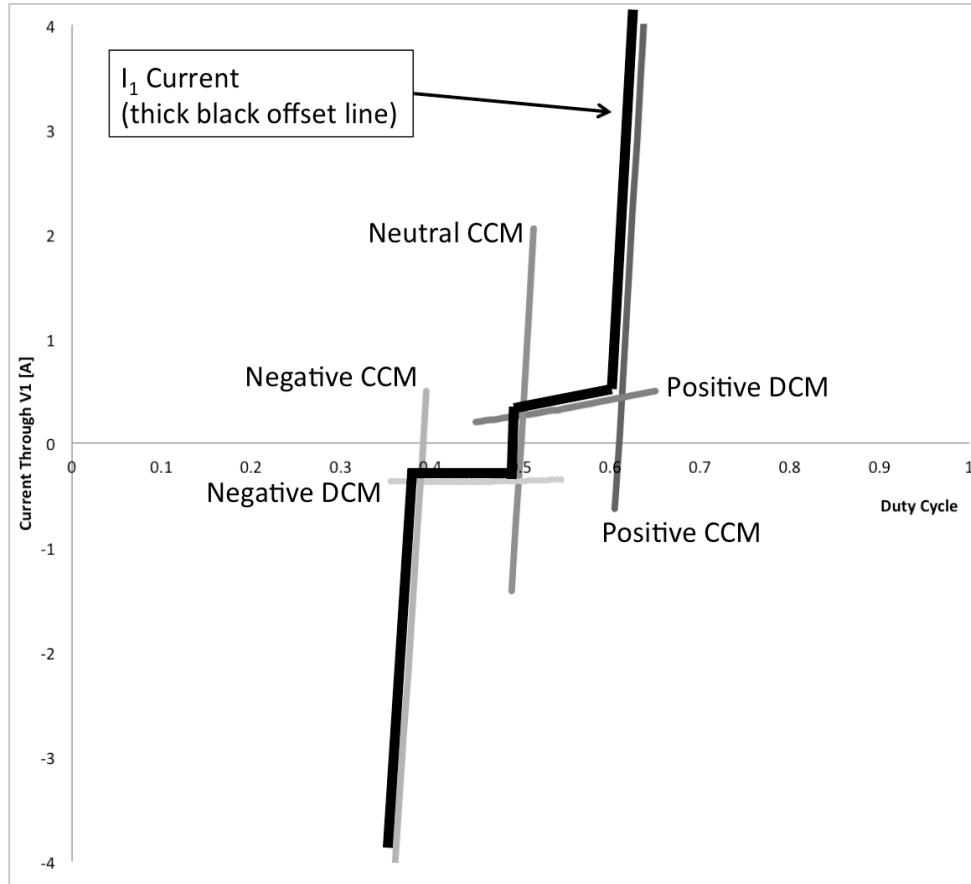


Figure 3.23 – Plot of average current through supply 1 versus duty cycle through all five modes of operation shown in Figure 3.22. The bold line is offset to make it easier to see.

To demonstrate the transition from state to state, Figure 3.23 shows how each of the above equations intersect each other on the same plot. The full result of the piecewise functions is shown in Figure 3.24.

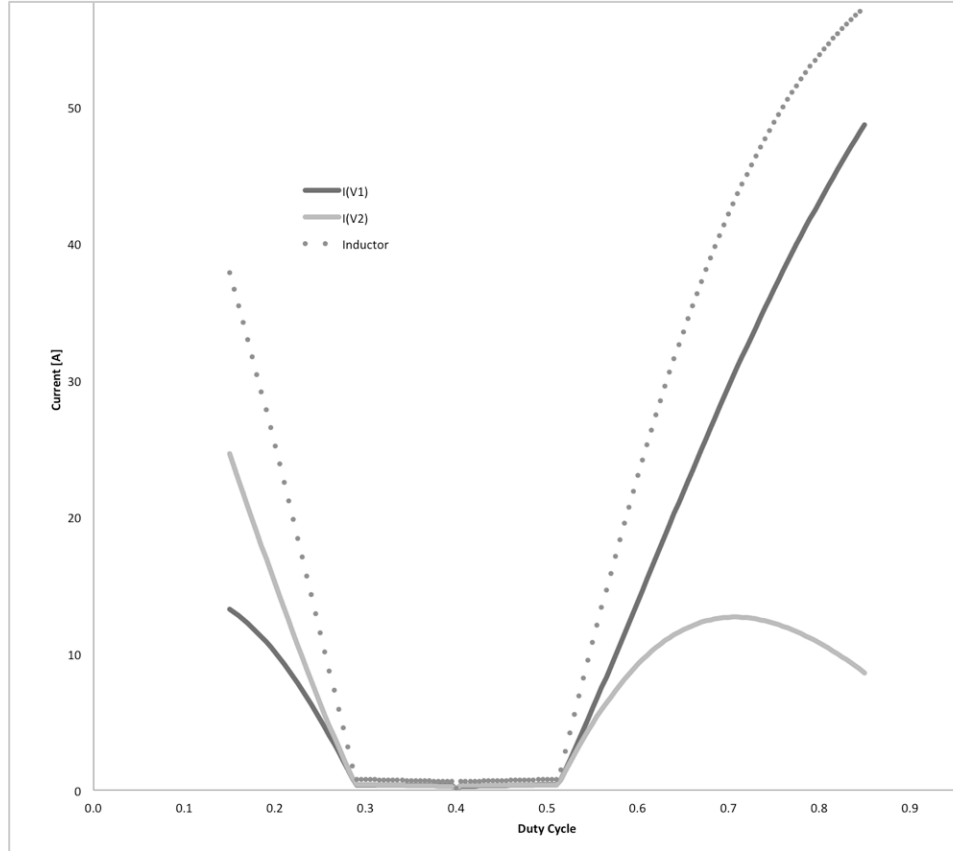


Figure 3.24 – Plot of inductor current, V1, and V2 current versus duty cycle. All values are absolute values. $V1 = V2 = 3.3V$. $R1 = 53\text{ m}\Omega$, $R2 = 43\text{ m}\Omega$, $\alpha = 10\%$, $L = 10\mu H$, $f = 100\text{kHz}$

3.1.4.B DC/DC Current measurement

Measuring the current of the DC/DC converter is essential to maintain safe and efficient operation. In revision A of the circuit, a discrete instrumentation amplifier (similar to the main current sense circuit described in a previous section) was designed. The initial circuit utilized a single $250\mu\Omega$ resistor to sense the current however this required a large gain because the peak current was only 30A. To achieve a maximum voltage output, a gain of 400 was selected. However, this circuit was severely impacted by the offset error from taking the difference of two voltage dividers. In many cases, the

circuit saturated with zero current through the resistor. Additionally, the selected amplifiers did not have sufficient bandwidth to capture a 100kHz⁵ signal. To remedy these problems in revision B, higher bandwidth amplifiers were used. A 1mΩ sense resistor was used and 0.1% tolerance resistors were used in the voltage divider. However, this circuit cost nearly \$20 in components. It also required several milliamps of current to operate, which meant that the microcontroller had to disable some of the LDOs to minimize power usage. It also added more components, which made for a less than optimal routing solution on the PCB. As a result, this circuit was removed in the final revision.

While there is no direct measurement of current through the inductor, the final solution for the main current sensor (described in 3.1.3.b) has sufficient bandwidth to capture the 100kHz signal. Also with the microcontroller's 2 million samples per second sample (MSPS) rate, it is possible to estimate current being sourced or sunk by the cell. This solution is not perfect, but it does reduce the overall bill of materials cost, radically improves the routing solution on the PCB, and reduces the resistance of the DC/DC by removing one more sense resistor.

3.1.5 Safety

The goal of this project is to design a battery management system. One important role of a BMS is to prevent damage to the cell or the users. The 100Ah batteries used in

⁵ 100kHz is the frequency that the DC/DC operates at.

this project are capable of sourcing a significant amount of power in the case of a short circuit. To protect the batteries, most of the connections are fused.

In the case that one DC/DC converter fuses fail, the DC/DC sub-circuit will not operate. This will prevent balancing but the battery will not cause damage to itself or the surroundings. There is no hardware circuit to detect a blown fuse so future improvements of the software will have to determine how to detect this failure. A failure of the DC/DC disable switch will cause the over-voltage detector to trigger. The fuse in series with the inductor will not trigger the detector. In this scenario, the circuit is wasting a small amount of power, but no damage will be caused by continuous operation.

In the event that the fuse to the logic fails, a larger problem occurs. In this situation, there no longer is power to enable or disable gates. As a safety design, all power MOSFETs have a resistor between the gate and source to discharge the gate. This will ensure that any active gate will automatically be disabled in a power loss state.

Other safety concerns occurs when the cell reaches a critically low or high voltage or excessive current into our out of the cell. A several hundred-amp fuse would easily handle the excessive current cases but it would be unable to protect a low voltage or over voltage cell. In addition to be an incomplete safety solution, there are other issues with using a fuse: first each of these fuses can cost several hundred dollars, which is more than the entire circuit board cost. Second, these fuses are as large as the entire circuit board, which leaves very little room for any components. Since voltage and current protection was required, a disconnect switch using 8 power MOSFETs was constructed. The circuit is composed of four parallel MOSFETS in anti-series with another set of four to make switch capable of blocking current in both directions. See Figure 3.25.

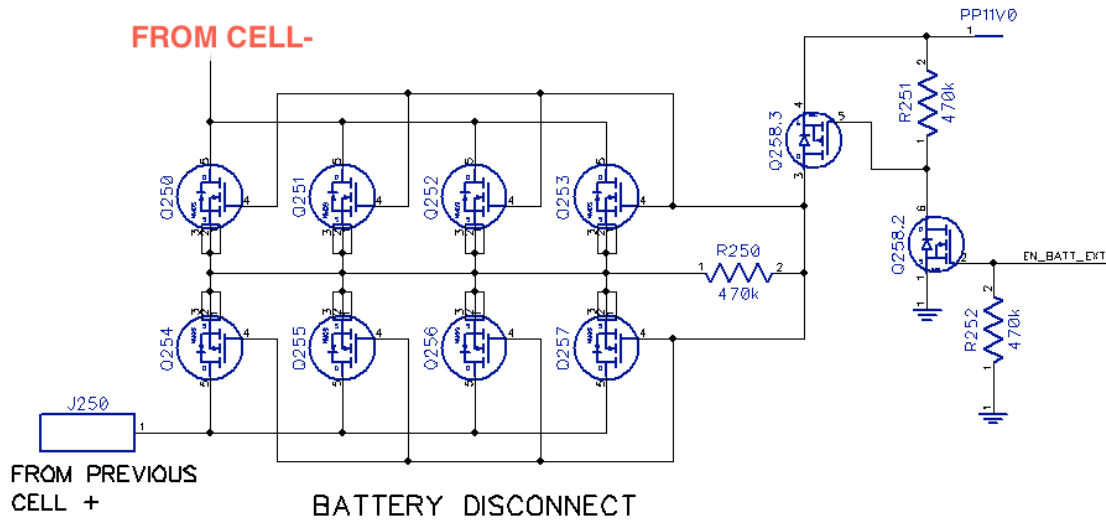


Figure 3.25 – Schematic of the emergency disconnect switch.

This circuit is capable of handling 800A continuously (an improved cooling solution must be added to achieve this) and surges that exceed several thousand amps. By using this many MOSFETs in parallel, the DCR is decreased significantly and reduces the loss through the disconnect switch. The gate driving mechanism can enable the switch very fast, however it is reasonably slow to disable. It takes approximately 50ms to completely turn off the switch. This slow discharge was purposefully designed to prevent an inductive kick. With conceivably hundreds of amps going through this circuit, turning it off very fast would cause the parasitic inductance of the current path to increase the voltage until it breaks down the MOSFET.

Finally, the power sense resistors and power pulse resistors both can get hot and neither is rated for high wattage. To protect these circuits from fire, thermistors were placed near each of the respective circuits and are monitored by the analog-to-digital converter of the microcontroller. Using a similar calibration to that of the external temperature sensor, they ensure that the resistors remain in a safe operating region.

3.1.6 Input power

Designing a good input power filtering and protection became very important to this design as it became apparent that a battery cell could provide a harsh voltage environment. Revisions A and B used only a small resistance and a large capacitance to filter the input using. Unfortunately, early testing showed that the terminal voltage could fluctuate several hundred millivolts. With such a large input capacitance (1mF), the fuse blew immediately. Using such a large capacitor was also quite bulky and limited placement locations. As a result, a LC filter with damping was used as the primary input filter. Figure 3.26 shows the low-pass filter design. This filter has a smaller input capacitor (10 μ F) that allowed for a ceramic capacitor to be used instead of a large electrolytic capacitor. Also since the damping capacitor must be larger than the storage capacitor, using a smaller capacitor was beneficial. The inductor was selected to only be 10uH so that the component would be small. Using a simple LC filter only would cause a dangerous condition at 16kHz where the circuit would resonate. Since the input frequencies could not be know at the time of designing, all frequencies must be considered. In the case of a 16kHz input frequencies, the output would be nearly 20dB greater than the input. To suppress this, the circuit was damped using a RC circuit. To determine the damping capacitor C101, an approximation of four times larger than C100 was used to select 47 μ F. To estimate the resistive component of this circuit, the following equation was used:

$$R_{105} = \sqrt{\frac{L_{101}}{C_{100}}}$$

Equation 3.12 – Equation to estimate series resistance if snubber.

This resulted in an estimation of R105 being 0.5Ω . Simulation of this circuit showed that when using the damping circuit was used, the peak output gain was only 1.6dB instead of the previous 20dB. Additionally, the cut off frequency shifted down from 16kHz to 11.5kHz.

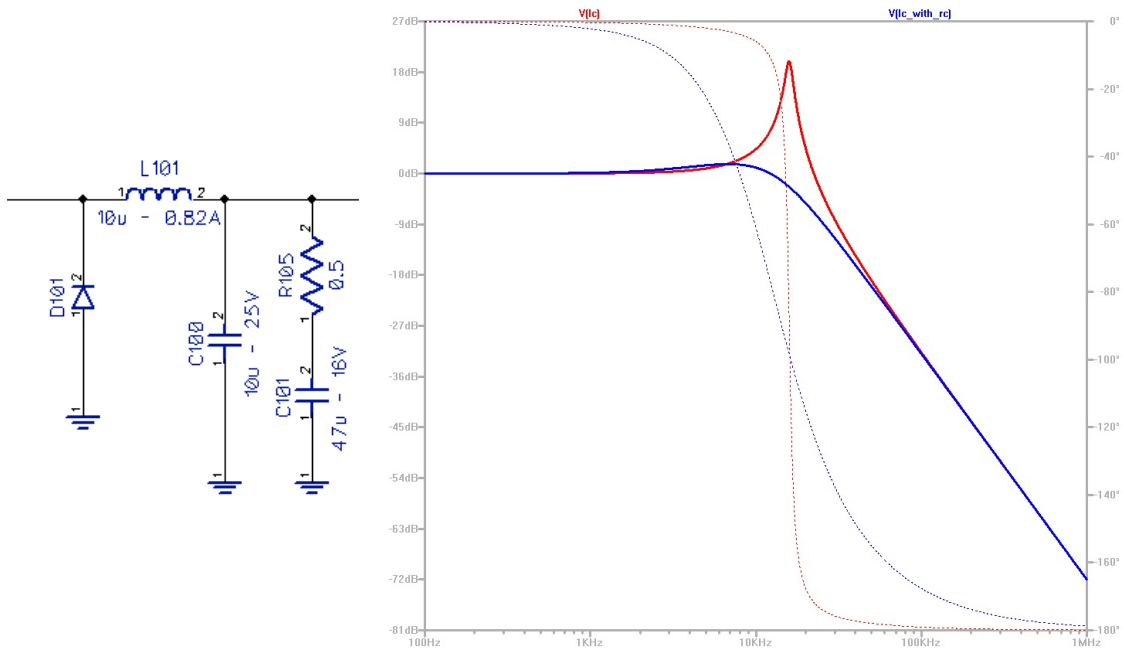


Figure 3.26 – Schematic and plot of frequency response. The plot shows LC filter only versus LC filter with RC damping.

While the input is protected against high frequency noise, there are three other circuits protecting the logic from the user and the environment. First, there is a fuse to protect in case of a short. This fuse is rated for 820mA, but the circuit should not exceed 400mA input. Next, there is a bidirectional voltage suppression diode that triggers at $\pm 8V$. The diode protects the negative and over-voltage protection circuits from breaking down their MOSFETS. Finally, there is a negative-voltage and over-voltage protection circuits.

The negative-voltage circuit protection is composed of a single P-channel MOSFET (Q100). This circuit is achieved by connecting the gate to ground, the drain to

the input, and the source to the output. When the input voltage is negative, the source voltage is discharged to the same voltage as the gate, which disables the MOSFET. However, when the voltage on the drain increases with a positive voltage, the MOSFET enables.

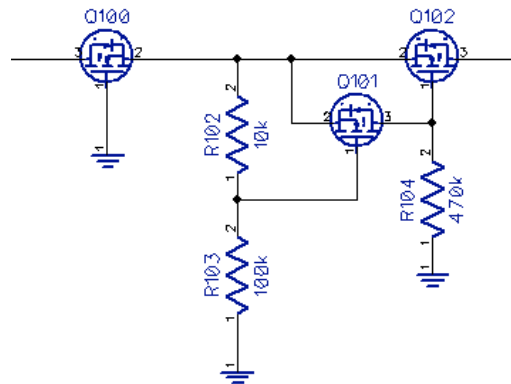


Figure 3.27 – Schematic of over-voltage and negative voltage protection on input.

The over voltage circuit protection is achieved by combining R103, R102, Q101, Q102, and R104. In a safe operating voltage Q102 conducts current through. When the input voltage reaches a certain threshold the voltage divider network R102 and R103 enable the MOSFET Q101, which disables Q102.

3.1.7 Other Electrical Design Considerations

3.1.7.A Input voltage range

The working voltage range was primary dictated by the cell operating voltage. The safe working voltage for this circuit is between 2.5 and 4.3V. The initial goal was to make the working range between 2.2 and 4.3V. While the upper end can be lowered, there is no reason to do so as the LDO's can safely operate up to 4.5V. The reason for

increasing the minimum voltage was to ensure the analog LDO's operate correctly. Additionally, the boost circuit is designed to not brownout until below 2.5V. While the input range is smaller than desired, this does not impact compatibility with other cell chemistries. Most cells, including the LiFePO₄ cells used for testing, operate a voltage range between 3 to 4V. Using a system voltage lower than 2.2V was an option, but the number of available components becomes very restrictive and other design goals would have to become more flexible: most notably low power consumption.

Low power consumption turned out to be a challenging design goal. All of the ICs selected have very minimal quiescent current draw. Typically ranging from 1 μ to 150 μ A. The microcontroller is a special case. During normal operation, it can draw between 1 and 10mA depending on what internal modules it is using. However in sleep, the microcontroller can drop down to 200 μ A. The goal was to reach less than 1mA on average during normal operation by using a combination of sleep and active states.

3.1.7.B Communication

Another feature of this design is the communication scheme between each of the cells. This feature is absolutely critical for safety and convenience of the user. A lot of time was spent trying to design a system that was simple and robust enough to work with any cell configuration. Research revealed some interesting techniques of using current to communicate to a higher or lower potential. However, these systems did not work if the two cells were at the same potential. In the end, opto-isolators were used despite having to power an LED with 10 to 20mA.

Communication is based around each channel using a Universal Asynchronous Receiver/Transmitter (UART). This posed an initial challenge of finding a low power microcontroller with at least four UARTs. The XMEGA32A3 was selected with seven USARTs (Universal Synchronous and Asynchronous Receiver/Transmitter), which can be used in a UART mode. Using this system allows for bidirectional communication with only two wires and allows for near transparent transfer through opto-isolators.

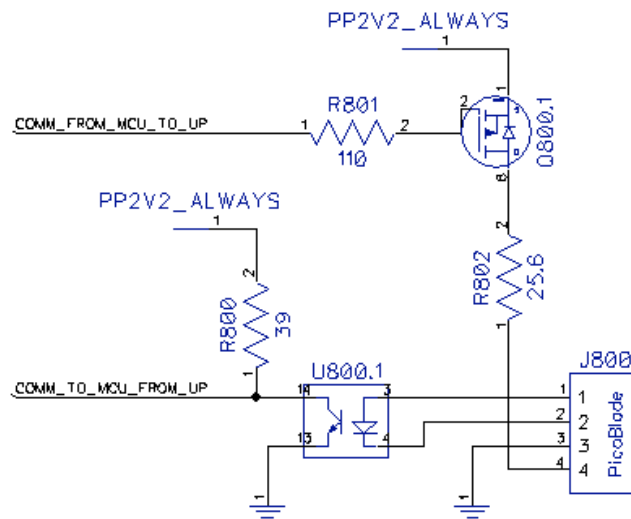


Figure 3.28 – Schematic of single channel transmitter and receiver for isolated communication.

One thing that needed to be accounted for is that UART communication idles in a high state. This would consume a lot of power to always be running the LEDs. To prevent excessive power consumption, the output from the transmit pin (net COMM_FROM_MCU_TO_UP in Figure 3.28) goes to the gate of a p-channel MOSFET. This inverts the logic so that the LED only enables when the transmit pin goes low. On the output of the opto-isolator, the logic is inverted again so that the receiver side (net COMM_TO_MCU_FROM_UP) will have the same state as the

transmitter side. The circuit shown in Figure 3.28 is only one of four identical communication circuits. The other three are for left, right, and down.

To connect the boards together, Molex PicoBlade[®] connectors were used. These are 0.050in pitch wire-to-board connectors to minimize the required space. J800 is an example of one of these in Figure 3.28. The connector is placed on the diode side of the opto-isolator side so that the transmit side is powering the diode on the receiver side's board. This was done so that the communication through the cable was pulses of current going to a low impedance sink instead of a high impedance sink. This helps to reduce the effect of noise coupling onto the communication lines.

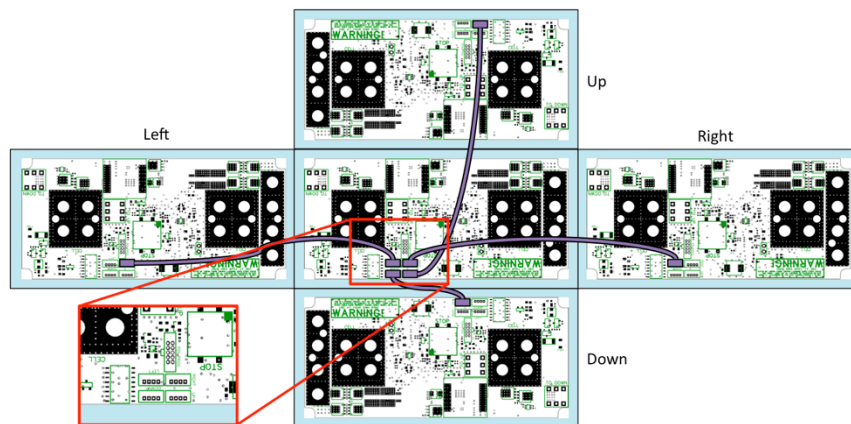


Figure 3.29 – Multiple board communication wiring diagram

3.1.7.C PCB

The careful design of the printed circuit board (PCB) was just as important as careful selecting components. In many cases the routing alone can induce failures, even in perceived simple and robust designs. Parasitic effects from poor or unavoidable choices in routing can result in desirable results such as data corruption or ringing.

Another important concern for routing is how the ground planes/nets are routed so that current surges do not circulate near sensitive analog components.

During revision A's component placement and routing, the goal was to use a 2-layer board to minimize cost. However, during placement it quickly became apparent that it would be impossible to find an acceptable routing solution with so many high current components in close proximity to highly sensitive analog circuits. To prevent potential problems, revisions A and B were both routed on 4-layer circuit boards. All revisions of the board used only through-hole vias. Blind and stacked vias were not used because of their higher cost. The stackup was as follows:

- 1 – Signal and components (Top)
- 2 – Power
- 3 – Ground
- 4 – Signal and components (Bottom)

The problem with even a 4-layer stackup is the complexity of the circuit required that few traces could have a simple straight shot from start to finish. This caused many traces to change layers numerous times. Every layer change blocks routing through and around the layer change. As a result, other traces were forced to route around this location. The end result was a complex set of traces woven into each other. This introduced crosstalk, parasitic elements, and reduced the locations that components could be placed. Additionally the power planes were pierced many times making the power planes less effective. In revision B of the hardware, to protect the analog signals from electrical noise, the top layer was filled in with a ground plane to protect the analog circuit as much as possible. This caused two layers of signals, power planes, and ground panes to all share 3 layers. This solution did prove to be noise resistant from external

sources, however the solution was not optimal since there was too much interaction between the nets as they weaved in and out of each other.

In the final version, revision C, a 6-layer circuit board instead of 4-layer was used. Using 6-layers improved the routing solutions dramatically: significant reduction in layer changes, more space to separate nets and shield them from each other, less vias piercing ground and power planes, more room to place shielding around the analog nets, and less interaction of the high current nets with the analog nets. Unfortunately, the cost to fabricate the board more than doubled. The stackup is as follows:

- 1 – Components and signals (in analog area: short connections and minimal components)
- 2 – Signal (as little analog on this layer as possible)
- 3 – Power planes
- 4 – Ground
- 5 – Signals
- 6 – Components and signals (in analog area: short connections)

This stackup resulted in a very solid ground plane and clean power planes. Figure 3.30 shows the ground layer and Figure 3.31 shows the power layer. Additionally, any layer that has free space, it is filled with the corresponding ground plane (analog or digital). Another benefit of not using a discounted board spec was that there was no limit on the number of vias that could be used.

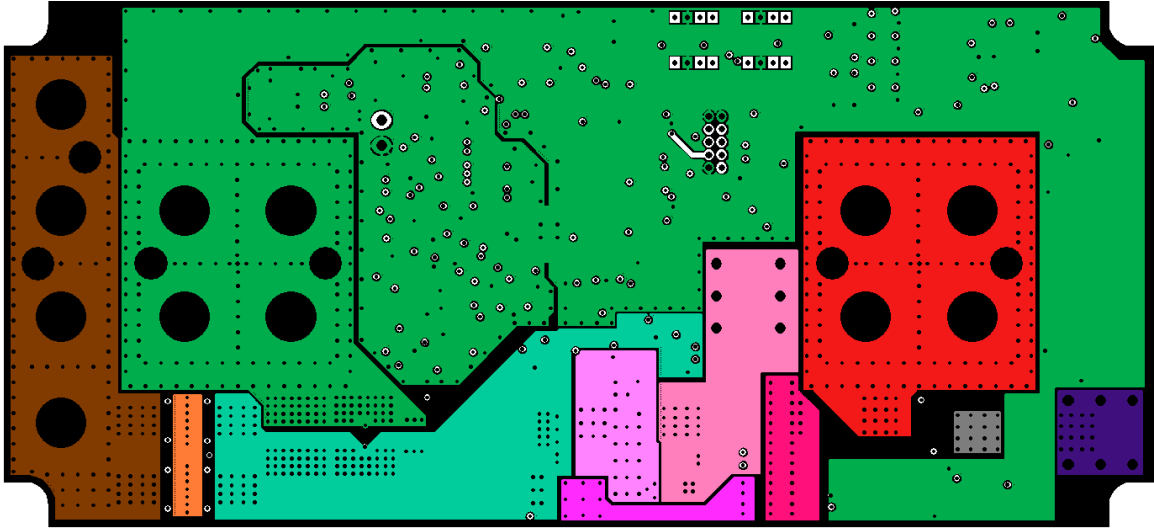


Figure 3.30 – A screen capture of the ground plane layer (ISL4). The analog and digital grounds are merged on this plane. Green shows ground. The high current areas did not have ground fill, however the teal area is similar to a ground.

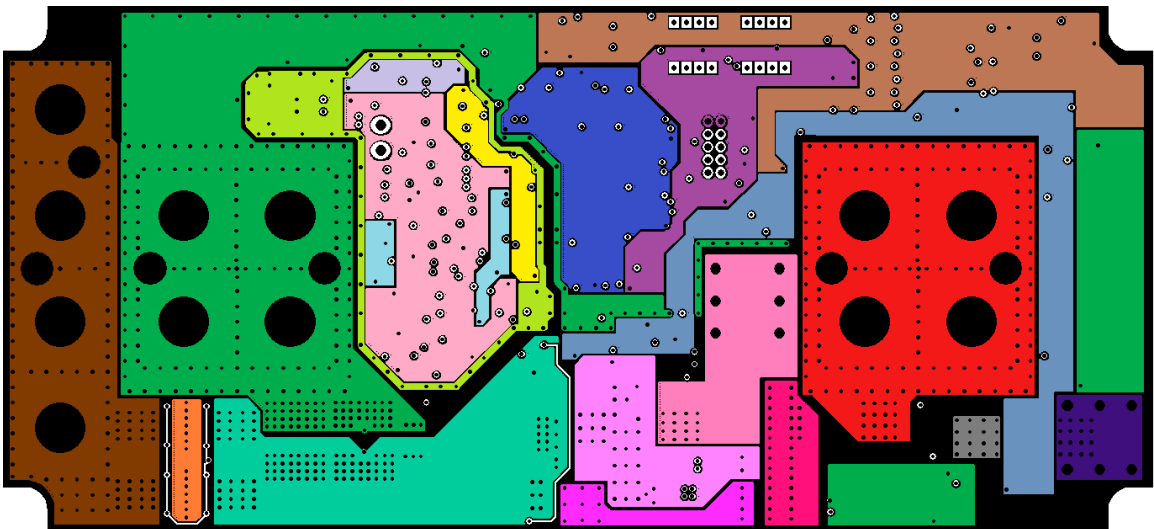


Figure 3.31 – A screen capture of the power plane layer (ISL3). Dark green is digital ground. Pale green is analog ground.

In revisions A and B, the 4-layer discount spec required that no more than 35 vias per square inch be used. This limited the design to roughly 350 vias. Revision C had no via limit and as a result, there is just over thousand vias. While revision C has significantly more vias than previous revisions, it has significantly less vias in areas where signal traces are routing, which permits cleaner routing solutions. See screen

captures of the signal layers shown the Appendices (Figure 5.16 and Figure 5.19). The vast majority of the vias are used in the high current areas. This was done to minimize the resistance due to vias, which can be a couple milliohms per via ^[23]. Another usage of vias was for connecting the ground planes on multiple layers very tightly together. This was done to minimize any ground bounce due to inductance associated with the vias. One final usage was ground stitching, which was most heavily used in the analog area. By placing vias at the edge of the ground plane and spacing them close together, they create a faraday cage around the analog signals. While this shield is not perfect it provides some protection while also lowering the ground plane's resistance.

Finally, thermal reliefs were used on the component pads as any design would. It is worth noting that a few thermal reliefs were omitted to improve the connections around the high current areas. There were a few particularly difficult to solder components as a result of this. While they are difficult to solder by hand, it is still possible. Unfortunately this means that in a production line, a reflow oven may not be capable of soldering some of the components.

3.2 Software

The software for this project evolved each time a new revision of hardware was completed. The first revision of the software was written for the Atmel XMEGA32A4 microcontroller (MCU). This controller has 32KB of program memory and 2KB of RAM. This MCU was selected because it was under \$6 per IC, yet still had a 12-bit 2MSPS ADC (mega-samples-per-second analog-to-digital converter) built-in, which

would minimize the difficulty of interfacing with a high speed ADC. Also, this chip is built on the AVR core, which would allow Arduino to be loaded onto the MCU if assembly, C, or C++ was not desired. With the low cost and high speed ADC, this chip was selected despite its small RAM. The RAM was a concern because this type of project would greatly benefit from a real-time operating system (RTOS). An RTOS would allow for relative ease of controlling timing constraints while keeping the code modular. Unfortunately, RTOSs require a significant amount of overhead in RAM space and some extra overhead in the program memory. With only 2KB, an RTOS would not fit and so the less optimal solution of a round-robin type control structure was used. It is worth noting that by revision B of the hardware, the MCU had been upgrade to the XMEGA128A3 with 128K of program memory and 8K RAM, which could handle an RTOS. However there was not enough time to convert the code from round robin to RTOS.

In writing the code there were three options: use an Arduino variant for the XMEGA, use the Atmel supplied libraries, or write everything from scratch. The most logical choice would to be do one of the first two. The author did the third option. The reason for this choice was that the first two options obfuscate the operation of the hardware from the user. Since this was the first time using the XMEGA chipset, writing everything from the ground up was a good way to learn it, unfortunately it took nearly three and a half months. If this project started over, with the current knowledge, using premade libraries would be the preferred choice. Figure 3.32 shows a basic block diagram of separate modules that make up the design of the software.

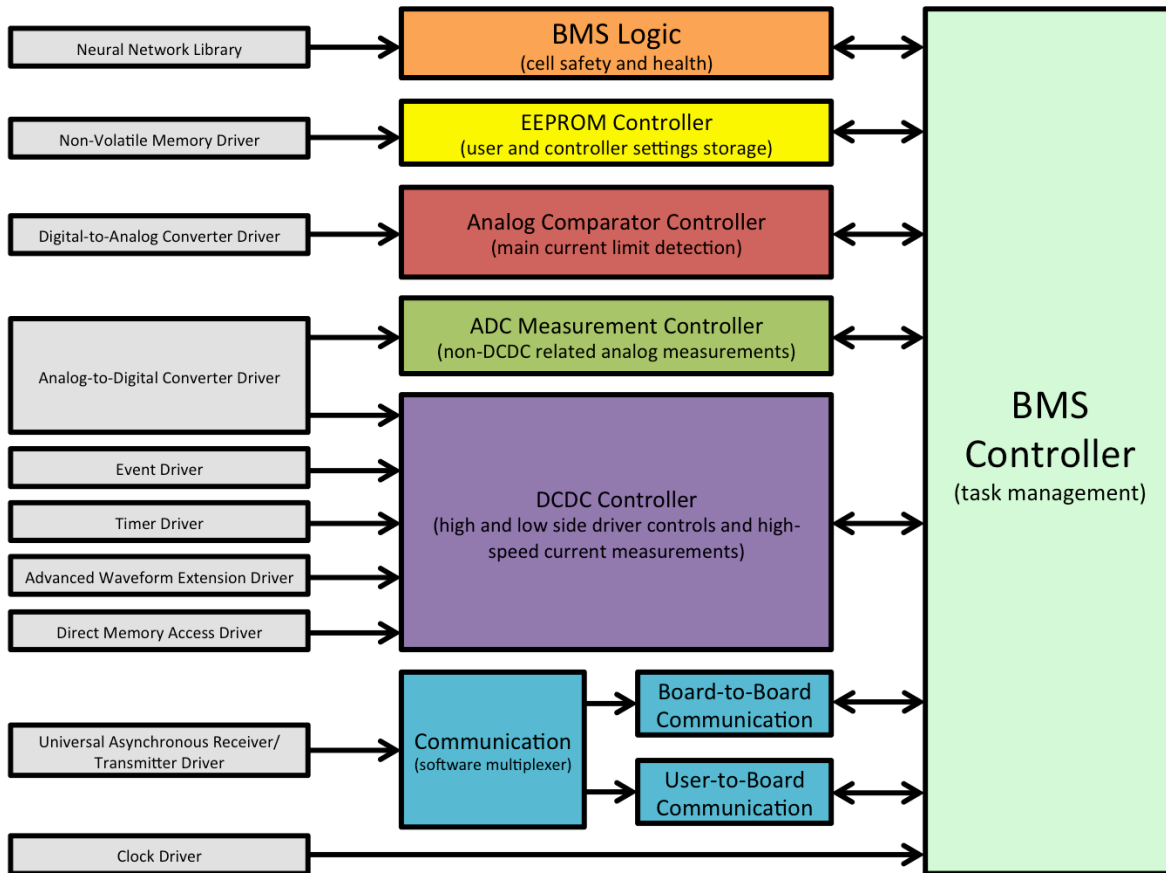


Figure 3.32 – Block diagram of software design.

3.2.1 Task management

As mentioned previously, the first MCU lacked sufficient RAM storage to run a RTOS. Since the author of the code was only proficient in basic software development, using the simplest task management algorithm was the safest route. However, a simple loop between tasks or even using round robin scheduling has limitations. Ultimately a queuing system was utilized to achieve the scheduling requirements.

The design behind the queue was based off how the hardware interprets commands and turns them into actions. The software adds an operation code to the

queue. It eventually reaches the front of the queue and is executed. There was a value associated with it, which also permits a timeout if the operation cannot be performed.

In the event that a timeout does not occur, the operation code is placed on the queue and has to make its way to the front again. While this is not a precision controlled timeout, it does achieve the goal of removing tasks that cannot ever be completed. In most cases, the timeouts are used for communication between cells. It is also used to create a delay between operations and yield to other operation codes that can be performed.

3.2.2 Logic Controller

The logic controller is the collection of functions that would ensure the health and safety of both the cell and users. While this function is arguably the most important function, it was never completed because it would be of little use without the drivers written first. With limited time to develop the software and hardware, the software drivers to validate the hardware was done first. It would have been possible to write the logic controller and test it via simulation, but the hardware could not be tested. The intended goal of this block would be to utilize both neural networks and fuzzy logic to help adapt to the hardware because each board will be slightly different.

This block was also intended to improve efficiency as much as possible. For example, the balancing DC/DC could always run so that all cells are equally balanced. However, if they are only transferring a small amount of charge at a time, the overhead of the transfer makes the efficiency very low. Also, if the system attempted to transfer at

maximum current and then stop, again the efficiency would be lower. The plan was to utilize this logic block to attempt to transfer charge at the highest efficiency without allowing the cells to have too large of a difference in useable capacity.

3.2.3 DC/DC Controller

The DC/DC controller was designed to interface the hardware drivers with the task management system. The DC/DC controller manages the hardware switching signals, the DC/DC down connection switch, and the DC/DC disconnect (over-voltage detection) circuit.

The hardware switches are driven by two complementary signals with inserted dead time. This is achieved by using the 16-bit timer on port C. The timer was configured to output a pulse-width modulation (PWM) waveform at a desired frequency and duty cycle. However, when the PWM was operating at 100kHz, it had only 80 discrete duty cycle values. By utilizing the hi-resolution module in the XMEGA, 640 discrete duty cycle values were achieved. The hi-res module does this by clocking on both rising and falling edges and ignoring the least significant bits of the counter. The next step was to include the Advanced Waveform Extension (AWeX) to achieve a complimentary set of waveforms. This waveform also included a set of registers to control the deadtime between high-to-low transitions and low-to-high transitions.

Outputting the waveform was only one part of the control system for the DC/DC converter. Monitoring the current was also a critical component. At steady state, the current was expected to be a triangular waveform flowing through the inductor. In

revision A and B of the hardware, there was current sensing through the inductor. In revision C, this was removed to save space and cost. By capturing current measurements at 2MSPS, twenty current measurements could be captured per period of the waveform. This would still permit an estimation of the operating conditions of the converter.

To achieve a sampling rate of 2 MSPS, the event system module and the direct memory access (DMA) modules were used in conjunction with the ADC. The DMA allows for memory to be pulled from a given location and moved to another location in a very predictable low number of clock cycles. Additionally, the DMA can be configured to automatically increment or decrement the data address to store large amounts of data. In order to use the DMA, it has to be triggered by software or a hardware event. Since software is slower than hardware, the event system was configured to have the ADC trigger an event on the DMA upon completing a conversion. Using these three modules together achieved the maximum sampling rate.

The ultimate goal was to have closed-loop feedback by measuring the current. However, this code was never completed. Currently only manual control of the DC/DC converter is possible. The current can also be manually measured, but there is no code written to link them together. Additionally, the interrupt service routine for the over-voltage detector (DC/DC disconnected state) was never written. Finally, the MCU used in revisions B and C had two ADCs, both capable of sampling at 2MSPS. It was intended to use the second one to monitor the cell voltage simultaneously to gather information on the voltage and instantaneous power.

3.2.4 ADC Controller

The ADC (analog-to-digital converter) controller is another block of code to make the interfacing with the hardware less difficult to understand. The ADC driver has simple functions to set various registers for any XMEGA platform (by changing the header file). This controller is primarily used on signals that are sampled at a slow rate, for example to probe the instantaneous voltage of the cell.

Since all of the signals are converted to a count between 0 and 2048, the code scales the appropriate signal to the correct units. Additionally, the controller supports user calibration of all of the analog signals. It uses a value defined in the header file, but has been set to a default of 5 user calibrations. It then performs a linear interpolation to find a best-fit line for the calibration values and returns the R^2 value to the user so that they know if they have any outliers in the calibration. Future improvements would be to use a third order interpolation because the ADCs are non-linear.

3.2.5 Analog Comparator Controller

The analog comparator controller is very basic and only monitors two things: the two digital-to-analog converters (DACs) and the external interrupts coming from the comparators. The comparator compares the DAC output values with the analog 800A current measurement signal. By adjusting one of the DAC's output voltage, it sets the threshold for detecting an over discharge or over charge. Each over current state has its own DAC output. Currently the code has been written to drive the DAC with a desired output. However there is no code to convert a desired current to a 10-bit unsigned

integer. Additionally, there is no code written to process the event of an external interrupt output by the comparators.

3.2.6 Communication Controller

The communication controller is the combination of two smaller controllers. There is the internal communication for board-to-board communication and a separate one for communication with an external source, which in most cases is a computer. Each of the four connectors (for communication cables) has a dedicated UART channel.

By default all of the channels are configured to be internal (board-to-board). Board-to-board communication is exceptionally basic as only basic information is transferred between boards. All of the internal communication is based around a request for information and a response. In most cases, the request is a lowercase character and the response begins with a capital version of the same character. Each request expects a certain number of bytes to be returned. For example, a request for a cell's voltage would be responded with a five-byte response. The response starts with an uppercase character followed by four bytes that make up the floating-point value. For basic error catching, each message is encapsulated in a '{' for start message and a '}' for end of message. See the example below in Figure 3.33 where one board requests another board's cell voltage.

```
Board 1 sends battery voltage request to board 2: {v}  
//Message would actually be sent as the following bytes: 123 118 125  
Board 1 puts a task on its own queue to process response with a set timeout limit.  
  
Board 2 receives battery voltage request from board 1: {v}  
Board 2 puts a measure battery voltage task on its own queue.  
Board 2 puts a send battery voltage task on its own queue.  
Board 2 eventually measures battery voltage.  
Board 2 sends battery voltage response to board 1: (V3.123)  
//Message would actually be sent as the following bytes: 123 86 59 223 71 64 125  
  
Board 1 receives battery voltage response from board 2: (V3.123)  
Board 1 processes battery voltage task.
```

Figure 3.33 – Example of communication between two boards.

Only basic requests and responses were written for the DC/DC converter as it is the only code that needed it at the time. The goal however was to design it so that a more generalize command could pass larger amounts of data through. This could be utilized so a computer could access any board's data in the network without it directly being connected. Figure 3.34, shows an example of a computer communicating to a board that it is not directly connected to.

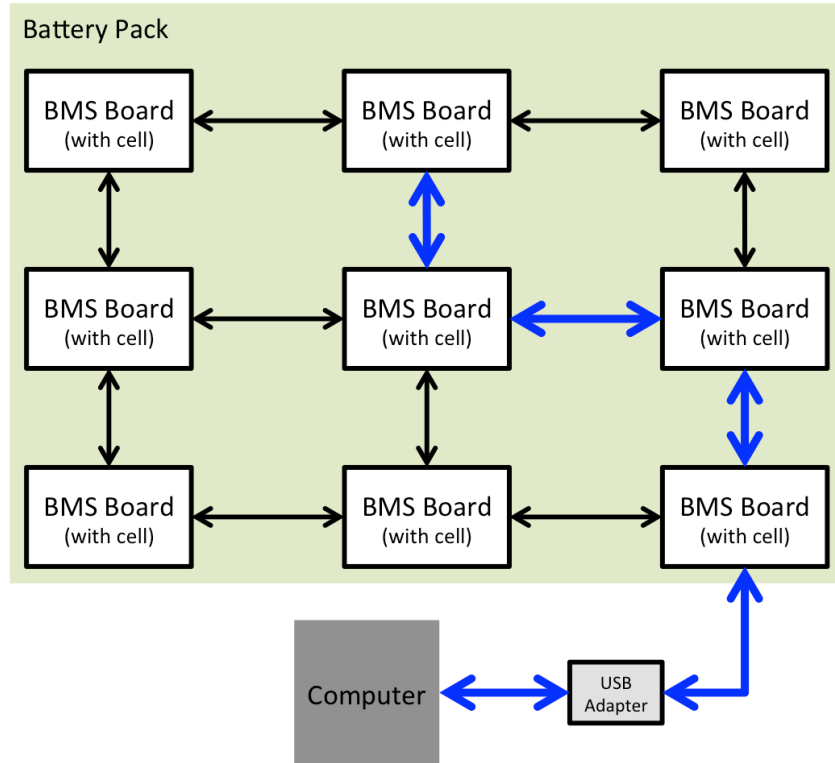


Figure 3.34 – Diagram of showing how the communication network can transfer data.

The internal communications also handles when it is appropriate to switch over to external communications. When the internal communications has no message started (ie. it did not receive a '{') and it receives a '%' it switches to external communication mode. In the event that a user accidentally pressed the '{' character, simply sending a '}' character will end the message and most likely receive a failed message (string of "{?}"). Then sending a '%' will switch to external communications. A list of finished internal communication commands can be found in Appendix F.

3.2.6.A External Communication (User interface)

The external communications code is used to make a terminal-like command-line interface. This code was originally meant only to configure the system, however grew in scope to incorporate abilities to test individual parts of the hardware. Instead of having to write code, compile, and install it on the device; connecting the board to the computer and opening a terminal program was all that was required to test sub-circuits and different sections of the code. A full list of commands is available in the Appendix F.

The user input interpreting was originally a massive set of nested **IF** statements. However, this initial design was quickly abandoned as the scope of the interface rapidly grew and needed to be more modular. To combat wasting an excessive amount of time, a tree-like structure was coded. Options that had similar sub-options were grouped together to save data space and to minimize the amount of copy pasting in the code. Figure 3.35, shows a basic tree structure a user would see. Figure 3.35, also shows how it is coded in the program to save space.

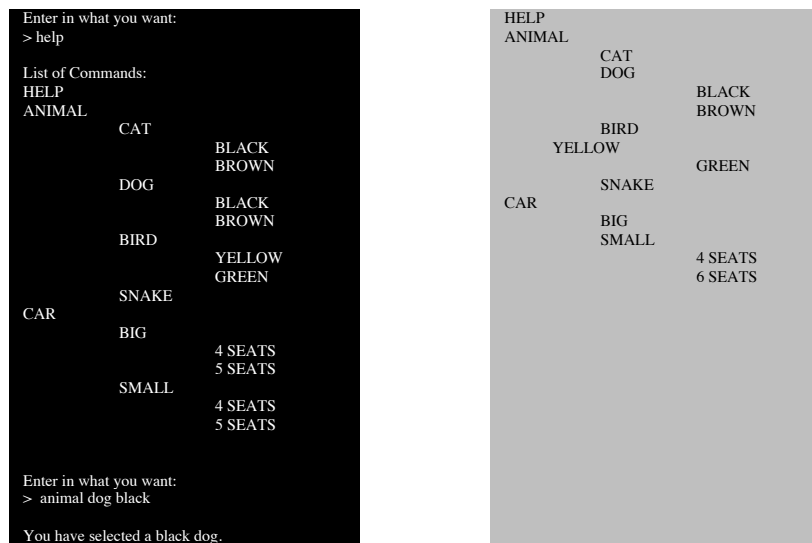


Figure 3.35 – Example showing how the user interface tree-structure is set up.

The figure on the left is the user interface in a console. The figure on the right is how the structure is set up in code to achieve the user interface on the left side.

Each term, for example “dog” is a type of data that stores several pieces of data. One piece is the level. For example “dog” would be a level 1 (“animal” would be zero and “black” would be 2). It also has a data pointer that points to a string of the characters. It has a unique value between 1 and 49. So “animal” can have up to 48 unique sub-keywords at level 1, as can “help”, and “car”. This part will be explained later. Finally, there is a variable that stores what kind of operation to perform on this keyword. There are two basic types: *command* and *next*. A *command* means that it is the last keyword in a string that is submitted to the MCU. So in the example in Figure 1, “black” would have the *command* operation. However “animal” and “dog” would have the *next* keyword. *Next* implies that there is at least one more keyword before there is a command operation. In practice, there are actually several combinations of these basic operations. Some keywords can be a *command* or possibly a *next*. In this case, the processor has to look to see if there is anything valid after the current keyword. Additionally sometimes there are variables being entered in by the user, especially during calibration. In this case, then it may be a *command variable* or a *next variable*. In these cases, a *command variable* means that if the parser sees a variable, it interprets it as the end of a complete command. Similarly, a *next variable* means that the parser has to look ahead. There are also cases of it being a *command*, *command variable*, *next*, or *next variable*. In any of these cases, there are *#defines* used to aid in reading the code. See Figure 3.36, which is a small section of *switchboard.c*, which outlines how to interact with the analog-to-digital converter, help, and emergency stop.

```

void sw_config_keywords(void)
{
    uint16_t i = 0;
    sw_keyword_set(i++, 0,SW_EMERGENCY, sw_str_stop, SW_OP_KEY_C_N);

    sw_keyword_set(i++, 0,SW_HELP, sw_str_help, SW_OP_KEY_C);

    //////////// ADC ////////////
    sw_keyword_set(i++, 0,SW_ADC, sw_str_adc, SW_OP_KEY_C_N);
    sw_keyword_set(i++, 1,SW_ADC_HELP, sw_str_help, SW_OP_KEY_C);
    sw_keyword_set(i++, 1,SW_ADC_ALL, sw_str_all, SW_OP_KEY_C_N);
    sw_keyword_set(i++, 2,SW_ADC_RAW, sw_str_raw, SW_OP_KEY_C);
    sw_keyword_set(i++, 1,SW_ADC_CALIB, sw_str_calibrate, SW_OP_KEY_N);
    sw_keyword_set(i++, 2,SW_ADC_CAL_TEST, sw_str_test, SW_OP_KEY_C);
    sw_keyword_set(i++, 2,SW_FACTORY, sw_str_factory, SW_OP_KEY_N);
    sw_keyword_set(i++, 3,SW_VAR, sw_str_var, SW_OP_VAR_C);
    sw_keyword_set(i++, 1,BMS_PIN_I_800A, sw_str_current800a, SW_OP_KEY_C_N);
    sw_keyword_set(i++, 1,BMS_PIN_C_800A, sw_str_coulomb800a, SW_OP_KEY_C_N);
    sw_keyword_set(i++, 1,BMS_PIN_V_BATT, sw_str_vbatt, SW_OP_KEY_C_N);
    sw_keyword_set(i++, 1,BMS_PIN_I_120A, sw_str_current120a, SW_OP_KEY_C_N);
    sw_keyword_set(i++, 1,BMS_PIN_C_120A, sw_str_coulomb120a, SW_OP_KEY_C_N);
    sw_keyword_set(i++, 1,BMS_PIN_I_DCDC, sw_str_dcdc, SW_OP_KEY_C_N);
    sw_keyword_set(i++, 1,BMS_PIN_V_TEMP, sw_str_temperature, SW_OP_KEY_C_N);
    sw_keyword_set(i++, 2,SW_ADC_RAW, sw_str_raw, SW_OP_KEY_C);
    sw_keyword_set(i++, 2,SW_ADC_SETTINGS, sw_str_settings, SW_OP_KEY_C_N);
    sw_keyword_set(i++, 3,SW_ADC_OFFSET, sw_str_offset, SW_OP_KEY_C_N);
    sw_keyword_set(i++, 3,SW_ADC_GAIN, sw_str_gain, SW_OP_KEY_C_N);
    sw_keyword_set(i++, 3,SW_ADC_CALIB, sw_str_calibrate, SW_OP_KEY_C_N);
    sw_keyword_set(i++, 4,SW_VAR, sw_str_var, SW_OP_VAR_C);

    //////////// PIN ////////////
    sw_keyword_set(i++, 0,SW_PIN, sw_str_pin, SW_OP_KEY_C_N);
}

```

Figure 3.36 – A section of the configuration code showing the tree-structure that was described in Figure 3.35.

In Figure 3.36, the third usage of “sw_keyword_set” will be the example. The first parameter just is an index at where in the array of keywords it is stored. The lower the index, the quicker the command will be processed. This is why emergency stop is the first one. The second parameter, which is the level, is 0. All subsequent values are higher than 0 until it gets to SW_PIN, which is a different command (SW_PIN sets inputs and outputs). This level helps the parser execute faster by skipping any keyword that does not meet the level it is looking for. Next is a #DEFINE value that is the unique value for the keyword. For this example, SW_ADC happens to have a unique value of 2.⁶ Next there is a pointer to a string of characters and the value is stored in

⁶ Values must only be unique for a given level within a keyword. For example: ADC level two can have unique numbers 2-49 used. ADC level 3 can use these same numbers. Similarly, keyword PIN can also have level two use the same unique numbers used in ADC because they are treated as independently. As a result each

“sw_str_adc”. Finally, the operation is “SW_OP_KEY_C_N”. This means that the keyword can be a *command* or *next*. If the user enters in ADC only, they will get the help menu. If they put a keyword after it, it will execute a different command.

The reason for the unique values for each word is that if the user enters in “adc cur120 settings calibrate 87.25” this will have a unique code of 4932311602. This command⁷ is composed of 49 for variable, 32 for calibrate, 31 for settings, 16 for cur120, and 2 for ADC. This unique code allows the sub functions to quickly route this code to the correct sub-function and execute the calibration.

By encoding it this way, which seems complicated, it reduced the code complexity in trying to parse user commands significantly. It should be noted that in that example, the unique code would actually 14579149, because the system uses base 50 instead of 100. Base 100 was used for the above example for clarity purposes. Base 50 is used so a higher number of keyword levels could fit in a 32 bit unsigned integer.

One final feature of the communication code is that it does not require to type out the entire command. In the previous example of “adc cur120 settings calibrate 87.25”, this is a very verbose command to type. However, it could also be triggered by typing “adc cur1 set cal 87.25”, or simply “a cur1 s c 87.25”. The string parser will match as many characters to the keyword until it finds a space entered by the user. This allows for quick entry, however the user must be aware of other similarly spelled commands. If the user typed “a c s c 87.25”, this would actually calibrate the 800A current measurement

keyword (ex: ADC, PIN, or whatever the level 0 name is) can each have 5,764,801 sub keywords. This assumes that the system does not run out of memory first.

⁷ “ad cur120 settings calibrate 87.25” will update the 120A current range calibration with a value of 87.25A. This assumes that 86.25A was actually being measured through the sense resistors.

instead of the 120A current. The parser uses the first match on a keyword that matches the user's string, which is why 'c' would trigger cur800A instead of cou800A (coulomb counting 800A range), cou120A (coulomb counting 120A range), or cur120A, which are index 0, 1, 2, and 3 respectively.

3.3 Mechanical

Most of the development for this project relies on electrical hardware and software design, however there was an important mechanical aspect as well. Early designs considered current coil sensors, magnetic sensors, IC current sensors, or sense resistors. Some goals considered were durable and compactness. Initially coil current sensors were considered since they are a very low loss solution.

Coil sensors that were capable of measuring up to 800A were very large, but could have fit on a circuit board. However, durability was a primary concern with this design. Additionally, having a method to run a heavy gauge wire through the sensor and connect it to the circuit posed more reliability problems. Finally, as mentioned in the electronics section, the accuracy was poor at low currents. Smaller coil sensors were considered by splitting the current through two paths. This solution was more less challenging to design than the larger sensors, however durability and accuracy were still potential problems.

Magnetic sensors offered a good solution initially because they were compact and easy to implement in hardware. Initial solutions included a copper trace close to the sensor or mounting the sensor on a bus bar. The both designs had the same problems that

could not be reliably resolved: magnetic noise would cause unpredictable errors, especially since the application for this design is unknown.

Another set of designs considered using IC current sensors. One limitation of these type of sensors was that the maximum, peak, current was about 200A. Additionally some of these sensors were large (XY size), unidirectional, and expensive. One possible solution utilized multiple sensors and another was to split the current. Multiple sensors were rejected because of the cost and the single sensor with splitting the current was rejected because of lack of reliability in the calibration.

The final solution used sense resistors. One problem with sense resistors is that the easier they are to measure (larger resistor value), the more losses that will be incurred. With potentially 1000A flowing through the resistor, using very low resistance resistors was required. Unfortunately, accurate low resistance ($<1\text{m}\Omega$) resistors are challenging to purchase in low volume and many are too large for the size constraints. Additionally most of these sense resistors are less than 5W, which significantly limits the maximum continuous current. With a measurement goal of 800A, this meant that a single sense resistor alone was insufficient. The ultimate solution used four sense resistors in parallel. While these sense resistors are the largest passives on the circuit board, they occupy an acceptable amount of XY space and have a very low Z height.

To measure the current through the cell required the circuit be broken to insert the current sensor. As a result, a third terminal (See Figure 3.37) was required so that a busbar or cable could be connected to it. Not surprisingly, this created several problems. First, the battery does not have a third terminal so the mounting location of the third terminal is only supported by the strength of the PCB. For the prototypes, a standard

1.5mm thick board with 1oz copper, on all layers, was used. This thickness was chosen to save money in a small run of boards for prototyping. In production a thicker board, 3-4mm, should be used to add more strength to the mounting location. Next, threads for screws were required to secure the connection to the third terminal. Using a 1.5mm thick PCB did not leave enough material to place sufficient threads in the holes. To solve this problem, a strip of aluminum was placed on the backside. This aluminum has threads on it so that screws can be securely attached to the circuit board. Since the backside was not a primary path for current, aircraft grade aluminum (alloy 7075) was used because of its high strength. Additionally it would be the less likely that the user could strip the threads accidentally as 7075 has the strength of mild steel while maintaining good corrosion resistance.

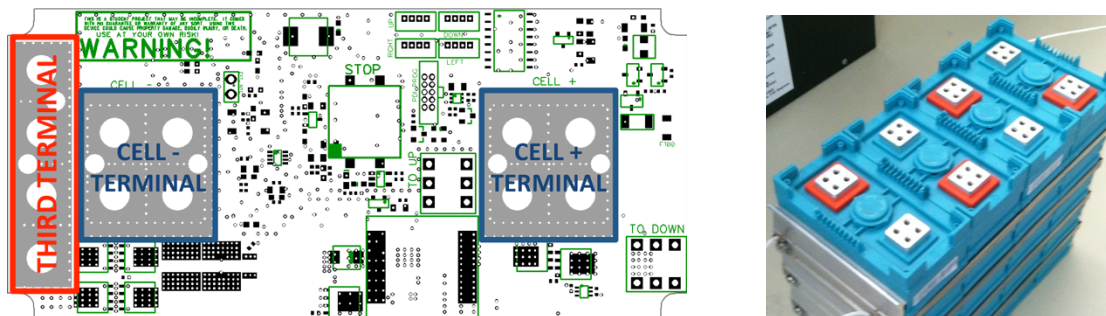


Figure 3.37 – Image showing where the cell terminal connects to the board and where the third terminal is to utilize the emergency disconnect switch.

The goal of this design was to allow for either busbars or direct wire connections to be used. Unfortunately, any location that has a circuit component, a busbar cannot be directly connected to a terminal because it would short components. Additionally, some of the components are tall (power inductor and DC/DC screw terminals), which added an additional challenge. The bottom side can only accommodate short components otherwise spacers would be required between the cell and the board.

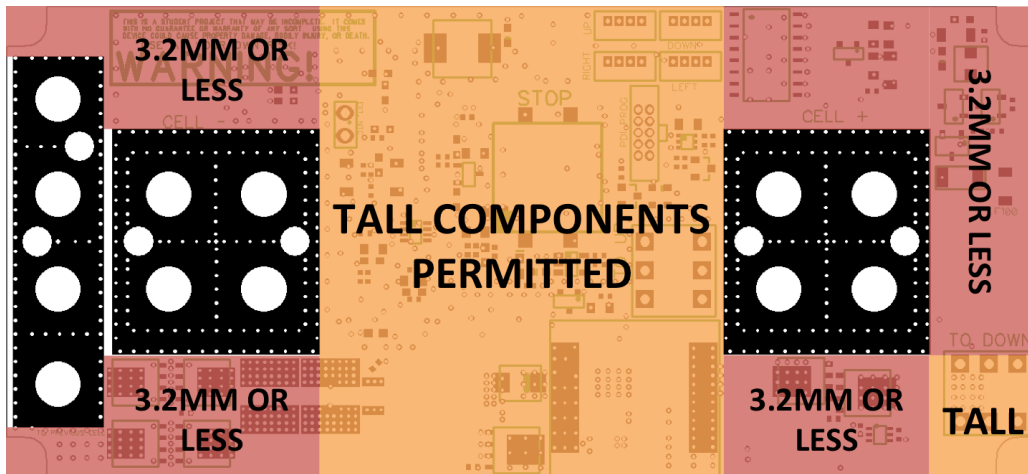


Figure 3.38 – Image showing the different zones on the board where certain height components were allowed.

The final solution was to restrict any component taller than 3.2mm (0.125in) from being placed on the bottom side or outside of the center section of the top. See Figure 3.38. There is an additional zone in the bottom right corner for one of the DC/DC screw terminals. Spacers were required since there are components that are possibly 3.2mm tall around the terminals. These spacers are 4.8mm thick (0.19in) and are made from 1100-H14: an alloy close to pure aluminum. This alloy has high electrical conductivity. It also has low strength, which is not a concern since the spacers are under compression. The added series resistance of the spacer will be negligible because the thickness is 4.8mm thick with a cross sectional area of 575mm².

Adding spacers adds another item that the user would have to manage and remember to use. To minimize the impact on the user, a spacer is placed on both sides of the PCB board and held together with screws. The spacer between the battery and the PCB is not required for component height, but it adds a place to screw the two spacers together with the PCB between them. Other options for spacer attachments were considered, but screws yielded the easiest and most reliable solution. By countersinking the holes on the top spacer, threading the bottom spacer holes and using small #4-32

screws, the spacers can be held together and leave a flush surface on top and bottom to allow for mounting of wires or busbars. See Figure 3.39. #4 screws are very small and making holes for them is exceptionally challenging. However, the benefits of using screws outweighed their challenge.

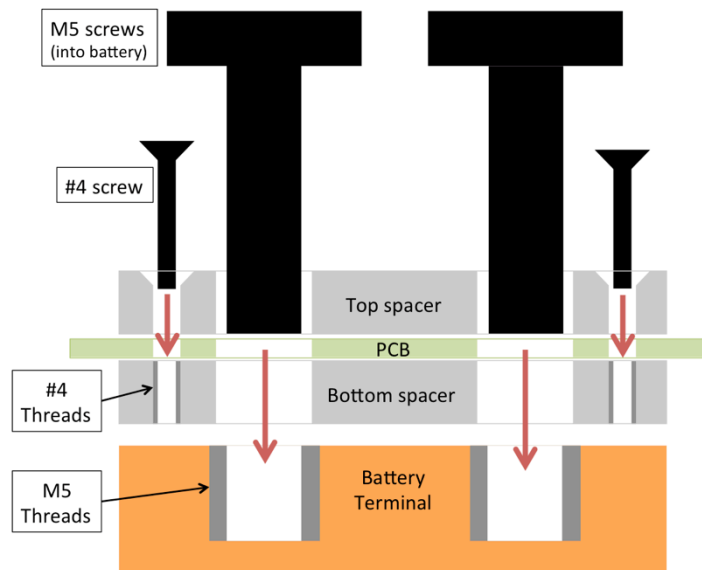


Figure 3.39 – Image showing a cross-section view of the assembly of spacers, PCB, and battery to reach the correct height.

A special spacer was also made for the third terminal as well to keep the busbars on the same plane. The top spacer is made from low resistance 1100 aluminum while the back size is made from stronger 7075 aluminum. These two are also screwed together with #4 screws.

Finally, custom busbars were designed. Most battery packs typically have their own busbar because terminal size and screw orientation change from manufacturer to manufacturer. The cell used in this design originally had busbars made of five to ten thin strips of aluminum stacked on each other. These no longer work on this design because the third terminal needs to be part of the circuit now. To resolve this issue, a L-shaped busbar was designed using 4.8mm thick 1100 aluminum. Heaver aluminum could be

used if lower DCR is required, however for testing it was not required. Large holes to allow the screw to go through it were added in this design to easily disconnect the board from the cell for testing. A more permanent solution would use slightly larger spacers to elevate the L-shaped bar above the screws with a thin Mylar pad to prevent shorts to the screw heads.

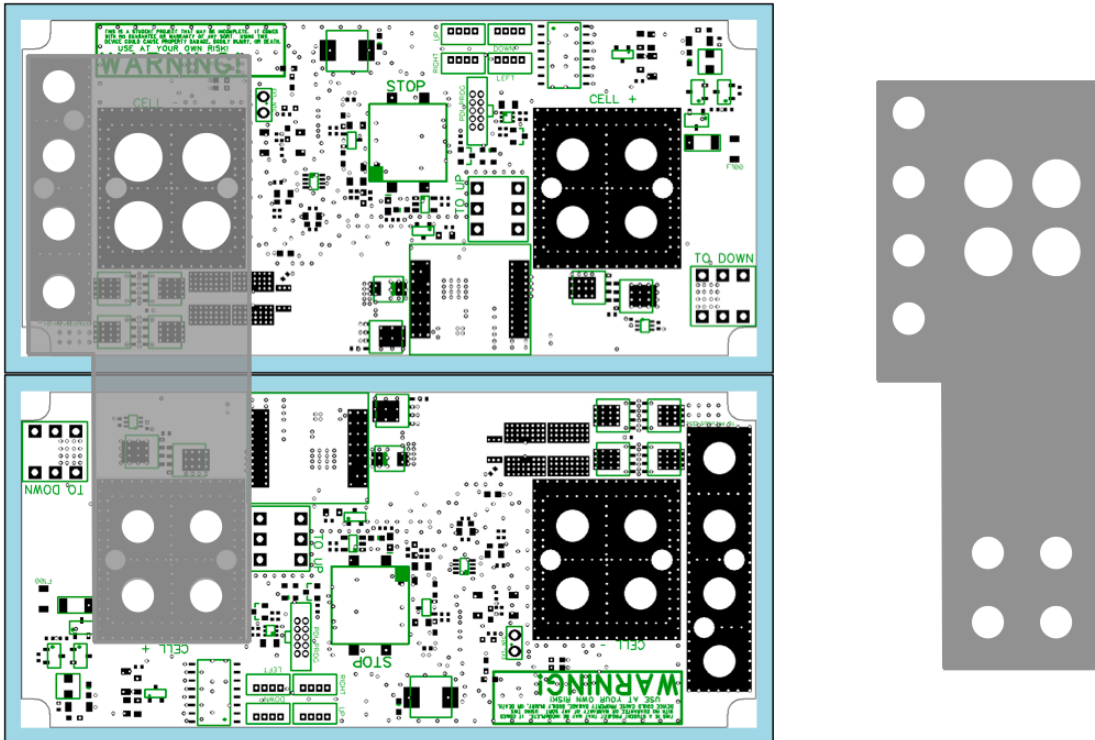


Figure 3.40 – Image showing how a busbar connects the third terminal of one cell and the positive terminal of the other cell.

Chapter 4 – Results and Verification

The results and verification section of the paper only covers the electrical hardware. Software results were covered in the design section because of the nature of the building/testing process. The mechanical results are not summarized because the proposed bus bar system was not fabricated before the time of writing this. Heavy gauge wire jumpers were used in lieu of bus bars.

4.1 Measurement Circuits

4.1.1 Battery Voltage

As noted in the design section, the battery cell voltage measurement circuit was a summing amplifier with one of the summed sources connected to 1.1V (1.1316V during testing). The goal of this design was to shift and scale the measurement voltage from 2.2-4.2V to a voltage range of 0-2.048V. Finally, a bypass capacitor C_{753} was added to reduce noise. The circuit was presented in the design section is presented again as Figure 4.1.

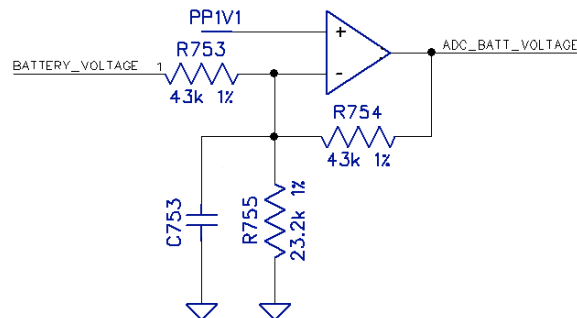


Figure 4.1 – Battery cell measurement circuit (same as Figure 3.4).

Initially C_{753} was populated with 100pF capacitor to introduce a low pass filter around 50kHz. This capacitor resulted in an oscillation at 121kHz on top of the desired

signal. This oscillation made valid measurements nearly impossible to capture. Removing the capacitor fixed the problem.

With a stable and reliable output from the circuit, the DC and AC responses of the circuit were measured. The design was to have an output equal to $4.24V - V_{batt}$. However measurement of the input and output relationship of the circuit revealed a relationship shown in Equation 4.1.

$$V_{out} = 4.3745V - (0.9993)V_{batt} \quad \text{Equation 4.1 - Output relationship from the battery voltage circuit.}$$

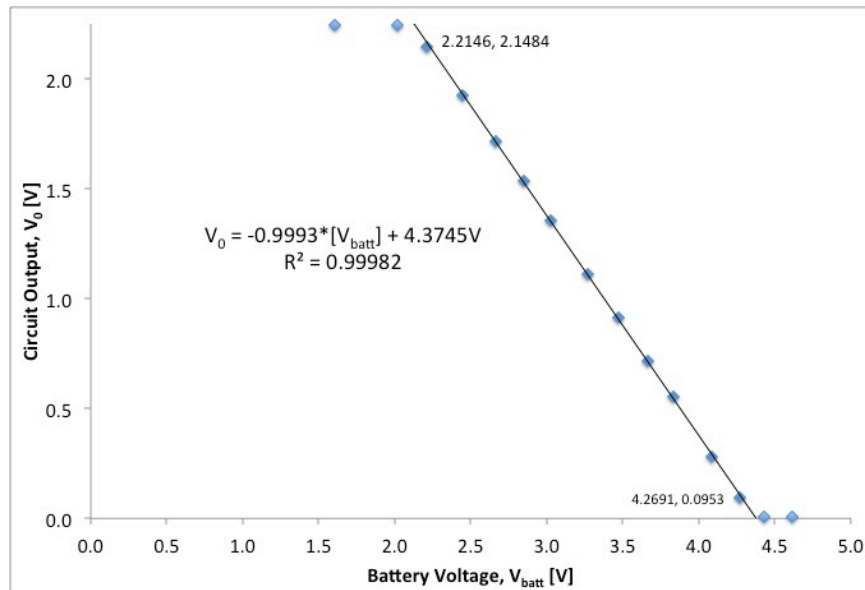


Figure 4.2 – Plot of output from cell voltage measurement circuit as cell voltage changes.

The gain was nearly the predicted value, however the offset was slightly different. The gain applied to the -1.1V input was ideally -3.85. However, the -1.1V supply was measured to be -1.1316V, which results in an offset of 4.36V. This is closer to the measured 4.37V and the tolerance of the resistors could be the source of the remainder of the error. An equation was determined using Figure 4.2, which shows the DC response from the circuit. Several data points are shown in the saturation region to demonstrate that the circuit is cable of measuring the target range of 2.4 to 4.2V.

Next the frequency response was measured and plotted. The AC response showed that there was a roll off in frequency as expected. However, the transfer function appears to be more complicated than expected. Figure 4.3 shows the frequency response. While there is a sharp roll off around 250kHz, there is a droop in gain at 8kHz. This earlier roll off frequency is undesirable because it limits the ability to capture transients. At this time, the source of the earlier roll off is unknown, however it most likely has to do with the internals of the op-amp.

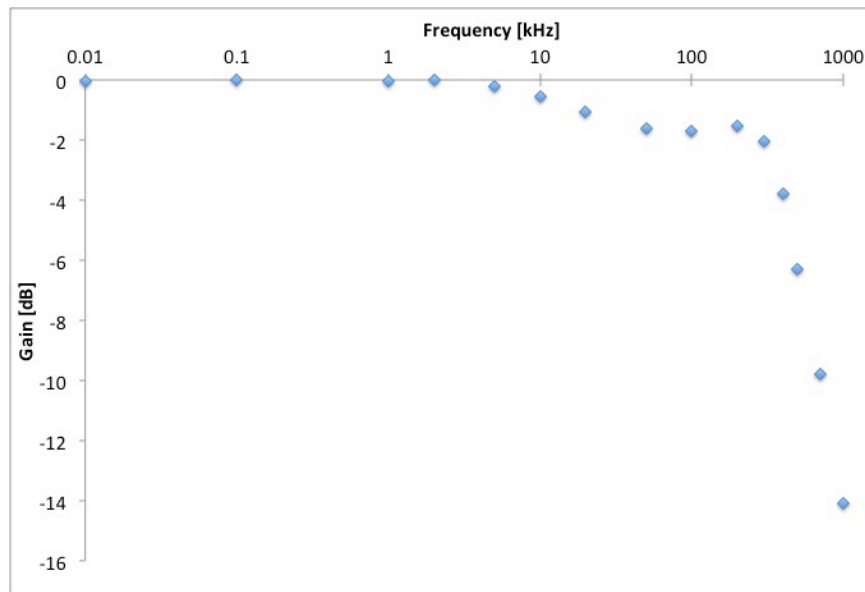


Figure 4.3 – Plot of the frequency response of cell voltage measurement circuit.

4.1.2 Current Measurement

The current measurement capability was one of the most crucial parts of the design. The instantaneous current is important for detecting excessive current conditions, as well counting coulombs. As noted in the design section, each stage of the amplifier circuit introduces gain and offset errors. There are four major areas that introduce error:

sense resistor, parallel voltage dividers, first gain stage ($\pm 800A$ range), and the second gain stage ($\pm 120A$ range).

Each of the sense resistors was $250\mu\Omega$ (1% tolerance). However since each resistor is physically large (nearly 17 times larger than an 0805 component), the actual resistance depends on where the voltage measurement is taken on the resistor. Figure 4.4 shows the resistor and Figure 4.5 shows the placement of the voltage measurement. Due to the physical location of the measurement point, the resistance that the amplifier circuit sees was an average resistor value of $57\mu\Omega$ (or $228\mu\Omega$ each). The physical system still sees resistance and losses from a $62.5\mu\Omega$ resistor. Table 4.1 shows the measured data points to calculate the effective sense resistor. These measurements were collected using an Agilent 6572A 20V 100A supply.



Figure 4.4 – $250\mu\Omega$ sense resistor (size 2725) on a penny.

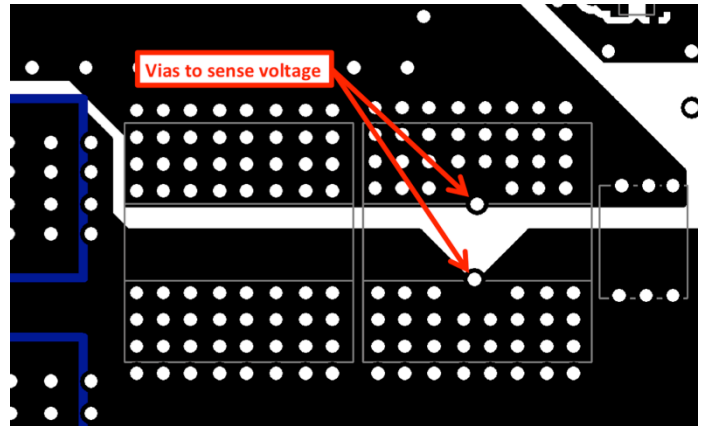


Figure 4.5 – PCB layout showing assembly outline of sense resistors and sensing vias.

Table 4.1 – Sense resistor measurements

Current [A]	Voltage [mV]	Resistance [$\mu\Omega$]
15.03	0.860	57.22
50.0	2.863	57.26
75.0	4.292	57.23
100.0	5.719	57.19
Average		57.225
Std. Dev.		0.029

The placement of the sensing vias was selected based on application notes for the resistor [24]. Placing the measurement points (vias) further away from each other would have yielded a larger effective resistance. The lower resistance does not add a direct error, however it reduces the amplifier output by almost 10%.

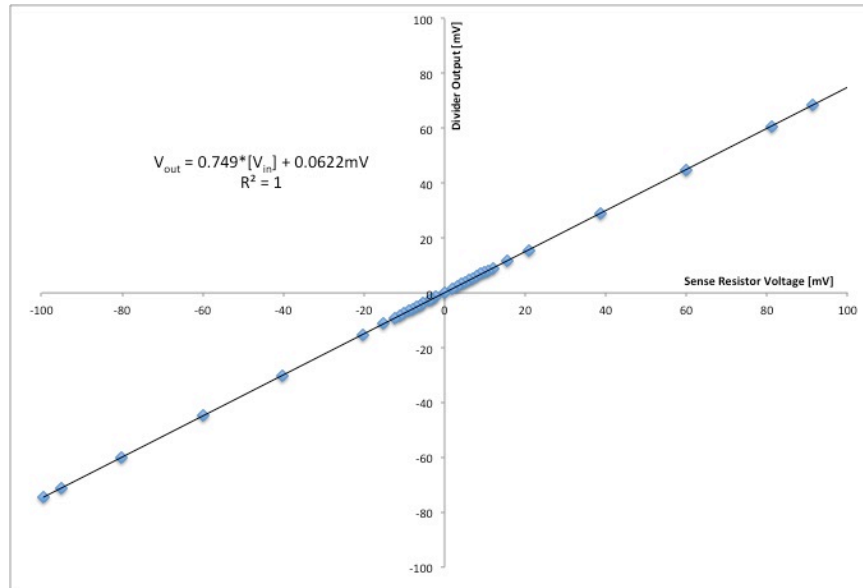


Figure 4.6 – Output of voltage divider for current sense resistor.

As expected, the difference between the two voltage dividers introduced an offset. In addition, there was an error in the gain. Figure 4.6 shows a plot of the difference between the two voltage dividers versus the voltage across the sense resistor. See Table 5.3 for the raw data. A linear trend line was added to the plot. The trend line has an excellent correlation to the data and shows that the gain of the voltage divider was 0.749 (0.750 was ideal). Also there was an offset of 62.2 μ V. While an ideal case would be

0 μ V, the measured offset was excellent considering the worst case could be as high as 1620 μ V for the divider. This data was collected from the only fully functional revision C prototype.

Next the instrumentation amplifier circuit introduces offset and gain errors while generating the ± 800 A range output. This circuit has three discrete op-amps; each with its own offset error resulting in a cumulative offset error. Figure 4.7 shows a plot of the output voltage versus sense resistor voltage. A gain of $-11.935^{\text{V}}/\text{V}$ and offset of 1.250V was calculated which includes the combined gain and offsets from the op-amps and voltage divider.

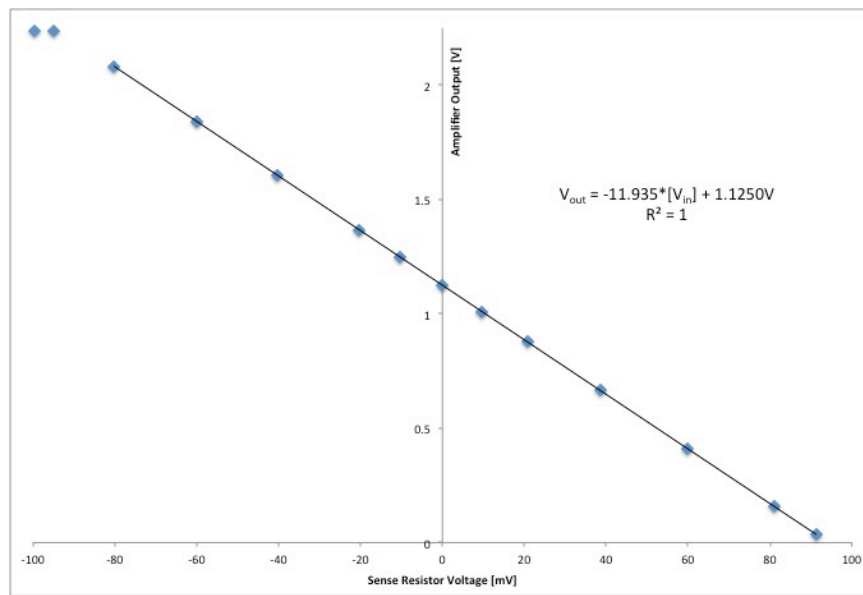


Figure 4.7 – Plot of 800A range output DC response.

The final gain stage generates the ± 120 A range output. This output adds one op-amp, which results in a combined gain of $-94.672^{\text{V}}/\text{V}$ and offset of 1.0695V. Figure 4.8 shows a plot of this relationship and Table 4.2 summarizes the gains and offsets. In this circuit all outputs were center around PP1V1. Ideally both the 800A and 120A ranges should had an offset of 1.1316V (measured value of PP1V1). However, this was not the

case and there was an offset of 6.6mV and 52.1mV (relative to the measured PP1V1 value) for $\pm 800A$ and $\pm 120A$ range respectively. To mitigate these offsets, the board uses the auto-calibration circuit.

When the auto-calibration circuit (this is different from the software calibration done at the “factory”) was activated, it shorted the input to the first stage of amplifiers. Shorting the inputs caused most of the offsets from the $\pm 800A$ and $\pm 120A$ ranges to be measurable. While each board will have unique values, this circuit’s measured offset values were 4.7mV and 35.8mV for the $\pm 800A$ and $\pm 120A$ ranges respectively and this data is summarized in Table 4.2.

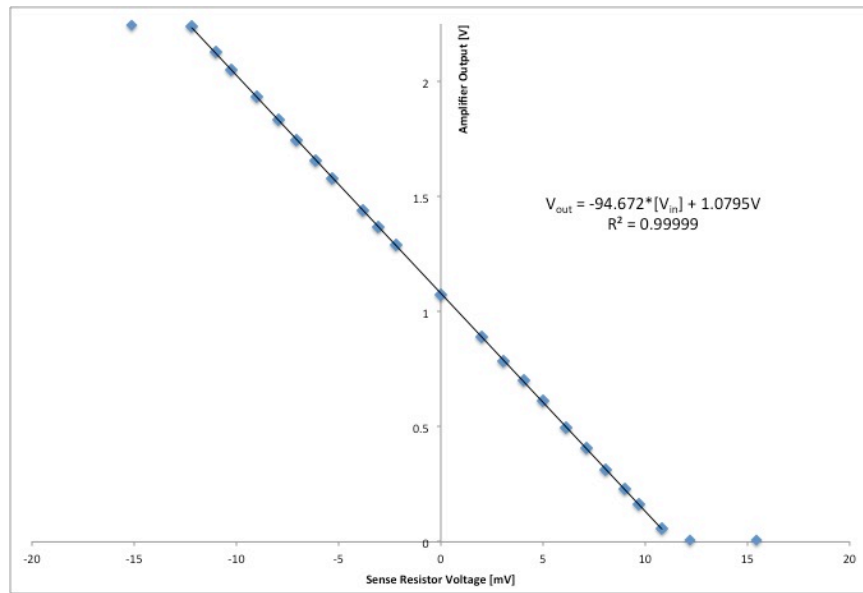


Figure 4.8 – Plot of 120A range output DC response.

PP1V1 voltage reference was measured to be 1.1316V.

Table 4.2 – Summary of current sense amplifier offsets and gains.

Offsets are in millivolts. PP1V1 Reference Voltage: 1.1316V

Stage	Measured (Plot)		Individual Stages		Auto-Calibration Offset		Net Offset
	Offset	Gain	Offset	Gain	Measured	Actual	
Divider	0.0622	0.749	0.0622	0.749	0	0	0.0622
800A	1125.0	11.935	6.6	15.935	1126.9	4.7	1.9
120A	1079.5	94.672	52.1	7.932	1095.8	35.8	16.2

Table 4.2 shows a summary of the measured offsets and gains from each stage that were calculated using linear regression from the plots in Figure 4.6, Figure 4.7, and Figure 4.8. The individual stage offsets were calculated by taking the difference from the ideal data and the measured data. The gains were measured by dividing out previous stage's gains. The auto-calibration offset's values were what the ADC measured and the actual offset is the difference from the measured and the ideal case. Finally, the net offset is calculated by subtracting the auto-calibration's actual offset from the individual stage's offset. By using the auto-calibration circuit the effective offset of the circuit was 1.9mV for $\pm 800\text{A}$ range and 16.2mV for $\pm 120\text{A}$ range. This set of data was from one board, however each board will be unique. The auto-calibration process is performed for every measurement and the remaining offsets are removed by the software calibration.

Next the frequency response of the amplifier circuit was analyzed. Initially the circuit included R710, R711, C701, and C702, which were optional low-pass filters for $\pm 800\text{A}$ and $\pm 120\text{A}$ current ranges. These filters were meant to reduce noise because the bandwidth of the amplifiers was expected to be lower. The amplifiers had better than expected bandwidth and the $\pm 120\text{A}$ current range had a bandwidth slightly higher than 200kHz, The $\pm 800\text{A}$ range had a bandwidth of nearly 250kHz. See Figure 4.9.

Finally, any noise has a detrimental impact. Testing for noise was exceptionally limited as the testing capabilities available at this time were limited. It was fortunate that access was briefly granted to higher end equipment to do some measurements on the analog supply. Two wires were attached to either side of the LDO's output capacitor from PP2V2_VA rail. These wires were less than $\frac{1}{2}$ inch long and twisted to reduce measurement error. At the end of the wire was a two-pin 0.1" header to plug into a

TDP1500 active differential probe. This probe was connected to a Tektronix MSO3034 oscilloscope. Figure 4.10, shows a screen capture of the supply output.

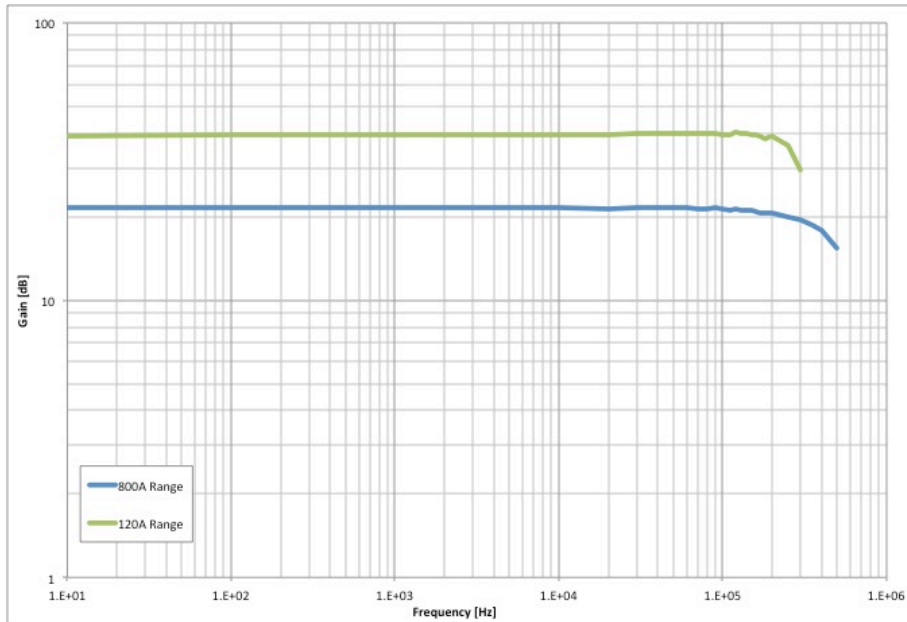


Figure 4.9 – Frequency response of the current sense amplifier for both 800A and 120A range.

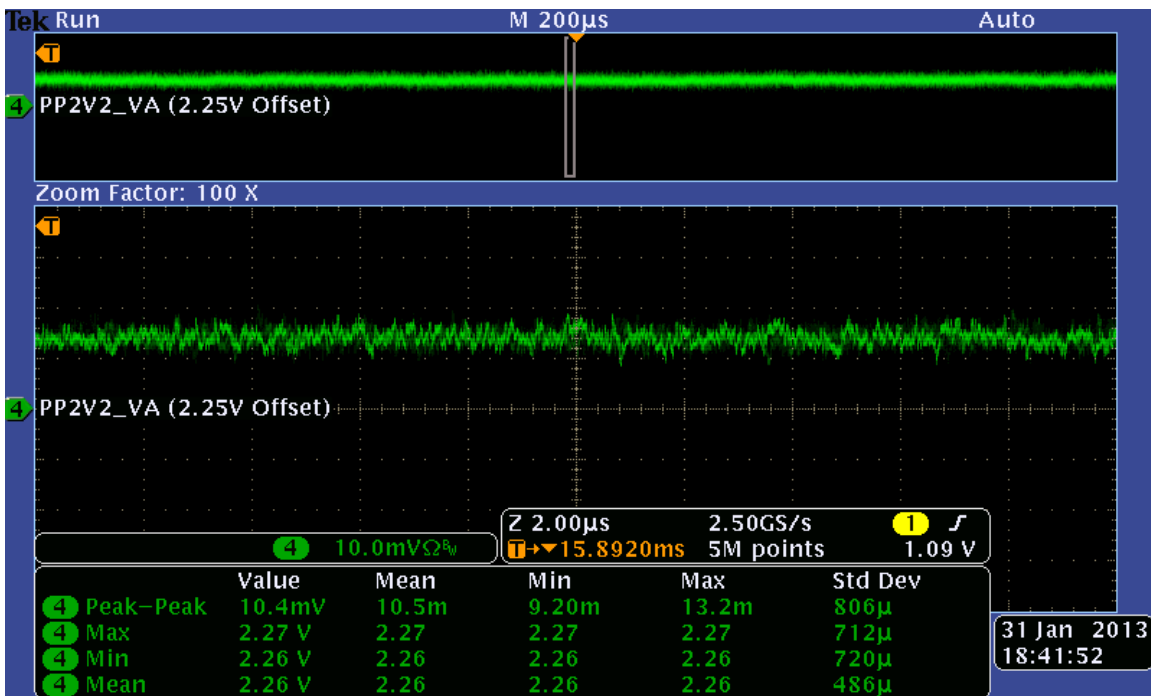


Figure 4.10 – Screen capture of ripple on PP2V2_VA supply output.

The ripple on PP2V2_VA was measured to be as large as 13.2mV. This ripple was significantly larger than expected. Each of the op-amps has a reasonably high PSRR but the noise was evident on the output. See Figure 4.11. The peak-to-peak value of this AC noise was hard to get an exact value. By making previous waveforms persist, a trend was seen for the peak-to-peak noise. The output is approximately 24mV_{pp} on the $\pm 120\text{A}$ range. This resulted in an estimated error of $\pm 2.18\text{A}$. A similar measurement was done on the $\pm 800\text{A}$ range see Figure 4.12. The peak-to-peak voltage is roughly 4.5mV , which results in an estimated error of $\pm 3.28\text{A}$.

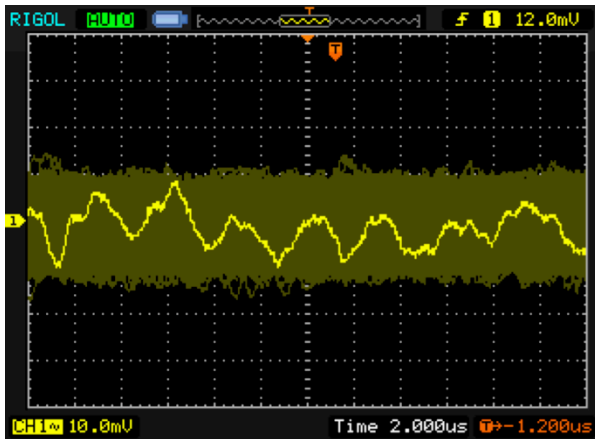


Figure 4.11 – Screen capture of noise on the output of 120A range from 0A input current. AC coupling is on.

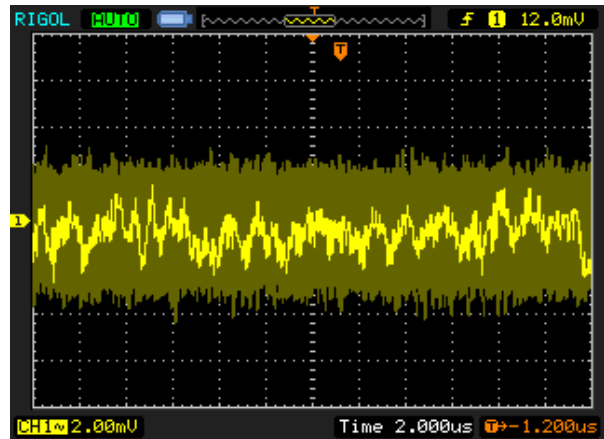


Figure 4.12 – Screen capture of noise on the output of 800A range from 0A input current. AC coupling is on.

Both Figure 4.11 and Figure 4.12 were measured at the output of the respective op-amps. This noise was a larger problem than expected because the reduced sensitive in the measurements due to poor placement of the vias on the sense resistors. It should be pointed out that this is less than 2% error on the $\pm 120\text{A}$ range and 0.4% for the $\pm 800\text{A}$ range.

The noise on the output ultimately impacted the ADC values as the signals bounce. Also after issues were starting to emerge, research into the ADC found that there has been many complaints by other users^[25] of the in accuracies of the ADC. Atmel's

recommends several fixes to improve measurements but in many cases, they are impractical in a real system [26].

Table 5.4 lists samples taken at 20A intervals between -100 and 100A (using the 120A range) and the difference from the expected value and the actual value was plotted. See Figure 4.13. The groupings show there was an underlying 3rd order trend. This could be accounted for in a more complicated ADC calibration, but the large distribution of values was a more significant problem. The largest measured error was 1.76A. To make the problem even worse, each single measurement is the average of 40 discrete samples. One partial explanation for the large distribution is that the analog rail supplying the MCU is a copy of the circuit supply power to the analog section which means a significant ripple is present on the MCU's analog supply. Interestingly enough, the data measured, during testing, seemed to be less during testing on revision B than on Rev C. A different LDO was used in revision B, but it was replaced on revision C because it was exceptionally hard to solder by hand. Out of five tries, only one was successfully soldered. The other four backup ICs were destroyed during attempts.

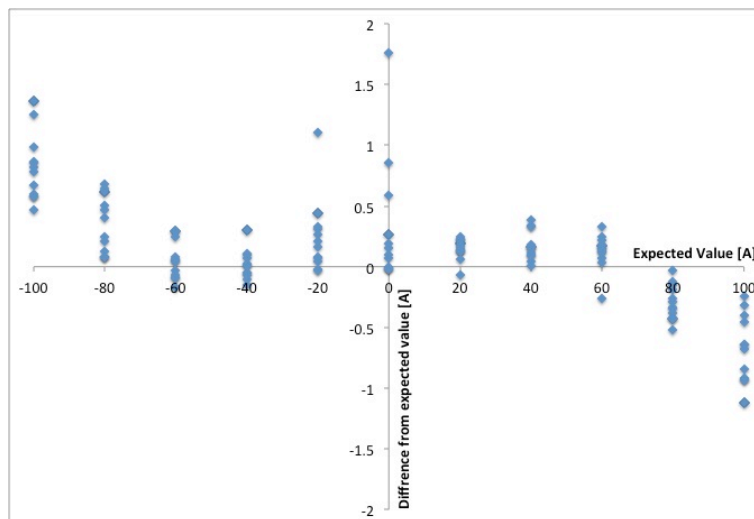


Figure 4.13 – Plot of difference from measured value and expected value for the calibrated $\pm 120\text{A}$ current range.

Despite poor individual samples, the software calibration appears to be generating a reasonably accurate linear regression. Reading the measured values from the microcontroller, the gain for the ADC measurement is $0.17589126 \text{ A}/_{\text{ADC}}$ and the offset was 4.22007 A . Using the random samples from Table 5.4, a gain of $0.17589128 \text{ A}/_{\text{ADC}}$ and offset of 4.22007 A was determined using Excel. Both Excel and software determined an R^2 value for their respective data sets of 0.99999 . See Figure 4.14 for the Excel generated version.

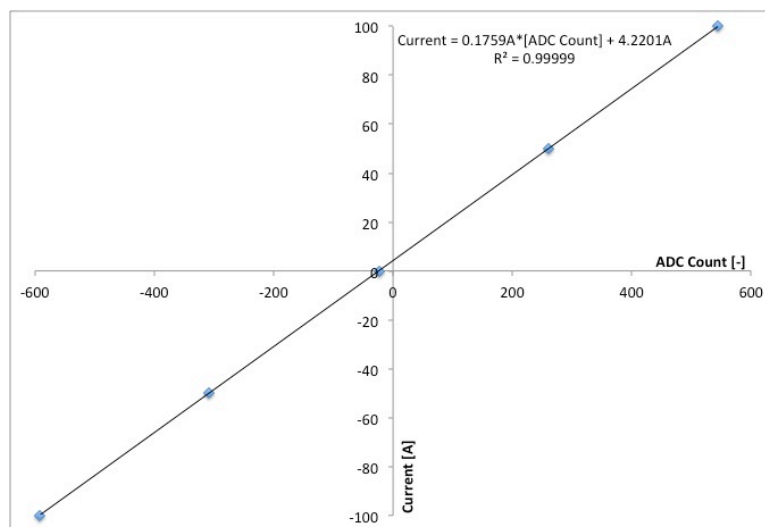


Figure 4.14 – Plot of randomly sampled data's linear regression for comparison with BMS's calculated regression.

4.1.3 Coulomb Counting

The coulomb counting circuit was not successfully verified. This circuit is the only one that could not be checked. While testing the circuit, input waveforms were not generating expected output waveforms. Even though the feedback capacitors are exceptionally large (by design), both high and low frequencies would not pass through.

Both theory and simulations show that these frequencies should be passed through. While this test showed the circuit did not work, other tests showed expected but inconclusive results.

Since all analog integrators will slowly reach saturation due to input offsets of the op amp, they need to be reset regularly. While monitoring the output with no input the output saturates very slowly as expected. Using the reset circuit, the output returns to a neutral state. By introducing a constant DC bias on the input, the direction of saturation (positive or negative rail) could be controlled. This result is expected from an analog integrator.

Further testing should be conducted to see if the exceptionally large capacitors were causing issues. These capacitor sizes were selected to allow for reasonable periods of sleep for the microcontroller. While this circuit is an unknown, it does not impact the safety of device or the device's ability to protect the user or battery. A quick solution would be to use digital integration, but this will increase the circuit's power consumption.

4.1.4 Current pulse

The current pulse circuit is used to measure the internal resistance of the cell. As noted in the design section, to measure the resistance two terminal voltages must be measured at two different currents. To ensure that the voltage change is significant enough to detect, a large change in current was required. This measurement requires that the pulse timeout (to prevent destruction of the circuit board), the current sensing circuit work, and cell voltage circuit all work.

The pulse timeout circuit limits the pulse width that the power MOSFET receives with a period of 4.5 seconds. The active pulse width that the MOSFET gate sees is only 55.8ms. See Figure 4.15 for results. When the MOSFET is enabled, the 100mΩ (3W) resistor is shorted across the terminal. Assuming a worst case of 4.2V cell voltage, the resistor should only see an average dissipation of 2.2W. This circuit is only for safety purposes and should not be relied upon.

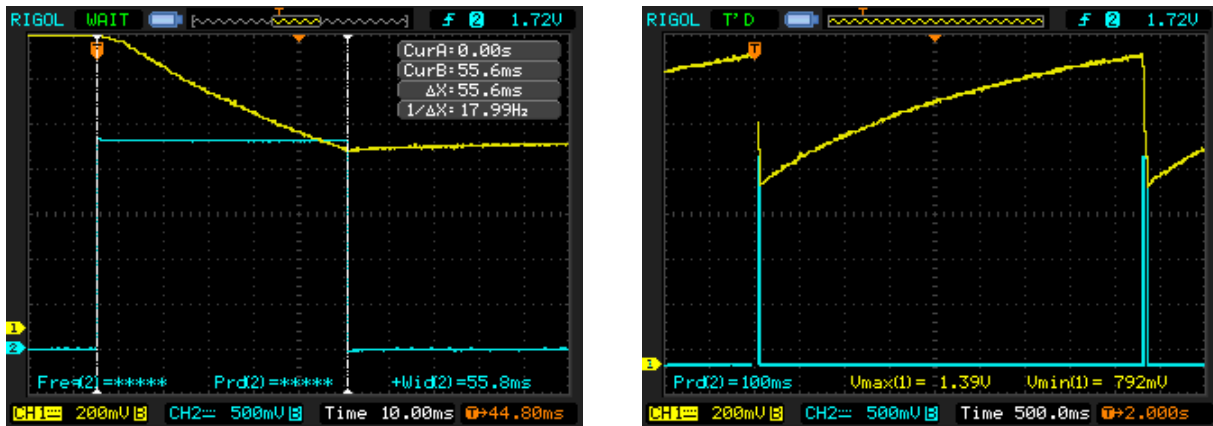


Figure 4.15 – Screen captures of MOSFET gate pulse and full period of timeout circuit.

Channel 1 (Yellow) is the timeout capacitor voltage and channel 2 (Blue) is the output logic to MOSFET gate.

While the circuit to enable the MOSFET gate works as designed, it relies on both the current and cell voltage measurement circuits. As noted in section 4.2 the current measurement circuit is capable of measuring up to 200kHz. While noise may be an issue, sufficient data processing could make these measurements useable. However, the low bandwidth of the cell voltage measurement circuit degrades the usefulness of the circuit. The low bandwidth limits the speed and number of measurements that can be used within a pulse. Sampling before enabling and sampling after the voltage has stabilized will permit the estimation of the internal resistance. To ensure the voltage is stable, the current should be sampled several extra times to ensure it is reasonably constant. These

systems have been tested individually, but the software to combine them all was not finished.

4.1.5 Temperature sensor

The BMS design includes three temperatures sensors. There are two negative temperature coefficient (NTC) resistors near potentially high temperature components and one circuit for use of an external NTC probe. All three circuits use a voltage divider circuit with a 100k Ω pull up resistor. Only the external probe utilizes a voltage follower to buffer the output circuit incase the user does not use a 100k Ω NTC resistor as expected. The buffer was added to prevent loading on the ADC input.

Since all three circuits utilize the same voltage divider, only one circuit was tested. To make the test simple, various fixed value resistors were tested in place of the NTC. This was done to have more reliable measurements as the resistance of the NTC varies quickly as its temperature changes. Additionally, plotting data with temperature would only apply to one specific NTC. Table 4.3 lists all of the measured resistances and their corresponding output. Figure 4.16 shows a plot of the data and includes a line for the ideal case. This was measured using the external temperature circuit that includes a voltage follower.

Table 4.3 – NTC circuit output based on measured NTC resistance (including voltage follower).

Op-amp Output	
$R_{NTC} [\Omega]$	$V_{out} [V]$
9.9E+6	2.2436
3.5E+6	2.2029
996.2E+3	2.0597
328.0E+3	1.7378
219.8E+3	1.5577
100.0E+3	1.1323
55.0E+3	0.8051
32.6E+3	0.5573
14.7E+3	0.2915
6.7E+3	0.1438

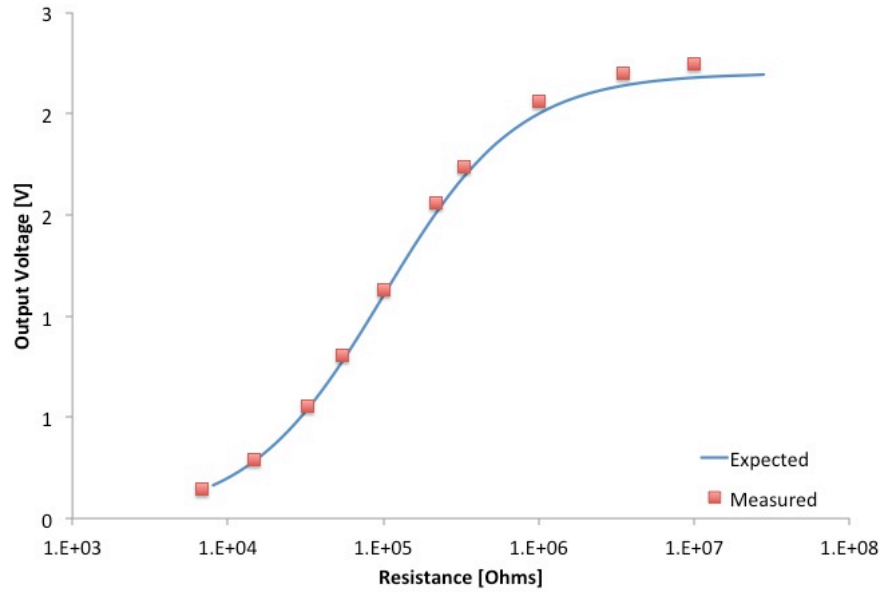


Figure 4.16 – Plot of output voltage from NTC circuit versus NTC resistance.

The output from the circuit closely follows the expected (ideal) line. There is nearly no deviation at low resistances with significantly more deviation as the resistance increases. While this plot is useful for verify the output, it does not give an intuitive feel for how the temperature affects the output voltage. Figure 4.17 shows a plot of output voltage versus temperature. The plot was generated by using the data measured in Table 4.3 and estimates the temperature of the NTC that would create this resistance. As expected the data between 25C and 85C is reasonably linear. By using a linear regression, a basic approximation can be determined. However, all of the data can be fit with an R^2 value of 0.998 by using a third order polynomial regression.

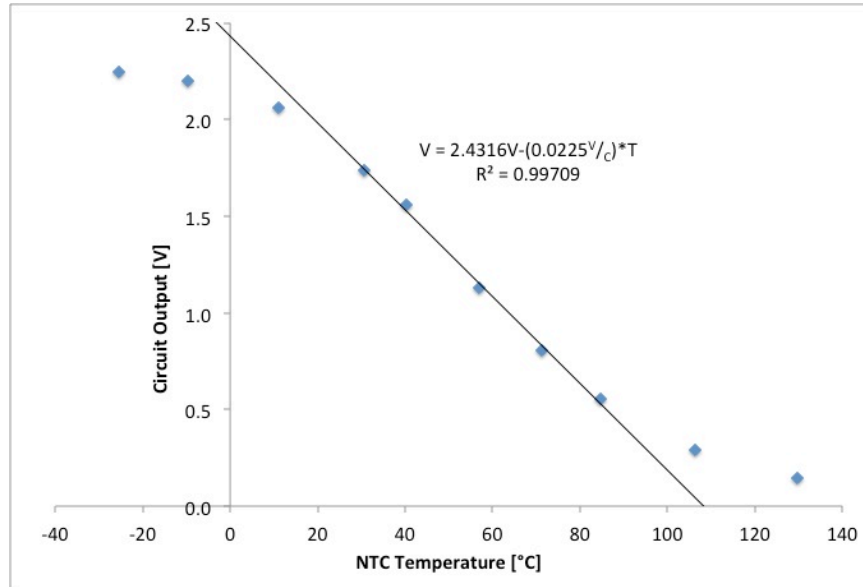


Figure 4.17 – Plot of output voltage from NTC circuit versus temperature.

Resistance values were calculated from data sheet based off of measured data shown in Figure 4.16. Linear fit uses data from 30C to 85C. Using a third order fit results in an R² value of 0.998 and fits all of the data, instead of the limited linear range.

4.2 Active balancing DC/DC converter

The DC/DC converter had a peak efficiency of 85.3%. While this was at a very low transfer rate, less than an amp from one cell to another, the converter maintained a reasonably efficiency throughout the entire working range of the converter. One failure in the design was to consider how the device was to be tested. Previous revisions were easier to test because the inductor current was more accessible from the topside. However, in revision C, the routing was the utmost importance and the previously accessible test point (the fuse) was placed on the bottom side. This resulted in requiring that the board not be directly attached to the cell as designed. Doing so, added unnecessary inductance and resistance. Figure 4.18 shows a picture of the set up. The

black electrical tape is covering probe wires to the gates of the MOSFETs to monitor the switching signals. Behind the tape was white 12-gauge wire, which created a current loop (using the fuse as part of the loop) to probe. Black 10-gauge wires were used to make the connections to the cell. To the left of the image shows a second PCB mounted directly to the cell as the design intended.

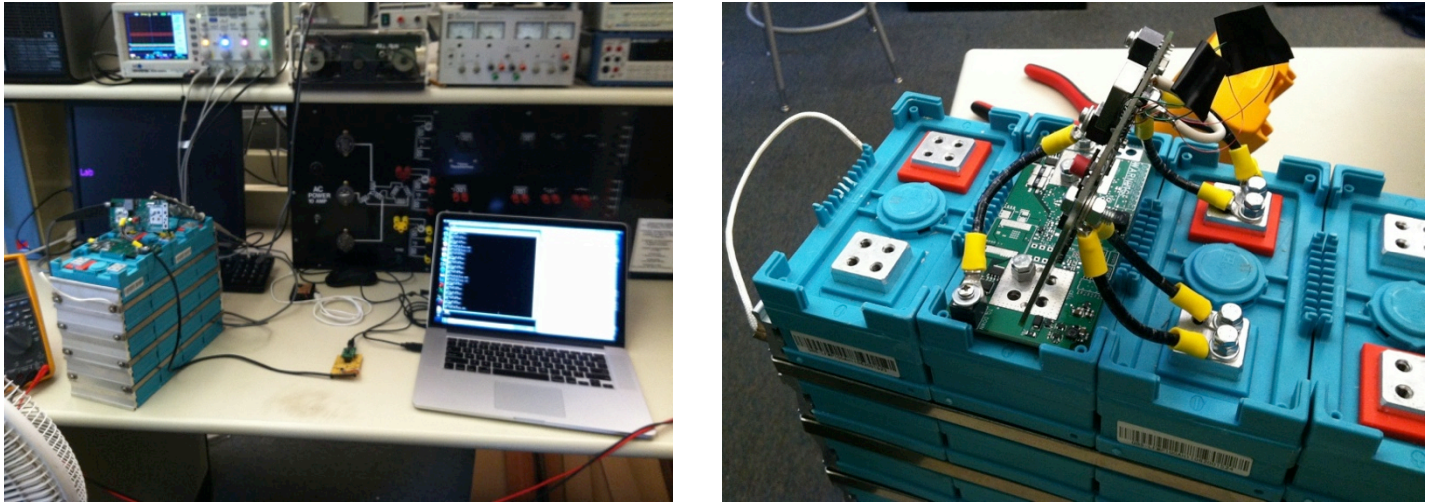


Figure 4.18 – Test setup to measure DC/DC converter efficiency.

Figure 4.19 shows a plot of efficiency versus duty cycle. The peak efficiency, as noted, was near to the neutral allowing an average transfer rate of 2.28A. In contrast, minimum efficiency was measured to be 58.1%. At 58.1%, there was 21.3A current in the inductor, but only an average of 7.82A was entering into the receiving cell. The cell, that the charge was transferred from, contributed an average of 13.49A. The efficiencies shown in Figure 4.19 ignore the cost of driving the gates. At 100kHz switching frequency, the system draws approximately 50mA from the cell at 3.3V. If this loss is included, the efficiencies drop significantly near the neutral point. It decreases the peak efficiency to 80.5% at 2.28A. The plot in Figure 4.20 shows both the efficiency of the converter only and the converter with gate driving losses.

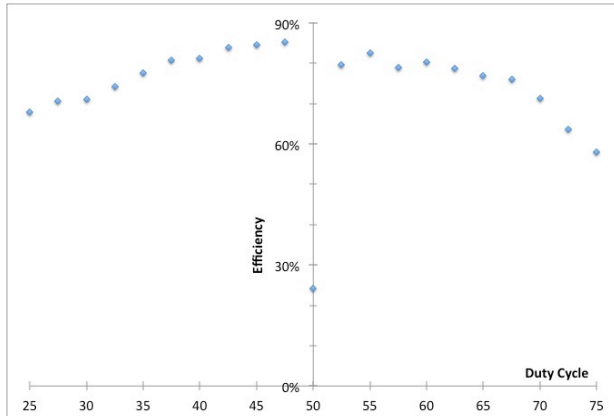


Figure 4.19 – Plot of balancing DC/DC converter efficiency versus set duty cycle.

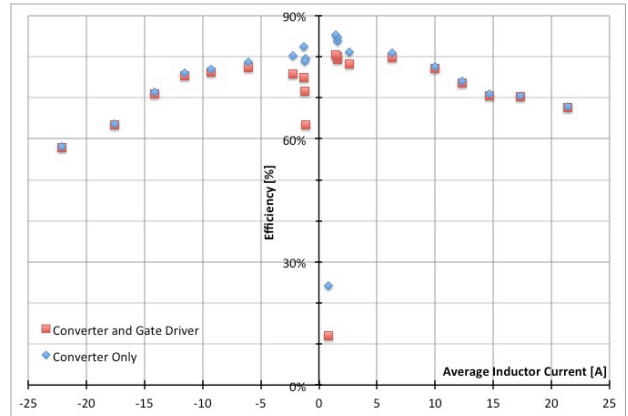


Figure 4.20 – Plot of balancing DC/DC converter efficiency versus average inductor current.

The goal was originally to have a high current converter that could transfer 30A from cell-to-cell. 25A was chosen instead because of availability of components. Depending on how the transfer rate is being defined, the goal may have been met: 25A can flow through the inductor. However at 100% efficiency, with 25A in the inductor, only 12.5A will enter the receiving cell. As a result, to achieve a 25A transfer rate, an inductor of 50A (assuming 100% efficiency) is required; or in a more practical case of 50% efficiency, an inductor of 75A is required.

The lowest measured efficiency was actually 24.1%. This data point was near the neutral point (zero net charge transfer) and this is a case that would never be used. This lower efficiency at the neutral point was expected from the simulation results. The measurements shown in Figure 4.19 and Figure 4.20 are when the cells are at an equal voltage of 3.3V. Under normal operation, the converter would not operate because the cells were already balanced. The selected duty cycle ranges were limited by the inductor's 25A maximum current. Table 5.9 summarizes the collected data points in the appendix.

While Figure 4.19 demonstrates how changing the duty cycle affects efficiency, Figure 4.20 is far more useful as it shows the efficiency as a function of inductor current. Near the neutral point, there is a large clump of data points. This occurs as the converter goes through the five various modes of CCM and DCM. During these transitions, the current does not vary much as the duty cycle changes. Figure 4.21 shows a plot of current contributions from each cell. As shown previously, towards the middle there is a long transition of low charge transfer rates. Figure 4.22 shows the same data summed together and the absolute value taken.

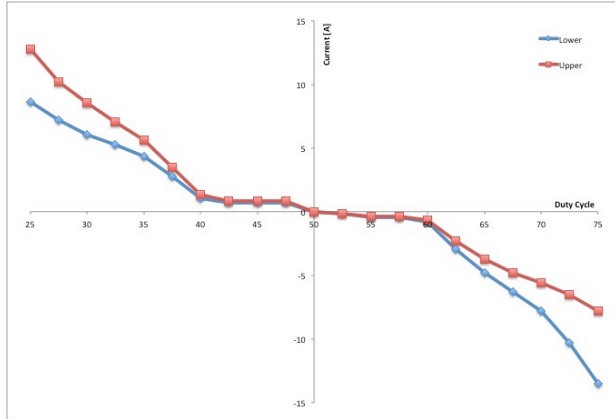


Figure 4.21 – Plot of balancing DC/DC converter current contributions from each cell.

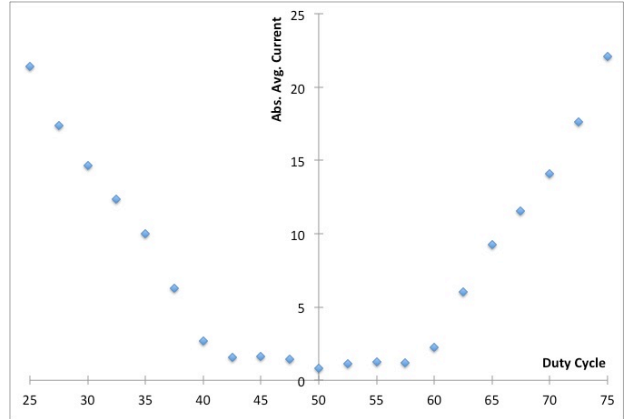


Figure 4.22 – Plot of balancing DC/DC converter absolute value of inductor current versus set duty cycle.

Figure 4.21 and Figure 4.22 plots neutral point (50%) differ from Figure 3.24's (40%). This is because Figure 3.24's formula considers the duty cycle from 0% to 90%, where the last 10% are part of the dead time. The hardware controller that generates the switching signals for Figure 4.21 and Figure 4.22 automatically inserts the deadtime, allowing 0% to 100% to be selected.

Figure 4.22 shows that as average inductor current nears the DCM and neutral CCM transitions, the inductor current changes very little relative to the duty cycle. This is very similar to the simulations shown in Figure 3.24. Updating the model with slightly higher resistor values yields Figure 4.23. The measured data points fit the approximation outlined in Section 3 with a R^2 value of 0.9952.

V1=3.33V, V2=3.33V, R1=0.052ohm, R2=0.052ohm, L=4.7uH, f=100kHz

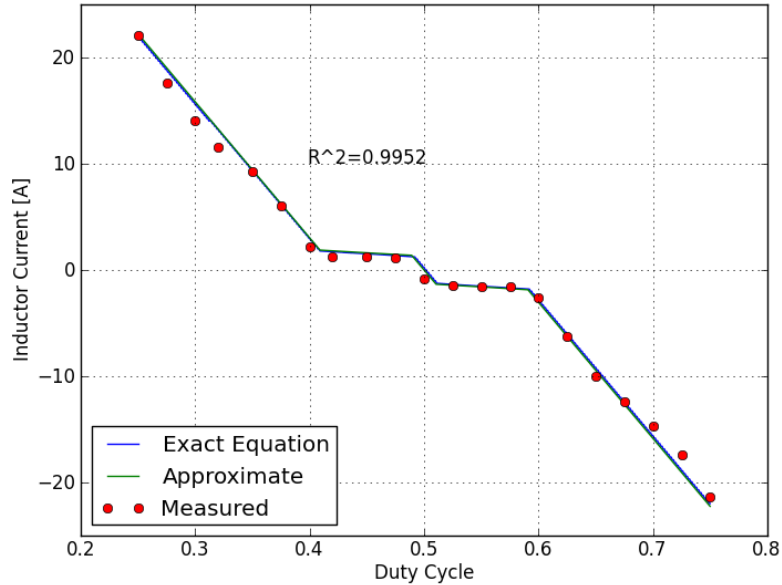


Figure 4.23 – Plot of measured data compared with exact equations and approximate equations.

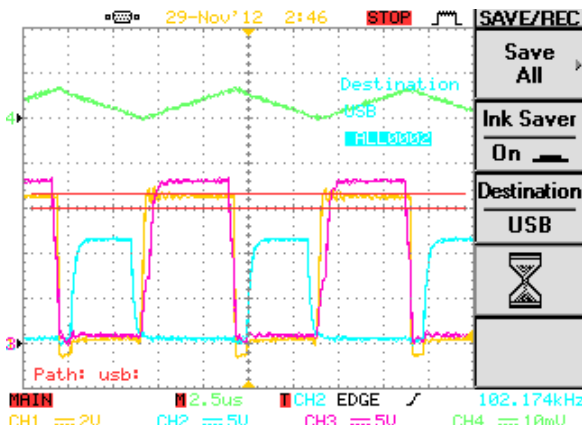


Figure 4.24 – Screen capture of active balancing circuit operating at 42.5% duty cycle.

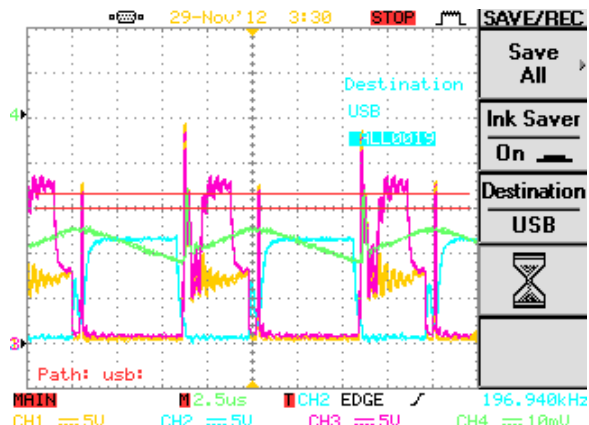


Figure 4.25 – Screen capture of active balancing circuit at 70% duty cycle. This screen capture shows significant ringing on the high side gate.

CH1 is the switching node, CH2 is the low side MOSFET gate, CH3 is the high side MOSFET gate, and CH4 is the current probe (5A/10mV).

Ringing in the converter became more noticeable as the duty cycle increased. Populating the pads for an RC snubber could minimize this ringing possibly but there was not sufficient time to tune the snubber before testing. Additionally, each configuration with different bus bars potentially would require a different selection of resistors and

capacitors for the snubber. Figure 4.26 shows four PCBs mounted to the four cells of the pack. At the time of the picture, not all components were populated on the boards.

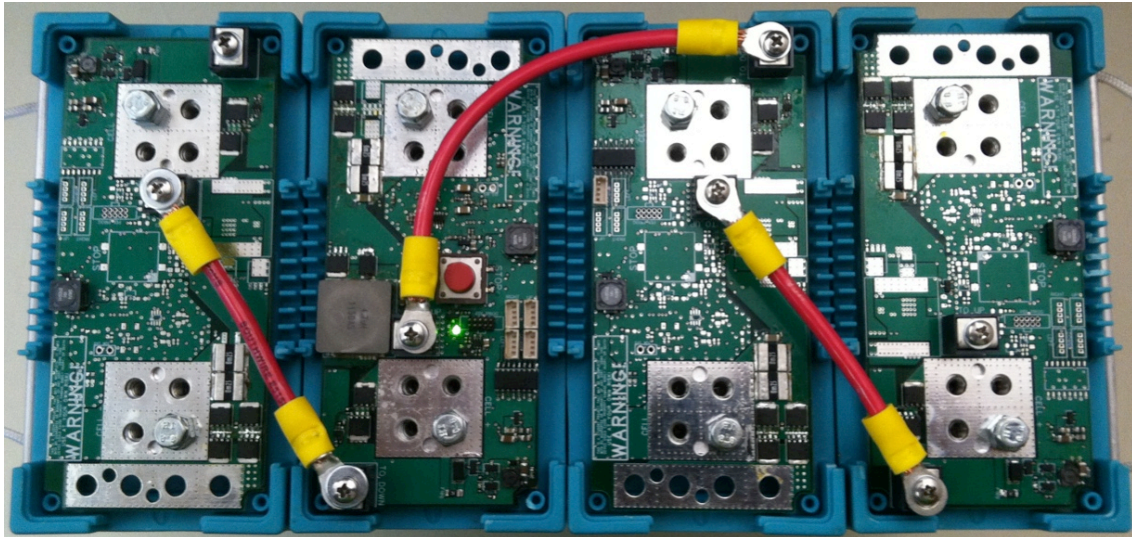


Figure 4.26 – Picture of four PCBs mounted on top of the battery pack. Not all components are populated.

4.3 Input Power and Supplies

4.3.1 System Power Measurements

The goal for current draw was to be less than 1mA average current consumption. This was to be achieved by sleeping the microcontroller as much as possible and relying on low power consumption circuits to gather data. The active balancing circuit current draw was exempt from this 1mA average current draw. Despite the goal of less than 1mA, the idle current was measured to be 4.794mA, which was nearly 5 times the goal. At nearly 5mA of continuous draw, this would discharge a 100Ah cell in 2.3 years. Depending on the application, this may not be an issue.

The measured total of 4.794mA was slightly higher than a real use case because the software had not been optimized. Sleep had not been introduced and minimizing the usage of microcontroller modules had not been implemented. Even if these had been added, the total would still have exceeded 3.5mA. Table 4.4 summarizes the power sources and their current draw.

Table 4.4 – Summary of power consumption.

Supply Name	Balancer Disabled	Balancer Enabled	
Microcontroller		1.090mA	Analog + Digital
PP2V2		1.013mA	Digital Section
PP2V2_VA		1.222mA	Analog Section
PP11V0	1.469mA	48.797mA	Gate Driver + Ext. Disconnect + DCDC Down Enable. (3.3V input)
Total	4.794mA	52.122mA	

The current draw from PP2V2 (PP2V2_ALWAYS), which is the supply for digital logic ICs, was higher than expected by nearly 4 times. There are only a few current sinks attached to this supply and all of the datasheets specify that the current draw should be in the microamp range. At this time, there is no explanation to why the current draw is higher than expected, but it is likely the communications circuit is responsible.

The current draw from PP2V2_VA was also analyzed because the current was higher than expected since all of the components selected have very low current consumption. After looking through all of the data sheets and compiling a list of current sinks, the value seemed reasonable. Table 4.5 details a list of current sinks attached to the PP2V2_VA rail. Figure 4.27 shows a breakdown of the currents in a pie chart, which was generated from the maximum current draw of each IC. While 1.222mA is closer to the maximum supply draw of all of the ICs, it is not unreasonable.

Table 4.5 – Breakdown of analog current sinks based off of IC data sheets.

Sub Circuit	TYP [uA]	MAX [uA]
Supply Voltages	248	333
NTC	7.72	44
External Temp	85	170
Current Amplifier	261	402
Coulomb Counting	140	210
Battery Voltage	65	100
Current Limit Detection	100	124
	907	1383

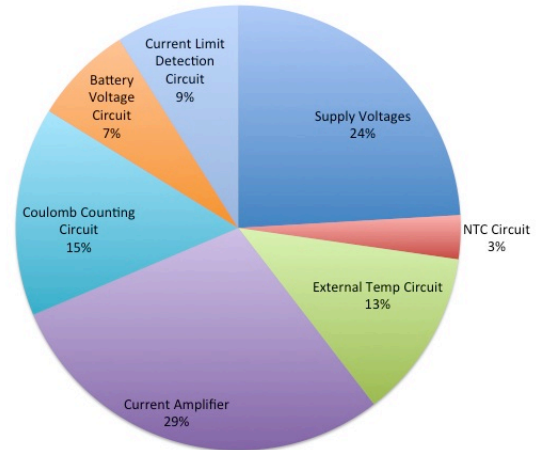


Figure 4.27 – Pie chart showing sinks of analog supply (PP2V2_VA) current consumption.

The PP11V0’s boost’s quiescent current and draw from enabling the battery disconnect circuits is covered in the Boost Efficiency section of this paper. It should be noted that the gate driver used for the switching signals of the balancing circuit draws a significant amount of current. As noted in Table 4.4, when the gate driver is idle, the boost draws 1.469mA. At this input current, from collected data shown in the Boost Efficiency section, the efficiency is between 65% and 71%. Using efficiency between these values results in a value that is nearly the typical quiescent current draw for the gate driver (LM5109) of 0.3mA.

Finally, the high current state of PP11V0 is when the gate driver is actively running at 100kHz. The measured input current was 48.8mA, and using an efficiency of 68.8% (a data point was taken at 47.4mA for measuring the boost efficiency) as an estimate, this results in an output current of just under 10mA. Reviewing the data sheet for the LM5109 shows that a capacitive load of 4.4nF should have a current draw of approximately 6mA. The gates of the MOSFETs used in the balancing circuit have an input capacitance of nearly 6.8nF, which would result in a current of more than 6mA.

4.3.2 Input Filter

The input filter is one of the first circuits that input power goes through before reaching the voltage regulators. The circuit is comprised of a second order LC filter with a damping circuit. It has a cutoff frequency just above 5kHz and does not resonate. See Table 5.5 for a list of data points and Figure 4.28 for a plot of these data points.

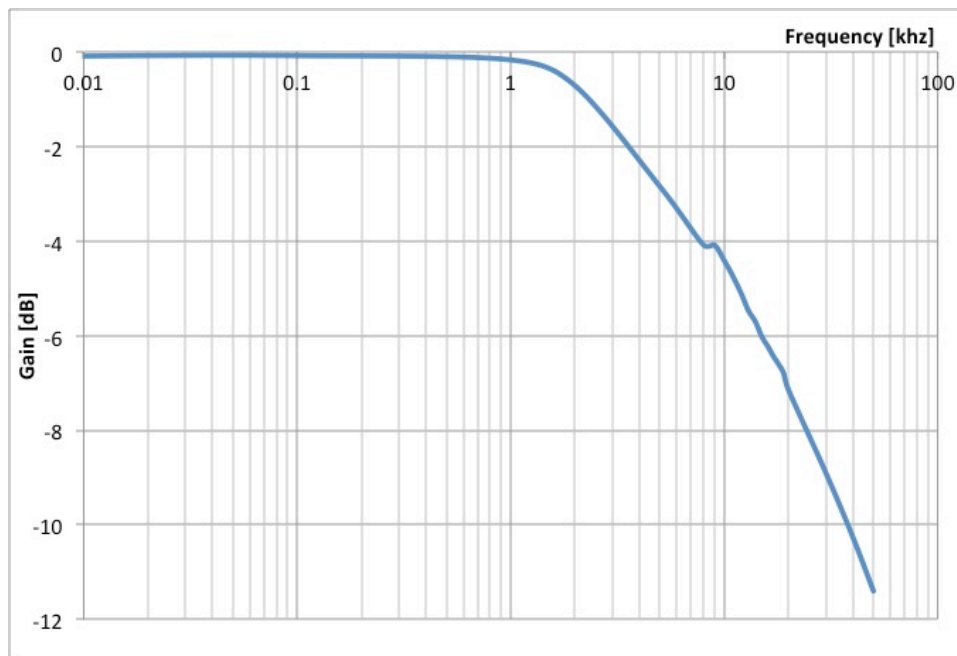


Figure 4.28 – Plot of frequency response of input power filter.

As the main input filter, it expects to see a non-trivial amount of current. Estimations and testing showed that this should not exceed 500mA. In order to test the frequency response and detect any resonance, a function generator capable of sourcing more than 500mA was required. Unfortunately, the function generators in the lab are not capable of sourcing this much current. To remedy this, a high-powered op-amp ($\pm 16V$

rails at 3A, 3MHz bandwidth with unity gain) was set up to be a voltage follower to add a buffer for the function generator.

The input filter was initially a nice-to-have feature to help the voltage regulators to maintain a constant output voltage. It was during early testing of the DC/DC converter that the filter's importance became evident. The initial filter comprised of a simple RC filter with a very small resistor and a very large capacitor. Unfortunately, during the testing of the converter, the voltage of the cell jumped up and down approximately 100mV (this may have been due to the length of wires used), which resulted in a rapid charging and discharging of the previous design's input capacitor. This rapid charging and discharging exceeded 1A in some cases, which caused the input fuse to blow (it was rated at 400mA at that time). Additionally, the capacitors were not able to fully filter this response. As a result, the input to the regulators was noisy and the noise appeared on the output of the regulators as well. By changing the circuit to a LC filter, testing showed a more stable input to the regulators and a clean output from the regulators.

4.3.3 Input Protection

The input power to the logic and analog circuits has negative voltage protection and over voltage protection. Both circuits work, however the over-voltage protection

circuit varies slightly from one to the other, as the gate threshold of each MOSFET is not exactly the same. Testing of four circuits showed a sample range from 4.2 to 4.6V.

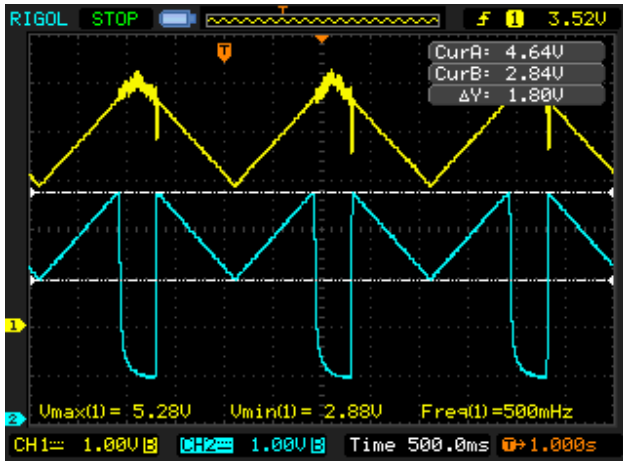


Figure 4.29 – Screen capture showing the overvoltage protection.

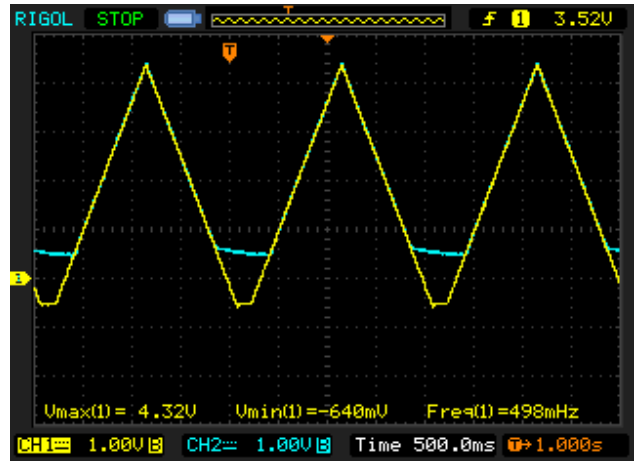


Figure 4.30 – Screen capture showing the negative voltage protection.

For both screen captures, channel 1 (yellow) is input and channel 2 (blue) is output from circuit.

Both the negative voltage and over voltage protection both suffer from slow response time. They both operated in the low tens of hertz. At higher frequencies, even 100Hz, they were incapable of protecting the circuit. Smaller resistors would fix the response time at the cost of power loss. Also by adding a diode between the drain and gate of the PMOS, the gate would discharge more rapidly in a negative voltage situation. Despite this draw back, these two circuits saved the test board numerous times due to user error during testing.

4.3.4 Boost Efficiency

The boost circuit is based off an example circuit from application notes for the IC^[27]. However, despite it being a previously tested circuit, each layout for a DC/DC

converter results in a slightly different efficiency. The boost converter was a concern since it could affect battery life if the converter was drawing a significant amount of current. The peak efficiency measured for the converter was 78% with an output load of 5mA, which is not a typical load. Near no load and around 10mA are typical loads for the BMS.

The datasheet specified the quiescent current as 65 μ A typical and 75 μ A maximum. However, 287 μ A was measured while only keeping the battery disconnect circuit enabled. Assuming a worst case of 75 μ A quiescent current this leaves 212 μ A unaccounted for. At a very low load (between 10-20 μ A), the efficiency was measured to be less than 25%. At 25% efficiency, with a 3.3V input and an 11V output, this results in an input current of over 200 μ A.

As expected, the efficiency of the converter was low through out most of the operating range. The main driving factor for choosing this IC was its low quiescent current. While near no-load is a typical operating point, another operating point is 10mA output current. This operating point is when the gate drivers are used to run the active balancing DC/DC converter. With a 10mA load, the efficiency ranges from 65 to 69%. Figure 4.31 shows a plot of boost efficiency and output voltage versus load current. The output voltage was measured and plotted because it droops at high load. However, during active balancing (100kHz switching frequency) the output of the boost did not droop. Increasing switching frequency could potentially cause the boost converter output to droop. This would have an adverse impact on not only the gate driver; but also the external disconnect switch, and the DC/DC down enable switch.

The converter's line and load regulation were measured. Line regulation was measured from 2.5V to 4.2V and resulted in a measurement of 7.2%. The measurement at 2.5V heavily affected this measurement, despite the IC being rated to operate at this point. The load regulation was measured from 10 μ A to 35mA (just above no-load and the highest measured data point before output voltage drooped), and this resulted in a load regulation of 2.04%.

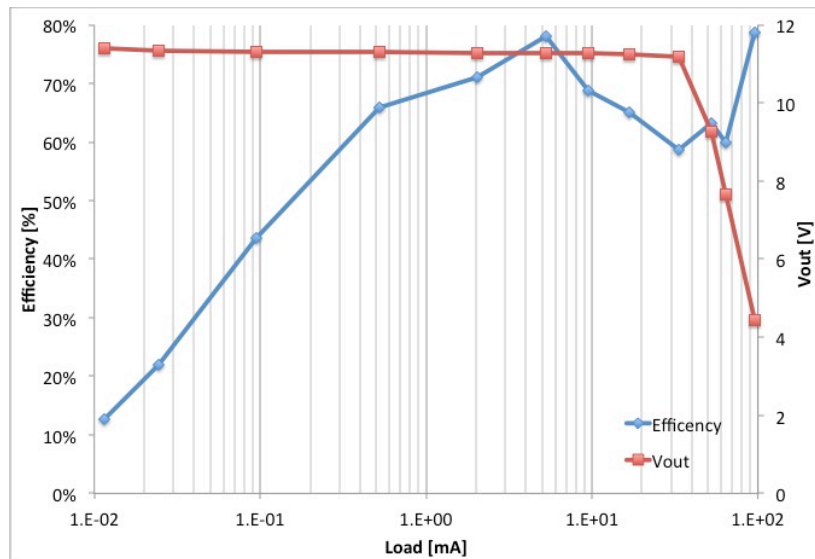


Figure 4.31 – Plot of boost efficiency and output voltage versus load current. $V_{in} = 3.3V$

4.3.5 Analog Power Filter

The analog power filter was intended to suppress the noise from the digital side. Unfortunately, the filter did not have an optimal frequency response. This filter was designed to be a second-order LC filter with a cut off around 10kHz. This filter was similar to the main power filter except the inductor was 10 times larger and the capacitor was a tenth of the size. This was done to make the resistor for the snubber 5 Ω instead of

0.5Ω to reduce the peak current near the un-damped resonant frequency. Unfortunately, the capacitance near each regulator (these were considered) shifted the resonant frequency lower than expected and caused the output to be insufficiently damped. Figure 4.32 shows a plot of the frequency response.

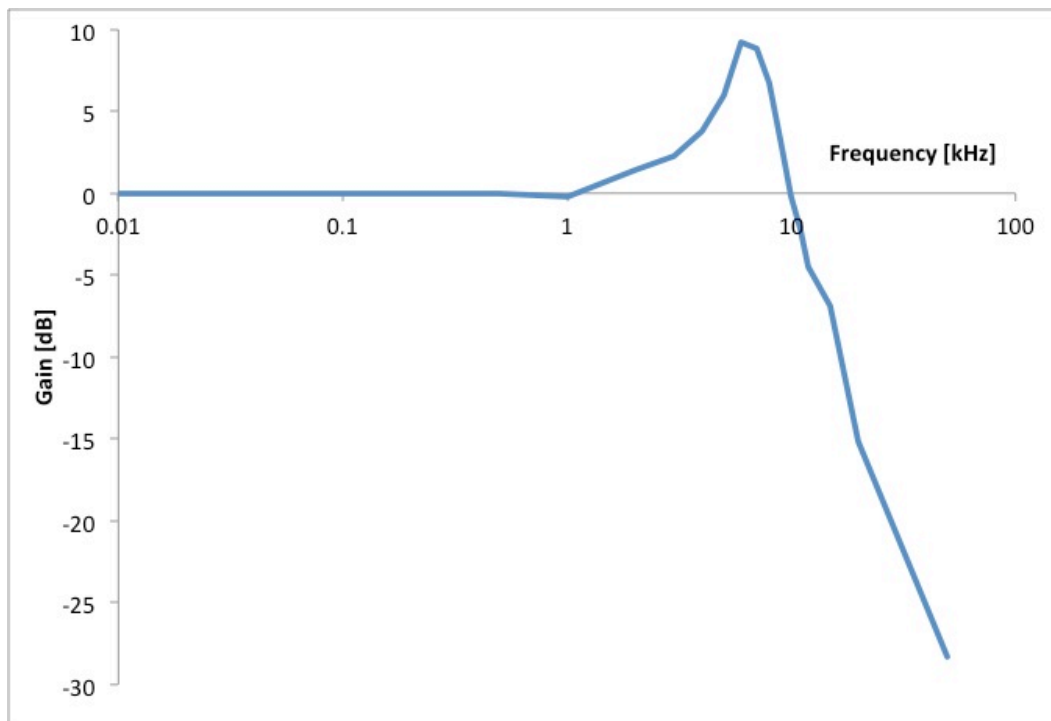


Figure 4.32 – Plot of frequency response of analog circuit power filter.

As expected, the resonant frequency was lower than 10kHz. However, the additional capacitance near each of the regulators affected the circuit more than expected. Evaluating the new resonant frequency, a snubber resistor of 2Ω should have been used to minimize the peaking.

While this is a problem because of the snubber's design, this will not damage the circuit. The regulators that connect to the output of the filter can handle an input voltage as high as 16V. The input protection circuits before this circuit prevent the output from reaching 16V. Additionally, the resonant frequency is 6kHz, which is a frequency easily

suppressed by the voltage regulator. Another mitigating factor is the input power filter, which was discussed in a previous section, has a cut off frequency around 5kHz. As a result, the input to the analog filter will be attenuated by at least 3dB.

Beyond the circuit components capable of handling the peak voltages, generating an input voltage change of a volt or more from such a large battery would be challenging. While not impossible, many applications would not ever see this occur. Finally, none of the internal circuits are designed or configured to switch at 6kHz. While the communication circuit or DC/DC converter both could be configured to operate at this frequency (and potentially cause the voltage to swing), neither would benefit from doing so. If the DC/DC converter did operate at such a low frequency, one of the fuses would blow before the analog filter began to resonate.

4.4 Communications

The communication circuit was designed to communicate with adjacent cells or a computer. The circuit has been verified to communicate bi-directionally via opto-isolators. The recommended baud rate is 9600 because it results in very low transmission errors.

The initial design goals aimed for 115.2k baud, however it was quickly obvious that the selected opto-isolators could not respond fast enough to this data rate. After some testing a lower baud rate of 19.2k was selected. This baud was used in revision A. However, it was found that differences in opto-isolator packages (same part number) were not able to reliably perform at this speed. The baud was dropped to 9.6k to make

data transmission reliable. While this data rate is low, very little data is being transferred between cells and the high speed was only a nice-to-have. Figure 4.33 and Figure 4.34 show screen captures of data being transferred.

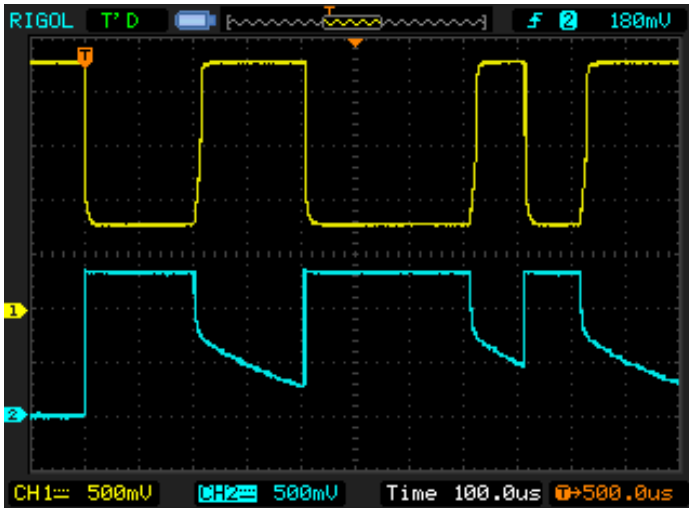


Figure 4.33 – Screen capture showing an ASCII ‘F’ being communicated from board to board. Channel 1 is the output phototransistor voltage and channel 2 is the input diode voltage.

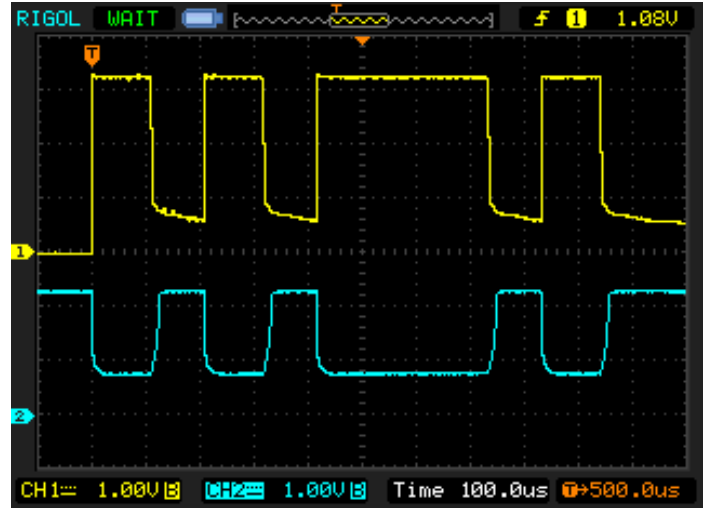


Figure 4.34 – Screen capture showing an ASCII ‘E’ being communicated from computer to board. Channel 1 is input diode voltage and channel 2 is the output phototransistor voltage.

While the communication system works, lower baud increases the power consumption during communication because of the losses due to the resistors. Modifying the resistors values may be a solution to decrease power, however this may cause errors in the data because the rise time (as the switches are turning off) will increase.

Finally, a converter board was used to communicate from a computer to the board. This interface was heavily used to validate all of the other subsystems. The converter board uses an opto-isolator and MOSFETs the same way that the BMS boards do. However, the logic voltage is 3.3V instead of the BMS’s 2.2V. As a result slightly larger resistors were used to maintain a similar current through the phototransistor and diode. The 3.3V rail was supplied by the FT232 UART-to-USB IC. For convenience, a breakout board made by SparkFun (BOB-00718) was used for prototyping. Figure 4.35

shows the converter board connected to a BMS that is also connected to an adjacent BMS board. Figure 4.36 shows the prototyped converter board.

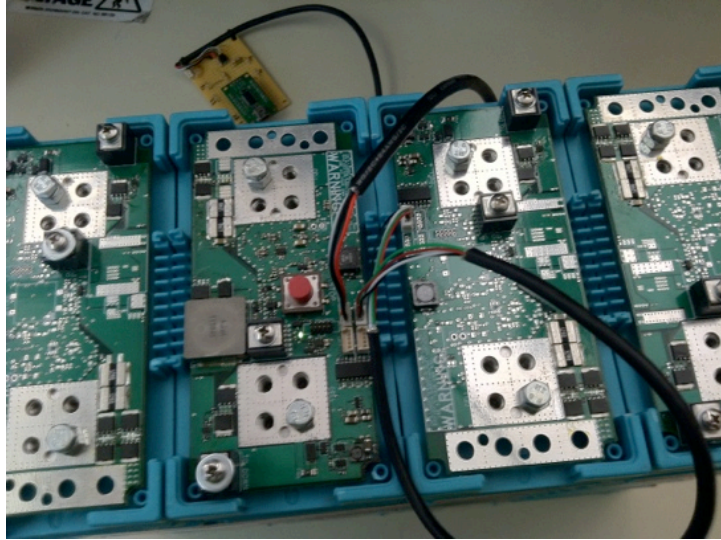


Figure 4.35 – *Picture of a BMS board connected to computer and to adjacent BMS board.*

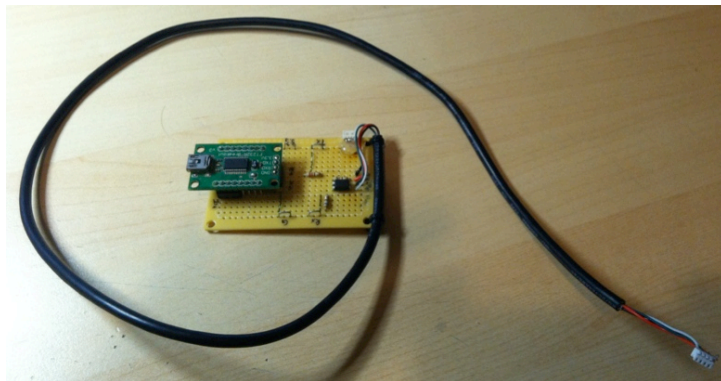


Figure 4.36 – *Picture of the computer-to-BMS interface board.*

Chapter 5 – Conclusion and Future Work

In summary, a battery management system was designed, fabricated, and tested. Three revisions of the circuit board were fabricated to meet most of the goals. The goal was to design a battery management system for a battery pack of large capacity cells of unknown configuration. Electrical hardware was developed to achieve this goal. The hardware is capable of performing rudimentary tasks such as monitoring battery voltage, but it is also capable of measuring current and performing balancing by utilizing an active balancing circuit to minimize heat and losses. While the hardware does work, with the exception of a few less critical sub-circuits, the software to support many of the tasks is still in its infancy. The software is capable of performing a variety of BMS related tasks when prompted to by the user using a command-line interface. The code still lacks a “brain” to determine the most prudent operation to maintain the health and safety of the cell. However, the code does permit validation of hardware components of the design.

Battery management is very open-ended in what capabilities should be available, however the design incorporated many high-end features to improve its usability. To allow for ease of use, custom bus bars were designed to aid in rapid deployment of the system. However, since the bus bars were not critical to the safety of the individual cells, the electrical hardware was given higher priority through the project. Table 5.1 summarizes the target goals also how well the goals were met.

Table 5.1 – This table outlines the goals and their currently measured values in revision C.

Primary Goal

Safe	Software is incomplete. Not 100% safe yet.
Unknown number of cells	Yes. System operates independent of cell quantity.
60Ah+ per cell	Yes – tested with 100Ah cells
Use Atmel AVR	Yes – used XMEGA family of Atmel AVR MCUs

Secondary Goals

Durable	Yes - No loose or delicate components. However, a protective chassis over each cell would be beneficial.
Fits within cell outline	Yes
Low Profile	3/8" height above terminals
Ease of use	Bulbar design have not been use.
Minimal setup	Additional 6 screws and two jumpers for DC/DC converter.
Low Cost	\$94 parts + \$100 board Goal: <\$50 total
High Performance	Project is incomplete. Definitely achievable with one more revision and software support.

Design Overview		
Category	Current Status	Goal
Operating Range	2.5-4.2V	2.4-4.2V (LiFePO ₄ is 2.8-3.6V)
Over Voltage	Protected	Protected
Negative Voltage	Protected	Protected
Fused input	Yes	Present
Current Draw	3.9mA sleep 4.8mA active 52mA balancing	<1mA sleep <2mA active <200mA balancing
Current Measurement		
Range (120A range)	±186A	±120A
Accuracy (120A range)	±2.18A (±2%)	<±1.2A (±1%)
Range (800A range)	±1491A	±800A
Accuracy (800A range)	±3.28 (±0.4%)	<±4A (±0.5%)
Low Resistance Switch	0.7mΩ	<1mΩ
Discharge Limit	Hardware Yes; Software No	Variable
Charge Limit	Hardware Yes; Software No	Variable
Coulomb Counting	Hardware status unknown Software can use digital integration	<5% Error
Battery Voltage	±3mV	<±5mV
Balancing		
Type	Active Cell-to-Cell	Active
Current	22A tested (25A limit)	≥20A
Efficiency	85.3%	≥90%
Cell Profiling		
Internal Resistance	Hardware support. No software yet.	±0.1mΩ
Internal Capacitance	Hardware support. No software yet.	
Capacity Estimation	Hardware needs more testing	5% Error
Remaining Charge	Hardware needs more testing	5% Error
Emergency Disconnect	400A tested 2k+ simulated	800A+ breaking
Temperature Measurement	Cell Temp (optional auxiliary probe) Current sense resistors Power Pulse resistor	Cell temperature Current sense Power Pulse
Communication		
Generalized?	Can connect to any device within 3kV of cell's potential.	
Baud	9.8k	116.2k
User Interface	Yes, via adapter	Required

5.1 Hardware

The hardware portion of the circuit is nearly complete. Ideally, all circuits would work perfectly, but some of the smaller circuits were overshadowed by the more important circuits such as the emergency disconnect circuit and the active balancing DC/DC converter circuits. A few circuits do not work correctly; for example, the threshold detector to determine if the DC/DC converter is not connected does not work as intended. By changing the circuit to a peak detector or using a higher bandwidth op-amp, the circuit would work. There are other circuits that need more testing, and in some cases better equipment to be used to perform the testing. The noise and ripple riding on the analog 2.2V rails was not measured thoroughly enough. One measurement of the output supply was taken, and samples at the input of each amplifier should have been measured as well. Unfortunately, each test is very time consuming to solder probe wires in. As a result a more accurate understanding of the noise is needed in conjunction with an improved noise suppression system. Even without these tests or improvement, digital signal processing could help clean up the data. Some design choices should be reconsidered to reduce cost and improve quality. Below is a brief description of issues and potential solutions:

Integrated ADC:

The use of an internal ADC was problematic because its exceptionally close proximity to high frequency digital circuits. The XMEGA was selected because it satisfied many design goals and it had an integrated high speed ADC. As it turned out

afterwards, this was not one of the best-designed ones. A future design would benefit from using a discrete ADC IC made by a company that specializes in analog ICs.

Current Sense Resistors:

Another concerning design choice was the use current sense resistors on each cell. In its current state, the sense resistors nearly double the cell's internal resistance (1.4m Ω total). This adds more resistance to the discharge path, which may be unacceptable in certain applications. In a system that has very large continuous currents, a single probe on the output of the entire pack may be superior. Further investigation is required to determine if this design choice needs to be changed.

Current Sensing Amplifier:

One of the biggest design choices in this project was how to measure current into and out of the cell. The solution that was chosen is high bandwidth, but very high cost. If high bandwidth is necessary, then the presented design is a good choice. However, many designs may not need such a high bandwidth amplifier and using a limited bandwidth of 1-10kHz could have reduced the component cost to only a few dollars instead of nearly thirty. Also, using a lower bandwidth solution would have permitted the use of multiple ICs that would permit variable gain, yet reducing complexity.

5.2 Software

As in nearly every project, the devil is in the details. After months of design work and several months of code writing, the result was still in an insufficient amount of code. Most of the code was written on a smaller processor that lacked the capabilities to run a RTOS to handle the time sensitive tasks. As a result, the code was written using a queuing task management system. This system worked reasonably well until more complicated interactions between tasks started to be written. At that point, the program memory space of the processor was maxed out and a larger processor with more RAM was used. The new processor was fully capable of handling a RTOS, which would be the ideal way to handle this project. Also, now that the hardware is done, starting the code over would result in a cleaner solution.

One important factor in this code was its safety. Since a failure of the code could cause destruction, rigorously tested code is required. As an electrical engineer, not a software engineer, time was spent ensuring that the hardware would be safe and leave the software task to a more experienced code writer.

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Appendices

A. System Overview

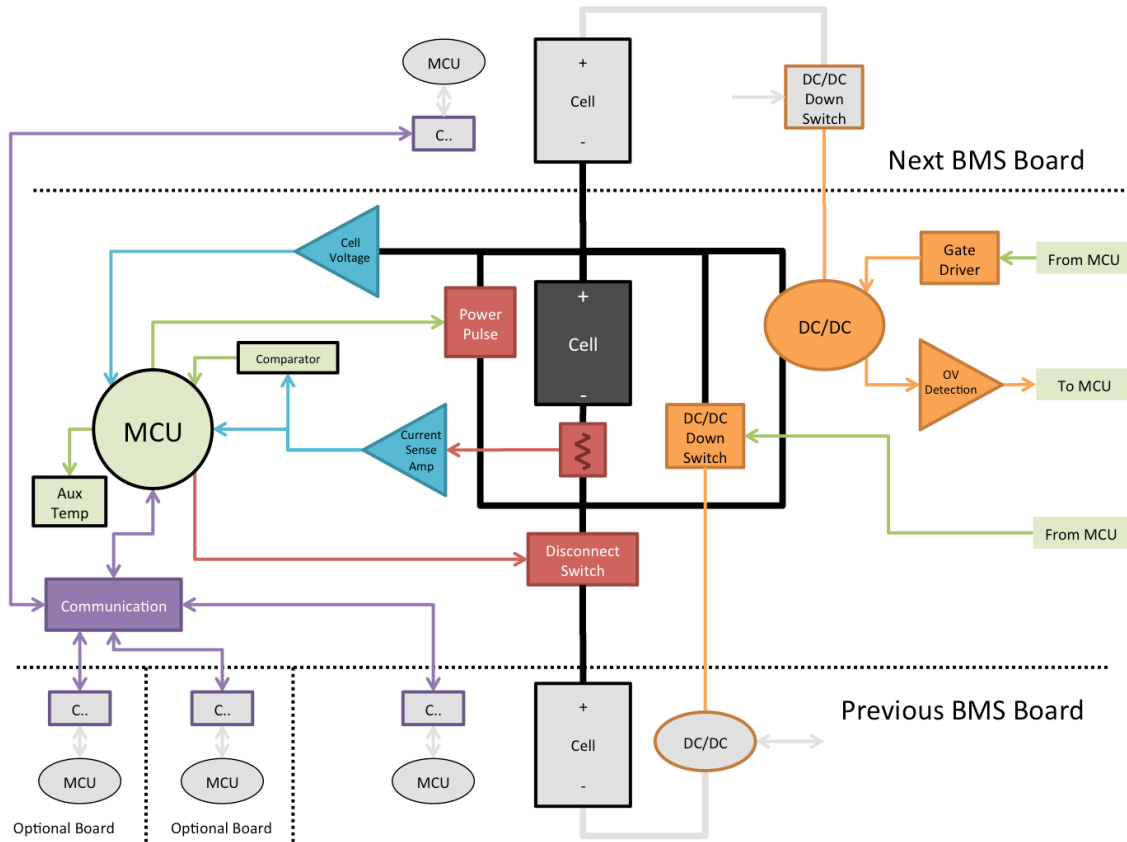


Figure 5.1 – System overview of the design. Shows connections to adjacent cells.

A.1 Power Distribution

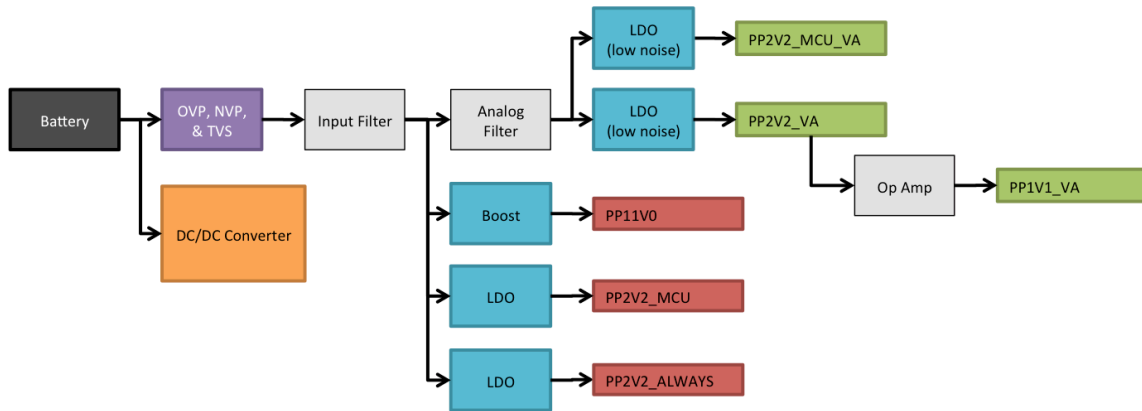


Figure 5.2 – Overview of supply voltage generation.

B. Schematic (Revision C)

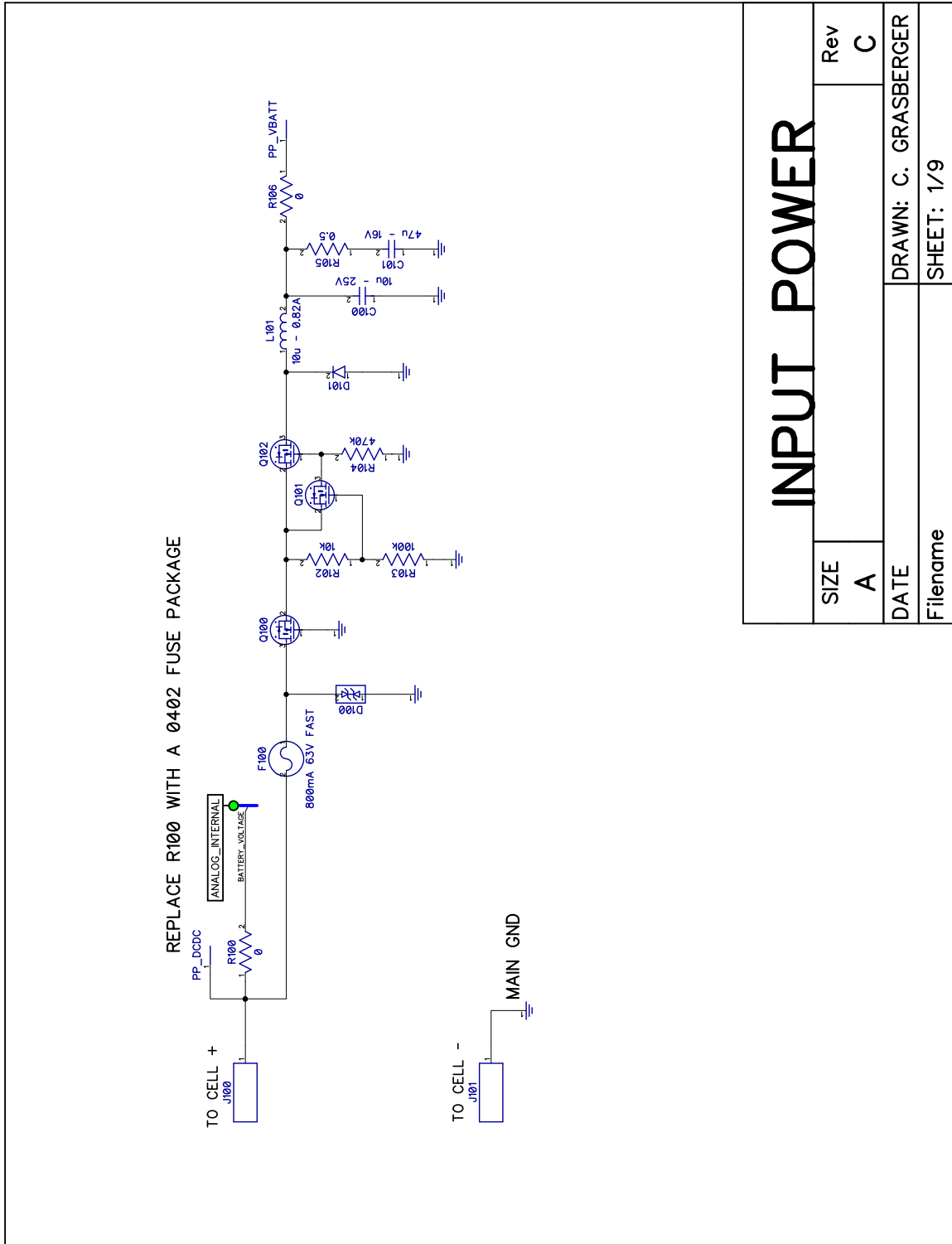
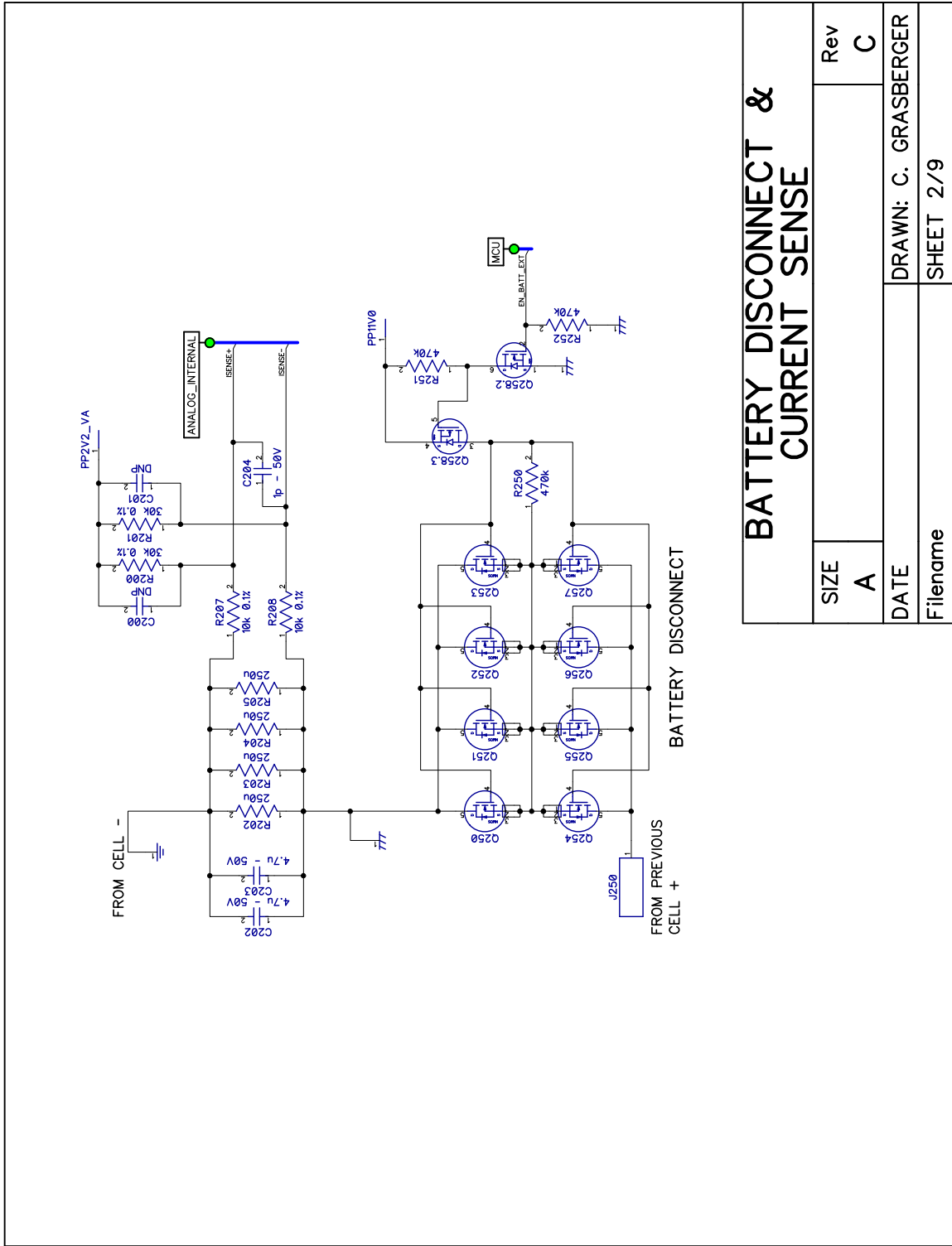


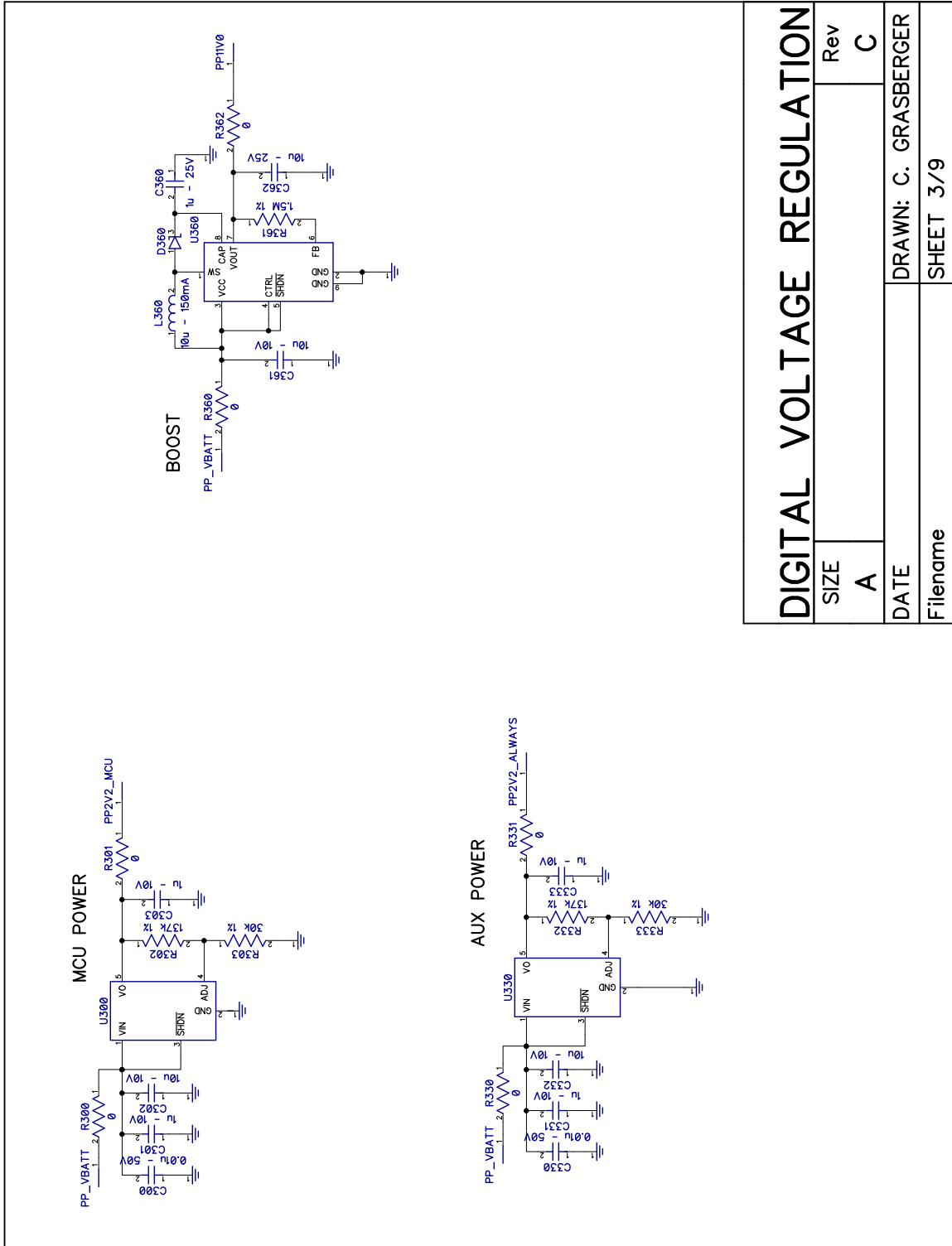
Figure 5.3 – Revision C Schematic – Page 1 – Input Power



BATTERY DISCONNECT & CURRENT SENSE

Rev	C
SIZE	A
DATE	
Filename	
DRAWN: C. GRASBERGER	
SHEET 2/9	

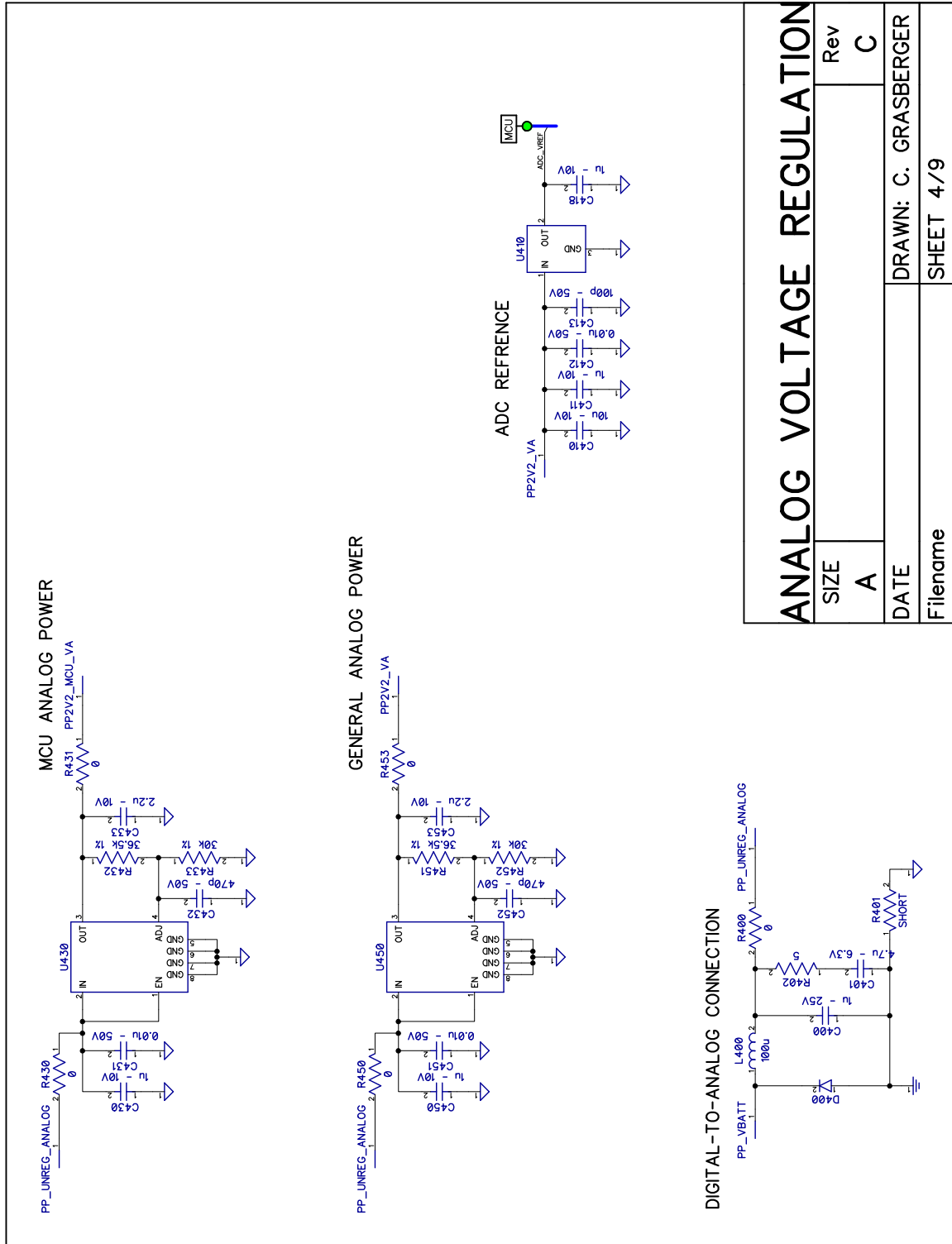
Figure 5.4 – Revision C Schematic – Page 2 – Disconnect



DIGITAL VOLTAGE REGULATION

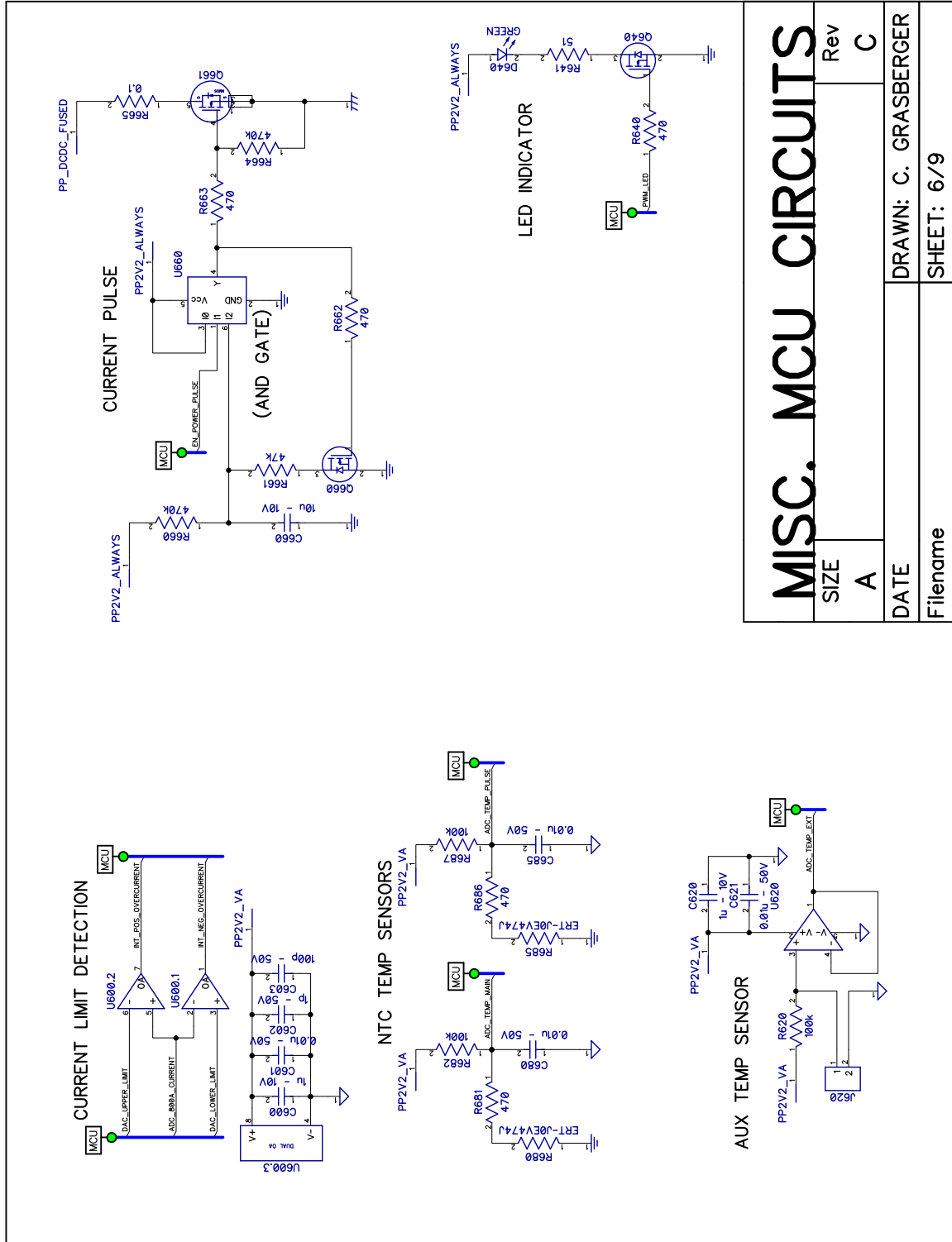
SIZE	Rev
A	C
DATE	DRAWN: C. GRASBERGER
Filename	SHEET 3/9

Figure 5.5 – Revision C Schematic – Page 3 – Digital Voltage Regulation



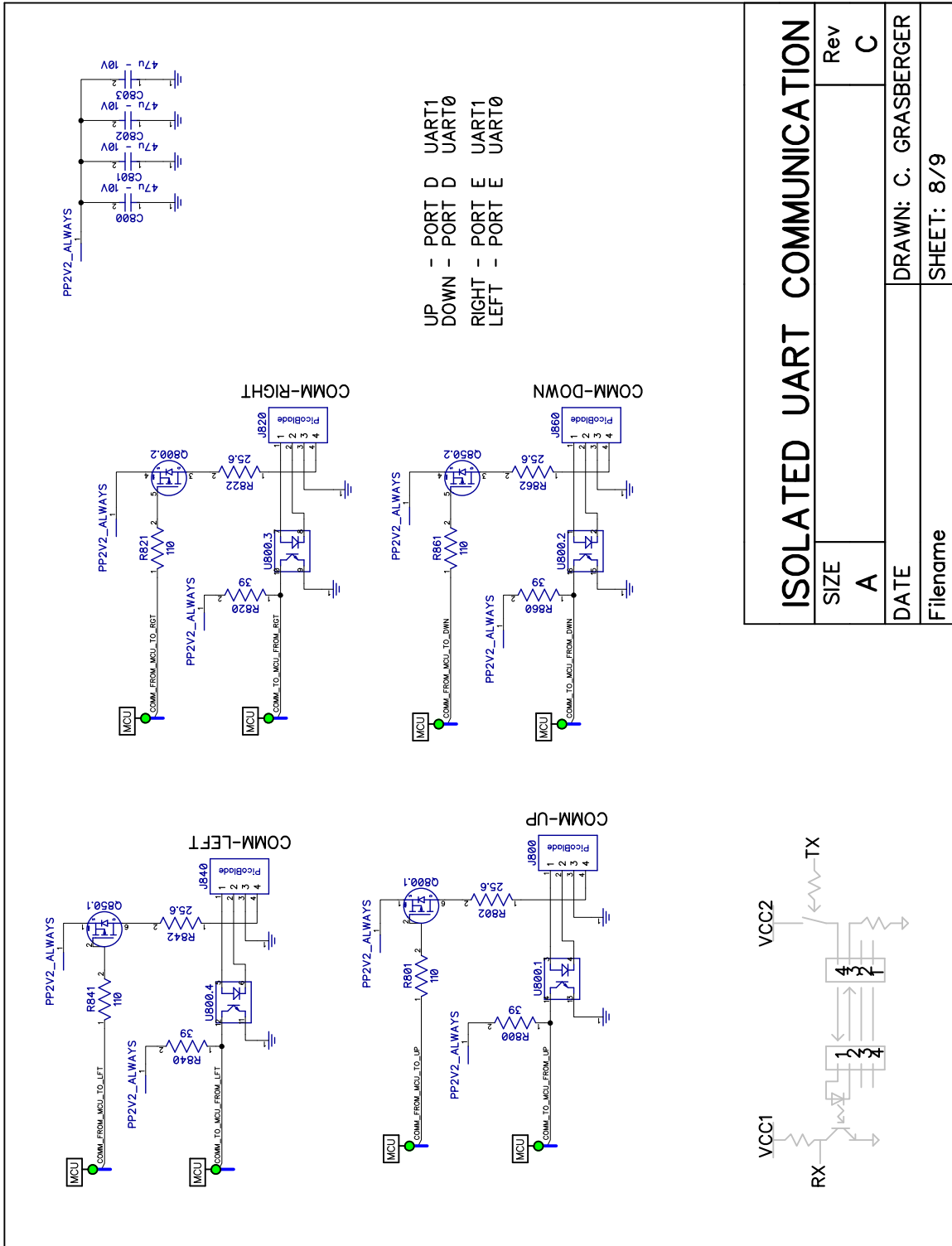
ANALOG VOLTAGE REGULATION		Rev
SIZE	A	C
DATE	DRAWN: C. GRASBERGER	
Filename	SHEET 4/9	

Figure 5.6 – Revision C Schematic – Page 4 – Analog Voltage Regulation



MISC. MCU CIRCUITS		Rev
SIZE	A	C
DATE	DRAWN: C. GRASBERGER	
Filename	SHEET: 6/9	

Figure 5.8 – Revision C Schematic – Page 6 – Miscellaneous MCU Circuits



ISOLATED UART COMMUNICATION		Rev	C
SIZE	A	DATE	DRAWN: C. GRASBERGER
Filename		SHEET: 8/9	

Figure 5.10 – Revision C Schematic – Page 8 – Communication

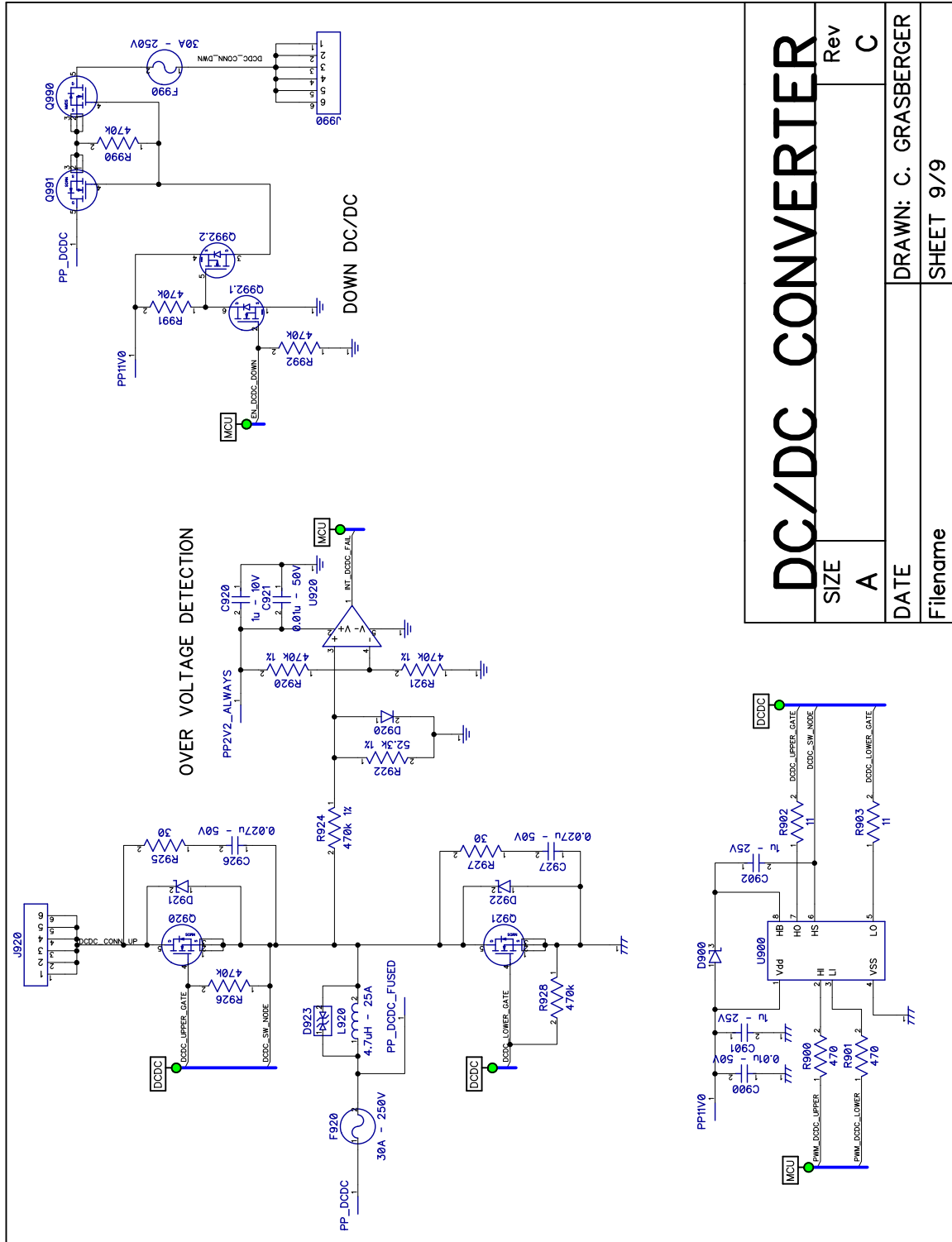


Figure 5.11 – Revision C Schematic – Page 9 – DC/DC Converter

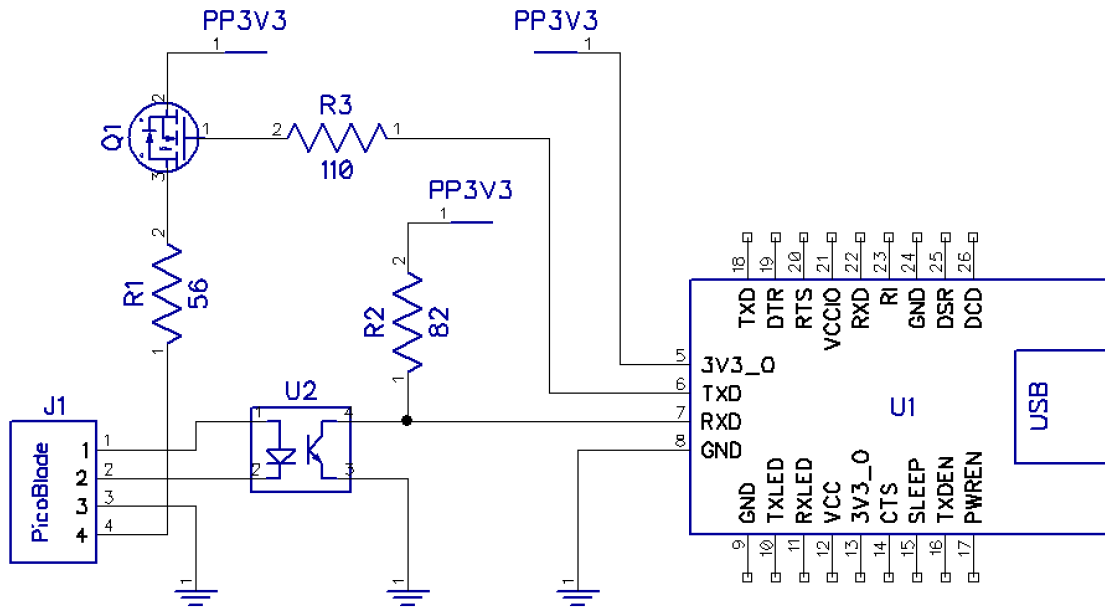


Figure 5.12 – Schematic for UART-to-USB adapter board.

The UART-to-USB adapter board is not integrated into the main PCB. See Figure 4.36 for a picture of the assembled circuit.

C. Printed Circuit Board (Revision C)

C.1 Highlighted areas

C.1.1 Top Layer

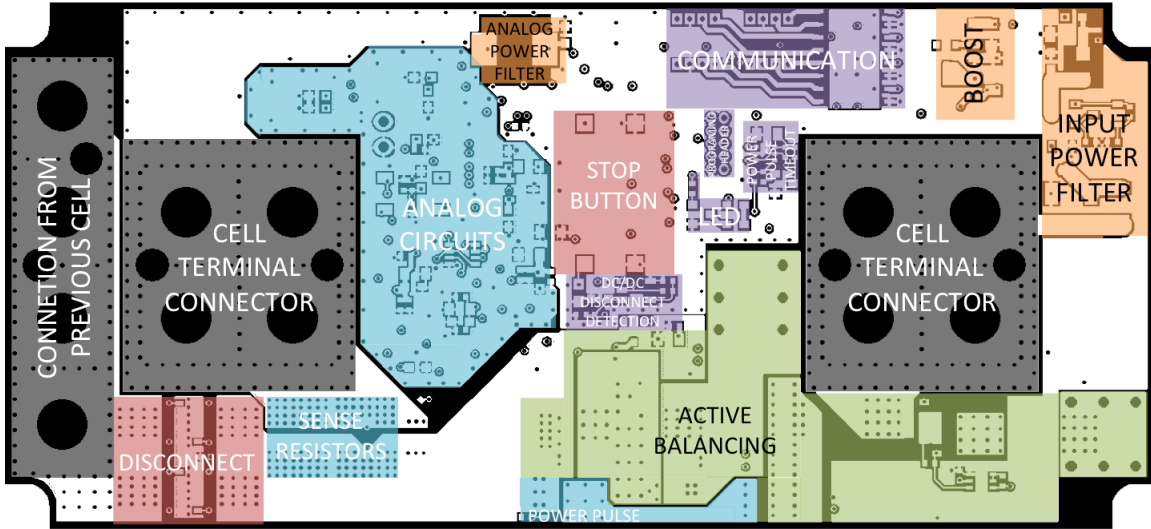


Figure 5.13 – Top side of Revision C board with important zones highlighted.

C.1.2 Bottom Layer

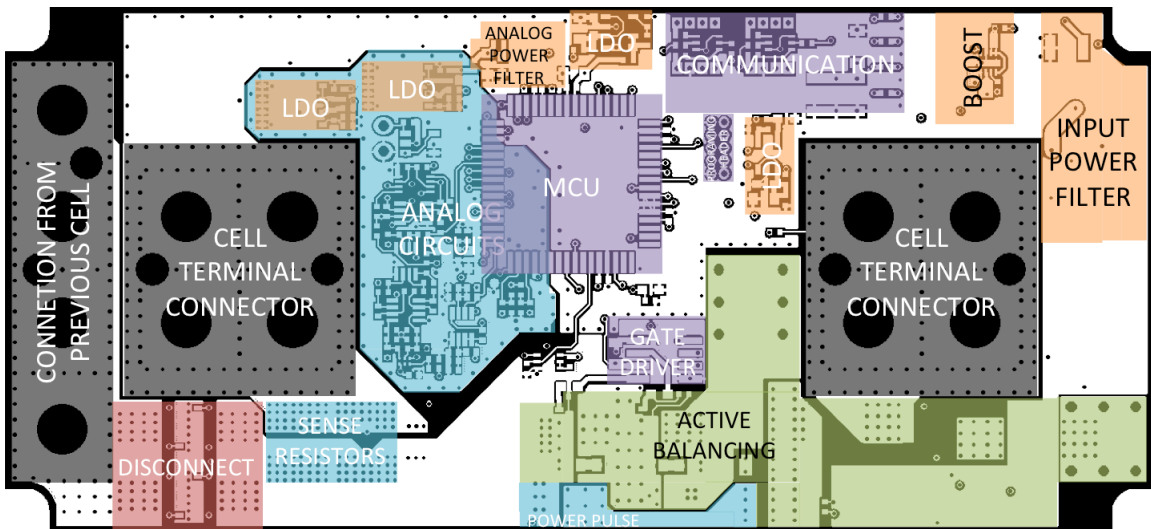


Figure 5.14 Bottom side of Revision C board with important zones highlighted

C.2 Plain Gerber

C.2.1 TOP – SIGNAL & COMPONENTS

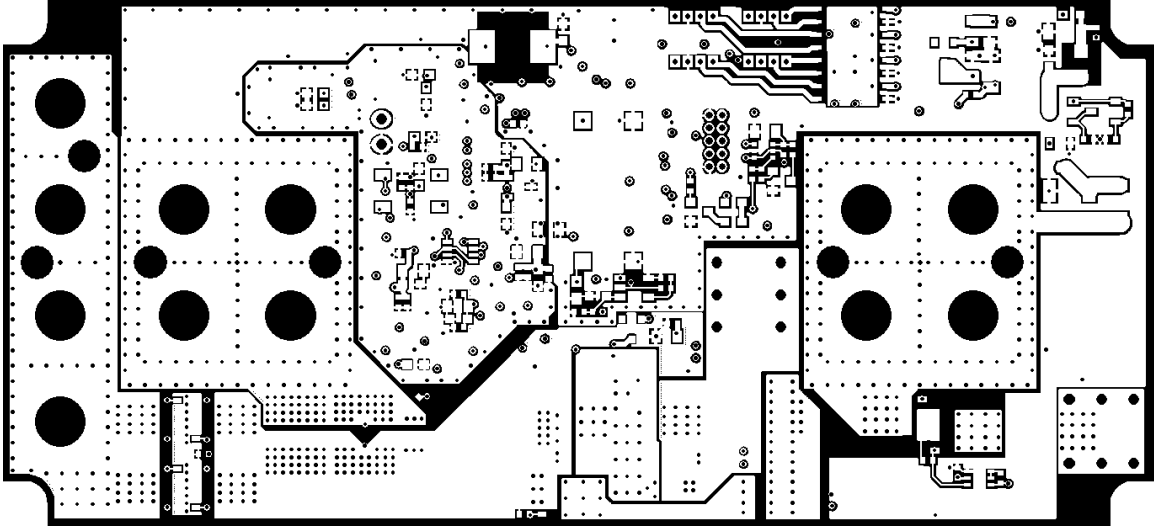


Figure 5.15 – Screen capture of top layer from PCB Gerber file.

C.2.2 ISL2 – SIGNAL

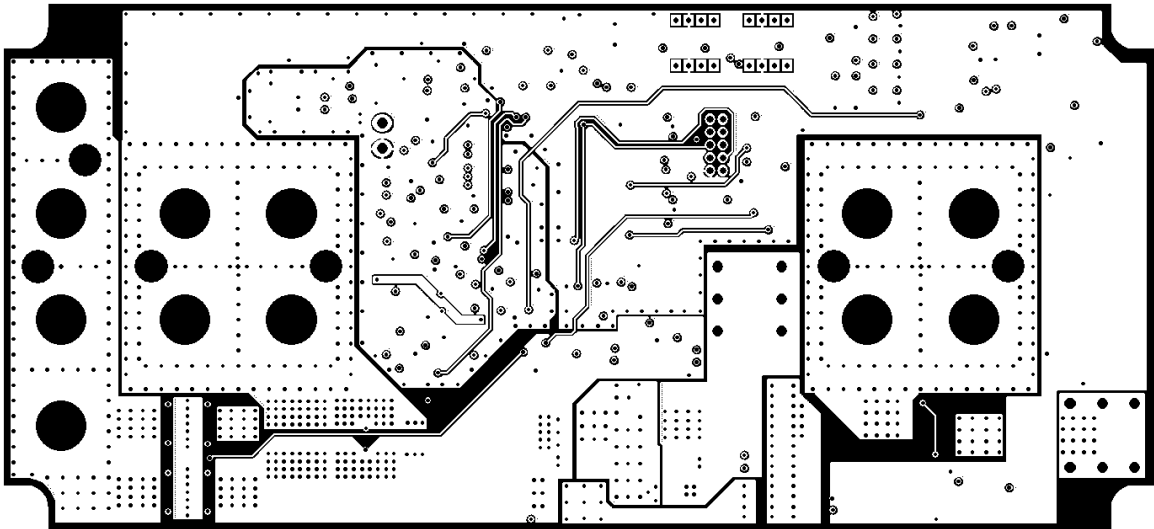


Figure 5.16 – Screen capture of inner layer 2 (signal layers) from PCB Gerber file.

View is looking through the top to the backside. Image may be flipped as a result.

C.2.3 ISL3 – POWER

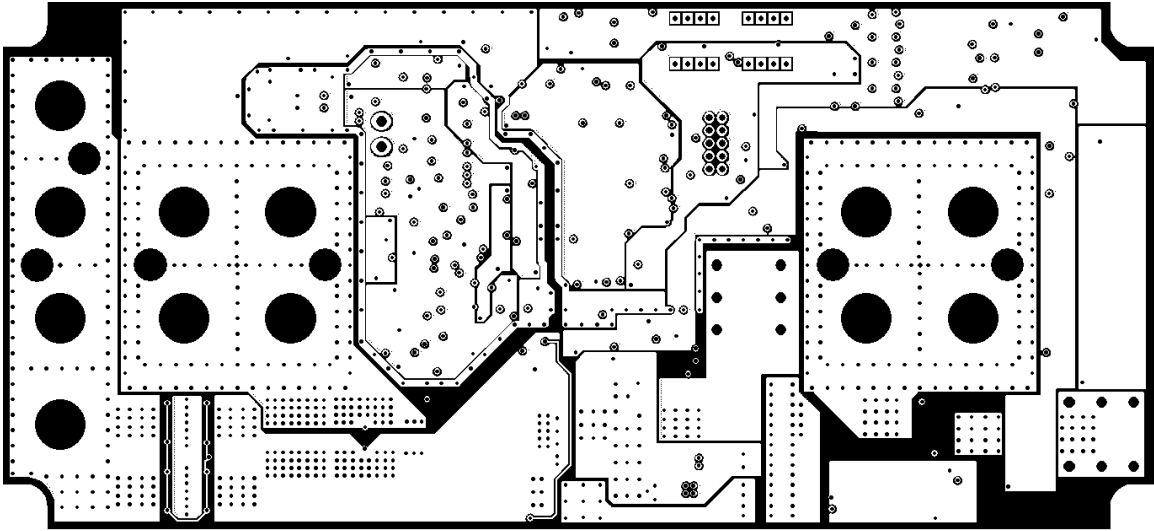


Figure 5.17 – Screen capture of inner layer 3 (power planes) from PCB Gerber file.

View is looking though the top to the backside. Image may be flipped as a result. Color images can be seen in Figure 3.30

C.2.4 ISL4 – GROUND

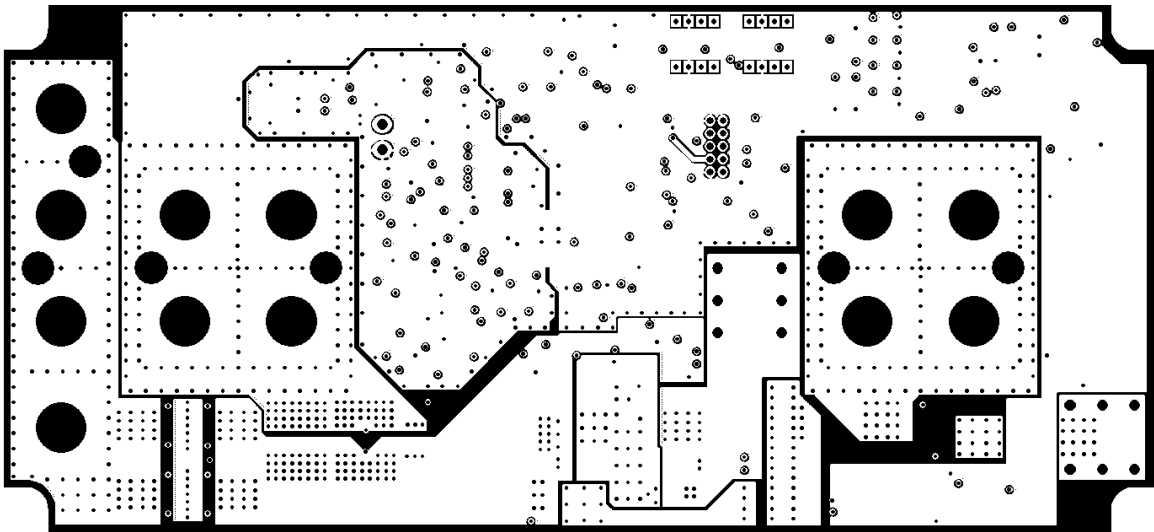


Figure 5.18 – Screen capture of inner layer 4 (ground planes) from PCB Gerber file.

View is looking though the top to the backside. Image may be flipped as a result. Color image can be seen in Figure 3.31

C.2.5 ISL5 – SIGNAL

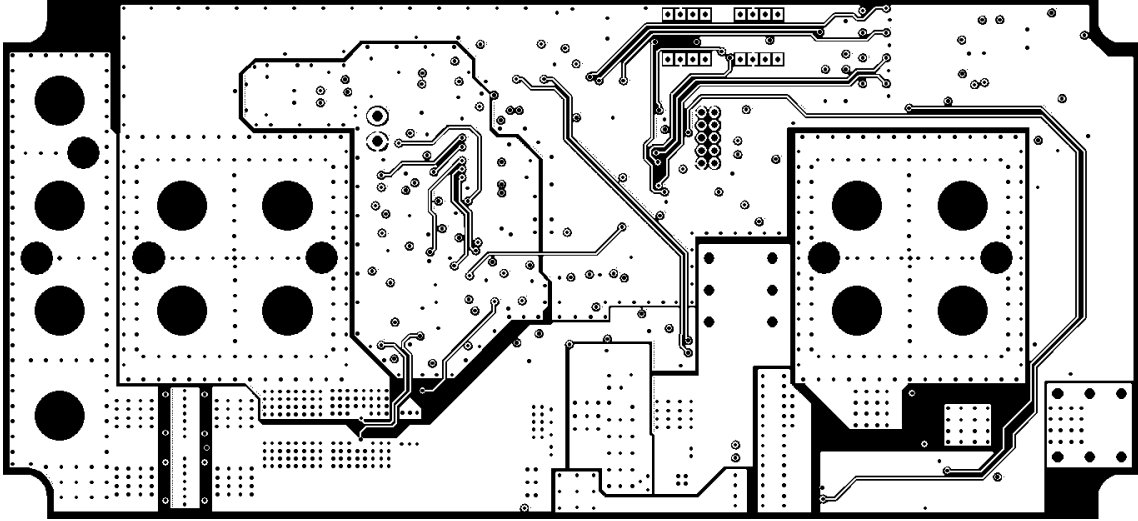


Figure 5.19 – Screen capture of inner layer 5 (signals) from PCB Gerber file.

View is looking through the top to the backside. Image may be flipped as a result.

C.2.6 BOTTOM – SIGNAL & COMPONENTS

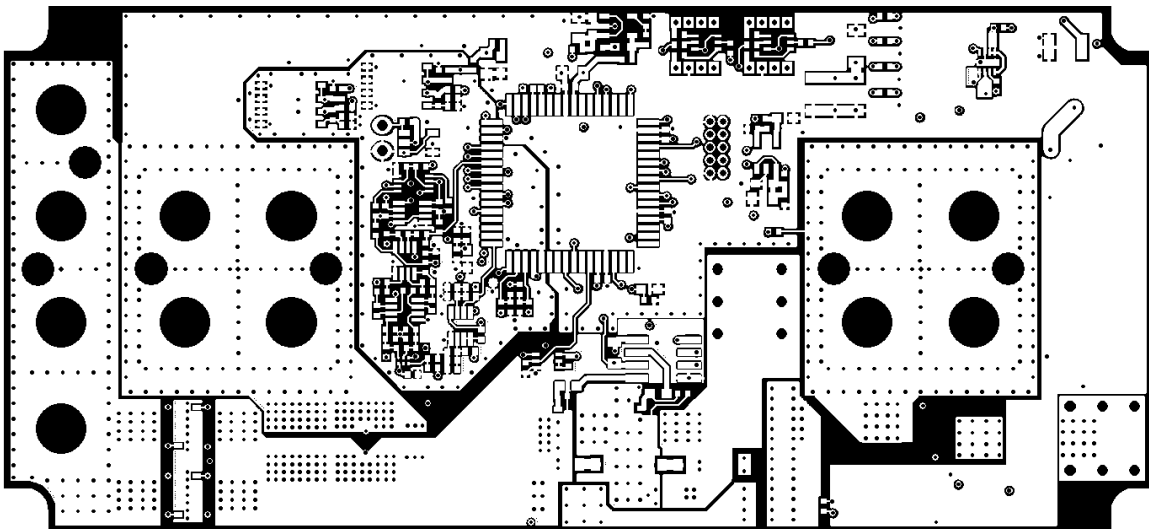


Figure 5.20 – Screen capture of the bottom side (layer 6) from PCB Gerber file.

View is looking through the top to the backside. Image may be flipped as a result.

C.3 Revision C PCB Photos

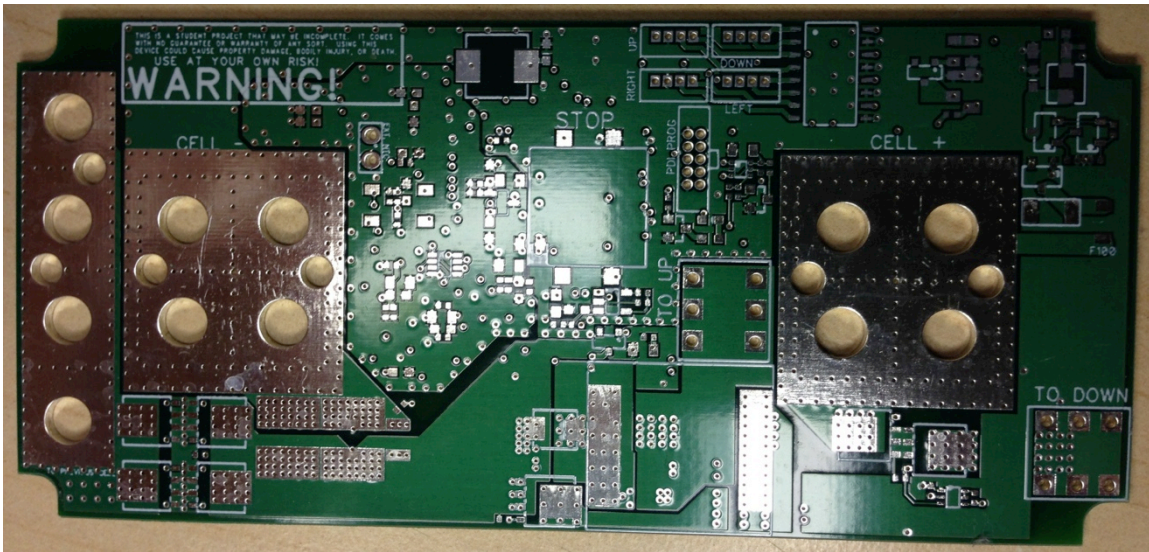


Figure 5.21 – Picture of a blank revision C PCB topside

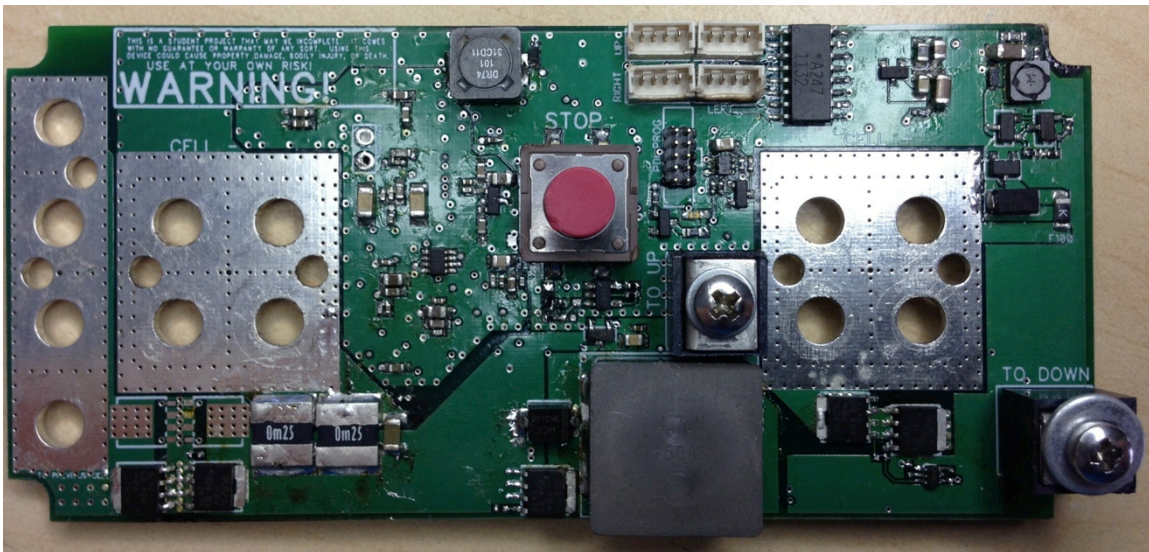


Figure 5.22 – Picture of nearly fully populated revision C PCB topside.

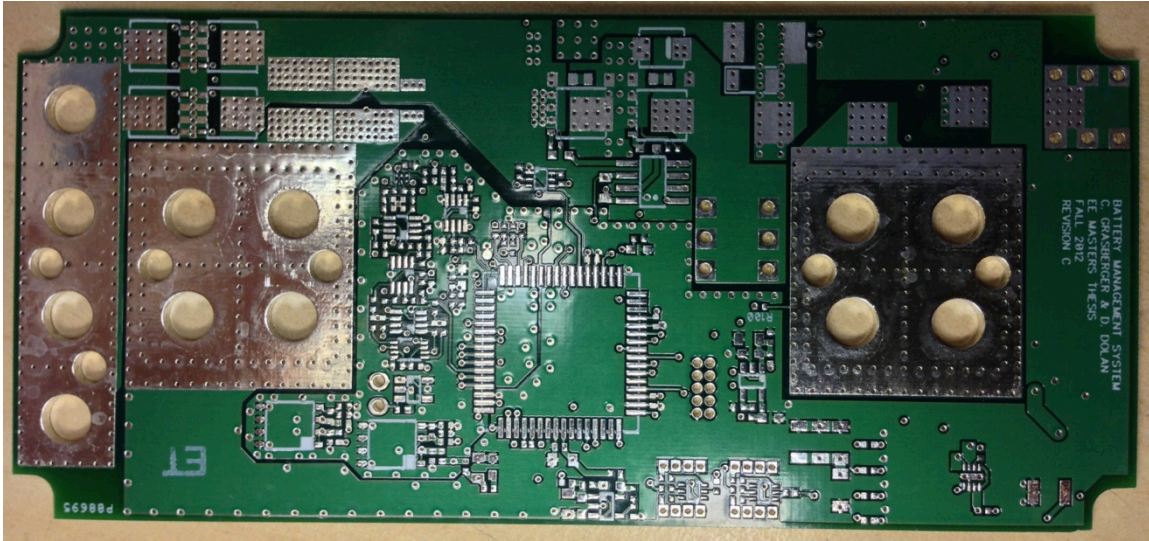


Figure 5.23 – Picture of a blank revision C PCB bottom side.

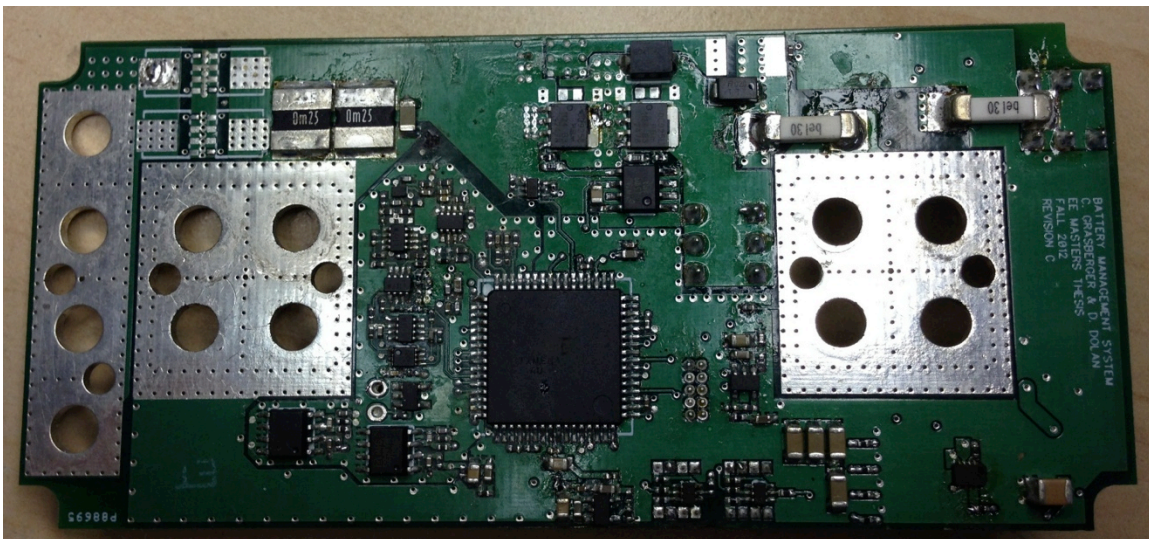


Figure 5.24 – Picture of a nearly fully populated revision C PCB bottom side.

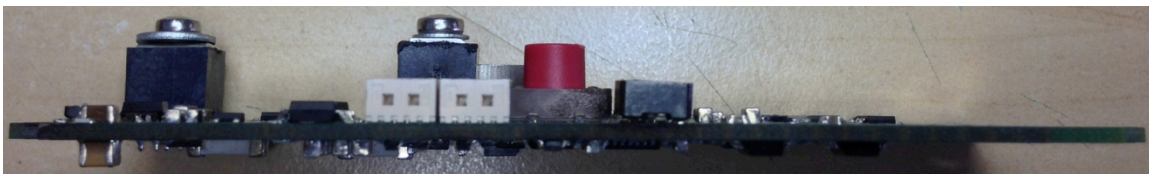


Figure 5.25 – Picture of a nearly fully populated revision C PCB edge view showing component height.

D. Bill of Materials (Revision C)

Table 5.2 – Revision C Bill of Materials

Parts that are marked do not populate (DNP) are not listed

RefDes	Value	Qty	Many	Manu #	Digikey
R680, R685	470k NTC	2	Panasonic	ERT-J0EV474J	P11446CT-ND
R100, R106, R300, R301, R330, R331, R360, R362, R400, R430, R431, R450, R453, R751	0	14	Stackpole	RMCF0402ZTOR00	RMCF0402ZTOR00CT-ND
R402	5	1	Yageo	RC0402JR-075R1L	311-5.1JRCT-ND
R802, R822, R842, R862	25.6	4	Stackpole	RMCF0402FT25R5	RMCF0402FT25R5CT-ND
R800, R820, R840, R860	39	4	Yageo	RC0402JR-0739RL	311-39JRCT-ND
R801, R821, R841, R861	110	4	Stackpole	RMCF0402FT110R	RMCF0402FT110RCT-ND
R640, R662, R663, R681, R686, R700, R758, R759, R760, R900, R901	470	11	Yageo	RC0402JR-07470RL	311-470JRCT-ND
R704, R705, R710, R711	3k 1%	4	Stackpole	RMCF0402FT3K00	RMCF0402FT3K00CT-ND
R207, R208	10k 0.1%	2	TE	7-1879208-3	A102579CT-ND
R102, R661, R701	10k 1%	3	Yageo	RC0402FR-0710KL	311-10.0KLRCT-ND
R706, R709	12k 1%	2	Yageo	RC0402FR-0712KL	311-12.0KLRCT-ND
R702, R703, R707	15k 1%	3	Yageo	RC0402FR-0715KL	311-15.0KLRCT-ND
R755	23.2k 1%	1	Panasonic	ERJ-2RKF2322X	P23.2KLCT-ND
R200, R201	30k 0.1%	2	TE	8-1879208-4	A102785CT-ND
R303, R333, R433, R452	30k 1%	4	Yageo	RC0402FR-0730KL	311-30.0KLRCT-ND
R432, R451	36.5k 1%	2	Susumu	RR0510P-3652-D	RR05P36.5KDCT-ND
R750, R752, R753, R754	43k 1%	4	Panasonic	ERJ-2RKF4302X	P43.0KLCT-ND
R922	52.3k 1%	1	Panasonic	ERJ-2RKF5232X	P52.3KLCT-ND
R103, R620, R682, R687	100k	4	Yageo	RC0402FR-07100KL	311-100KLRCT-ND
R708	105k 1%	1	Stackpole	RMCF0402FT105K	RMCF0402FT105KCT-ND
R302, R332	137k 1%	2	Panasonic	ERJ-2RKF1373X	P137KLCT-ND
R104, R250, R251, R252, R660, R664, R756, R757, R926, R928, R990, R991, R992, R920, R921, R924	470k 1%	16	Stackpole	RMCF0402FT470K	RMCF0402FT470KCT-ND
R361	1.5M 1%	1	Vishay	CRCW04021M50FKED	541-1.50MLCT-ND
R105	0.5	1	Stackpole	CSR0603FKR500	CSR0603FKR500CT-ND
R902, R903	11	2	Panasonic	ERJ-3GEYJ110V	P11GCT-ND
R641	51	1	Yageo	RC0603JR-0751RL	311-51JRCT-ND
R925, R927	30	2	Yageo	RC0805JR-0730RL	311-30ARCT-ND
R665	0.1	1	Bourms	CRA2512-FZ-R100ELF	CRA2512-FZ-R100ELFCT-ND
R1, R2, R3, R202	250u	4	Stackpole	CSS2725FTL250	CSS2725FTL250CT-ND
C204, C510, C602	1p - 50V	3	Murata	GRM1555C1H1R0CA01D	490-3199-1-ND
C413, C511, C603, C701, C702, C703, C707, C750, C758, C760, C784	100p - 50V	11	Yageo	CC0402JRNPO9BN101	311-1024-1-ND
C432, C452	470p - 50V	2	TDK	C1005C0G1H471J	445-2656-1-ND
C300, C330, C412, C431, C451, C512, C601, C621, C680, C685, C700, C704, C708, C751, C754, C757, C767, C768, C785, C900, C921	0.01u - 50V	21	Murata	GRM155R71H103KA88D	490-4516-1-ND
C502, C503, C504, C505, C507	0.1u - 25V	5	Taiyo	TMK105BJ104KV-F	587-1456-1-ND
C301, C303, C331, C333, C411, C418, C430, C450, C513, C600, C620, C705, C709, C762, C786, C920	1u - 10V	16	Murata	GRM188R61A105MA61D	490-1544-1-ND
C433, C453	2.2u - 10V	2	Taiyo	LMK107BJ225KA-T	587-1253-1-ND
C401	4.7u - 6.3V	1	Taiyo	JMK107BJ475KA-T	587-1785-1-ND
C926, C927	0.027u - 50V	2	Yageo	CC0805KRX7R9BB273	311-1139-1-ND
C360, C400, C901, C902	1u - 25V	4	Yageo	CC0805KKX7R8BB105	311-1456-1-ND
C302, C332, C361, C410, C501, C514, C660, C706, C763	10u - 10V	9	Yageo	CC0805KKX5R6BB106	311-1460-1-ND
C100, C362	10u - 25V	2	Taiyo	TMK316BJ106ML-T	587-2259-1-ND
C755, C756, C800, C801, C802, C803	47u - 10V	6	Murata	GRM31CR61A476ME15L	490-5528-1-ND
C202, C203	4.7u - 50V	2	Taiyo	UMK316ABJ475KD-T	587-2988-1-ND
C101	47u - 16V	1	Murata	GRM32ER61C476ME15L	490-3888-1-ND
D100, D923		2	Bourms	SMAJ8.5CA	SMAJ8.5CABCT-ND
D101, D400, D920		3	Comchip	CDSU101A	641-1002-1-ND
D360, D900		2	Fairchild	BAT54	BAT54FSCT-ND
D500		1	Comchip	CPDU5V0U-HF	641-1303-1-ND
D640		1	OSRAM	LG L29K-G2J1-24-Z	475-2709-1-ND
D921, D922		2	Micro	SK310B-TP	SK310B-TPCT-ND
F100		1	Bourms	SF-1206F080-2	SF-1206F080-2CT-ND
F920, F990		2	Bel Fuse	SMM 30	507-1524-1-ND
J500		1	Sullins	GRPB052VWVN-RC	S9015E-05-ND
J920, J990		2	Molex	760010106	WM4669-ND
J800, J820, J840, J860		4	Molex	53047-0410	WM1733-ND
Housings J800, J820, J840, J860		4	Molex	51021-0400	WM1722-ND
Terminal Pins J800, J820, J840, J860		8	Molex	50058-8000	WM1775CT-ND
L101	10u - 0.82A	1	Abracon	ASPI-0418S-100M-T3	ASPI-0418S-100M-T3CT-ND

L360	10u - 150mA	1	TDK	MLZ2012M100W	445-6396-1-ND
L400	100u	1	Cooper	DR74-101-R	513-1225-1-ND
L920	4.7uH - 25A	1	Vishay	IHLP6767GZER4R7M01	541-1255-1-ND
Q100, Q101, Q102		3	Alpha	AO3415A	785-1193-1-ND
Q250, Q251, Q252, Q253, Q254, Q255, Q256, Q257, Q661, Q920, Q921, Q990, Q991		13	NXP	PSMN0R9-25YLC,115	568-6720-1-ND
Q258, Q992		2	Vishay	SI1563EDH-T1-E3	SI1563EDH-T1-E3CT-ND
Q640, Q660		2	IR	IRLML6346TRPBF	IRLML6346TRPBFCT-ND
Q800, Q850		2	Vishay	SI1905DL-T1-E3	SI1905DL-T1-E3CT-ND
SW500		1	E-Switch	TL3300CF260Q	EG4905CT-ND
U300, U330		2	Microchip	MCP1824T-ADJE/OT	MCP1824T-ADJE/OTCT-ND
U360		1	Linear	LT3494EDDB#TRMPBF	LT3494EDDB#TRMPBFCT-ND
U410		1	TI	REF3020AIDBZR	296-26321-1-ND
U430, U450		2	Micrel	MIC5209YM	576-1278-ND
U500		1	Atmel	ATXMEGA128A3-AU	ATXMEGA128A3-AU-ND
U600		1	STM	TSV6392ILT	497-11450-1-ND
U620, U920		2	Microchip	MCP6L01RT-E/OT	MCP6L01RT-E/OTCT-ND
U660		1	Fairchild	NC7SZ58P6X	NC7SZ58P6XCT-ND
U700, U730, U750, U770		4	Linear	LTC6256CTS8#TRMPBF	LTC6256CTS8#TRMPBFCT-ND
U701		1	NXP	NX3L1T66GM,115	568-5548-1-ND
U751		1	TI	SN74LVC2G66DCUR	296-13272-1-ND
U800		1	Avago	ACPL-247-500E	516-2466-1-ND
U900		1	National	LM5109AMA/NOPB	LM5109AMA-ND

E. Sub System Raw Data

E.1 Current Sense Amplifier

Table 5.3 – DC response from ± 800 and ± 120 A current ranges.

Sense Resistor Voltage [mV]	Divider Output [mV]	800A Range [V]	120A Range [V]
100.61	75.54	0.00810	0.00648
91.31	68.44	0.03477	0.00674
81.06	60.80	0.15740	0.00612
59.86	44.831	0.41118	0.00661
38.625	28.947	0.6645	0.00661
20.784	15.633	0.8773	0.00661
15.446	11.600	0.9412	0.00666
12.166	9.114	0.9802	0.00663
10.836	8.136	0.9962	0.05620
9.718	7.307	1.0095	0.16153
8.998	6.815	1.0179	0.22923
8.067	6.146	1.0286	0.31402
7.107	5.389	1.0401	0.40514
6.156	4.679	1.0513	0.49751
4.975	3.771	1.0659	0.6111
4.042	3.103	1.0770	0.6992
3.086	2.374	1.0880	0.7861
2.002	1.575	1.1008	0.8883
0.000	-0.150	1.1240	1.0729
-2.186	-1.544	1.1511	1.2872
-3.043	-2.229	1.1612	1.3671
-3.829	-2.770	1.1702	1.4387
-5.313	-3.880	1.1880	1.5808
-6.117	-4.529	1.1978	1.6583
-7.062	-5.219	1.2088	1.7465
-7.955	-5.881	1.2196	1.8320
-8.993	-6.590	1.2321	1.9322
-10.250	-7.605	1.2472	2.0525
-11.030	-8.190	1.2565	2.1259
-12.202	-9.071	1.2705	2.2375
-15.122	-11.250	1.3055	2.2423
-20.363	-15.178	1.3678	2.2422
-40.380	-30.175	1.6068	2.2422
-60.00	-44.867	1.8414	2.2422
-80.20	-60.00	2.0824	2.2422
-95.06	-71.12	2.2370	2.2421
-99.60	-74.54	2.2362	2.2420
Shorted Analog Switch	0	1.1269	1.0958

Table 5.4 – Random samples from $\pm 120A$ current range after calibration. All units are in amps.

Expected Current [A]	-100	-80	-60	-40	-20	0	20	40	60	80	100
Samples [A]	-99.1468	-79.3591	-60.0286	-40.1045	-18.8964	0.5879	20.2438	40.1547	60.0743	79.9720	99.7554
	-99.4239	-79.9219	-60.1649	-39.9770	-19.6880	-0.0145	19.9360	40.0447	60.3250	79.6598	99.6851
	-99.5294	-79.9175	-60.0946	-40.0650	-20.0221	-0.0057	20.1426	40.3305	60.2195	79.8489	99.5971
	-99.4063	-79.9219	-59.9539	-40.1529	-19.6704	-0.0233	20.2306	40.1854	60.1271	79.8137	99.3201
	-99.3271	-79.7504	-59.7560	-39.9023	-20.0265	-0.0145	20.1382	40.1151	60.1843	79.6642	99.3597
	-99.4239	-79.7944	-60.0858	-40.0518	-19.9254	0.0998	20.1294	40.3833	59.7402	79.8797	99.3597
	-99.2172	-79.8691	-59.7076	-39.9286	-19.8375	0.0690	20.1250	40.0931	60.1535	79.7390	99.5487
	-99.1776	-79.3195	-60.0638	-39.9946	-19.7363	0.1570	20.2218	40.0095	60.0348	79.4839	99.1574
	-99.0149	-79.5965	-59.9451	-39.8935	-19.9166	0.1922	20.0635	40.3349	60.1447	79.7126	99.0694
	-99.1336	-79.4998	-59.9363	-40.0474	-19.7935	1.7576	20.1646	40.0975	60.2502	79.5763	99.0826
	-98.7511	-79.5350	-59.9231	-39.9814	-19.9562	0.8562	20.2174	40.1634	60.1139	79.6159	99.0738
	-98.6323	-79.3855	-59.7120	-39.6956	-19.5560	0.2625	20.1910	40.1634	60.1711	79.5763	98.8803
Average [A]	-99.1820	-79.6559	-59.9476	-39.9829	-19.7521	0.3270	20.1503	40.1730	60.1282	79.7119	99.3241
STDEV [A]	0.2746	0.2336	0.1533	0.1204	0.3071	0.5249	0.0860	0.1185	0.1447	0.1442	0.2787
Max [A]	-98.6323	-79.3195	-59.7076	-39.6956	-18.8964	1.7576	20.2438	40.3833	60.3250	79.9720	99.7554
MIN [A]	-99.5294	-79.9219	-60.1649	-40.1529	-20.0265	-0.0233	19.9360	40.0095	59.7402	79.4839	98.8803
Range [A]	0.8970	0.6024	0.4573	0.4573	1.1301	1.7809	0.3078	0.3738	0.5848	0.4881	0.8751

E.2 Power Measurements

Table 5.5 – Frequency response of input power filter.

Frequency [kHz]	Gain [dB]
0.01	-0.08
0.1	-0.08
1	-0.17
2	-0.71
5	-2.85
8	-4.08
9	-4.08
10	-4.41
11	-4.75
12	-5.11
13	-5.48
14	-5.70
15	-6.02
16	-6.23
17	-6.44
18	-6.61
19	-6.80
20	-7.15
30	-8.91
40	-10.25
50	-11.40

Table 5.6 – Frequency response of analog circuit power filter.

Frequency [kHz]	V _{in} [mV _{pp}]	V _{out} [mV _{pp}]	Gain [dB]
0.01	882	882	0.00
0.1	978	976	-0.02
0.2	952	952	0.00
0.5	944	944	0.00
1	980	952	-0.25
2	880	1030	1.37
3	880	1140	2.25
4	890	1370	3.75
5	912	1820	6.00
6	840	2440	9.26
7	840	2320	8.82
8	784	1700	6.72
9	840	1170	2.88
10	888	864	-0.24
11	880	680	-2.24
12	936	560	-4.46
15	920	416	-6.89
20	1050	184	-15.13
50	1040	40	-28.30

Table 5.7 – Boost voltage and current measurements.

V _{in}	I _n [mA]	V _o	I _o [mA]	P _{in} [mW]	P _o [mW]	Eff [%]
3.3112	333.0E-3	11.403	0.00	1.1	0.0	0.0%
3.1112	334.0E-3	11.401	0.01	1.0	0.1	12.6%
3.3111	380.0E-3	11.326	0.02	1.3	0.3	22.0%
3.3111	744.0E-3	11.309	0.10	2.5	1.1	43.7%
3.3106	2.7E+0	11.294	0.52	9.0	5.9	65.8%
3.3089	9.8E+0	11.283	2.05	32.5	23.1	71.0%
3.0050	25.2E+0	11.274	5.24	75.8	59.1	78.0%
3.3000	47.4E+0	11.267	9.56	156.6	107.7	68.8%
3.2925	87.9E+0	11.253	16.75	289.4	188.5	65.1%
3.2728	193.0E+0	11.171	33.15	631.7	370.3	58.6%
3.2573	235.6E+0	9.25	52.50	767.4	485.6	63.3%
3.2523	253.2E+0	7.65	64.50	823.5	493.4	59.9%
3.2423	166.8E+0	4.45	95.63	540.8	425.6	78.7%

Table 5.8 – Boost voltage measurements for line regulation calculation.

V _{in} [V]	V _{out} [V]
2.5015	10.420
4.1521	11.234

E.3 DC/DC Converter Measurements

Table 5.9 – Measurements from Revision C Balancing DC/DC converter.

Set Duty Cycle [%]	Lower Cell Voltage [V]	Upper Cell Voltage [V]	Duty From Current [%]	Upper Cell Current [A]	Lower Cell Current [A]	Upper Cell Power [W]	Lower Cell Power [W]	Switching Only Efficiency [%]	Entire Converter Efficiency [%]
25.0	3.3410	3.3328	40.7	-8.64	12.76	-28.86	42.52	67.9%	67.61%
27.5	3.3401	3.3340	41.7	-7.17	10.18	-23.94	33.94	70.5%	70.21%
30.0	3.3392	3.3352	41.7	-6.06	8.55	-20.24	28.53	71.0%	70.56%
32.5	3.3387	3.3359	42.9	-5.24	7.07	-17.50	23.60	74.2%	73.65%
35.0	3.3382	3.3365	44.1	-4.36	5.62	-14.56	18.74	77.7%	77.04%
37.5	3.3380	3.3369	45.1	-2.79	3.45	-9.31	11.52	80.8%	79.72%
40.0	3.3378	3.3372	46.1	-1.07	1.32	-3.57	4.40	81.2%	78.34%
42.5	3.3378	3.3372	46.5	-0.73	0.87	-2.43	2.89	83.9%	79.47%
45.0	3.3378	3.3372	46.7	-0.72	0.85	-2.39	2.82	84.7%	80.13%
47.5	3.3384	3.3368	46.9	-0.68	0.80	-2.28	2.68	85.3%	80.45%
50.0	3.3406	3.3333	48.7	0.05	0.01	0.16	0.04	24.1%	12.07%
52.5	3.3403	3.3337	50.3	0.19	-0.15	0.63	-0.50	79.6%	63.46%
55.0	3.3399	3.3340	50.5	0.47	-0.39	1.56	-1.29	82.6%	74.88%
57.5	3.3398	3.3342	51.1	0.47	-0.37	1.57	-1.24	78.9%	71.59%
60.0	3.3397	3.3343	52.5	0.79	-0.63	2.62	-2.11	80.3%	75.72%
62.5	3.3397	3.3343	54.9	2.96	-2.33	9.88	-7.77	78.6%	77.38%
65.0	3.3397	3.3342	54.9	4.81	-3.71	16.06	-12.36	77.0%	76.20%
67.5	3.3384	3.3351	54.9	6.28	-4.78	20.95	-15.93	76.0%	75.46%
70.0	3.3370	3.3360	56.9	7.79	-5.56	26.00	-18.54	71.3%	70.90%
72.5	3.3353	3.3368	59.7	10.28	-6.54	34.29	-21.84	63.7%	63.39%
75.0	3.3335	3.3376	61.9	13.49	-7.82	44.96	-26.11	58.1%	57.87%

F. Communication

F.1 External Commands (User Interface)

Table 5.10 – Table of basic commands to control the BMS

Parameters inside of [] are required. Parameters inside < > are optional. is used to separate each of the optional or required parameters. Commands are case-insensitive, but capitalization was used for clarity in this list.	
STOP	Performs an emergency stop
HELP	Lists all of the root commands. Ex: ADC, PIN, ...
ADC <help>	Provides detailed help on sub commands for ADC
ADC ALL <raw>	Measures all ADCs channels and displays the value. Raw will display value in ADC counts.
ADC [cur800 cur120 cou800 cou120 vbatt temperature] <raw>	Measures specific ADC channel. Raw will display value in ADC counts.
ADC CALIBRATE FACTORY [#password]	This saves calibration data to reserved part of the EEPROM so that they can over write user calibrations with defaults if required.
ADC [cur800 cur120 cou800 cou120 vbatt temperature] SETTINGS <offset gain calibrate> <#value>	View and change settings for specific channels
PIN <help>	Provides detailed help on sub commands for PIN
PIN [led dcdc dcdc_down batt_ext reset_coulomb current_cal] <dir out in> <#value toggle>	Configures select GPIO's as inputs or outputs, gets the current IO state, or sets the output state.
PIN [power_pulse DCDC_lower DCDC_upper] <dir out in> <#value #password toggle #password>	Configures special GPIO's that can cause damage if improperly used. Requires a password.
REG <help>	Provides detailed help on sub commands for REG
REG [#address] <bin dec hex>	Reads MCU's register. Can be displayed as binary, decimal, or hexadecimal.
REG [#address] <#value>	Write MCU register with second parameter
REG [#address] [or and] <#value>	Write MCU register by ANDing or ORing it with second parameter.
CURRENT	Displays instantaneous current through sense resistors. Will automatically adjust current range based on magnitude of measurements.
CURRENT HELP	Provides detailed help on sub commands for CURRENT
DCDC <help>	Provides detailed help on sub commands for DCDC
DCDC [down auto] <#value>	Enables down switch or enables auto-mode. Auto-mode is incomplete. Down switch is to enable another board's DC/DC converter to transfer charge to this board.
DCDC PWM <enable frequency duty deadtime> <#value>	Enable the PWM to run, set the frequency, set the duty cycle, or change the dead time.
DCDC PWM <up down>	Up and down increment the duty cycle by 2.5% to prevent errors from typos
DCDC <voltage ovp >	Gets voltage from adjacent cells or checks the state of the OVP circuit.
DCDC TEST [run stop]	Runs or stops the auto-mode. Auto-mode is incomplete.
COMMS [ping] <all left right up down>	This will ping all of the directions or individual directions. If there is a response, it will report it, otherwise it will time out.
COMMS DISPLAY [in out] <#value>	This shows debug information about commands being sent and received. These are suppressed normally so that the command line interface does not scroll too fast.
EEPROM <help>	Provides detailed help on sub commands for EEPROM
EEPROM CURRENT	Displays which memory sector is being read from currently
EEPROM DEFAULT	Loads the default settings into all of the current variables. This does not write them to the EEPROM.
EEPROM WRITE	Writes current variables to the next memory sector.
EEPROM READ <0 1 >	Read memory sectors. A specific sector can be selected
EEPROM ERASE [0 1 all]	Erases specific memory sectors. A specific sector or both.
EEPROM ERASE FACTORY [#password]	Erases the reserved section in the EEPROM for calibration data.

F.2 Internal Commands

Character/Byte	Description
{	Start character. This starts all internal messages.
}	Stop Character. This ends all internal messages.
v	Request battery voltage
V	Responding with battery voltage
d	Request that the DC/DC converter down connection switch is enabled. The cell of lower potential controls the PWM switches, however the higher one can refuse to enable the down switch to protect itself
D	Responding that the DC/DC converter down connection switch was enabled
E	Responding that the DC/DC convert switch was NOT enabled.
e	Placeholder. Not used.
255	Emergency broadcast. This will trigger whatever the safety protocol is configured to be.
%	Switch from internal communication to external communication. This does not require the start and stop characters.
?	Error message. This if the message is not recognized. This may be an unsupported message or a poorly formatted one.

G. Revision B

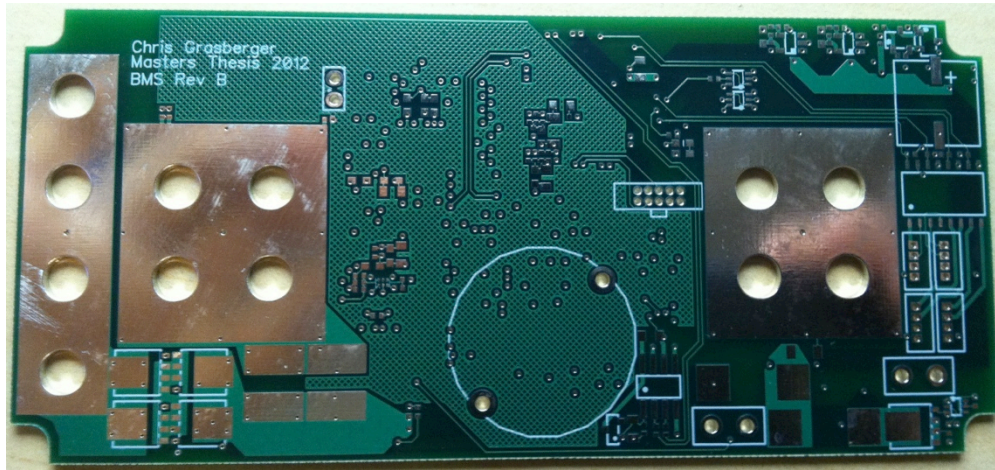


Figure 5.26 – Picture of blank Revision B PCB top side.

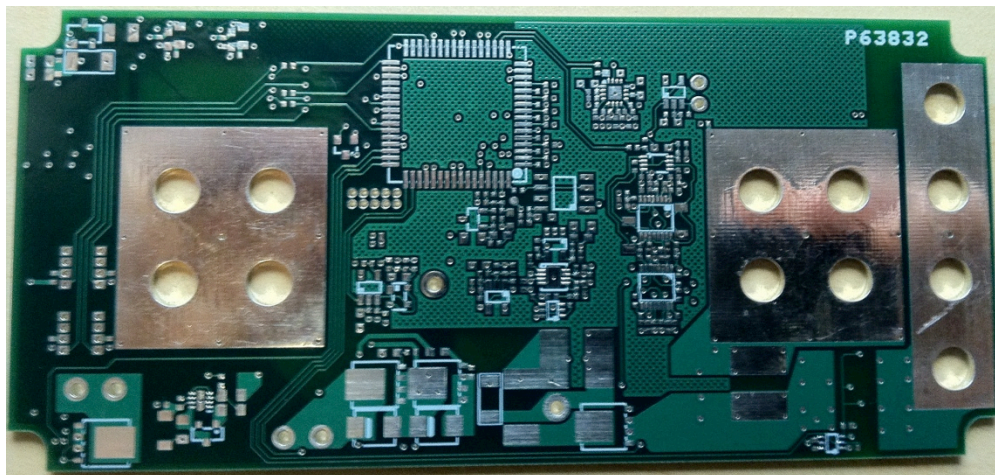


Figure 5.27 – Picture of blank Revision B PCB bottom side.

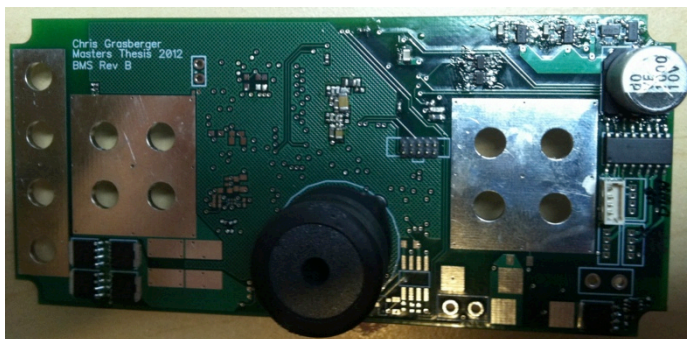


Figure 5.28 – Picture of Revision B PCB top side nearly fully populated.

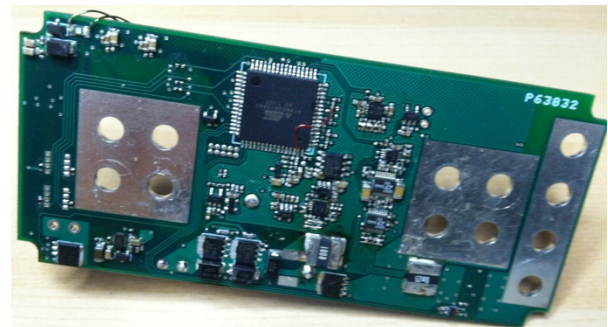
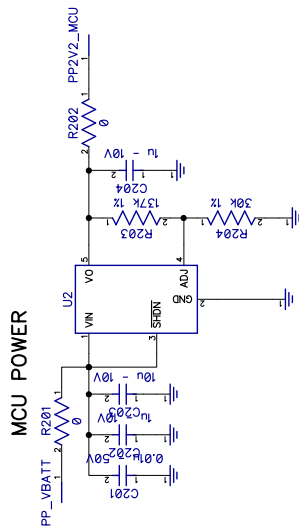


Figure 5.29 – Picture of Revision B PCB bottom side nearly fully populated.

DIGITAL VOLTAGE REGULATION

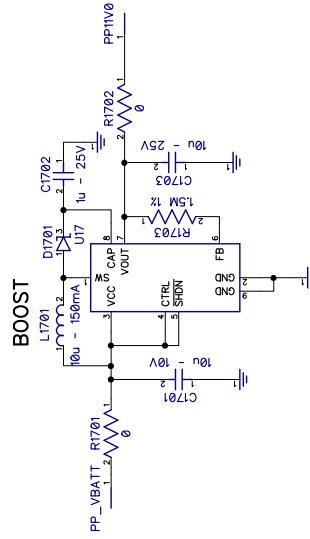
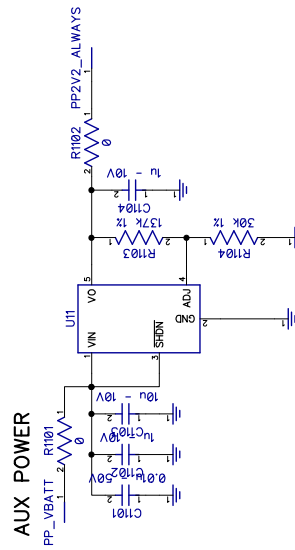


$$V_o = 2.282V = (.41) * (137k + 30k) / 30k$$

$$V_{o_min} = 2.238V$$

$$V_{o_max} = 2.327V$$

$$I_{o_max} = 300mA$$



$$V_o = 11.32V = (1.225V) * (1.5M / 182k + 1)$$

$$V_{o_min} = 11.03V$$

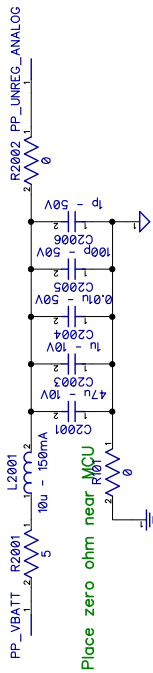
$$V_{o_max} = 11.68V$$

$$I_{o_max} = 180mA$$

Figure 5.31 – Revision B Schematic – Page 2 – Digital Voltage Regulation

ANALOG VOLTAGE REGULATION

DIGITAL-TO-ANALOG CONNECTION



$V_o = 2.25V = (0.5V)(105k/30k + 1)$
 $V_{o_min} = 2.205V$
 $V_{o_max} = 2.295V$
 $I_{o_max} = 200mA$ ea.

ADC REFERENCE

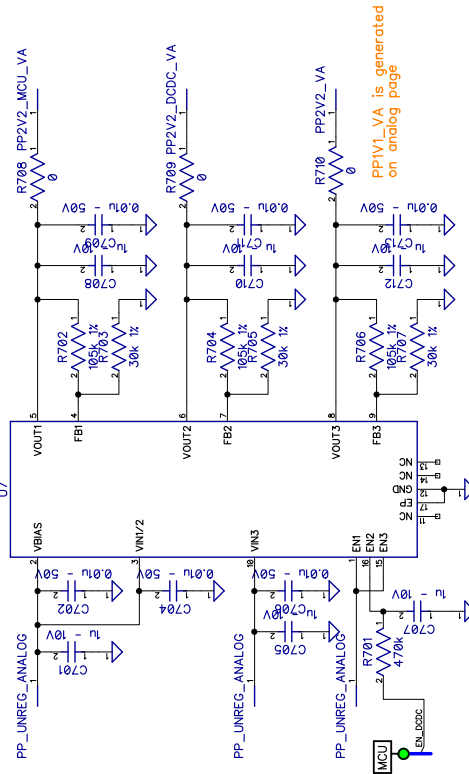
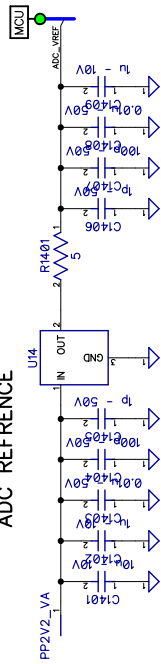
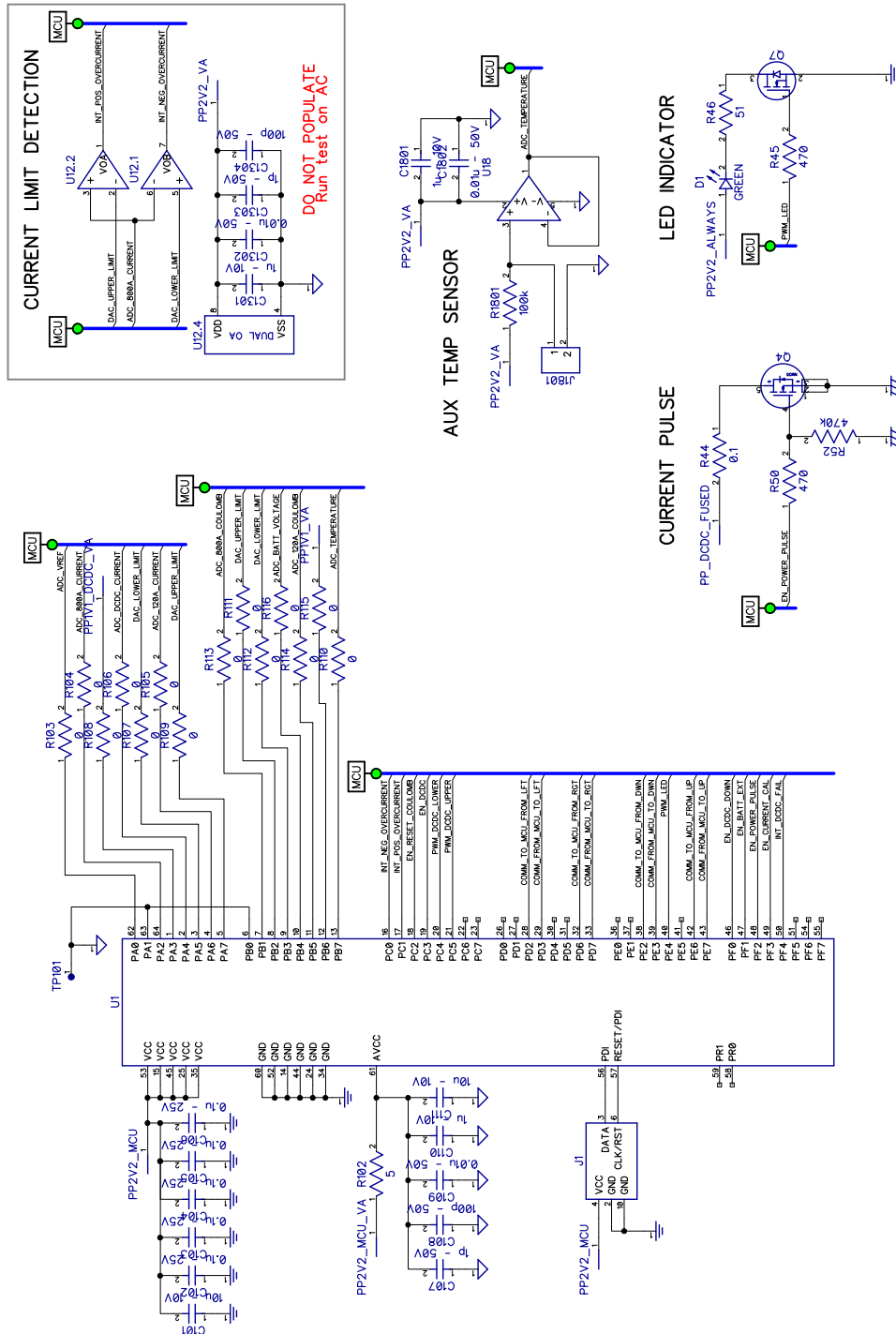


Figure 5.32 – Revision B Schematic – Page 3 – Analog Voltage Regulation

CONTROLLER



ANALOG MEASUREMENT

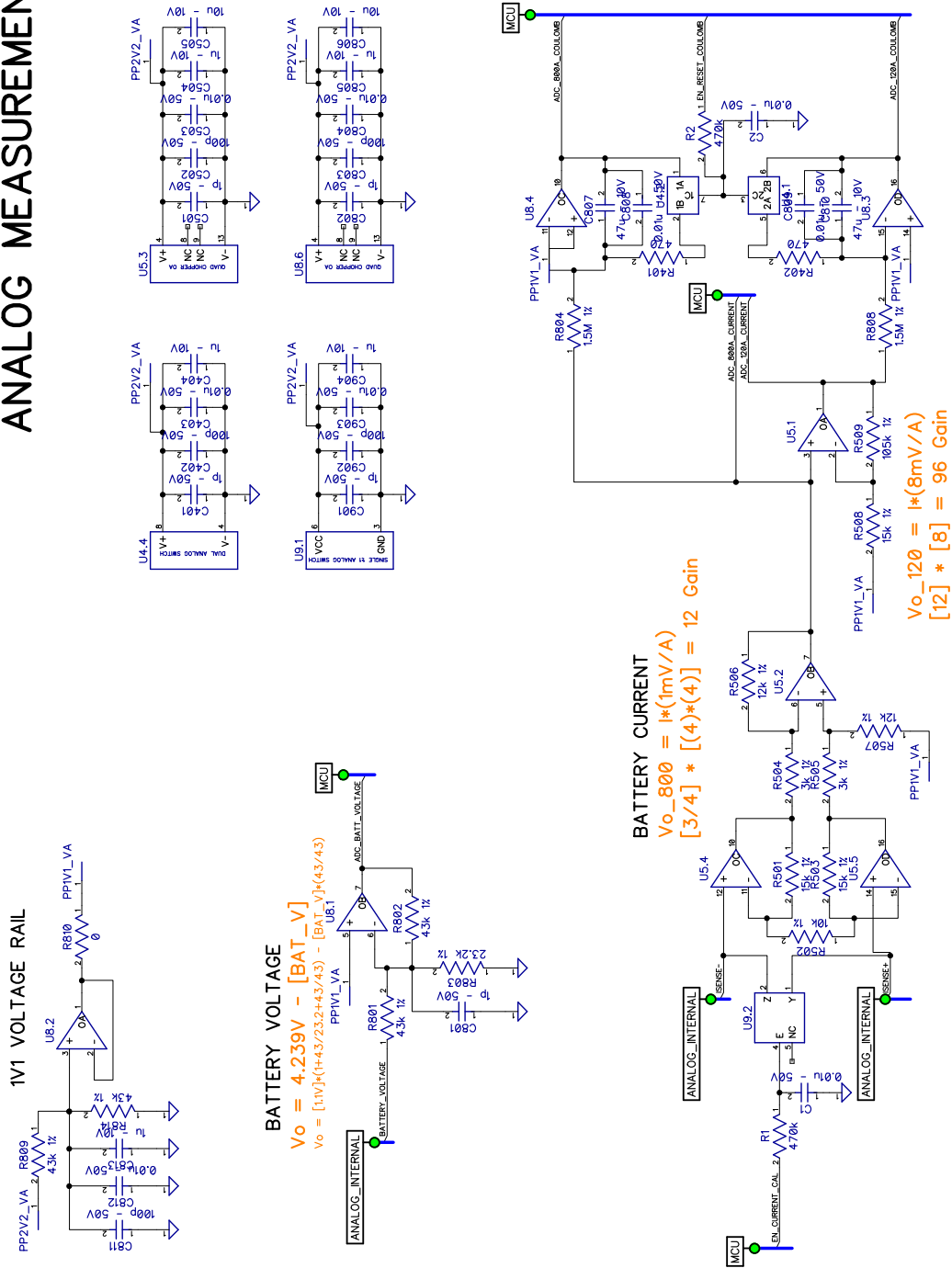


Figure 5.34 – Revision B Schematic – Page 5 – Analog Measurement

COMMUNICATION

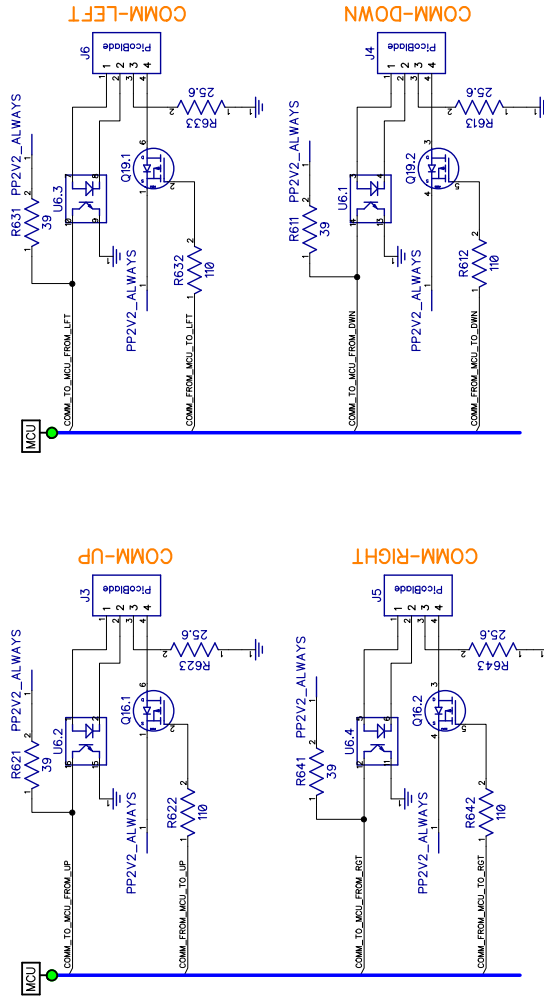
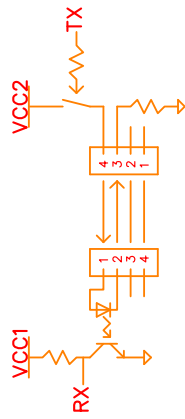
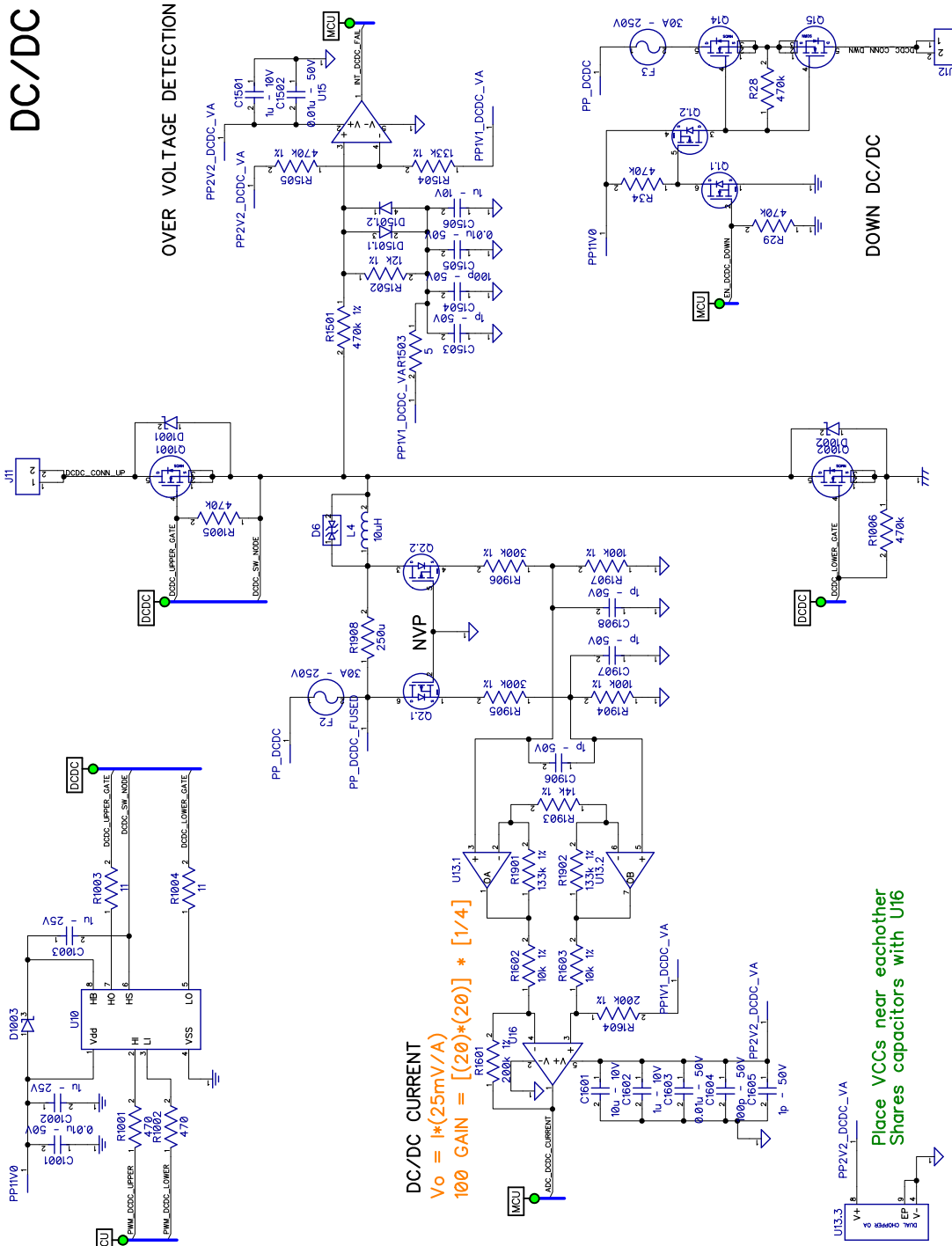


Figure 5.35 – Revision B Schematic – Page 6 – Communication



DC/DC

OVER VOLTAGE DETECTION

DOWN DC/DC

DC/DC CURRENT
 $V_o = I * (25mV/A)$
100 GAIN = [(20)*(20)] * [1/4]

Place VCCs near eachother
 Shares capacitors with U16

Figure 5.36 – Revision B Schematic – Page 7 – DC/DC

G.2 Bill of Materials

Table 5.11 – Revision B Bill of Materials

RefDes	Value	Qty	Manu	Manu PN	Digikey
R101, R103, R104, R105, R106, R107, R108, R109, R110, R111, R112, R113, R114, R115, R116, R201, R202, R302, R708, R709, R710, R810, R1101, R1102, R1701, R1702, R2002, R2204, R2205, R2301, R2302, R2303, R2304	0	33	Stackpole	RMCF0402ZT0R00CT	RMCF0402ZT0R00CT-ND
R102, R1401, R1503, R2001	5	4	Yageo	RC0402JR-075R1L	311-5.1JRCT-ND
R613, R623, R633, R643	25.6	4	Stackpole	RMCF0402FT25R5	RMCF0402FT25R5CT-ND
R611, R621, R631, R641	39	4	Yageo	RC0402JR-0739RL	311-39JRCT-ND
R612, R622, R632, R642	110	4	Stackpole	RMCF0402FT110R	RMCF0402FT110RCT-ND
R45, R50, R401, R402, R1001, R1002	470	6	Yageo	RC0402JR-07470RL	311-470JRCT-ND
R504, R505	3k 1%	2	Stackpole	RMCF0402FT3K00	RMCF0402FT3K00CT-ND
R502, R1602, R1603	10k 1%	3	Yageo	RC0402FR-0710KL	311-10.0KLRCT-ND
R506, R507, R1502, R2201	12k 1%	4	Yageo	RC0402FR-0712KL	311-12.0KLRCT-ND
R1903	14k 1%	1	Yageo	RC0402FR-0714KL	311-14.0KLRCT-ND
R501, R503, R508	15k 1%	3	Yageo	RC0402FR-0715KL	311-15.0KLRCT-ND
R803	23.2k 1%	1	Panasonic	ERJ-2RKF2322X	P23.2KLCT-ND
R204, R703, R705, R707, R1104	30k 1%	5	Yageo	RC0402FR-0730KL	311-30.0KLRCT-ND
R801, R802, R809, R814	43k 1%	4	Panasonic	ERJ-2RKF4302X	P43.0KLCT-ND
R1508, R1509, R1904, R1907, R1801, R2202	100k 1%	6	Yageo	RC0402FR-07100KL	311-100KLRCT-ND
R509, R702, R704, R706	105k 1%	4	Stackpole	RMCF0402FT105K	RMCF0402FT105KCT-ND
R1504, R1901, R1902	133k 1%	3	Panasonic	ERJ-2RKF1333X	P133KLCT-ND
R203, R1103	137k 1%	2	Panasonic	ERJ-2RKF1373X	P137KLCT-ND
R1601, R1604	200k 1%	2	Yageo	RC0402FR-07200KL	311-200KLRCT-ND
R1506, R1507, R1905, R1906	300k 1%	4	Panasonic	ERJ-2RKF3003X	P300KLCT-ND
R301, R303, R1501, R1505, R2101, R1, R2, R28, R29, R34, R52, R701, R1005, R1006, R2102, R2103, R2203	470k 1%	17	Stackpole	RMCF0402FT470K	RMCF0402FT470KCT-ND
R804, R808, R1703	1.5M 1%	3	Vishay	CRCW04021M50FKED	541-1.50MLCT-ND
R1003, R1004	11	2	Panasonic	ERJ-3GEYJ110V	P11GCT-ND
R46	51	1	Yageo	RC0603JR-0751RL	311-51GRCT-ND
R2305	0	1	Stackpole	RMCF1206ZT0R00	RMCF1206ZT0R00CT-ND
R44	0.1	1	Bourns	CRA2512-FZ-R100ELF	CRA2512-FZ-R100ELFCT-ND
R1908, R2104, R2105, R2106	250u	4	Stackpole	CSS2725FTL250	CSS2725FTL250CT-ND
C107, C301, C401, C501, C801, C802, C901, C1303, C1405, C1406, C1503, C1508, C1510, C1605, C1906, C1907, C1908, C2006	1p - 50V	18	Murata	GRM1555C1H1R0CA01D	490-3199-1-ND
C108, C302, C306, C402, C502, C803, C811, C902, C1304, C1404, C1407, C1504, C1604, C2005	100p - 50V	14	Yageo	CC0402JRNPO9BN101	311-1024-1-ND
C1, C2, C109, C201, C304, C305, C403, C503, C702, C704, C706, C709, C711, C713, C804, C808, C809, C812, C903, C1001, C1101, C1302, C1403, C1408, C1502, C1505, C1603, C1802, C2004, C2204	0.01u - 50V	30	Murata	GRM155R71H103KA88D	490-4516-1-ND
C102, C103, C104, C105, C106	0.1u - 25V	5	Taiyo	TMK105BJ104KV-F	587-1456-1-ND
C110, C202, C204, C303, C404, C504, C701, C705, C707, C708, C710, C712, C805, C813, C904, C1102, C1104, C1301, C1402, C1409, C1501, C1506, C1602, C1801, C2003	1u - 10V	25	Murata	GRM188R61A105MA61D	490-1544-1-ND
C1002, C1003, C1702, C2203	1u - 25V	4	Yageo	CC0805KKX7R8BB105	311-1456-1-ND
C101, C111, C203, C505, C806, C1103, C1401, C1601, C1701, C2202	10u - 10V	10	Yageo	CC0805KKX5R6BB106	311-1460-1-ND
C1703	10u - 25V	1	Taiyo	TMK316BJ106ML-T	587-2259-1-ND
C807, C810, C2001	47u - 10V	3	Murata	GRM31CR61A476ME15L	490-5528-1-ND
C2201	1000u - 10V	1	CDE	AVE108M10G24T-F	338-1792-1-ND
D1		1	OSRAM	LG L29K-G2J1-24-Z	475-2709-1-ND
D2, D6		2	Bourns	SMAJ8.5CA	SMAJ8.5CABCT-ND
D1001, D1002		2	Micro	SK310B-TP	SK310B-TPCT-ND
D1003, D1701		2	Fairchild	BAT54	BAT54FSCT-ND
D1501		1	NXP	BAV23.215	568-1620-1-ND
F2, F3		2	Bel Fuse	SMM 30	507-1524-1-ND
F2201		1	Little Fuse	0466.125NR	F1450CT-ND
J1		1	Sullins	GRPB052VWVN-RC	S9015E-05-ND
J11, J12		2	TE	1586037-2	A30602-ND
J3, J4, J5, J6		4	Molex	53047-0410	WM1733-ND
L4	10uH	1	Abracon	AIRD-02-100K	535-11399-ND
L1701, L2001	10u - 150mA	2	TDK	MLZ2012M100W	445-6396-1-ND
Q1, Q22		2	Vishay	SII563EDH-T1-E3	SII563EDH-T1-E3CT-ND
Q2, Q16, Q19		3	Vishay	SII905DL-T1-E3	SII905DL-T1-E3CT-ND
Q4, Q14, Q15, Q1001, Q1002, Q2101, Q2102, Q2103, Q2104		9	NXP	PSMN0R9-25YLC.115	568-6720-1-ND

Q7		1	IR	IRLML6346TRPBF	IRLML6346TRPBFCT-ND
Q2201, Q2202, Q2203		3	Alpha	AO3415A	785-1193-1-ND
U1		1	Atmel	ATXMEGA128A3-AU	ATXMEGA128A3-AU-ND
U6		1	Avago	ACPL-247-500E	516-2466-1-ND
U7		1	Analog	ADP323ACPZ-R7	ADP323ACPZ-R7CT-ND
U10		1	National	LM5109AMA/NOPB	LM5109AMA-ND
U17		1	Linear	LT3494EDDB#TRMPBF	LT3494EDDB#TRMPBFCT-ND
U5, U8		2	Linear	LTC6257CMS#PBF	LTC6257CMS#PBF-ND
U2, U11		2	Microchip	MCP1824T-ADJE/OT	MCP1824T-ADJE/OTCT-ND
U12		1	Microchip	MCP6052-E/SN	MCP6052-E/SN-ND
U3, U15, U18		3	Microchip	MCP6L01RT-E/OT	MCP6L01RT-E/OTCT-ND
U9		1	NXP	NX3L1T66GM,115	568-5548-1-ND
U13		1	TI	OPA2320AIDRGT	296-28361-1-ND
U16		1	TI	OPA320AIDBVT	296-29510-1-ND
U14		1	TI	REF3020AIDBZR	296-26321-1-ND
U4		1	TI	SN74LVC2G66DCUR	296-13272-1-ND

H. Revision A

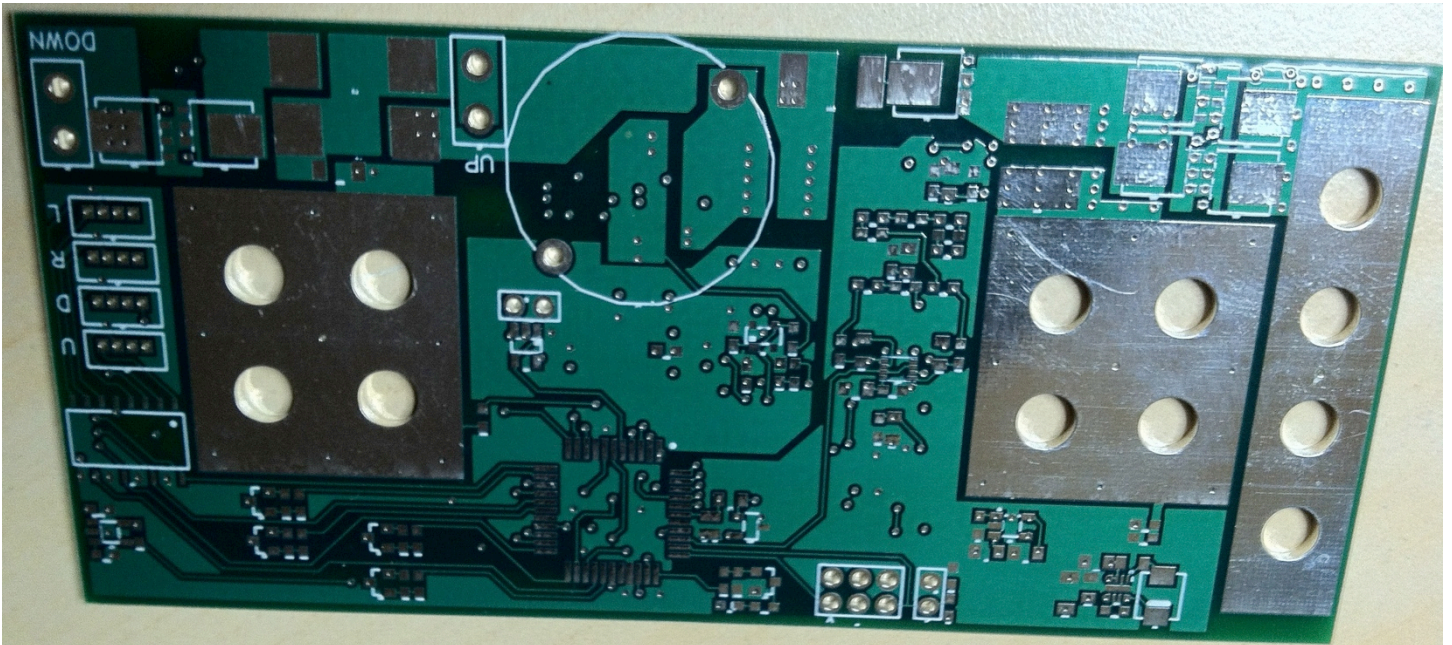


Figure 5.37 – Picture of blank Revision A PCB topside.

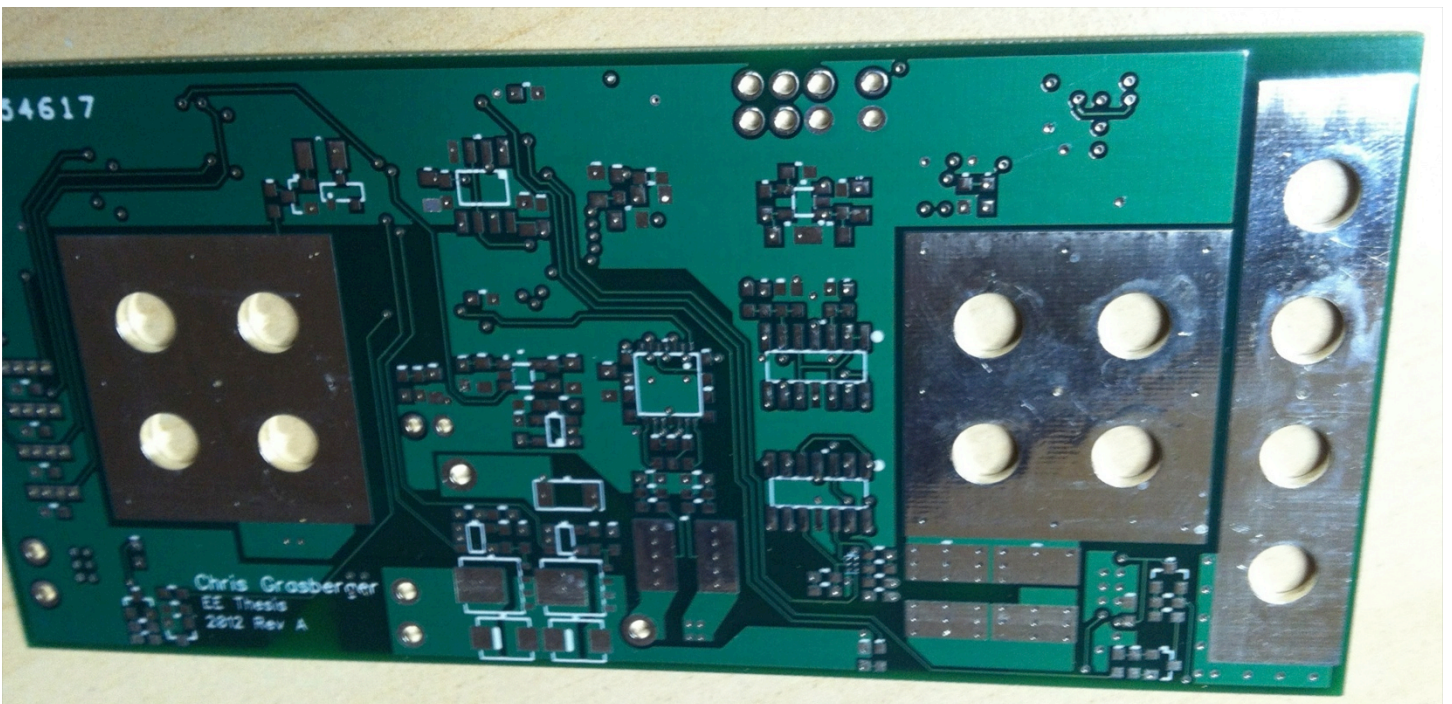


Figure 5.38 – Picture of blank Revision A PCB bottom side.

H.1 Schematic

POWER INPUT

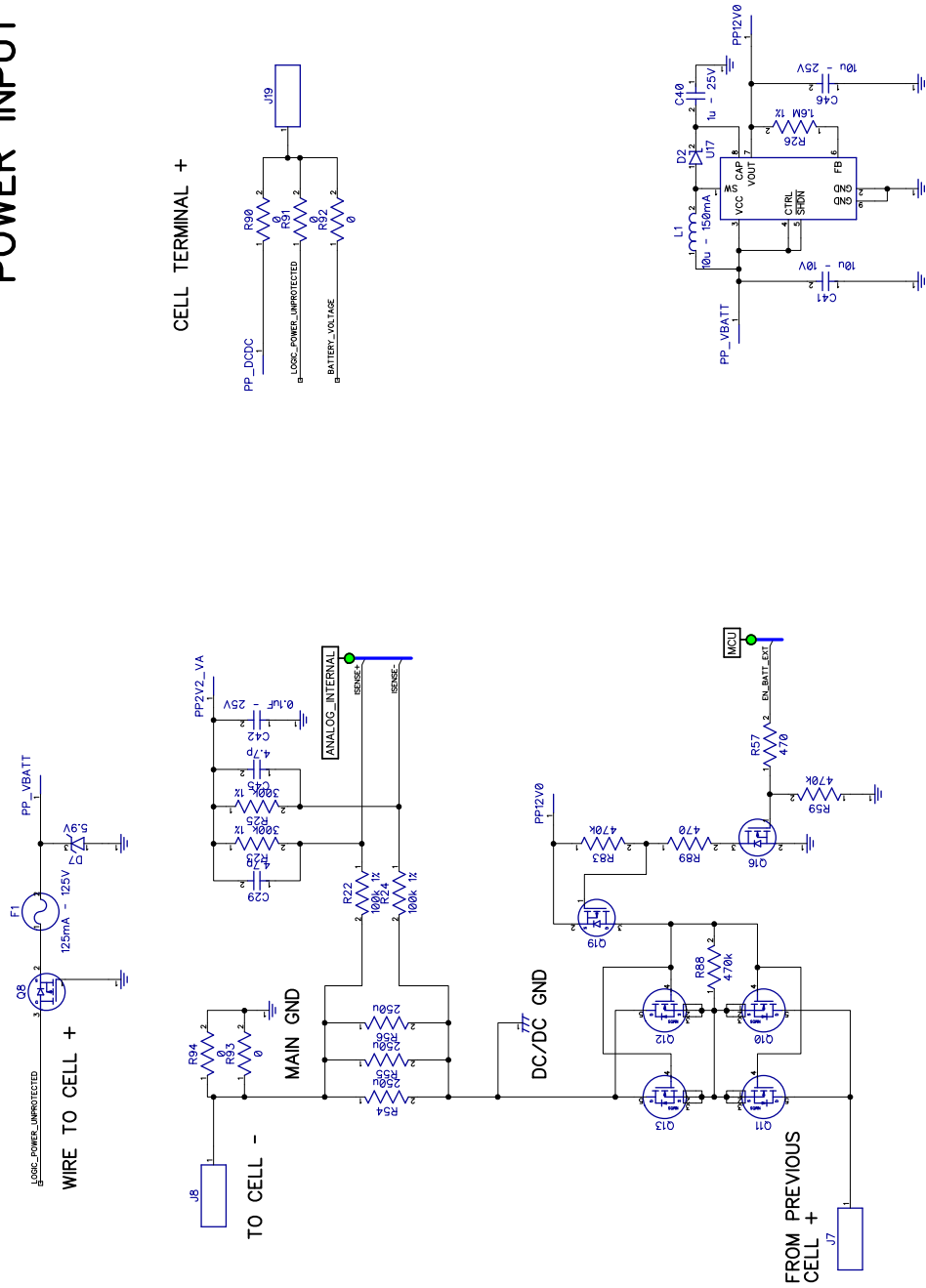


Figure 5.39 – Revision A Schematic – Page 1 – Power Input

CONTROLLER

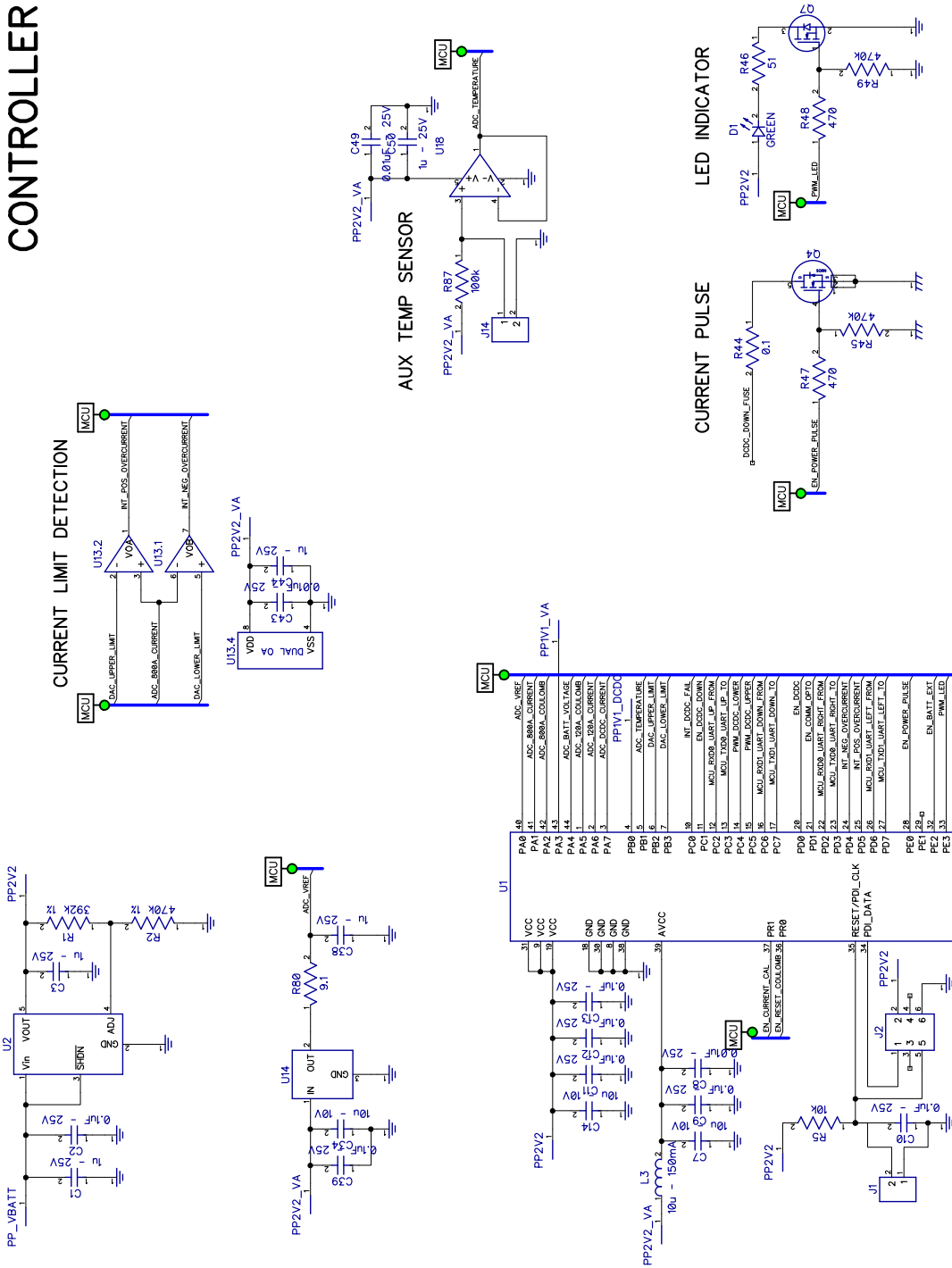


Figure 5.40 – Revision A Schematic – Page 2 – Controller

ANALOG MEASUREMENT

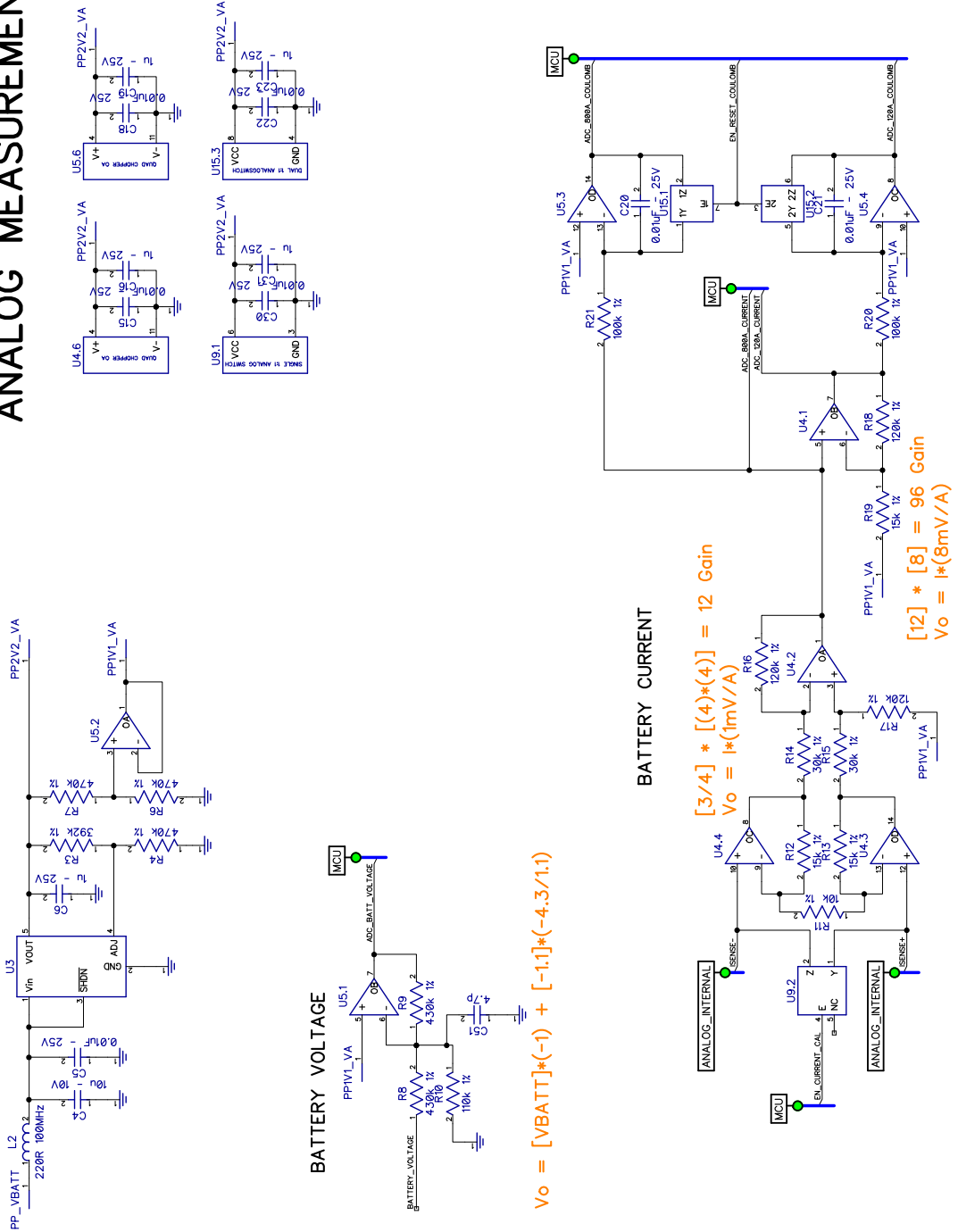


Figure 5.41 – Revision A Schematic – Page 3 – Analog Measurement

COMMUNICATION

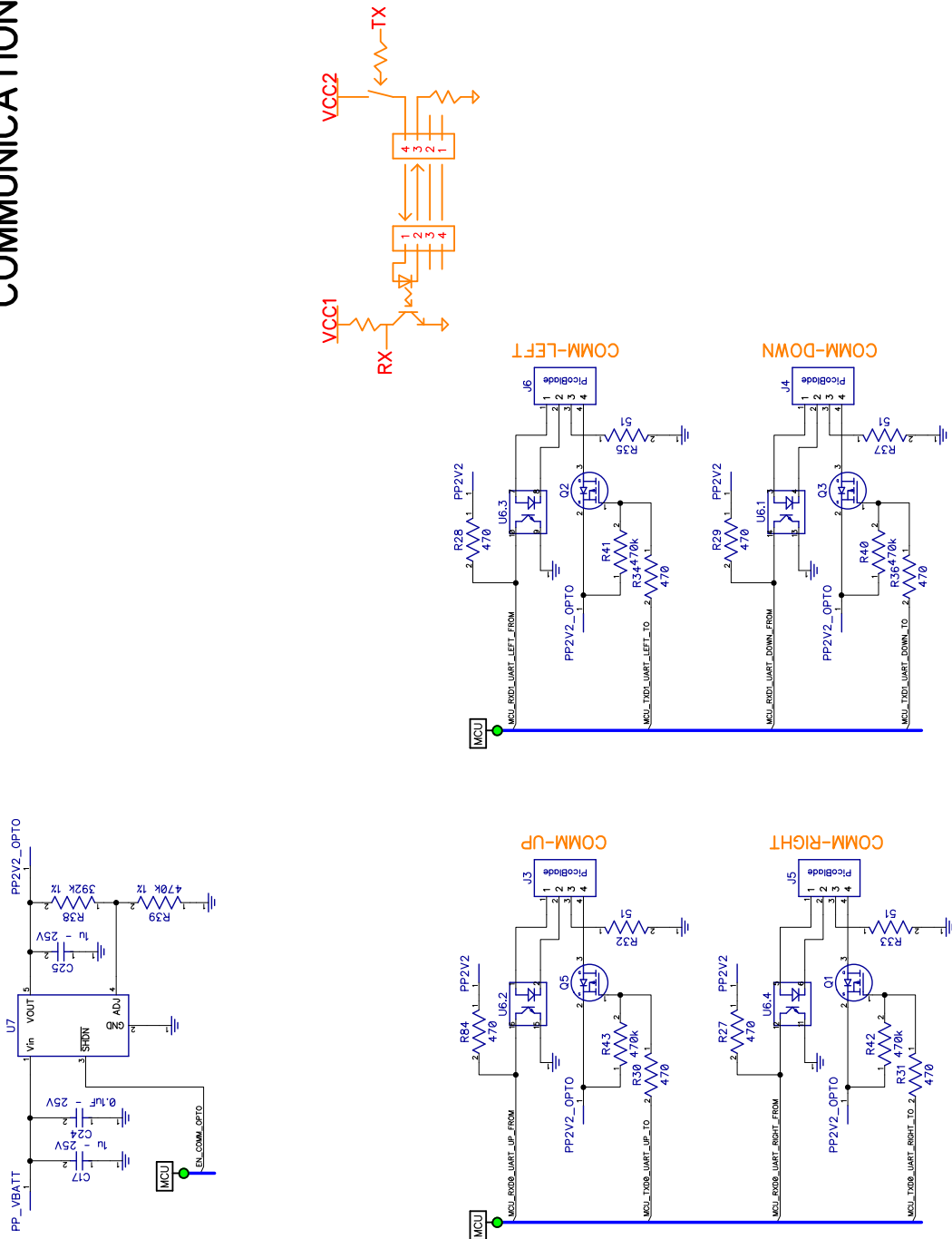


Figure 5.42 – Revision A Schematic – Page 4 – Communication

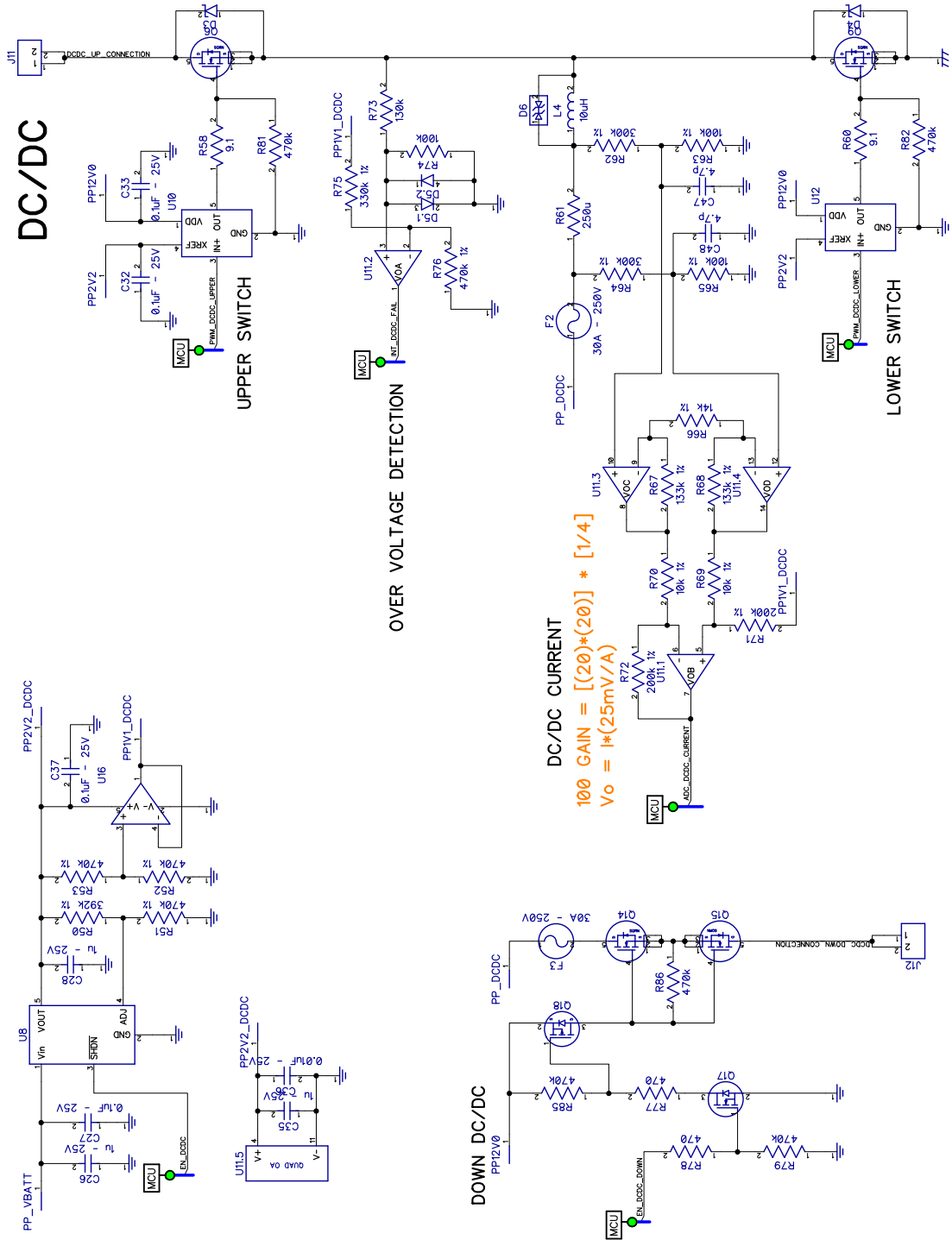


Figure 5.43 – Revision A Schematic – Page 5 – DC/DC

H.2 Bill of Materials

Table 5.12 – Revision A Bill of Materials

RefDes	Value	Qty	Manu	Manu PN	Digikey
C29, C45, C47, C48, C51	4.7p	5	Murata	GRM1885C1H4R7CZ01D	490-1389-1-ND
C5, C8, C15, C18, C20, C21, C22, C30, C36, C43, C49	0.01uF - 25V	11	Yageo	CC0603KRX7R8BB103	311-1360-1-ND
C2, C9, C10, C11, C12, C13, C24, C27, C32, C33, C37, C39, C42	0.1uF - 25V	13	Yageo	CC0603KRX7R8BB104	311-1341-1-ND
C1, C3, C6, C16, C17, C19, C23, C25, C26, C28, C31, C35, C38, C40, C44, C50	1u - 25V	16	Yageo	CC0805ZRY5V8BB105	311-1358-1-ND
C4, C7, C14, C34, C41	10u - 10V	5	Yageo	CC0805ZKY5V6BB106	311-1355-1-ND
C46	10u - 25V	1	TDK	C3216Y5V1E106Z	445-3469-1-ND
R90, R91, R92, R93	0	4	Yageo	RC0603JR-070RL	311-0.0GRCT-ND
R54, R55, R56, R61	250u	4	Stackpole	CSS2725FTL250	CSS2725FTL250CT-ND
R44	0.1	1	Bourns	CRA2512-FZ-R100ELF	CRA2512-FZ-R100ELFCT-ND
R58, R60, R80	9.1	3	Panasonic	ERJ-3GEYJ9R1V	P9.1GCT-ND
R32, R33, R35, R37, R46	51	5	Yageo	RC0603JR-0751RL	311-51GRCT-ND
R27, R28, R29, R30, R31, R34, R36, R47, R48, R57, R77, R78, R84, R89	470	14	Yageo	RC0603JR-07470RL	311-470GRCT-ND
R11, R69, R70, R5	10k 1%	4	Yageo	RC0603FR-0710KL	311-10.0KHRCT-ND
R66	14k 1%	1	Yageo	RC0603FR-0714KL	311-14.0KHRCT-ND
R12, R13, R19	15k 1%	3	Yageo	RC0603FR-0715KL	311-15.0KHRCT-ND
R14, R15	30k 1%	2	Yageo	RC0603FR-0730KL	311-30.0KHRCT-ND
R20, R21, R22, R24, R63, R65, R74, R87	100k 1%	8	Yageo	RC0603FR-07100KL	311-100KHRCT-ND
R10	110k 1%	1	Yageo	RC0603FR-07110KL	311-110KHRCT-ND
R16, R17, R18	120k 1%	3	Yageo	RC0603FR-07120KL	311-120KHRCT-ND
R73	130k	1	Yageo	RC0603FR-07130KL	311-130KHRCT-ND
R67, R68	133k 1%	2	Yageo	RC0603FR-07133KL	311-133KHRCT-ND
R71, R72	200k 1%	2	Yageo	RC0603FR-07200KL	311-200KHRCT-ND
R23, R25, R62, R64	300k 1%	4	Yageo	RC0603FR-07300KL	311-300KHRCT-ND
R75	330k 1%	1	Yageo	RC0603FR-07330KL	311-330KHRCT-ND
R1, R3, R38, R50	392k 1%	4	Yageo	RC0603FR-07392KL	311-392KHRCT-ND
R8, R9	430k 1%	2	Yageo	RC0603FR-07430KL	311-430KHRCT-ND
R2, R4, R6, R7, R39, R51, R52, R53, R40, R41, R42, R43, R45, R49, R59, R76, R79, R81, R82, R83, R85, R86, R88	470k 1%	23	Yageo	RC0603FR-07470KL	311-470KHRCT-ND
R26	1.6M 1%	1	Panasonic	ERJ-3EKF1604V	P1.60MHCT-ND
D1	GREEN	1	OSRAM	LG L29K-G2J1-24-Z	475-2709-1-ND
D2, D3, D4		3	Micro	SK310B-TP	SK310B-TPCT-ND
D5		1	NXP	BAV23,215	568-1620-1-ND
D6		1	Bourns	SMAJ8.5CA	SMAJ8.5CABCT-ND
D7	5.9V	1	NXP	PLVA659A,215	568-6832-1-ND
F1		1	Little Fuse	0466.125NR	F1450CT-ND
F2, F3		2	Bel Fuse	SMM 30	507-1524-1-ND
J7		1	N/A	N/A	N/A
J8, J19		2	N/A	N/A	N/A
Headers (J1, J2, J11, J12, J14)			FCI	78511-436HLF	609-3510-ND
J3, J4, J5, J6		4	Molex	53047-0410	WM1733-ND
PicoBlade Female			Molex	51021-0400	WM1722-ND
PicoBlade Female Crimps			Molex	50058-8000	WM1775CT-ND
L1, L3		2	TDK	MLZ2012M100W	445-6396-1-ND
L2		1	Wurth	742792034	732-1602-1-ND
L4	10uH	1	Abracon	AIRD-02-100K	535-11399-ND
Q1, Q2, Q3, Q5, Q8, Q18, Q19		7	IR	IRLML5103TRPBF	IRLML5103PBFCT-ND
Q4, Q6, Q9, Q10, Q11, Q12, Q13, Q14, Q15		9	NXP	PSMN0R9-25YLC,115	568-6720-1-ND
Q7, Q16, Q17		3	IR	IRLML6346TRPBF	IRLML6346TRPBFCT-ND
U1		1	Atmel	ATXMEGA32A4-AU	ATXMEGA32A4-AU-ND
U2, U3, U7, U8		4	Micro	TC1071VCT713	TC1071VCT713CT-ND
U4, U5		2	TI	OPA4330AIDR	296-27626-1-ND
U6		1	Avago	ACPL-247-500E	516-2466-1-ND
U9		1	NXP	NX3LIT66GM,115	568-5548-1-ND
U10, U12		2	Fairchild	FAN3111ESX	FAN3111ESXCT-ND
U11		1	Microchip	MCP6284-E/ST	MCP6284-E/ST-ND
U13		1	Microchip	MCP6052-E/SN	MCP6052-E/SN-ND
U14		1	TI	REF3020AIDBZR	296-26321-1-ND
U15		1	NXP	74HC2G66GD,125	568-5432-1-ND
U16, U18		2	Microchip	MCP6L01RT-E/OT	MCP6L01RT-E/OTCT-ND
U17		1	Linear	LT3494EDDB#TRMPBF	LT3494EDDB#TRMPBFCT-ND

I. Calculation

I.1 DC/DC Converter's Modes of Operation

Switch 1 conducts

$$V_1 = \frac{dI}{dt}L + IR_1$$

Equation from the circuit

$$I_{sw1}(t_{sw1}) = \left(i_{sw1_initial} - \frac{V_1}{R_1}\right)e^{-\frac{R_1 t_{sw1}}{L}} + \frac{V_1}{R_1}$$

Solution for current due to switch 1

$$e^{-\frac{R_1 t_{sw1}}{L}} \approx 1 - \frac{R_1 t_{sw1}}{L}$$

$$-\frac{R_1 t_{sw1}}{L} \approx \text{small}$$

(Using current values, $t_{sw1} = T_{\text{period}}$ would result in a 1% error. SW1 would never be on for the whole period)

$$I_{sw1}(t_{sw1}) = \left(i_{sw1_initial} - \frac{V_1}{R_1}\right)\left[1 - \frac{R_1 t_{sw1}}{L}\right] + \frac{V_1}{R_1}$$

Substitute for exponential

$$I_{sw1}(t_{sw1}) = i_{sw1_initial} - (i_{sw1_initial}R_1 - V_1)\frac{t_{sw1}}{L}$$

Diode 1 conducts

$$V_1 + V_d = \frac{di}{dt}L + iR_1$$

Equation from the circuit

$$I_{d1}(t_{d1}) = \left(i_{d1_initial} - \frac{V_1 + V_d}{R_1}\right)e^{-\frac{R_1 t_{d1}}{L}} + \frac{V_1 + V_d}{R_1}$$

Solution for current due to diode 1

Substitute for exponential values similar to switch 1

$$I_{d1}(t_{d1}) = \left(i_{d1_initial} - \frac{V_1 + V_d}{R_1}\right)\left[1 - \frac{R_1 t_{d1}}{L}\right] + \frac{V_1 + V_d}{R_1}$$

Substitute for exponential

$$I_{d1}(t_{d1}) = i_{d1_initial} + (V_1 + V_d - i_{d1_initial}R_1)\frac{t_{d1}}{L}$$

Switch 2 conducts

$$-V_2 = \frac{di}{dt}L + iR_2$$

Equation from the circuit

$$I_{sw2}(t_{sw2}) = \left(i_{sw2_initial} + \frac{V_2}{R_2}\right)e^{-\frac{R_2 t_{sw2}}{L}} - \frac{V_2}{R_2}$$

Solution for current due to switch 2

Substitute for exponential values similar to switch 1

$$I_{sw2}(t_{sw2}) = \left(i_{sw2_initial} + \frac{V_2}{R_2}\right)\left[1 - \frac{R_2 t_{sw2}}{L}\right] - \frac{V_2}{R_2}$$

Substitute for exponential

$$I_{sw2}(t_{sw2}) = i_{sw2_initial} - (i_{sw2_initial}R_2 + V_2)\frac{t_{sw2}}{L}$$

Diode 2 conducts

$$-V_2 - V_d = \frac{di}{dt}L + iR_2$$

Equation from the circuit

$$I_{d2}(t_{d2}) = \left(i_{d2_initial} + \frac{V_2 + V_d}{R_2}\right)e^{-\frac{R_2 t_{d2}}{L}} - \frac{V_2 + V_d}{R_2}$$

Solution for current due to diode 2

Substitute for exponential values similar to switch 1

$$I_{d2}(t_{d2}) = \left(i_{d2_initial} + \frac{V_2 + V_d}{R_2}\right)\left[1 - \frac{R_2 t_{d2}}{L}\right] - \frac{V_2 + V_d}{R_2}$$

Substitute for exponential

$$I_{d2}(t_{d2}) = i_{d2_initial} - (i_{d2_initial}R_2 + V_2 + V_d)\frac{t_{d2}}{L}$$

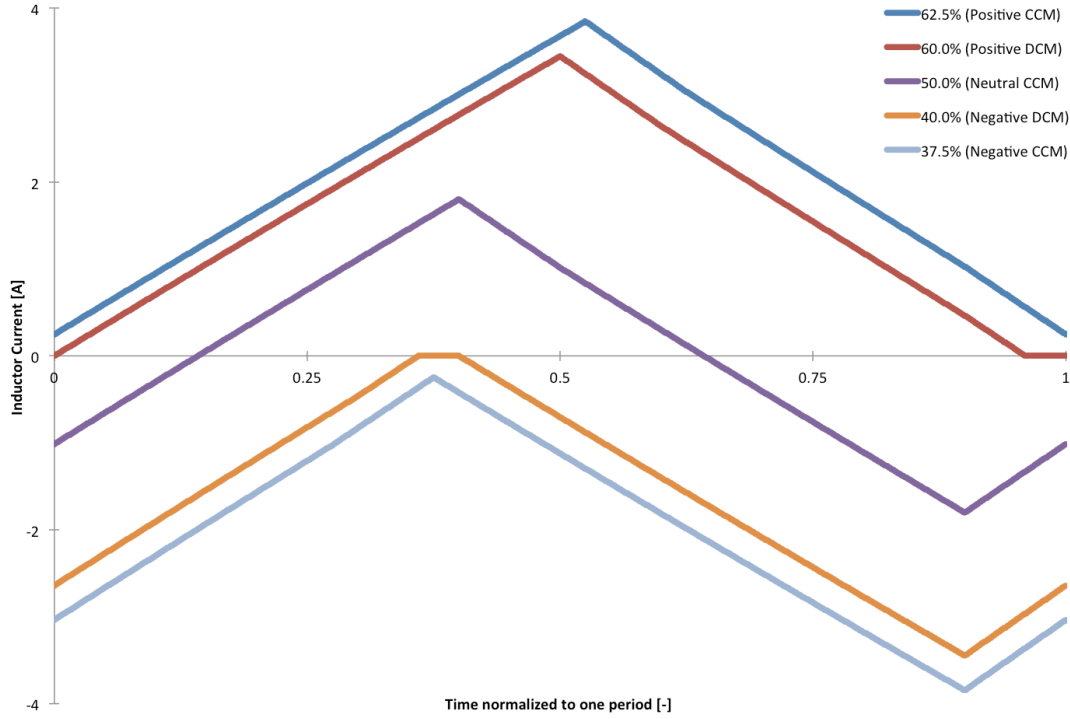


Figure 5.44 – Plot showing five modes of operation of the DC/DC converter.

Positive CCM

$$I_{sw1,posCCM} = I_{sw1}(t_{sw1}) = i_{sw1_initial} - (i_{sw1_initial}R_1 - V_1) \frac{t_{sw1}}{L}$$

$$I_{sw1,posCCM} = i_{min} - (i_{min}R_1 - V_1) \frac{DT}{L}$$

$$i_{sw1_initial} = i_{min}$$

$$t_{sw1} = DT$$

$$I_{d2,part1,posCCM} = I_{d2}(t_{d2}) = i_{d2_initial} - (i_{d2_initial}R_2 + V_2 + V_d) \frac{t_{d2}}{L}$$

$$i_{d2_initial} = I_{sw1,posCCM}$$

$$t_{d2} = \alpha T$$

$$I_{d2,part1,posCCM} = \left[i_{min} - (i_{min}R_1 - V_1) \frac{DT}{L} \right] - \left[(i_{min} - (i_{min}R_1 - V_1) \frac{DT}{L}) R_2 + V_2 + V_d \right] \frac{\alpha T}{L}$$

$$I_{d2,part1,posCCM} = i_{min} - (i_{min}R_1 - V_1) \frac{DT}{L} - (i_{min} - (i_{min}R_1 - V_1) \frac{DT}{L}) \frac{DTR_2}{L} + V_2 + V_d \frac{\alpha T}{L}$$

$$I_{sw2,posCCM} = I_{sw2}(t_{sw2}) = i_{sw2_initial} - (i_{sw2_initial}R_2 + V_2) \frac{t_{sw2}}{L}$$

$$i_{sw2_initial} = I_{d2,part1}$$

$$t_{sw2} = (1 - D - 2\alpha)T$$

$$I_{sw2,posCCM} = I_{d2,part1} - (I_{d2,part1}R_2 + V_2) \frac{(1 - D - 2\alpha)T}{L}$$

$$I_{sw2,posCCM} = \left[i_{min} - (i_{min}R_1 - V_1) \frac{DT}{L} - (i_{min} - (i_{min}R_1 - V_1) \frac{DTR_2}{L} + V_2 + V_d) \frac{\alpha T}{L} \right] - \left[(i_{min} - (i_{min}R_1 - V_1) \frac{DT}{L} - (i_{min} - (i_{min}R_1 - V_1) \frac{DTR_2}{L} + V_2 + V_d) \frac{\alpha T}{L}) R_2 + V_2 \right] \frac{(1 - D - 2\alpha)T}{L}$$

$$I_{d2,part2,posCCM} = I_{d2}(t_{d2}) = i_{d2_initial} - (i_{d2_initial}R_2 + V_2 + V_d) \frac{t_{d2}}{L}$$

$$i_{d2_initial} = I_{sw2,posCCM}$$

$$t_{d2} = \alpha T$$

$$I_{d2,part2,posCCM} = I_{sw2,posCCM} - (I_{sw2,posCCM}R_2 + V_2 + V_d) \frac{\alpha T}{L}$$

$$I_{d2,part2,posCCM} = \left[i_{min} - (i_{min}R_1 - V_1) \frac{DT}{L} - (i_{min} - (i_{min}R_1 - V_1) \frac{DTR_2}{L} + V_2 + V_d) \frac{\alpha T}{L} \right] - \left[(i_{min} - (i_{min}R_1 - V_1) \frac{DT}{L} - (i_{min} - (i_{min}R_1 - V_1) \frac{DTR_2}{L} + V_2 + V_d) \frac{\alpha T}{L}) R_2 + V_2 \right] \frac{(1 - D - 2\alpha)T}{L}$$

$$- \left[(i_{min} - (i_{min}R_1 - V_1) \frac{DT}{L} - (i_{min} - (i_{min}R_1 - V_1) \frac{DTR_2}{L} + V_2 + V_d) \frac{\alpha T}{L}) \right]$$

$$- \left[(i_{min} - (i_{min}R_1 - V_1) \frac{DT}{L} - (i_{min} - (i_{min}R_1 - V_1) \frac{DTR_2}{L} + V_2 + V_d) \frac{\alpha T}{L}) R_2 + V_2 \right] \frac{(1 - D - 2\alpha)T}{L}$$

$$I_{sw1,posCCM} + I_{d2,part1,posCCM} + I_{sw2,posCCM} + I_{d2,part2,posCCM} = 0$$

Solve for i_{min} using symbolic equation solver

$$i_{posCCM} = i_{min} = \frac{L \left((i_{min} - (i_{min}R_1 - V_1) \frac{DT}{L} - (i_{min} - (i_{min}R_1 - V_1) \frac{DTR_2}{L} + V_2 + V_d) \frac{\alpha T}{L}) R_2 + V_2 \right) \frac{(1 - D - 2\alpha)T}{L} + (i_{min} - (i_{min}R_1 - V_1) \frac{DT}{L} - (i_{min} - (i_{min}R_1 - V_1) \frac{DTR_2}{L} + V_2 + V_d) \frac{\alpha T}{L}) R_2 + V_2}{L \left((i_{min} - (i_{min}R_1 - V_1) \frac{DT}{L} - (i_{min} - (i_{min}R_1 - V_1) \frac{DTR_2}{L} + V_2 + V_d) \frac{\alpha T}{L}) R_2 + V_2 \right) \frac{(1 - D - 2\alpha)T}{L} + (i_{min} - (i_{min}R_1 - V_1) \frac{DT}{L} - (i_{min} - (i_{min}R_1 - V_1) \frac{DTR_2}{L} + V_2 + V_d) \frac{\alpha T}{L}) R_2 + V_2}$$

Ignore terms with T^2 , T^3 , and T^4

$$i_{posCCM} = \frac{DV_1 - (1 - D)V_2 - \alpha V_d}{DR_1 + (1 - D)R_2}$$

This is the minimum value, not the average. Converting to an average is easy but results in a complicated expression.

Positive DCM

$$I_{sw1, posDCM} = I_{sw1}(t_{sw1}) = i_{sw1_initial} - (i_{sw1_initial}R_1 + V_1) \frac{t_{sw1}}{L}$$

$$i_{sw1_initial} = 0$$

$$t_{sw1} = DT$$

$$I_{sw1, posDCM} = V_1 \frac{DT}{L}$$

$$I_{d2, part1, posDCM} = I_{d2}(t_{d2}) = i_{d2_initial} - (i_{d2_initial}R_2 + V_2 + V_d) \frac{t_{d2}}{L}$$

$$i_{d2_initial} = I_{sw1, posDCM}$$

$$t_{d2} = \alpha T$$

$$I_{d2, part1, posDCM} = I_{d2, part1, posDCM} - (I_{d2, part1, posDCM}R_2 + V_2 + V_d) \frac{\alpha T}{L}$$

$$I_{sw2, posDCM} = I_{sw2}(t_{sw2}) = i_{sw2_initial} - (i_{sw2_initial}R_2 + V_2) \frac{t_{sw2}}{L}$$

$$i_{sw2_initial} = I_{d2, part1}$$

$$t_{sw2} = (1 - D - 2\alpha)T$$

$$I_{sw2, posDCM} = I_{d2, part1} - (I_{d2, part1}R_2 + V_2) \frac{(1 - D - 2\alpha)T}{L}$$

$$I_{d2, part2, posDCM} = I_{d2}(t_{d2}) = i_{d2_initial} - (i_{d2_initial}R_2 + V_2 + V_d) \frac{t_{d2}}{L}$$

$$i_{d2_initial} = I_{sw2, posDCM}$$

$$t_{d2} = D_{posDCM}T$$

$$I_{d2, part2, posDCM} = I_{sw2, posDCM} - (I_{sw2, posDCM}R_2 + V_2 + V_d) \frac{D_{posDCM}T}{L}$$

$$I_{d2, part2, posCCM} = 0$$

Solve for D_{posDCM} using symbolic equation solver. D_{posDCM} is the non-zero time of the diode.

$$D_{posDCM} = \frac{D^2 L^2 R_2 T^2 V_1 - D^2 L^2 (R_2)^2 T^2 V_1 + D L^2 V_1 D L^2 R_2 T^2 V_1 - D L^2 R_2 T^2 V_1 - D L^2 R_2 T^2 V_1 - D L^2 R_2 T^2 V_1 - 2 D L (R_2)^2 T^2 V_1 + D L (R_2)^2 T^2 V_1 + L^3 V_1 - L^3 V_1 - L^3 V_1 - 2 L^2 R_2 T^2 V_1 + L^2 R_2 T^2 V_1 - 2 L^2 R_2 T^2 V_1 + L^2 R_2 T^2 V_1}{D^2 L (R_2)^2 T^2 V_1 - D^2 (R_2)^2 T^2 V_1 + D L^2 R_2 T^2 V_1 + D L^2 R_2 T^2 V_1 + D L^2 R_2 T^2 V_1 - D L (R_2)^2 T^2 V_1 - D L (R_2)^2 T^2 V_1 - D L (R_2)^2 T^2 V_1 - 2 D (R_2)^2 T^2 V_1 + D (R_2)^2 T^2 V_1 + L^3 V_1 - L^3 V_1 + L^3 V_1 - 2 L^2 R_2 T^2 V_1 + L^2 R_2 T^2 V_1 - 2 L^2 R_2 T^2 V_1 + L^2 R_2 T^2 V_1}$$

$$I_{avg} = \frac{\int_a^c f(t) dt}{c - a}$$

$$I_{avg} = \frac{\int_a^b f(t) dt + \int_b^c f(t) dt}{c - a}$$

$$I_{posDCM} = \frac{\int_0^{(1-\alpha+D_{posDCM})T} f(t) dt + \int_{(1-\alpha+D_{posDCM})T}^T f(t) dt}{T}$$

$$a = 0$$

$$b = (1 - \alpha + D_{posDCM})T$$

$$c = T$$

$$\int_{(1-\alpha+D_{posDCM})T}^T f(t) dt = 0$$

Because this is the time when the diode has reached zero and the switch has not enabled again

$$f(t) \approx \frac{I_{sw1, posDCM}}{2}$$

$$I_{posDCM} = \frac{\int_0^{(1-\alpha+D_{posDCM})T} f(t) dt}{T}$$

$$I_{posDCM} \approx \frac{I_{sw1, posDCM} (1 - \alpha + D_{posDCM})}{2}$$

Ignore terms with T^2 , T^3 , and T^4

$$I_{posDCM} \approx \left(\frac{1}{2} \right) \frac{D^2 T (V_1^2 + V_1 V_2) + D T V_1 V_d (1 - 2\alpha)}{D T R_2 (V_1 + V_2) + T R_2 (V_2 (\alpha - 1) - V_d \alpha) + L (V_d + V_2)}$$

This is the average value, not the minimum.

Negative CCM

$$I_{sw2,negCCM} = I_{sw2}(t_{sw2}) = i_{sw2_initial} - (i_{sw2_initial}R_2 + V_2) \frac{t_{sw2}}{L}$$

$$i_{sw2_initial} = i_{max} \text{ (all values are negative now)}$$

$$t_{sw2} = (1 - D - 2\alpha)T$$

$$I_{sw2,negCCM} = i_{max} - (i_{max}R_2 + V_2) \frac{(1 - D - 2\alpha)T}{L}$$

$$I_{d1,part1,negCCM} = I_{d1}(t_{d1}) = i_{d1_initial} + (V_1 + V_d - i_{d1_initial}R_1) \frac{t_{d1}}{L}$$

$$i_{d1_initial} = I_{sw2,negCCM}$$

$$t_{d1} = \alpha T$$

$$I_{d1,part1,negCCM} = I_{sw2,negCCM} + (V_1 + V_d - I_{sw2,negCCM}R_1) \frac{\alpha T}{L}$$

$$I_{sw1,negCCM} = I_{sw1}(t_{sw1}) = i_{sw1_initial} - (i_{sw1_initial}R_1 - V_1) \frac{t_{sw1}}{L}$$

$$I_{sw1,negCCM} = I_{d1,part1,negCCM}$$

$$t_{sw1} = DT$$

$$I_{sw1,negCCM} = I_{d1,part1,negCCM} - (I_{d1,part1,negCCM}R_1 - V_1) \frac{DT}{L}$$

$$I_{d1,part2,negCCM} = I_{d1}(t_{d1}) = i_{d1_initial} + (V_1 + V_d - i_{d1_initial}R_1) \frac{t_{d1}}{L}$$

$$i_{d1_initial} = I_{sw1,negCCM}$$

$$t_{d1} = \alpha T$$

$$I_{d1,part2,negCCM} = i_{d1_initial} + (V_1 + V_d - i_{d1_initial}R_1) \frac{t_{d1}}{L}$$

$$I_{sw2,negCCM} + I_{d1,part1,negCCM} + I_{sw1,negCCM} + I_{d1,part2,negCCM} = 0$$

Solve for i_{max} using symbolic equation solver

$$i_{negCCM} = i_{max} = \frac{(D + 2\alpha)V_1 + (D + 2\alpha - 1)V_2 + 2\alpha V_2}{(D + 2\alpha)R_1 + (1 - D - 2\alpha)R_2}$$

$$i_{negCCM} = \frac{(D + 2\alpha)V_1 + (D + 2\alpha - 1)V_2 + 2\alpha V_2}{(D + 2\alpha)R_1 + (1 - D - 2\alpha)R_2}$$

This is the minimum value, not the average. Converting to an average is easy but results in a complicated expression.

V1=3.33V, V2=3.33V, R1=0.052ohm, R2=0.052ohm, L=4.7uH, f=100kHz

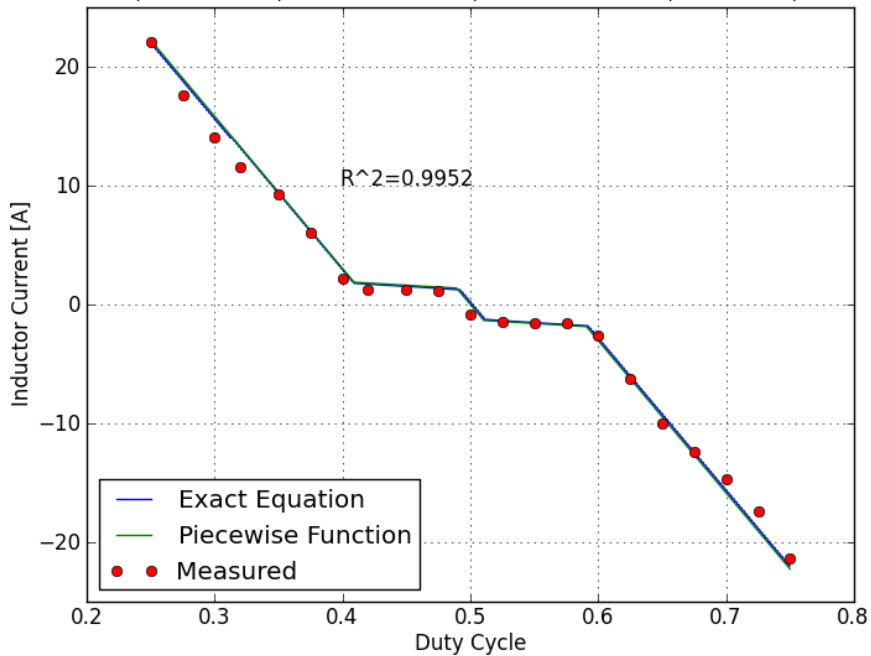


Figure 5.45 – Exact equation, piecewise equation, and measured data plotted.

I.2 Gains and Offsets of Current Measurement Path

$$V_{in,IA} = I_{batt}R_{sense}G_{divider} + E_{off,divider}$$

Calculating the voltage that will be input to the instrumentation amplifier circuit.

$$V_{in,IA2} = (V_{in,IA} + E_{off,1})G_1$$

Gain from IA circuit stage 1

$$V_{in,ADC} = (V_{in,IA2} + E_{off,2})G_2$$

Gain from IA circuit stage 2

$$V_{in,ADC} = [(V_{in,IA} + E_{off,1})G_1 + E_{off,2}]G_2$$

$$VAL_{ADC} = (V_{in,ADC} + E_{off,ADC})G_{ADC}$$

Gain and offset from ADC

$$VAL_{ADC} = \{[(V_{in,IA} + E_{off,1})G_1 + E_{off,2}]G_2 + E_{off,ADC}\}G_{ADC}$$

$$VAL_{ADC} = \{[(V_{in,IA} + E_{off,1})G_1 + E_{off,2}]G_2 + E_{off,ADC}\}G_{ADC}$$

$$VAL_{ADC} = [(V_{in,IA} + E_{off,1})G_1 + E_{off,2}]G_2G_{ADC} + E_{off,ADC}G_{ADC}$$

$$VAL_{ADC} = (V_{in,IA} + E_{off,1})G_1G_2G_{ADC} + E_{off,2}G_2G_{ADC} + E_{off,ADC}G_{ADC}$$

$$VAL_{ADC} = V_{in,IA}G_1G_2G_{ADC} + E_{off,1}G_1G_2G_{ADC} + E_{off,2}G_2G_{ADC} + E_{off,ADC}G_{ADC}$$

$$VAL_{ADC}(V_{in,IA} = 0) = \beta_{auto-cal}$$

Shorting the input to get the calibration coefficient right before measuring actual value.

$$\beta_{auto-cal} = E_{off,1}G_1G_2G_{ADC} + E_{off,2}G_2G_{ADC} + E_{off,ADC}G_{ADC}$$

$$VAL_{ADC} = V_{in,IA}G_1G_2G_{ADC} + \beta_{auto-cal}$$

$$VAL_{ADC} = [I_{batt}R_{sense}G_{divider} + E_{off,divider}]G_1G_2G_{ADC} + \beta_{auto-cal}$$

$$VAL_{ADC} = I_{batt}R_{sense}G_{divider}G_1G_2G_{ADC} + E_{off,divider}G_1G_2G_{ADC} + \beta_{auto-cal}$$

$$G_{cal} = R_{sense}G_{divider}G_1G_2G_{ADC}$$

$$E_{cal} = E_{off,divider}G_1G_2G_{ADC}$$

Calibration coefficients determined at the “factory” by measuring a known input.

$$VAL_{ADC} = I_{batt}G_{cal} + E_{cal} + \beta_{auto-cal}$$