DESIGN AND FABRICATION OF ELECTROSTATICALLY ACTUATED SERPENTINE-HINGED NICKEL-PHOSPHOROUS MICROMIRROR DEVICES

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ABSTRACT

DESIGN AND FABRICATION OF ELECTROSTATICALLY ACTUATED SERPENTINE-HINGED NICKEL-PHOSPHOROUS MICROMIRROR DEVICES

Nicholas A. Wiswell

A process for micromachining of micro-mirror devices from silicon-on-insulator wafers was proposed and implemented. Test methods and force applicators for these devices were developed. Following successful fabrication of these devices, a novel process for fabrication of devices out of the plane of the silicon wafer was proposed, so that the devices could be actuated electrostatically. In particular, the process makes use of thick photoresist layers as a sacrificial mold into which an amorphous nickel-phosphorous alloy may be deposited. Ideal design of the electrostatically actuated micro-mirrors was investigated, and a final design was selected and modeled using FEA software, which found that serpentine-hinged devices require approximately 33% of the actuation force of their straight-beamed counterparts. An aqueous electroless plating solution composed of nickel acetate, sodium hypophosphite, citric acid, ammonium acetate, and Triton X-100 in was developed for use with the process, and bath operating parameters of 85℃ and 4.5 pH were determined. However, this electroless solution failed to deposit in the presence of the photoresist. Several mechanisms proposed for deposition failure included leaching of organic solvents from the photoresist, oxidation of the nickel-titanium seed layer on which the deposition was intended to occur, and nonlinear diffusion of dissolved oxygen in the solution.

Keywords: MEMS, Micromirror, Serpentine, Silicon, Digital Mirror Device, Digital Light Projection, Electroless Deposition, Nickel Phosphorous, Process Integration, Semiconductor

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Key Terms

MEMS – **M**icro**e**lectrical**m**echanical **S**ystems, devices which capitalize on electrical and mechanical behavior at the microscale and whose size is generally below 1 mm.

Wafer – A thin, circular section of monocrystalline silicon, used as a substrate for processing of microelectronics and MEMS. It may contain impurities, often boron (p-type) or phosphorous (n-type) to alter its electrical properties.

DMD – **D**igital **M**icromirror **D**evice. A bistable, electrostatically actuated mirror device invented by Texas Instruments, similar to those discussed in this thesis.

DLP – **D**igital **L**ight **P**rojection. A light projection technology enabled by large arrays of closely packed, independently actuating DMDs.

PVD – **P**hysical **V**apor **D**eposition, a general term for a family of vacuum processes which produce chemisorbed adatoms by condensation of vaporized material.

Sputtering – A PVD process wherein the vaporized material is produced by accelerating a glow discharge plasma into a solid target, “sputtering” the material.

CVD – **C**hemical **V**apor **D**eposition. A family of vapor-phase deposition techniques, where deposits are obtained by chemical reaction of the substrate and/or the influent gas, rather than by condensation as in PVD. CVD is not constrained to operation in a vacuum.

Spin-Coating – A technique that enables even deposition of liquid coatings onto a wafer surface by centrifugal force accompanying high rotational speeds.

Photoresist – or **PR**. A viscous, photodefinable polymer with good resistance to chemical attack. Its viscosity allows it to be “cast” onto a wafer to a known thickness by spin-coating. Positive photoresist becomes soluble upon exposure to the correct wavelength of light; negative photoresist becomes insoluble.

Electroplating – A method of metal deposition wherein metal ions are reduced from solution onto a work piece by electrons provided via electric current.

ELD – **El**ectroless **D**eposition, alternatively Electroless Plating. A variation of electroplating wherein the reduction of metal ions is performed by reducing agents in the plating solution rather than by electric current.

CMP – **C**hemical **M**echanical **P**olishing. A planarization technique, used to planarize wafer surfaces, particularly after electroplating.

1. Introduction

1.1 The Digital Micromirror

In 1987, Dr. Larry Hornbeck, a staff scientist at Texas Instruments, developed the first practical digital micromirror [1]. At the time, the field of Microelectromechanical Systems – or MEMS – was in its infancy, and efforts to create micromirror arrays were little more than yet another Department of Defense-funded science experiment [2] [3]. Yet following Hornbeck's 1987 success, Texas Instruments began to aggressively pursue commercialization options for the digital micromirror device (DMD), integrating hundreds of thousands of the mirrors on a single chip. By the early 1990s, the first digital light projection (DLP) chips had reached the market and enabled the first cheap, lightweight, digital, full-color projectors. By the end of the decade, most of the initial problems with the DLP chips – particularly with overheating – had been overcome, and DLP-powered technology became affordable and commonplace. Today, almost all digital projectors contain a DLP chip. Moreover, digital micromirrors have found many other applications, including fiber optic switches and 3D imaging.

The functional heart of a modern DLP chip is an array of millions of digital micromirrors. These mirrors are "digital" because they have two states – they can be tilted completely to one side or the other depending on the applied voltage. Typically, in commercial devices, these tilt angles are about 10 degrees in either direction, and are well-defined because the mirror will usually encounter a

mechanical stop [4]. Because of their small size, digital micromirrors are also capable of switching between these “on” and “off” states extremely rapidly, generally as much as 100,000 times a second [5]. This extreme switching speed is critical – although most video projection applications require switching between successive image frames only every 16 milliseconds, the micromirrors create color greyscales by switching on and off about 100 times per frame, far faster than is visible to the eye [5]. In this way, a mirror may flip over 6,000 times per second in typical operation. This would normally lead to concerns about fatigue of the mirror hinges, but the small size of the mirrors results in unusual material properties. A typical micromirror may survive 5 trillion cycles – equating to over 200,000 operating hours [6].

Micromirrors have changed dramatically since their invention in 1987. The initial design, as submitted in the 1988 patent, consisted of a square metal mirror fabricated on top of a silicon wafer. The mirror was suspended from microscopic metal beams to permit torsion.

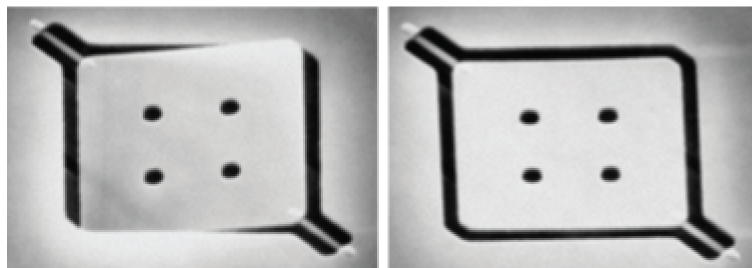


Figure 1: Primitive micromirrors: 10 degree tilt with applied voltage from hidden electrode (left), and neutral position with no voltage (right).

The key to the success of the digital micromirror is the fact that its tilt is controlled entirely by the voltage applied; if voltage is applied on an electrode, the mirror will rotate toward it. The face of the mirror itself effectively forms a pair of parallel-plate capacitors with the two electrodes below.

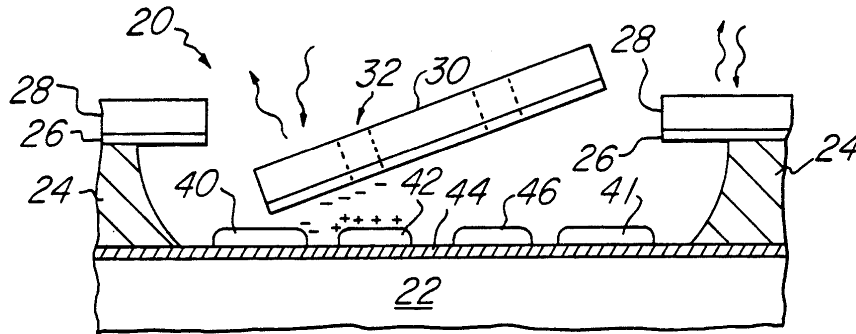


Figure 2: Cross-section of the original micromirror [1].

In Figure 2, the layer labeled 22 is the silicon wafer. 42 and 46 are the electrodes that pull the wafer down in either direction, and 40 and 41 are stops to keep the mirror from touching the electrode and discharging [1].

By placing voltage on only one electrode ("42" in Figure 2), the attractive force on the mirror can be estimated with the parallel-plate capacitor equation [7] [8].

$$F_d = -\frac{\frac{1}{2}(\varepsilon_r\varepsilon_0 WLV^2)}{d^2} \qquad \text{(Equation 1)}$$

Here, $\varepsilon_r\varepsilon_0 = 8.85 * 10^{-12}\ F/m$ for air, W and L are the sides of the mirror, given in the patent as W = L = $19\ \mu m$, d is the separation of the mirror from the electrode, given in the patent as d = $2.3\ \mu m$, and V is the voltage applied. The

patent suggests that a voltage of 50V is sufficient to achieve 10 degrees of rotation, so

$$F_d = -\frac{\frac{1}{2} * \left(8.85 * 10^{-12} \frac{F}{m}\right) * (19\ \mu m)^2 * (50\ V)^2}{(2.3\ \mu m)^2} = -0.755\ \mu N \quad \text{(Equation 2)}$$

This implies that a single micromirror (as described in Hornbeck's original 1988 patent) requires only $0.755\ \mu N$ of attractive force to achieve 10 degrees of rotation, and that this is achievable with a capacitive electrode. Of course, the torsion elastic modulus, or "rotational spring constant", of the hinges which oppose the pull of the electrode – and thus determine the degree of tilt achieved by any applied force - can be controlled by varying their thickness, length, and width. Another way to influence the torsion elastic modulus is by using a hinge geometry other than a straight beam [7].

Despite the ability to tilt the mirror 10 degrees in either direction in a fraction of a second, the first digital micromirror had limitations for projection applications – particularly because the spacing between each mirror due to the hinges was large, and this contributed to gaps between projected pixels

Ultimately, the solution to this issue was the three-level design present in modern DMDs: electrodes and circuitry on the bottom layer, the hinges and capacitor plate on the second layer, and the actual mirror on the third layer, joined with a post to the second layer. This permits the mirror to completely cover the hinges.

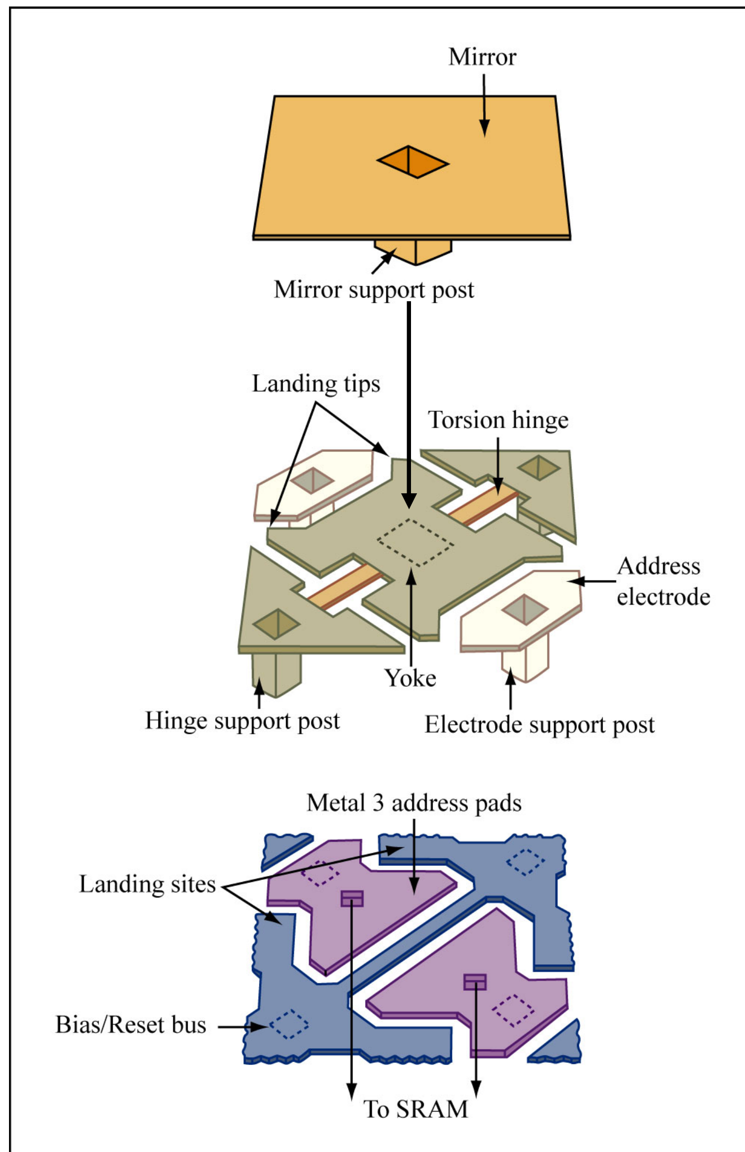


Figure 3: Modern DMD with three-level design. (Courtesy MIT Open Courseware)

1.2 Micromirrors at Cal Poly

In 2007, graduate student Steven Meredith began exploring the visco-elastic response of aluminum layers on silicon micromirrors, and in so doing created the first micromirror structures at Cal Poly. Rather than being made entirely of deposited aluminum, these devices were micromachined from monocrystalline

silicon and then covered with a deposited aluminum layer. Furthermore, instead of resting on supports deposited above the surface of silicon wafers, these planar devices were made by etching deep pits directly into the silicon wafers over which the thin micromirror could rotate. Many of these design decisions were made to match the capabilities of the Cal Poly Microfabrication Lab. Similar work was undertaken by graduate student Dylan Chesbro. Both Steven Meredith and Dylan Chesbro used identical straight-beam hinged mirrors, and neither reported electrostatic tilt angles much in excess of 0.3 degrees [9] [10]. Furthermore, Dylan Chesbro reported that this 0.3 degree angle was not stable over time, which would be unacceptable for commercial applications.

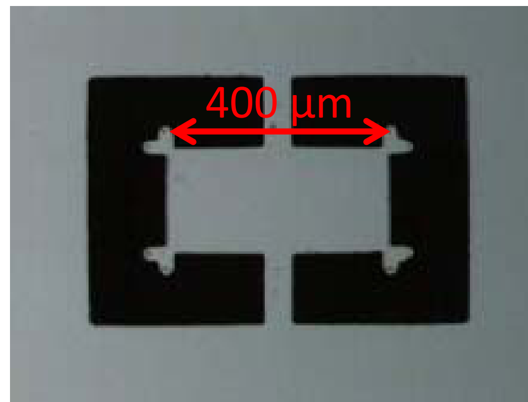


Figure 4: Prior design of micromirrors at Cal Poly [9].

These devices had other issues besides the limited deflection angle. These difficulties included a very poorly controlled device thickness resulting from a problematic etch step, and a large amount of wasted space on each wafer. This wasted space resulted from a processing need to draw vacuum upon a region of the wafer after 10-micron thick device membranes had been formed.

1.3 Initial Motivations

In order to address the issues encountered in the past with Cal Poly micromirrors, a study of the mechanical behavior of different hinge designs was desired. It was hoped that by exploring improvements to the device design, electrostatic tilt angles in excess of 10 degrees could be eventually obtained.

Further, exploring new processing techniques is crucial to continuous improvement in process capability of the entire Cal Poly Microfabrication lab. Improvements in yield and reductions in scrap rate also contribute to cost savings.

1.4 Initial Scope

1.4.1 Design Constraints

The use of serpentine hinge structures in at least one design was necessary in order to explore its potential to contribute significantly to the achievable tilt of the mirror devices. Initially, it was the most significant design change made to address the issue of limited tilt. A serpentine hinge performs the same function as a straight torsion beam hinge, but is expected to have a much lower torsion elastic modulus for the same effective hinge length [7].

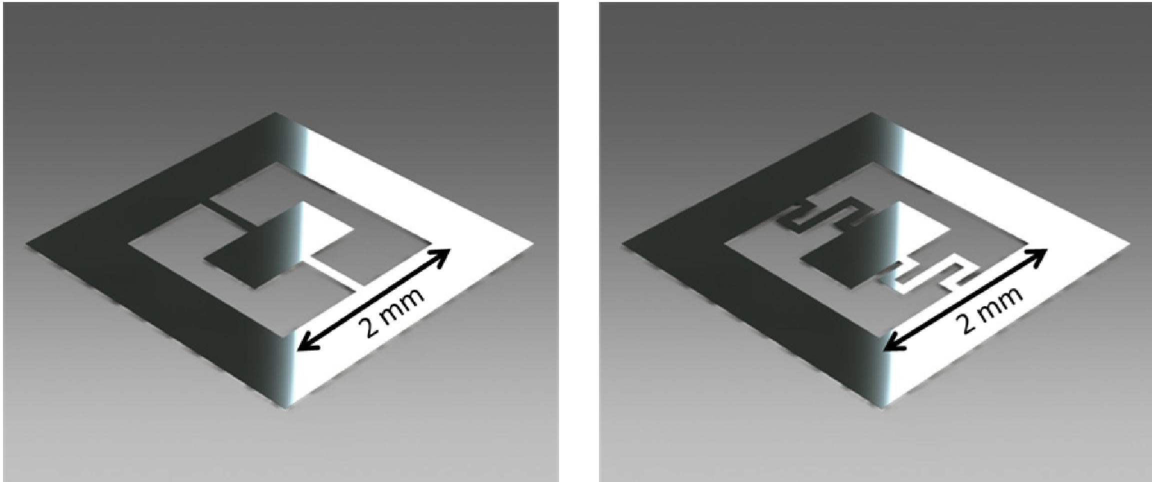


Figure 5: A straight-beam hinge CAD render (left) and serpentine-hinge CAD render (right).

Serpentine hinge structures increase the potential for the phenomenon of "pistoning", where actuation of the micromirror can cause undesired oscillation out of the plane of the silicon mirror [7]. In commercial mirrors, this "pistoning" is not an issue because the mirror snaps down onto mechanical stops that prevent any oscillations and define the "on"-state tilt angle, but without the use of these stops, the "pistoning" could become a concern.

The device material was constrained to monocrystalline silicon, since the fabrication process and processing equipment are specific to silicon wafers. However, the use of silicon for MEMS applications is very common. Some benefits of silicon include:

1) It is very strong, with a Young's modulus ranging from 130-188 GPa (depending on the direction of applied stress, resulting from monocrystalline anisotropy), making it suitable for mechanical applications. [11]

2) The difference between the coefficient of thermal expansion of silicon and its oxide is small. This is very important to avoid film stresses and warping of devices during processing. [12]
3) With a density of 2.3 g/cm^3 silicon is a lightweight material, less dense than even aluminum (2.7 g/cm^3).
4) Silicon forms silicides with many metals, enabling good electrical contact. [13]

Typically polycrystalline silicon is used for MEMS applications, but this is a result of processing concerns rather than performance benefits.

1.4.2 Process Constraints

The introduction of silicon on insulator (SOI) wafers into the process flow was meant to address the poorly controlled device thickness. These SOI wafers have an embedded oxide layer 10 microns below the top surface, and 400 microns above the bottom surface; as a result, any etch operation started from the top will by halted by a silicon dioxide layer after exactly 10 microns of etch, and any etch operation started from the bottom will be halted after 400 microns of etch, preventing it from cutting into the thickness of the 10 micron devices.

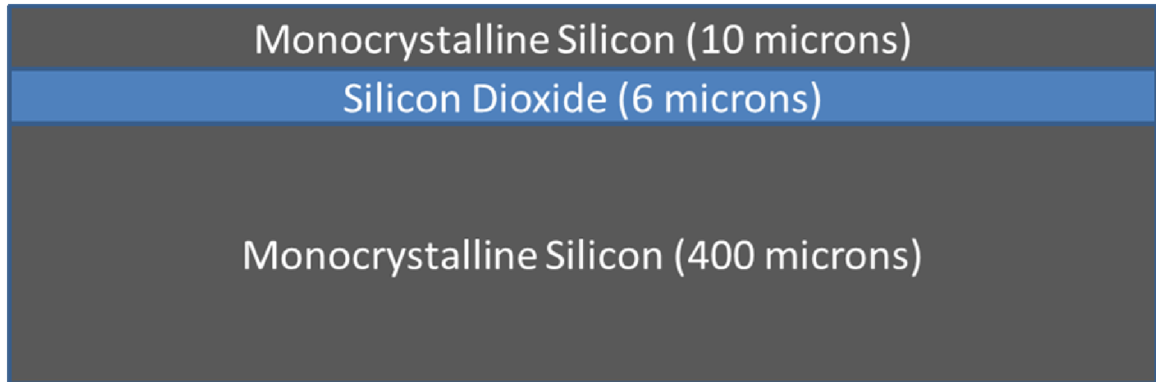


Figure 6: Cross-section of SOI wafers used for processing.

The use of SOI wafers, while a convenient method to guarantee a controlled thickness for the devices, is extremely expensive, at a cost of approximately $180 per wafer. Although this cost was accepted with the understanding that no alternative approach would be as effective, the expense made it even more imperative that the entire surface of the wafer be useful for devices, unlike the previous device fabrication process that did not use most of the center.

Ultimately, standardizing the thickness of the devices permits direct comparison of the mechanical properties – particularly the torsion elastic modulus – of one fabricated device to another, and ensures repeatability of mechanical performance for the same design. As a result, the use of an SOI wafer made it possible to make direct comparisons between straight-beam and serpentine-hinged devices, as well as devices of different hinge width and overall size. The process would need to be compatible with the buried oxide.

Besides compatibility with SOI wafers, the process had to address a number of practical constraints. Manufacturability is a constant constraint; Dylan Chesbro

reported a wafer scrap rate in excess of 75% in his thesis [10]. A high wafer scrap rate is a drain on funds and resources, and represents an enormously larger time investment to create a functional device wafer. Anything that will decrease the difficulty of manufacture or increase the yield per wafer is of enormous benefit. Moreover, if processes are not available in the Cal Poly Microfabrication Lab, they cannot be used to produce devices, no matter how effective they might otherwise be.

Economic concerns – particularly with regard to the expense of the wafer and the materials required to process it – were another major constraint on process design. For example, there are several methods of silicon etching available in the Microfabrication Lab. Reactive Ion Etching (RIE) through a silicon wafer is faster, more controlled, and more anisotropic than wet etching through the wafer with tetramethyl ammonium hydroxide (TMAH) – but it is also vastly more expensive. Decisions to use TMAH in the process at all were largely cost-conscious.

1.5 Initial Objectives

The initial objectives were therefore: to design several new devices utilizing both straight-beam and serpentine hinges, of various hinge width and overall size; to design a workable process to create the devices as designed; to use the new process to create functional devices; and to characterize the mechanical behavior of these devices in order to study the impact of hinge type, hinge width, and overall size on performance.

These initial goals were established as part of an iterative design process: the initial devices would bear significant similarities to devices previously fabricated

by other students, with a focus on resolving known issues. Once these goals were met, the next design iteration could apply lessons learned through the initial design toward improving performance.

2. Planar Micromirror Design

2.1 Mechanical Design of Micromirror Devices

In order to enable more informed design of the micromirror devices, Finite Element Analysis (FEA) software was employed to study their mechanical response to applied force. Using the COSMOSWorks FEA extension to SolidWorks, several iterations of designs featuring different beam widths, lengths, and mirror sizes were simulated to judge their relative ability achieve 10 degrees of tilt. The applied force used to create a response angle in the FEA package was nominally 100 micronewtons, as a similar force was reported in Steve Meredith's thesis during mirror actuation [9]. Although actual deflection angles for serpentine designs were significantly higher than for straight beam designs, the limitations of the COSMOSWorks FEA software – particularly the assumption of isotropy for single-crystalline silicon and mesh sizes that are too large for a small device like a micromirror – meant that deflection reported by the software was more useful for design purposes than for characterization.

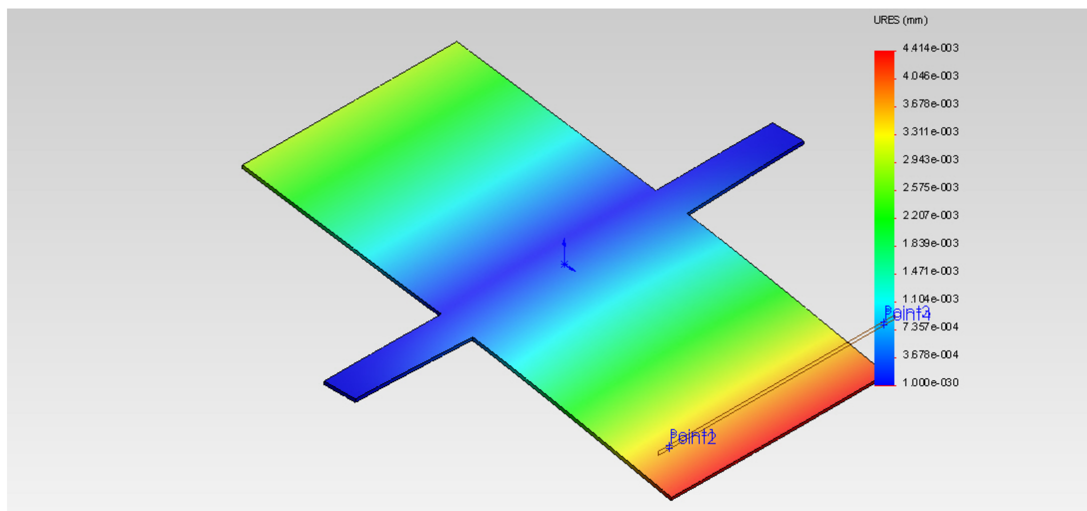


Figure 7: FEA of straight-beam micromirror

Eventually, one serpentine-hinge design was identified that appeared capable of achieving the desired tilt angle while also surviving any harsh processing steps. Because the overall objective was to study the relative efficacy of straight hinges and serpentine hinges, the same design footprint was used for both serpentine and straight-beam micromirrors. The final result of the modeling was seven devices of varying hinge type, hinge width, and mirror size, but with a common footprint, hinge length, and device thickness.

Table I: Matrix of Fabricated Micromirror Dimensions

Design #	Footprint	Hinge Type	Hinge Width
1	1 mm	Serpentine	80 µm
2	2 mm	Beam	160 µm
3	2 mm	Serpentine	160 µm
4	2 mm	Beam	240 µm
5	2 mm	Serpentine	240 µm
6	5 mm	Serpentine	400 µm
7	5 mm	Serpentine	600 µm

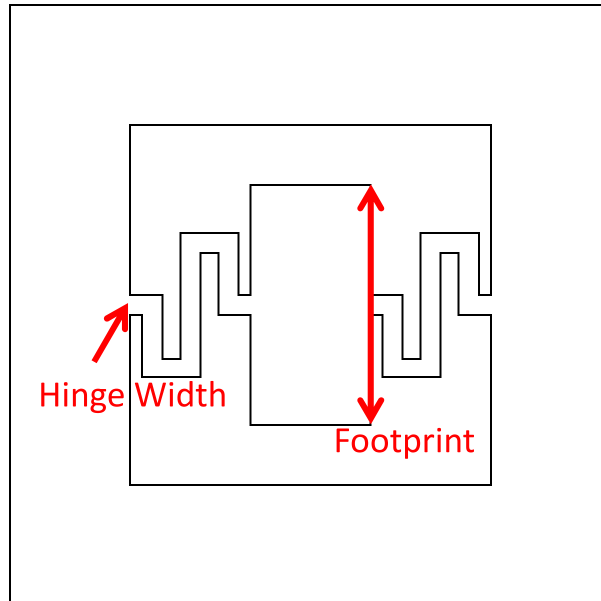


Figure 8: CAD Top View of Final Device Design #2.

It should be noted that all of these devices are large in comparison to previous micromirrors. This was a conscious decision made for two reasons. The first was simple: larger devices are easier to fabricate. The second was to make them easier to test: although small sizes are beneficial for electrostatically actuated micromirrors, electrostatic actuation is difficult to achieve for devices micromachined from the silicon substrate, as there is nowhere to deposit the conductive traces. In light of this, these mirrors were designed to be actuated mechanically, not electrostatically, and their size reflects this. The designs for electrostatically actuated serpentine-hinged devices were much smaller, to permit the devices to achieve 10 degrees of tilt before reaching the plane of the surface holding the static charge.

2.2 Overall Process Design

The fabrication process used by previous students, although similar to the planar process described herein to create serpentine devices, was unsuitable because it used a vacuum chuck to suction the center of the device wafer after reaching a point in the process where the device footprints were 10 micron thick silicon membranes. In the past, this problem was circumvented by leaving the center of the wafer free of devices, permitting vacuum to be drawn without shattering device membranes and breaking the vacuum seal. However, because of the expense of SOI wafers, it was desirable to use the entire surface area of the wafer, and so the process needed to be changed in order to avoid needing to suction the center of the wafer after creating devices.

The process step that required the suction was photoresist spin coating, wherein a photoactive polymer solution is dispensed onto the wafer. This photoresist is part of photolithography and is critical for creating geometries on the wafer. To solve the problem, the 10-micron deep device pattern was formed first; the photolithography step performed last created the geometries for the through-wafer device “windows”, rather than the geometries for the devices themselves.

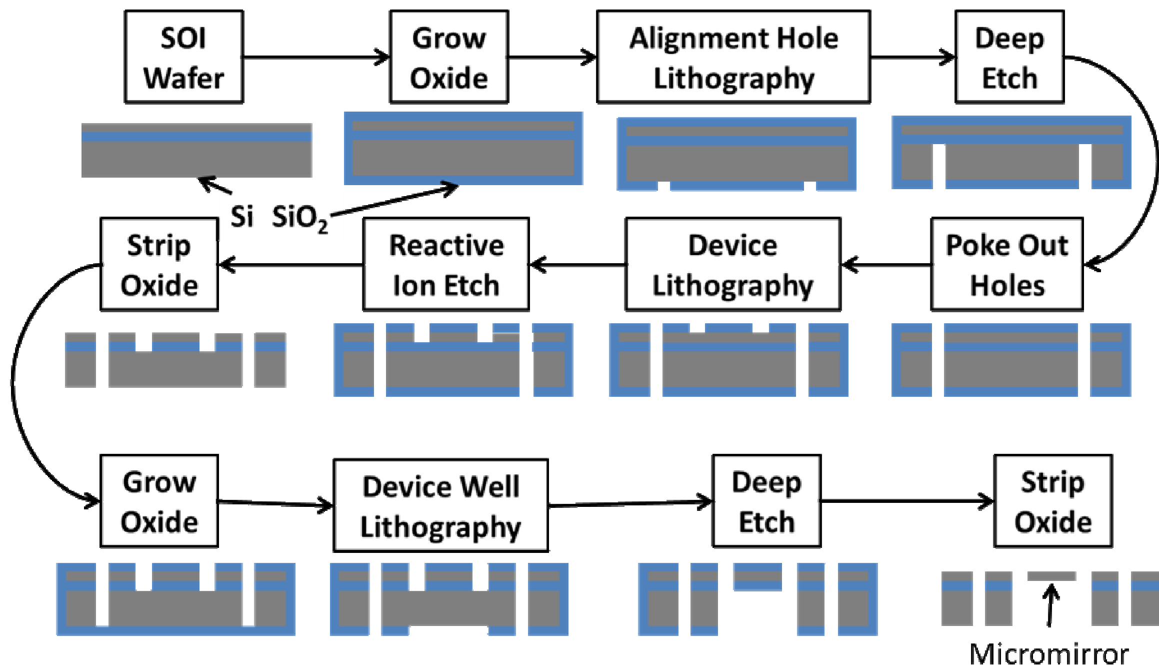


Figure 9: General overview of processing steps to create micromirror devices.

Figure 9 illustrates a simplified process flow for the planar devices. The cross-sections are not to scale, and show only a single device on the wafer surface between the two alignment holes. Two general types of process steps are shown: the etch steps, where the portions of the wafer not covered with silicon dioxide are removed, and the patterning steps, in which oxide is grown or shaped by lithography to create an etch mask. The oxide growth was accomplished by placing the wafers in a furnace, and the lithography was accomplished first by spin-coating the wafers with photoactive photoresist, then exposing certain portions of the photoresist, determined by the photomask, to ultraviolet light. This caused a chemical reaction in the exposed portions of photoresist that rendered it soluble, so it could be removed with a developing agent. The exposed oxide regions could then be removed with hydrofluoric acid. The etch steps, reactive

ion etching (RIE) and deep etching, were similar in their removal roles, except RIE produced much better uniformity and anisotropy, but was more expensive than the tetramethyl ammonium hydroxide (TMAH) deep etch. Because of the expense, TMAH was used for the bulk etch through the 400 microns of silicon wafer, and the RIE was limited to creating the actual device geometries.

Beyond the fact that the device geometries were created on the top of the wafer prior to creating the pits for them to be suspended over, it is worth noting that an entire deep etch step was necessary simply to create alignment holes. The topside photomask could not be used without first creating alignment holes, since alignment would have then been impossible to the bottom photomask. This was previously not the case: the device wells and alignment holes were created simultaneously during the first etch step.

2.3 Design and Creation of Micromirror Photolithography Masks

2.3.1 Mask Layout

Using the geometries of the seven devices, a top-side photomask was created to enable lithographic patterning onto the wafer and ultimately fabrication of the planar micromirror devices. At the time of the creation of the photomask, it was believed that mechanical testing would be possible using an existing microhardness tester. This microhardness tester was capable of extremely fine force resolution, but required test devices to be mounted onto a SEM stage. The square outlines on the top mask delineate squares that would fit onto a large SEM stage, and could serve as guides to assist in cleaving the wafer into test

coupons. Unfortunately this microhardness tester was not available, and so these test coupons are of no significance; however, all test coupons include design numbers 1-5, but the coupons labeled “A” feature design number 6, while the coupons labeled “B” feature design number 7 instead (note that “A” and “B” are inverted on the mask).

Additional features on the photomask were the plus-sign shaped alignment marks. These were intended to enable accurate alignment to the mask used for the bottom side of the wafer. These alignment marks were made very large (5 mm) because they would eventually need to become actual holes passing through the wafer. After the design was completed, the plastic photomask was printed using a very high-resolution printer (20,000 DPI) and attached to a glass plate for use in a lithographic aligner.

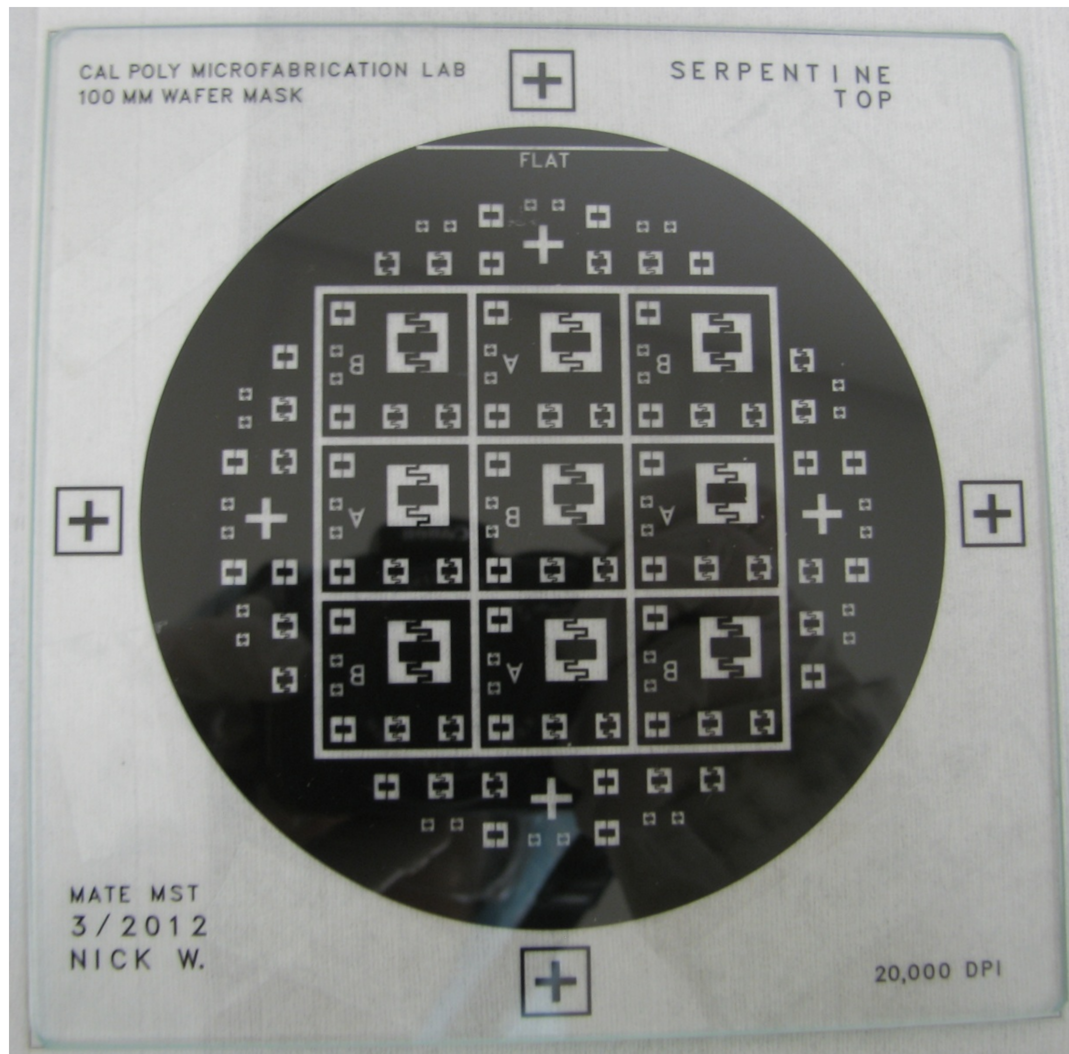


Figure 10: Topside photomask used to create devices attached to glass plate.

2.3.2 Anisotropic Etch Compensation

The bottom side of the wafer required an additional photomask in order to create deep through-hole “wells” that the micromirror devices could be suspended above and rotate into. However, because these holes were to be fabricated using deep tetramethyl ammonium hydroxide (TMAH) through-hole etching, it was necessary to compensate for the anisotropy of the etch so that the profile of the

holes would match the profile of the devices once the etch reached the top side of the wafer.

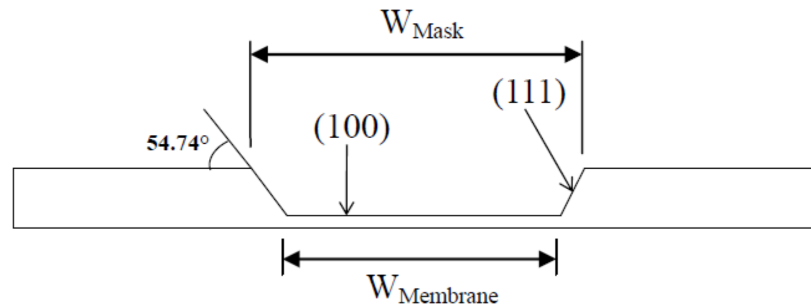


Figure 11: TMAH etches the different planes of monocrystalline silicon wafers at different rates, producing a 54.74 degree sidewall slope.

The (100) plane of silicon is attacked much more readily by TMAH than the (111) plane, which has atomic smoothness and closer atomic packing [14] [15]. The result of this etch-rate mismatch is flat, sloping walls through the wafer. The slope of these walls is a characteristic 54.74 degrees.

Because the depth of etch is approximately 400 microns (to the oxide etch stop of the SOI wafer), the difference in size of the resulting topside hole was approximated.

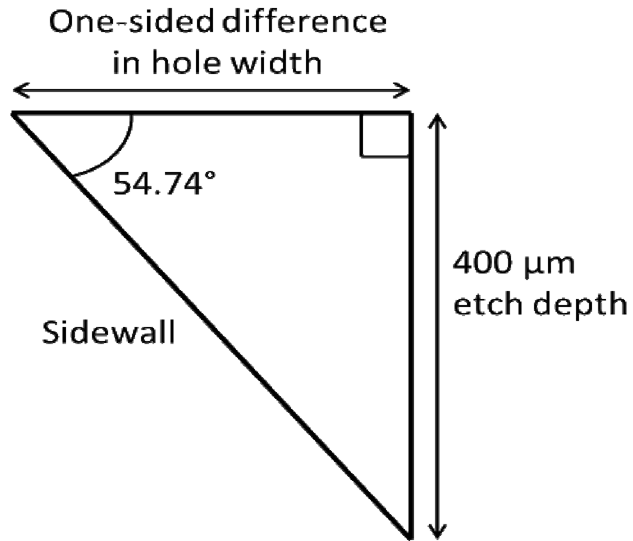


Figure 12: Geometry of etch compensation (not to scale).

Based on this geometry, the one-sided difference in hole width is

(Equation 3)

This provides a one-sided difference of 566 µm. By expanding each side of the top mask windows and alignment marks by this amount, the bottom-side mask was created.

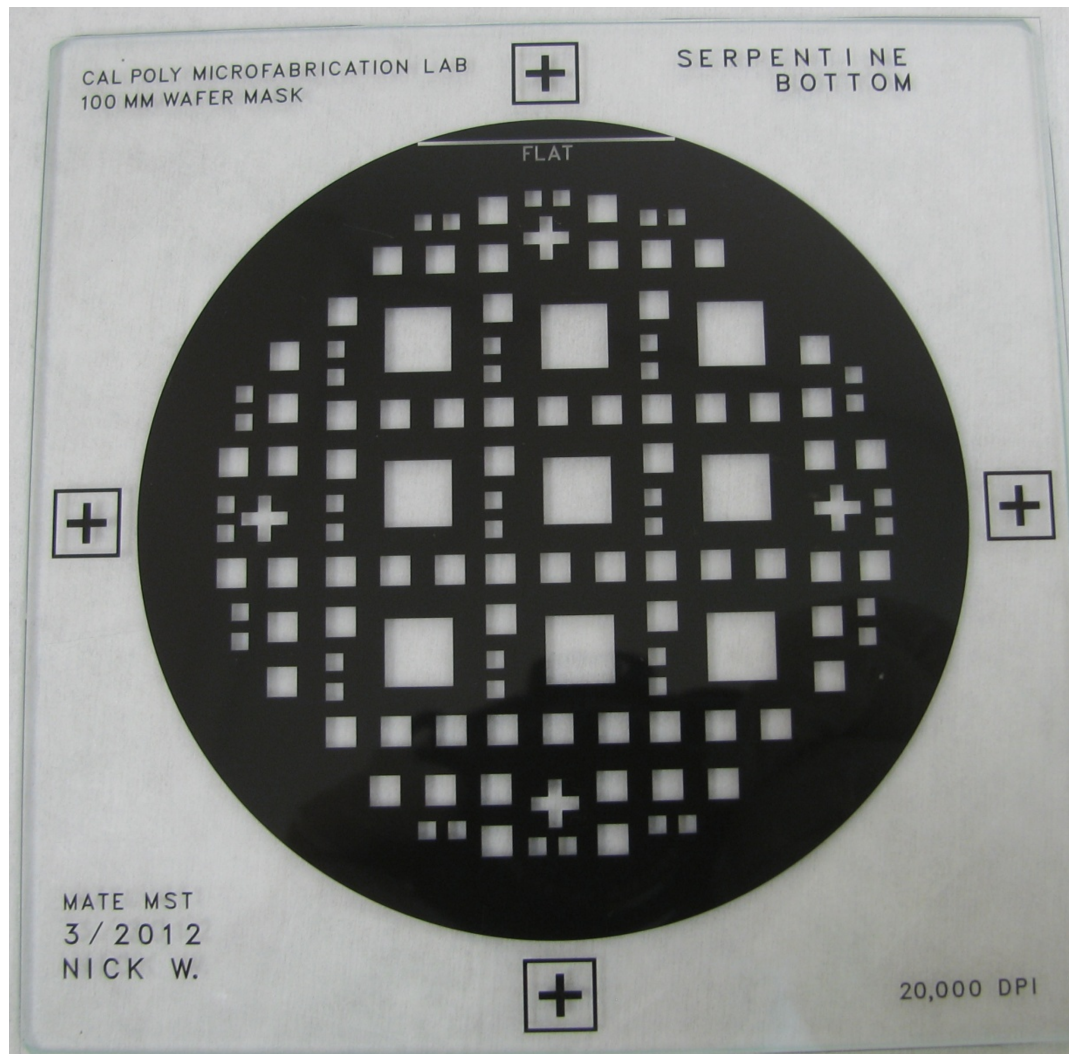


Figure 13: Bottom photomask used to create device wells attached to glass plate.

With the photomasks complete, actual fabrication of the planar devices could be attempted.

3. Planar Micromirror Fabrication

3.1 Silicon Oxide Growth

Although silicon oxide layers are not a part of the final micromirror device, they are instrumental as etch masks that define the actual geometries of the devices. One of the benefits of using silicon as a substrate is its stable, unreactive, thermally grown oxide. However, temperatures in excess of 900 degrees Celsius are required to produce oxide layers of any appreciable thickness. A tube furnace with built-in gas flow control and capable of maximum temperatures potentially as high as 1400 Celsius was used for oxide growth.

Figure 14: Thermal oxidation furnace in Cal Poly Microfabrication Lab.

When the furnace was hot, wafers were placed slowly into the tube (approximately 1 centimeter per second) to avoid thermal warping from rapid temperature change. The device wafers themselves were loaded into a quartz boat and surrounded with a dummy wafer on either side. These dummy wafers

served to deflect the turbulent flow of gas through the furnace away from the device wafers and ensure an even oxide layer.

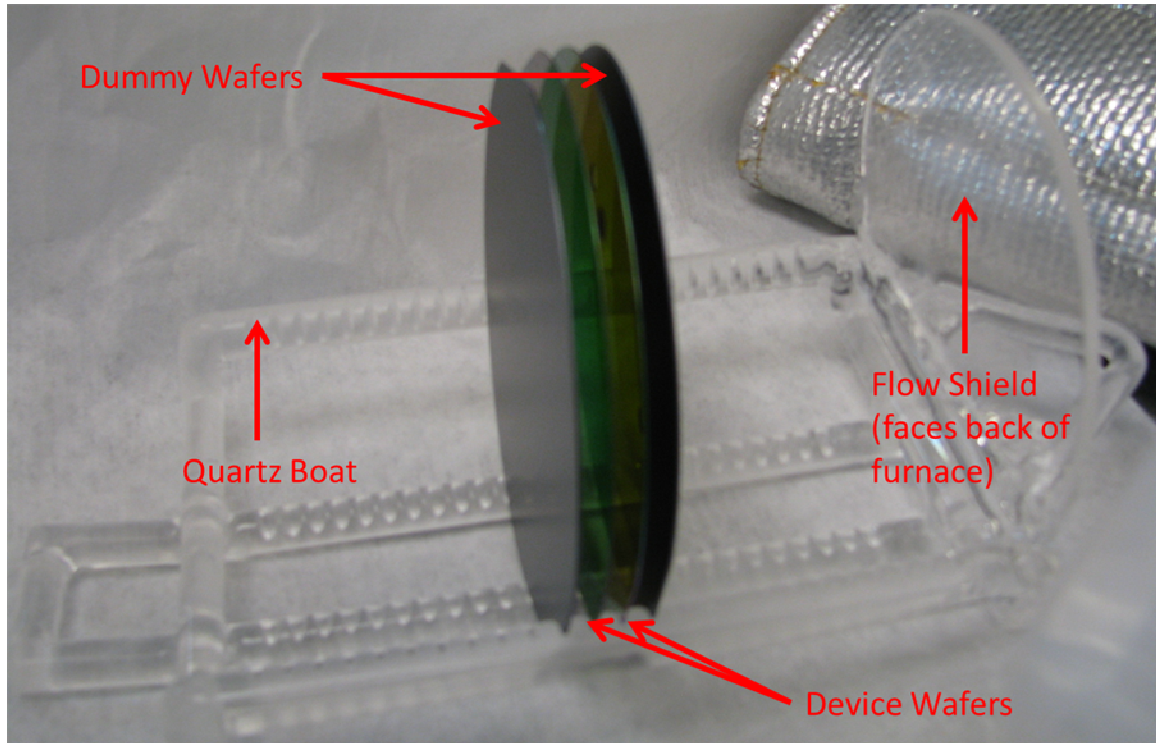


Figure 15: Oxidation boat with wafers loaded.

When the wafers were loaded into the furnace and the desired temperature was reached, the gas flowing into the furnace was changed from pure nitrogen to pure oxygen combined with water vapor. This allowed the oxidation process to begin. Once the desired time had elapsed, the flow gas was switched back to nitrogen to purge the furnace atmosphere and stop the oxide growth.

Part of the challenge with the oxidation furnace was determining what thickness of oxide was appropriate, and which process parameters would create an oxide

of that thickness. It was desirable to use the thinnest oxide permissible, because each time an oxide is grown in a furnace, some of the silicon layer that it grew upon is consumed: typically, for every micron of oxide that is created, 450 nanometers of silicon are lost [16]. Since the SOI wafers being used had a well-defined 10 micron device layer before oxidation, it was of interest to restrict oxidation as much as possible, so that the device layer did not become significantly smaller than 10 microns.

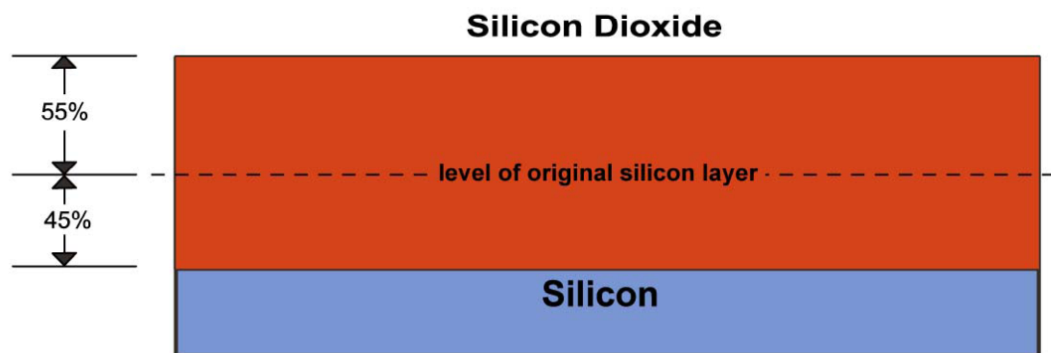


Figure 16: Relationship between oxide growth and consumption of the silicon substrate [17].

Because the only role of the silicon dioxide layer was to protect areas of silicon from etchants, the required thickness of oxide was determined entirely by the relative etch rate of silicon to silicon dioxide, known as the selectivity. The selectivity was used to ensure that the etch process would complete before the oxide layer was etched away.

Only two etch processes were used: SF_6/O_2 reactive ion etching (RIE), and tetramethyl ammonium hydroxide (TMAH) deep etch. The selectivity of silicon to

silicon dioxide of the RIE etch was approximately 100:1, and the selectivity of silicon to silicon dioxide of the TMAH deep etch was in excess of 1000:1 [18] [19].

The depth of the RIE etch was 10 microns. A selectivity of 100:1 implies that the required oxide thickness was 0.1 micron, or 1000 angstroms. Similarly, the depth of the TMAH etch was 400 microns, so a selectivity of 1000:1 implies a required oxide thickness of 0.4 microns, or 4000 angstroms. In order to cover both situations, the target oxide thickness was arbitrarily set to be 5000 angstroms.

In order to create an oxide with the desired 5000 angstroms of thickness, the Deal-Grove model, a theoretical framework relating the thickness of oxide to the temperature, process time, and presence of water vapor in the atmosphere, was used. The equation models the two processes which create oxide on a wafer: surface interaction and diffusion-limited transport. The relationship is [20]

$$t = \frac{X_O^2}{B} + \frac{X_O}{\frac{B}{A}} \qquad \text{(Equation 4)}$$

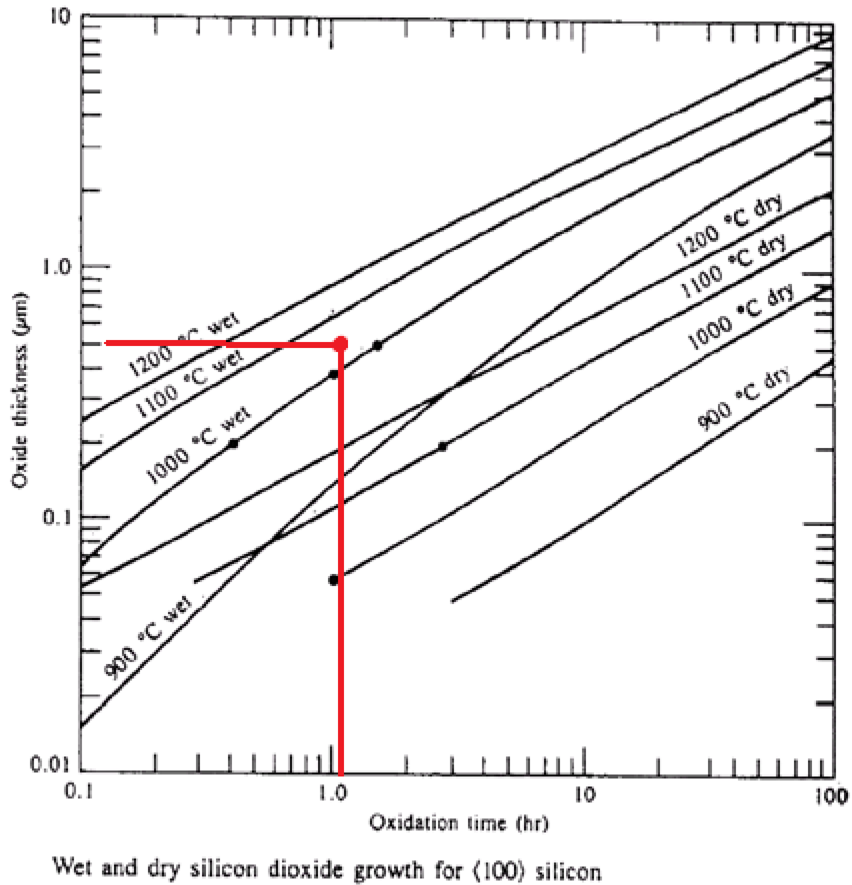


Figure 17: Deal-Grove curves. The required process time for a 5000 angstrom wet oxide at 1050℃ is approximately one hour [20].

Once a wafer was run in the furnace for 1 hour and 7 minutes at 1050 degrees Celsius, the final step was to verify that the oxide thickness was approximately 5000 angstroms. Oxide thickness measurements accurate to within a few angstroms could be obtained with a Filmetrics reflectometer, which uses spectral reflectance to mathematically determine the thickness of the oxide. Typically, a thin film will have strong thin-film interference at certain wavelengths and weak interference at others, depending on the thickness of the film. By analyzing the wavelength-based response, the Filmetrics device could determine the oxide thickness by comparison with a mathematical model. Generally, wafers had a

measured oxide thickness within a range of a few hundred angstroms from the target of 5000 angstroms.

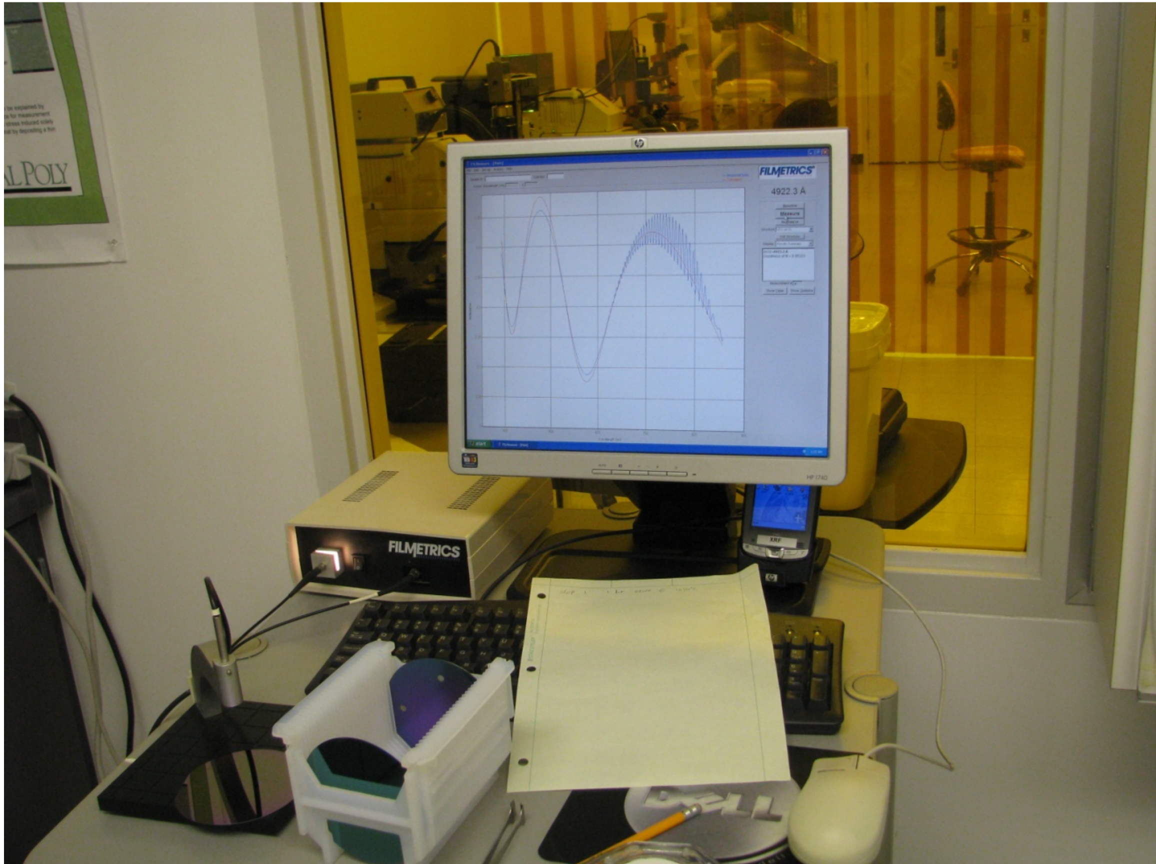


Figure 18: Filmetrics device measuring an oxide thickness of 4922 Å on an SOI wafer.

3.2 Photolithography

Photolithography was used to shape the oxide layer. The shaping of the oxide layer ultimately allowed transfer of the oxide pattern into the silicon substrate using etch processes to remove silicon not protected by an oxide layer. Several unit steps are involved in the photolithography used to shape the oxide. In order

of execution, these steps are: the deposition and spin-coating of photoresist, exposure of the photoresist, development of the photoresist, etching of the oxide, and finally the removal of the photoresist.

Photoresist spin-coating is a process that has been well-established by previous projects in the Microfabrication Lab. There are two types of photoresist for processing purposes: positive photoresist and negative photoresist. Positive photoresist becomes soluble in developing solution when exposed to light. Negative photoresist becomes insoluble when exposed. Because positive resist is easier to remove from the surface of the wafer after photolithography, it was selected for use. Consequently, the photomask was designed to expose the regions that should become soluble.

In order to spin-coat photoresist onto the wafer, approximately 2.5 mL of MicroChem MCC primer was dispensed onto the wafer, then spun for at 300 RPM for 30 seconds and 3000 RPM for 20 seconds. This caused the primer to evaporate and leave a better adhesion surface for the photoresist. Approximately 4 mL of Rohm-Haas Microposit S1813 positive photoresist was then dispensed onto the wafer, and spun using the following program.

Table II: Photoresist Spin-Coat Program

Step	Spin Speed (RPM)	Duration
1	200	20
2	500	10
3	4000	20
4	300	5

Once photoresist covered the wafer, it was soft-baked at 90℃ for 60 seconds to remove excess solvent. After the soft-bake, the wafer was exposed in the aligner. In order to create the alignment marks for the first deep etch step, aluminum foil was used to cover all of the features on the bottom photomask except the alignment marks. Because the alignment marks created this way were very large, successive lithography steps required alignment by hand rather than with the aligner microscope. This was accomplished through use of a small magnifying glass. Once the wafer was aligned and ready for exposure, the light integral was set to 4.5, corresponding to a dose time of 16.7 seconds, or 108 mJ/cm^2 of light energy. After being exposed, the wafer was ready for development.

In order to develop the wafer, it was submerged and agitated in Microposit CD-26 developer for 2 minutes. This removed the parts of the photoresist that had been exposed through the photomask, exposing the oxide. Before moving on to the oxide etch step, the wafer was hard-baked at 150℃ for 60 seconds to ensure that it would withstand the etching. At this point, the quality and “sharpness” of the features in the photoresist were verified with an optical microscope.

In order to remove the newly exposed oxide, the wafer was submerged in buffered oxide etchant (BOE). The active chemical in BOE is hydrofluoric acid, which attacks silicon dioxide but not photoresist. Because the oxide layer was 5000 angstroms thick, and BOE has a well-established etch rate of 800 angstroms per minute, wafers were left submerged for about 7 minutes to ensure the oxide was completely removed. For those steps that required the oxide on

the back side of the wafer to be left intact during the etch, the wafer was mounted in a Teflon fixture exposing only the top side of the wafer, and BOE was very carefully deposited onto the surface.

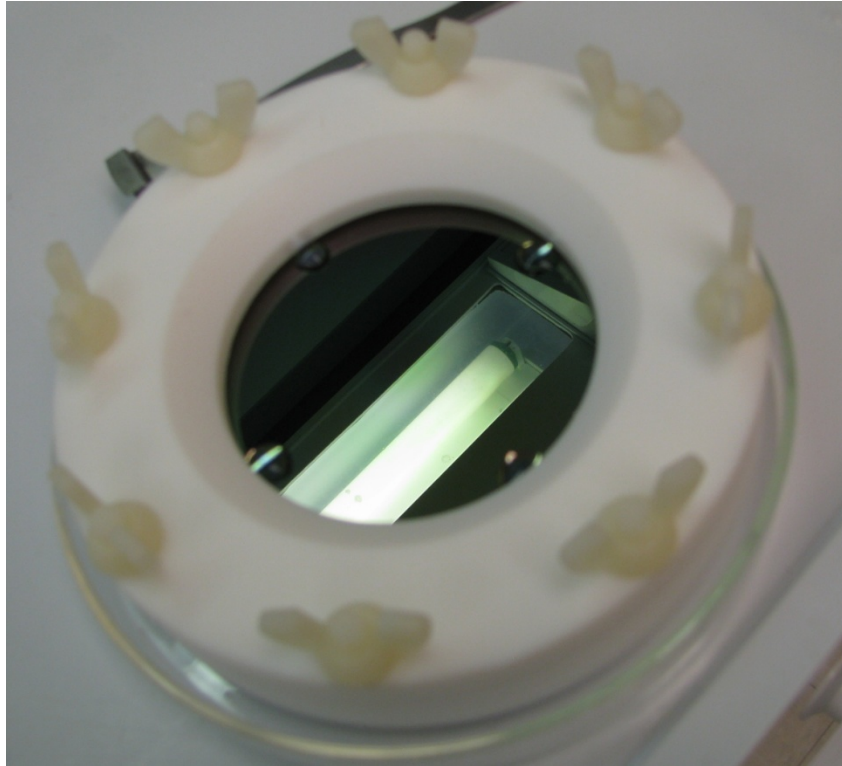


Figure 19: Creating alignment holes in oxide with BOE and Teflon fixture.

Finally, once the desired oxide pattern had been created, the wafer was submerged in Shipley photoresist stripper at 60℃ for 2 minutes to ensure removal of the photoresist.

3.3 Deep Etch

The deep etch step was used for two purposes: to create alignment holes which travel all the way through the wafer and enable the patterns on each side to be

aligned, and to dramatically thin the silicon wafer below the device layer, enabling them to flex into the pit below.

The deep etch process used 25% tetramethyl ammonium hydroxide (TMAH) solution at 85°C to remove silicon. Unfortunately, TMAH etch rates are extremely sensitive to both temperature and TMAH concentration [15] [18]. In order to keep concentration constant, the TMAH solution was held in a reflux condenser chamber intended to condense evaporated liquid. Furthermore, to control temperature, a coil heater was installed on the condenser chamber, and connected to an Omega temperature controller. This controller monitored temperature from a thermocouple inside the chamber and would set a duty cycle for the heater to maintain temperature at 85°C. Unfortunately, it would often permit temperature swings of as much as a few degrees Celsius.

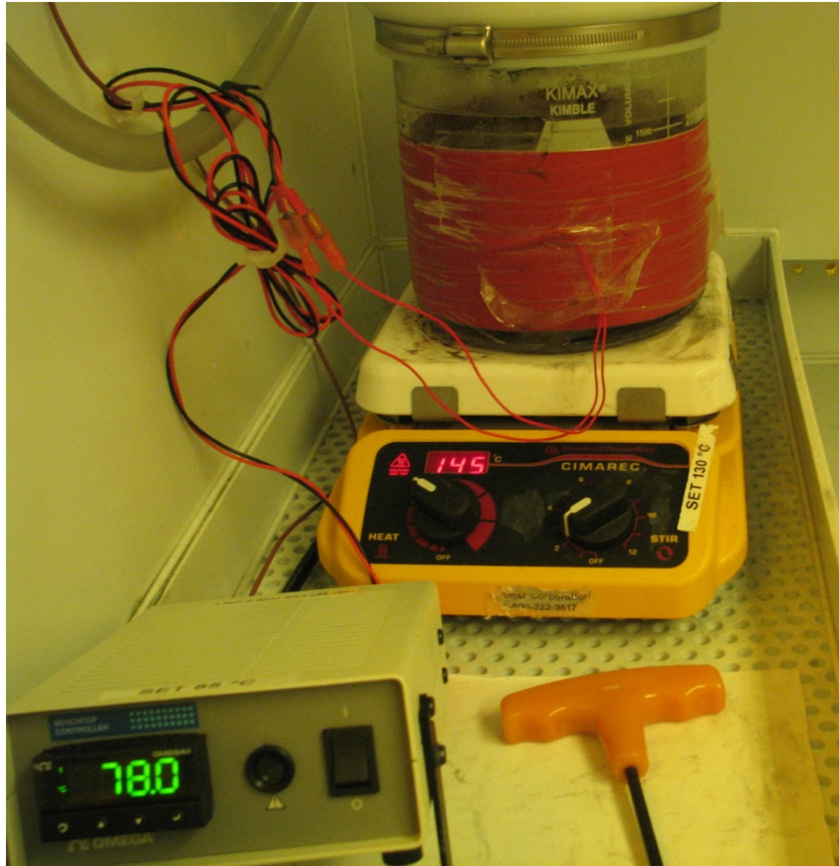


Figure 20: Condenser chamber with coil heater warming up to 85°C.

In order to determine etch rates for the TMAH, wafers were placed into the solution for a two hour period, then removed and placed in a profilometer. A profilometer can measure the depth of geometries on a surface by dragging a stylus along its surface.

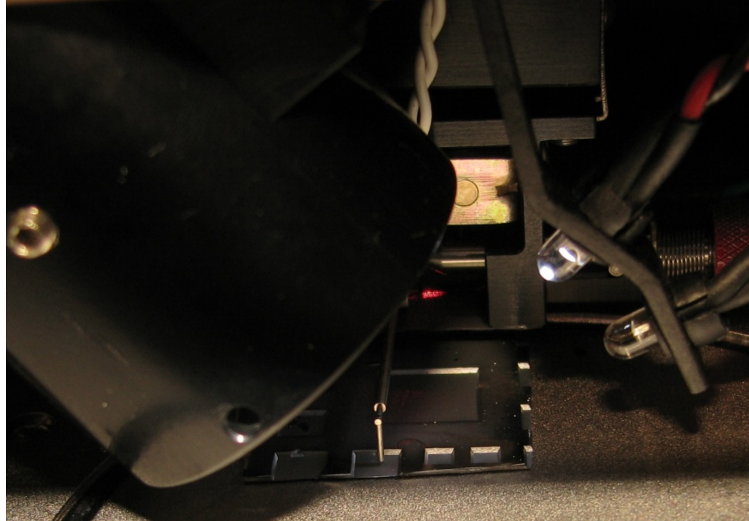


Figure 21: Profilometer measuring etch depth on a chunk of silicon.

By measuring the change in depth of the exposed features for every two hours of TMAH exposure, etch rates were established for four different test wafers.

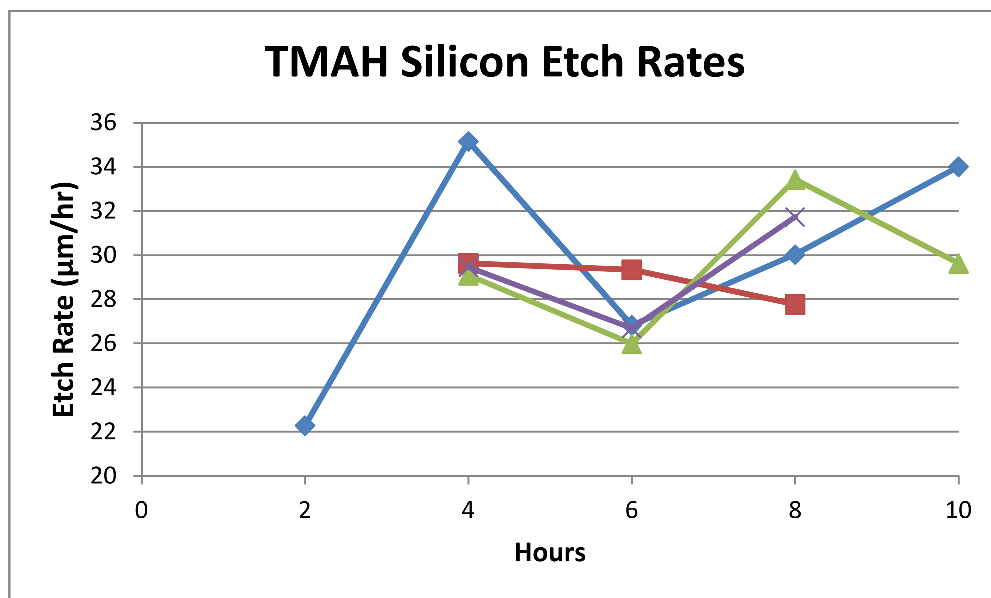


Figure 22: Etch rate measurements of TMAH deep etch over 2 hour intervals.

The etch rate was highly unpredictable, ranging from 22.3 µm/hr to 35.1 µm/hr. This unpredictability was likely due to poor temperature control. The best method

to compensate for this variation was simply to get close to the desired etch depth, and then begin making frequent measurements with the profilometer until the desired etch depth was achieved. Typical etch times to achieve 400 microns of depth were about 15 hours.

Unpredictable etch depth was not the only difficulty with the deep etch – imperfections in the oxide could lead to deep trenches over the course of 15 hours of etching. This was very harsh on the wafers, especially since two 15-hour deep etches were required to create devices, and this 30 hours of exposure to TMAH could make the wafers brittle, leading to breakage and wafer scrapping.

3.4 Reactive Ion Etch

A Reactive Ion Etcher was used in order to create the device geometries. Deep etching was undesirable because it creates sloping sidewalls that would not have been appropriate for the sides of the devices, and also because it has a tendency to undercut and etch beneath oxide masks, which could have seriously interfered with the structure of the mirror hinges.

In reactive ion etching, a plasma of reactive ions is created, and then these ions are accelerated toward the charged substrate. By accelerating these ions downward, a straight etch profile is ensured. Once the ions reach the surface, they tend to react with it and remove surface material.

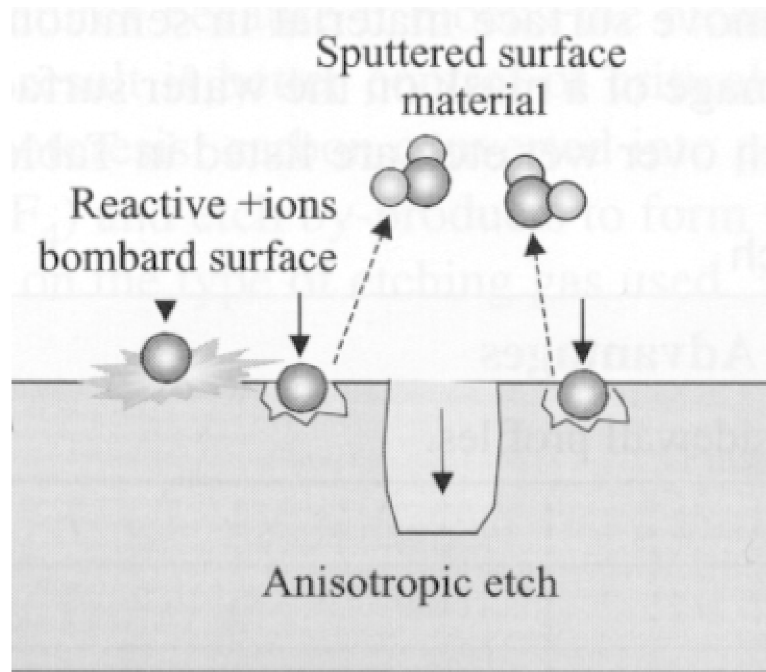
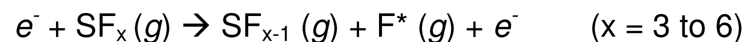


Figure 23: Reactive ion etching.

In the case of the RIE tool used for processing, the process gases available were limited to oxygen (O_2) and sulfur hexafluoride (SF_6). In the plasma, the SF_6 breaks apart when impacted by free electrons, producing fluorine radicals. The products can be struck again to produce even more radicals:



$$e^- + SF_x\,(g) \rightarrow SF_{x-1}\,(g) + F^*\,(g) + e^- \qquad (x = 3 \text{ to } 6)$$

The fluorine radicals (F^*) react with the silicon to produce volatile products, particularly SiF_4, which are vented out of the chamber [21].

One of the potential downsides to RIE is the sensitivity of the results to the process parameters. However, careful experimentation and control permits repeatable results. A gas mixture of 60% SF_6 and 40% O_2 at a power setpoint of 500 watts and pressure setpoint of 300 millitorr produced a black silicon wafer, which effectively destroyed any devices on the wafer.

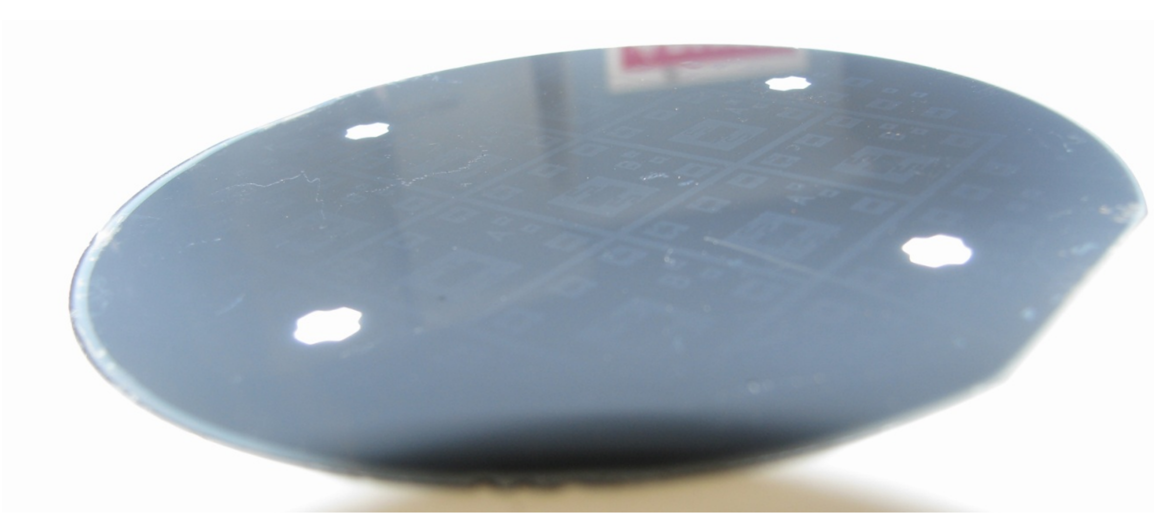


Figure 24: Black silicon wafer produced by RIE. The alignment holes and some device outlines are visible.

Similarly, a gas mixture of 70% SF_6 and 30% O_2 at a power setpoint of 300 watts and pressure setpoint of 300 millitorr caused the process wafer to inexplicably explode inside the chamber. The cause for this could not be determined, but the process parameters were considered unsuitable.

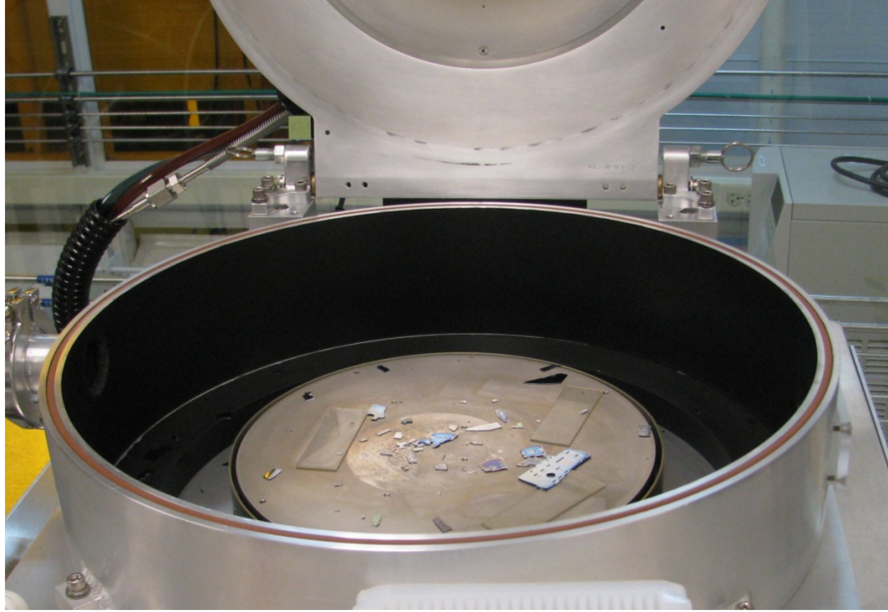


Figure 25: Wafer debris produced by RIE recipe.

The process identified as suitable for etching purposes was a mixture of 80% SF_6 and 20% O_2 at a power setpoint of 300 watts and pressure setpoint of 300 millitorr. The etch rate measured with the profilometer for this recipe was approximately 2.2 µm/min. In order to ensure the RIE would etch through the 10 microns of topside silicon and reach the oxide etch stop, a process time of 5 minutes was used.

4. Testing

4.1 Test Apparatus

After obtaining devices, the next step was to attempt mechanical testing in order to enable calculation of the torsion elastic moduli of the various hinge types and performance comparisons between the different designs. The necessary test apparatus would apply forces on the order of tens of micronewtons to an extremely small area on the edge of the micromirror. It would then need to measure either the displacement of the edge of the mirror, permitting calculation of the angle using the known mirror length, or simply measure the angular deflection directly.

After attempts to obtain a microhardness tester to use for this purpose and a number of design iterations, the final design for a micro-force applicator was a turntable arm with an extremely fine needle mounted on one end, and a depth micrometer mounted on the other.

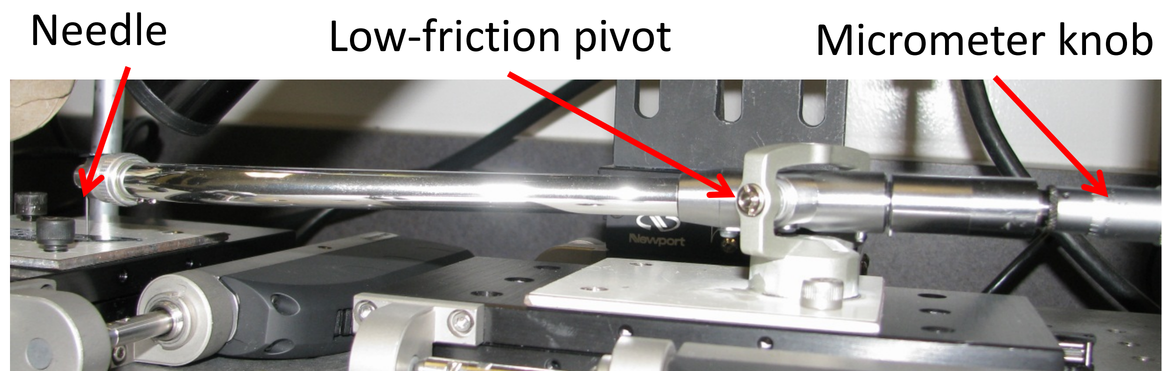


Figure 26: Turntable arm used to apply micro-forces.

The motion of the micrometer barrel causes the micrometer to extend and retract. This extremely fine motion along the center axis of the turntable arm creates a small change in the moment at the pivot. To compensate for this change in moment, a small reaction force develops at the needle, which can be used to actuate the mirror devices.

To calibrate the turntable arm, the needle was placed on a very sensitive scale. One division on the micrometer (corresponding to 1 micron of travel of the micrometer) produced approximately 38 micronewtons of force at the needle, permitting 38 micronewtons of force resolution applied to the device.

The turntable arm was positioned such that the top of the arm would be parallel to the floor when resting on the surface of a flat silicon wafer. A small mirror was mounted on the arm above the needle; when the force from the needle caused torsion in a micromirror device, this mirror would sink down toward the wafer a distance equal to the deflection of the micromirror device. By bouncing a laser beam off of this mirror and into a position sensitive detector (PSD), the deflection resulting from a known applied force could be recorded as a change in voltage.

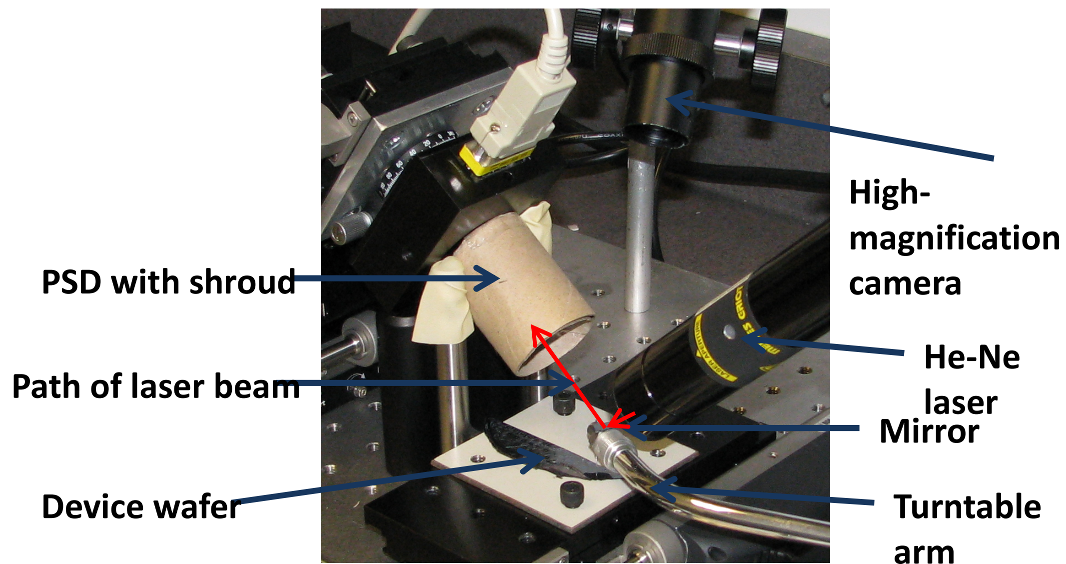


Figure 27: Optics of test apparatus.

4.2 Test Methods

In order to enable the accurate placement of the force needle on the edge of the micromirrors, a high-magnification video camera was focused at the landing point of the force needle, and stepper motors were used to position the device wafer beneath the needle. Once alignment was satisfactory, the turntable arm was set to the desired force using the micrometer, and lowered onto the device by slowly raising a vertically-positioned stepper motor and allowing the arm to rotate to contact the micromirror. This kept the arm from oscillating and ensured an accurate application of force.

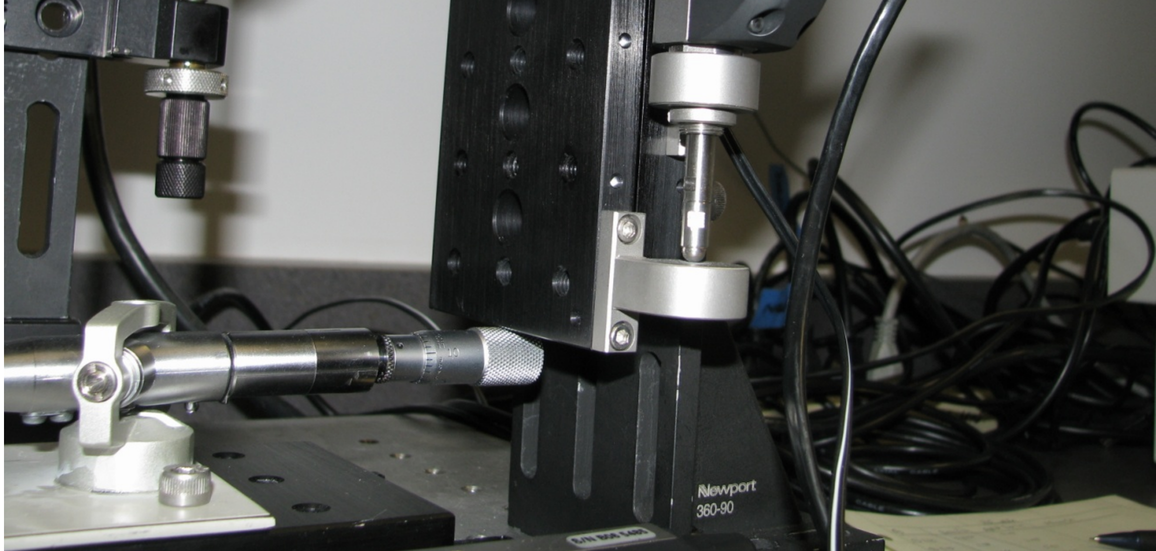


Figure 28: Stepper motor being used to slowly raise and lower the turntable arm and force application needle.

Once the needle was in full contact with the test device, the deflection of the device could be recorded as an output voltage from the position-sensitive detector. The change in voltage from the undeflected neutral point would correspond to a linear displacement on the face of the position-sensitive detector.

Because the position-sensitive detector had a correspondence of 1 millivolt to 1 micron vertically on the detector, the change in voltage, measured in millivolts, due to the applied force was approximately equal to the displacement of the mirror, measured in microns.

If the tip of the force needle was placed approximately at the edge of the device, the length of the mirror could then be used to find the deflection angle.

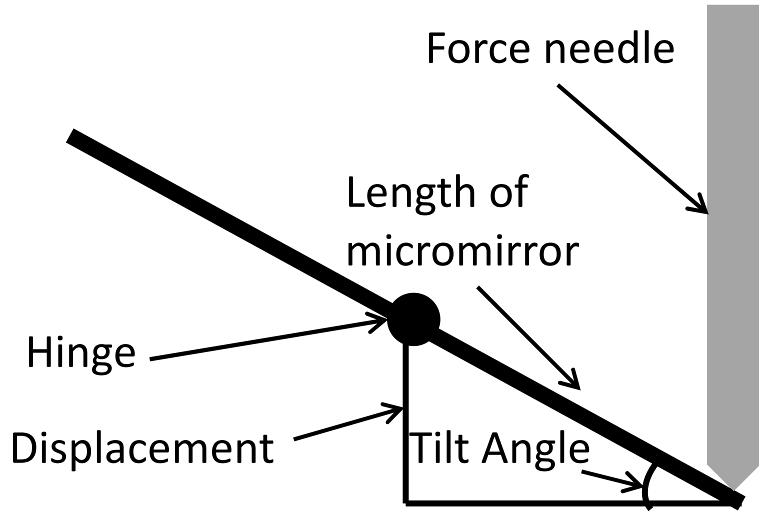


Figure 29: Relationship between tilt and displacement.

Assuming the case of a micromirror with a 2 mm footprint (i.e. a 1mm length from the pivot to the edge of the mirror), and a displacement of 5 microns (5 mV from the photosensitive detector), the angle would be

$$\theta = \sin^{-1}\frac{Displacement}{Length} = \sin^{-1}\frac{5\ \mu m}{1mm} = 0.3° \qquad \text{(Equation 5)}$$

Since the applied force is known from the micrometer, it is then possible to calculate the elastic torsion modulus, $\kappa = \frac{\tau}{\theta}$ [8]. First, however, the torque must be found, again assuming the applied force is at the edge of the device.

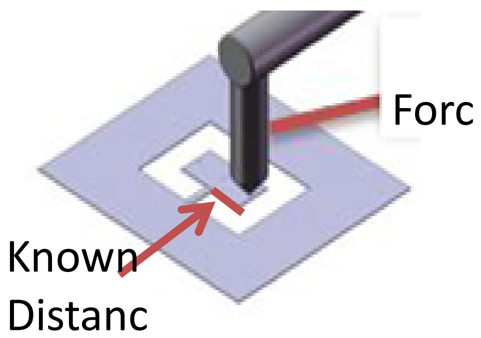


Figure 30: Calculating torque on a micromirror.

The torque is then $\tau = Fd$, and the torsion elastic modulus can be written as

$$\kappa = \frac{Fd}{\theta} \qquad \text{(Equation 6)}$$

Where F is the force applied with the needle and set with the micrometer, d is half the device “footprint” (Table I), and θ is the tilt angle calculated with Equation 5.

It should be noted that this method is only an approximation, since there is a resultant force as well as a torque about the hinge. Therefore the displacement used in calculating the tilt angle involves a component produced by the vertical flexion of the hinges downward. The results from the FEA model suggest this component is small enough to neglect for the straight-beam devices, but it is not clear that this would be an appropriate assumption for the serpentine-hinged devices.

Ideally, calculation of the tilt angle would be accomplished through a direct optical measurement of the device surface, and not by measuring the displacement of the edge.

5. Preliminary Results

5.1 Overview

All seven device types were successfully fabricated, and no defects or artifacts of the processing method were visible, an improvement over previous devices (see Figure 4). One sample device from each design was selected and inspected under an optical microscope. All planar device geometries were within 5% of the design specification and mask dimensions. Thickness could not be effectively measured, although the nominal thickness of the SOI device layer was 10 microns. No obvious film strain or warping was visible. The relative mechanical properties of straight-hinged and serpentine-hinged devices could not be established due to limitations in the testing equipment.

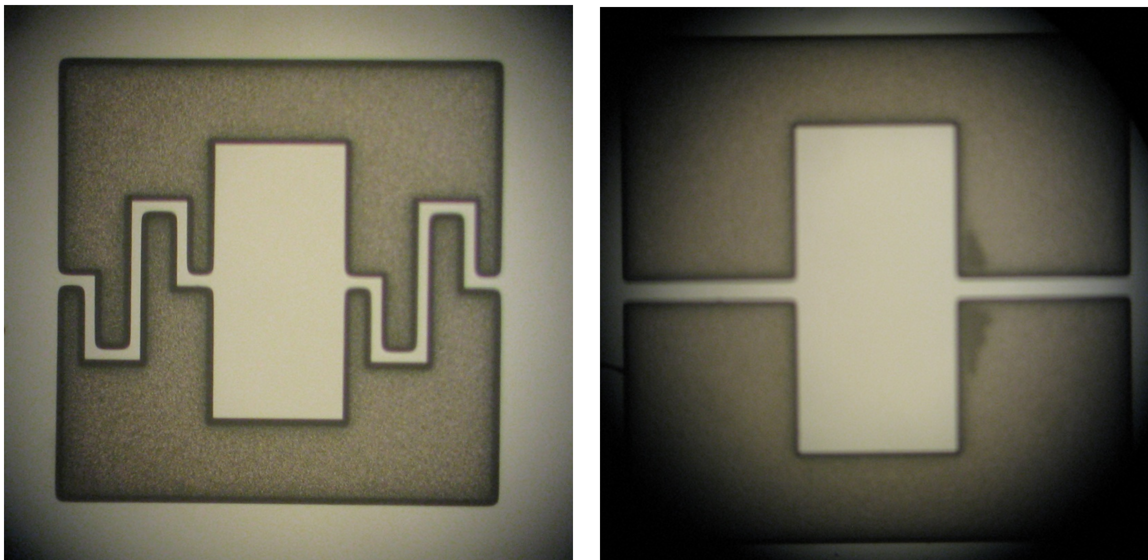


Figure 31: Optical microscope images of completed devices of design #1 (left) and design #2 (right).

5.2 Testing Difficulties

It was recognized that the test setup for measuring the actuation angle of the devices was not suitable to gather data on applied force vs. tilt angle. The poor repeatability of data was believed to result from a variety of issues:

1) Placement of the force application needle anywhere except the exact edge of the mirror would produce a varying range of moments about the hinges, and therefore a varying range of deflection angles.
2) Placement of the force application needle anywhere except the exact edge of the mirror would make accurate trigonometric calculations of the deflection of the device based on the movement of the force arm mirror impossible, since its distance from the device's rotational axis would be unknown.
3) While calculations allowed the vertical displacement of the force arm mirror to be related to the displacement of the mirror (assuming placement of the needle on the exact edge of the device), it was extremely difficult to account for the tilt angle of the force arm mirror.
4) The precision of force applied was only as exact as the calibration and ability to manipulate the micrometer allowed, which was questionable.
5) Electronic noise from the PSD and amplifier made it difficult to resolve small deflections; although the devices may have tilted substantially in response to large applied force, the motion of the mirror on the arm was small.

5.3 Process Feasibility

In the sense that the process already described is capable of producing functional devices, it is successful – however, it is not a practical, repeatable method.

The wafers used in the process become excessively fragile, and while the devices themselves seem capable of surviving the processing, the wafers do not. Over 80% of the process wafers ended up snapping before yielding devices. This extremely high scrap rate is unsurprising for two reasons: a total process time in excess of 50 hours per wafer, providing ample opportunities for mishandling, and two 15-hour deep etches, both of which are extremely harsh on the wafer due to pitting around defects and scratches in the oxide. By the end of the second deep etch, the wafers tended to be very brittle, and keeping them intact was a challenge.

The very high scrap rate combined with the $180 price per SOI wafer results in a very time- and cost-inefficient way to produce test devices. A variety of possible solutions to the scrapping problem were considered.

5.3.1 Boron Etch Stop

By diffusing boron into a normal silicon wafer, a boron etch stop can be created to replace the silicon dioxide etch stop of the SOI wafer [22] [23]. This would greatly reduce costs while still providing the benefit of an etch stop, although the device thicknesses would be more difficult to control.

5.3.2 Deep Reactive Ion Etching

Another option would be to cut deep chemical etching out of the process entirely, and use deep RIE (DRIE) instead; however, this would be associated with significant cost, since SF_6 is a very expensive gas, and RIE components can wear quickly. Still, DRIE is a common technique frequently used in MEMS processing, and with the correct process parameters, etch rates significantly higher than 2.2 microns per minute may be obtainable [21]. A boron etch stop could still be combined with DRIE through the use of optical emission spectroscopy, although the etch rate of DRIE is predictable and uniform enough to simply calculate the appropriate etch time.

5.3.3 Electrostatic Discharge Machining

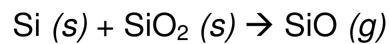
Silicon cannot easily be mechanically drilled because it has a propensity to shatter [24]. Rather than using a drill to create fine holes, electrostatic discharge could be used create small holes in a silicon wafer [24] [25]. Using a rotating tungsten electrode and about 200 volts of bias, it is possible to use sparking to bore a hole 50 microns or less in diameter through a 400 micron-thick wafer in less than two minutes [26] [27]. This would not only enable alignment without the need for an initial15-hour deep etch step, it would create holes small enough to permit alignment using the lithography microscope.

5.3.4 Improved Deep Etch Mask

The fragility of the wafers following repeated deep etch steps was substantially a result of etch attack of the substrate through microscopic pinholes in the oxide. These pinhole defects are formed for a variety of reasons, including particles on

the wafer surface, metallic impurities in the furnace, and evaporation of the native oxide before reaching process temperatures.

To address these concerns, a range of techniques could be employed. Perhaps most simple is the inclusion of a small amount of oxygen (2-3%) in the nitrogen atmosphere during the ramp to process temperature. The primary reason for this is to avoid the evaporation of the native oxide. In an inert atmosphere above 600℃, the following reaction proceeds:



As the native oxide evaporates, voids are created in the film. The resulting surface defects contribute to pinholes [17].

As an additional benefit, the introduction of a small amount of oxygen during temperature ramp will allow any organic impurities on the surface to be converted to CO and CO_2.

The wet oxidation method employed to reduce processing time reduces oxide density and produces more defects in the oxide, partially as a product of the higher growth rate, and partially as a result of impurities introduced by the steam. In order to mitigate the impact of the lower-quality wet oxide, it could be useful to begin the oxidation process by forming a high-quality dry oxide. This could allow the higher performance of the dry oxide as an etch mask to be enjoyed without sacrificing thickness.

It has been reported that chlorine introduced to the atmosphere of an oxidation furnace (as HCl) is incorporated into the film and serves to getter metallic impurities [17]. The lower concentration of metallic impurities leads to a lower concentration defects and voids in the film. However, this method is less useful for wet processes than for dry processes. Steam reacts more aggressively with the metal impurities than HCl, and also causes oxide growth that is too rapid to include a substantial amount of chlorine in the film. It could be useful for improving the quality of the bottom dry layer in a dry/wet process.

Alternatively, silicon nitride could be used as the deep etch mask for the alignment marks. Although the Cal Poly cleanroom does not possess the equipment needed to deposit silicon nitride, it is possible to purchase wafers with the nitride pre-deposited. Patterning could be achieved with the same Teflon one-sided etcher and buffered oxide etchant used for the silicon oxide.

5.3.5 Non-planar Deposited Devices

Instead of seeking a solution to the deep etch difficulties, a wholly alternative processing method could be developed. Rather than forming micromirrors by etching into the silicon, free-standing micromirrors that rise up from the silicon substrate can be deposited onto the wafer. This permits electrostatic actuation with simple circuits in the wafer below. Most commercial micromirrors have been created this way; although most use Chemical Vapor Deposition (CVD) processes unavailable at Cal Poly, electrodeposition and sacrificial photoresist processes have been used to create 3-dimensional structures [28].

6. Re-evaluation of Scope and Objectives

6.1 Decision to Explore a New Device and Process

Of the methods considered for improvement in Section 5.3, creating a new process for depositing non-planar devices appeared to hold the most promise for improving yield, broadly improving performance, and reducing the difficulty of gainfully testing the associated devices.

6.1.1 Postponement of Mechanical Testing

Since significant difficulty was experienced with mechanically actuating the planar silicon devices and measuring their deflection, we decided to wait until the new process yielded devices, and compare the beam and serpentine hinges on those devices. Electrostatic actuation would facilitate testing, since no external apparatus would be necessary to apply force, and the deflection angle resulting from an applied voltage could be measured by bouncing a laser beam off of the device surface and into a photosensitive detector.

Previous students had bonded the silicon devices to a glass substrate with electrodes already deposited onto it, in order to facilitate electrostatic testing. However, this was considered disadvantageous compared to a one-process solution, since it was reported to produce poor device/electrode alignment and poor consistency in device-electrode spacing distance. Both of these limitations seriously complicate effective comparison of device performance.

6.1.2 Reduction of Viscoelastic Effect

Steven Meredith and Dylan Chesbro reported viscoelastic behavior of the micromirrors when 100-150nm layers of gold, aluminum, and aluminum-titanium were deposited via physical vapor deposition [9] [10]. Viscoelasticity refers to the phenomenon of coincident viscous and elastic deformation. Figure 32 illustrates the various responses of materials to stress. A perfect elastic response demonstrates a linear Hookean relationship, a perfect plastic response shows no strain recovery upon unloading of stress, an elastic-plastic response shows some characteristics of each, and a viscoelastic response shows hysteresis that occurs as a product of gradual stress relaxation while under load.

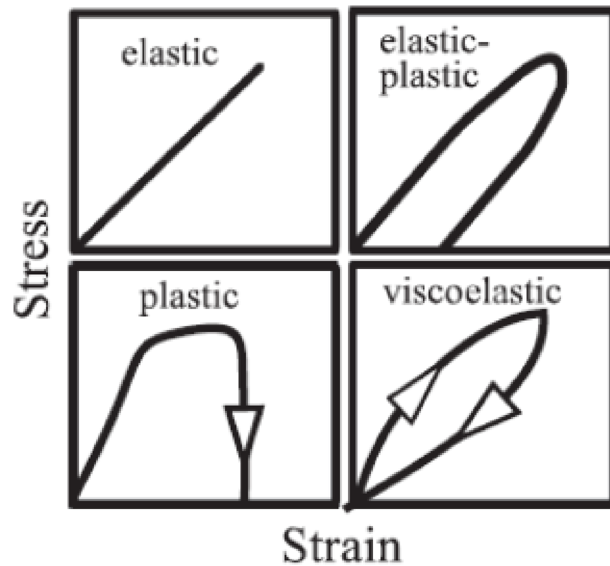


Figure 32: Stress-strain plots by material type [29]

The stress relaxation effect is of the greatest interest within the scope of this thesis. Figure 33 demonstrates the response of a hypothetical viscoelastic material to a loading that is periodically increased but otherwise constant.

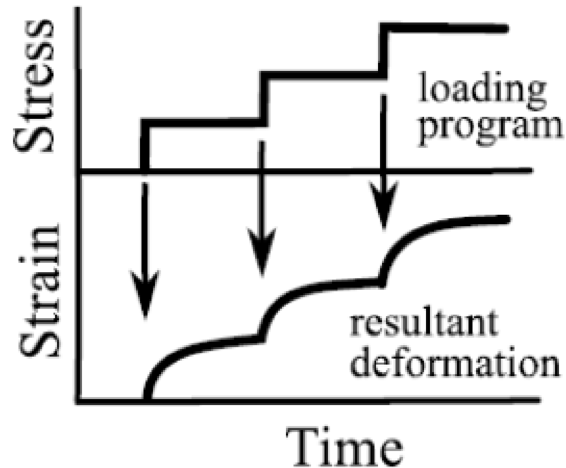


Figure 33: Loading of a viscoelastic material [29]

For the previously-studied mirrors, about 99% of the deformation was instantaneous and 1% occurred over a 33-second hold period.

Still, because it is important for the devices to exhibit a near-instantaneous and repeatable response to applied force, the viscoelasticity is undesirable. A 1% drift in deflection may be beyond tolerance for a projection application. Two mechanisms have been proposed as the cause for the viscoelastic response for the metal deposited onto the micromirrors [9].

The first is the motion of point defects along grain boundaries. When the material is placed under stress, point defects begin to diffuse along grain boundaries until they encounter a “triple point”, the intersection of three grains, where the defects pile up.

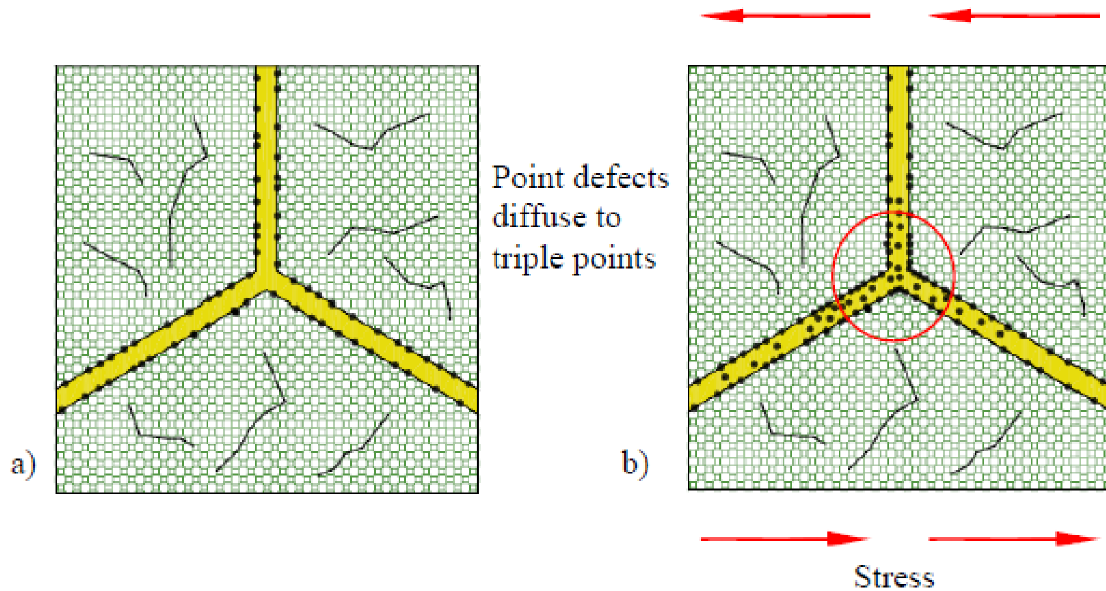


Figure 34: Capture of point defects at grain boundary triple point [9]

After stress has been applied to the material for a sufficient period of time, the concentration of point defects at the “triple points” reaches equilibrium. Releasing the stress allows the defects to diffuse back out of the “triple points”, and the device to eventually recover to its neutral state. Although longer grain boundaries permit point defects to travel further, the dominant factor is the amount of grain boundary surface area per unit volume, and the viscoelastic effect contributed by this mechanism is inversely proportional to grain size [9].

The second mechanism is the bowing of dislocations inside the grains. A dislocation that is pinned at two points will bow outward under applied shear stress, as atoms and vacancies diffuse into the dislocation from adjacent sites. As bowing decreases the radius of curvature of the dislocation, tension along the dislocation increases and eventually reaches a maximum equilibrium value dependent on the applied stress. This tension provides the means for the dislocation to recover to its original state, allowing the device to eventually do so

as well. For a given shear stress, the magnitude of this mechanism's effect is proportional to the dislocation concentration in the grains, and inversely proportional to the concentration of precipitates that limit dislocation bowing [9].

The selection of a reflective material to use for the device itself could eliminate the need for the deposition of a reflective PVD layer. Further, an appropriate material and deposition process will minimize the grain boundary surface area per unit volume and reduce the concentration of dislocations, thereby minimizing viscoelastic behavior.

6.1.3 Improvement of Achievable Electrostatic Deflection

Previous electrostatically actuated devices at Cal Poly were fabricated using a process similar to the planar method of Section 3. The completed devices are suspended by their hinges over a window etched through a silicon wafer, and rotate into this space. Placing electrodes for electrostatic actuation below the devices would therefore limit the device-electrode spacing to less than the thickness of the wafer, which is typically on the order of 400 microns.

Recalling Equation 1, the parallel-plate force equation,

$$F_d = -\frac{\frac{1}{2}(\varepsilon_r \varepsilon_0 W L V^2)}{d^2} \qquad \text{(Equation 1)}$$

It is clear that the force on the devices is inversely proportional to the separation distance. For a mirror only a few hundred microns on a side, a 400 micron separation distance is in fact so great a distance that the parallel-plate

approximation begins to break down due to fringing effects at the edges. It would be of substantial benefit to find a way to reliably reduce this separation.

The most straightforward method, and the one used by previous students [10], is to use spacers only a few tens of microns tall so that electrodes may be placed above the devices while still permitting rotation. However, attempting to mount the devices upside-down onto the spacers produces difficulties with alignment, consistency in parallel-plate separation distance, and the risk that the devices may discharge by tilting into the electrodes.

A nonplanar method alleviates these difficulties by integrating the device and electrodes onto one substrate. The device-electrode separation distance can be arbitrarily selected to maximize tilt, and the electrodes can be designed in such a manner that the device will not discharge upon deflection into the substrate.

6.1.4 Improved Thickness Control

The planar process adopted the SOI wafer in order to solve the difficulties previously experienced minimizing variation in the device thickness. However, SOI wafers are expensive, and the SOI wafers were only available in top layer thicknesses of either 10µm or 20µm. These both produce unnecessarily thick device layers. Although thick hinges help prevent breakage during processing and vertical displacement during actuation, they also seriously impede torsion. Freedom to adjust the device thickness enables selection of the optimal balance between risk of breakage, vertical displacement, and ease of torsion.

A process that creates the device layer via deposition rather than material removal will not need an etch-stop, so the SOI wafer becomes unnecessary.

Furthermore, since device thickness would become a parameter controlled by the length of the associated deposition step, it would become possible to mechanically test devices of different thicknesses using the same process and lithographic masks.

6.1.5 Development of New Process Capabilities

The ability to create the planar devices was a product of institutional knowledge and the efforts of previous students. A constant goal of the Cal Poly Microfabrication Lab is to enhance and extend the processing techniques and capabilities for future use.

Since the successful implementation of the planar silicon process has been repeatedly demonstrated and iteratively improved over the past several years, this goal is best served by the development of a new process. PVD is the only existing process in the Microfabrication Lab which is capable of thick conductive film deposition, and its use is undesirable for thick films because of expense, film stress, and thermal effects. Further, no deposition process (PVD included) has been used on a sacrificial layer with the intention of creating a hinge structure. As will be discussed later (see Section 7.1), PVD is not appropriate for this application without a corresponding CMP step.

6.2 Revised Device Constraints

Devices deposited out of the wafer plane and actuated by electrodes below have an entirely different set of design constraints from planar silicon devices. An accurate accounting of these differences was necessary before designing the new devices.

Note that “device” in the context of the out-of-plane design generally refers to only the elements lying in the plane of the mirror, such as the mirror surface and hinges, not the supporting pillars or electrodes. The requirements for the support pillars and electrodes will largely be determined by the design selected for the mirror and hinges.

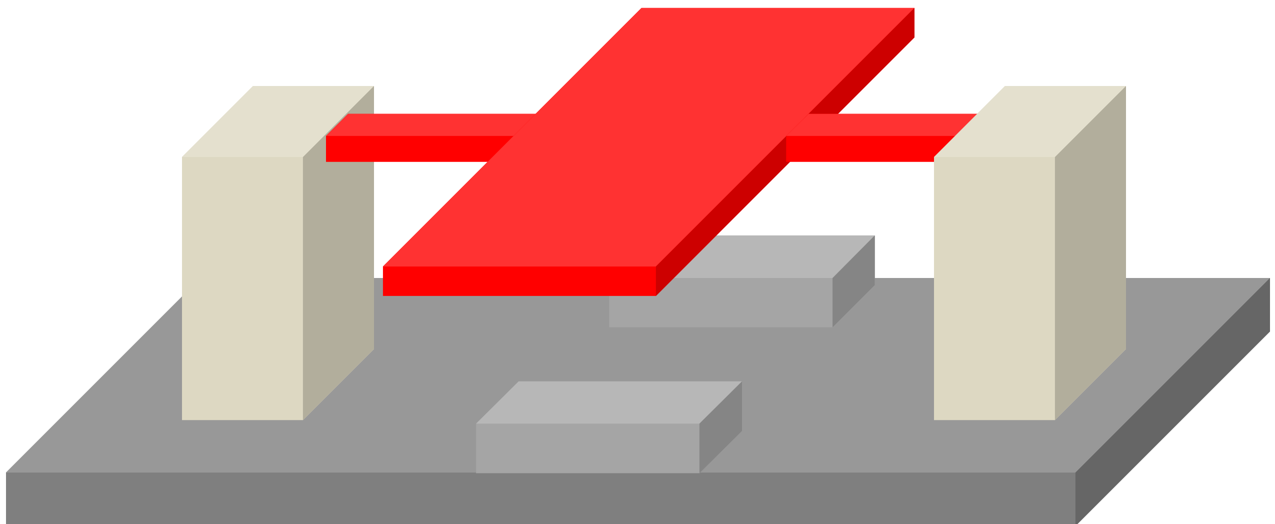


Figure 35: Hypothetical mirror device shown in red

6.2.1 Minimizing Voltage Required for Mirror Tilt

Achieving a large tilt in the mirror device remains one of the most important design objectives. Although the amount of voltage applied to the electrode may be increased arbitrarily to generate the torque necessary to obtain the target 10°

of tilt, a high applied voltage is undesirable and all design parameters must be selected such that the voltage necessary is as small as possible.

A high applied voltage is undesirable for several reasons. One is that a higher actuation voltage results in much greater energy use. The amount of energy stored in a capacitor at full charge, U, is given as follows,

$$U = \frac{CV^2}{2} \qquad \text{(Equation 7)}$$

where C is the capacitance, determined by the geometry and dielectric material of the capacitor, and V is the applied voltage. Clearly, the energy required to obtain a single actuation of a mirror device is proportional to the square of the voltage necessary to actuate it. Toward commercial applications, minimizing the energy per actuation is critical in order to avoid device overheating and excessive power consumption, as well as the expense of integrating a power supply capable of delivering high current at high voltage.

Furthermore, if the applied voltage is too high, the device may discharge to the actuating electrode. Besides damaging both the device and the electrode, discharge will cause the electrostatic force to temporarily drop, and therefore the device to spring back. As the voltage recovers, the electrostatic force will again tilt the device down, permitting it to discharge again, and creating an oscillatory loop that will create serious instability in the tilt angle. Either the device or the electrode – depending on which is the cathode – will quickly be destroyed by arc

sputtering. The voltage at which this discharge occurs is the breakdown voltage, given by Paschen's Law [30],

$$V = \frac{apd}{\ln(pd) + b} \qquad \text{(Equation 8)}$$

where a and b are constants specific to the particular gas, p is the ambient pressure, d is the gap size, and V is the breakdown voltage. Figure 36 shows the Paschen curves for common gases, all of which exhibit a characteristic minimum discharge voltage at some value of pd. For air, the minimum discharge voltage is 327 V, and the corresponding value of pd is 0.567 $torr \cdot cm$ [31]. Therefore, given an ambient pressure of p = 1 atm = 760 torr,

$$d = \frac{0.567\ torr \cdot cm}{760\ torr} = 7.46\ \mu m \qquad \text{(Equation 9)}$$

At the size scale of these micromirror devices, it is nearly a certainty that the electrode-mirror separation will be $7.46\ \mu m$ at some point during the device actuation.

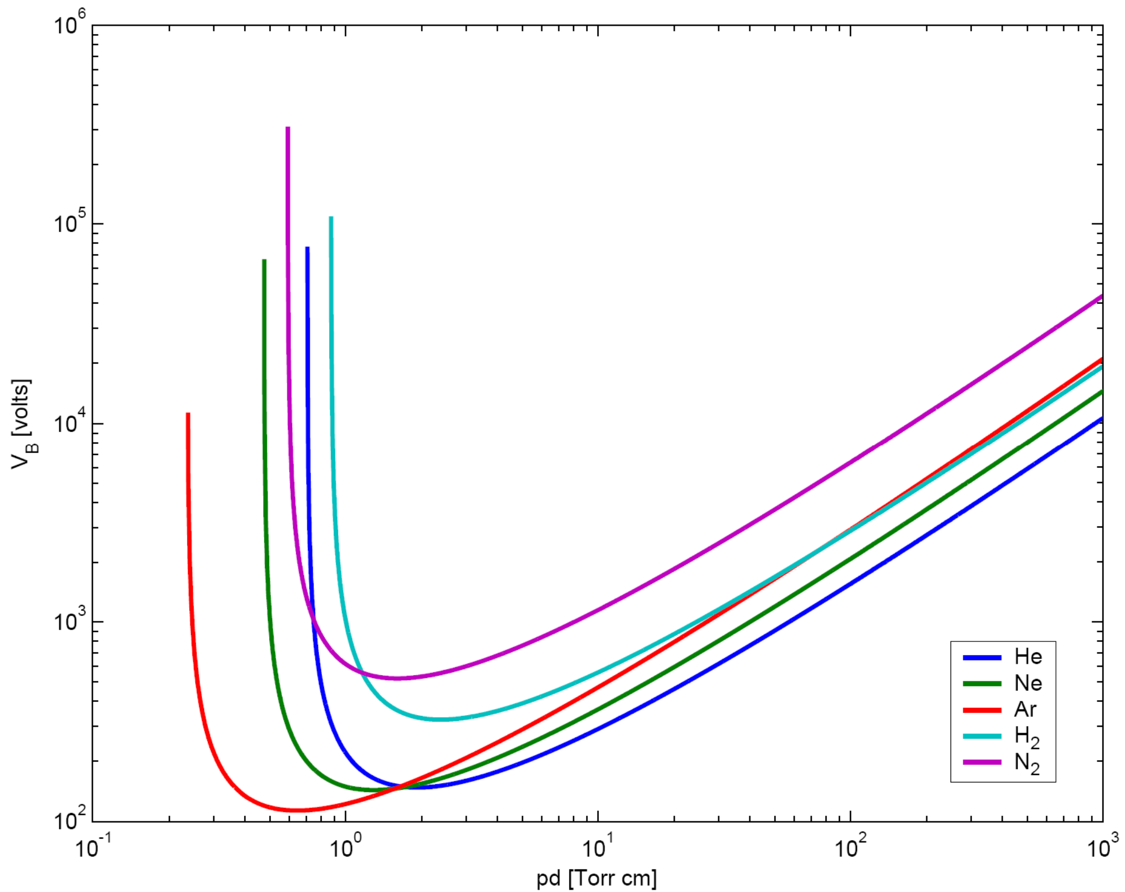


Figure 36: Paschen curves of common engineering gases

This makes 327 volts the absolute maximum permissible voltage for actuation. Compensating for unexpected effects, such as transient overvoltage and greater fields at sharp geometric corners, would suggest a maximum design voltage substantially less than 327 volts.

Keeping voltages low also helps reduce safety concerns, particularly given the high currents ideal for quickly charging and actuating devices.

It is with the ultimate goal of reducing necessary voltage that serpentine micromirrors are explored as an alternative to straight-beam micromirrors, as they reduce the torque needed to obtain a 10° tilt.

6.2.2 Device Thickness

In the planar micromirror process, the SOI wafer constrained the device thickness to either 10 or 20 microns, depending on the wafer specification. For the out-of-plane design, the device layer is deposited, and so the thickness can be controlled by varying either the deposition time or deposition rate.

However, there are some limits on deposited device thickness. Although a thinner device will reduce the torsion elastic modulus of the hinges, it also will make the devices more fragile and prone to breaking during processing. As a result, thickness will be constrained to be no less than 5 microns. If high yield can be demonstrated for 5 microns of thickness, thickness can be reduced for future devices in to improve performance.

Additionally, there is a practical upper bound to the thickness, although it is unlikely it will be desirable to design a device so thick. Because the sidewalls of the device will be defined during deposition by a photoresist “mold” (see 9.5 Photoresist Constraints), processing difficulty increases beyond about 20 microns and becomes nearly impossible beyond about 40 microns.

Finally, because the hinges and the mirror are co-deposited, they must be of equal thickness.

6.2.3 Beam and Mirror Geometry

The mirror cross section must be rectangular, because the fabrication process is limited to producing vertical sidewalls and planar surfaces. This also applies to the hinge cross-sections.

Also, the mirror shape must be rectangular, with the hinges centered along the long side. Although functional mirror devices could be constructed out of a variety of different axially symmetric shapes, a rectangular device is the most efficient use of space for a 2-dimensional device footprint.

It is worth noting that the mirrors in commercial TI DMD chips are square, with the hinge axis placed along the square's long axis. This enables ultra-dense packing of the devices. However, it is enabled by the 3-layer device design; the hinges are located on the second layer, and the mirror is the third layer, connected to the yoke on the second layer (see Figure 3). Although the process may be eventually capable of producing 3-layer devices (see 6.3.1 Layer Iterability), the initial device will use a more conservative 2-layer design. Therefore the rectangular footprint is more appropriate.

Finally, several device designs must be created to fabricate otherwise identical designs with hinges of both straight-beam and serpentine geometries, in order to enable comparison as part of the project objectives.

6.2.4 Device Size

Texas Instruments digital mirror devices are 17µm square. However, to facilitate testing, the initial devices fabricated using this process may be significantly larger: very small devices that contact the run the risk of "sticking" or even pulling in spontaneously due to van der Waals forces [32]. Again, final design improvements are left until after successful process implementation and mechanical testing.

Assuming a particular minimum degree of tilt, there is a geometrical constraint on the maximum mirror length, as a function of the separation of the device from the substrate and the degree to which the hinges “sag” toward the substrate when electrostatic force is applied.

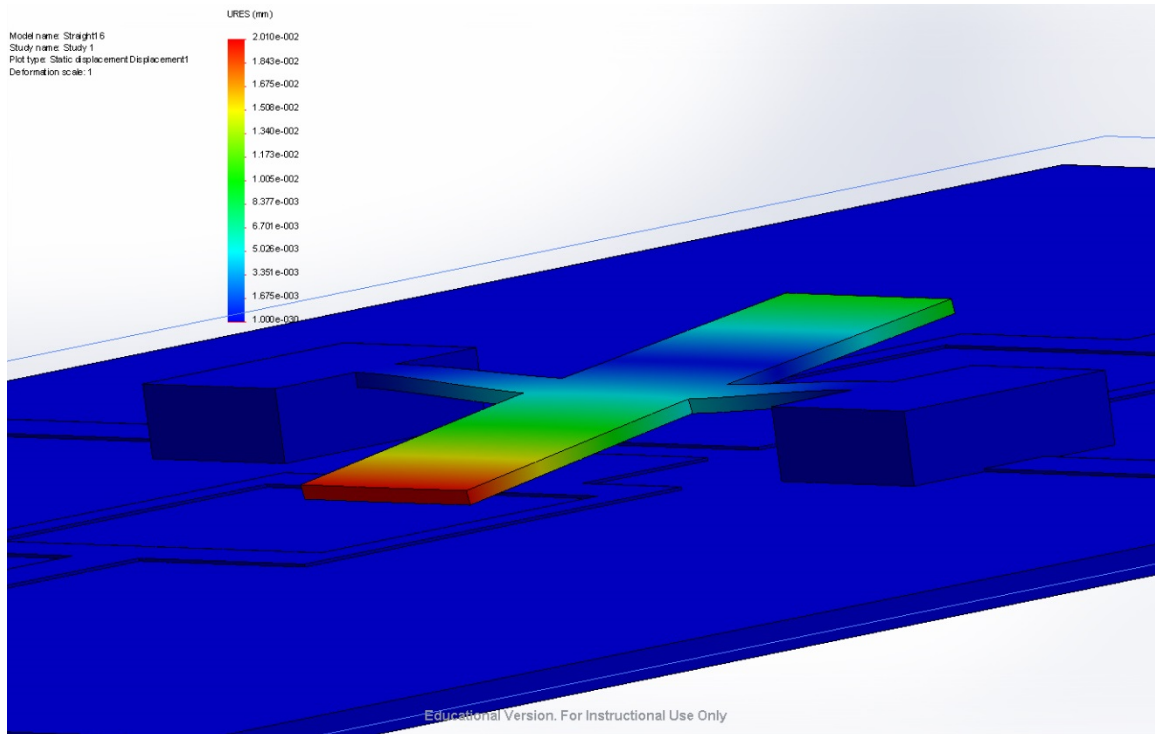


Figure 37: FEA model illustrating “hinge sag” of straight-beam device

A model for this can be expressed as follows, with the assumption that the mirror is a rigid surface:

$$\theta \leq \sin^{-1}\left(\frac{d - \delta_{\max}}{\ell}\right) \quad \text{(Equation 10)}$$

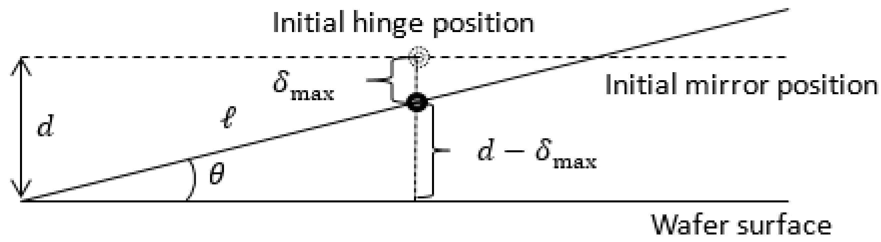


Figure 38: Trigonometric model of maximum mirror tilt

Where θ is the tilt angle, d is the initial distance between the wafer surface and the plane of the bottom of the mirror, $\delta_{\max}$ is the hinge sag, and ℓ is the length of the mirror from the hinge axis. When the device touches the surface, θ is at maximum. If this is set to be the minimum of 10° when the surface is contacted, a relation for the required device parameters can be found:

$$\sin 10° = \frac{d - \delta_{\max}}{\ell} \quad \text{(Equation 11)}$$

Therefore,

$$\ell \leq 5.759 * (d - \delta_{\max}) \quad \text{(Equation 12)}$$

The hinge sag effect is discussed further in Section 8.1.3.

There is no clear limit to the width of the mirror, but when force is applied, a mirror that is too wide may stop acting as a rigid surface and begin to sag, exaggerating the sag of the hinges and seriously deteriorating optical quality. A wider mirror will increase the surface area for the electrostatic effect and produce a commensurate increase in force, exaggerating the risk the mirror will lose planarity.

In order to avoid this effect, the design will maintain the width of the mirror as equal to the length from the hinge axis to either edge of the mirror, i.e. W = ℓ.

As an additional note, increasing the area of the mirror will increase the capacitance of the electode-mirror system, and thus increase its RC constant. This implies it will take take longer to charge and develop the maximum force, which will increase switching time. Therefore it would be desirable to keep the devices as small as practicable.

6.2.5 Electrode Separation Distance

Once again referring to the parallel-plate force equation,

$$F_d = -\frac{\frac{1}{2}(\varepsilon_r \varepsilon_0 W L V^2)}{d^2} \quad \text{(Equation 1)}$$

it is clear that making d, the distance between the device and electrode, as small as possible will be advantageous for reducing the voltage necessary to develop any given force.

There is a complication to the minimization of the electrode separation distance. As was discussed in the previous section, the geometry of the final device must be such that it is physically capable of tilting 10° before encountering a surface.

Rearranging Equation 12 yields

$$d \geq \frac{\ell}{5.759} + \delta_{\max} \quad \text{(Equation 13)}$$

Just as was the case for the device thickness, there is an upper bound (about 20 microns) to the separation distance due to processing difficulties related to the thickness of the photoresist (see 9.5 Photoresist Constraints). Because the size of the device will ultimately demand a large separation distance per Equation 13, the separation distance will ultimately be constrained by the photoresist thickness.

6.2.6 Actuation

Because contact of the mirror with the actuating electrode will cause discharge and ensuing material damage and tilt oscillation, it is important to ensure the mirror can come into contact with the wafer surface without discharging. This means that the electrode, and the conductive traces connecting it to the voltage source, must be placed on the wafer in such a way that the actuating mirror will strike an insulating silicon oxide, and not the traces.

The area of this insulating oxide must be sufficient to ensure that the devices will snap down onto it in all cases, even considering substantial lithographic misalignment and the hinge sag effect.

Additionally, the electrostatic traces on the surface of the wafer must connect to solder pads to facilitate testing, and the hinge structure supporting the mirrors should have traces to facilitate grounding (or device biasing, if desired).

6.2.7 Reflectivity

The surface of the mirror must be reflective, in order to fulfill its primary function and permit testing. The reflectivity across the visible wavelengths should be as uniform as possible, in order to avoid “coloring” the reflections.

Although PVD was used to deposit thin films of reflective materials like aluminum and gold on the surface of the planar silicon devices created by previous students, the deposited films are known to cause an undesirable viscoeleastic response to actuation [9]. Further, PVD as a final step could short the traces necessary for electrostatic actuation on the wafer surface, and potentially cause undesirable thin-film stress, warping the mirror surface. Therefore, PVD deposition of a final reflective layer is not an option; the mirror material must be suitably reflective as deposited.

6.2.8 Conductivity

In order to develop force between the mirror surface and the electrode, both surfaces must collect charge, and so both must be conductive. The greater the resistivity of their materials, the larger the RC constant and therefore the longer it will take to charge the device. In order to permit the device to switch quickly, both the device and its supporting pillars should be formed from material with reasonably high conductivity.

The electrode and conductive traces should also be deposited with a conductive material, such as gold or aluminum, at a thickness suitable to minimize resistivity.

6.2.9 No Yield at Snapdown

When the device has rotated to its full extent and contacted the surface, the stress in the hinges must not be great enough to cause the material to yield. If the material yields, the device will not recover to its original state when the voltage is removed.

Although it is difficult to predict yield behavior at the micromirror size scale because of different behavior in thin films, the risk of device yielding can be reduced by selecting a material that has a high bulk yield stress and by using FEA to determine the maximum von Mises stress of various device designs at snapdown.

6.2.10 Device Density

Because DMDs are primarily used for projectors in commercial applications, they must be placed into arrays, with each individual device representing a pixel. The space on the wafer surface that is not covered by a mirror will appear as dead space on the projection. This “dead space” between pixels is very undesirable and must be minimized for commercial applications.

Because it is not an immediate goal to produce a device array capable of image projection, poor device density is acceptable. However, the device design should be density-aware in such a way that the difficulty of adjusting the design to produce a dense device array in the future is minimized.

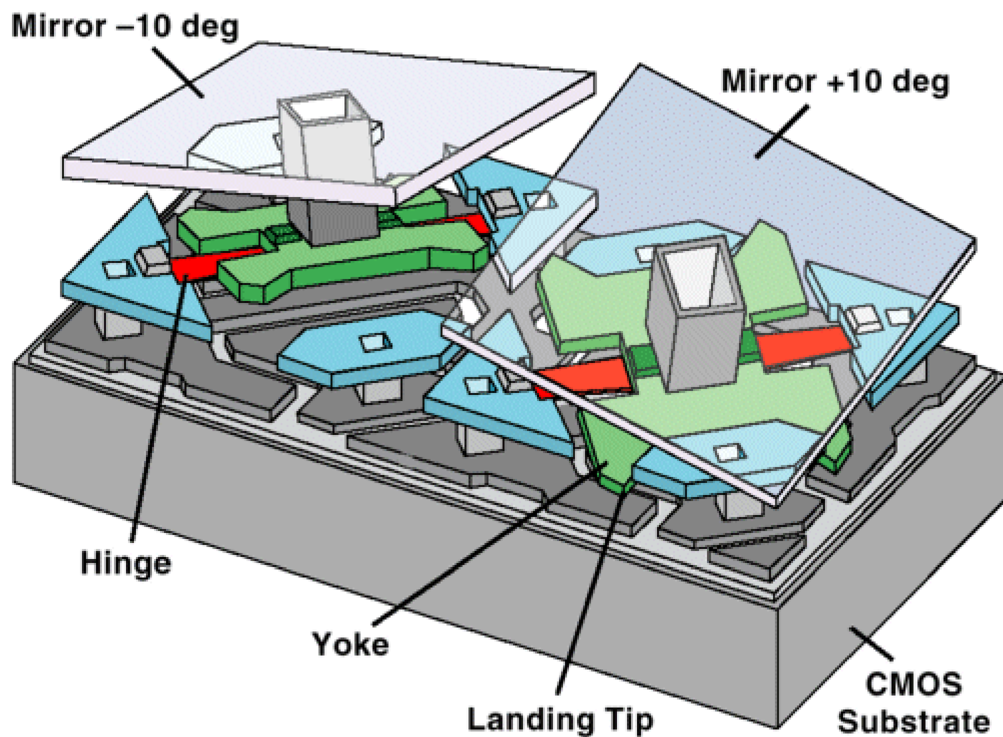


Figure 39: Layout of commercial Texas Instruments DMD

Commercial devices use a 3-layer design in order to achieve nearly 100% device coverage of the wafer surface. The CMOS logic is placed on the first layer, while the electrodes and hinges are placed in the second layer, with the reflective mirror surface placed on the third layer and connected to the hinges assembly in the second [6]. In this way, the mirror surface can cover the hinges.

To achieve similar coverage, the hinges – either straight beam or serpentine - would be connected mechanically to an additional third layer. Although this does not constrain the new design, it carries implications for the process requirements.

6.3 Revised Process Constraints

6.3.1 Layer Iterability

As discussed in the previous section, it is a requirement of the process that additional layers can be added, if desired. This should be achievable without substantial changes to the preceding process flow.

A planar device deposited out of the wafer plane already requires an iterable process: the geometry of the mechanical supports separating Layer 1 and Layer 2 will differ from the geometry of the devices in Layer 2. Therefore, the shape of the “mold” formed by photoresist or other sacrificial material will differ for the deposition of the supports and the deposition of the devices, and the deposition cannot be accomplished in a single step.

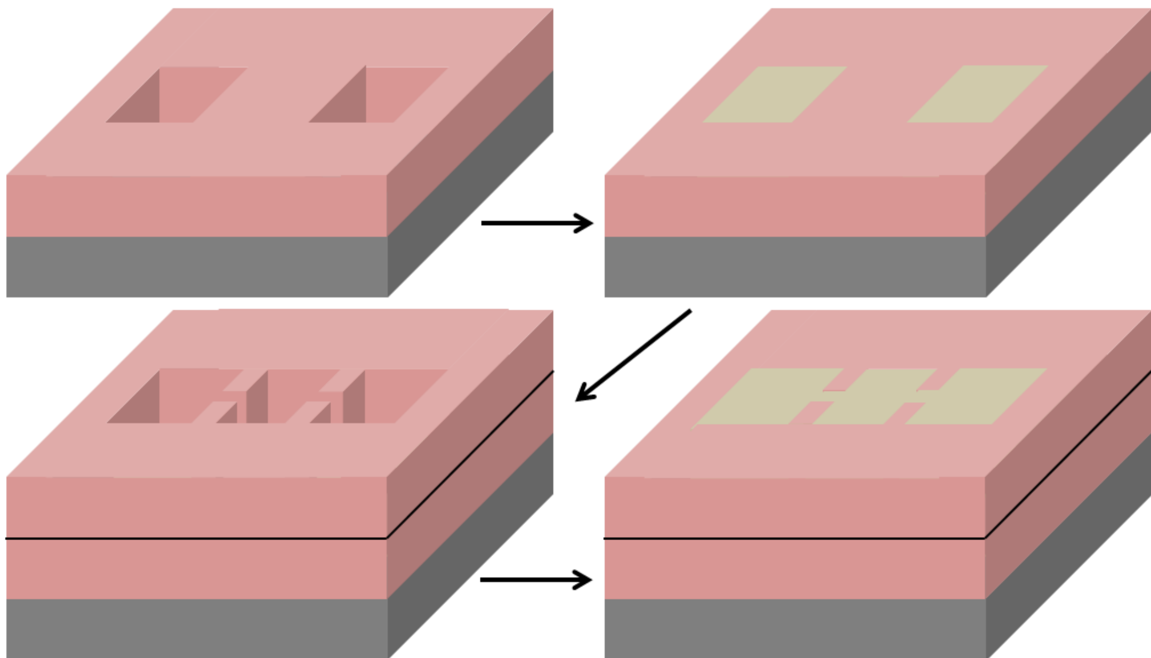


Figure 40: A multi-level sacrificial layer process

Because this implies an additional sacrificial layer must be deposited via spin-coating onto the surface created by the prior step, it is critical that the surface at the end of each deposition step be as uniform as possible, to avoid propagating non-uniformities through each layer. Perfect uniformity of an underlying layer is shown by the black line in Figure 40. Propagating non-uniformity at the end of each deposition cycle will ultimately limit the maximum number of layers.

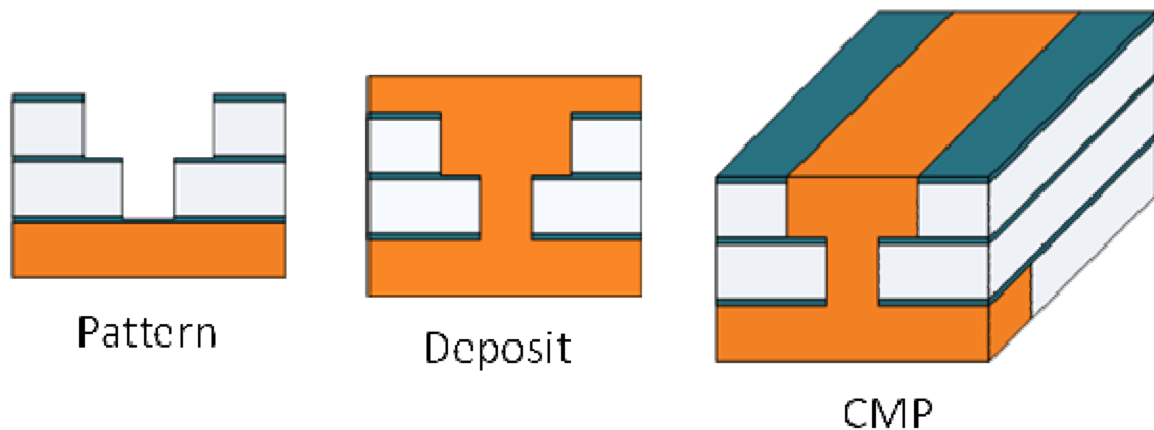


Figure 41: Simplified single damascene process flow

Non-uniformity of sequential layers is controlled in industry by a Chemical Mechanical Polishing (CMP) step. For example, in the damascene process (see Figure 41), excess copper material (overburden) deposited by the deposition step is removed by CMP to leave a smooth surface and copper-filled recesses, so that the process can be repeated [16].

However, the Cal Poly Microfabrication Lab lacks CMP capabilities, and so optimizing uniformity will be necessary to correctly fabricate devices and ensure layer iterability. Still, non-uniformity cannot be eliminated altogether, and if a three-level device is to be fabricated, it will likely require the use of external CMP resources for at least one processing step.

As a guideline for the initial two layer device, the within-wafer non-uniformity (WINWU) of the underlying layer must be no more than 10% of the thickness of the device layer, when measured in several locations.

6.3.2 Thickness Control

Because the deposition process will determine the thickness of the device layer, and because the device thickness is an important parameter for device performance, good control of the thickness of the deposit will be a requirement for successful processing.

The most important factor for controlling the thickness of the deposit is the deposition rate. The deposition rate must be well-established, and must not drift appreciably during the process. Furthermore, the desired length of the deposition step must not be too short, so that deposition can be accurately executed for the desired amount of time. To the extent that process parameters may shift during the process, the process time must also not be too long.

As a general guideline, the process is too short if it is less than 5 minutes.

Because the deposit will form part of the surface for the next deposition step, and since there will be no intermediate CMP process, it is important that the thickness of the sacrificial layer, or deposition “mold”, and the deposit are the same for any process step which is followed by another deposition cycle. If they are not, the surface will not be planar for spin-coating (see Figure 42). To avoid non-uniformity in the spin-coated layer, the mismatch in thickness between the sacrificial layer and deposit should be no more than 0.5 microns.

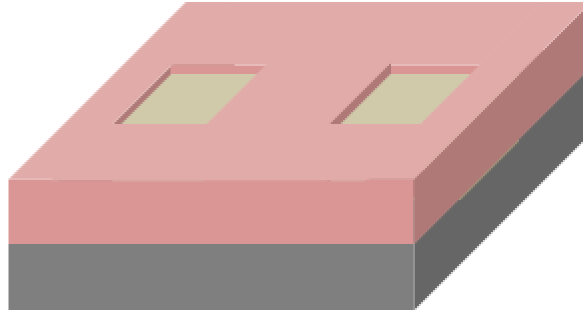


Figure 42: Insufficient Deposit Thickness

6.3.3 Yield

The planar process had a variety of processing issues, particularly a high scrap rate. Scrapped wafers have effectively a 0% yield, and high scrap rates greatly increase the cost and time required to create a functional wafer.

In addition, high yield on completed wafers is important. Modern commercial DLP chips contain arrays of about a million DMDs. A single non-functional mirror will cause a “dead pixel” and an essentially worthless DLP chip. Because a silicon die large enough to accommodate a million or more DMDs is very large, the defect density must be very low to cause zero non-functional DMDs [6].

In order to successfully scale the single mirror design to a mirror array, the process must demonstrate a very high yield rate. Even if the yield is 99% for individual devices, the yield of 10x10 arrays may be as low as 50%.

It is important to note that yield concerns are major motivators for the use of appropriate technology such as CVD and CMP in MEMS processing, and it is very unlikely the process described herein can attain yields approaching those required for commercial processes.

6.3.4 Deposition Methods

Because of the foregoing constraints such as reflectivity, conductivity, and yield strength, the deposited material will almost certainly need to be metallic.

The only established metal deposition process in the Cal Poly Microfabrication Lab is PVD via sputter deposition, which is available for a variety of metals, including aluminum, gold, nickel, chromium, and silver.

CVD is not possible, because the equipment for CVD processing is not present in the Cal Poly Microfabrication Lab, and CVD cannot be accomplished without careful control of parameters such as pressure, temperature, flow, and gas composition.

Wet chemical deposition processes such as electroplating and electroless deposition (ELD) do not have established processes or equipment in the Lab, but may be accomplished with rudimentary beaker batch processing, since most of the process parameters which must be controlled are either chemical, electrical, or thermal in nature. Demonstration of a process using such a makeshift setup will likely be associated with a high defect density due to particle issues, but industrial semiconductor processing tools exist for both electroplating and ELD.

Finally, as mentioned previously, CMP is not available, and any deposition process which requires one or more subsequent CMP steps cannot be explored.

6.3 Summary

Following the difficulties characterizing the mechanical behavior of the planar devices, we concluded that it would be best to postpone mechanical testing and comparison of the devices until a new, non-planar, electrostatically actuated device could be created. The new objectives for this device were:

1) To reduce tilt drift due to viscoelasticity
2) To increase the tilt achievable from low-voltage electrostatic actuation
3) To improve device-layer thickness control
4) To extend the process capabilities of the Cal Poly Microfabrication Lab.

7. Deposition Method Selection

Prior to designing a final process flow, it was necessary to establish the method that would be used for device deposition, since the remaining process steps would depend on this technique.

7.1 PVD

The Cal Poly Microfabrication Lab has several processing tools capable of sputter deposition. Fundamentally, this PVD technique works by accelerating ions of an inert gas into a "target" composed of the material desired for deposition on the substrate. These ions strike the target and physically dislodge the atoms, some of which reach the target and chemisorb on the surface.

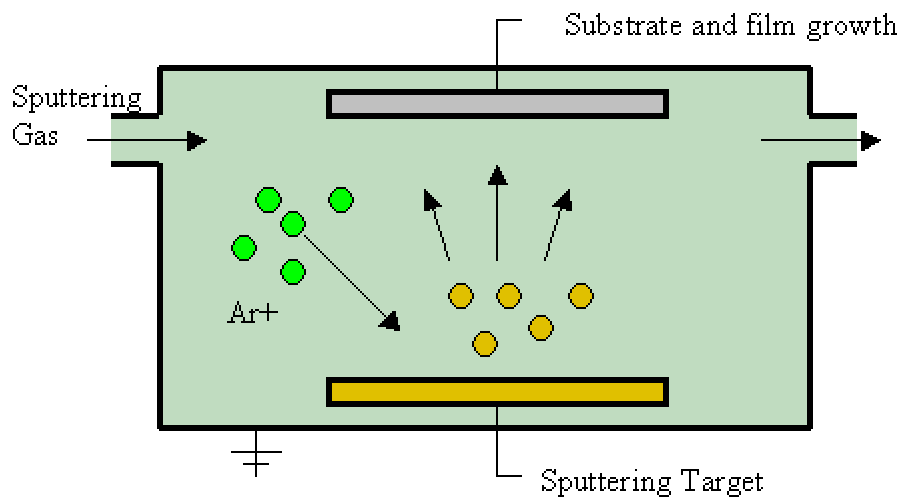


Figure 43: Diagram of sputtering process

The ion source is a plasma generated inside the sputtering chamber, and the ions are accelerated by the negative potential applied to the target.

In the sputtering systems used at Cal Poly, argon is used as the inert gas for the plasma, due to its large mass and therefore greater potential to knock atoms free

from the target [33]. Notably, the Cal Poly systems also make use of magnetron guns. In this configuration, the target is placed in the center of a ring of strong permanent magnets, so that incoming argon ions are “trapped”: when they strike the surface, rather than returning into the chamber plasma, the magnetic field makes the ions much more likely to be immediately accelerated into the target again. While this increases the sputter rate, it also prevents the use of ferromagnetic targets because of interference with the magnetron gun.

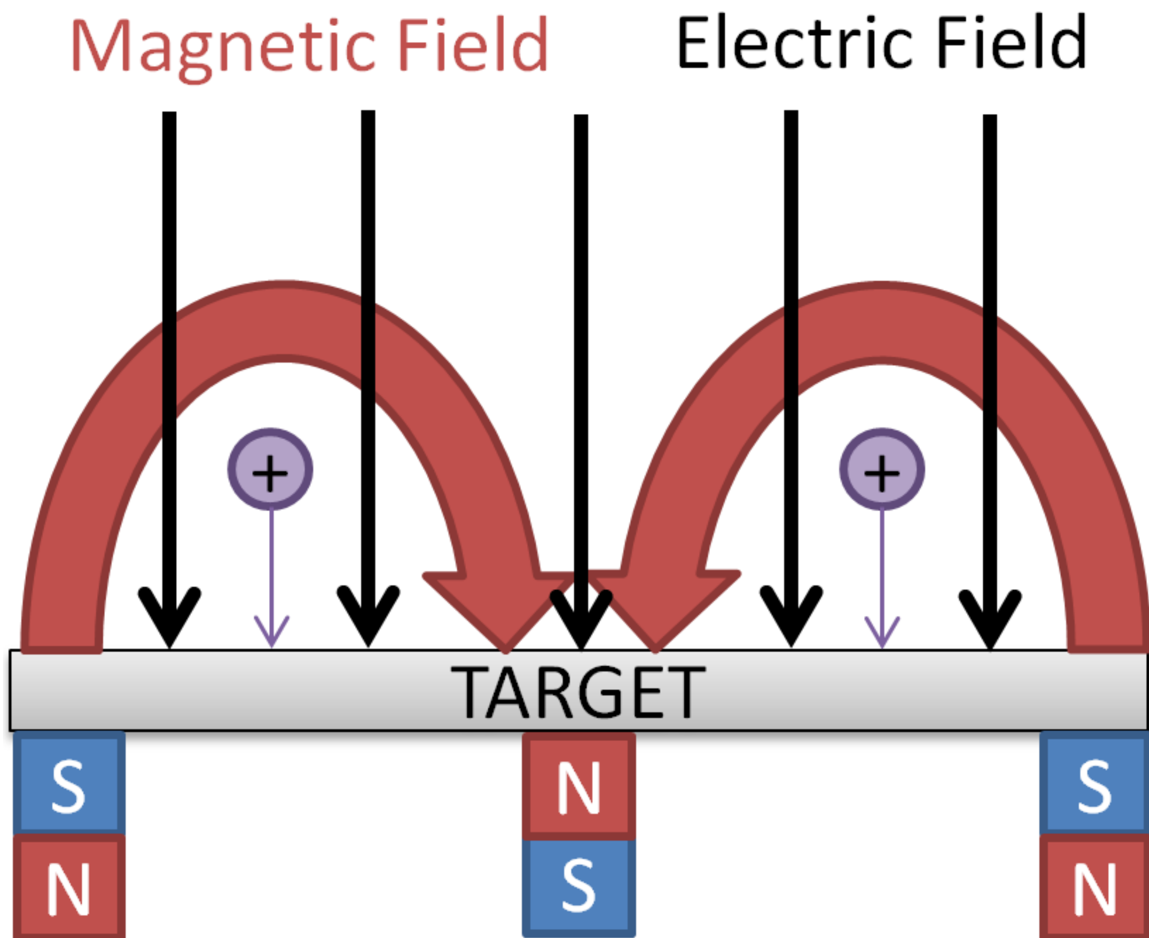


Figure 44: Diagram of a magnetron gun

Work by J. Thornton in 1974 established relationships between sputtering process parameters and the structure of the resulting film [34]. In particular, various combinations of substrate temperature as a fraction of the melting point of the film being deposited (homologous temperature) and the energy of the sputtered ions results in four potential “zones” representing structure of the deposited film.

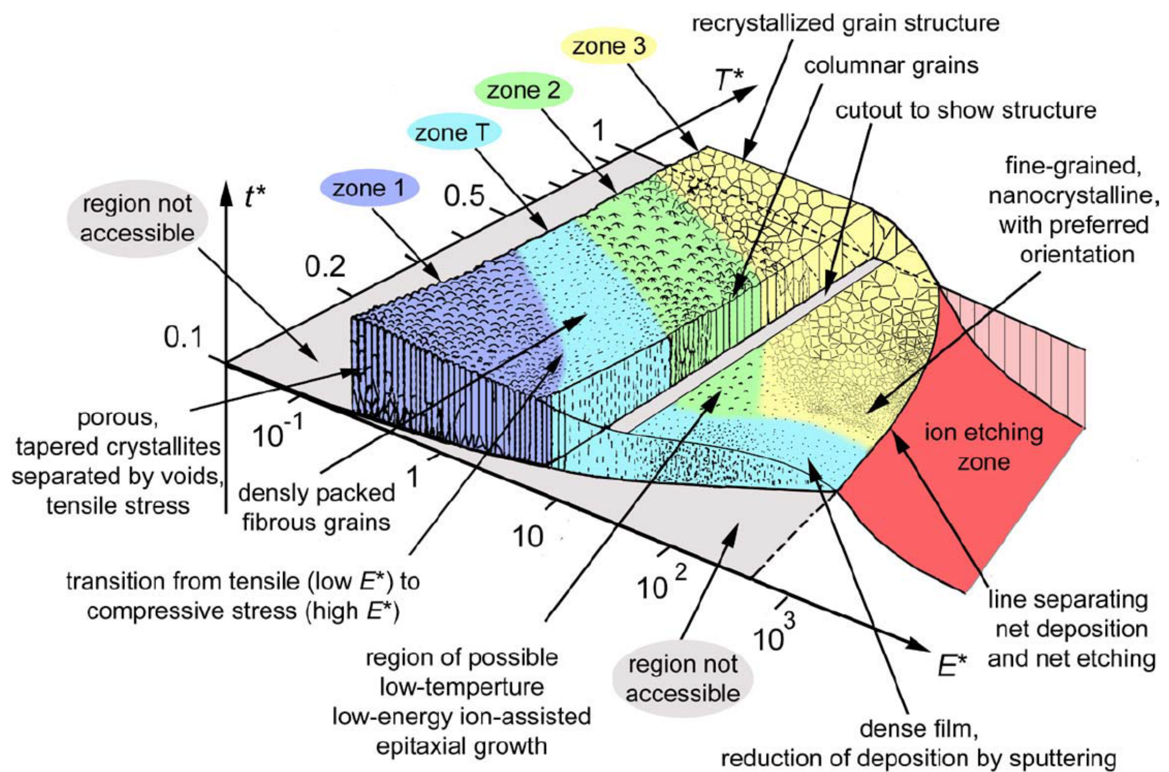


Figure 45: Sputter deposited film structure [35]

Only one of these zones (the “t zone”, light blue in Figure 45) minimizes stress and voids in the film. However, because the Cal Poly equipment lacks direct temperature control of the substrate, over the thick, multi-micron deposition process necessary to form micromirror devices, the heat generated by the process could cause a temperature increase sufficient to cause drift out of the “t

zone" [35]. Even if the process remains firmly within the desired regime, sputter deposited films tend to have high compressive stress that grows with thickness [36], and would likely become unacceptable for a film several microns thick.

Furthermore, a sputter deposited film deposits uniformly on the surface. This raises the question of how the desired hinge structure may be formed. If a uniform metal layer is deposited, an etch mask is deposited on top, and the deposited metal is etched away, severe mask undercut will occur: if the layer is 10 microns thick, it is a reasonable estimation that an anisotropic etchant will undercut the mask by ten microns [16]. This is clearly not suitable for forming the mirror structure.

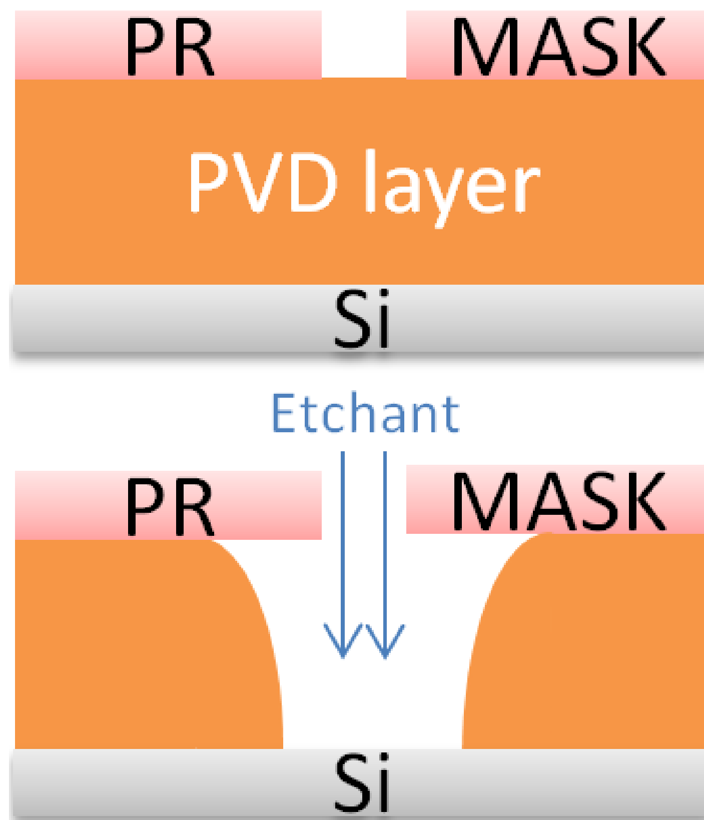


Figure 46: Undercut during etching of thick PVD layer (not to scale)

Depositing onto a sacrificial “mold” is similarly not suitable. As the trenches in the mold are filled, so is the surface of the sacrificial layer covered with overburden.t This makes the surface non-uniform for subsequent steps, and prevents effective removal of the sacrificial layer.

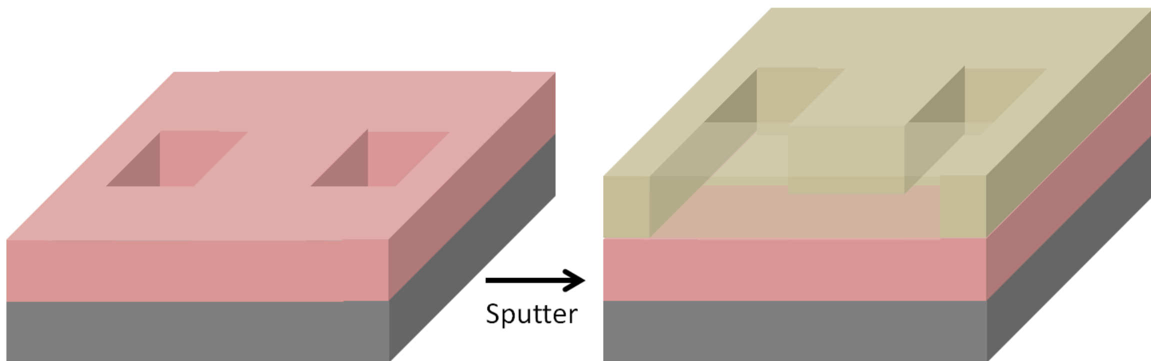


Figure 47: Overburden resulting from sputtering (transparent for visibility)

CMP could remove the excess material, but as mentioned previously, CMP is not an available technique in the Cal Poly Microfabrication Lab.

Regardless, a thick sputter deposited film represents significant expense, as the process could take longer than an hour, quickly using up sputter targets and the effluent argon gas.

Therefore, PVD may have a role in the final process flow for the deposition of thin films, but is not appropriate for the deposition of thick films.

7.2 Electroplated Nickel

Electroplating was initially considered a good candidate for device deposition. Nickel and copper electroplating techniques are frequently used in microelectronics processing. Nickel was selected over copper for electroplating

onto silicon because its reflectivity was more equal across the visible wavelengths, and therefore more suitable as a mirror, avoiding copper's brownish tint. Because the electroplating reaction is dependent on current, insulating photoresist will not plate, and so photoresist can be used as a mold into which the material could "grow" from the substrate. If the deposition process is terminated when the thickness of the deposit is equal to the thickness of the photoresist (see Section 6.3.2), a planar layer can be obtained. However, a variety of practical difficulties presented during initial testing, and electroplating was deemed unsuitable.

7.2.1 Deposition Difficulties on p-type Silicon

As a proof of concept, a 2x4 cm p-type silicon coupon was obtained for plating. This coupon was cleaned in a standard piranha solution for 10 minutes at 70C, and received a 30 second dip in 6:1 buffered oxide etchant afterward, in order to strip any native oxide. Immediately afterward, the coupon was connected with a clip-on wire to the negative terminal of a current source power supply. Nickel foil was attached to the positive terminal, and both were immersed in a typical Watts nickel bath.

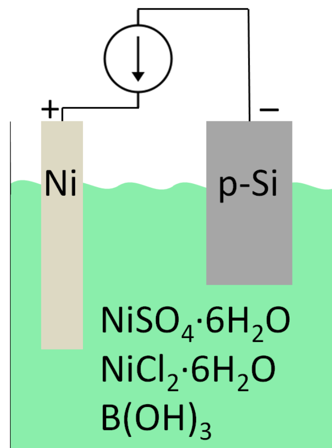


Figure 48: Electroplating proof of concept test

Because the optimal current density for Watts nickel is in the 0.005 to 0.1 $\frac{A}{cm^2}$ range [37], and the total area of both sides of the silicon coupon was 16 cm^2, the current source was set to the minimum of 0.08 A. However, the source reached its voltage limit and could not generate 0.08 A of current. After 15 minutes no visible plating had occurred on any part of the coupon and the experiment was terminated.

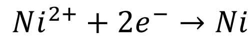
There were two immediately obvious explanations for the apparent lack of result. One was the high resistivity of the silicon. The wafer from which the p-type coupon was cut was 525 microns thick, and the resistivity specification was between 20-100 ohm-cm.

Assuming the best case, 20 ohm-cm, the resistance through the approximately ½ cm of coupon between the wire and the surface of the plating bath would be

$$R = \frac{\rho L}{A} = \frac{(20\ \Omega cm)\left(\frac{1}{2} cm\right)}{2cm * 0.0525cm} = 95\ \Omega \qquad \text{(Equation 14)}$$

Combined with the contact resistance of the wire to the coupon, which was likely significant (see 7.2.3), and the resistance of the plating bath, it is therefore unsurprising that the power supply reached its limit of 15V before a current output of 0.08A. The coupon may also have had a significantly higher resistivity than 20 ohm-cm.

The other obvious explanation for the difficulties was that p-type silicon has a majority of holes as its charge carriers. The electroplating reaction is



$$Ni^{2+} + 2e^{-} \rightarrow Ni$$

Therefore, a lack of electrons at the silicon surface could prohibit the deposition from initiating.

In order to address both of these concerns, the experiment was repeated with n+ doped silicon.

7.2.2 Deposition Difficulties on n+-type Silicon

A heavily doped n+ wafer was obtained, with a resistivity between 0.01-0.05 ohm-cm, and the experiment was repeated. Although in this case the current supply indicated that 0.08A was being supplied, the only visible plating occurred at the rough edges where the coupon was cleaved from the wafer. This small quantity of deposit displayed poor adhesion and flaked off. Despite the fact that the literature indicates it is possible to deposit directly onto highly doped,

polished silicon [38], a range of other practical issues were sufficient to dismiss electroplating for use in the process.

7.2.3 Electrical Contact to Silicon

Because silicon is a semiconductor, it is important to pay attention to its band structure. When a semiconductor and a metal are placed in intimate contact, the behavior of the junction is not necessarily ohmic. The charge in the regions near the junction will diffuse until the chemical potential for electrons – known as the Fermi level – of both materials is equal. Because the density of charge carriers in the semiconductor is low compared to the density of charge carriers in the metal, only the semiconductor demonstrates a “band bending” effect as a result of this diffusion [39].

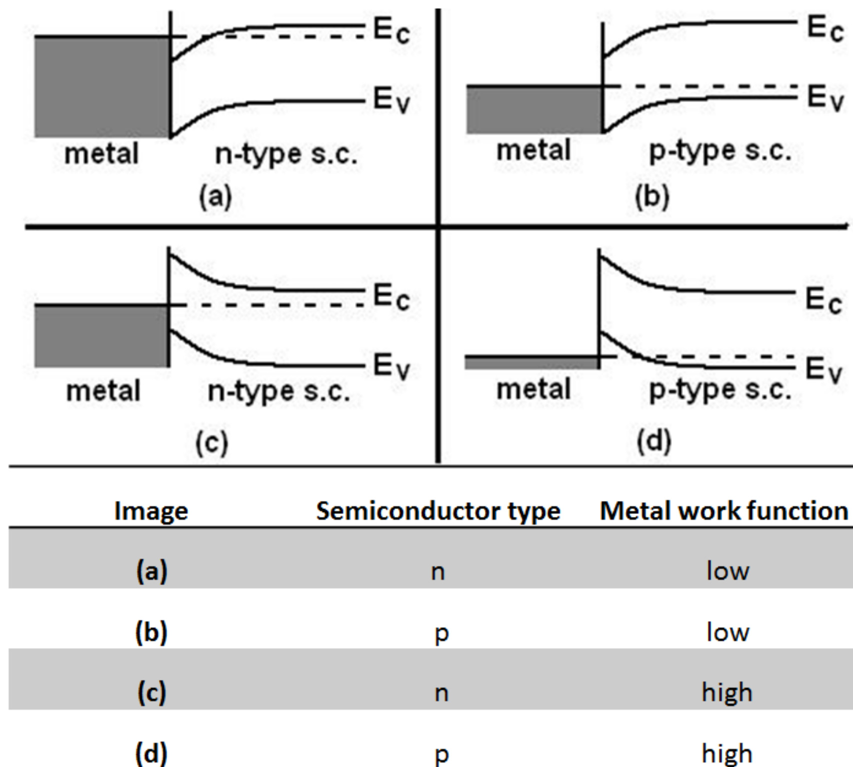


Image	Semiconductor type	Metal work function
(a)	n	low
(b)	p	low
(c)	n	high
(d)	p	high

Figure 49: Band bending at semiconductor/metal contacts with various work functions. The equilibrium Fermi level is shown as a dashed line. [40]

Since the electroplating current flows out of the semiconductor and into the wire, holes in the valence band are moving out of the semiconductor and into the wire in a p-type material. Figure 49(d) indicates that there may be an energy barrier between the p-type semiconductor valence band (Ev) and the metal. Similarly, because electrons flow out of the wire and into the conduction band (Ec) of an n-type semiconductor, Figure 49(c) indicates there may be an energy barrier. To determine whether these charge carriers experience an energy barrier during the electroplating, it is necessary to determine the initial difference in the Fermi levels of the contact materials.

Usefully, the difference in Fermi levels is equal to the negative difference in work functions, since the work function is defined as the difference between the Fermi level and the vacuum level, and the vacuum level is the same for all materials.

$$W_{Si} - W_{Fe} = \left(\phi - E_{F_{Si}}\right) - \left(\phi - E_{F_{Fe}}\right) = E_{F_{Fe}} - E_{F_{Si}} \qquad \text{(Equation 15)}$$

Here, W_{Si} is the work function of the silicon, W_{Fe} is the work function of the steel clip, ϕ is the vacuum level, $E_{F_{Fe}}$ is the Fermi level of the steel clip, and $E_{F_{Si}}$ is the Fermi level of the silicon.

Using a table of work functions, W_{Si} is found to be 4.63 eV for n+ silicon, and W_{Fe} is found to be 4.67 eV [41] [42]. Thus, the difference in Fermi levels is -0.04 eV.

Because this difference is small and negative, the band is similar to Figure 49(a), and the electrons can tunnel through without any appreciable resistance, forming an ohmic contact.

It is possible that the lack of plating on even the edges of the p-doped silicon, and the inability of the power supply to provide enough current, was because the energy barrier was substantially larger for the p-type silicon, which has a work function of 5.03 eV [41].

Regardless, the need to ensure that contacts are ohmic is an additional factor complicating direct silicon electroplating.

7.2.4 Seed Layer Interference with Traces

In order to avoid issues with resistivity and adhesion, it is common in industry to use PVD to deposit a conductive seed layer. However, because conductive traces and device electrodes must be patterned on the surface before the devices can be deposited above them, it is not possible to deposit a continuous seed layer without shorting the traces.

A solution to this problem is the use of a metal for the seed layer that can be preferentially etched away without damaging the devices or traces. However, this introduces risk of undercutting the deposited devices, as well as shorts due to incomplete etching. It also introduces the difficulty of creating an electrical contact to the thin seed layer after photoresist has been dispensed onto the surface, and when the first layer of metal has already been deposited.

7.2.5 Control of Current Density

Another major concern is the difficulty of delivering equal current density to all points on the surface of a wafer. Although heavy doping may permit sufficient current to be delivered to the substrate near the metal contact point, the combination of high resistivity and a thin wafer substrate will cause a dramatic drop in current delivered as distance increases from the contact. Because current determines plating rate, this is unacceptable for uniformity reasons.

In order to mitigate the distribution issue, it is possible to deposit a conductive film on the backside of the wafer. However, this metal backside will plate as well, and cannot be easily passivated like the backside of a silicon wafer.

Furthermore, the concept of “throwing power” in electroplating measures the ability of the solution to achieve a uniform deposit on the active cathode surface [43] [44]. Parameters which impact the throwing power, besides the current distribution already discussed, include polarization and cathode efficiency.

Polarization is the change in local cathodic potential, which is a result of concentration gradients and reaction rates in the plating bath. Typically the severity of polarization-related issues increases with current density [37].

The cathode efficiency, by contrast, is the percentage of electrons delivered to the active cathode surface which are used for the redox reaction. For nickel, it tends to improve with greater current density, frustrating any attempts to adjust for issues with the polarization [37] [45].

Taken together, these electrochemical effects can produce substantial non-uniformity, especially when compared to so-called “electroless” deposition methods.

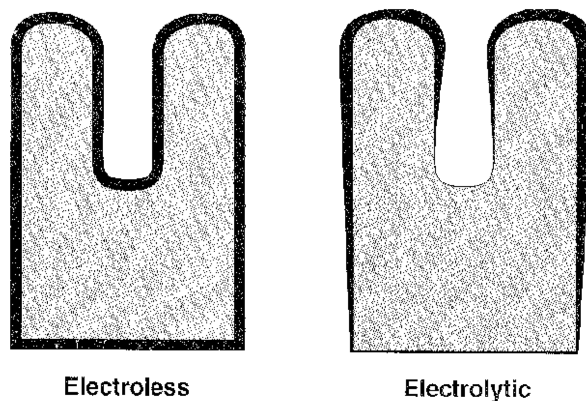


Figure 50: Comparison of electroless and electrolytic throwing power [46]

Considering the small and complex geometries involved in the deposition of micromirrors, as well as the other factors mentioned, it was concluded that electroless deposition would serve as a more suitable deposition method.

7.3 Electroless Nickel

Electroless deposition is used extensively for microelectronics applications. Besides applications in device packaging, its suitability for use in the critical process flow of cutting-edge logic and memory chips is being explored, particularly for back-end-of-line processes like interconnect capping and through-silicon vias.

Further, the literature contains many examples of successful electroless deposition directly onto silicon [47] [48] [49] [50]. This includes deposition of cobalt, copper, silver, platinum, and palladium. Nickel was again selected over copper for optical reasons, over the precious metals due to cost concerns, and cobalt for the greater deposition rate.

7.3.1 Characteristics and Advantages

Electroless deposition proceeds only upon surfaces catalytic to the deposition. However, unlike displacement reactions, electroless deposition does not terminate upon the deposition of a few atomic layers. Electroless processes are autocatalytic and will self-propagate: each atomic monolayer that is deposited will serve as the catalytic surface for the next layer.

However, this means initiation will occur only on catalytic surfaces. For electroless nickel, the following materials, among others, are catalytic and can

initiate deposition: silicon, copper, aluminum, tungsten, cobalt, platinum, silver, vanadium, titanium, nickel, gold, iron, tin and palladium [51]. Many polymers and insulating materials are excluded; most photoresist will not plate.

Unlike electroplating, where metal ions are reduced out of solution by an electric current, in electroless plating the ions are precipitated by reducing agents in the solution. The oxidation potential of these reducing agents must be sufficient to overcome the reduction potential of the metal species, as well as the inefficiency of the liquid system.

Some reducing agents appropriate for electroless nickel include hypophosphites, borohydrides, amine boranes (particularly dimethylamine borane), and hydrazine [52]. The most common of these for industrial applications is hypophosphite, typically as the sodium salt, in part because hypophosphite chemistries are simpler and better-understood, and in part because of the safety issues associated with dimethylamine borane and hydrazine [53].

Each of these reducing agents tends to partially co-deposit with the nickel, producing Ni-P alloys with hypophosphite chemistries, Ni-B alloys with borohydrate or amine borane chemistries, and oxygen and nitrogen impurities in the nickel with hydrazine chemistries. The bath chemistry may be chosen so as to improve the mechanical characteristics of the deposited alloy, which may be annealed or left as deposited. Some more complex electroless nickel deposition chemistries even include additional metals, such as tungsten, to deposit

alongside the nickel and further improve the structure and mechanical chacteristics of the alloy [54].

7.3.2 Process Integration

Since electroless deposition is conformal, but will not deposit onto photoresists, it is possible to use a thick photoresist as a kind of deposition mold. If photoresist is deposited onto a catalytic substrate and patterned such that the regions where deposition is desired are exposed, it is possible to create high aspect ratio devices with vertical sidewalls. Furthermore, if the process is terminated when the thickness of the deposit is approximately equivalent to the thickness of the photoresist, a planar surface will result without the use of CMP, and an additional layer of photoresist may be coated to produce another “layer” and fulfill the constraint for iterability.

In order to avoid further exposing the previous layer(s) of photoresist during lithography of the most recently deposited one, PVD can be used to deposit a thin reflective film onto the surface of the previous layer. This film may subsequently be patterned to the shape of the mold and used as a catalytic layer for the ensuing deposition.

Additionally, this method allows a conductive layer to be deposited onto the silicon, patterned to form traces and electrodes, and remain on the surface while the device is fabricated above.

This general outline is illustrated in Figure 51. For visibility the device shown is not a micromirror. All resists shown are positive tone.

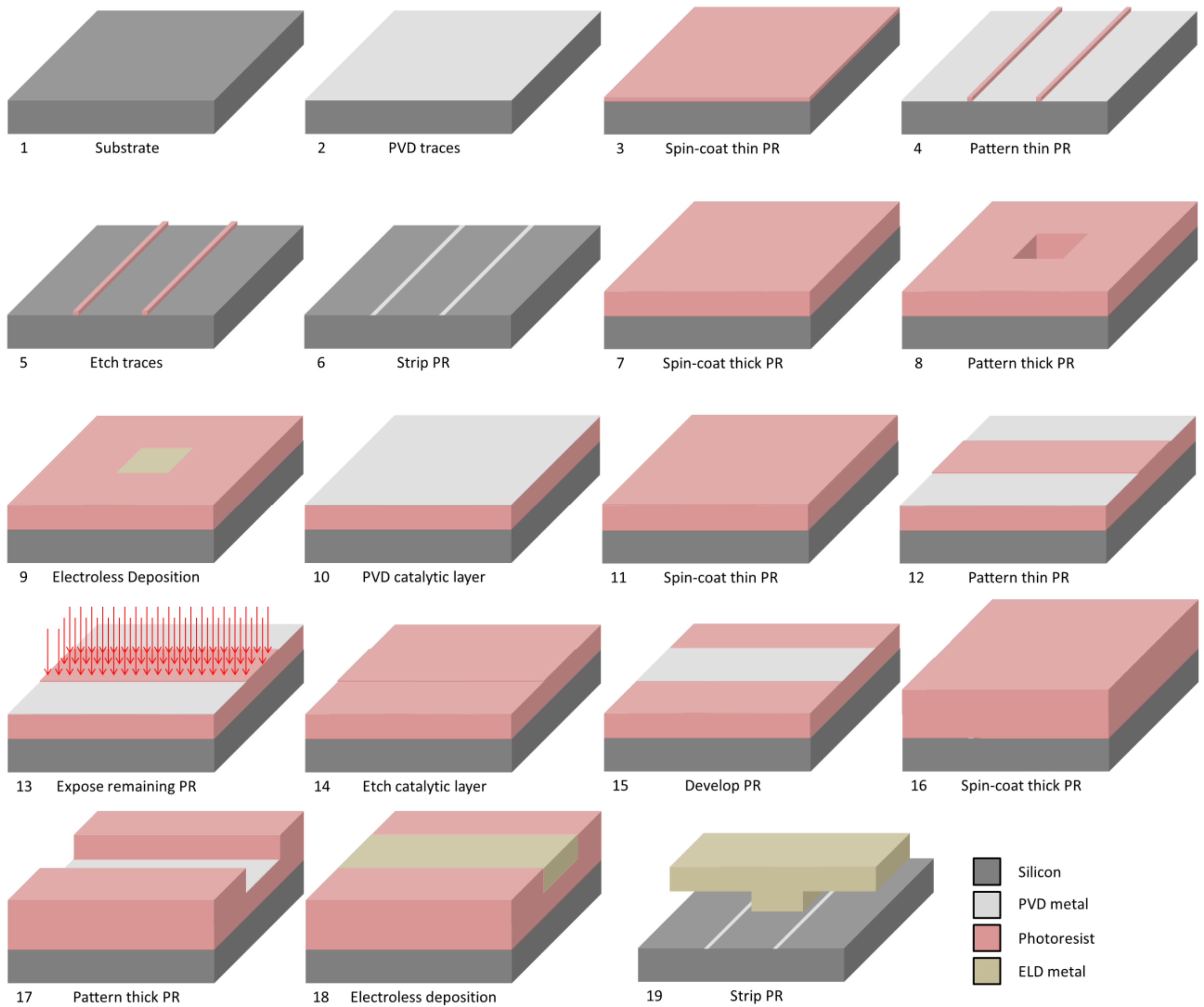


Figure 51: Multilayer ELD process flow

8. Final Device Design

Before the process can be explored in detail, it is necessary to establish the device design, so that the deposition steps and lithographic masks can be developed appropriately.

Because the immediate objective is obtaining functional devices, achieving optimal performance of is lesser importance, and so the design selected for fabrication should not push the limits of process capability. However, understanding the relation of design parameters to the performance of the device is important not only to optimize design when performance does not come at the cost of manufacturability, but also for enabling future improvement of the design once pilot devices can be obtained.

Beginning from the device constraints outlined in Section 6.2, the necessary design decisions are: electrode separation distance, mirror and hinge geometry, electrode size and placement, and electroless alloy selection. The resulting device should be able to achieve 10 degrees of tilt at the smallest voltage.

8.1 Optimization of Straight Beam Model

8.1.1 Assumptions and Limitations

In order to begin developing the model to optimize, a number of assumptions must be made, of varying legitimacy.

The first of these is that the mirror surface is perfectly rigid. Although this is clearly an approximation, planarity of the surface during actuation is necessary for optical reasons, and so design will be constrained to produce a rigid mirror.

Therefore the selected design will be checked via FEA for mirror planarity and this requirement can verified. As noted in Section 6.2.2, the thickness of the mirror and the hinges will be equal due to co-deposition. To permit the hinges to be thinner in future devices, three electroless deposition steps will be necessary.

Second is the assumption that the parallel-plate force approximation is accurate. Assuming the maximum separation of 20 microns, and a mirror device 100 microns square, it is likely that there will be substantial fringing effects in the electrostatic field at the edges that make this approximation relatively inaccurate.

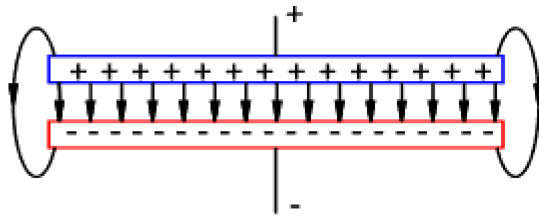


Figure 52: Fringing on parallel plates of finite length

According to Nishiyama and Nakamura, a reasonable correction factor for the capacitance of parallel-plate mirrors with an aspect ratio $b = \frac{separation}{width}$ less than 1 and greater than 0.1 is [55]

$$C_{CF} = 1 + 2.343b^{0.891} \quad \text{(Equation 16)}$$

For the aspect ratio 0.2 corresponding to 20 microns separation and 100 square,

$$C_{CF} = 1 + 2.343 * 0.2^{0.891} = 1.509 \quad \text{(Equation 17)}$$

which is a substantial deviation from the approximation.

Deriving a new expression for force,

$$U = C\frac{V^2}{2} = \left(1 + 2.343 * \left(\frac{d}{\sqrt{W\ell}}\right)^{0.891}\right) * \frac{(\varepsilon W\ell)}{d} * \frac{V^2}{2}$$ (Equation 18)

$$F = \frac{\partial U}{\partial d} = V^2 * \frac{1.0438\varepsilon W\ell}{\left(\frac{d}{\sqrt{W\ell}}\right)^{0.109} d\sqrt{W\ell}} - \left(1 + 2.343 * \left(\frac{d}{\sqrt{W\ell}}\right)^{0.891}\right) * \frac{(\varepsilon W\ell)}{2d^2}$$ (Equation 19)

Using $\varepsilon = 8.85 * 10^{-12}\ F/m$ for air, a W and ℓ of 100 μm, d of 20 μm, and V = 50 volts,

$$F = -2.934 * 10^{-7} N = -0.2934 \mu N$$ (Equation 20)

Compared to the force with the approximation

$$F_d = -\frac{\frac{1}{2}(\varepsilon W\ell V^2)}{d^2} = -2.766 * 10^{-7} N = -0.2766\ \mu N$$ (Equation 1)

Although the two attractive forces are clearly not the same, they are not as different as might be expected from a capacitance correction factor of 1.509.

The percent error is

$$\%d = \left|\frac{corrected - approx}{corrected}\right| = \left|\frac{(2934 - \ 2766)}{2934}\right| * 100\% = 5.73\%$$ (Equation 21)

which is small enough to neglect for the purposes of optimization, particularly considering that the approximation underestimates the total force.

Another complication where the parallel-plate force approximation may be incorrect is any difference in area of the electrode and the mirror surface; again, by using the area of the smaller electrode, the worst-case result is a too-small force approximation.

Finally, to simplify the derivations in the following sections, it must be assumed that the electrode is rectangular and exactly as wide as the device. Since this is the optimal use of space, it would follow that such an electrode can produce the greatest force, and it is natural to constrain the electrodes to this design.

8.1.2 Pull-in Voltage

To find the voltage required to cause the device to touch the surface, it is first necessary to develop a thorough understanding of "pull-in". The pull-in voltage is the point at which the electrostatic force, which is inversely proportional to the square of separation, begins to overwhelm the mechanical restoring force of the hinges, which is proportional to the displacement. When this pull-in point is reached, the device will snap down onto the surface without any additional voltage being applied, and a small decrease in voltage will not be sufficient to cause it to disengage from the surface.

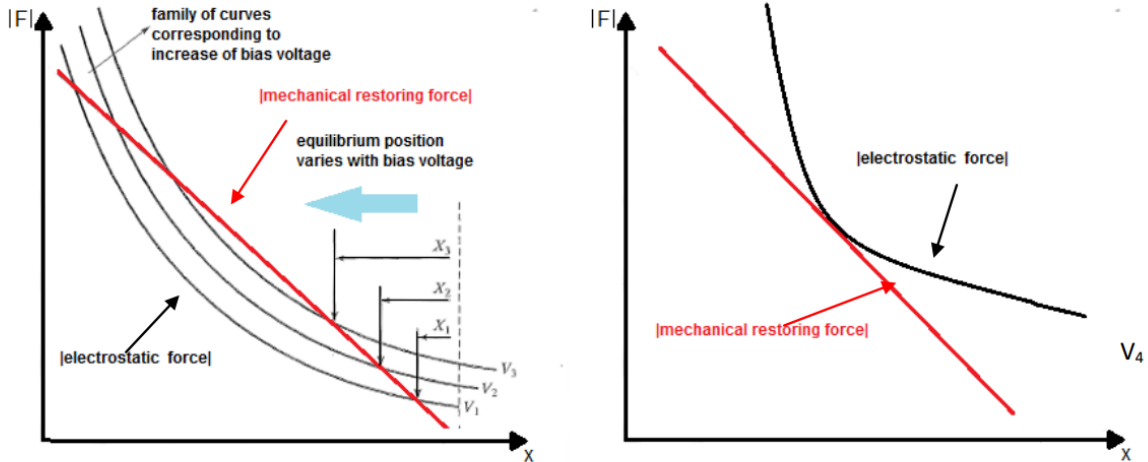


Figure 53: Restoring force and electrostatic force vs plate separation [56]

In order to develop a clearer understanding of the phenomenon, a conductive plate on a Hookean spring will be considered.

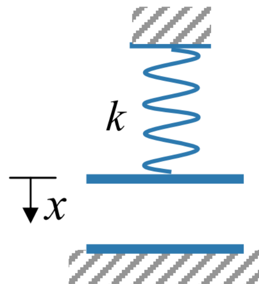


Figure 54: Simplified pull-in model [57]

If d is the initial separation and A is the area of the plates, the capacitance is

$$C = \frac{\varepsilon A}{d - x} \qquad \text{(Equation 22)}$$

so the total energy of the system is

$$E = \frac{1}{2}kx^2 - \frac{1}{2}\frac{\varepsilon A}{d - x}V^2 \qquad \text{(Equation 23)}$$

and the force is

$$F = \frac{\partial E}{\partial x} = kx - \frac{1}{2}\frac{\varepsilon A}{(d-x)^2}V^2 \qquad \text{(Equation 24)}$$

The pull-in point occurs when the force from each component is equal, and the net force is zero [57], so

$$kx = \frac{1}{2}\frac{\varepsilon A}{(d-x)^2}V^2 \qquad \text{(Equation 25)}$$

Since the net force on the system at equilibrium will never be positive (repulsive), when F is zero, the equilibrium force is at maximum at the pull-in point.

Therefore, the pull-in point is when $\frac{\partial F}{\partial x} = 0$:

$$\frac{\partial F}{\partial x} = \frac{\varepsilon A}{(d-x)^3}V^2 - k = 0 \qquad \text{(Equation 26)}$$

Substituting Equation 25,

$$\frac{2kx}{d-x} - k = 0 \qquad \text{(Equation 27)}$$

And therefore the pull-in point is at

$$x = \frac{d}{3} \qquad \text{(Equation 28)}$$

Therefore, the amount of voltage required to achieve snap-down is equal to the amount necessary to pull the device one-third of the separation distance, which can be found by substituting Equation 28 into Equation 25,

(Equation 29)

(Equation 30)

This result can be applied to any parallel-plate capacitor with a restoring force linearly proportional to distance, where k is the effective spring constant.

8.1.3 Torque vs Force

Before a model of the mechanical behavior of the device can be developed, equations relating the force and torque at the hinges to the device geometry and voltage must be found. Figure 55 shows and are the width and length of the mirror, respectively, and and are the distance between the electrode and the hinge axis and mirror edge, respectively.

Figure 55: Electrode placement

In order to ensure functional devices, some constraints were set in terms of these variables:

$\frac{(\ell_1+\ell_2)}{\ell} < 0.5$ in order to ensure sufficient torque is developed,

$\ell_1 > 0.05\ell$ to ensure adequate spacing from the electrode on the opposite side of the hinge,

$\ell_2 > 0.1\ell$ to ensure there is sufficient room so that the mirror does not touch the electrode on snap-down,

and of course, $\ell_1 + \ell_2 < l$

If x is a dummy variable measuring distance from the axis ($x = 0$) to the edge of the mirror ($x = \ell$), then the force $dF = P(x)Wdx$ for a thin sliver of the mirror is

$$dF = P(x)Wdx = -\frac{\frac{1}{2}(\varepsilon V^2)}{s(x)^2}Wdx \qquad \text{(Equation 31)}$$

$s(x)$, the separation at x, also depends on the angle of tilt and hinge pull (see Figure 38). Using the small angle approximation,

$$\mathrm{s(x)} = d - x * \sin(\theta) - \delta_{\max} = d - \theta x - \delta_{\max} \qquad \text{(Equation 32)}$$

$$dF = P(x)Wdx = -\frac{\frac{1}{2}(\varepsilon V^2)}{(d - \theta x - \delta_{\max})^2}Wdx \qquad \text{(Equation 33)}$$

Unfortunately $\delta_{\max}$ is dependent on the force, and differential methods become necessary. To avoid this, an approximation is made and $\delta_{\max}$ is excluded from the computation.

It is worth noting that a very precise solution for the force between two non-parallel finite plates exists, but cannot be expressed in closed form. It may be of use for optimization via numerical methods [58].

Dropping $\delta_{\max}$ gives

$$dF = P(x)Wdx = -\frac{\frac{1}{2}(\varepsilon V^2)}{(d-\theta x)^2}Wdx \qquad \text{(Equation 34)}$$

And

$$F = \int_{\ell_1}^{\ell-\ell_2} P(x)Wdx = \int_{\ell_1}^{\ell-\ell_2} -\frac{\frac{1}{2}(\varepsilon V^2)}{(d-\theta x)^2}Wdx \qquad \text{(Equation 35)}$$

So

$$F = -\frac{1}{2}\varepsilon V^2 W \frac{(\ell_1+\ell_2-l)}{(\ell_1\theta-d)(\ell_2\theta+d-\theta l)} \qquad \text{(Equation 36)}$$

The torque T may be found similarly, since $dT = xdF$

$$dT = P(x)Wxdx = -\frac{\frac{1}{2}(\varepsilon V^2)}{(d-\theta x)^2}Wxdx \qquad \text{(Equation 37)}$$

And

$$T = \int_{\ell_1}^{\ell-\ell_2} P(x)Wxdx = \int_{\ell_1}^{\ell-\ell_2} -\frac{\frac{1}{2}(\varepsilon V^2)}{(d-\theta x)^2}Wxdx \qquad \text{(Equation 38)}$$

So

$$T = -\frac{1}{2}\varepsilon V^2 W\Big(\frac{(-ln(l\theta-\theta\ell_2-d)l\theta + ln(l\theta-\theta\ell_2-d)\,\theta\ell_2)}{\theta^2(-l\theta+\theta\ell_2+d)} + \frac{ln(l\theta-\theta\ell_2-d)\,d+d}{\theta^2(-l\theta+\theta\ell_2+d)} - \frac{(-ln(\theta\ell_1-d)\,\theta\ell_1 + ln(\theta\ell_1-d)\,d+d)}{\theta^2(-\theta\ell+d)}\Big) \qquad \text{(Equation 39)}$$

Although the hinge pull was not a part of the calculation, maximizing the ratio of torque to force will reduce hinge pull:

$$\frac{T}{F} = \frac{1}{\theta^2(l - l_2 - l_1)}(\ln(l\theta - \theta l_2 - d)l\,\theta^2 l_1 - \ln(l\theta - \theta l_2 - d)\theta^2 l_1 l_2 - \ln(\theta l_1 - d)l\,\theta^2 l_1 + \ln(\theta l_1 - d)\,\theta^2 l_1 l_2 - \ln(l\theta - \theta l_2 - d)dl\theta - \ln(l\theta - \theta l_2 - d)d\,\theta l_1 + \ln(l\theta - \theta l_2 - d)d\,\theta l_2 + \ln(\theta l_1 - d)dl\,\theta + \ln(\theta l_1 - d)d\,\theta l_1 - \ln(\theta l_1 - d)d\,\theta l_2 + \ln(l\theta - \theta l_2 - d)d^2 - \ln(\theta l_1 - d)d^2 + dl\,\theta - d\theta l_1 - d\theta l_2 \quad \text{(Equation 40)}$$

Using the constraints listed earlier in the section, $\frac{(\ell_1+\ell_2)}{\ell} < 0.5$, $\ell_1 > 0.05\ell$, $\ell_2 > 0.1\ell$ and $\ell_1 + \ell_2 < l$, the optimization routine in Maple 18 always reports local maxima such that ℓ_1 is 0.4ℓ, the maximum allowed, and ℓ_2 is $0.1\,\ell$, the minimum allowed. This is an unsurprising result, since the ratio $\frac{T}{F}$ is maximized if all force occurs at the edge of the device, but it serves to validate the expression.

8.1.4 Tilt vs Displacement

As discussed previously in 6.2.4, force at the hinges causes the whole device to "sag" toward the electrode. Using the expressions for force and torque already developed, it is possible to find both the tilt and displacement at the hinges. This treatment will apply only to rectangular-sectioned, straight-beam hinges, because of the mechanical complexity of the serpentine beams.

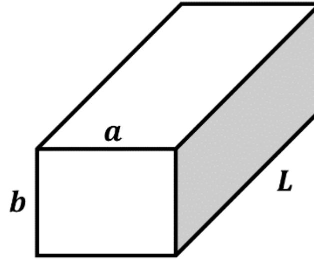


Figure 56: Hinge beam variables

Because the hinges on each side are identical, and because the device is symmetrical about two axes, it can be assumed that the torsion of each beam at the mirror is equal, and the torque at each hinge is – (see Figure 55), so

–— (Equation 41)

where L is the length of the hinge beam, J is the polar moment of inertia, and G is the shear modulus.

Furthermore, because the mirror surface is assumed to be rigid, the maximum deflection of each beam is equal and occurs at the mirror, and the beam is fixed-free with a force at the end of – (see Figure 55), so the mirror displacement is

–— (Equation 42)

where L is the length of the hinge beam, I is the second moment of area, and E is the elastic modulus.

In order to permit comparison of the two, the conversion formula of elastic moduli is used, where is Poisson's ratio,

(Equation 43)

So that

$$\frac{\theta}{\delta_{\max}} = \frac{6TI(1+\nu)}{JFL^2} \qquad \text{(Equation 44)}$$

Here, I and J correspond to a beam with the geometry shown in Figure 56, where a > b, i.e., a beam wider than it is thick. This is a reasonable constraint, since the beams cannot be thinner than 8 microns, and it is unlikely that a beam thicker than 8 microns will be desired.

The second moment of area, I, is

$$I = \frac{ab^3}{12} \qquad \text{(Equation 45)}$$

And the polar moment of inertia, J, is approximately

$$J = ab^3\left(\frac{1}{3} - 0.21\frac{b}{a}\left(1 - \frac{b^4}{12a^4}\right)\right) \qquad \text{(Equation 46)}$$

Substituting these into Equation 45,

$$\frac{\theta}{\delta_{\max}} = \frac{(1+\nu)}{\left(\frac{2}{3} - 0.42\frac{b}{a}\left(1 - \frac{b^4}{12a^4}\right)\right)L^2} * \frac{T}{F} \qquad \text{(Equation 47)}$$

And substituting the result obtained for $\frac{T}{F}$ in the previous section,

$$\begin{aligned}\frac{\theta}{\delta_{\max}} = {} & \frac{(1+\nu)}{\left(\frac{2}{3} - 0.42\frac{b}{a}\left(1 - \frac{b^4}{12a^4}\right)\right)L^2} \\ & * \left(\frac{1}{\theta^2(l - l_2 - l_1)}(\ln(l\theta - \theta l_2 - d)l\,\theta^2 l_1\right. \\ & - \ln(l\theta - \theta l_2 - d)\theta^2 l_1 l_2 - \ln(\theta l_1 - d)l\,\theta^2 l_1 \\ & + \ln(\theta l_1 - d)\,\theta^2 l_1 l_2 \\ & - \ln(l\theta - \theta l_2 - d)dl\theta - \ln(l\theta - \theta l_2 - d)d\,\theta l_1 \\ & + \ln(l\theta - \theta l_2 - d)d\,\theta l_2 + \ln(\theta l_1 - d)dl\,\theta \\ & + \ln(\theta l_1 - d)d\,\theta l_1 - \ln(\theta l_1 - d)d\,\theta l_2 \\ & + \ln(l\theta - \theta l_2 - d)d^2 - \ln(\theta l_1 - d)d^2 + dl\,\theta - d\theta l_1 \\ & \left. - d\theta l_2\right)\end{aligned} \qquad \text{(Equation 48)}$$

Hence it is clear that maximizing the ratio of beam width to thickness, minimizing the length, placing the electrode below to the edge of the mirror, and choosing a material with relatively high Poisson's ratio will reduce the hinge pull at snap-down.

Notably, the size of the device is not important, only the hinge length. Although halving the beam length will reduce the hinge pull by a factor of 4 for any given angle, the initial device design will be relatively large and will use relatively long hinges to ensure snap-down can be achieved. Future designs may reduce the separation distance and device size in order to enable reduction of the beam length.

8.1.5 Efficient Design Manifold

By using the equations already developed, it is possible to find the voltage required to obtain the snap-down condition in terms of all other variables.

At equilibrium, the additional electrostatic torque resulting from a differential increase in the tilt angle will be equal to the additional restoring torque. This can be expressed as $\frac{dT_{res}}{d\theta} = \frac{dT_{es}}{d\theta}$

Beginning again from Equation 41,

$$\theta = \frac{1}{2}\frac{T_{res}L}{JG} \qquad \text{(Equation 41)}$$

So

$$\frac{dT_{res}}{d\theta} = \frac{2JG}{L} \qquad \text{(Equation 49)}$$

And substituting Equations 43 and 46,

$$\frac{dT_{res}}{d\theta} = \frac{Eab^3(\frac{1}{3} - 0.21\frac{b}{a}\left(1 - \frac{b^4}{12a^4}\right))}{L(1+\nu)} \qquad \text{(Equation 50)}$$

Next, differentiating Equation 39,

$$T_{es} = -\frac{1}{2}\varepsilon V^2 W(\frac{(-ln(l\theta - \theta\ell_2 - d)l\theta + ln(l\theta - \theta\ell_2 - d)\,\theta\ell_2)}{\theta^2(-l\theta + \theta\ell_2 + d)} + \frac{ln(l\theta - \theta\ell_2 - d)\,d + d}{\theta^2(-l\theta + \theta\ell_2 + d)} - \frac{(-ln(\theta\ell_1 - d)\,\theta\ell_1 + ln(\theta\ell_1 - d)\,d + d)}{\theta^2(-\theta\ell + d)}) \qquad \text{(Equation 39)}$$

$$\frac{dT_{es}}{d\theta} = \varepsilon V^2 W(\frac{(-\theta l_1 + d)^2\left((-l + l_2)\theta + d\right)^2 ln\left((l - l_2)\theta - d\right)}{(-\theta l_1 + d)^2\left((-l + l_2)\theta + d\right)^2\theta^3} - \frac{(-\theta l_1 + d)^2\left((-l + l_2)\theta + d\right)^2 ln(\theta l_1 - d)}{(-\theta l_1 + d)^2\left((-l + l_2)\theta + d\right)^2\theta^3} + \frac{(2l_2(l - l_2)\theta^2 - \frac{3}{2}d(l + l_1 + l_2)\theta + d^2)(l - l_1 - l_2\theta d)}{(-\theta l_1 + d)^2\left((-l + l_2)\theta + d\right)^2\theta^3} \qquad \text{(Equation 51)}$$

Then, because $\frac{dT_{res}}{d\theta} = \frac{dT_{es}}{d\theta}$,

$$\frac{Eab^3(\frac{1}{3} - 0.21\frac{b}{a}\left(1 - \frac{b^4}{12a^4}\right))}{L(1+\nu)} = \varepsilon V^2 W(\frac{(-\theta l_1 + d)^2\left((-l + l_2)\theta + d\right)^2 ln\left((l - l_2)\theta - d\right)}{(-\theta l_1 + d)^2\left((-l + l_2)\theta + d\right)^2 \theta^3} - \frac{(-\theta l_1 + d)^2\left((-l + l_2)\theta + d\right)^2 ln(\theta l_1 - d)}{(-\theta l_1 + d)^2\left((-l + l_2)\theta + d\right)^2 \theta^3} + \frac{(2l_2(l - l_2)\theta^2 - \frac{3}{2}d(l + l_1 + l_2)\theta + d^2)(l - l_1 - l_2\theta d)}{(-\theta l_1 + d)^2\left((-l + l_2)\theta + d\right)^2 \theta^3} \quad \text{(Equation 52)}$$

And $T_{res} = T_{es}$,

$$\frac{\theta Eab^3\left(\frac{1}{3} - \frac{0.21 * b}{a}\left(1 - \frac{b^4}{12a^4}\right)\right)}{L(1+\nu)} = -\frac{1}{2}\varepsilon V^2 W(\frac{(-ln(l\theta - \theta\ell_2 - d)l\theta + ln(l\theta - \theta\ell_2 - d)\,\theta\ell_2)}{\theta^2(-l\theta + \theta\ell_2 + d)} + \frac{ln(l\theta - \theta\ell_2 - d)\,d + d}{\theta^2(-l\theta + \theta\ell_2 + d)} - \frac{(-ln(\theta\ell_1 - d)\,\theta\ell_1 + ln(\theta\ell_1 - d)\,d + d)}{\theta^2(-\theta\ell + d)}) \quad \text{(Equation 53)}$$

This system of two equations allows θ to be eliminated. Minimizing V as a function of all design parameters will give the “efficient design manifold”, a surface in 10-dimensional space that corresponds to all possible devices which

minimize the voltage necessary to achieve snapdown. Constraining parameters will yield a subspace of feasible devices; for example, E must be kept within physical limits. If sufficiently constrained, a single device may result.

Table III: Design variables

Variable	Description
$\boldsymbol{V}$	Voltage across the electrode and mirror
$\boldsymbol{\theta}$	Critical device tilt
$\boldsymbol{W}$	Mirror width
$\boldsymbol{\ell}$	Length from hinge axis to mirror edge
$\boldsymbol{\ell_1}$	Distance from hinge axis to electrode
$\boldsymbol{\ell_2}$	Distance from electrode to mirror edge
$\boldsymbol{L}$	Hinge length
$\boldsymbol{a}$	Hinge width
$\boldsymbol{b}$	Device thickness
$\boldsymbol{\nu}$	Poisson's ratio
$\boldsymbol{E}$	Elastic modulus

Table IV: Design constraints

Constraint	Description
$\boldsymbol{\ell_1} + \boldsymbol{\ell_2} \leq \boldsymbol{\ell}$	Size of electrode cannot be negative
$\boldsymbol{V}, \boldsymbol{\theta}, \boldsymbol{W}, \boldsymbol{\nu}, \boldsymbol{E}, \boldsymbol{\ell}, \boldsymbol{L}, \boldsymbol{a}, \boldsymbol{b} > 0$	Device parameters must be positive
$\boldsymbol{\ell_1}, \boldsymbol{\ell_2} \geq \mathbf{0}$	Device parameters cannot be negative
$\boldsymbol{a} > b$	Hinges must be wider than device thickness
$\boldsymbol{\theta_{max}} \geq \mathbf{10}^\circ$	Mirror must tilt 10 degrees or more at snapdown

Some of these design constraints are expressed in terms of the variables in Table III. The constraint of 10 degrees of obtainable tilt, however, is expressed in terms of $\delta_{\max}$ and d, the initial separation.

$$\sin \boldsymbol{\theta}_{max} = \frac{\boldsymbol{d} - \boldsymbol{\delta}_{\max}}{\boldsymbol{\ell}} \quad \text{(Equation 54)}$$

Finding an expression for $\delta_{\max}$,

$$\delta_{\max} = \frac{1}{2}\frac{FL^3}{3EI} \quad \text{(Equation 55)}$$

Substituting Equations 36 and 46,

$$\delta_{\max} = \frac{\varepsilon V^2 W \frac{(\ell - \ell_1 - \ell_2)}{\theta_{max}^2(\ell - \ell_1)\ell_2} L^3}{Eab^3} \quad \text{(Equation 56)}$$

Using the small-angle approximation,

$$\boldsymbol{\theta}_{max} = \frac{\boldsymbol{d} - \frac{\boldsymbol{\varepsilon V^2 W} \frac{(\boldsymbol{\ell} - \boldsymbol{\ell}_1 - \boldsymbol{\ell}_2)}{\boldsymbol{\theta}_{max}^2(\boldsymbol{\ell} - \boldsymbol{\ell}_1)\boldsymbol{\ell}_2} \boldsymbol{L}^3}{\boldsymbol{Eab}^3}}{\boldsymbol{\ell}} \quad \text{(Equation 57)}$$

Here, V is the snapdown voltage, and θ_{max} is the angle at snapdown. In order to obtain the constrained design relation, a solution must be found for the system with Equations 52 and 53, and the value of θ_{max} in Equation 57 for any set of parameters must be 10 degrees or greater. Due to the complexity of these equations, and the implicit nature of Equation 57, this is left to numerical methods.

As an iterative optimization algorithm, the partial derivative of V with respect to each design parameter can be calculated via numerical methods, and the design value for that parameter can be decreased for any parameter with a positive partial, and increased for any parameter with a negative partial, until a solution is

found. Because this solution may be a local, and not a global, minimum for V, the process should be repeated with different initial design parameters.

8.2 Device Material

Having identified ELD nickel as the deposition method, it is necessary to select a co-deposition alloy. Because the reducing agent will co-deposit with the nickel, and because hydrazine can be excluded for safety reasons, the choice is limited to the alloys produced by the other common reductants, either a nickel-phosphorous alloy (hypophosphite) or nickel-boron alloy (amine boranes).

Thick nickel-boron deposits tend to be associated with greater intrinsic tensile stress than thick nickel-phosphorous deposits [53]. In addition, hypophosphite is safer and more widely used for plating applications. As a result, a hypophosphite chemistry and nickel-phosphorous alloy was selected for device deposition.

The properties of nickel-phosphorous alloys vary significantly with the phosphorous concentration. The concentration of phosphorous in the deposited alloy can be controlled by varying process parameters so that the properties of the deposit are as desired.

8.2.1 Reflectivity & Resistivity

To enable the device surface to function as a mirror, a high reflectivity is important. The greatest reflectivity of a nickel-phosphorous alloy occurs in the 11-13% range by weight, but is acceptable anywhere in the 9-15% weight range [59].

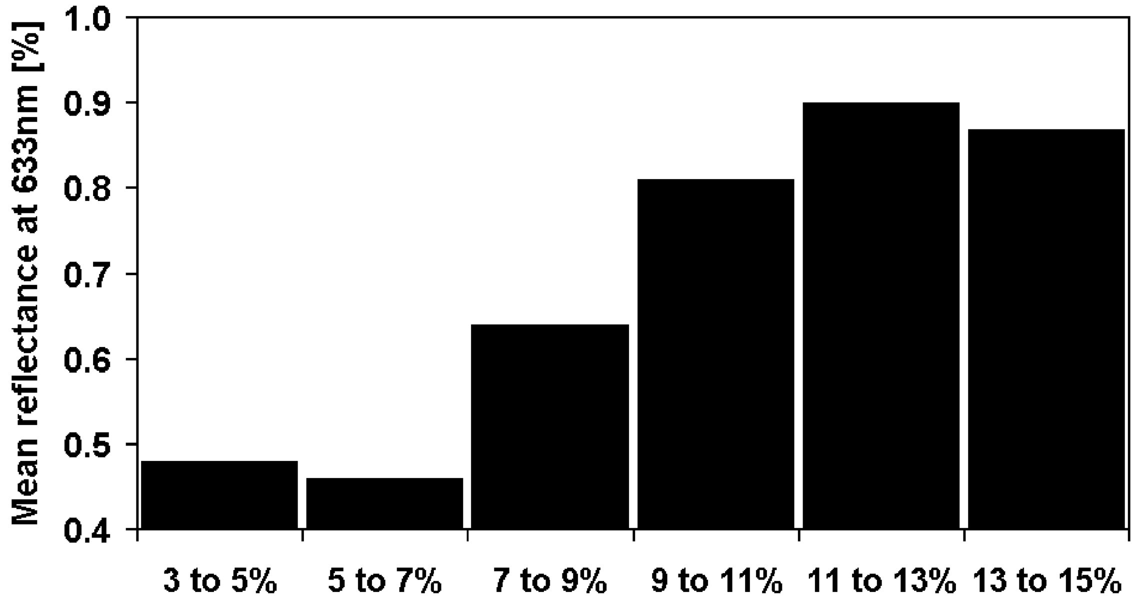


Figure 57: NiP reflectivity vs phosphorous concentration [59]

The resistivity of the deposit, although less important than the actuating traces, should also be considered.

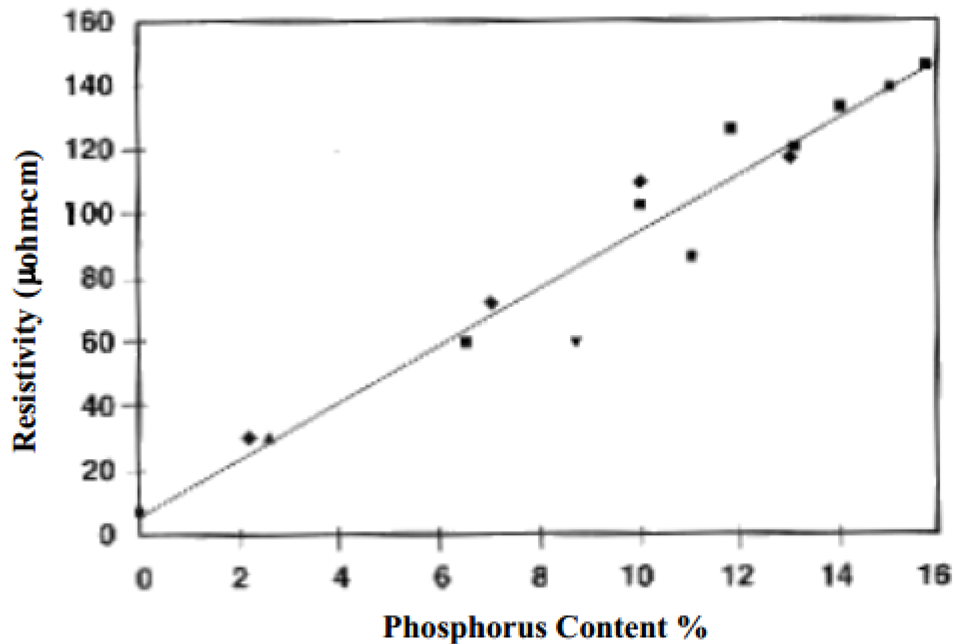


Figure 58: NiP resistivity vs phosphorous concentration [46]

Based on Figure 57 and Figure 58, a phosphorous content by weight of 11% appears appropriate, corresponding to a reflectivity of about 90% at 633nm and a

resistivity of about $90\ \mu\Omega \cdot cm$. Although this is more than an order of magnitude higher than bulk nickel at about $7\ \mu\Omega \cdot cm$, it suggests the alloy will be sufficiently conductive.

8.2.2 Minimizing Film Stress

For the NiP alloy, both intrinsic and extrinsic film stress should be minimized, in order to combat warping and delamination in the thick deposit.

The major factor influencing the intrinsic stress is the presence of two non-equilibrium phases, β and γ. β is a microcrystalline solid solution of phosphorous in nickel, and γ is a fully amorphous metallic glass [60]. According to W. Liu, et al., this amorphous phase is a result of the electronegative P drawing electrons from the Ni bonding, and the P-P segregation force reaching a critical point [61].

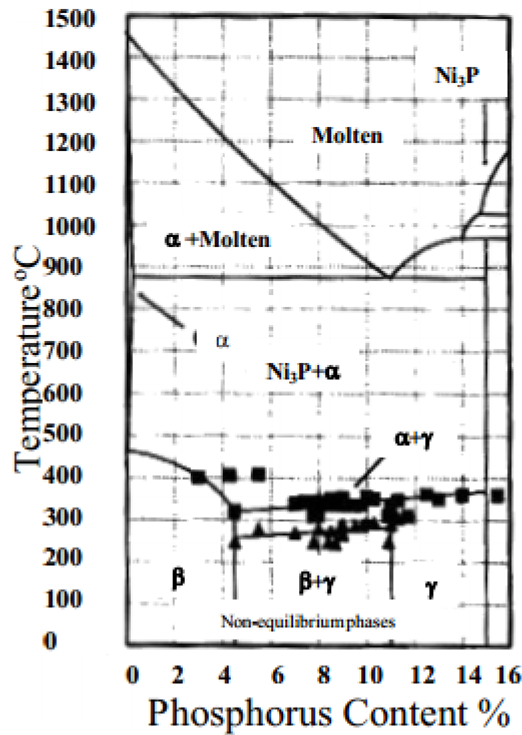


Figure 59: Non-equilibrium as-deposited NiP phase diagram [60]

Between approximately 4.4% and 11% P by weight, the alloy microstructure is composed of a dispersion of these two phases, producing substantial intrinsic tensile stress [60]. Importantly, the non-equilibrium structure is destroyed when heated above about 250C.

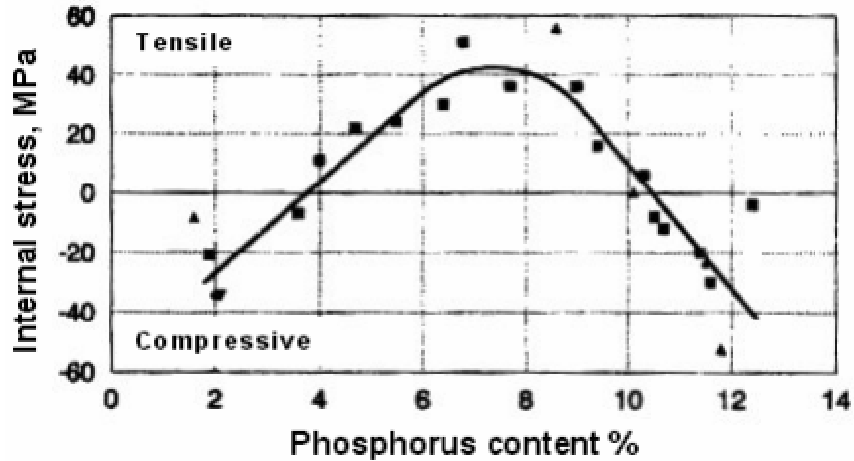


Figure 60: Intrinsic NiP stress vs phosphorous concentration [60]

Minimization of internal stress recommends selection of a NiP alloy composed of either entirely β (4.4% P or less) or entirely γ (11% P or more). Because 11% P is also optimal for reflectivity reasons, it is the natural choice.

Finally, the extrinsic stress, which is largely a product of a different coefficient of thermal expansion from the substrate, must be addressed.

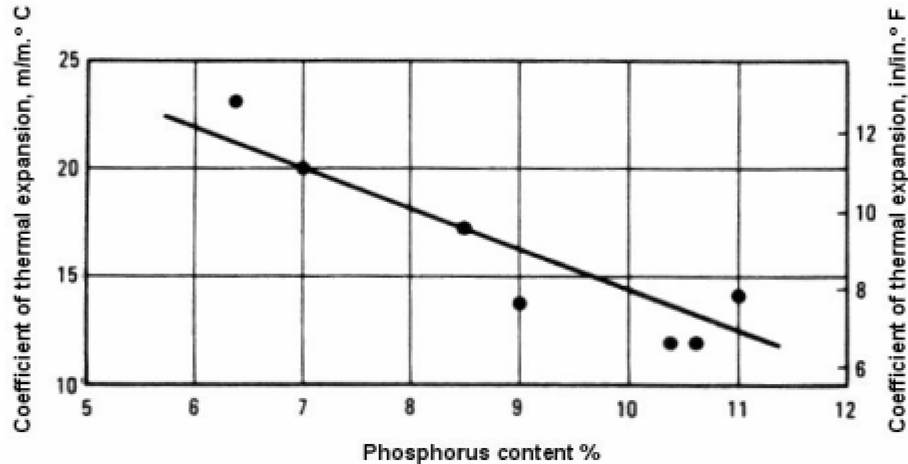


Figure 61: Coefficient of thermal expansion in NiP vs P concentration [62]

The coefficient of thermal expansion of PVD Nickel is approximately $13\,\frac{\mu m}{m*C^{\circ}}$, which matches very well with the value at 11% P in the deposit, according to Figure 61. The coefficient for silicon is lower, at about $2.6\,\frac{\mu m}{m*C^{\circ}}$ [12], but because lower concentrations of phosphorous have higher coefficients of thermal expansion, 11% remains the best choice.

8.2.3 Minimizing the Viscoelastic Response

As discussed in Section 6.1.2, the metal films deposited onto the surfaces of previous micromirrors produced a viscoelastic effect in the device. These effects was produced via two mechanisms. The magnitude of effect of these effects were proportional to

1) The inverse of grain size
2) Dislocation concentration

Because NiP-γ is amorphous, there are neither grains nor dislocations. Thus, the drift of point defects and the bowing of dislocations cannot occur and no viscoelastic effect will result from the previously-studied mechanisms.

However, metallic glasses are known to be viscoelastic materials, with a non-zero strain rate [63]. Fortunately, this strain rate has an Arrhenius dependence on temperature, and so it is hoped that the strain rate for room temperature operation is negligible.

If it is not negligible, however, the deformation due to the strain rate is non-recoverable and will quickly destroy the devices. Very little is known in the literature about the strain rate of NiP alloys, and so the performance of the devices must be observed to determine whether the reduction of viscoelastic response has been successful.

8.2.4 Maximizing Material Yield Strength

It is important to select a material with a high yield stress, so that no yielding occurs in the hinges. Unfortunately limited data exists for phosphorous concentrations above 10%, but Figure 62 makes it clear that a high-phosphorous NiP alloy will display the greatest tensile strength and ductility.

A final accounting of mechanical data, based on empirical results for 11% P amorphous NiP, can be found in Table V.

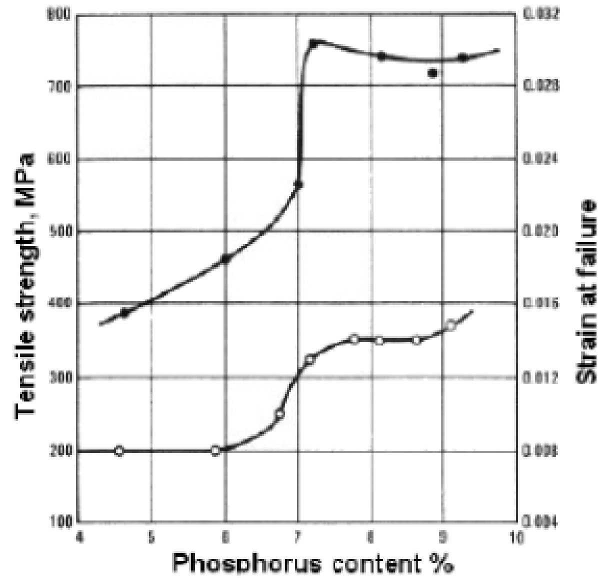


Figure 62: NiP tensile strength and failure strain vs P concentration [62]

Table V: Material properties of as-deposited NiP alloy [64] [65]

Material Parameter	Value
Phosphorous by weight	11%
Density	$7.75\ g/cm^3$
Electrical resistivity	$90\ \mu\Omega \cdot cm$
Coefficient of thermal expansion	$12 \frac{\mu m}{m * C^{\circ}}$
Modulus of elasticity	$114\ GPa$
Tensile strength	$700 - 750\ MPa$
Yield strength	$\sim 700\ MPa$
Poisson's ratio	0.3539

8.3 Selected Final Device Parameters

Considering the constraints of Section 6.2, the following device parameters were selected for initial fabrication:

Table VI: Final Device Parameters

Variable	Value	Description
d	$20\ \mu m$	Electrode separation
W	$100\ \mu m$	Mirror width
ℓ	$100\ \mu m$	Length from hinge axis to mirror edge
ℓ_1	$10\ \mu m$	Distance from hinge axis to electrode
ℓ_2	$20\ \mu m$	Distance from electrode to mirror edge
L	$100\ \mu m$	Hinge length
a	$16\ and\ 24\ \mu m$	Hinge width
b	$5\ \mu m$	Device thickness

Four distinct device designs were created using these parameters: a serpentine and a straight-beam device with 16 micron wide hinges, and a serpentine and a straight-beam device with 24 micron wide hinges. The dimensioned drawings of these devices can be found in Appendix A.

It is worth noting that for the constraint of $10°$ of tilt and the selected device parameters,

$$\sin 10° \leq \frac{20\ \mu m - \delta_{\max}}{100\ \mu m} \quad \text{(Equation 58)}$$

And so

$$\delta_{\max} \leq 2.635\ \mu m \quad \text{(Equation 59)}$$

8.4 Mask Layout

As discussed in section 6.2.6 Actuation, it is an important requirement that the mirror does not discharge on snapdown. As a result, the connection of the electrostatic traces to the actuating electrode must not be in the path of the tilting

mirror, and the electrode must also not extend into the rotational path of the mirror. This design requirement is given by

(Equation 60)

$$(\ell - \ell_2)^2 < \ell^2 - (d - \boldsymbol{\delta}_{\mathbf{max}})^{\mathbf{2}}$$

Or

(Equation 61)

$$2\ell\ell_2 - \ell_2^2 > (d - \boldsymbol{\delta}_{\mathbf{max}})^{\mathbf{2}}$$

For the selected design, this means $\delta_{\max} < 80\mu m$. Since $\delta_{\max}$ can be no greater than $d = 20\mu m$, the condition is fulfilled and there will be no discharge on snapdown. If $\delta_{\max} = 0\mu m$, the minimum value of ℓ_2 given $d = 20\mu m$ and $\ell = 100\mu m$ is about $\ell_2 = 2\mu m$. However, a much larger value was selected because of the risk of lateral misalignment during processing, and because snapdown discharge will lead to rapid failure.

In order to avoid placing the actuating trace in the path of the mirror, a wide "snapdown pad" was created by splitting the trace into two and routing it symmetrically around each side of the landing area. This is visible in Figure 63.

Figure 63: Schematic of device traces

To facilitate grounding of the devices, the “support pillars” of each device are connected in series. They could not be connected in parallel, because they would otherwise intersect the biasing traces. Each row of devices, alternating between the four designs from left to right, is connected to solder pads at the edge of the wafer. Figure 64 omits the snap-down pads shown in Figure 63 for clarity.

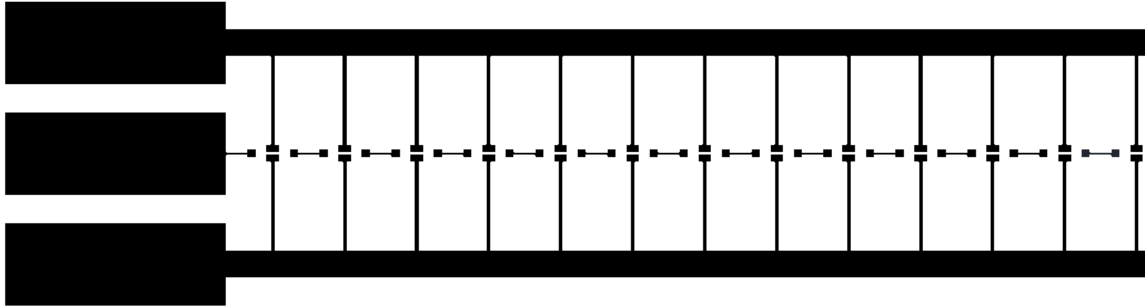


Figure 64: Part of one row of device traces and electrodes

All 5 mask layers used for processing may be found in Appendix B.

8.5 FEA Results

In order to model the behavior of the devices, the SolidWorks FEA simulation was used. However, the Solidworks FEA simulation is not a multiphysics package, and so a constant force was assumed on the surface of the mirror to produce the tilt. Although this is not an accurate model for electrostatic actuation, it provided useful information about the relative force required to actuate each device, the “hinge pull” effect for each design, and the maximum von Mises stress in each device at snapdown.

Using a solid model of each design with nickel-phosphorous material properties, a distributed force was applied normal to the region of the mirror located directly above the electrode.

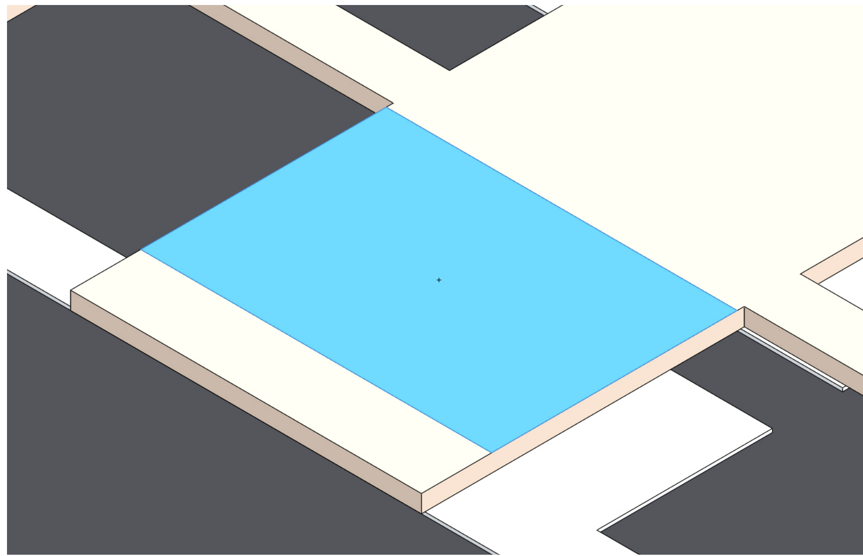


Figure 65: Force application zone

A variety of forces were tested for each design to find the range over which the mirror tilted appreciably. Two forces, one in the middle of the non-contact range, and one barely producing surface contact, were selected for simulation.

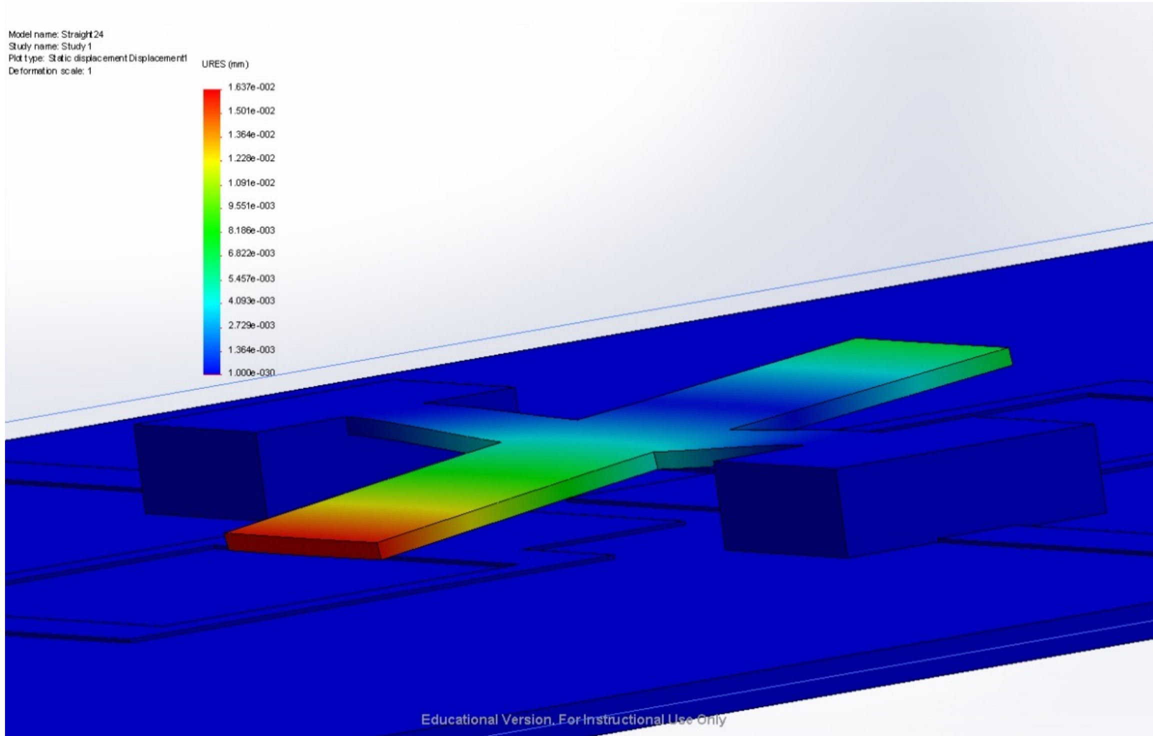


Figure 66: Non-contact displacement of 24-micron straight-beam

The vertical displacements of a variety of nodes along the edge of the mirror were collected from the resulting displacement plot.

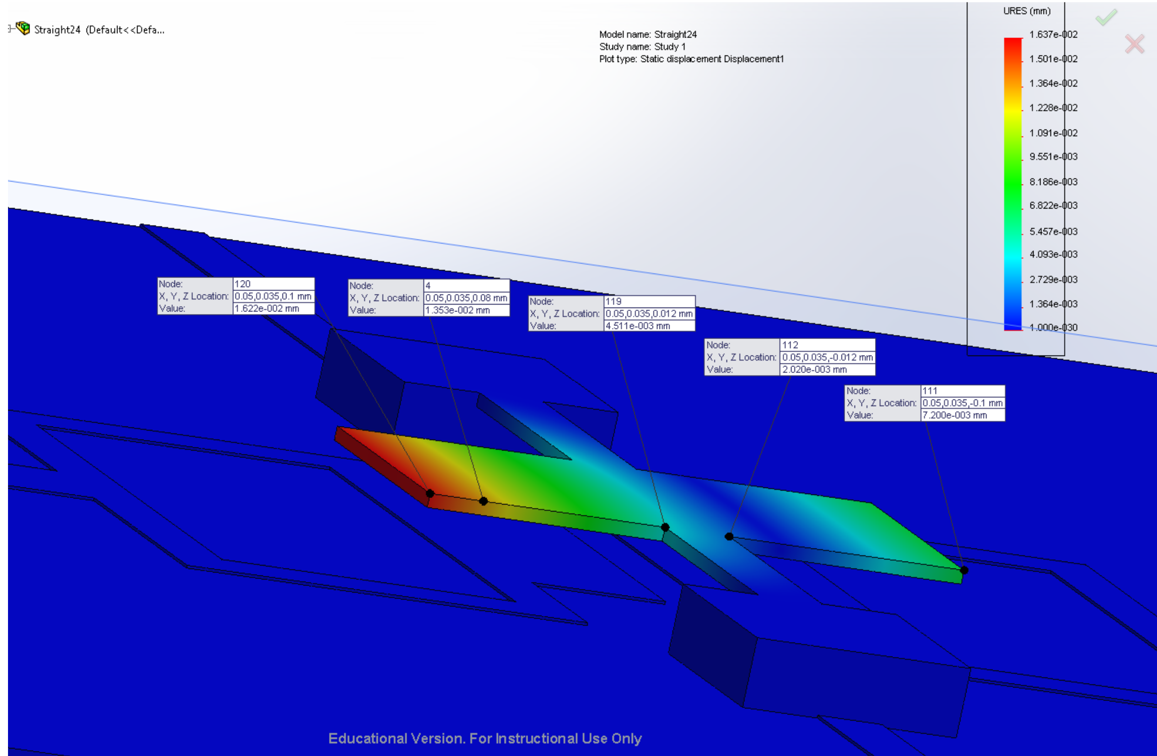


Figure 67: Tabulating displacement vs position

These displacement values were plotted against position, and a line was fitted to the data. The arctangent of the slope of this line provides the tilt angle of the device, and the y-intercept provides $\delta_{\max}$. Furthermore, a high coefficient of determination for the fitted line verifies the assumption of a rigid mirror surface in the analytic model.

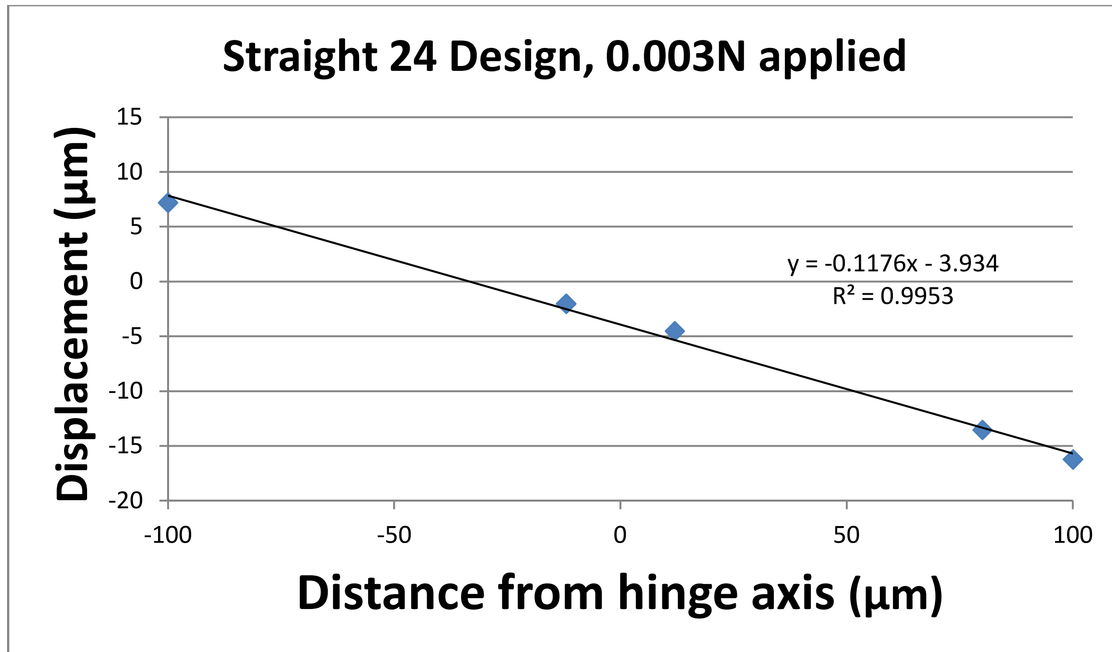


Figure 68: Regression of displacement vs position

The maximum von Mises stress was also recorded for comparison against the material yield strength, $\sigma_{YS} = 700\ MPa$. This process was repeated for all four designs, with two forces each. The results are summarized in Table VII. The complete FEA results can be found in Appendix C.

Table VII: Summary of FEA results

Design	Force	Contact?	θ	$\delta_{\max}$	R^2	von Mises
Straight 24	$0.003\ N$	No	$6.707°$	$3.939\ \mu m$	0.9953	$152.5\ MPa$
	$0.0045\ N$	Yes	$8.284°$	$4.794\ \mu m$	0.9958	$196.3\ MPa$
Straight 16	$0.002\ N$	No	$7.080°$	$4.486\ \mu m$	0.9972	$152.4\ MPa$
	$0.003\ N$	Yes	$\mathbf{8.604}°$	$4.447\ \mu m$	0.9980	$180.9\ MPa$
Serpentine 24	$0.001\ N$	No	$6.017°$	$4.022\ \mu m$	0.9992	$109.4\ MPa$
	$0.0015\ N$	Yes	$8.037°$	$5.625\ \mu m$	0.9992	$153.7\ MPa$
Serpentine 16	$0.0005\ N$	No	$5.023°$	$3.488\ \mu m$	0.9982	$70.4\ MPa$
	$0.001\ N$	Yes	$7.902°$	$6.284\ \mu m$	0.9970	$119.9\ MPa$

According to the FEA results, the devices do not yield at snapdown but do have difficulty obtaining 10 degrees of tilt due to substantial hinge pull. This effect is worse for the serpentine devices. Although the severity of the effect is

exaggerated by the simulation because the force is evenly distributed through the rotation, it is evident that thin, straight beam hinges are the best design given the requirements. To further reduce the “hinge pull” behavior, future devices might halve the hinge length and width. Halving the length will reduce the vertical deflection resulting from force at the hinges by a factor of 8, and halving the hinge width will double the vertical deflection per unit force but substantially reduce the torque needed to obtain tilt, and thus reduce the force at the hinges.

The primary benefit of the serpentine devices appears to be lower von Mises stress. Although it also provides greater deflection for a given force and hinge thickness, this comes at the cost of greater vertical deflection than would result from simply reducing the hinge thickness. The serpentine design would therefore be most appropriate in cases where very large tilt angles are desired, perhaps above 45 degrees, to avoid brittle fracture of the hinge material (or plastic deformation in crystalline materials).

9. Process Development

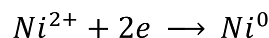
Having obtained a detailed design for the devices, a detailed process for their fabrication was needed. Because some of the steps outlined in the generic process flow proposed in Section 7.3.2 were similar or identical to those used previously in the planar process, they required little optimization or development.

The primary focus, therefore, was the deposition process. This could be reduced to three distinct components:

1) The surface preparation, whether a cleaning, sensitizing or activating step or the deposition of a catalytic seed layer
2) The ELD process capable of depositing the amorphous NiP alloy to the thickness desired for the step, at a concentration of 11% P, with good substrate adhesion, low film stress, high planarity and high reflectivity
3) The thick photoresist spin-coating program, capable of spin-coating a layer of photoresist to a uniform thickness of 20 microns to form the device supports and a uniform thickness of 5 microns to form the device layer, and which would be totally unreactive with the ELD solution

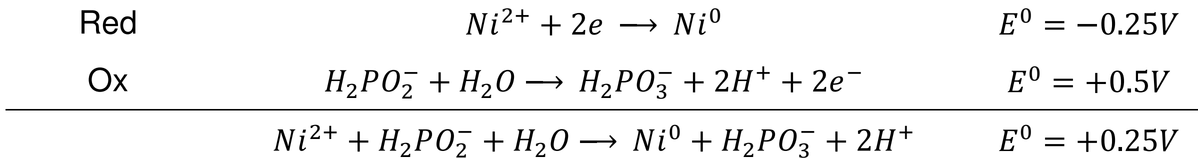
9.1 Introduction to ELD

Fundamentally, electroless nickel functions via the same reduction half-reaction as nickel electroplating [52],



$$Ni^{2+} + 2e \longrightarrow Ni^0$$

but the reducing electrons are supplied by a reducing agent, rather than via an electrical current. Assuming the use of the hypophosphite ion as the reducing agent, since its co-deposition is necessary for a nickel-phosphorous alloy, the half-reactions are [53]



Red	$Ni^{2+} + 2e \longrightarrow Ni^0$	$E^0 = -0.25V$
Ox	$H_2PO_2^- + H_2O \longrightarrow H_2PO_3^- + 2H^+ + 2e^-$	$E^0 = +0.5V$
	$Ni^{2+} + H_2PO_2^- + H_2O \longrightarrow Ni^0 + H_2PO_3^- + 2H^+$	$E^0 = +0.25V$

$\Delta G^0 = -nFE^0 < 0$ and the reaction proceeds spontaneously.

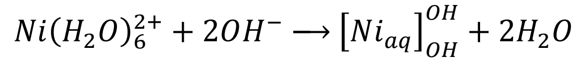
However, this reaction does not account for co-deposition of phosphorous, and there are many intricacies to the reaction. The original discovery of electroless nickel reduction in 1844 by Wurtz [66] consisted of nothing more than the spontaneous reduction of nickel cations into a black powder precipitate. Over 100 years later, in 1946, Brenner and Riddell published the first paper describing the necessary conditions to obtain an ELD solution that did not decompose spontaneously or form deposits onto the walls of the container [67].

A variety of mechanisms to explain all phenomena involved with the electroless deposition reaction have been proposed over the years, receiving the support of various authors [53]. The most comprehensive mechanism proposed to date, proposed by Cavalotti and Savalgo, involves the following [68]:

1) Ionization of water at the surface of a hydrogenation-dehydrogenation catalyst, such as nickel:

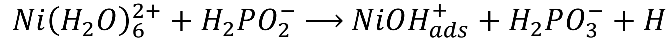
$$2H_2O \longrightarrow 2H^+ + 2OH^-$$

2) Coordination of hydroxyl ions to hydrated nickel ions:



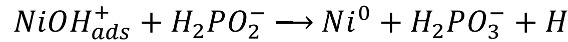
$$Ni(H_2O)_6^{2+} + 2OH^- \longrightarrow [Ni_{aq}]_{OH}^{OH} + 2H_2O$$

3) Reaction of hydrolyzed nickel with hypophosphite:



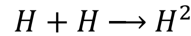
$$Ni(H_2O)_6^{2+} + H_2PO_2^- \longrightarrow NiOH_{ads}^+ + H_2PO_3^- + H$$

4) The nickel deposition step:



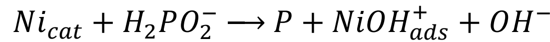
$$NiOH_{ads}^+ + H_2PO_2^- \longrightarrow Ni^0 + H_2PO_3^- + H$$

5) Simultaneous evolution of hydrogen from the two previous steps:



$$H + H \longrightarrow H^2$$

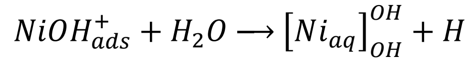
6) Notably, by a side reaction, the phosphorous deposition is produced:



$$Ni_{cat} + H_2PO_2^- \longrightarrow P + NiOH_{ads}^+ + OH^-$$

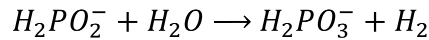
The adsorbed hydrolyzed nickel product may be returned to the bulk by step 4.

7) Additionally, a desorption reaction which competes with step 4:



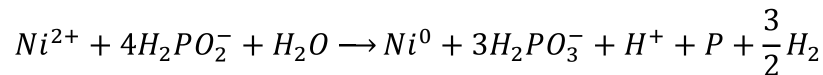
$$NiOH_{ads}^+ + H_2O \longrightarrow [Ni_{aq}]_{OH}^{OH} + H$$

8) Finally, the side reaction of hypophosphite with water:



$$H_2PO_2^- + H_2O \longrightarrow H_2PO_3^- + H_2$$

Supporting work by Randin and Hintermann proposed an overall reaction [69]:



$$Ni^{2+} + 4H_2PO_2^- + H_2O \longrightarrow Ni^0 + 3H_2PO_3^- + H^+ + P + \frac{3}{2}H_2$$

This implies that four hypophosphite ions are consumed during the deposition of each nickel ion.

It must be emphasized that $[Ni_{aq}]_{OH}^{OH}$ in fact represents loose bonding of the hydroxide ion in the hydration shell of the nickel ion, and not nickel hydroxide precipitate. Formation of nickel hydroxide will prevent reaction with the hypophosphite.

Also notable in the equivalent reaction is the presence of the hydrogen ion in the products. There is, unsurprisingly, a deleterious impact of low pH on the deposition rate. Low pH simultaneously increases the P concentration in the deposited film, which can be understood by examination of step 6.

Because the pH of the solution is a factor which has a direct and significant impact on the plating process, it is imperative that good pH control be achieved by buffering the bath. Without an effective buffer, the pH of the bath will decrease over time, affecting the plating rate, P concentration, and quality of the deposit. If pH drifts too much, plating may cease entirely.

Similarly to the hydrogen ion concentration, the concentration of free nickel ions in solution has a strong influence on the reaction rate and concentration of phosphorous in the deposit. By adding complexing agents to the solution, some fraction of the nickel ions will be complexed, and if the standard electrode potential of the reduction half reaction of chelated nickel is sufficiently smaller than for uncomplexed nickel, they will be unavailable for deposition.

Specifically, if $\Delta E^0_{red_{chelated}} - \Delta E^0_{red_{uncomplexed}} < \Delta E^0_{ox} + \Delta E^0_{red_{uncomplexed}}$, or equivalently $\Delta E^0_{red_{chelated}} - \Delta E^0_{red_{uncomplexed}} < 25mV$ then $\Delta E^0 < 0$. Thus $\Delta G^0 = -nFE^0 > 0$, and spontaneity is not implied.

Furthermore, the reaction cannot proceed faster than the rate of dissociation of the chelating agents. The concept of unchelated metal ion concentration, pM, may be usefully compared to the analogous concept of pH [53], where the complexing agents act as "buffers" for the nickel concentration in solution. Suitable organic acid salts may fulfill a dual role as both buffers and complexants.

Beyond the necessary components of metal ions, reducing agents, complexing agents, and buffer agents, commercial electroless deposition solutions frequently include accelerators and stabilizers. Stabilizers are useful to limit the formation of nodules (see Section 9.2.7) and prevent sudden and unpredictable spontaneous decomposition of the solution [70].

This spontaneous decomposition of the solution occurs when plating initiates on particles of near-colloidal size in the solution. Once initiation occurs on these particles, the surface area of nickel in the solution rises dramatically, and the solution rapidly "plates out", turning black as the nickel nanoparticles grow. Although the rate of nickel chelate dissociation will help limit the progression of this reaction, complexing agents can neither prevent plate-out, nor stop it once it begins.

Stabilizers substantially reduce the possibility of this sudden bath decomposition by generally inhibiting homogenous nucleation, at the cost of also depressing the plating reaction. Accelerators are used to compensate for the loss of plating rate associated with stabilizer use.

Unfortunately, the most effective stabilizers, particularly to combat nodule formation, are heavy metal ions such as Pb^{2+}. Because of the health hazard, stabilizers were not considered for any ELD formulations in this thesis.

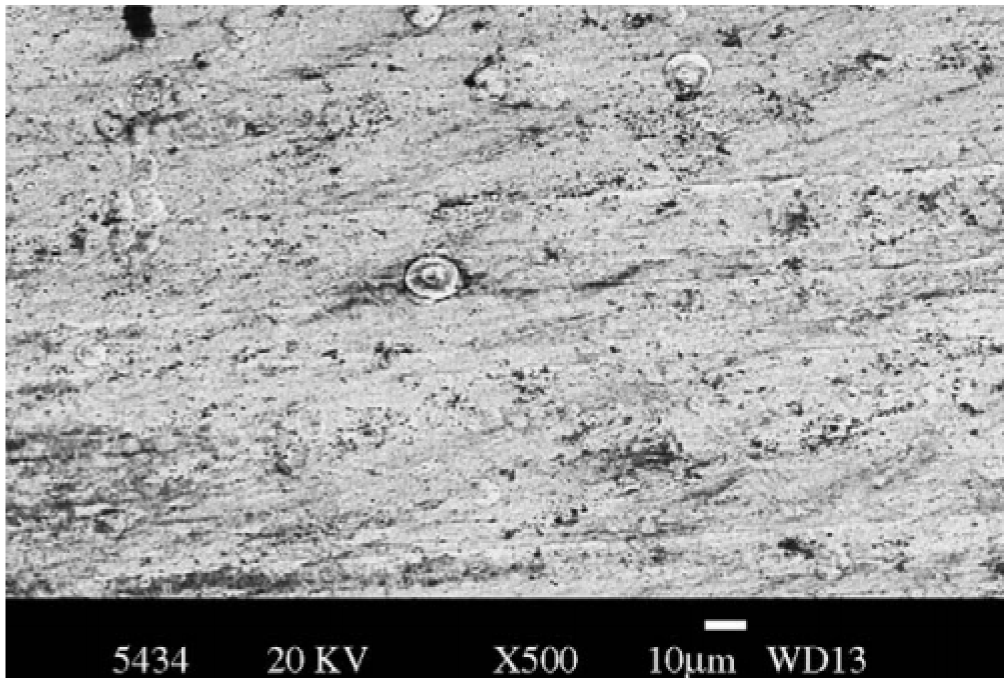


Figure 69: 11% P deposit obtained using 1ppm lead acetate [70]

Additionally, surfactants are known to enhance wetting of the plating surface, and promote smoothness of the deposit [71]. Particularly for plating small features like the hinge of a micromirror, it is beneficial to include a surfactant in the plating bath.

To summarize, the constituents of modern nickel-phosphorous ELD solutions often include [72]:

Table VIII: Makeup of ELD solution

Constituent	Purpose	Sources/Examples
Nickel ions	Metal source	Nickel chloride, nickel sulfate, nickel acetate
Hypophosphite ions	Reducing agent	Sodium hypophosphite, potassium hypophosphite
Complexants	Complex Ni, prevent precipitation of Ni phosphate	Acetate, propionate, succinate, aminoacetate, citrate, etc.
Buffers	Long-term pH regulation	Salts of some complexants
Surfactants	Increase surface wettability	Triton X-100
Accelerators	Accelerate deposition rate	Fluorides, borates, anions of mono- and di-carboxylic acids
Stabilizers	Shield active nuclei	Thiourea, ions of Pb, Sn, As, Mo, Cd, Th, Sb, etc

The final ingredients to produce deposition on a catalytic surface from a hypophosphite ELD solution are energy in the form of heat, and an appropriate pH. Typically, solutions are operated in the temperature range of 60-95℃ and a pH of 4-6.

In industry, ELD solutions are reused by replenishing the nickel ions, in order to spare the cost of a new bath makeup. However, the baths have a finite life; after about 5 turnovers – that is, a total Ni^{2+}consumption of 5 times the initial concentration – the age of the bath begins to have an impact on the deposit, particularly the internal stress, ductility, fatigue resistance, and phosphorous content [73].This effect is attributed to the decomposition of chemicals in the

bath, including the complexants and accelerators, but also to the buildup of phosphite, a reaction side-product.

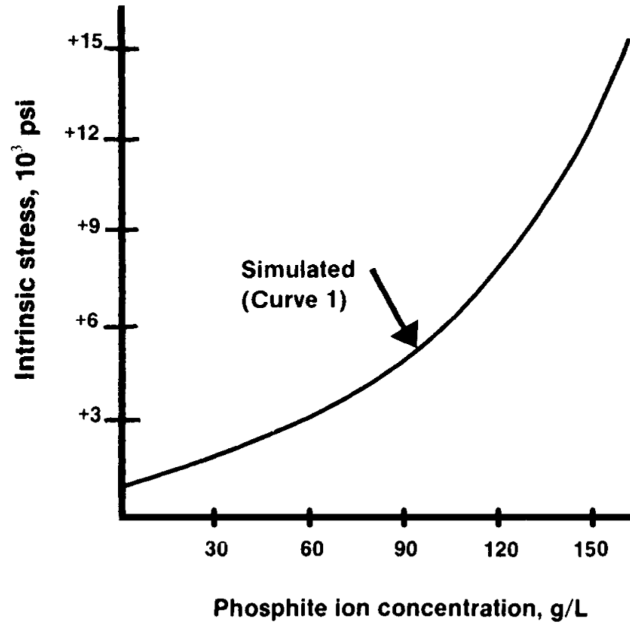


Figure 70: Phosphite concentration vs intrinsic stress in deposit [53]

9.2 ELD Constraints

It was believed that developing an electroless chemistry from scratch would provide the greatest latitude and a deposit of the highest quality. Before this chemistry could be developed, however, an understanding of the requirements and constraints was needed.

9.2.1 Basic Considerations

The success criteria for the ELD bath were the ability to deposit an amorphous, 11% P NiP to a thickness of either 5 or 20 microns, with good substrate adhesion, low film stress, high planarity and high reflectivity.

A critical requirement was that the NiP could not deposit onto the photoresist mold. If it did so, the deposited layer would not be conformal, and it would become difficult to strip the photoresist after completion of processing. Further, it could not plate onto silicon oxide, so that the backside of the wafer would be shielded from deposition.

Additionally, the chemistry had to be compatible with a glass beaker, where deposition would occur with stirring and heat provided by hotplate. This meant that fluoride ions could not be added to the solution– in the low pH chemistry, etching of the glass beaker would result. Further,

The ELD solution would also need to plate onto small features on the wafer, such as the hinges of the mirror, at a rate comparable to larger features, and do so in the presence of photoresist.

Finally, the solution could not require replenishment of nickel ions, as there was no way to measure the nickel concentration during the deposition process. Since the volume of the deposit could be substantial, but the volume of the bath would be small, the concentration of nickel would therefore need to be large. Because commercial baths can achieve 5 turnovers before the bath age becomes a significant factor, it was approximated that the initial concentration of nickel could be about 5 times higher than in commercial baths in order to offset the need to replenish the nickel. This would require a correspondingly larger concentration of other constituents in the makeup.

9.2.2 Deposition Rate

Because the plating bath would be a relatively small volume of aqueous solution in a beaker at elevated temperature, water loss was a concern. Furthermore, a long process would provide more opportunity for drift of temperature or other process parameters. Therefore, the desired deposition time was no longer than 2 hours; since the thickest step was a 20 micron deposit, this implied a target rate of at least 10 microns per hour.

9.2.3 Plating on Silicon

Initially, it was believed that the substrate for deposition would be bare Si, and development was directed toward obtaining a chemistry capable of creating a thick deposit on Si.

However, it was later concluded that this added unnecessary complexity, particularly because of the palladium strike (Section 9.3.2) and the hydrophobicity of hydrogen-terminated silicon after removal of the native oxide [74], which produced tenacious bubbles on the surface, and corresponding unplated zones. The sputtered material used for the electrostatic traces could easily serve as the catalytic surface for the NiP deposit. The final chemistry and photomasks are not compatible with direct silicon deposition.

9.3 ELD Surface Preparation

9.3.1 Doped Si

P-doped silicon is reported to plate much faster than n-doped silicon, which is attributable to the photovoltaic effect and electronegativity of p-doped silicon [75].

Additionally, the adhesion of NiP is greater on p-doped silicon [49]. Therefore, its use was preferred.

Because the deposition reaction is catalytic only on the silicon surface, and not the oxide, it was first necessary to strip the oxide. After the removal of organic contaminants in a piranha solution, the silicon samples received a BOE dip.

Plating generally did not initiate on the p+ silicon, and where it was achieved, the NiP layers immediately flaked off, re-formed, and flaked off again. This extremely rapid delamination process rapidly contaminated the bath with thousands of pieces of NiP film, and resulted in bath decomposition.

Therefore, a more suitable surface preparation was pursued.

9.3.2 Palladium Strike

The literature includes many examples of palladium activation of a silicon surface for electroless nickel deposition [47] [48] [49] [76] [77] [78]. A variety of different mixtures were attempted based on published results, in order to produce better initiation and adhesion of the ELD process on silicon.

The most effective formulation for the Pd strike was

Table IX: Preparation of palladium strike

Component	Quantity
1% Hydrofluoric acid	215 mL
Ammonium Fluoride	2.79 g
0.1 M Hydrochloric acid	1.5 mL
Palladium Chloride	10 mg

The palladium chloride was dissolved in the hydrochloric acid before mixing.

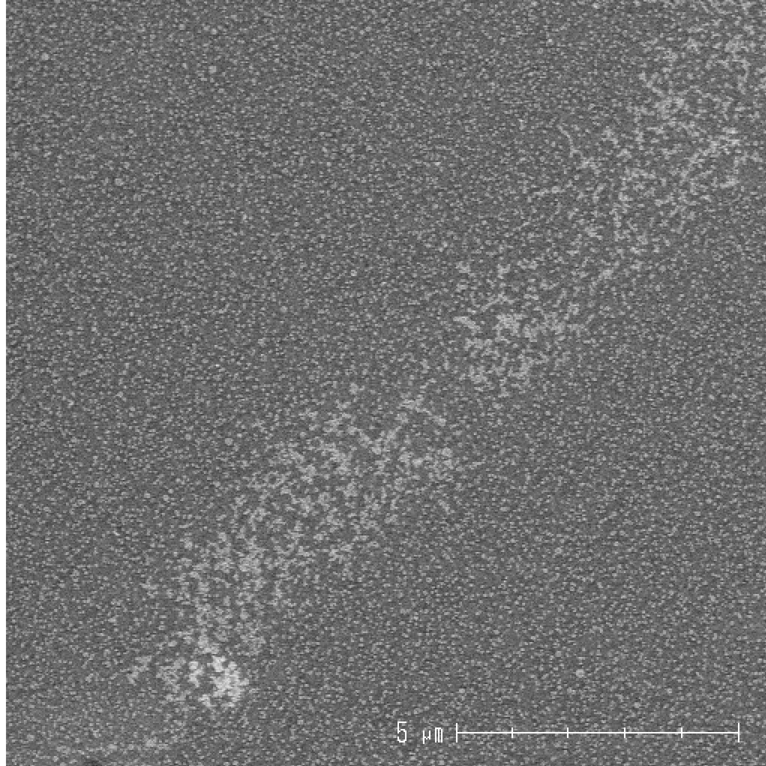


Figure 71: Uneven distribution of Pd nuclei on silicon surface

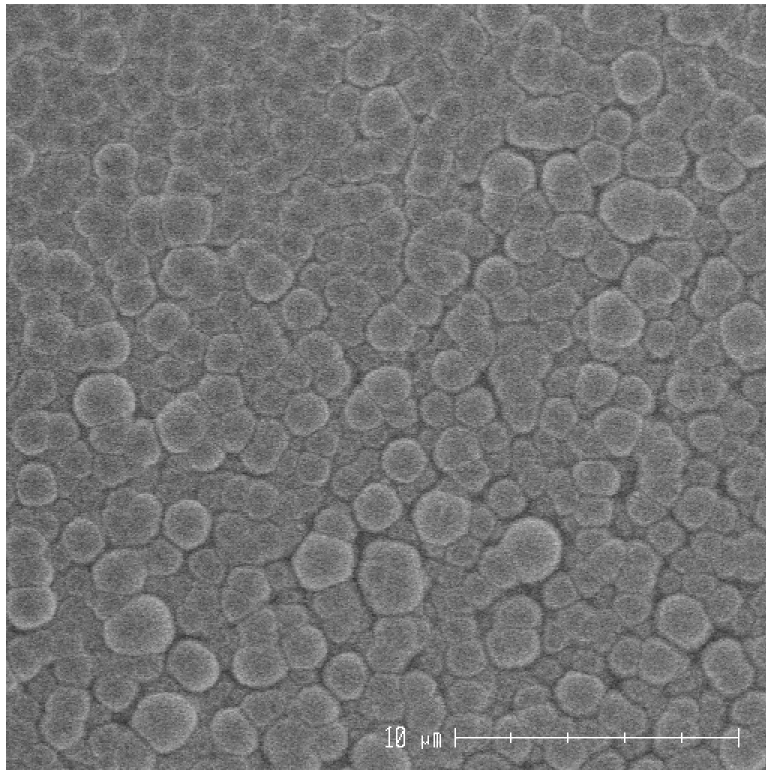


Figure 72: Highly nodular film resulting from palladium nuclei

However, it was observed that the distribution of the palladium nuclei on the silicon substrate was sparse and uneven, producing a highly nodular deposit with poor uniformity. Worse, the palladium nuclei sometimes appeared to dislodge from the silicon surface, encouraging plate-out of the unstabilized bath. Further, loose palladium nuclei in solution could bond to photoresist, producing undesirable non-uniformities. It was therefore considered an undesirable method.

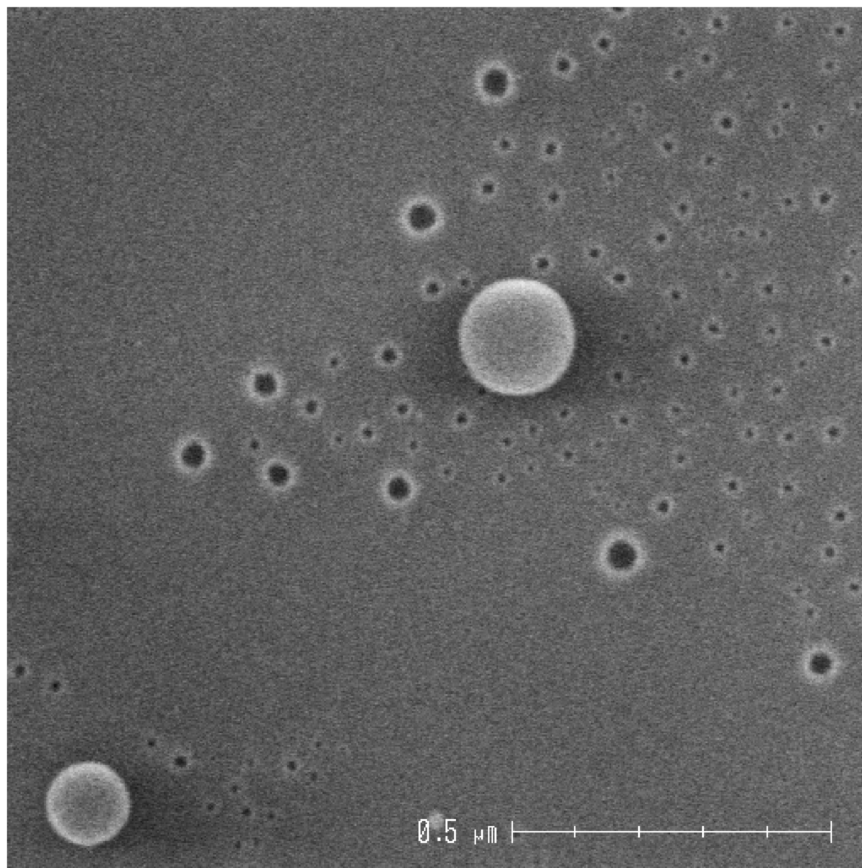


Figure 73: Stray Pd nuclei producing nodules on photoresist

9.3.3 PVD Ruthenium

Following the abandonment of direct-silicon ELD, PVD Ru was explored as a highly unreactive and catalytic substrate. Good adhesion and highly uniform deposits were observed on Ru.

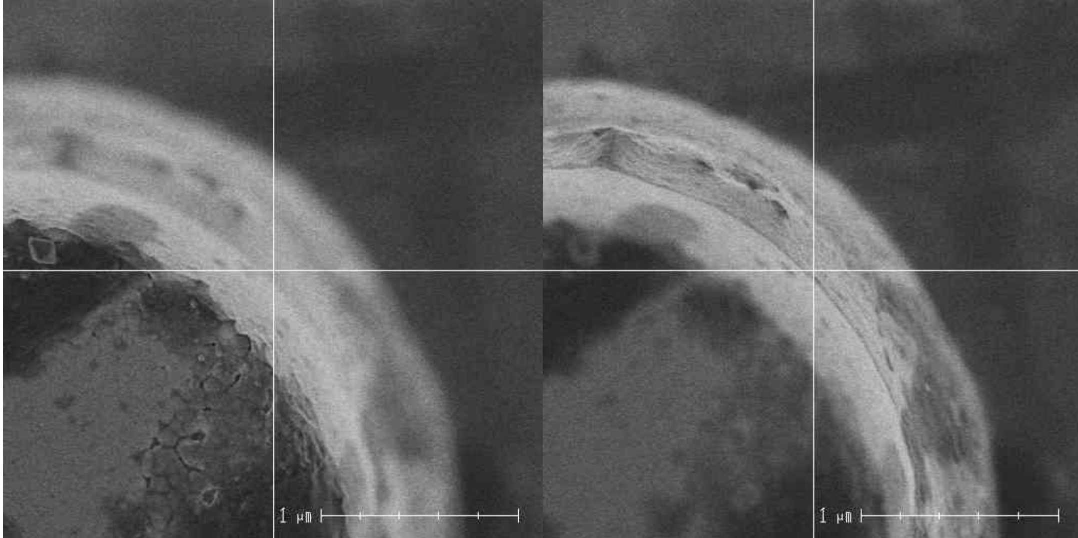


Figure 74: Organic contamination on a Ru surface provides a section view of the deposited NiP film, estimated to be 8 microns thick.

However, large and unusual defects were observed on the Ru substrate. No suitable explanation for these defects was found, and no solutions were offered in the literature.

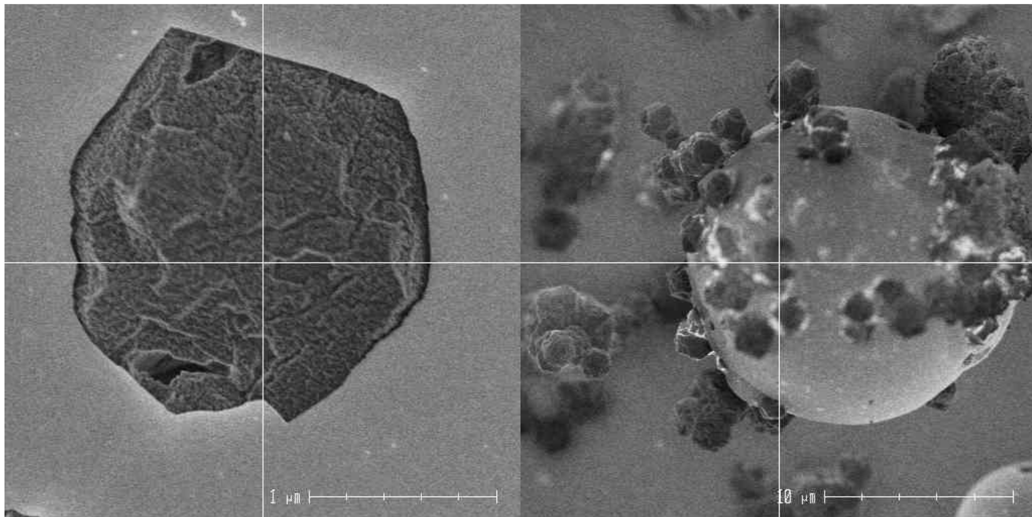


Figure 75: Defects observed on Ru

Regardless, a method to deposit PVD Ruthenium was not available in the Cal Poly cleanroom, so although it was useful for development of the ELD solution, it could not be integrated into the final process.

9.3.4 PVD NiTi

A sputtered stoichiometric NiTi seed layer was initially regarded as a good choice because of its nickel content and high adhesion to silicon. However, there were inconsistent difficulties initiating deposition on bare NiTi that appeared to be associated with the age of the deposit. This was attributed to the non-catalytic, 10-15 nm thick TiO_2 native oxide which forms on the surface [79].

9.3.5 PVD NiV

As discussed in Section 7.1, ferromagnetic materials cannot be safely sputtered with a magnetron, and so pure Ni cannot be deposited as a seed layer in the Cal Poly Microfabrication Lab. However, alloying 7% vanadium into the target completely removes the ferromagnetic character above approximately 250K [80].

Although this initiation layer was never tested, it is believed that it would serve as a catalytic layer without additional treatment, because of its chemical similarity to nickel. Furthermore, the coefficient of thermal expansion of the primarily nickel alloy was expected to be comparable to bulk nickel, which would match well with the thermal coefficient of the deposit and minimize thermal expansion. However, little data is available in the literature to support this conclusion.

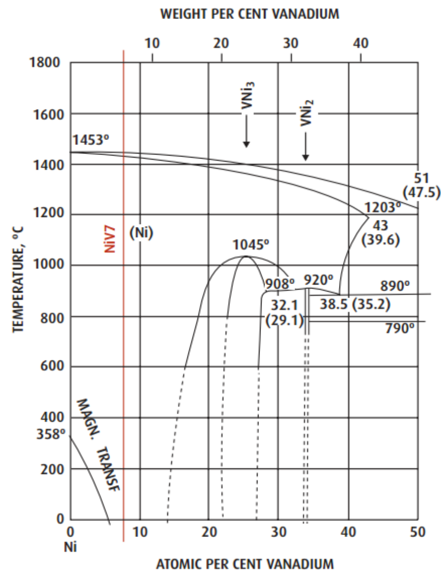


Figure 76: NiV phase diagram confirms 7% V is a solid solution in Ni [81]

9.4 ELD Process Development

9.2.1 Selection of Nickel Source

Common compounds used to deliver nickel ions into ELD solution include nickel sulfate, nickel chloride, and nickel acetate. Because it is the cheapest of these, nickel sulfate is the most widely used. However, nickel acetate was selected for this application because of the complexing acetate ion it would bring into solution.

9.2.2 Selection of Complexation Agents

To compensate for the large Ni^{2+}concentration, approximately 5 times that of commercial baths, approximately 5 times the concentration of complexing agents would be necessary as well. A variety of complexation agents were tested during development of the solution. Ligands tested included acetate, citrate, lactate, succinate, and ammonium. The final selections of acetate and citrate served as pH buffers.

9.2.3 Selection of pH and Buffer System

Before an appropriate buffer system could be selected, the effect of pH on the process needed to be understood. A lower solution pH increases stability of the bath [53], which was critical without the addition of a stabilizer. Furthermore, a low pH increases the phosphorous concentration of the deposit, though at the cost of deposition rate.

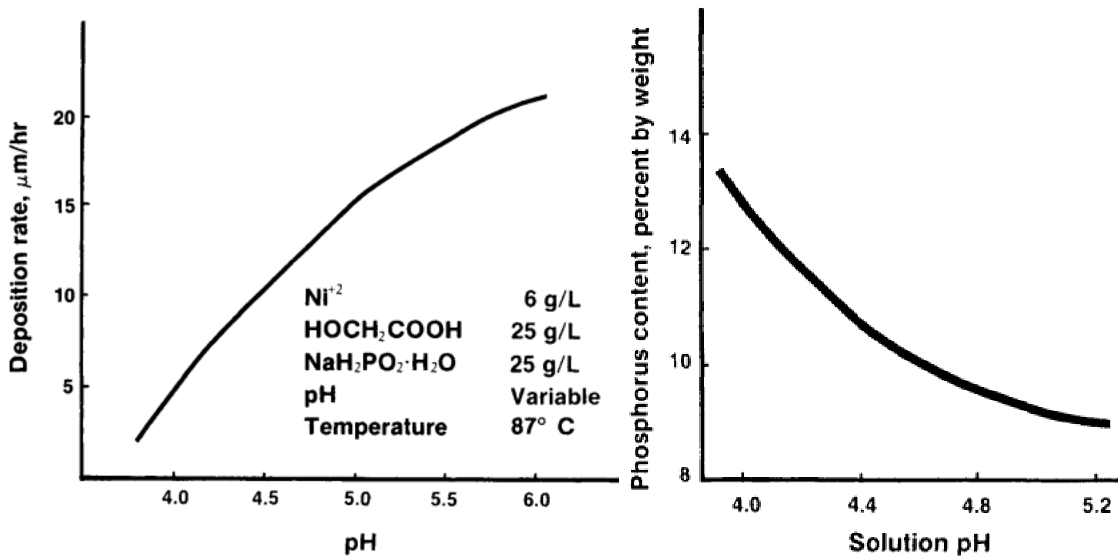


Figure 77: Deposition rate and deposit %P vs solution pH [53]

A pH of 4.5 was selected, and it was understood that the resulting low deposition rate would need to be compensated for through manipulation of other solution parameters.

Ammonium acetate, with pKas of 4.75 and 9.25, acts as an effective buffer without the addition of acetic acid. The pKa of 4.75 supports stability of the 4.5 pH, and both the ammonium and acetate ions contribute to the chelation of the nickel.

9.2.4 Determination of Concentrations

The optimal stoichiometric ratio of $Ni^{2+}$to $H_2PO_2^-$, as established in Section 9.1, is 1:4, or 0.25. However, a variety of side reactions impact the real ideal mixture.

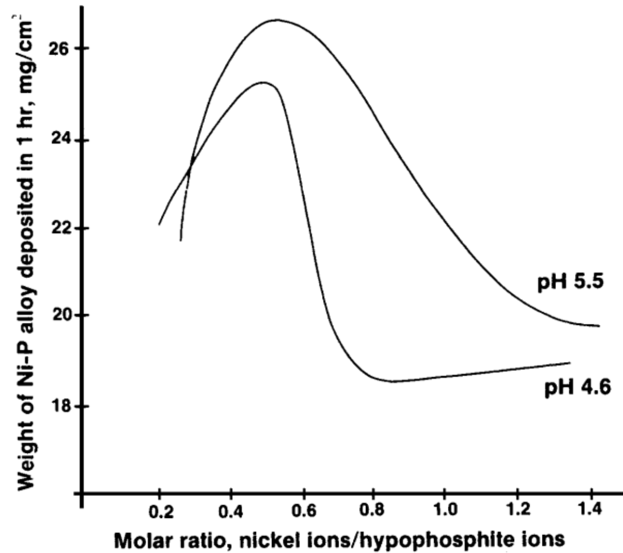


Figure 78: Deposition rate vs molar ratio of $Ni^{2+}$to $H_2PO_2^-$ [53]

Testing revealed that a ratio of 0.472 $Ni^{2+}$to $H_2PO_2^-$ was ideal, and this was used in the final formulation.

As mentioned previously, a high concentration of nickel was desirable in order to eliminate the need to add nickel to the bath during the deposition. Fortunately, there is little dependence of phosphorous concentration in the deposit on the Ni^{2+} beyond a few grams per liter, and so the changing concentration of the large quantity of nickel in solution during deposition would have little effect.

To compensate for the loss of phosphorous concentration in the deposit, a greater concentration of $H_2PO_2^-$ was beneficial, as phosphorous content in the film is proportional to the hypophosphite. This larger concentration of hypophosphite allowed the desired ratio of 0.472 $Ni^{2+}$to $H_2PO_2^-$ to be maintained.

Both sodium hypophosphite and potassium hypophosphite were used interchangeably during solution development.

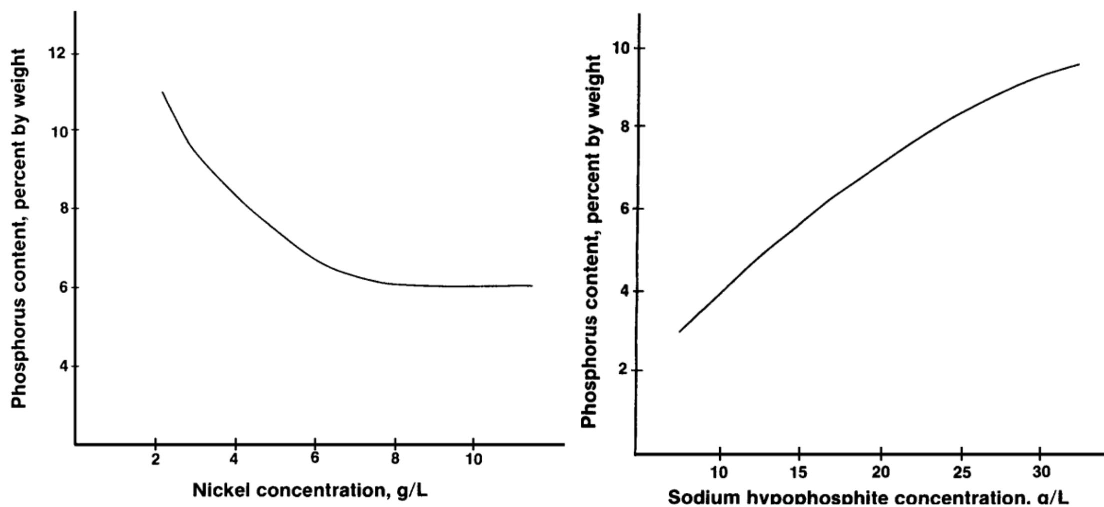


Figure 79: Deposited phosphorous concentration vs $Ni^{2+}$and $H_2PO_2^-$ [53]

9.2.5 Additives

Sodium saccharin has been proven to reduce film stress and increase brightness in the deposit [37]. Although it was tested a variety of concentrations in solution, it did not make a noticeable impact on the resulting film quality and was left out of the final formulation.

It is believed that saccharin's mechanism of action may be dependent on suppressing growth along certain crystal planes, and so has little effect on a fully-amorphous deposit.

A surfactant, Triton X-100, was added to increase wettability.

Citric acid was used to adjust the solution pH to 4.5. Citrate also serves as a strong nickel complexant.

Various other additives exist but were not explored.

9.2.6 Operating Temperature

There is a strong dependence on the plating rate on temperature; increasing the temperature by 10℃ may double the reaction rate [53]. However, above some temperature the bath may be unacceptably prone to spontaneous decomposition. A range of temperatures were tested and 85℃ was found to be a good compromise between plating rate and bath stability.

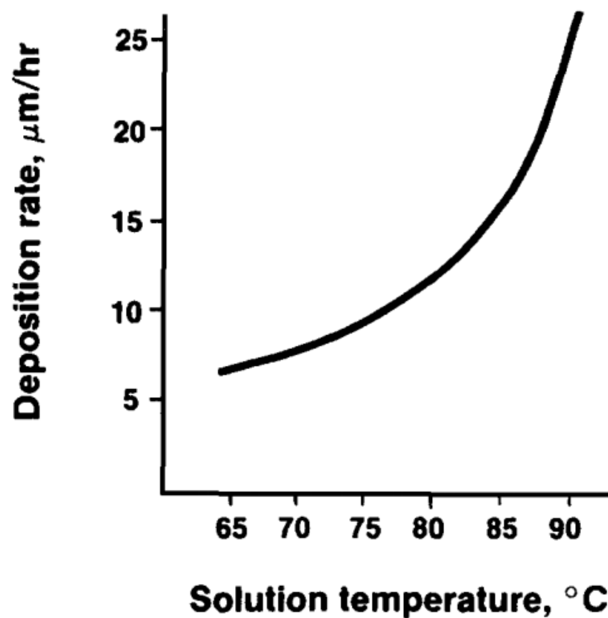


Figure 80: Deposition rate vs solution temperature [53]

9.2.7 Testing

The final ELD solution formulation, operated at 85℃ and pH 4.5, was

Table X: Final ELD solution formula

Component	Quantity
Nickel Acetate Tetrahydrate	47.28 g/L
Sodium Hypophosphite Monohydrate	55.90 g/L
Citric Acid Monohydrate	28 g/L
Ammonium Acetate, Anhydrous	20 g/L
Triton X-100	50 ppm

Slightly more or less than 28 g/L citric acid may be necessary to obtain pH 4.5.

Because no stabilizers were used, difficulties with nodule formation were persistent. The size of the nodules in the final formula were significantly reduced, but are still a prominent feature on the surface of the deposit. However, it is known that the nickel film may "heal" the voids created by the nodules as two-dimensional film growth occurs [82], and therefore the bulk film quality may be much higher than suggested by the surface.

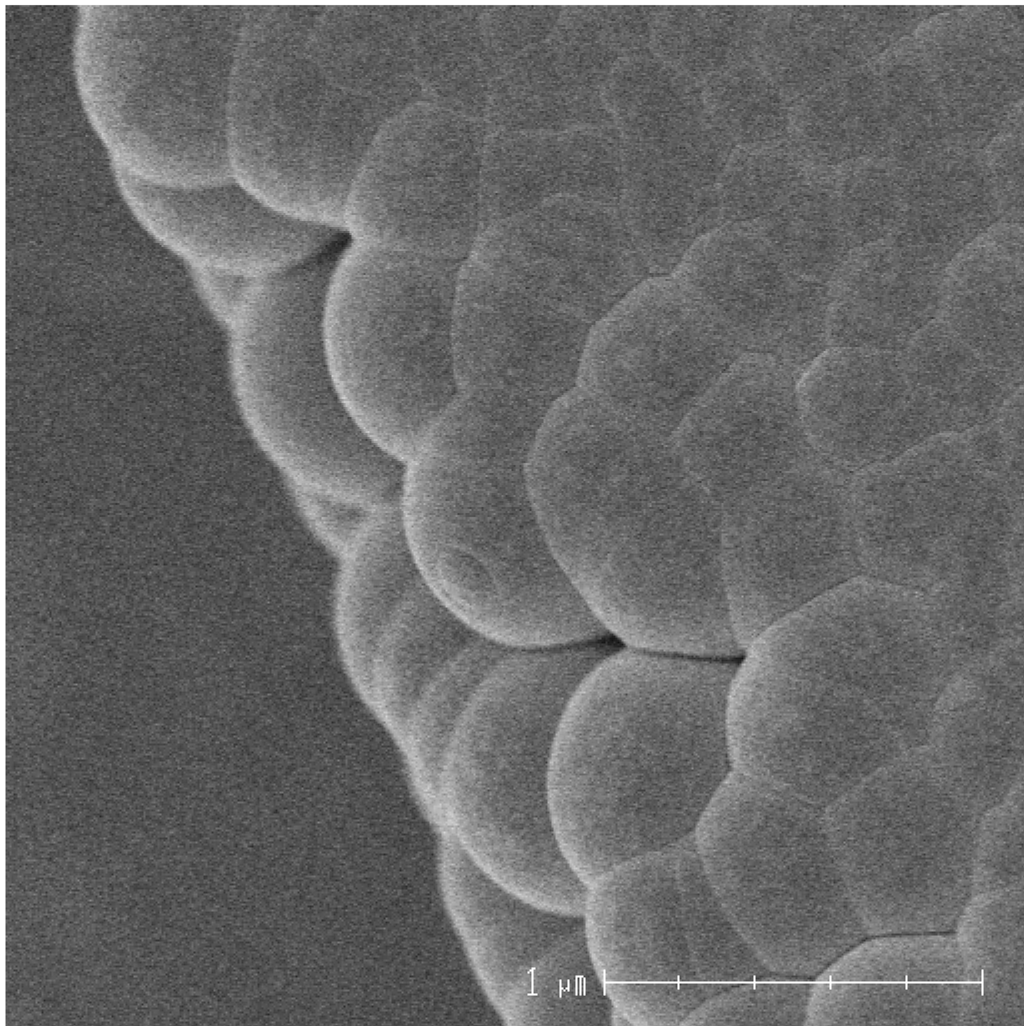


Figure 81: NiP nodules apparently displaying healing mechanism

The deposit thickness of a successful deposit on NiTi film with the final formula was measured by profilometer to be 8 microns thick, with good uniformity. The deposition time was 35 minutes, implying a plating rate of 13.7 microns per hour.

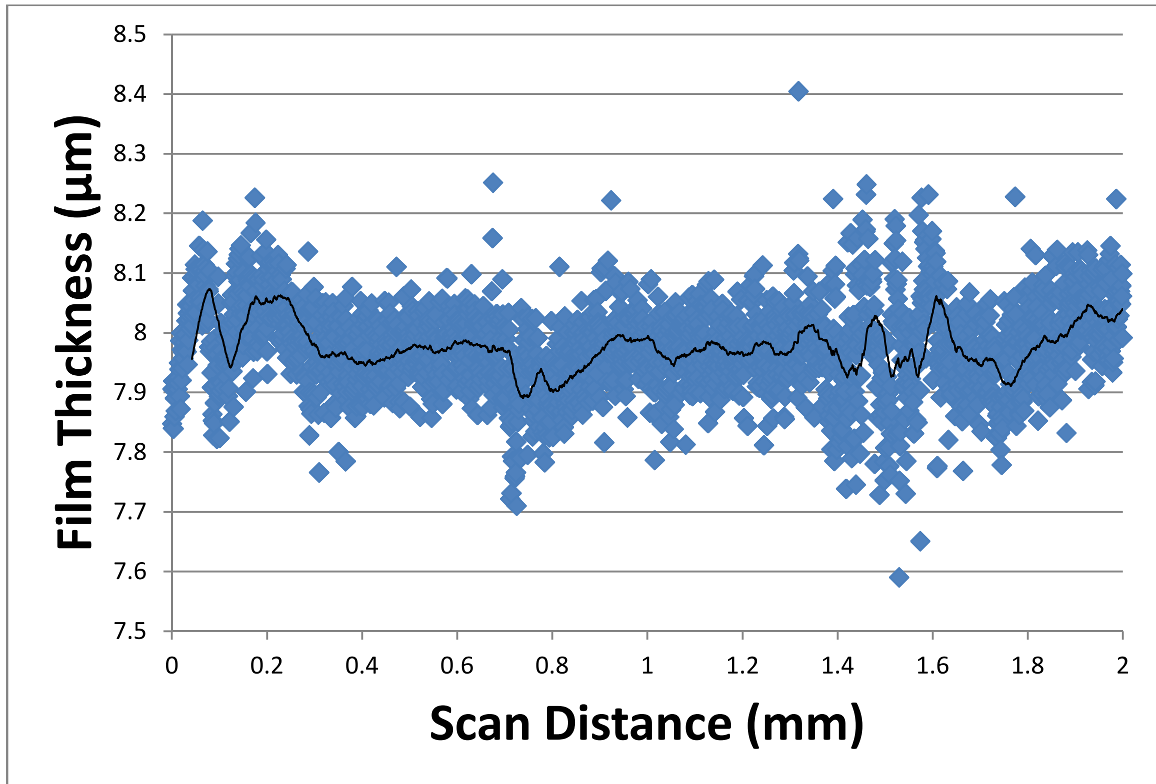


Figure 82: Profilometer scan of deposit thickness with distance

EDX measurements found a slightly higher than desired P concentration in the deposit of about 12.5 wt%. Notably, the nodules on the surface display P concentrations about 1% higher than the bulk. The cause of this is not clear.

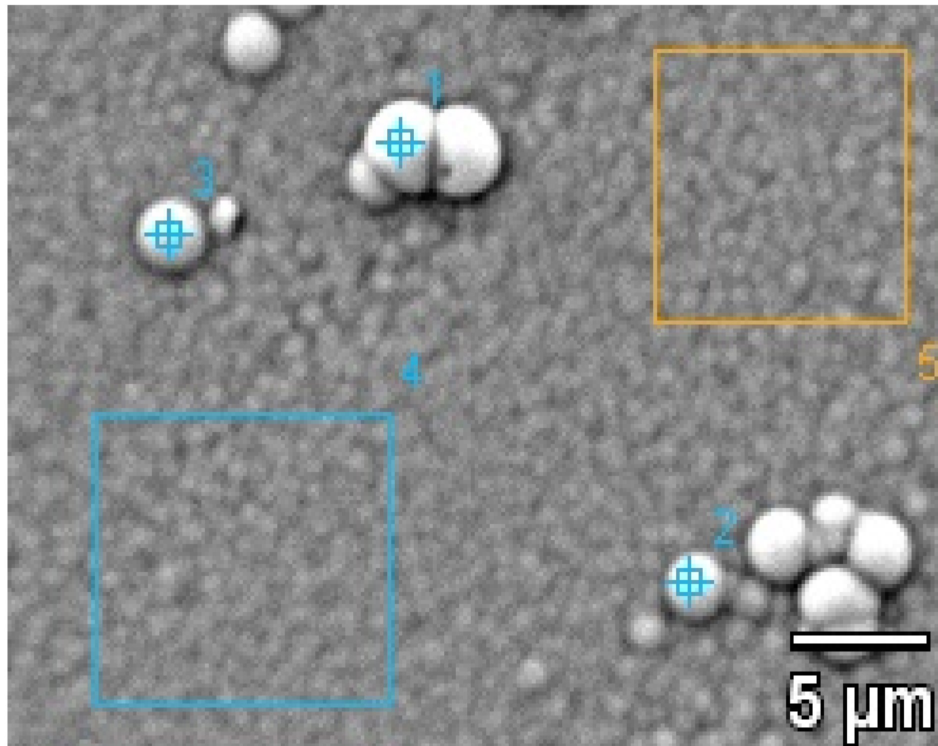


Figure 83: EDX scan locations

Table XI: EDX results for P concentration in NiP film

Location	%wt P
1	13.88 ± 0.09
2	13.58 ± 0.09
3	13.63 ± 0.09
4	12.40 ± 0.09
5	12.55 ± 0.09

Also notable is the apparent nucleation of a new nodule, the black dot near EDX location 1, where phosphorous concentration is greatest.

9.5 Photoresist Constraints

Successful photoresist processing constituted the remaining portion of the deposition process. Most common positive-tone photoresists are not sufficiently

thick for the application, and so alternatives had to be explored. The photoresist also needed good resistance to degradation in the plating bath, and could not interfere with the plating reaction.

9.3.1 Suitable Thickness

The maximum thickness for the deposition step was 20 microns, and therefore a photoresist capable of attaining 20 microns of thickness with a single spin was required.

9.3.2 Suitable Uniformity

The photoresist would require a total within-wafer non-uniformity (WINWU) of no more than a few hundred nanometers when a 5 micron thick coating was spun onto an underlying layer 20 microns thick.

9.6 SU-8

SU-8 is a photoresist widely used in MEMS applications, and was the first photoresist considered. However, it is well-known that SU-8 stripping does not occur through dissolution of the polymer from the substrate, but instead by causing the photoresist layer to swell and detach. Out of concern for the integrity of the devices deposited on top of the SU-8, it was not used [83] [84].

Additionally, it may be difficult to obtain an SU-8 layer only 5 microns thick.

9.7 SPR220

SPR-220 was considered for use as the photoresist mold. However, obtaining a uniform 20 micron film was difficult, because the spin speed was below 750

RPM. Furthermore, the SPR220 was not stable in the hot solution. The sidewalls of the photoresist became much less sharp, and the photoresist lost thickness during the attempted deposition.

Because of the loss of photoresist volume, it was suspected that the SPR220 was leaching into the ELD solution. Unsurprisingly, significant difficulty plating was experienced in the presence of the SPR220. As a result, SPR220 was abandoned.

9.8 ma-P 1275

ma-P 1275 is a thick positive-tone photoresist designed for high stability in plating solutions. A photoresist layer 20 microns thick with good uniformity was obtained by dispensing 5mL of the photoresist onto a wafer spinning at 100 RPM over 30 seconds, then casting the photoresist at 500 RPM for 60 seconds.

A 20 minute prebake at 100℃ was given before an exposure dose of $1800\frac{mJ}{cm^2}$ (corresponding to a light integral of 168 on the Microfabrciation Lab aligner), and the film was developed for 3 minutes in a standard 2.38% TMAH developer.

10. Processing

10.1 Process Integration

Based on the generic process proposed in Section 7.3.2, a comprehensive process flow was developed.

Table XII: Final Process Flow

Step	Process	Parameter
1	Grow thermal oxide	1000 Å
2	Spin-coat 1 micron positive photoresist layer	S1812
3	Lithographically pattern photoresist	Mask 1
4	6:1 BOE etch front side only	2 min
5	Sputter deposit NiV, 7% V	100 nm
6	Spin-coat 1 micron positive photoresist layer	S1812
7	Lithographically pattern photoresist	Mask 2
8	Etch NiV film	Transene NiV Etchant
9	Spin-coat 20 micron positive photoresist layer	ma-P 1275
10	Lithographically pattern photoresist	Mask 3
11	ELD ANiP film	20 microns
12	Sputter deposit NiV, 7% V	100 nm
13	Spin-coat 1 micron positive photoresist layer	S1812
14	Lithographically pattern photoresist	Mask 4
15	Bright-field expose remaining resist	No mask
16	Etch NiV film	Transene NiV Etchant
17	Develop remaining photoresist	
18	Spin-coat 5 micron positive photoresist layer	ma-P 1275
19	Lithographically pattern photoresist	Mask 5
20	ELD ANiP film	5 microns
21	Strip photoresist	

10.2 Oxidation

The oxidation step is similar to that used in the planar process, but a similarly thick oxide is not necessary. To preserve the electrode separation distance, an oxide only 1000 angstroms thick is used. Using the methods described in Section 3.1, but assuming a dry atmosphere, process parameters of 1050℃ and 190 minutes are obtained.

The use of a dry oxidation process will improve the oxide quality and reduce risk of breakdown [17].

10.3 Failure to Deposit

Ultimately the new process was never carried to completion and no devices were obtained because the ELD solution did not plate on NiTi in the presence of patterned ma-P 1275, after several attempts. Several theories about the cause were developed.

It is important to note that the lack of a result is not a result of the belief that the process is unworkable, but due to limitations on time and resources. It is believed that the process, as designed, can be carried to completion with proper control of the ELD solution, photoresist, and seed layer.

10.2.1 Oxidation of Seed Layer

The most obvious explanation for the lack of plating is the oxidation of the NiTi catalytic surface used during the processing attempt.

Although plating was sometimes achieved on fresh PVD NiTi, ostensibly because the native TiO_2 had not yet covered the surface, it is possible that some part of the lithography processing encouraged this oxidation to complete, either the photoresist or the TMAH-based developer.

Alternatively, it is possible that either chemicals in the photoresist or TMAH-based developer removed nickel or nickel oxide from the surface. Chan, et al.

state that in addition to TiO_2, part of the oxide that forms on NiTi during first exposure to atmosphere at room temperature is NiO, which is catalytic [85].

Toward solving this issue in the future, PVD NiV is indicated, but it has not been tested and is not a known good solution

10.2.2 Photoresist Incompatibility

Another credible explanation for the failure to plate is due to polymer and solvent leaching from the photoresist at high temperature. Because the SPR220 was observed to lose volume during the process, it is possible that ma-P 1275 exhibits the same behavior.

In any event, only a small amount of organic solvents and polymer are necessary to poison deposition. Although both soft-bakes and hard-bakes were attempted to remove as much solvent as possible, not all of the solvent can be driven from the photoresist.

Furthermore, it is stated in the patent literature that carbon chains from degraded polymers can be responsible for causing nodules in electroless solutions [86]. Some direct evidence of this was observed.

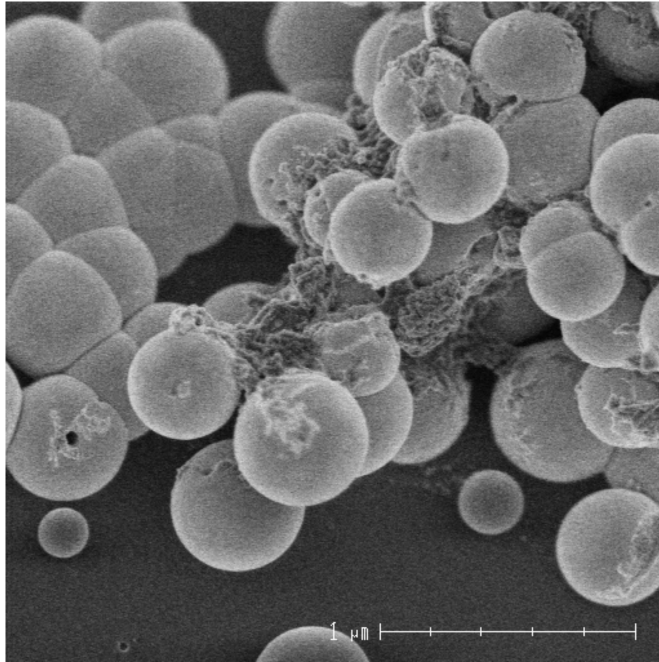


Figure 84: Nodules and organic contaminant observed in poorly-plated film

10.2.3 Dissolved Oxygen

Dissolved oxygen in the ELD solution can inhibit deposition on small patterns due to nonlinear diffusion of the dissolved oxygen to the patterns. Generally the rate of dissolved oxygen reduction is greater than the rate of oxidation of the hypophosphite, and nuclei in small patterns on the surface of a wafer may not attain the potential necessary to initiate deposition [87]. This effect can be mitigated by bubbling nitrogen into the solution, in order to displace the oxygen out of solution.

11. Conclusions and Recommendations

11.1 CVD/CMP/Strip

It must be emphasized that this process for fabricating micromirrors is not a proposal for broad commercial application, as the defect density is likely to be very high. Commercially, processing of similar MEMS hinge structures is generally accomplished via polysilicon and sacrificial layer CVD [84]. Any difficulties with non-uniformity can be solved by CMP in between steps.

However, the process does offer a viable method for wet deposition of MEMS structures. Furthermore, the unusual metallic glass may have niche applications.

11.2 Straight Beam and Serpentine Hinges

Variation between the mechanical behavior of the straight-beam hinge and serpentine hinge designs in the FEA simulation was substantially less than expected. Although the serpentine hinges appear to require approximately one-third the force to actuate, and therefore approximately 57.7% as much voltage as the straight-beam devices, they suffer from a greater “hinge pull” effect.

In a general sense, the serpentine design may be appropriate for large devices where the distance from the electrode to the mirror must be large so that the mirror has sufficient space to rotate. However, the optimal design is to simply shrink the micro-mirror length by an order of magnitude to approximately 10 microns, so that the separation distance between the electrode and the device may also be reduced by an order of magnitude, to about 2 microns. In doing so, the force per unit area of the electrode will be increased by a factor of 100 at any

given voltage – or, alternatively, the voltage required for a given force will be reduced by a factor of 10.

Correspondingly, the device hinges will shrink substantially. Vertical displacement of the hinges – the “hinge pull” – will decrease as the cube of the hinge length. In such a situation, it is optimal to use straight beam hinges.

11.3 Amorphous Nickel Phosphorous

The suitability of the use of amorphous nickel-phosphorous alloy for micromirror devices is unclear without successful fabrication and mechanical testing.

However, amorphous nickel-phosphorous is a metallic glass, and therefore typical characteristics of metallic glasses are likely to apply. Of these characteristics, the viscoelastic response, large elastic region, and fatigue/failure mechanism are perhaps the most important.

11.3.1 Viscoelasticity

An anelastic component of viscoelastic flow is associated with bulk metal glasses [88]. However, there is an Arrhenius dependence of strain rate on temperature; unfortunately, because no material in the literature could be found to characterize the activation energy for amorphous NiP, it is uncertain the impact it would have on its mechanical behavior under sustained load at room temperature. Although anelastic flow in other metallic glasses such as Pd82Si18 is relatively small at room temperature, and operates on a time scale of several hours

In the case that the elastic character of amorphous NiP dominates, as is the case with many metallic glasses, ANiP may prove to be a suitable material for use in MEMS.

11.3.2 Elastic Region

Because of the glassy character of the alloy, amorphous NiP may be repeatedly loaded nearly to the ultimate strength of the material without causing plastic deformation due to dislocation motion.

Since the stresses involved in the precise motion of an actuator device are consistent and predictable, the ability to load the material nearly to failure may be an asset.

Compared to the default MEMS material, polysilicon, NiP has a somewhat lower elastic modulus of 114 GPa vs 169 GPa for polysilicon, which may ultimately be beneficial to reduce the actuation force necessary in devices. Its tensile strength, approximately 750 MPa, is lower than that of polysilicon at 1.20 GPA, but for applications where no more than 750 MPa of material strength is needed, NiP may be superior [89]. Pure aluminum, the material used for the mirror device in the TI DMD devices, has a lower elastic modulus of about 69 GPa, but also a much lower yield strength, approximately 7-11 MPa, and a tensile strength of about 90 MPa. Although hinges of the same size will be more pliable if made from aluminum, they can be made smaller from NiP because of the higher stress tolerance before failure.

11.3.3 Fatigue

Normal crystalline metal DMDs do not exhibit fatigue because the formation and propagation of cracks is dependent on the build-up of dislocations at grain boundaries; but because the devices are so small, they are often only one grain thick, and a sufficiently high mechanical stress cannot develop [90].

This benefit may potentially be lost in metallic glasses, since there is little impediment to crack propagation in the amorphous matrix, and cyclic fatigue can become a serious problem [91] [92] Still, there is no potential for dislocation pile-up, and so the crack defects must already exist or must be created through some other mechanism. For very small devices, it is possible that the probability of such large defects may be suitably low, so that the yield would remain acceptable, and faulty mirror arrays would simply be discarded after burn-in testing.

Using the modified Griffith's criterion to obtain the critical crack length in an axially loaded plane,

$$\sigma_f = \sqrt{\frac{E G_c}{\pi a}} \qquad \text{(Equation 62)}$$

Where E is the elastic modulus, G_C is the critical strain energy release rate, a is the critical crack size, π is the constant, and σ_f is the critical plane stress, and

using the expression for critical strain energy release rate in terms of the stress intensity known to be $K_{IC} = 7.1\ MPa \cdot m^{\frac{1}{2}}$ for NiP [93],

$$G_C = \frac{K_{IC}^2(1+\nu^2)}{E} = \frac{\left(7.1\ MPa \cdot m^{\frac{1}{2}}\right)^2 * (1 + 0.3539^2)}{114\ GPa} = 497.6\ Pa \cdot m \qquad \text{(Equation 63)}$$

Then, calculating the critical strain energy release rate to find the critical plane stress assuming a crack as long as the device thickness of 5 microns,

$$\sigma_f = \sqrt{\frac{114 * 10^9 Pa * 497.6\ Pa * m}{\pi * 5\ \mu m}} = 1.90\ GPa \qquad \text{(Equation 64)}$$

Because the critical stress is substantially larger than the tensile strength of NiP, it appears a reasonable conclusion that there is no crack size able to propagate without having already caused the device to fail, and therefore brittle fracture is not a failure mechanism for NiP in MEMS applications.

Unfortunately plane strain is a poor approximation here because of the torsion of the hinge, but it does provide an order-of-magnitude estimate and serves to illustrate that brittle cracking is not a likely failure mechanism.

11.4 Future Work

11.4.1 Optimize Design

Using the equations developed in Section 8, it is possible to conduct an iterative search for the optimal device design parameters over the full design space, using appropriate constraints for each design variable.

Additionally, it would be worthwhile to consider beams with square cross-sectional hinges (in order to minimize the hinge sag effect) which connect to the long axis of a square micromirror. Because a square mirror that rotates along the diagonal strikes the substrate at only one point, it would be possible to facilitate tilt at a lower voltage by using up less electrode area for the snapdown pad.

Finally, the use of a multiphysics simulation package, such as COMSOL, would provide a much more accurate picture of the behavior of the mirror device when a dynamic electrostatic force is applied. It would also be useful for verifying and optimization work done using the analytical equations.

11.4.2 Complete Process Development

Overcoming the process difficulties encountered will enable fabrication of the devices, and the mechanical characterization of the device behavior that was part of the original project objectives.

There are a few options to address the difficulties besides those already mentioned. One is the use of a supercritical CO_2 emulsion for ELD, which has been shown to substantially suppress growth of nodules [94]. However, the expense and extra effort may be difficult to justify.

Further development of the ELD chemistry will be challenging, because sodium hypophosphite is a DEA Schedule 1 substance, creating significant legal hurdles to its acquisition. As a result, it may be valuable to test the effectiveness and film quality of several commercial ELD solutions. Three commercial high-P solutions are:

1) Uyemura International Corporation ANP1012
2) Enthone Inc. ENfinity 12 series
3) OM Group, Inc. 5023 Nickel Process

Additionally, AZ 4620 has been mentioned as the photoresist used during a similar thick electroless NiP deposition process on a silicon substrate [95]. Testing of AZ 4620 for suitability in this process may be fruitful.

Finally, the installation of a nitrogen bubbler would be invaluable to displace dissolved oxygen from the electroless bath.

11.4.3 Magnetically Actuated Cobalt or NiFe Devices

It is well known that Co and NiFe deposits are also obtainable through electroless deposition. Unlike high phosphorous NiP, these deposits are strongly ferromagnetic. This ferromagnetism allows for their implementation of magnetic actuation. An electromagnetically actuated mirror device could either be actuated in two axes, with an electrostatic parallel-plate actuator driving one axis and a magnetic coil driving the other, or the magnetic coil could serve as a repulsive force to create stability over the angles where the micromirror would otherwise snap down onto the surface. If the control of the actuation could be properly

tuned by external circuitry, it might be possible to rapidly rotate of the mirror to a wide variety of stable angles, making a kind of "analog mirror device".

11.4.4 NiP Strain Rate Dependence on Temperature

As discussed in 11.3.3, it is expected that the NiP alloy will have a strain rate with an Arrhenius-type temperature dependence. The author was unable to find any discussion of this effect for nickel-phosphorous alloys in the literature. Therefore, heating the mirror devices to a variety of temperatures and observing the strain rate dependence on temperature via their positional instability would constitute the first publication on that topic for a NiP alloy.

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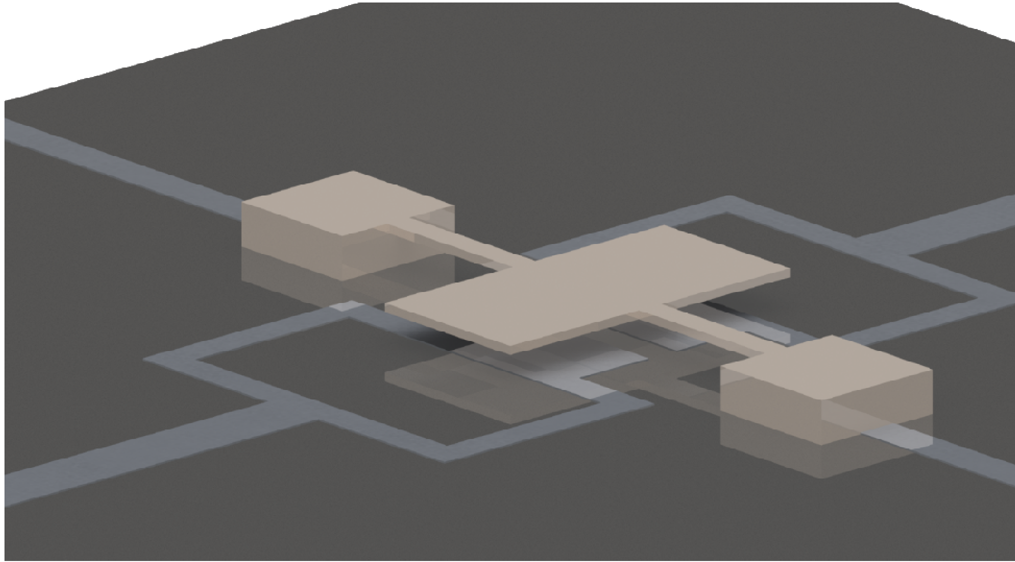
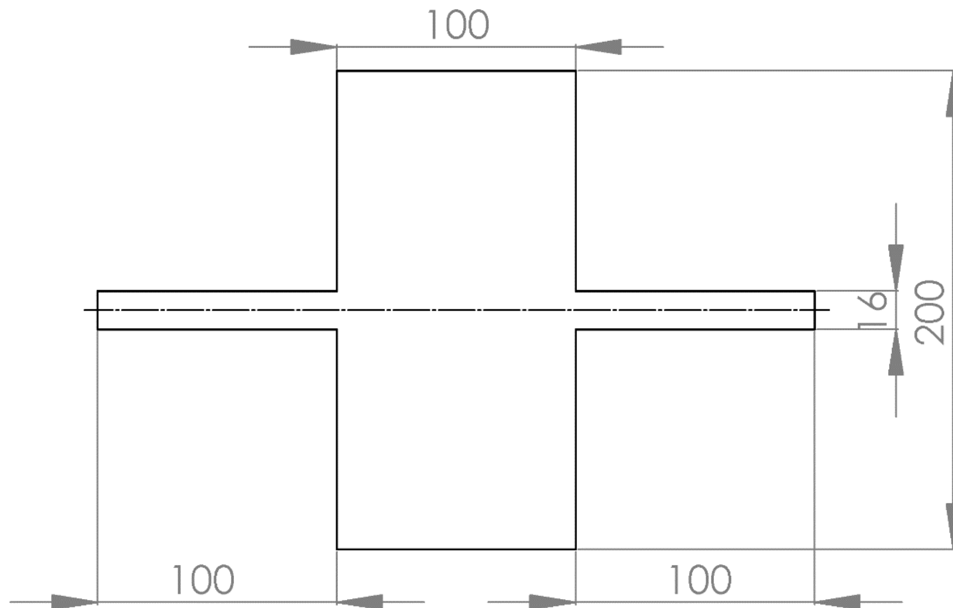
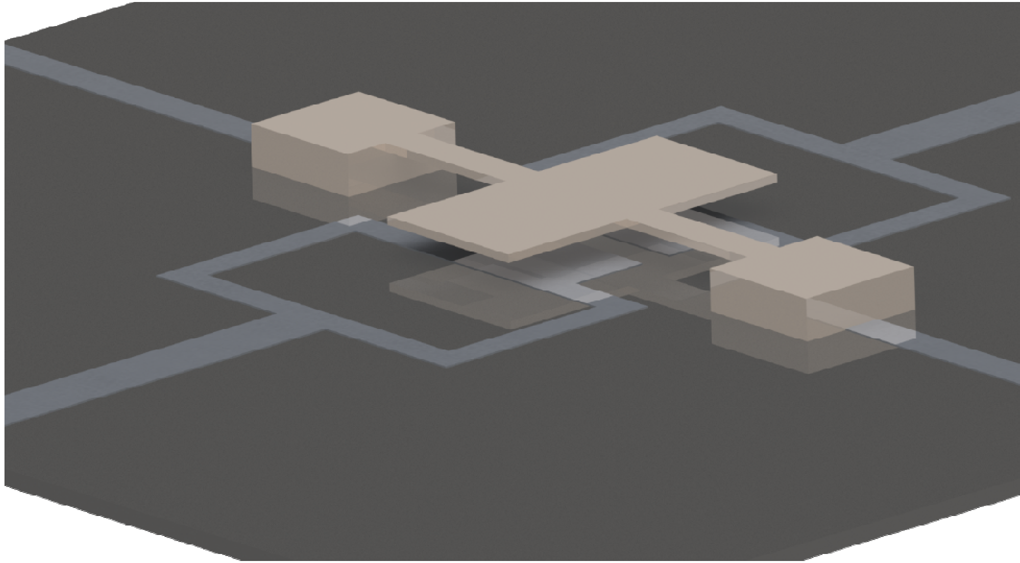
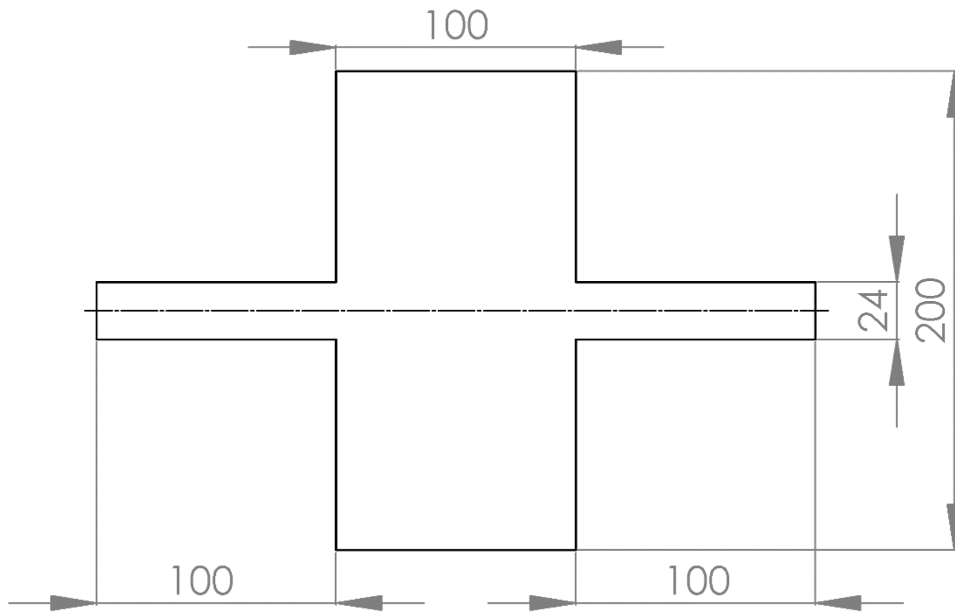
Appendix A: Final Device Designs



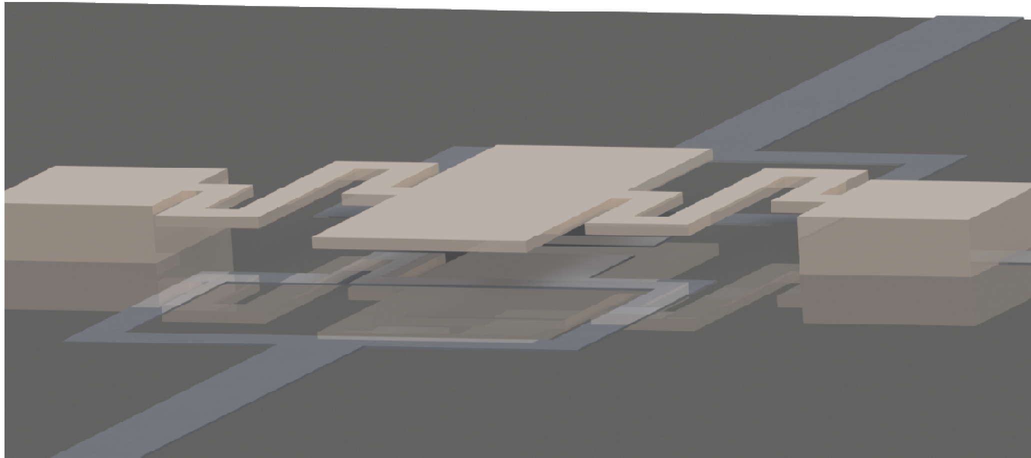


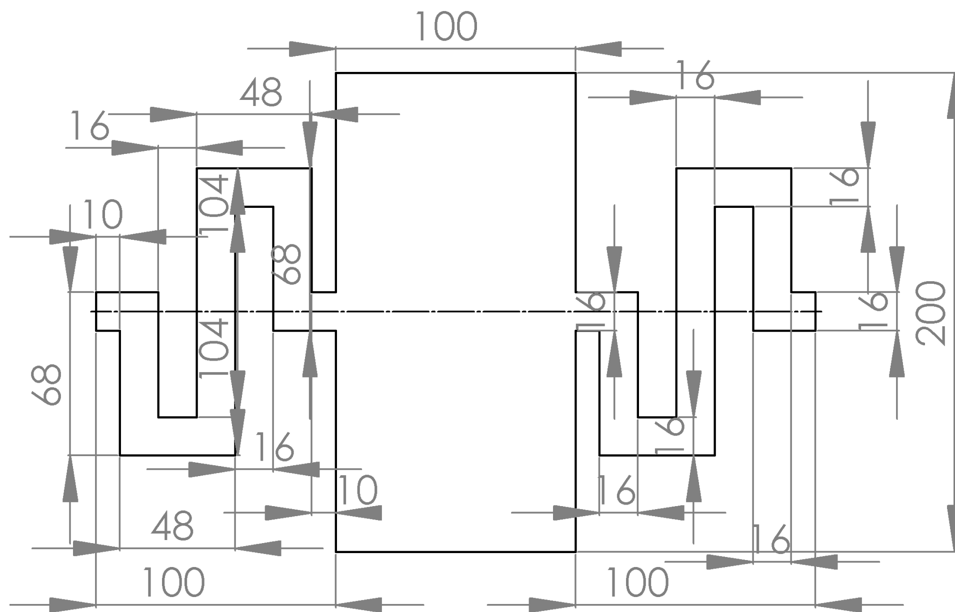
Straight-beam design, a = 16 microns



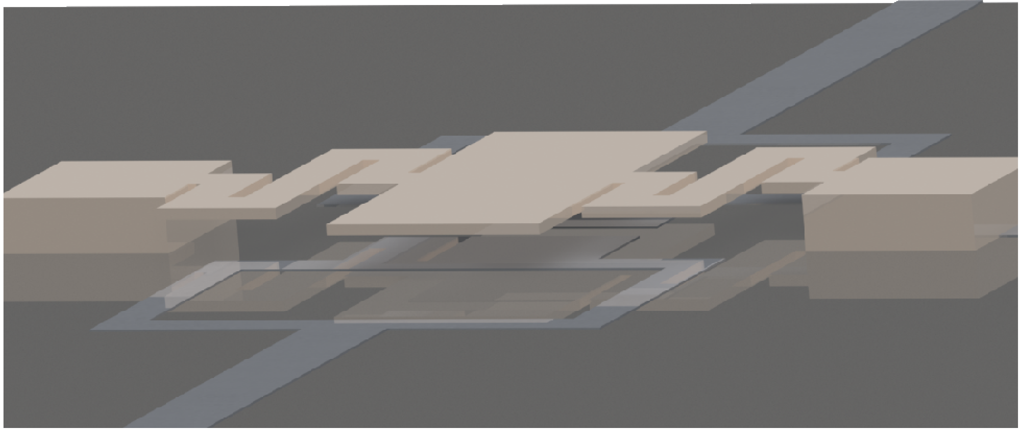


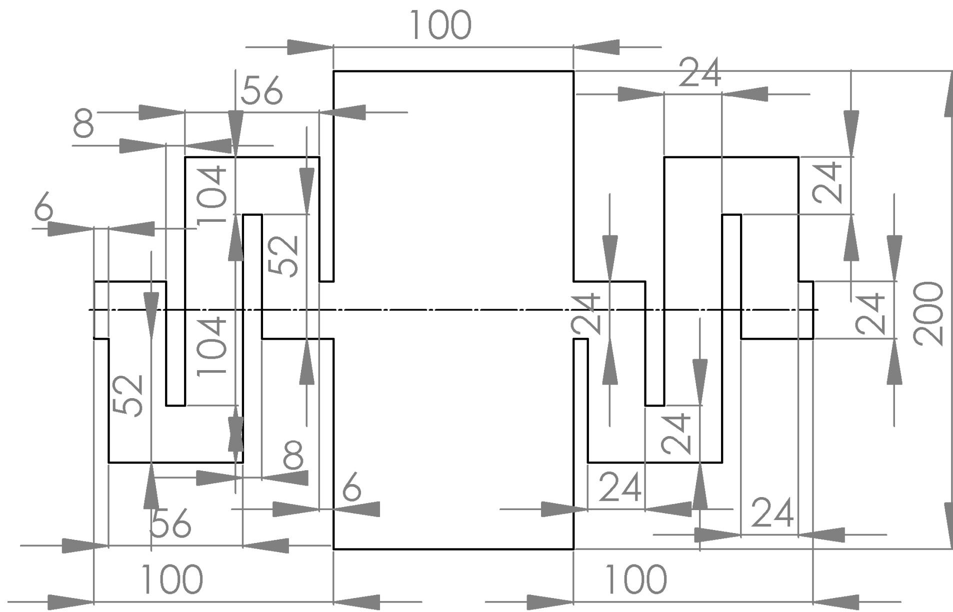
Straight-beam design, a = 24 microns





Serpentine hinge design, a = 16 microns





Serpentine hinge design, a = 24 microns

ALL UNITS MICRONS

Snapdown pad

Centerline intersects midpoint of edge

Centerline on device drawing is collinear

Support Pillar

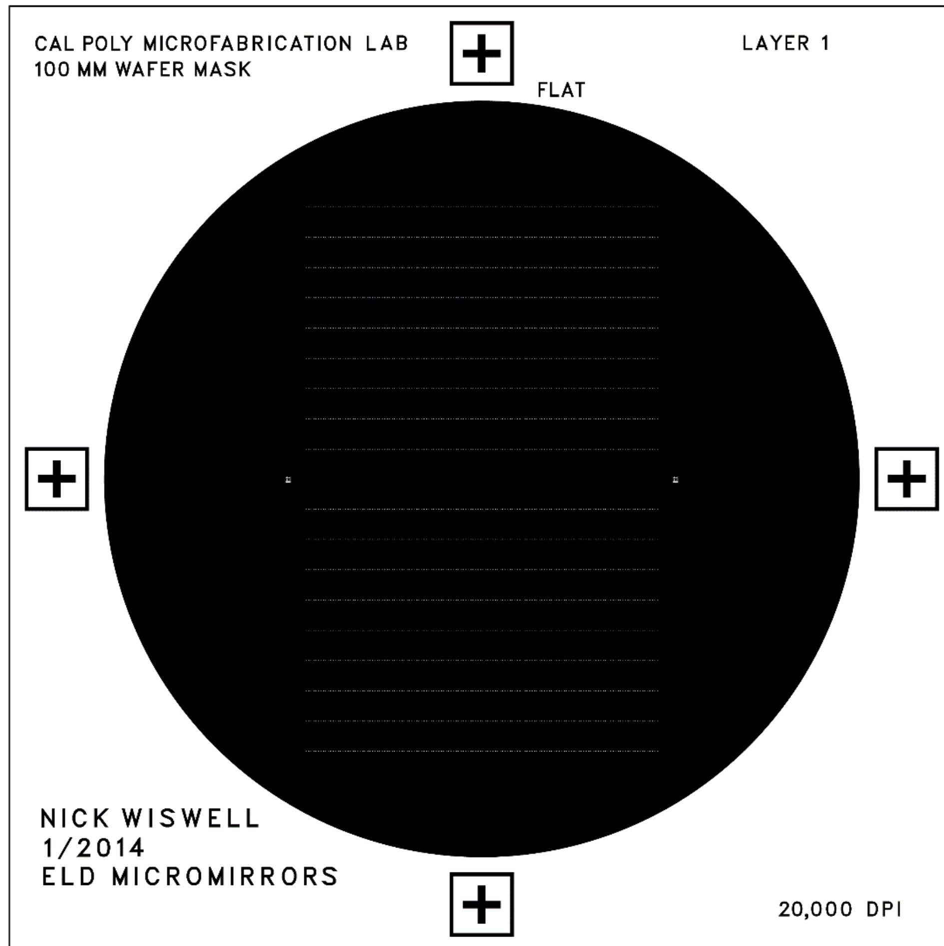
Electrode

Electrical traces

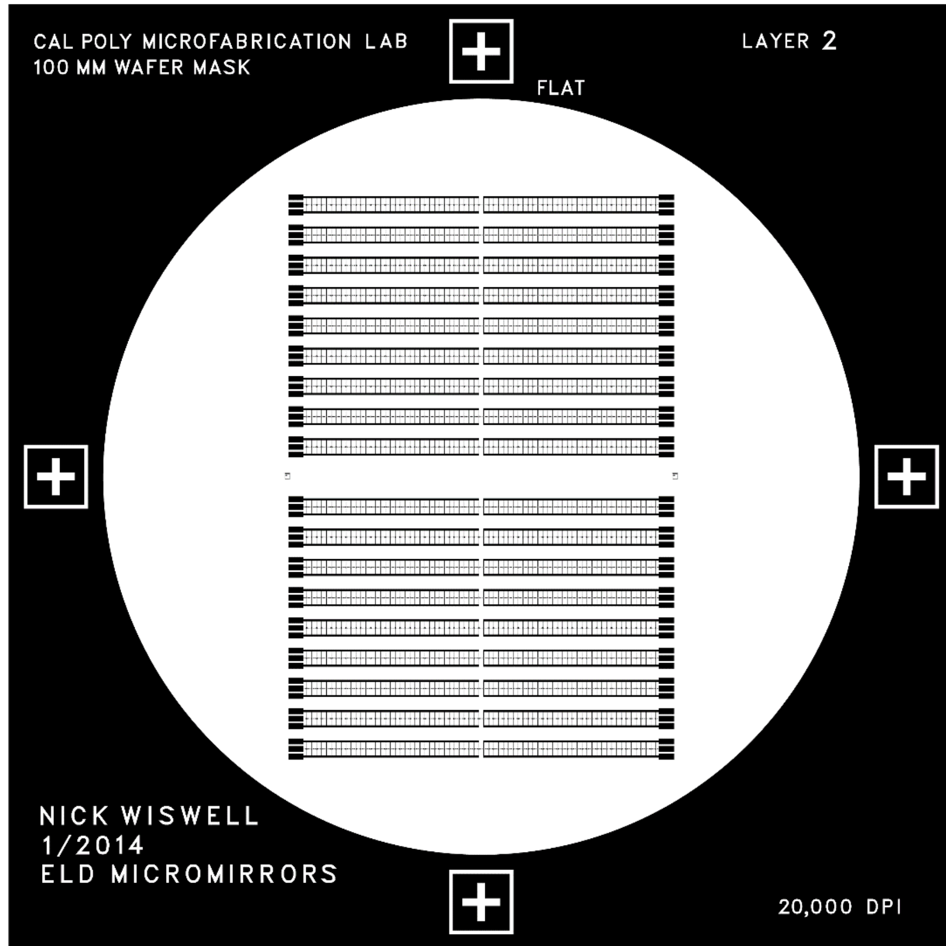
40 300 20 20 20 20 24 80 80 80 80 24 20 20 20 70 120 110 200 40

Common design of traces and electrodes below device layer

Appendix B: Processing Masks



Mask layer 1



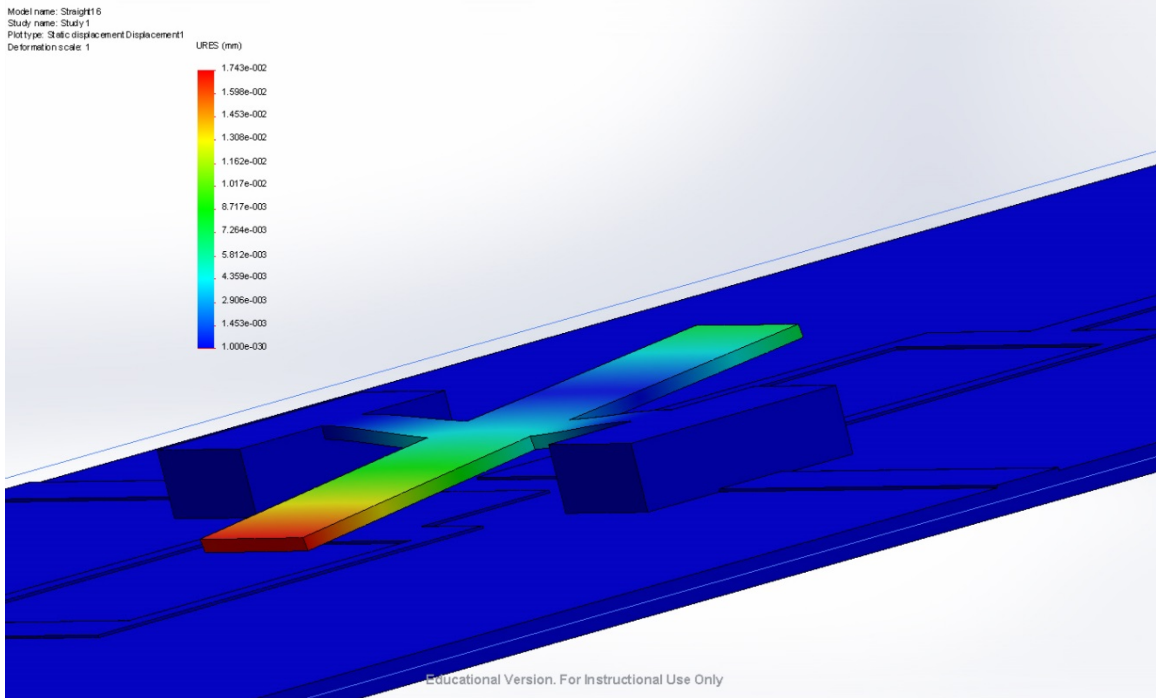
Mask layer 2

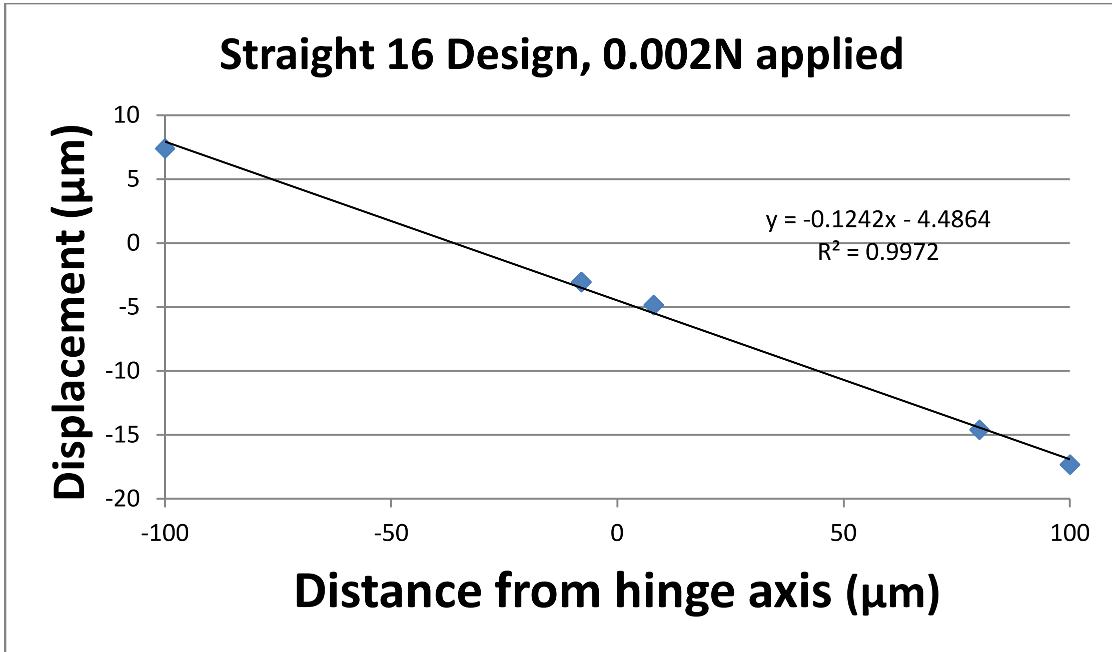
Mask layer 3

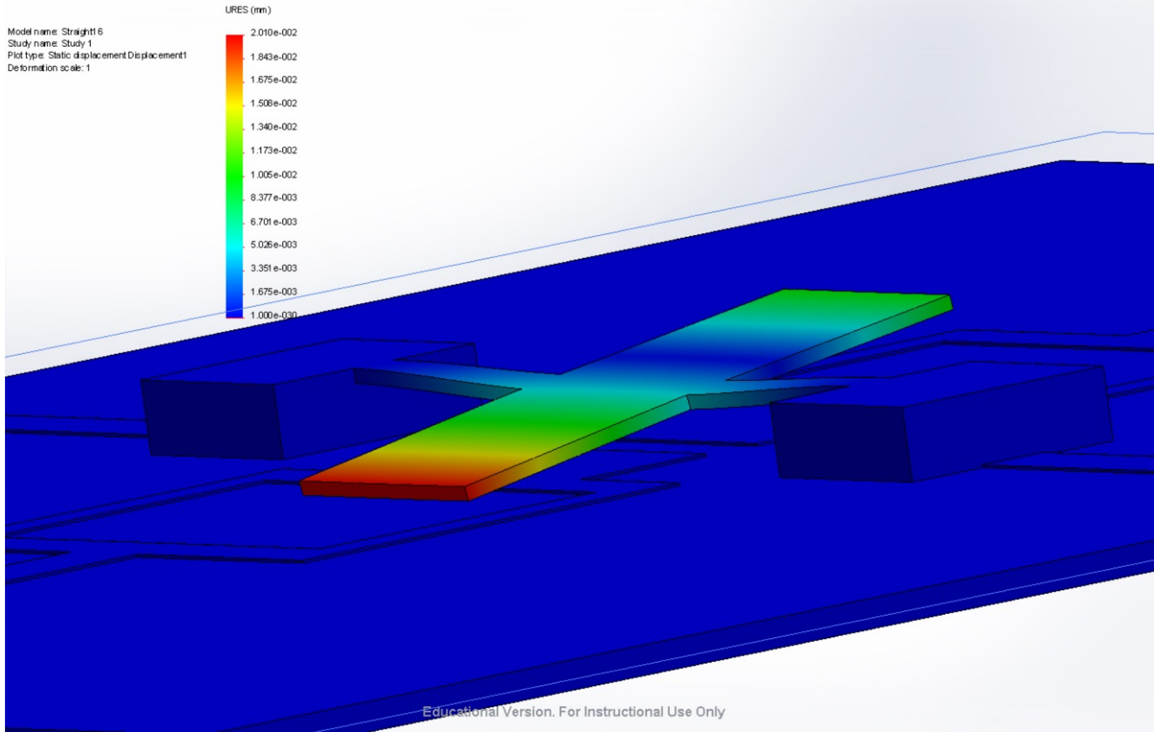
Mask layer 4

Mask layer 5

Appendix C: SolidWorks FEA







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Deformation scale: 1
URES (mm)
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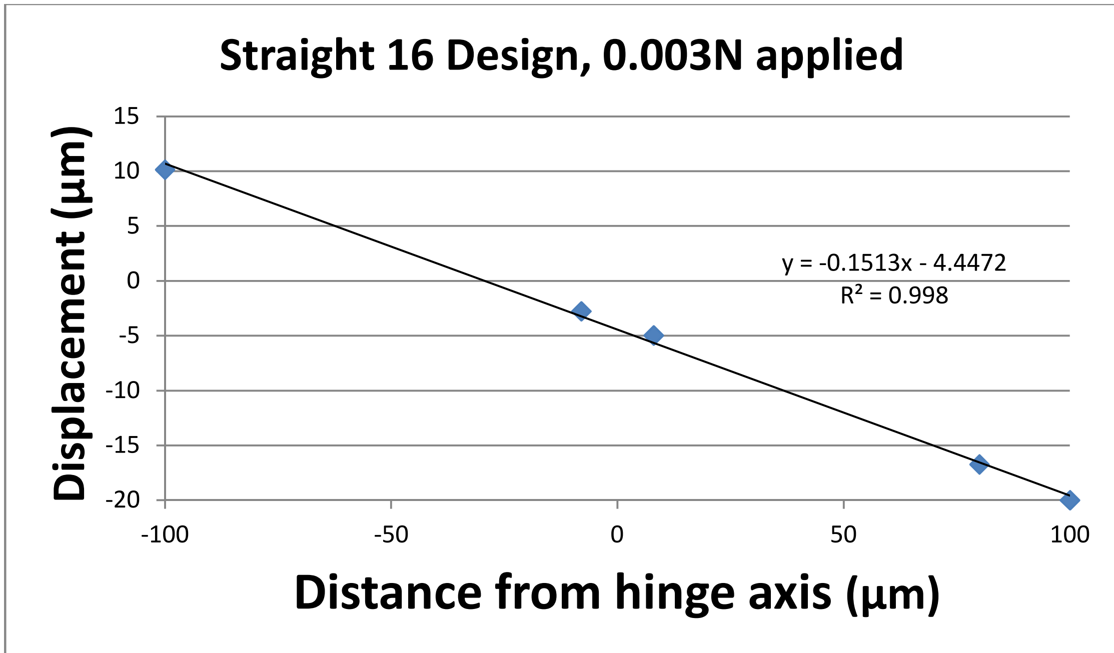
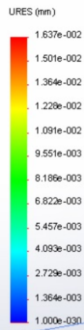
1.843e-002
1.675e-002
1.508e-002
1.340e-002
1.173e-002
1.005e-002
8.377e-003
6.701e-003
5.026e-003
3.351e-003
1.675e-003
1.000e-030
Educational Version. For Instructional Use Only



Straight 16 Design, 0.003N applied
Displacement (µm)
15
10
5
0
-5
-10
-15
-20
y = -0.1513x - 4.4472
R² = 0.998
-100
-50
0
50
100
Distance from hinge axis (µm)



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Study name: Study 1
Plot type: Static displacement Displacement1
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URES (mm)
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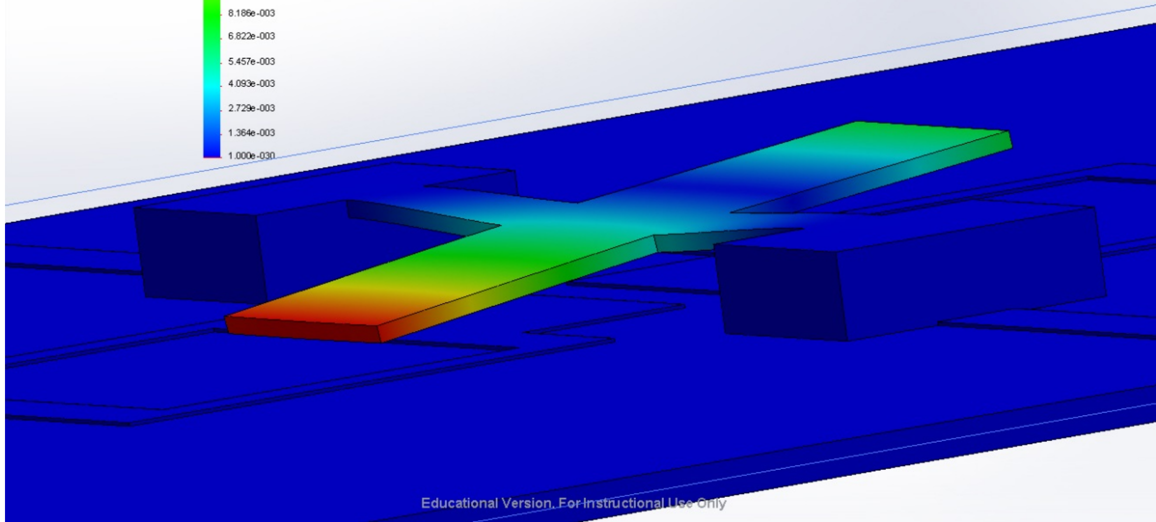
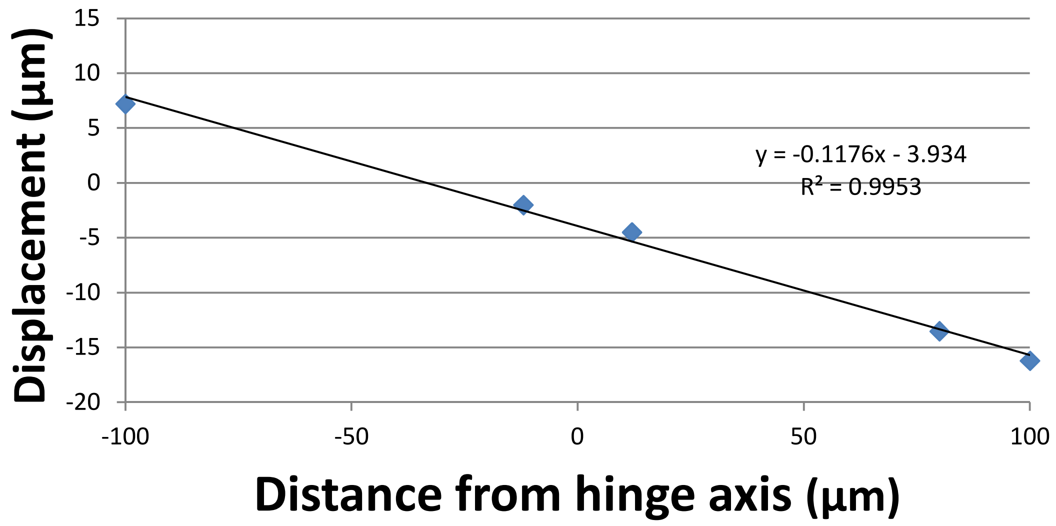
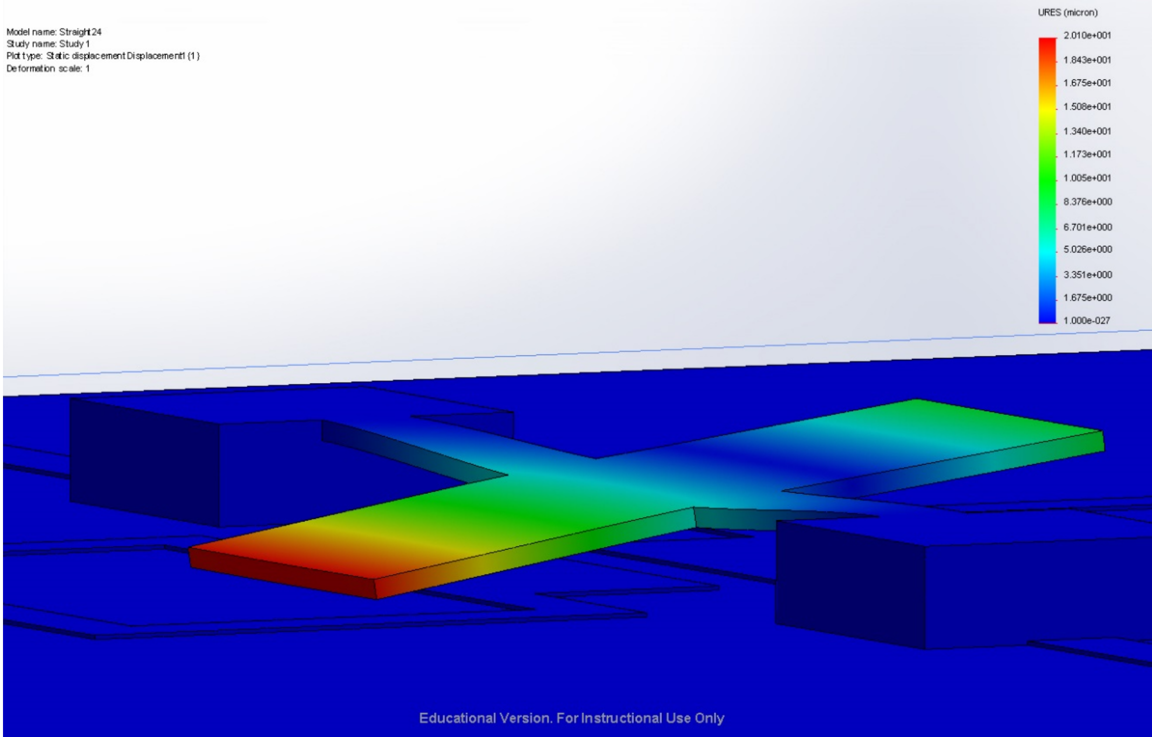
1.501e-002
1.364e-002
1.228e-002
1.091e-002
9.551e-003
8.186e-003
6.822e-003
5.457e-003
4.093e-003
2.729e-003
1.364e-003
1.000e-030



Educational Version. For Instructional Use Only



Straight 24 Design, 0.003N applied
Displacement (μm)
15
10
5
0
-5
-10
-15
-20
-100
-50
0
50
100
y = -0.1176x - 3.934
R² = 0.9953
Distance from hinge axis (μm)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Study name: Study 1
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URES (micron)
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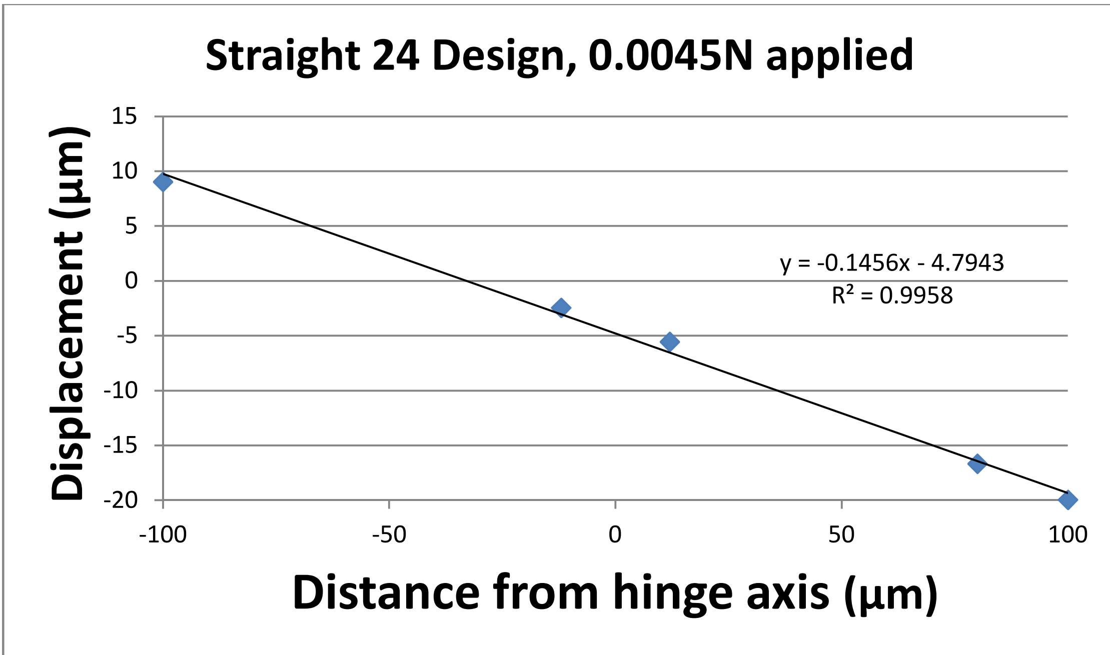
1.843e+001
1.675e+001
1.508e+001
1.340e+001
1.173e+001
1.005e+001
8.376e+000
6.701e+000
5.026e+000
3.351e+000
1.675e+000
1.000e-027
Educational Version. For Instructional Use Only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Displacement (µm)
15
10
5
0
-5
-10
-15
-20
-100
-50
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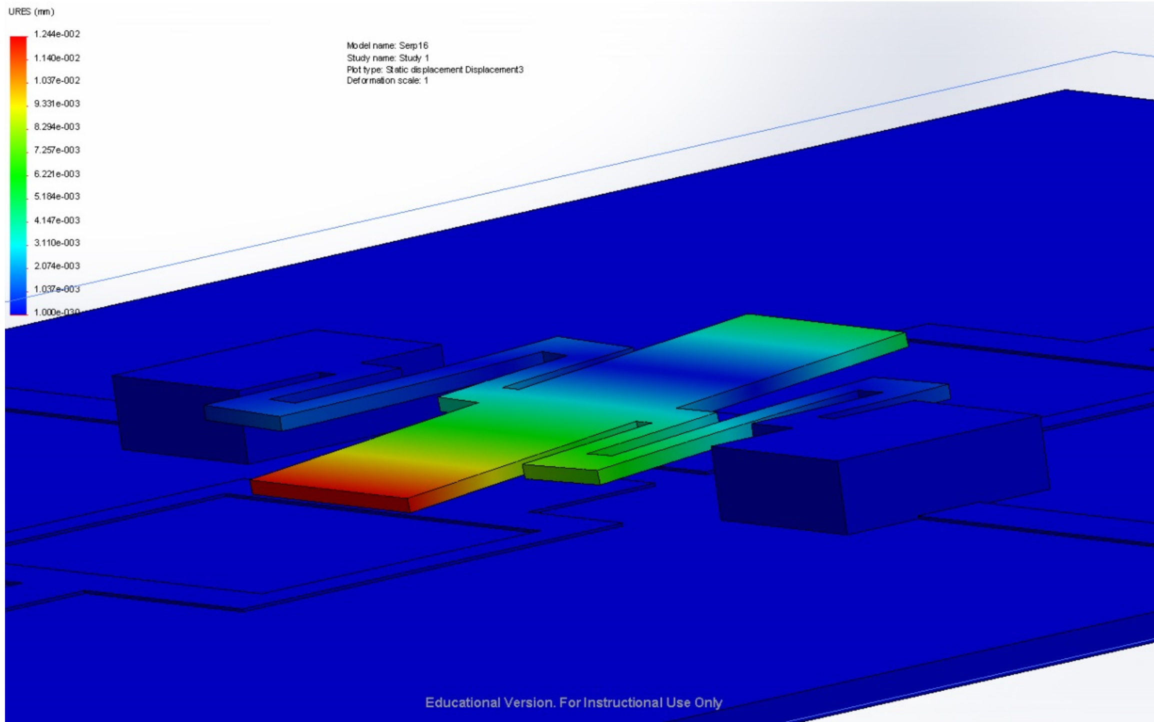
50
100
y = -0.1456x - 4.7943
R² = 0.9958
Distance from hinge axis (µm)


URES (mm)
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1.140e-002
1.037e-002
9.331e-003
8.294e-003
7.257e-003
6.221e-003
5.184e-003
4.147e-003
3.110e-003
2.074e-003
1.037e-003
1.000e-030
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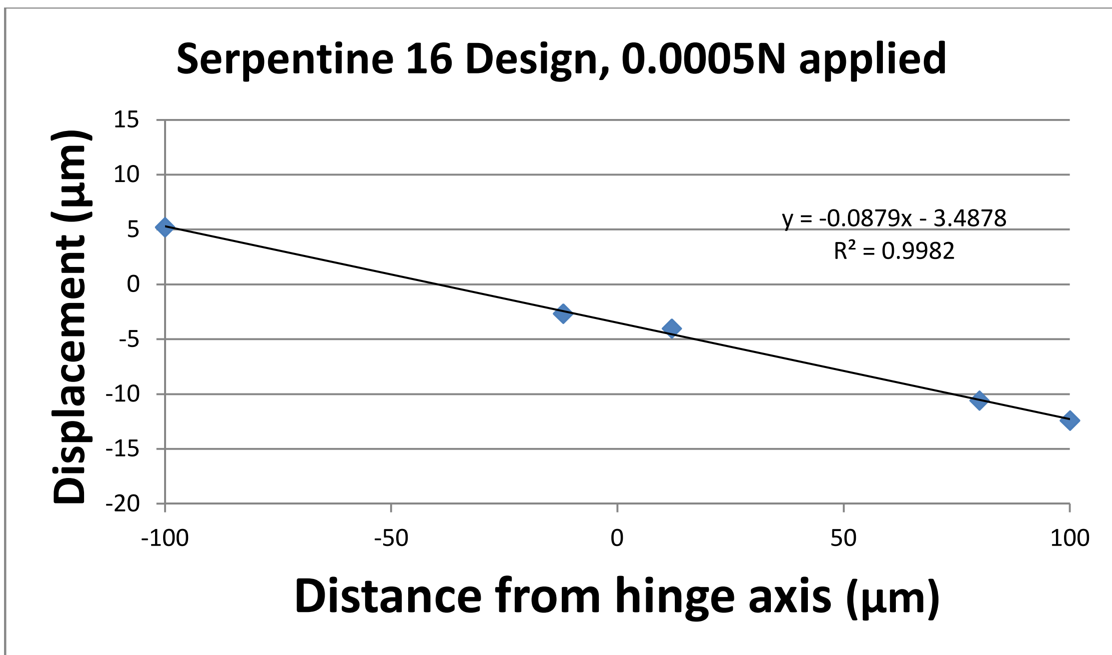
Study name: Study 1
Plot type: Static displacement Displacement3
Deformation scale: 1
Educational Version. For Instructional Use Only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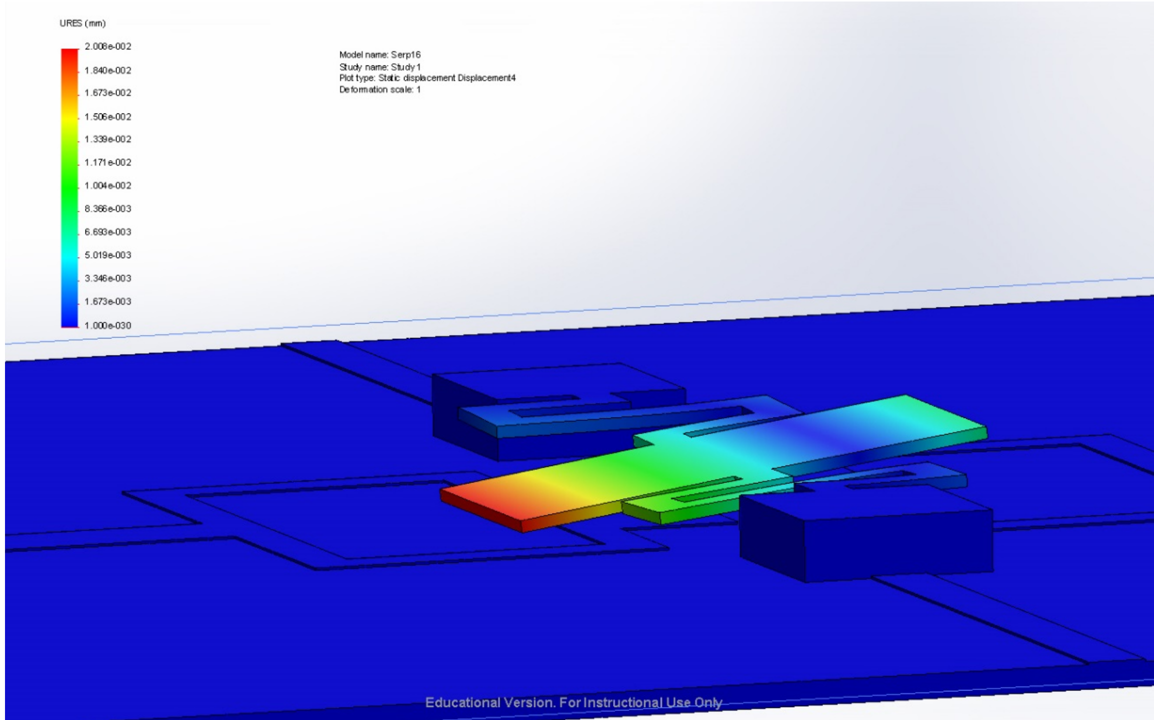
Displacement (μm)
15
10
5
0
-5
-10
-15
-20
-100
-50
0
50
100
Distance from hinge axis (μm)
y = -0.0879x - 3.4878
R² = 0.9982


URES (mm)
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3.346e-003
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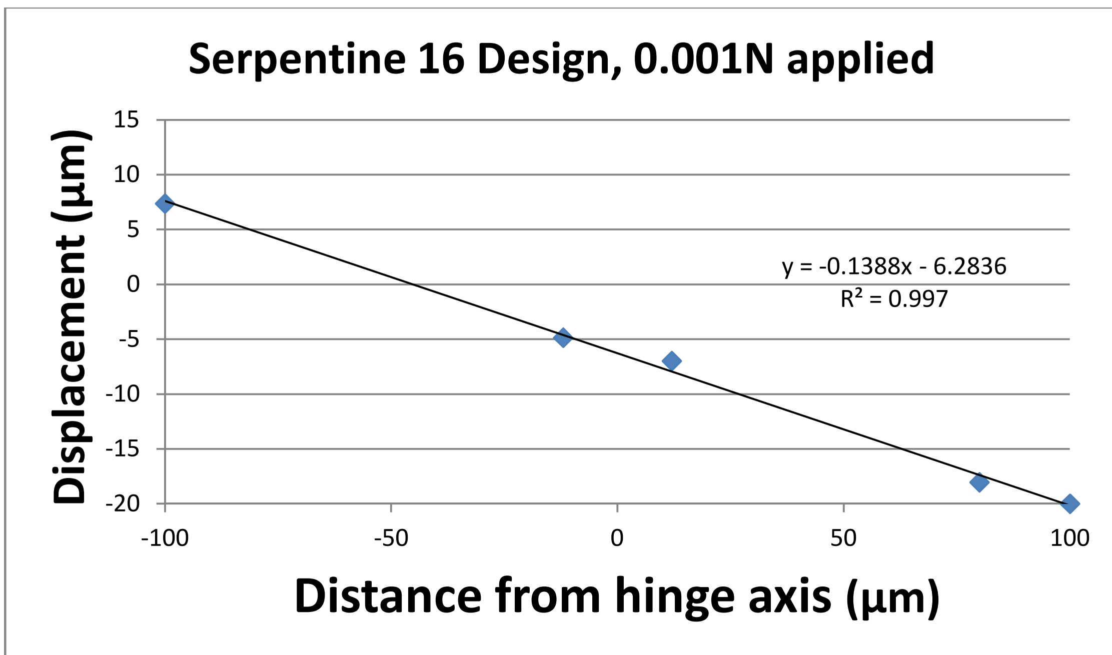
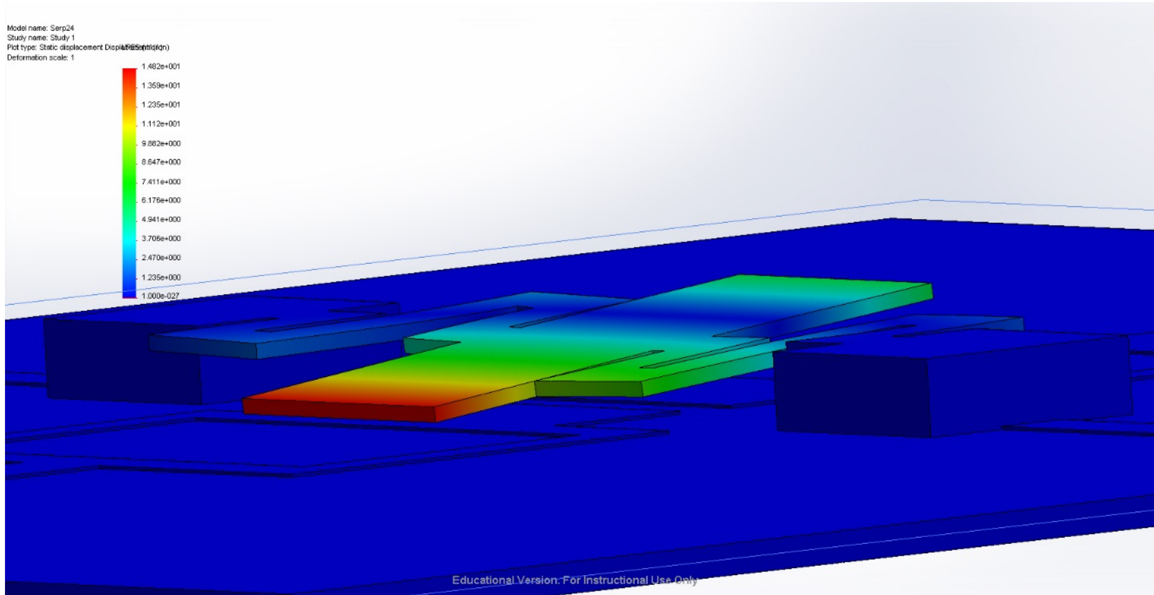
Educational Version. For Instructional Use Only


Serpentine 16 Design, 0.001N applied
Displacement (µm)
15
10
5
0
-5
-10
-15
-20
-100
-50
0
50
100
Distance from hinge axis (µm)
y = -0.1388x - 6.2836
R² = 0.997



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8.647e+000
7.411e+000
6.176e+000
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1.235e+000
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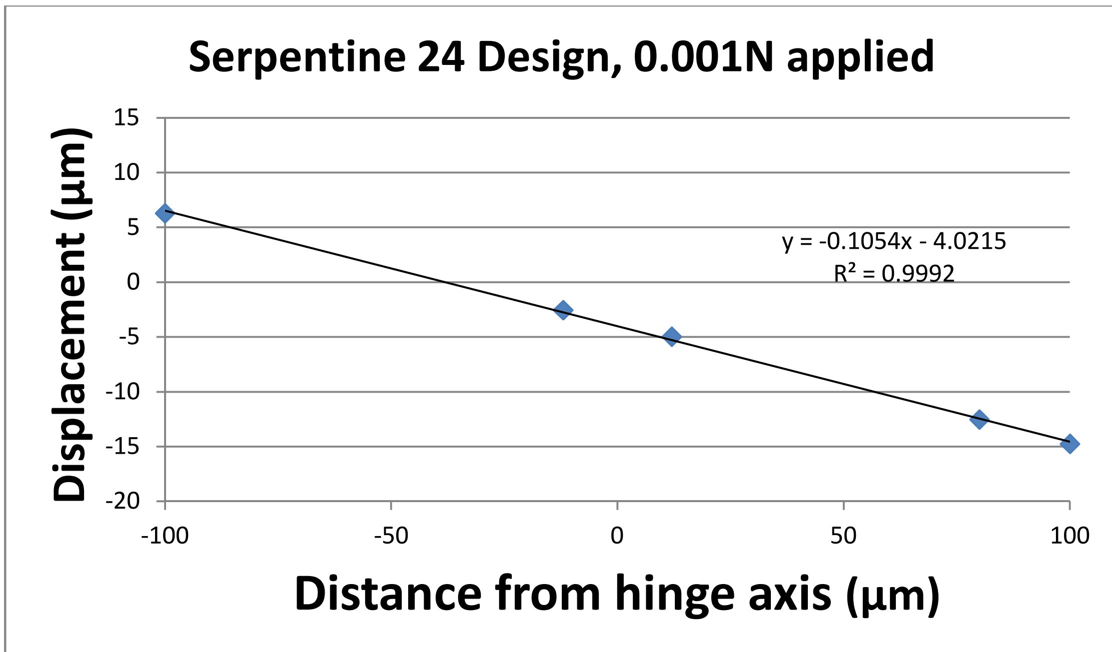
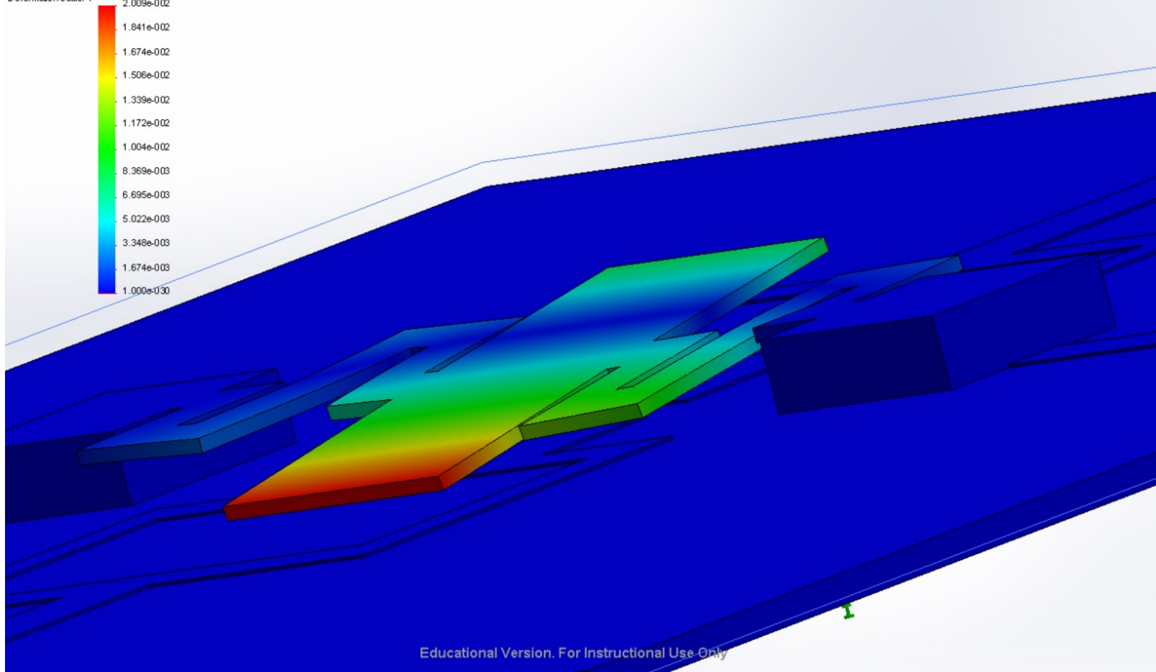


Serpentine 24 Design, 0.001N applied
Displacement (µm)
15
10
5
0
-5
-10
-15
-20
y = -0.1054x - 4.0215
R² = 0.9992
-100
-50
0
50
100
Distance from hinge axis (µm)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Study name: Study 1
Plot type: Static displacement Displacement2
Deformation scale: 1
URES (mm)
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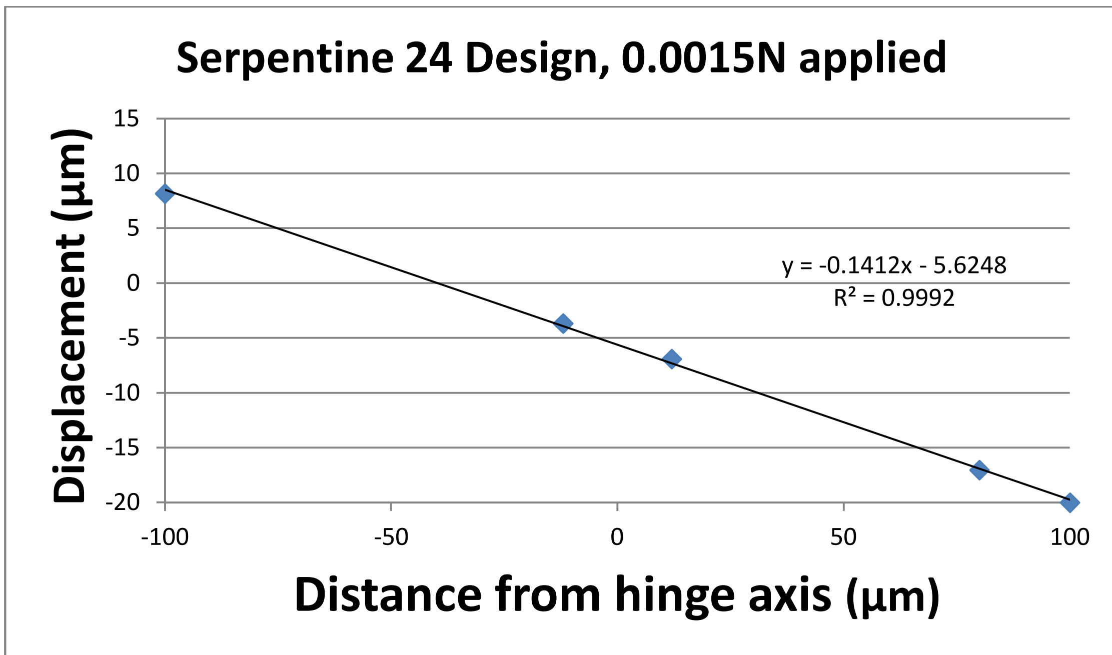
1.841e-002
1.674e-002
1.506e-002
1.339e-002
1.172e-002
1.004e-002
8.369e-003
6.695e-003
5.022e-003
3.348e-003
1.674e-003
1.000e-030
Educational Version. For Instructional Use Only


Serpentine 24 Design, 0.0015N applied
Displacement (µm)
15
10
5
0
-5
-10
-15
-20
-100
-50
0
50
100
Distance from hinge axis (µm)
y = -0.1412x - 5.6248
R² = 0.9992