

DIGITALLY-CONTROLLED TWO-PHASE ZERO-VOLTAGE-SWITCHING QUASI-
RESONANT BUCK CONVERTER

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ABSTRACT

Digitally-Controlled Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter

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This thesis entails the design, construction, and performance analysis of a digitally-controlled two-phase Zero-Voltage Switching Quasi-Resonant (ZVS-QR) buck converter. The converter is aimed to address the issues associated with powering CPUs operating at lower voltage and high current. To evaluate its performance, the Two-Phase ZVS-QR buck converter is compared against a traditional Two-Phase buck converter. The design procedure required to implement both converters through utilizing the characterization curve and formulas derived from their circuit configurations will be presented. Computer simulation of the Two-Phase ZVS-QR buck converter is provided to exhibit its operation and potential for use in low voltage and high current applications. In addition, hardware prototypes for both ZVS-QR and traditional buck converters are constructed utilizing a Programmable Interface Controller (PIC). Results from hardware tests demonstrate the success of using digital controller for the 60W 12VDC to 1.5VDC ZVS-QR buck converter. Merits and drawbacks based on the operation and performance of both converters will also be assessed and described. Further work to improve the performance of ZVS-QR will also be presented.

Keywords: Buck Converter; Zero-Voltage-Switching; Multi-Phase; Efficiency; Switching Loss

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1. Introduction

Moore's Law states that the number of transistors on a chip will double approximately every two years. As a result, the voltage regulator modules (VRMs) for these microprocessors must be able to supply the increase in current demand. Traditionally, power supplies are able to take offline power of 120 VAC and rectify it to either a +5 VDC or +12 VDC at which point the VRMs are responsible to step down the DC voltage to the microprocessor's desired DC input voltage – which can range from 3.3 VDC to as low as 0.8 VDC.

In 2008, Intel just announced the world's first 2-billion transistor microprocessor codenamed Tukwila [1]. With the massive amounts of transistor in the new processor, the demand for low voltage and high output current supply will be even more desired. The Intel Core i7-980x has a thermal design power of 130W [2]. However, according to the data sheet, the processor can pull as much power as 180 W (1.263 VDC/140 ADC). There are other processors out on the market that demand the VRM to supply upwards of 400 W [3].

With such a high demand for low voltage and high output current, a single buck converter will certainly be severely stressed for such a daunting task. Therefore, the multiphase buck converter is the solution to this high demanding task. It allows for the ability to supply a huge output current without the negative effects of severe efficiency losses and thermal problems. The theory behind the multiphase buck converter is to put n amount of buck converters in parallel to operate in an interleaving style. The switching signals will create phases and be out of phase by $360/n$ degrees from one another. The benefit of such a topology is the ability to disperse the load current across the n number of buck converters so that the output current and heat and power dissipation in each of the

buck converters are within the limits of modern single-phase buck converters. Typical modern single-phase buck converters have an output current in the range of 10 to 25 ADC. In addition, an inherent benefit of the interleaved multiphase buck converter is its ability to naturally reduce both the input and output ripple currents due to an increased effective frequency of n times the buck converter's switching frequency – which leads to a reduction in the size of the filtering components required. Although the multiphase buck converter topology is becoming a standard in the VRMs of mobile CPU application, the industry's demand for faster, more powerful applications and products will certainly cause the movement towards more wide spread development of VRMs for other applications and products with the interleaved multiphase buck converter based topology.

Even though the multiphase buck converter is able to supply a greater output current than the single-phase buck converter, it is not significantly more efficient. In order to increase the efficiency of the buck converter, the power loss within the circuit needs to be minimized. The most significant point of power loss in the buck converter is in the switch due to the nature of hard-switching used in traditional PWM buck converters [4]. Through changing the switching trajectory of the switch, either by implementing a zero-voltage-switching resonant circuit as discussed later or a zero-current-switching resonant circuit in the buck converter, will result in an increase in the buck converter's power efficiency [5].

An overview of how a traditional hard-switching buck converter operates and the shortcomings of the topology will be reviewed, and the analysis of a zero-voltage-switching quasi-resonant buck converter will be covered to illustrate its benefits. In addition, the design of the resonant tank in the zero-voltage-switching quasi-resonant

buck converter and of a multiphase buck converter is illustrated. Also, utilizing and configuring a PIC as a digital switching controller, instead of an analog switching controller, will be discussed. As a culmination of all the topics shown, a design example – along with simulation and hardware prototype results – is completed using the design equations presented.

2. Shortfalls of the Traditional Pulse Width Modulation (PWM) Converter

In the theoretical analysis of a buck converter, there are a few assumptions made:

- 1) The switches are assumed to have zero conduction losses
- 2) The switching transitions are assumed to be instantaneously on or off
- 3) The voltage instantaneously changes from zero volts to a positive voltage while the current changes from a positive ampere value to zero amperes during a turn-off condition and vice versa occurs for a turn-on condition.

For improving efficiency of real world buck converters, the first assumption will be adjusted by selecting a switch such as MOSFET that has low on resistance loss (R_{DS-ON} for MOSFET) to lower the conduction losses. Dealing with the last two assumptions in real world, however, has a much harder solution towards reducing the switching losses of a buck converter. This is true especially that these two assumptions represent the biggest issue in a real world application. For example, no switch is able to have the voltage and current values change instantly. Instead, the voltage and current values suffer a rise and fall time – which leads to switching losses. In turn, the switching losses is heavily dependent on converter's switching frequency [6]. The further presents a conundrum in the buck converter where in order to have a low output voltage, small current ripple, and small total package size; the switching frequency must be greatly increased. However, having an increased switching frequency leads to not only higher switching losses, but also electromagnetic interference, and switching stress – which ultimately leads to reduced power efficiency and possibly reliability.

Switching losses stem from the rise and fall time associated with the voltage and current waveforms. Due to the slope of the rising voltage and falling current – or vice versa – the overlap of the two waveforms results in power loss due to the fact that power

is the byproduct of voltage and current, as shown in Figure 2-1. The more often the voltage and current waveforms overlap each other such as what happens when switching frequency is increased, the higher the switching loss becomes. As a result, the switching loss is directly proportional to the switching frequency.

Electromagnetic interference results from the slope of the voltage and current waveform during the switching transitions – as shown in Figure 2-1 for PWM converters. During the turn-on time, the current waveform suffers a rising slope of di/dt due to the bad reverse recovery characteristics of the freewheeling diode. Similarly during the turn-off time, the voltage waveform suffers a rising slope of dv/dt due to the stray inductance of the switch's opening. The two rising edges during both the turn-on and turn-off time are the sources of the electromagnetic interference – which gets increasingly significant as switching frequency increases.

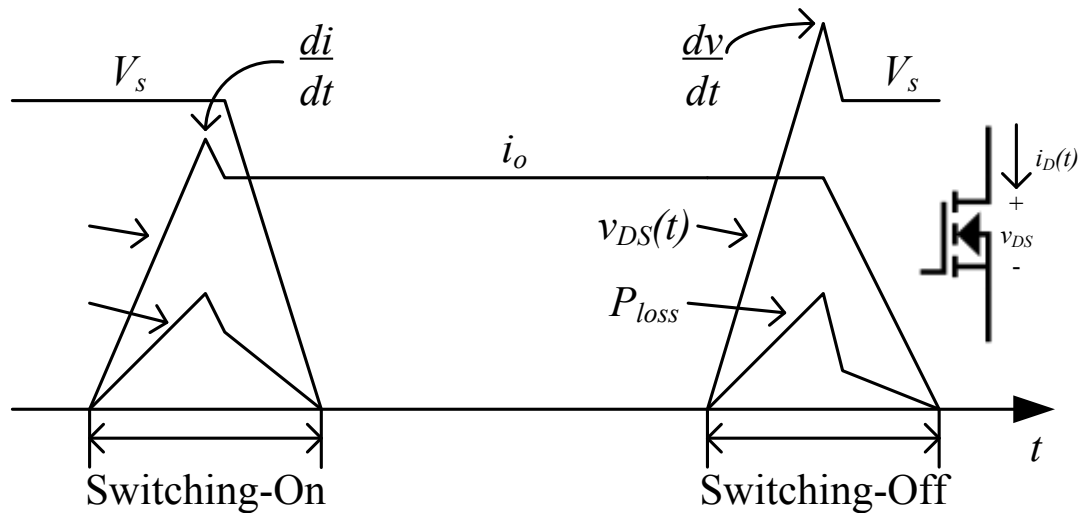


Figure 2-1: Switching Loss and EMI in a Hard-Switching Power Converter

Switching stress becomes a dominant factor as the required voltage and current of the switch increases. The switch has a safe operating area (SOA) as shown in Figure 2-2 in which the switching trajectory must fall within or else the switch risks being damaged or

even destroyed. An interesting point of concern is the spike of the voltage waveform during turn-off and the current waveform during turn-on. These spikes negatively impact the switching trajectory of the switch by pushing the switching trajectory closer towards the limits of the safe operating area. Due to the requirement of the switch's switching trajectory to stay within the safe operating area, the output current and voltage of the buck converter is limited.

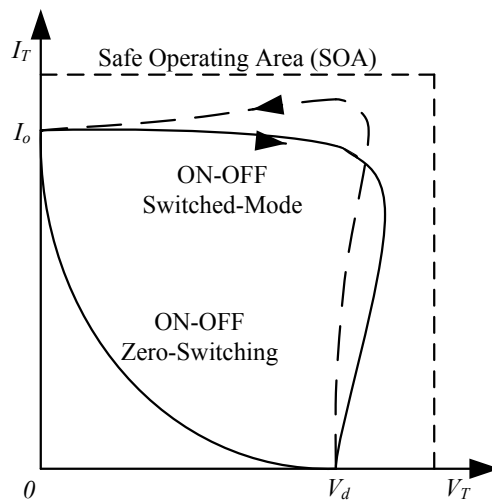


Figure 2-2: Switching Trajectory of a Switched Power Converter

The zero-voltage-switching quasi-resonant (ZVS-QR) buck converter addresses the three main issues that plague traditional PWM converters. Through the use of an inductor/capacitor (LC) resonant circuit in the buck converter, the switching trajectory is changed to allow for the buck converter to operate in zero-voltage-switching during both turn-on and turn-off times. The ability to have zero-voltage-switching allows for a reduction in the switching losses, reduction of the dv/dt and di/dt spike, and a reduction in the switching stress. As shown in Figure 2-3, the voltage waveform is changed to that of a resonant waveform and results in a smaller overlapping area of the voltage and current

waveform. This produces the ideal situation of greatly lowering power loss. The SOA shown in Figure 2-2 illustrates the switching trajectory of zero-voltage-switching changes in a manner that does not allow it to be anywhere near the safe operating area's limits. Overall, zero-voltage-switching helps the buck converter to increase power efficiency and reduce electromagnetic interference. With the three main issues addressed, the constraint of having a higher switching frequency is removed.

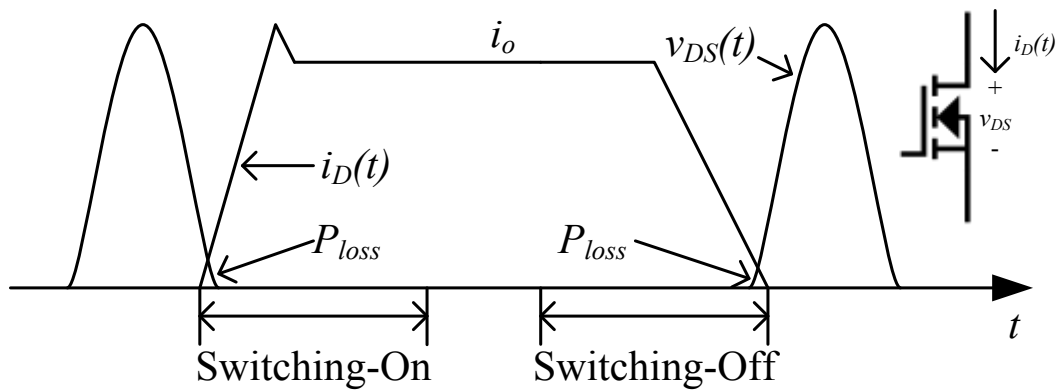


Figure 2-3: Switching Loss and EMI in a Resonant Power Converter

3. Analysis of a Zero-Voltage-Switching Quasi-Resonant Buck Converter

The difference between a traditional buck converter and a zero-voltage-switching quasi-resonant buck converter (ZVS-QR) is the addition of a resonant tank in the buck converter that contains a resonant inductor (L_r), resonant capacitor (C_r), and an anti-parallel diode (D_r) – as shown in Figure 3-1. The resonant inductor in series with the switch helps to limit the di/dt slope of the power switch while the resonant capacitor is used as a secondary energy transfer element. The inductor and capacitor together enter resonance at the moment the switch is turned off. The anti-parallel diode prevents the resonant capacitor (C_r) from reversing polarity. The rest of the ZVS-QR buck converter is a standard buck converter with the diode (D_m) being the freewheeling diode during the time the switch is off and the inductor (L_f) and capacitor (C_f) together operate as a second order low pass filter – but also provides a stable DC output source to the load. The ZVS-QR buck converter implements a soft-switching scheme for both the switch and the freewheeling diode because they both turn on and off at zero volts, and thus changing the switching trajectory from that of a regular buck. In order to simplify the analysis of the zero-voltage-switching quasi-resonant buck converter, the output inductor and capacitor will be grouped together to form a DC current source since the assumption is that the output filter produces a ripple free output due to very high switching frequency operation and large output inductance. In addition, the analysis begins with the following initial conditions:

- 1) the switch is on and current through the switch (Q) and resonant inductor (L_r) is the same as the output current (I_o)
- 2) the current in both the anti-parallel diode and the freewheeling diode is zero amperes

3) the voltage across the switch (Q) and the resonant capacitor (C_r) is zero volts

During one switching cycle, the zero-voltage-switching quasi-resonant buck converter can be broken into four different time intervals: (I) Linear Stage, (II) Resonant Stage, (III) Recovery Stage, and (IV) Freewheeling Stage – shown in figure 3-2. Also, the converter also has the following parameters:

$$\text{Characteristic Impedance: } Z_0 = \sqrt{\frac{L_r}{C_r}} \quad (3-1)$$

$$\text{Angular Resonant Frequency: } \omega_0 = \frac{1}{\sqrt{L_r C_r}} \quad (3-2)$$

$$\text{Resonant Frequency: } f_r = \frac{\omega_0}{2\pi} \quad (3-3)$$

$$\text{Switching Period: } T_s \quad (3-4)$$

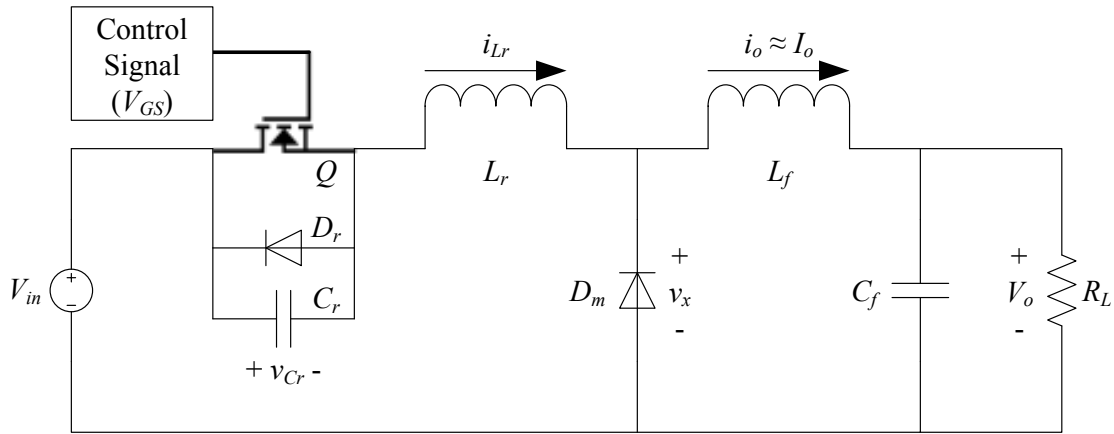


Figure 3-1: Circuit Diagram for Zero-Voltage-Switching Quasi-Resonant Buck Converter

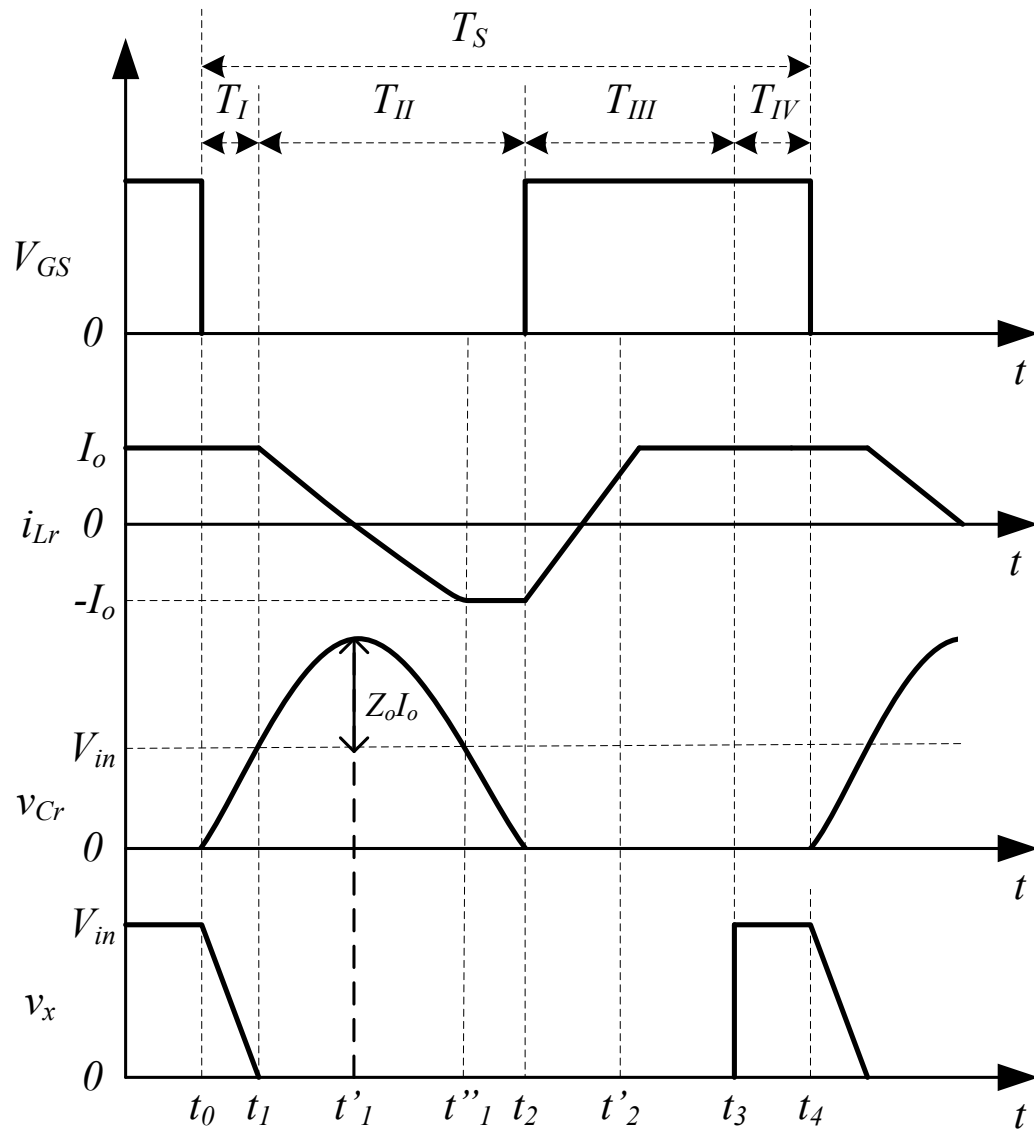


Figure 3-2: Steady-State Waveform of the Zero-Voltage-Switching Quasi-Resonant Buck Converter

3.1 Time Interval I: Linear Stage ($t_0 < t < t_1$)

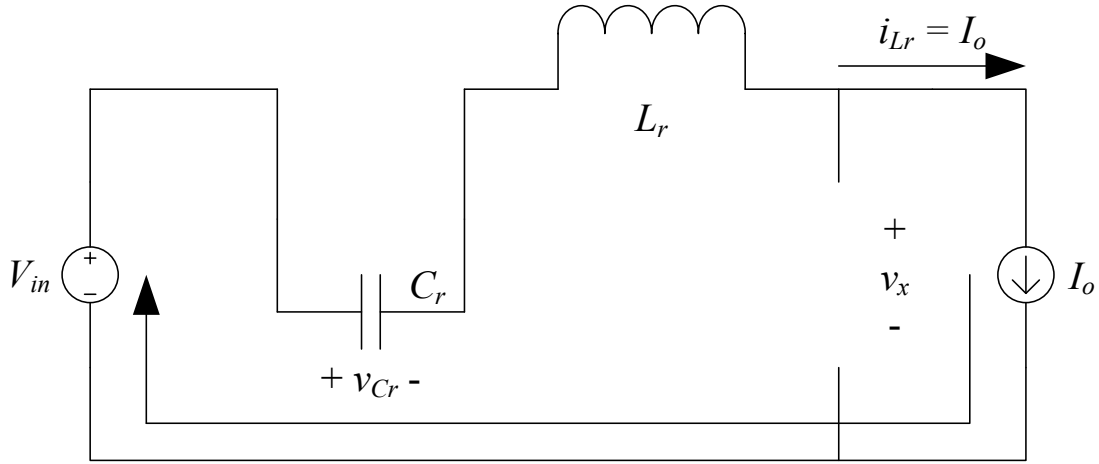


Figure 3-3: Equivalent Circuit for Time Interval I

After t_0 , the switch (Q) is turned off at zero volts. However, the current through the resonant inductor (L_r) cannot change instantaneously. As a result, the current through the resonant inductor remains the same as the output current (I_o) and linearly charges the resonant capacitor (C_r). The voltage across the resonant inductor remains at zero volts because there is no significant change in the current through the inductor. The voltage across the resonant capacitor charges according to the following equation

$$v_{C_r}(t) = \frac{1}{C_r} \int_0^t I_o d\lambda = \frac{I_o}{C_r} t \quad (3-5)$$

The voltage across the freewheeling diode is determined by the voltage difference

$$v_x(t) = V_{in} - v_{C_r}(t) = V_{in} - \frac{I_o}{C_r} t \quad (3-6)$$

Equation (3-6) shows that $v_x(t)$ is a linearly decreasing function, which starts at V_{in} . When $v_{C_r}(t)$ reaches the same voltage as V_{in} , the critical time, t_1 , is reached and $v_x(t)$

equals zero and the freewheeling diode turns on in a soft-switching manner. As a result, with V_{in} equaling v_{Cr} , the equation (3-5) can be used to solve for the critical time, t_1 .

$$t_1 = \frac{V_{in} C_r}{I_o} \quad (3-7)$$

Rearranging equation (3-7) and substituting into equation (3-6) will provide an alternate form of equation (3-6)

$$v_x(t) = V_{in} \left(1 - \frac{t}{t_1} \right) \quad (3-8)$$

Time Interval I is complete at $t = t_1$ when $v_{Cr}(t)$ equals V_{in} and $v_x(t)$ equals zero. As a result, Time Interval I can be summarized to the following equation

$$T_I = \frac{V_{in} C_r}{I_o} \quad (3-9)$$

3.2 Time Interval II: Resonance Stage ($t_1 < t < t_2$)

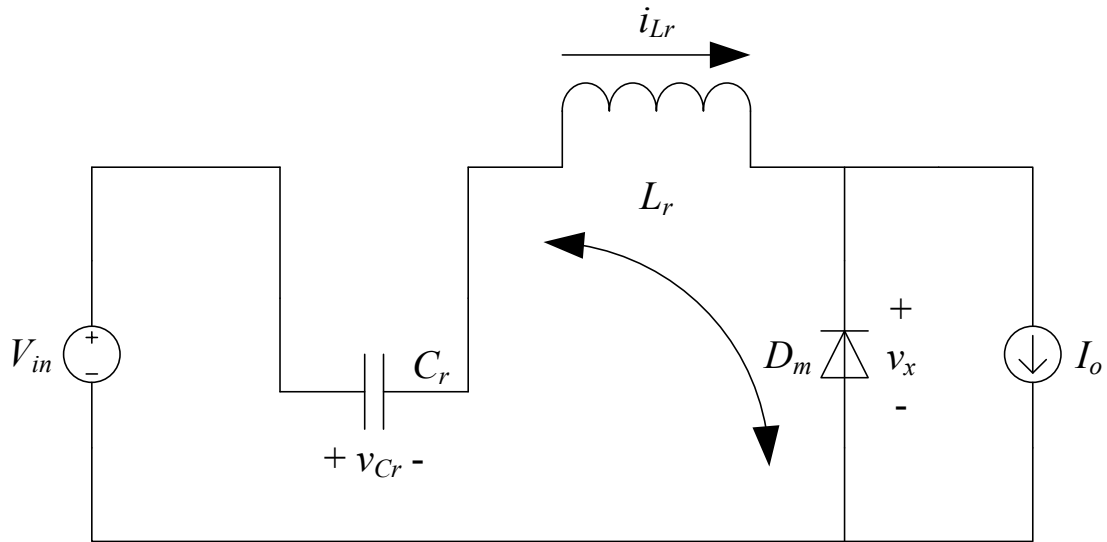


Figure 3-4: Equivalent Circuit for Time Interval II

After t_1 , $v_{C_r}(t)$ is greater than V_{in} and the freewheeling diode is forward biased. This results in both the resonant inductor (L_r) and resonant capacitor (C_r) to begin resonating. The KVL of the left loop of the circuit is

$$L_r \frac{di_L}{dt} + v_{C_r}(t) = V_{in} \quad (3-10)$$

$$L_r \frac{d^2 i_L}{dt^2} + \frac{dv_{C_r}(t)}{dt} = 0 \quad (3-11)$$

The capacitor current is related to the capacitor voltage by

$$i_{C_r}(t) = C_r \frac{dv_{C_r}(t)}{dt} \quad (3-12)$$

$$\frac{dv_{C_r}(t)}{dt} = \frac{i_{C_r}(t)}{C_r} \quad (3-13)$$

Equation (3-13) can then be substituted into equation (3-11)

$$L_r \frac{d^2 i_L}{dt^2} + \frac{i_{C_r}(t)}{C_r} = 0 \quad (3-14)$$

$$\frac{d^2 i_L}{dt^2} + \frac{i_{C_r}(t)}{L_r C_r} = 0 \quad (3-15)$$

Solving the differential equation of equation (15) results in

$$i_L(t) = I_o \cos \omega_o(t - t_1) \quad (3-16)$$

The resonant capacitor voltage can be expressed as the following with the initial condition of $v_{C_r}(t_1) = V_{in}$

$$v_{C_r} = \frac{1}{C_r} \int_{t_1}^t i_{C_r}(\lambda) d\lambda + v_{C_r}(t_1) \quad (3-17)$$

$$v_{C_r} = \frac{1}{C_r} \int_{t_1}^t I_o \cos[\omega_o(\lambda - t_1)] d\lambda + V_{in} \quad (3-18)$$

$$v_{C_r} = \frac{I_o}{\omega_o C_r} \sin[\omega_o(t - t_1)] + V_{in} \quad (3-19)$$

Using equations (3-1) and (3-2), the constant in front of equation (3-19) can be simplified to

$$\frac{I_o}{\omega_o C_r} = \frac{\sqrt{L_r C_r} I_o}{C_r} = \sqrt{\frac{L_r}{C_r}} I_o = Z_o I_o \quad (3-20)$$

This results in equation (3-20) being simplified to

$$v_{C_r} = Z_o I_o \sin[\omega_o(t - t_1)] + V_{in} \quad (3-21)$$

During Time Interval II will the voltage across the switch and resonant capacitor be at its maximum, which is when the $\sin[\omega_o(t-t_1)]$ from equation (3-21) equates to 1. The maximum $v_{C_r}(t)$ occurs at t_1' when

$$t_1' = \left(\sin^{-1} \frac{1}{\omega_o} \right) + t_1 \quad (3-22)$$

As a result, the maximum voltage across the switch and resonant capacitor is

$$v_{C_r, \max} = V_{in} + Z_o I_o \quad (3-23)$$

At t_2 , the voltage across the switch and resonant capacitor reaches zero volts [$v_{C_r}(t_2) = 0$], the current through the inductor is the negative value of the output current [$i_{L_r}(t_2) = -I_o$], and at the same time the anti-parallel diode begins to conduct so as to not have the resonant capacitor voltage reverse its polarity. Time t_2 can be solved from equation (3-21) by equating $v_{C_r}(t)$ to zero volts and substituting t_2 for t .

$$0 = Z_o I_o \sin[\omega_o(t_2 - t_1)] + V_{in} \quad (3-24)$$

$$t_2 = \frac{1}{\omega_o} \left[\sin^{-1} \left(\frac{V_{in}}{Z_o I_o} \right) + \pi \right] + t_1 \quad (3-25)$$

The Time Interval II can easily be solved by moving t_1 to the left hand side of equation (3-25) to summarize Time Interval II as

$$T_{II} = t_2 - t_1 = \frac{1}{\omega_o} \left[\sin^{-1} \left(\frac{V_{in}}{Z_o I_o} \right) + \pi \right] \quad (3-26)$$

3.3 Time Interval III: Recovery Stage ($t_2 < t < t_3$)

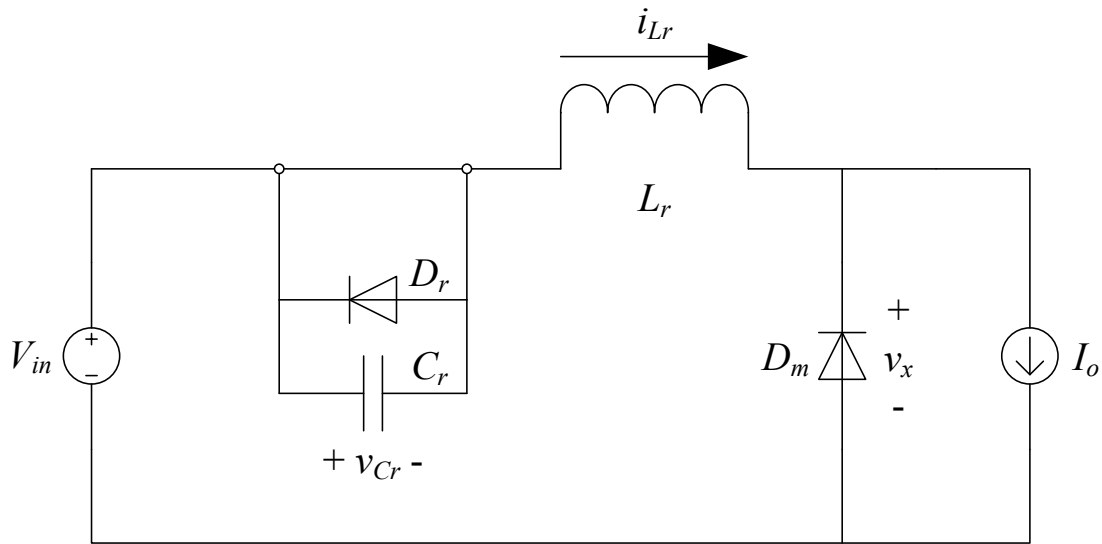


Figure 3-5: Equivalent Circuit for Time Interval III

After t_2 , both the freewheeling (D_m) and anti-parallel (D_r) diodes are forward biased. As a result, the voltage across the resonant capacitor (C_r) is held at zero volts by the anti-parallel diode. At the same time, the switch is turned on when the anti-parallel diode is conducting the negative resonant inductor (L_r) current to achieve zero-voltage-switching. This is the most important part of the switching cycle because the switch is turned on when zero volts is across the switch. This allows for the turn-on switching losses to be greatly reduced and the power efficiency of the buck converter to be proportionally increased.

During Time Interval III, the voltage across the resonant inductor is the same as V_{in} – which causes the resonant inductor current to return linearly from its negative peak of $-I_o$ to its positive peak of I_o . During the time the resonant inductor current is rising, the freewheeling diode current is falling by the same proportional amount. The resonant inductor current is expressed as

$$i_L(t) = \frac{1}{L_r} \int_{t_2}^t V_{in} d\lambda + i_L(t_2) \quad (3-27)$$

$$i_L(t) = \frac{V_{in}}{L_r} (t - t_2) + I_o \cos \omega_o (t_2 - t_1) \quad (3-28)$$

At t_3 , the resonant inductor current reaches I_o , so inserting I_o and $t = t_3$ into equation (3-28) and solve for t_3

$$i_L(t_3) = I_o = \frac{V_{in}}{L_r} (t_3 - t_2) + I_o \cos \omega_o (t_2 - t_1) \quad (3-29)$$

$$t_3 = \left(\frac{L_r I_o}{V_{in}} \right) [1 - \cos \omega_o (t_2 - t_1)] + t_2 \quad (3-30)$$

Time Interval III can easily be solved by moving t_2 to the left hand side of equation (3-30) to summarize Time Interval III as

$$T_{III} = \left(\frac{L_r I_o}{V_{in}} \right) [1 - \cos \omega_o (t_2 - t_1)] \quad (3-31)$$

3.4 Time Interval IV: Freewheeling Stage ($t_3 < t < t_4$)

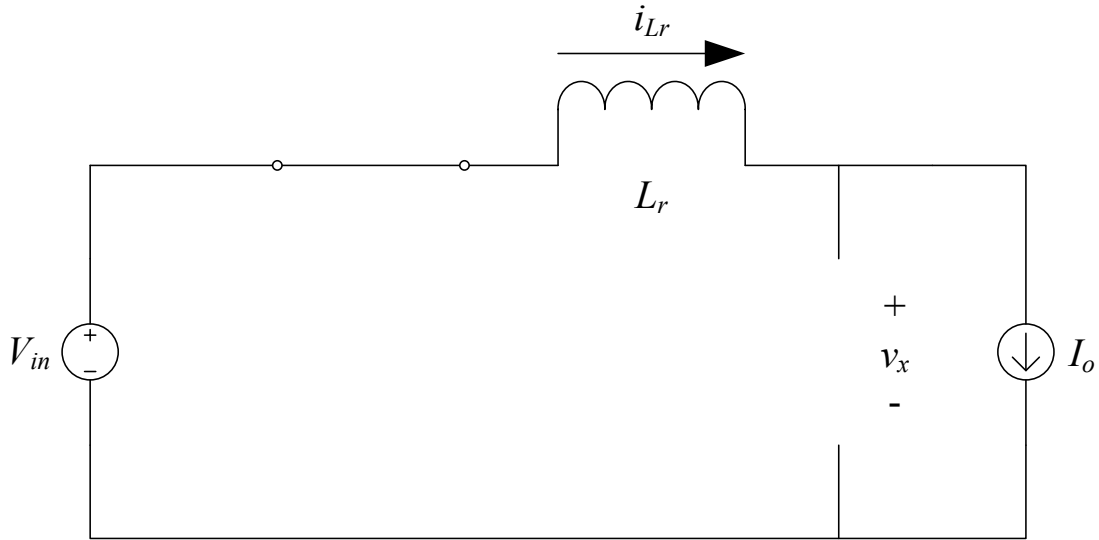


Figure 3-6: Equivalent Circuit for Time Interval IV

After t_3 , the switch (Q) remains closed and the freewheeling diode (D_m) turns off after the resonant inductor (L_r) current reaches the output current (I_o) value. As a result, both the freewheeling and anti-parallel (D_r) diodes are turned off. The current through the switch and resonant inductor is equal to the output current ($i_{Lr} = I_o$) and the voltage across the freewheeling diode is equal to V_{in} ($v_x = V_{in}$). The circuit now resembles a traditional hard switching PWM buck converter and remains as such until the next switching cycle begins.

At t_4 , the switch is turned off again to begin another switching cycle. Time Interval IV can be controlled by the switching frequency. Time Interval IV is determined by subtracting the previous three Time Intervals from the total switching period

$$T_{IV} = T_s - (T_I + T_{II} + T_{III}) \quad (3-32)$$

3.5 Output Voltage

During the analysis of a zero-voltage-switching quasi-resonant buck converter, the output voltage of the buck converter can be considered as the average voltage across the freewheeling diode, $v_x(t)$, because it is the input to the converter's output filter. However, the value of $v_x(t)$ varies throughout the switching period

$$v_x(t) = \begin{cases} V_{in} \left(1 - \frac{t}{t_1}\right) & 0 < t < t_1 \\ 0 & t_1 < t < t_3 \\ V_{in} & t_3 < t < T_S \end{cases} \quad (3-33)$$

The average value of $v_x(t)$ determines the output voltage of the zero-voltage-switching quasi-resonant buck converter as

$$V_O = \frac{1}{T_S} \int_0^{T_S} v_x(t) dt \quad (3-34)$$

$$V_O = \frac{1}{T_S} \left[\int_0^{t_1} V_{in} \left(1 - \frac{t}{t_1}\right) dt + \int_{t_1}^{t_3} 0 dt + \int_{t_3}^{T_S} V_{in} dt \right] \quad (3-35)$$

$$V_O = \frac{V_{in}}{T_S} \left[\frac{t_1}{2} + (T_S - t_3) \right] \quad (3-36)$$

$$V_O = V_{in} \left[1 - f_S \left(t_3 - \frac{t_1}{2} \right) \right] \quad (3-37)$$

The output voltage equation, equation (3-37), easily shows that the output voltage is highly dependent and inversely proportional upon the switching frequency. An increase in the switching frequency will result in a decrease in output voltage. More so, an increase or decrease in the switching frequency will affect Time Interval IV the most, but the constraint is the switching period cannot be less than t_3 .

4. Design Requirements

The Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter was designed to the parameter requirements listed in Table 4-1. The parameters were set to accomplish a Two-Phase ZVS-QR Buck Converter that was high power and has better efficiency over the traditional Pulse Width Modulation Buck Converter. Since many buck converters are being used in computing platforms, the proposed converter will be designed to have input and output voltages at the level that would be useable for such applications.

Since most computing power supplies or power adapters take the wall outlet 120VAC and convert it into 12 VDC for the main logic board, the proposed converter will have an input voltage of 12 VDC. Most of all computing applications then branch from the 12 VDC main power supply rail and convert it into the necessary voltage for their specific design block – typically 5.0 VDC, 3.3 VDC, 1.8 VDC, 1.5 VDC, and 0.9 VDC.

In terms of output power level, the output voltage and current levels were chosen so the converter could be used in realistic applications. Many of the computing memory modules require 1.8 VDC and 1.5 VDC for their VCC input pin and computing processors have their upper voltage requirement at approximately 1.6 VDC for Intel's VR10 and VR11 [7]. As a result, the common overlapping voltage level was 1.5 VDC, and this was chosen to simulate possible real world applications for the proposed converter's output voltage level. The output current level was chosen at 40 A because the industry's rule of thumb is approximately 20 A should be supplied by one phase. Since this proposed converter is a two phase design and following the industry's rule of thumb for buck converters, the total output current level was chosen at 40 A. This results in an output power level of 60W.

The switching frequency was selected to be 100 kHz because the controller for the proposed converter is a digital PIC controller from Microchip and it does not use the traditional analog compensation loops. The PIC uses a PID control scheme and uses a DAC to sense the input voltage instead of a traditional op amp. To keep things simple and not have compensation issues of running the converter too fast, a lower switching frequency of 100 kHz was chosen. However, with the two phase of the proposed converter, the effective switching frequency will be double that of the switching frequency of a single phase – which results in 200 kHz both at the input and output of the converter.

Most buck converters on the market have efficiencies of at least 80%. The better buck converters are seeing efficiency levels into the 90% range. As a result, a good efficiency target to meet would be greater than 85%. Since the basis of this proposed convert is increased efficiency, a similar board will be built using the traditional PWM converter with the exact same components and PCB layout. This will provide an equal and quantitative comparison between the Two-Phase ZVS-QR Buck Converter and the Two-Phase Pulse Width Modulation Buck Converter.

To ensure a stable and excellent quality output, the proposed converter should have its output voltage ripple, line regulation, and load regulation to be less than 1%. Under any circumstances, the peak-to-peak output voltage ripple should be within 1% of 1.5 VDC. The input voltage must be able to vary positively or negatively by 10% from its nominal 12 VDC value (13.2 VDC and 10.8 VDC, respectively). The output current must be able to sweep from a no load condition to a full load condition while maintaining its output voltage to within 1% of 1.5 VDC.

Table 4-1: Design Requirements of the Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter

Parameters	Requirement
Rated Power	60 Watts
Input Voltage	12 V _{DC}
Output Voltage	1.5 V _{DC}
Input Current Max	5 Amps
Output Current Max	40 Amps
Operating Frequency	100 kHz
Line Regulation	< 1%
Load Regulation	< 1%
Output Voltage Ripple	< 1% V _{P-P}
Efficiency	> 85%

5. Analysis of the Resonant Inductor and Resonant Capacitor Circuit Characteristics

In order for the resonant tank to allow zero-voltage switching in the buck converter, the following constraint equation must be maintained.

$$Z_O I_O > V_{in} \quad (5-1)$$

Substituting the impedance of a capacitor into the characteristic impedance of equation (5-1) results in the sizing constraint of the resonant capacitor

$$\left(\frac{1}{\omega_O C_r} \right) I_O > V_{in} \quad (5-2)$$

$$C_r < \frac{I_O}{\omega_O V_{in}} \quad (5-3)$$

Similarly, substituting the impedance of an inductor into the characteristic impedance of equation (5-1) results in the sizing constraint of the resonant inductor

$$(\omega_O L_r) I_O > V_{in} \quad (5-4)$$

$$L_r > \frac{V_{in}}{\omega_O I_O} \quad (5-5)$$

In order to derive the characteristic graph of the resonant tank, the conservation of energy is being used where the input energy (W_i) equals the output energy (W_o) – while ignoring power loss and having in the converter operate in steady state. The energy stored in the resonant tank is

$$W_i = V_{in} \left[\int_{t_1}^{t_2} i_{L_r} dt + \int_{t_2}^{t_3} i_{L_r} dt + I_O (T_S - T_{II} - T_{III}) \right] \quad (5-6)$$

Evaluating the integrals of equation (5-6) in separate parts for easier simplification results in

$$\int_{t_1}^{t_2} i_{L_r} dt = -C_r V_{in} \quad (5-7)$$

$$\int_{t_2}^{t_3} i_{L_r} dt = \frac{L_r I_O^2 [1 - \cos^2 \omega_o (t_2 - t_1)]}{2V_{in}} \quad (5-8)$$

A substitution variable for the pulse width angle (α), with units in radians, is used to simplify the evaluation of equation (5-8).

$$\alpha = \omega_o (t_2 - t_1) \quad (5-9)$$

The last portion of equation (5-8) is expanded by substituting the respective time interval equations.

$$I_O (T_S - T_{II} - T_{III}) = I_O \left[T_S - \frac{I_O L_r (1 - \cos \alpha)}{V_{in}} - \frac{\alpha}{\omega_o} \right] \quad (5-10)$$

The energy output of the resonant tank is

$$W_O = V_O I_O T_S \quad (5-11)$$

Equating both equation (5-6) and (5-10) together and solving for the voltage ratio of output voltage divided by input voltage leads to the characteristic equation of a zero-voltage-switching buck converter.

$$\frac{V_O}{V_{in}} = \frac{1}{I_O T_S} \left[\alpha + \frac{\omega_o I_O L_r}{V_{in}} (1 - \cos \alpha) + \frac{\omega_o C_r V_{in}}{2I_O} \right] \quad (5-12)$$

$$\frac{V_O}{V_{in}} = X = 1 - \frac{f_s}{2\pi f_r} \left[\alpha + \frac{X(1 - \cos \alpha)}{r} + \frac{r}{2X} \right] \quad (5-13)$$

where r is the normalized load resistance defined as $r = R_L / Z_0$. The value of the pulse width angle in radians determines whether Time Interval II's resonance waveform operates in half-wave or full-wave mode. The pulse width angle's value has the following allowable range

$$\pi < \alpha < \frac{3\pi}{2} \text{ Half-Wave Mode} \quad (5-14)$$

$$\frac{3\pi}{2} < \alpha < 2\pi \text{ Full-Wave Mode} \quad (5-15)$$

As a result, the voltage ratio is a function of the pulse width angle, the switching and resonant frequency ratio, the characteristic impedance of the resonant tank, and the output load current.

Equation (5-13) is the starting point of the design for the resonant tank of a zero-voltage-switching buck converter because it leads to the characterization graph shown in Figure 5-1. Figure 5-1 has the switching frequency to resonant frequency ratio as the independent variable and the voltage ratio as the dependent variable. The normalized load resistor is the changing parameter to output different DC characteristic curves. Thus, the normalized load resistor must be determined based the evaluation of the buck converter's requirements.

Normalized Output vs. Normalized Switching Frequency (Half Wave)

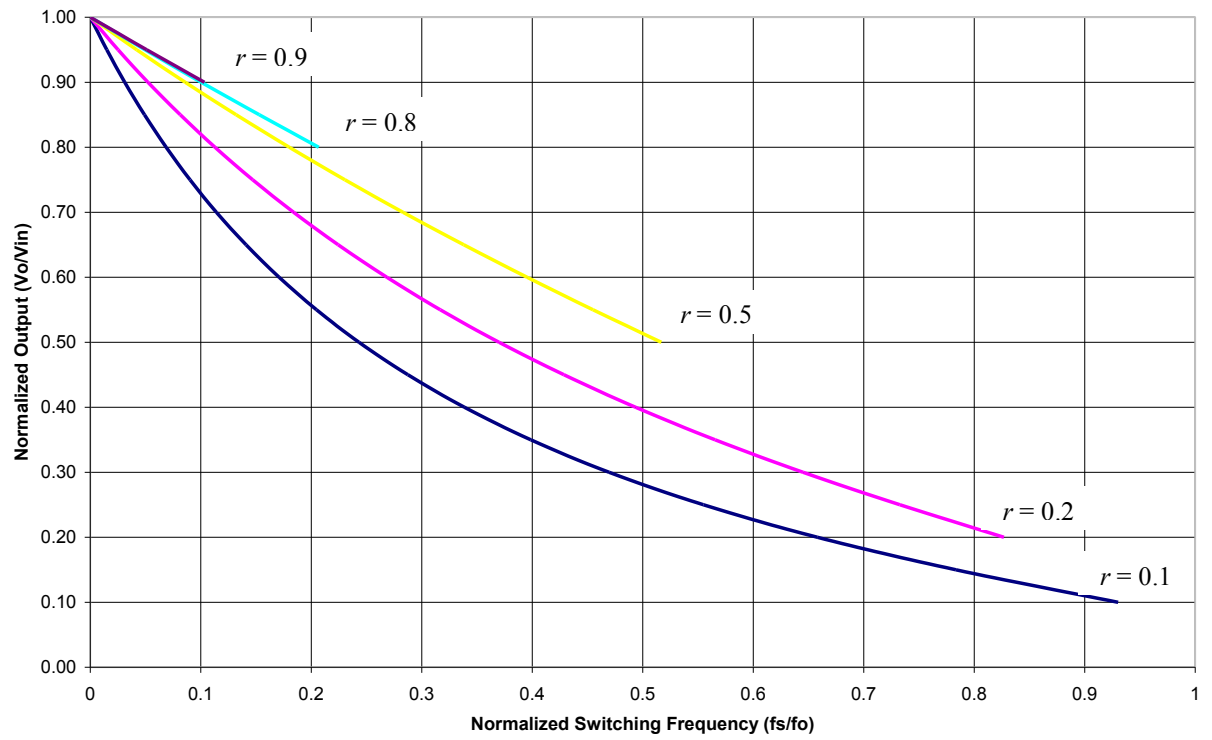


Figure 5-1: Normalized Output versus Switching Frequency with $r = RL/Z_o$ as a Parameter. ($\alpha = 5\pi/4$)

6. Design Calculations of a Multi-phase Buck Converter

The Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter is designed very similarly to that of a Two-Phase Pulse Width Modulating (PWM) Buck Converter. As a result, the design calculations will start off with baseline values by determining values for the Two-Phase PWM Buck Converter and then adding on additional operating conditions for the Two-Phase ZVS-QR Buck Converter. Since the components for the Two-Phase PWM Buck Converter and the Two-Phase ZVS-QR Buck Converter must be the same, then the component selection must also change with the additional operating conditions of the Two-Phase ZVS-QR Buck Converter.

6.1 Duty Cycle

Duty cycle is defined as the percentage of the switching period in which the top side MOSFET is conducting. For a PWM buck converter, the duty cycle (D) is determined by a voltage ratio – which is the output voltage divided by the input voltage assuming continuous conduction mode. With an input voltage of 12 VDC and an output voltage of 1.5 VDC, the duty cycle is 0.125. This means the top side MOSFET is only conducting 12.5% of the switching period.

$$V_{OUT} = DV_{IN} \quad (6-1)$$

$$D = \frac{V_{OUT}}{V_{IN}} \quad (6-2)$$

$$D = \frac{1.5V}{12.0V} = 0.125 \quad (6-3)$$

6.2 Inductor

The inductor is one of the main energy storage components in a buck converter. It is the charging and discharging of the magnetic field that creates the saw-tooth waveform

that flows through an inductor. A larger value inductor will reduce the ripple current through the inductor which will in turn reduce the peak-to-peak output voltage ripple. The opposite is also true with a smaller inductor which will result in a larger ripple current through the inductor and in turn causes an increase in the peak-to-peak output voltage ripple. With a buck converter, if the minimum value of the inductor current waveform drops below 0 A, then the buck converter is operating in discontinuous conduction mode (DCM). When the waveform minimum value is above 0 A, then the buck converter is operating in continuous conduction mode (CCM). The formulas and relationships generated in this paper assume the buck converter is operating in continuous conduction mode. As a result, every effort should be made to have the buck converter operate in continuous conduction mode – although it is impossible in a no load condition. The design does have control at which point the buck converter exits discontinuous conduction mode and enters continuous conduction mode. The inductor value is the controlling mechanism for determining the point at which the buck converter remains in continuous conduction mode for a pre-determined current value. This important inductor value is known as the critical inductance value and the formula to calculate its value is:

$$L_C = \frac{(1 - D) \overline{\overline{V_{OUT}}}}{2f_s \overline{\overline{I_{OUT,MIN}}}} \quad (6-4)$$

The critical inductance value is calculated slightly different for a multi-phase buck converter. The only difference is the sizing of the inductor which carries the output current is split between the n phases. As a result, the load output current should be divided by the n phases to determine the critical inductance.

$$L_C = \frac{(1 - D) \overline{V_{OUT}}}{2f_s \overline{I_{OUT,MIN}}/n} \quad (6-5)$$

$$L_C = \frac{(1 - 0.125) 1.5V}{2 * 100kHz \frac{4A}{2}} \quad (6-6)$$

$$L_C = 3.28\mu H \quad (6-7)$$

The critical inductance value is 3.28 μ H. This means as long as the current through the inductor is greater than 2 A per phase or a total output current of 4 A from the buck converter, then the buck converter will operate in CCM. Since there is no 3.28 μ H inductor value, the closest larger commercially available inductor value is 3.30 μ H.

6.3 Input Capacitor

The role of input capacitors for a buck converter is to provide a nice solid input voltage to the buck converter. For a buck converter, the input side is connected to the high-side MOSFET which makes it noisy because the current waveform is chopped into a section coinciding with the duty cycle when the high-side MOSFET is turned on. The input capacitors help to provide the current needed instantaneously when the high-side MOSFET turns on and prevents the input voltage from drooping at that point in time.

The formula for sizing the input capacitors is taken from [8] and is given by the following:

$$C_{IN} \geq \frac{D * \overline{I_O} * (1 - D)}{\Delta V_{IN} * f_{SW}} \quad (6-8)$$

$$C_{IN} \geq \frac{(0.125) * (40A) * (1 - 0.125)}{(0.120V) * (100kHz)} \quad (6-9)$$

$$C_{IN} \geq 365\mu F \quad (6-10)$$

A bulk input capacitance of 365 μF is the required minimum input bulk capacitance to keep the input voltage peak to peak ripple at 0.120 V. Many application engineers will place as much input capacitance as the design and PCB space will allow. These are often called “stiffening up the input voltage plane.” The more input capacitance the buck converter has, the less likely any instantaneous current demand will collapse the input voltage and cause the buck converter to operate outside of design requirements.

Although the formula dictates the input capacitors should be at least 365 μF , this is only for the bulk capacitors. In addition to the bulk capacitors, ceramic capacitors should be placed as close as possible to the input of the high-side MOSFET as possible. During the turn-on of the high-side MOSFET, current will need to be drawn from the capacitors before the input voltage’s power supply can supplement the necessary current. The current will first come from the ceramic capacitors due to their low ESR values and then the bulk capacitors with higher ESR values will help supply the necessary current until the input power supply can supply the needed current. Typically, 0.1 μF and 4.7 μF or 10 μF capacitors are placed in parallel as close to the input to the high-side MOSFET as possible. This is done to reduce the PCB DC resistance (DCR) which when it goes too high can negatively affect the current delivery of the input capacitor to the buck converter.

The input capacitors will also need to be selected based on its rated voltage. Unfortunately, capacitors do not maintain capacitance over its entire voltage range. As the voltage increases across the capacitor, the capacitance also decreases. Due to such the relationship, capacitors are typically de-rated in the designs. The industry’s rule of thumb is to double the desired operating voltage and then select the capacitor’s rated voltage

with this value as a minimum. For this design, the input voltage of 12.0 V will need to be doubled to 24.0 V in order to start the selection of the capacitors based on the parameter of rated voltage.

6.4 Output Capacitor

For the same role as the input capacitance supplying the instantaneous demand of current to the buck converter, the output capacitance supplies the instantaneous demand of current to the point of load. The formula for sizing the output capacitors is provided in [9]:

$$C_{OUT} \geq \frac{(1 - D)}{\frac{\Delta V}{V_{OUT}} * 8 * L * f_S^2} \quad (6-11)$$

$$C_{OUT} \geq \frac{(1 - 0.125)}{(0.01)(8)(3.3\mu H)(100kHz)^2} \quad (6-12)$$

$$C_{OUT} \geq 331\mu F \quad (6-13)$$

The minimum capacitance necessary at the output to maintain a peak-to-peak ripple current of less than 1% is 331 μ F. However, a higher output capacitance value than the minimum required will result in a further reduction of the peak-to-peak output voltage ripple. Having multiple output capacitors in parallel is even more beneficial because the more capacitors in parallel will result in a greater reduction in capacitor's ESR. This reduction in ESR will help to lower the peak-to-peak output voltage ripple and RMS loss of the capacitor.

As with the input capacitance bank, the output capacitance must also have ceramic capacitors to supply the instantaneous current demand from the point of load. Typically, 0.1 μ F and 10 μ F or 22 μ F capacitors are placed in parallel as close to the point of load as

possible. For point of loads that require voltage changes within a defined period of time such as CPU's Dynamic Voltage Identification (DVID) changes, then the output capacitor banks will have a higher number of ceramic capacitors than bulk capacitors. Usually in the output capacitor bank, there is a one-to-one ratio of bulk capacitors and ceramic capacitor pairs of 0.1 μF and 10 $\mu\text{F}/22 \mu\text{F}$.

The output capacitors will also need to be selected based on its rated voltage. As with the input capacitors, the output capacitance's rated voltage will also need to be doubled from its desired operating voltage. For this design, the output voltage is 1.5 V, so it is desirable to select a capacitor with a rated voltage equal to or greater than 3.0 V.

6.5 High-Side Power MOSFET

The two main parameters to concentrate on when selecting a MOSFET are the rated voltage and rated current capacity.

The rated voltage is calculated as the maximum drain-source voltage (V_{DS}) of the MOSFET at any given time. For a regular buck converter, this is simply the same as the input voltage because when the low-side MOSFET or freewheeling diode is conducting then the source of the MOSFET is directly connected to ground and the drain of the MOSFET is permanently connected to the input voltage.

$$V_{DS} = V_{IN} \quad (6-14)$$

$$V_{DS} = 12.0V \quad (6-15)$$

To calculate the RMS drain current (I_D) requirement for the high-size MOSFET, the following formula is used:

$$I_D = D * I_{OUT,max} \quad (6-16)$$

However, this design is for a two-phase buck converter, so the maximum current needs to be divided by the number of phases in the buck converter. In this case, the value is two. This results in the following revised formula:

$$I_D = \frac{1}{n} * D * I_{OUT,max} \quad (6-17)$$

$$I_D = \frac{1}{2} * (0.125) * (40A * 1.5) \quad (6-18)$$

$$I_D = 3.75A \quad (6-19)$$

The output current is multiplied by 1.5 to take into account the typical over current protection (OCP) level of 130% of the desired output current and then 20% additional overhead above the OCP value so it can sustain the current due to the converter having a constant current OCP protection topology, or having a multiphase buck converter lacking reasonable current balancing between phases.

Although the previous numbers are calculated to provide a preliminary MOSFET selection, the goal of this proposed converter is to illustrate the efficiency increase of using a Two-Phase ZVS-QR Buck Converter. The final MOSFET calculation numbers for the proposed converter will be solidified in the next section when higher stress operating conditions are taken into consideration.

6.6 Freewheeling Diode

Just like the MOSFET, the two main parameters are the rated voltage and rated current capacity. The rated voltage is calculated as the maximum voltage across the cathode and anode to resist any current flow. This is known as the DC blocking voltage. Just as the high-side MOSFET needs to tolerate the input voltage when the freewheeling

diode is conducting, the freewheeling diode must be able to tolerate the input voltage when the high-side MOSFET is conducting.

$$V_{RRM} = V_{IN} \quad (6-20)$$

$$V_{RRM} = 12.0V \quad (6-21)$$

To calculate the RMS diode forward current (I_F) for the freewheeling diode, the following formula is used:

$$I_F = (1 - D) * I_{OUT,max} \quad (6-22)$$

Just as with the high-side MOSFET, the current rating of the diode is divided by n-phases in the buck converter to produce a revised formula:

$$I_F = \frac{1}{n} * (1 - D) * I_{OUT,max} \quad (6-23)$$

$$I_F = \frac{1}{2} * (1 - 0.125) * (40A * 1.5) \quad (6-24)$$

$$I_F = 26.25A \quad (6-25)$$

As with the high-side MOSFET, the output current is multiplied by 1.5 to take into account the typical over current protection (OCP) level of 130% of the desired output current and then additional overhead above the OCP value to sustain the current due to the converter having a constant current OCP protection topology or having a multiphase buck converter without reasonable current balancing between phases.

6.7 Feedback Voltage Sensing Resistors

The buck converters are able to maintain output voltage regulation by sampling the output voltage and adjusting some control parameters in the buck converter. In the case of the traditional pulse width modulation buck converter, the control parameter being adjusted is the duty cycle. By sampling only the output voltage, the control loop is a

voltage mode control loop. If the sampling includes current sampling at either the high-side MOSFET or the inductor, then the control loop is a current mode control loop. Both the converters produced in this specific thesis will utilize voltage mode control loop.

The output voltage sampling must be compared to a steady and stable voltage source. The most logical choice is to use a voltage reference source since it is designed to be stable across a wide range of temperatures and conditions. The voltage reference must be chosen to have a value that is reasonably less than the designed output voltage of the buck converter. Since the desired output voltage is 1.5 V, then a voltage reference source should be about half of the value, which results in 0.75 V. Unfortunately there are not many external voltage references available at such a low value. As a result, due to the market availability of voltage reference sources, a value of 0.9 V for the voltage reference source was chosen. The selected component is the ISL21080DIH309 from Intersil. It provides an accuracy within 0.5% and has a temperature coefficient of 50ppm/°C. The voltage reference source will be connected to the external voltage reference pin of the Microchip dsPIC30F2020.

The output voltage will be sampled to the Microchip dsPIC30F2020 by means of a resistor divider. The resistor divider is chosen to have an input voltage of 1.5 V and have an output voltage of 0.9 V. This creates a voltage ratio of 0.6.

$$V_{OUT} = \frac{R_2}{R_1 + R_2} * V_{IN} \quad (6-26)$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{0.9V}{1.5V} = 0.6 \quad (6-27)$$

Selecting R_1 to have a value of 10 k Ω results in R_2 being 15 k Ω . This resistor divider network will reduce the output voltage level and feed it back into the Microchip

dsPIC30F2020 for PID control loop processing. With a total equivalent resistance of 25 k Ω , the total current flow through the resistors is 60 μ A. This equates to a power dissipation of the following:

$$P_{R1} = I^2R = (60\mu A)^2(10k\Omega) = 36\mu W \quad (6-28)$$

$$P_{R2} = I^2R = (60\mu A)^2(15k\Omega) = 54\mu W \quad (6-29)$$

With power dissipation in the microwatts, any resistor package size will work – even the tiny 01005 package size. A 01005 package size has a power rating of 31mW. However, for ease of soldering, a 0603 package size will be used – which has a power rating of 0.1 W.

Table 6-1: Summary of Component Selections for the Two-Phase Traditional PWM Buck Converter

Component	Component Size
Critical Inductance	3.3 μ H
Input Capacitance	470 μ F
Output Capacitance	470 μ F
High-Side MOSFET Voltage	12V
High-Side MOSFET Current	3.75A
Freewheeling Diode Voltage	12V
Freewheeling Diode Current	26.25A
Top Resistor of Feedback Ladder	10k Ω
Bottom Resistor of Feedback Ladder	15k Ω

7. Design Calculations of a Zero-Voltage-Switching Quasi-Resonant Buck Converter

7.1 Resonant Inductor and Capacitor

In order for the resonant tank to allow zero-voltage switching in the buck converter, the resonant capacitor and inductor are calculated using:

$$\frac{V_o}{V_{in}} = X = 1 - \frac{f_s}{2\pi f_r} \left[\alpha + \frac{X(1 - \cos \alpha)}{r} + \frac{r}{2X} \right] \quad (7-1)$$

The proposed converter will operate in half-wave mode and have a pulse width angle of $5\pi/4$ radians because it is the median point between the two half-wave mode limits. As a result, the voltage ratio is a function of the pulse width angle, the switching and resonant frequency ratio, the characteristic impedance of the resonant tank, and the output current.

Equation (7-1) is the starting point of the design for the resonant tank of a ZVS-QR buck converter because it leads to the characterization graph shown in Figure 5-1. Figure 5-1 shows the switching frequency to resonant frequency ratio as the independent variable, and the voltage ratio as the dependent variable. The normalized load resistor is the changing parameter to output different DC characteristic curves. Thus, the normalized load resistor must be determined based the evaluation of the buck converter's requirements.

The first step towards determining the normalized load resistor, the normalized output must be calculated. This can be thought of as the duty cycle because the normalized output is the output voltage divided by the input voltage. For the proposed converter, the normalized output is 0.125.

$$\text{Normalized Output} = \frac{V_O}{V_{IN}} = \frac{1.5V}{12.0V} = 0.125 \quad (7-2)$$

Referencing back to Figure 5-1, the normalized load resistance r-value curve that reaches a normalized output of 0.125 is $r=0.1$. Recall that the normalized load resistance r-value is defined as the output load resistance divided by the characteristic impedance.

Armed with the values for the normalized output (X), normalized load resistance (r), pulse width angle (α), and switching frequency (f_s), the values are placed into the following formula to calculate the resonant frequency (f_r):

$$\frac{V_O}{V_{IN}} = X = 1 - \frac{f_s}{2\pi f_r} \left[\alpha + \frac{X(1 - \cos \alpha)}{r} + \frac{r}{2X} \right] \quad (7-3)$$

The resonant frequency is calculated to be approximately 118 kHz. This will result in an angular frequency of the following:

$$\omega_o = 2\pi f_r = 2\pi * (118 \text{ kHz}) \quad (7-4)$$

$$\omega_o = 741415.866 \text{ rad/sec} \quad (7-5)$$

Since the design requirement is a 60W converter of an output voltage of 1.5V at 40A output current. This results in a load resistance of 0.0375Ω . Solving for the characteristic impedance results in:

$$Z_o = \frac{R_L}{r} = \frac{0.0375\Omega}{0.1} \quad (7-6)$$

$$Z_o = 0.375\Omega \quad (7-7)$$

The characteristic impedance is the square root of the resonant inductor divided by the resonant capacitor. After all of the above calculations, the limits for the selection of the resonant inductor (L_r) and resonant capacitor (C_r) may be determined as follows:

$$L_r > \frac{V_{IN}}{\omega_o I_o} = \frac{12.0V}{(741415.8662 \text{ rad/sec})(20A)} \quad (7-8)$$

$$L_r > 0.813\mu H \quad (7-9)$$

$$C_r < \frac{I_o}{\omega_o V_{IN}} = \frac{20A}{(741415.8662 \text{ rad/sec})(12.0V)} \quad (7-10)$$

$$C_r < 2.26\mu F \quad (7-11)$$

Due to the restrictions of certain capacitance and commercially available inductance values, the chosen inductance is 1.0 μ H, which results in a calculated resonant capacitor value of 1.8 μ F with the capacitor constraint of maintaining the resonant capacitance below 2.26 μ F. Based from the waveform diagram of Figure 3-2, the maximum voltage placed upon the capacitor is

$$V_{Cr,max} = V_{IN} + \frac{I_o}{\omega_o C_r} = 12.0V + \frac{20.0A}{(741415.8662 \text{ rad/sec})(1.8\mu F)} = 29.31V \quad (7-12)$$

However, due to the fact that the capacitor's value decreasing as the voltage is applied across the capacitor increases, the capacitor's rated voltage should be doubled from what is expected. Doubling the expected voltage would be approximately 60 V. Unfortunately, the most common voltage values are 50 V, 63 V, and 100 V – with the most abundant capacitor values to choose from at 50 V and 100 V. The capacitor dielectric is important since the capacitance may also vary as the temperature changes. The most temperature stable and commonly available capacitor dielectric is X7R and it will be used for the capacitor dielectric. As a result, the resonant capacitor is an X7R 100V 1.8 μ F capacitor.

The maximum current flowing through the resonant inductor is the same current supplied to the point of load. In this case, the total current of 40 A is split between two

phases to subject each phase to approximately 20 A. As long as the inductor can sustain at least 20 A, then the inductor will not saturate. The resonant inductor is chosen to be Vishay IHLP6767GZER1R0M01 due to its ability to maintain the inductance value of 1.0 μH from 0 A all the way to the desired 20 A. Vishay's inductor also has excellent electrical specifications with low DCR and very high DC saturation current. As a result, the resonant inductor is 1.0 μH 1.28 $\text{m}\Omega$ 48 A.

7.2 High-Side MOSFET

In the ZVS-QR Buck Converter, the high-side MOSFET is placed in parallel with the resonant capacitor. From the previous section, the resonant capacitor is calculated to experience a maximum voltage of about 30 V and the resonant inductor is expected to experience a maximum current of about 20 A. When deciding on a MOSFET, important parameters to concentrate on are drain-to-source break down voltage, threshold voltage, on resistance, maximum drain current, safe operating area curve and the thermal resistances.

During the development of the ZVS-QR Buck Converter, the solution to driving an N-channel MOSFET (NMOS) could not be found. NMOS required a high-side driver which takes from the phase node and add on the voltage from its VCC input. Unfortunately, the phase node in the ZVS-QR Buck Converter could see voltages as high as 40 V – which was the input voltage of 12.0 V plus the maximum voltage across the resonant capacitor of 28.0 V. During the design phase of this proposed converter, there was not a high-side driver that could accept the high voltage of the phase node to charge pump and add its VCC voltage to turn on the NMOS. As a result, the decision to use a P-channel MOSFET (PMOS) was reached. The operation of the PMOS was simple and did

not require a charge pump to turn on the MOSFET. PMOS operation only requires the voltage to either be grounded (ON) or connected to the source pin (OFF). Even though PMOS suffer from higher on-resistance and lack of high-speed capability because of higher junction capacitances like its NMOS counterpart, the ability to have a functional circuit far outweighs the disadvantages.

The PMOS drain-to-source break down voltage only has a rated voltage of 30 V or 60 V. Since a rated voltage of 30 V does not have enough margin from maximum resonant capacitor voltage calculated previously, a rated voltage of 60 V was chosen. The next parameter would be to eliminate the PMOS that cannot handle the current requirements of the proposed converter. Overshoot during the on/off switching of the high-side MOSFET is definitely a possibility if the MOSFET turn on time is very fast. Peak values during the turn-on portion could very easily double the nominal values. For a traditional PWM buck converter, the voltage peaks could be 24 V and current peaks could be 40 A for a very brief moment and possibly induce phase node ringing. MOSFETs with high voltage and current capability tend to have a more forgiving safe operating area curve as well. Safe operating area curves allow the designer to determine if the MOSFET may handle the transient voltage and current spikes that may occur during the switching portion. However, the current capability and the on resistance of the MOSFET are directly proportional. If the current capability increases, then the on resistance increases as well. After some parameter filtering, the PMOS of choice is Vishay SUD50P06-15. It is continuously rated for 60 V and 50 A, but at the same time has very reasonable on-resistance of 15 m Ω at a threshold voltage greater than 10 V. Also, it is pulse rated for 80

A. So reading the safe operating area curve, it can handle 40 A at 40 V for at least 100 μ s – which is perfect because it is much higher than the switching period of 10 μ s.

The PMOS driver to operate the high-side PMOS is the FAN3268T. It is one of the few synchronous PMOS/NMOS drivers on the market with high current drive and high input voltage.

The power loss of a MOSFET is the summation of the conduction losses and the switching losses. The conduction loss is the easiest to calculate using the output current, duty cycle, and $R_{DS(ON)}$.

$$P_{COND} = I_{OUT}^2 \times R_{DS(ON)} \times \frac{V_{OUT}}{V_{IN}} = (20A)^2 (15m\Omega) \left(\frac{1.5V}{12V} \right) = 0.75W \quad (7-13)$$

The switching loss is a little more difficult to calculate because it also requires information from the MOSFET driver and interpreting the graphs within the MOSFET's datasheet. Through examining the Gate Charge graph of the Vishay SUD50P06-15 datasheet, the V_{SP} is estimated to be about 3.7 V and the $Q_{G(SW)}$ is estimated to be about 38 nC. V_{SP} is the V_{GS} voltage where the V_{DS} changes. This is most notable to be the plateau of the Gate Charge graph. $Q_{G(SW)}$ is the switching gate charge measured from the gate charge at V_{TH} to the gate charge at which the V_{GS} ends its plateau. The PMOS driver is the FAN3268T and it has a source current of 2 A and sink current of 1.6 A.

$$R_{Driver (Source)} = \frac{V_{DD} - V_{SP}}{I_{SOURCE}} - R_{GATE} = \frac{12V - 3.7V}{2A} - 1.5\Omega = 2.65\Omega \quad (7-14)$$

$$R_{Driver (Sink)} = \frac{V_{SP}}{I_{SINK}} - R_{GATE} = \frac{3.7V}{1.6A} - 1.5\Omega = 0.813\Omega \quad (7-15)$$

Having the parameters from the PMOS and the high-side driver, the switching loss can be determined as follows:

$$t_{S,Rise} = \frac{Q_{G(SW)}}{I_{SOURCE}} = \frac{38nC}{2A} = 19ns \quad (7-16)$$

$$t_{S,Fall} = \frac{Q_{G(SW)}}{I_{SINK}} = \frac{38nC}{1.6A} = 23.8ns \quad (7-17)$$

Since the switching loss only occurs during the transition period of the MOSFET from either an on state to an off state or vice versa, the switching loss equation can be summarized below. Note that the first half of the equation is simply the equation of the area of a triangle because as the V_{DS} falls, the I_D rises and vice versa – which create an overlapping shape of a triangle.

$$P_{SW} = \left(\frac{V_{IN} \times I_{OUT}}{2} \right) (F_{SW}) (t_{S,Rise} + t_{S,Fall}) \quad (7-18)$$

$$P_{SW} = \left(\frac{12V \times 20A}{2} \right) (820kHz) (19ns + 23.8ns) = 4.21W \quad (7-19)$$

However, the switching power loss is only the loss from the MOSFET. There is also the power loss from the MOSFET driver which allows for the MOSFET to operate as a switch. P_{GATE} is the power taken from the MOSFET driver's input voltage supply used to drive the MOSFET's gate. Note that the gate capacitance is not the same as the switching gate capacitance used to determine switching power loss. The power required to charge the MOSFET's gate capacitor is:

$$P_{GATE} = Q_G \times V_{DD} \times F_{SW} = (165nC)(12V)(820kHz) = 1.6W \quad (7-20)$$

However, the power to charge the gate is not the same as the power loss of the MOSFET driver. The power loss of the MOSFET driver takes into account the total resistance from the MOSFET driver's input voltage supply to the MOSFET's gate capacitor – which is the resistance of the driver, the damping resistance, and the gate resistance.

$$R_{TOTAL,Source} = R_{DRIVER (SOURCE)} + R_{DAMPING} + R_{GATE} \quad (7-21)$$

$$R_{TOTAL,Source} = 2.65\Omega + 0\Omega + 1.5\Omega = 4.15\Omega \quad (7-22)$$

$$R_{TOTAL,Sink} = R_{DRIVER (SINK)} + R_{DAMPING} + R_{GATE} \quad (7-23)$$

$$R_{TOTAL,Sink} = 0.8125\Omega + 0\Omega + 1.5\Omega = 2.3125\Omega \quad (7-24)$$

The power loss of the driver to turn on the PMOS is:

$$P_{DRIVER,SOURCE} = \frac{P_{GATE} \times R_{DRIVER (SOURCE)}}{2(R_{TOTAL,Source})} \quad (7-25)$$

$$P_{DRIVER,SOURCE} = \frac{(1.6W)(2.65\Omega)}{2(4.15\Omega)} = 0.511W \quad (7-26)$$

The power loss of the driver to turn of the PMOS is:

$$P_{DRIVER,SINK} = \frac{P_{GATE} \times R_{DRIVER (SINK)}}{2(R_{TOTAL,Sink})} \quad (7-27)$$

$$P_{DRIVER,SINK} = \frac{(1.6W)(0.8125\Omega)}{2(2.3125\Omega)} = 0.281W \quad (7-28)$$

$$P_{DRIVER} = P_{DRIVER,SOURCE} + P_{DRIVER,SINK} \quad (7-29)$$

$$P_{DRIVER} = 0.5108W + 0.2811W = 0.792W \quad (7-30)$$

Still, the MOSFET does not only have a gate-source capacitance, but it also has a drain-source capacitance and drain-gate capacitance – which creates the MOSFET output capacitance (C_{OSS}). The power required to charge the MOSFET output capacitance is very minimal, but it is calculated with the following equation:

$$P_{COSS} = \frac{C_{OSS} \times V_{IN}^2 \times F_{SW}}{2} \quad (7-31)$$

$$P_{COSS} = \frac{(480pF)(12V)^2(820kHz)}{2} = 4.723mW \quad (7-32)$$

The total power loss of the building blocks used to operate the PMOS as a switch is:

$$P_{TOTAL} = P_{DRIVER} + P_{MOSFET} \quad (7-33)$$

$$P_{TOTAL} = (P_{DRIVER} + P_{GATE}) + (P_{COND} + P_{SW} + P_{COSS}) \quad (7-34)$$

$$P_{TOTAL} = 0.7919W + 1.6W + 0.75W + 4.21W + 0.004W \quad (7-35)$$

$$P_{TOTAL} = 7.357W \quad (7-36)$$

From the total power loss equation above, the switching loss account for over half of the total power loss in the PMOS. As a result, it is the Two Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter's purpose to attempt to eliminate the switching power loss from the equation.

7.3 Freewheeling Diode

The freewheeling diode selection is also similar to that of the high-side MOSFET, but few parameters are scrutinized. When deciding on a freewheeling diode, the important parameters to examine are the peak repetitive reverse voltage, average and peak rectified forward current, and maximum instantaneous forward voltage. Unfortunately with high power diodes, the diodes only come in a rectifier configuration, so the rated current at the top of datasheets are for both diodes. If only one diode is used, then the rated current per device must be divided in half to have a per diode rating. Since, the high-side MOSFET see about the same voltage stress as the freewheeling diode, then the 60 V rated voltage will be used. For continuous current, the rated current of 30 A should be enough since the 30 A is already 50% higher than the expected 20 A per phase of the proposed converter. The power dissipation will be heavily reliant on the forward voltage drop when the diode is conducting. Since the diode is a high powered diode, the goal should be to keep the forward voltage drop below 1.0 V. The chosen diode is ON Semiconductor MBRB60H100CTT4G. It has a rated voltage of 100 V, rated continuous current of 30 A

per diode, and a forward voltage drop of approximately 0.8 V. It is an added benefit that it can sustain peak repetitive forward current of upwards of 60 A.

7.4 Zero-Voltage-Switching Quasi-Resonant Buck Converter Timing Parameters

With the circuit specifications and the resonant component values determined, time t_1 , t_2 , t_3 can be found in order to calculate the constant turn-off time during the switching cycle for the zero-voltage-switching quasi-resonant buck converter as previously discussed. If a zero-current-switching quasi-resonant buck converter is used, then the turn-on time is instead set constant.

$$t_1 = 1.08\mu s \quad (7-37)$$

$$t_2 = 6.55\mu s \quad (7-38)$$

$$t_3 = 9.21\mu s \quad (7-39)$$

As a result, the constant turn-off time for this zero-voltage-switching buck converter is 6.55 μ s. Due to the constant turn-off time for the switch, the pulse width modulating (PWM) switching method cannot be used, but instead a pulse frequency modulation (PFM) switching method is required. The PFM switching method with a constant turn-off time will result in a varying duty cycle and switching frequency. Due to the lack of a set switching frequency, it is the reason the design did not start with determining the duty cycle of the buck converter.

7.5 Output Inductor and Capacitor

With the resonant tank circuit and timing parameters calculated, the two-phase buck converter capacitors (C_f) and inductors (L_f) need to be determined as follows – assuming

a duty cycle of 0.345, which is calculated from the time on divided by switching period since the time off is permanently defined above.

$$L_c = \frac{(1-0.345)}{2 \times 100\text{kHz}} \times \frac{1.5V}{4A/2} = 2.46\mu H \quad (7-40)$$

$$C \geq \frac{(1-D)}{\frac{\Delta V}{V_o} \cdot 8 \cdot L \cdot f_s^2} = \frac{(1-0.345)}{(0.01)(8)(3.3\mu H)(100\text{kHz})^2} = 248.106\mu F \quad (7-41)$$

Typically, the critical inductance (L_c) is multiplied by a value in the range of 1.1 to 2 to reduce the output current ripple, and the output capacitor is chosen to have a capacitance higher than the calculated capacitance to reduce the output voltage ripple. The low pass filter inductor is chosen to be 3.3 μ H due to its abundance in supply and current ratings. The low pass filter capacitor is chosen to be 470 μ F since this value is greater than the calculated value. Two of this capacitor will be used in parallel for lowering the ESR for improved efficiency while increasing the capacitance value to reduce the output voltage ripple. The calculated components above allow for one of the two-phase zero-voltage-switching quasi-resonant buck converters to be built, the other phase is an identical converter. The two converters are then paralleled together to operate in an interleaved fashion.

Table 7-1: Summary of Component Selections for the Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter

Parameter	Component Size
Resonant Inductance	1.0 μ H
Resonant Capacitance	1.8 μ F
Critical Inductance	3.3 μ H
Input Capacitance	470 μ F
Output Capacitance	470 μ F
High-Side MOSFET Voltage	60 VDC
High-Side MOSFET Current	50 ADC
Freewheeling Diode Voltage	60 VDC

Freewheeling Diode Current	30 ADC
Top Resistor of Feedback Ladder	10 k Ω
Bottom Resistor of Feedback Ladder	15 k Ω

8. Functionality Simulation

The simulation of the two-phase zero-voltage-switching quasi-resonant buck converter was completed in OrCAD PSpice to confirm the functionality of the circuit. Table 8-1 shows the summary of the circuit parameters from Chapter 7, and Figure 8-1 illustrates the circuit layout simulated in OrCAD PSpice. The load resistor is chosen to produce an output current of 40 ADC which represents the full load. The inherent benefit of a multiphase converter is the output voltage and current waveforms have ripple at a frequency of n times the switching frequency. In the simulation, a switching frequency of 93 kHz as can be seen in the ripple current of L_{f1} and L_{f2} in Figure 8-2 was used to obtain the proper output voltage and current. The inductor peak to peak ripple current is shown to be about 6 A. In addition, Figure 8-2 also shows how output current is being equally shared by the two inductors. It further demonstrates how the actual current will have a frequency double that of the switching frequency. This is evident from Figures 8-3 and 8-4 where the output voltage and current ripple frequencies are measured to be 183 kHz – which is almost twice the switching frequency.

Table 8-1: Circuit Parameters

Parameter	Component Size
Input Voltage	12 VDC
Resonant Inductor	1.0 μ H
Resonant Capacitor	1.8 μ F
Filter Inductor	3.3 μ H
Filter Capacitor	470 μ F
Characteristic Impedance	0.375 Ω
Switching Frequency	100 kHz
Resonant Frequency	118 kHz
Output Voltage	1.5 VDC
Output Current	40 ADC

Figure 8-5 illustrates the simulated waveforms of the resonant components to allow for a comparison to the mathematical waveforms in Figure 3-2. As expected, the resonant capacitor voltage starts to increase linearly until resonant mode is hit, causing voltage to follow sinusoidal shape. This voltage naturally goes to zero and stays at zero since the diode across the capacitor begins to conduct. Soon after resonant capacitor voltage reaches zero, the switch can now be turned on with zero voltage producing the soft-switching transition. The resonant inductor current on the other hand starts from output current until resonance occurs after which the resonant inductor current waveform decreases. The resonant inductor current continue to go below zero before it naturally swings upward following sinusoidal shape and eventually stops at its initial condition of the load current.

As previously mentioned, the benefit of this topology is not only its inherent ripple frequency multiplication effect, but also in its ability to nullify switching losses. Figure 8-6 shows one phase of the topology's switching signal and switch voltage to demonstrate the switch turning on and off at zero volts to avoid switching losses. As an extension of Figure 8-6, the phase delay of $360^\circ/n$ is shown in Figure 8-7 with the switching signal and switch voltage. With a reduction of the switching losses, the overall efficiency is increased over that of the traditional buck converter.

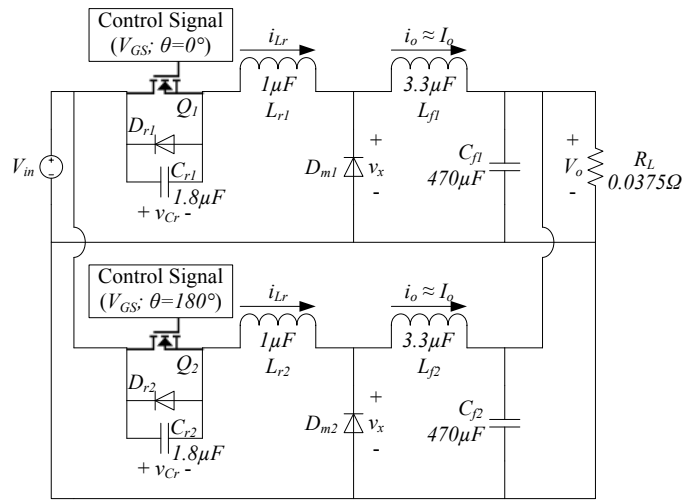


Figure 8-1: Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter

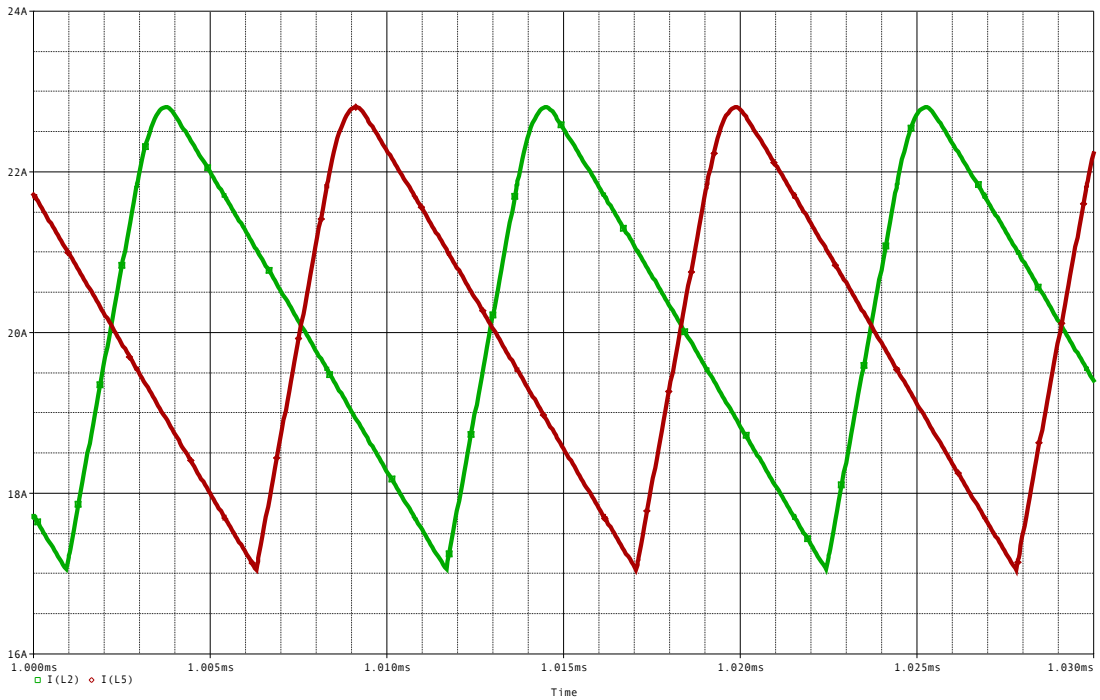


Figure 8-2: Waveforms of output filter inductor current i_{f1} and output filter inductor current i_{f2}

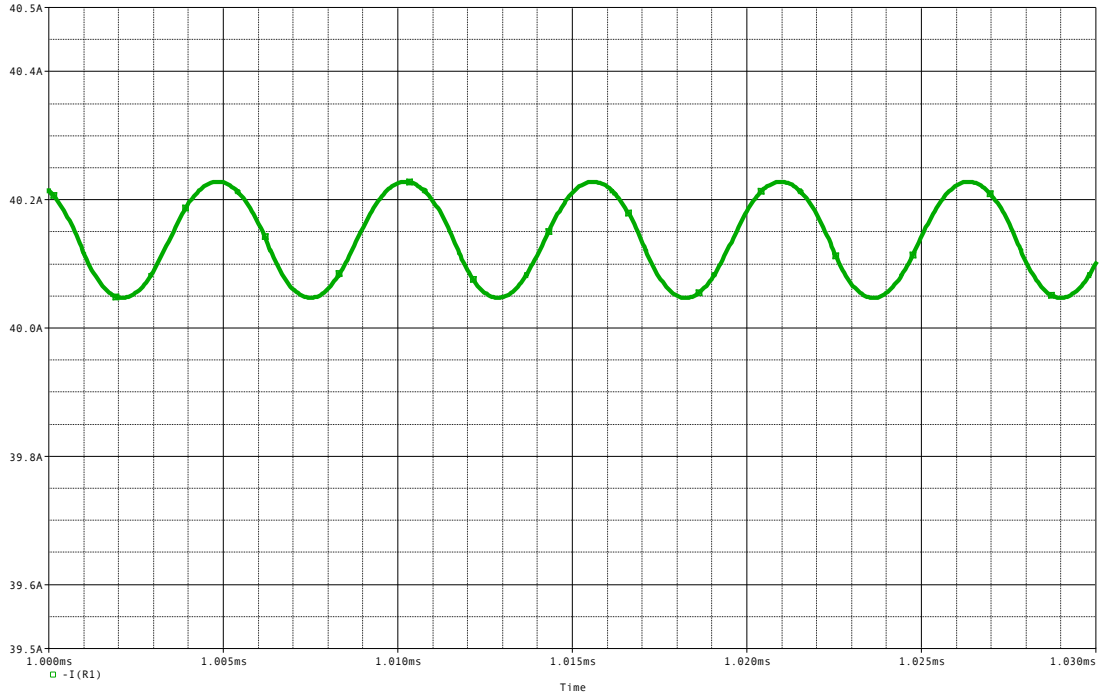


Figure 8-3: Waveform of output load current ripple i_{RL}

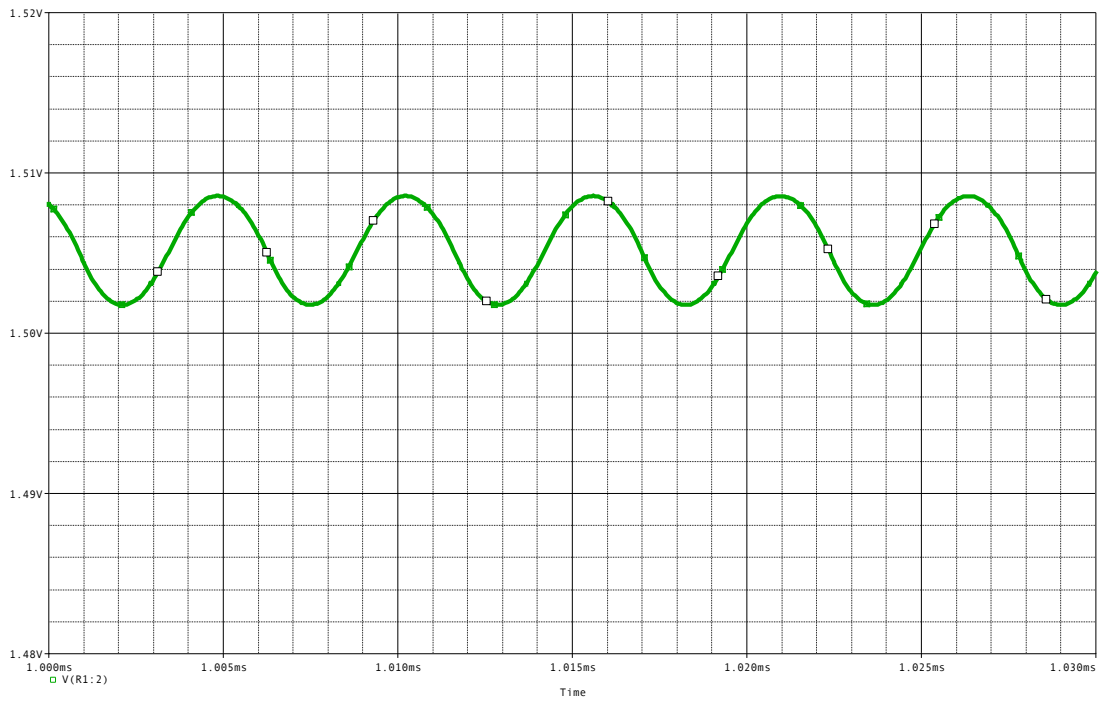


Figure 8-4: Waveform of output voltage waveform v_{RL}

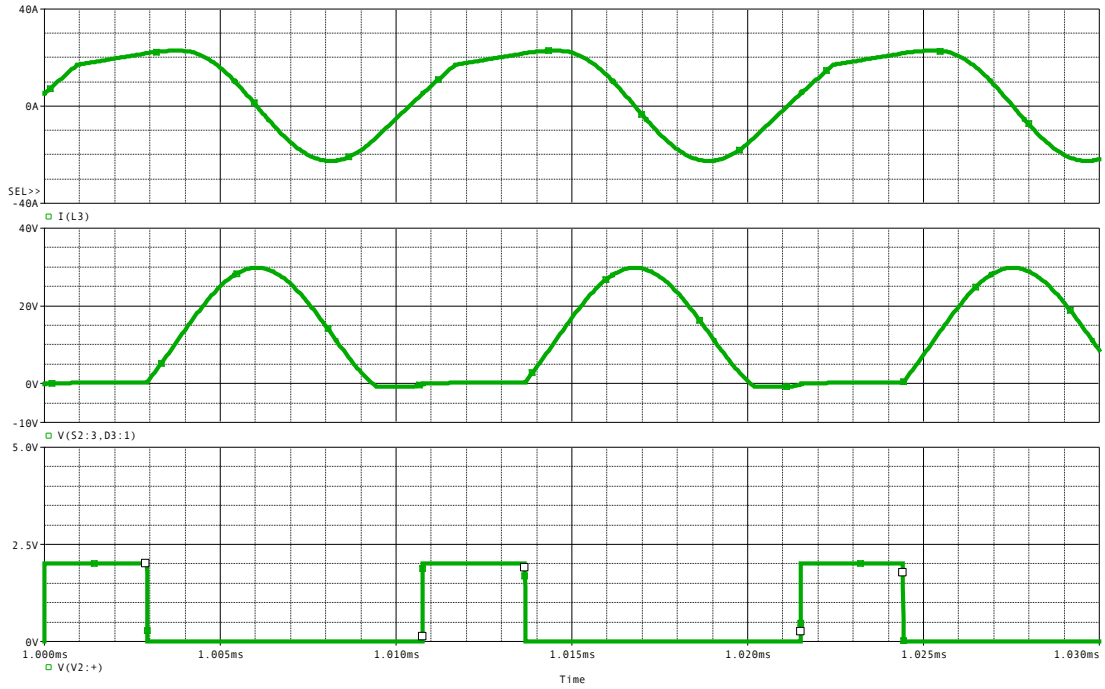


Figure 8-5: Waveform of the resonant current i_{Lr1} (top), the resonant voltage v_{Cr1} (middle), and switching signal V_{GS1} (bottom)

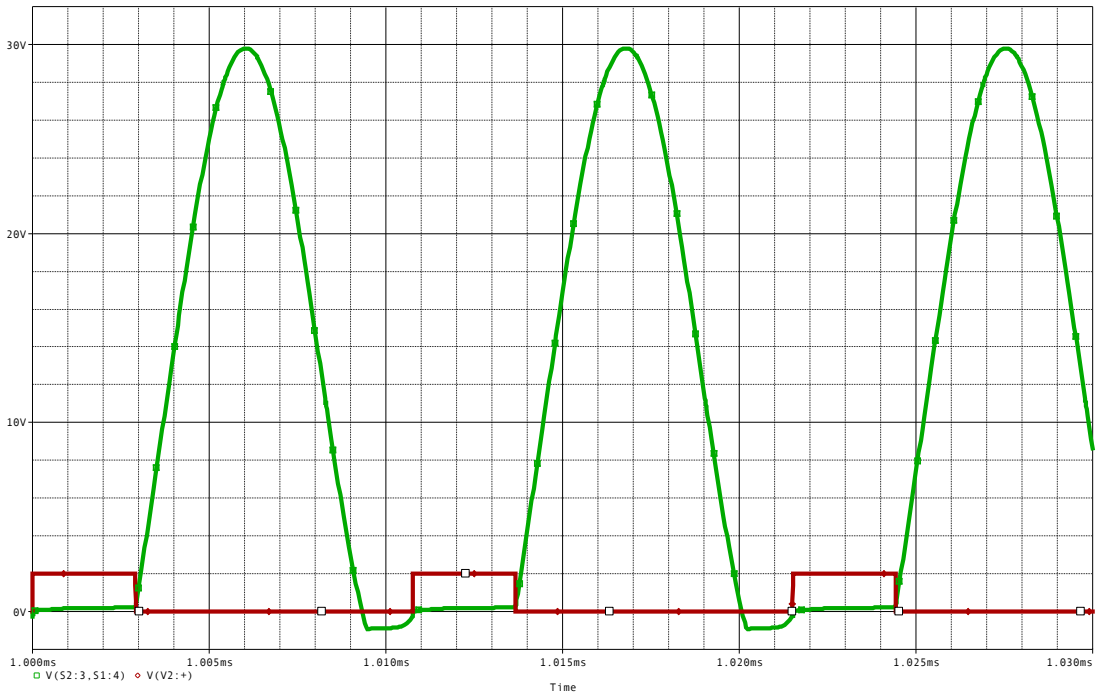


Figure 8-6: Waveform of switching signal V_{GS1} and switch voltage V_{DS1}

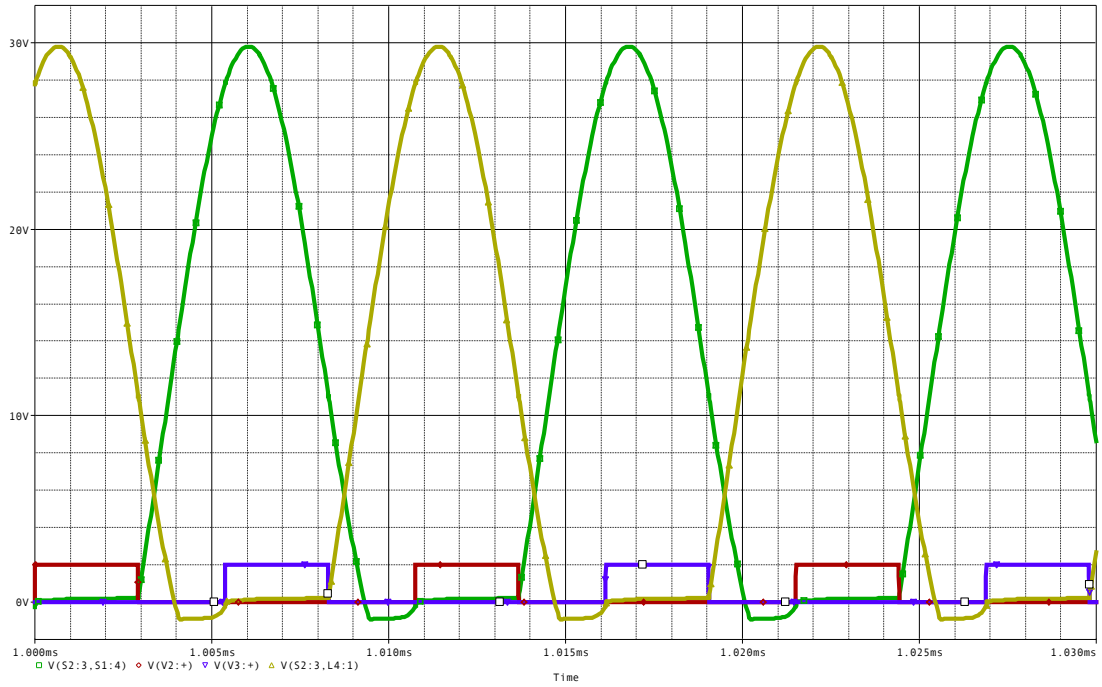


Figure 8-7: Waveform of switching signal V_{GS1} and V_{GS2} and switch voltage V_{DS1} and V_{DS2}

9. Hardware Implimentation and Results

When creating design prototypes, the first thought is to use a breadboard or prototype board. Unfortunately, the breadboard or prototype board makes it difficult to use surface mount components and have good PCB layout practices. As an example for a power converter, the ground plane is usually used as a heat sink for the MOSFETs. There is not much of a ground plane for a breadboard or prototype board. Thus, for the best performance and layout practices, a customized 4-layer board is used from ExpressPCB. The top layer has the majority of all the PCB traces. The second layer is the ground layer so as to have an isolation layer from the third layer, which is the power layer that has the 5.0V and 12.0V rails. The bottom layer has the gate signal from the Microchip dsPIC30F2020 and any other traces that cannot be physically routed on the top layer without intersecting.

9.1 Digital Microcontroller

The digital microcontroller must be able to create multiple PWM and PFM signals for the traditional PWM buck converter and the Zero-Voltage-Switching Quasi-Resonant Buck Converter, respectively. In addition, the digital microcontroller must be able to sample the output voltage and have an ADC to convert the output voltage for the microcontroller to use its DSP to adjust the gate signal to maintain the desired output voltage. The microcontroller that meets the two criteria is the Microchip dsPIC30F2020. It has up to four PWM outputs and an internal ADC that is able to use PID control to adjust the PWM signal to the MOSFET.

The dsPIC30F2020 is a DIP package because the development programmer board is only available for DIP packages. The dsPIC30F2020 requires a 5.0V VCC rail, so a LDO

is used to convert the 12.0V input voltage to 5.0V. The LDO of choice is Texas Instruments LM338.

The dsPIC30F2020 has multiple registers that adjust the configuration output, the duty cycle, and the period of the PWM signal. It is thoroughly explained in its datasheet [10]. However, the availability of sample codes made the most difference in understanding the operation of the dsPIC30F2020. The codes for the dual phase PWM and dual phase PFM operation with PID control are included in the Appendix.

9.2 Hardware Results and Analysis

The design of the PCB is to incorporate all the building blocks to create the final solution. The user simply needs to have an input voltage of 12.0 V and the board will complete the power conversion to generate 1.5 V at the output terminals able to supply up to 40 A given that there is ample input supply current from the power supply.

All the plots and calculations are done at full load of 40 A, unless otherwise stated. During full load, the power converter is operating at an input of 12.0 V and an output of 1.5 V and 40 A. Oscilloscope screen captures were taken at full load using an electronic load set to draw a steady 40A.

The efficiency graphs were generated from python automated data acquisition software based off of GPIB protocol built into each of the power supplies, multi-meters, electronic loads, and oscilloscope. This creates the most reproducible and reliable data.

Throughout this section, phase 1 and phase 2 will be often mentioned, but the names are arbitrary notations to distinguish the data of the two phases in the power converters. The names do not have any significant bearing on the functionality or performance of the

circuit. For consistency and accuracy, phase 1 and phase 2 will always represent the same current flow portion of the PCB through the analysis.

9.2.1 Output Voltage Ripple

Figure 9-1 presents the output voltage ripple under the full load condition of 40A. The peak-to-peak ripple is measured by the oscilloscope to be 34.0 mV or 2.27% with an output voltage of 1.5 V.

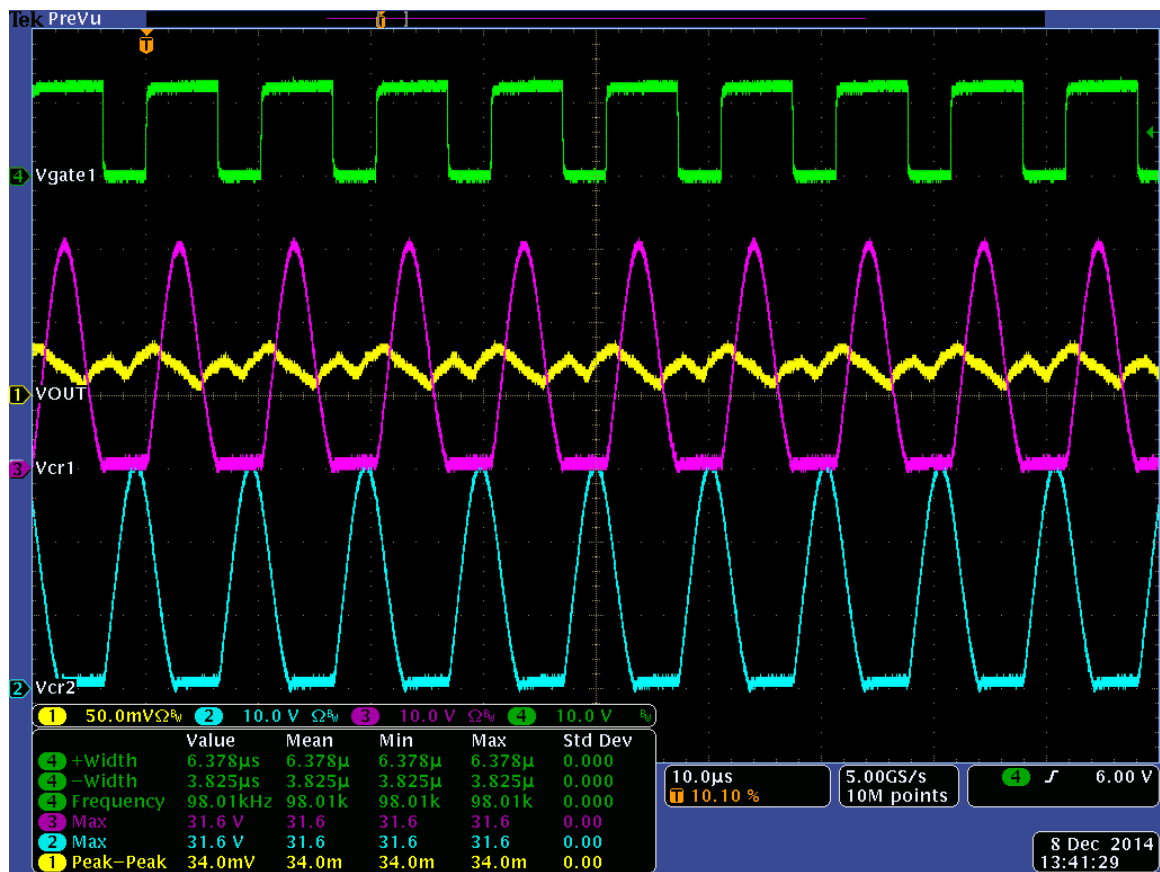


Figure 9-1: Output Voltage Ripple of Dual Phase Zero-Voltage-Switching Quasi Resonant Buck Converter at 100kHz

Comparing this to the design requirement of less than 1% of output voltage ripple, the converter is performing outside of its design requirements. There are only three main methods to reducing output voltage ripple: more output capacitance, higher output inductor, or higher switching frequency. The output capacitance is already at a very high

value of eight electrolytic capacitors at 2200 μ F each for a total output capacitance of 17,600 μ F. The output inductance is already chosen to have a safe DC current rating. As the inductance increases, the DC current rating of the inductor decreases. This only leaves the option of increasing the switching frequency to reduce the output voltage peak-to-peak ripple.

9.2.2 Switching Signal

In order to drive the MOSFET, the dsPIC30F2020 has its PWMxH output sends a gate signal to the PMOS driver (FAN3268T), which in turns sources and sinks the current necessary to drive the PMOS. The signal shown on the oscilloscope capture is taken at the PMOS, but its operation is inverted from the NMOS. Thus, if the signal is high, then the PMOS is off and vice versa. The gate signal has a constant off time (high value) with a varying on time (low value) because it is acting as a constant off time PFM modulator. The gate signal was initially programmed with the constant off time of the value calculated as t_2 in Chapter 7. However, the gate signal was modified to minimize the time between the voltage across the resonant capacitor (V_{Cr}) was at zero volts and the turn on portion of the PMOS. Thus, the constant off time values will be different than that calculated in Chapter 7.

Analyzing the code provided in the Appendix, the code takes phase 1's period of the switching frequency and divides it in half. The value is then used to time shift phase 2's period by that amount. This effectively phase shifts the gate signal of phase 1 and phase 2 by 180°.

It can be seen from the measurements of the oscilloscope in Figure 9-2 that phase 2's frequency (channel 4 – green) is almost the desired value of 100 kHz. Examining phase

1's frequency (channel 1 – yellow) it has almost the same switching frequency and duty cycle. The phase shifting is not exactly 180° , but it is phase shifted according to the algorithm in the code. Due to imperfect the phase shifting of 180° , the effective switching frequency may not be exactly doubled as expected.

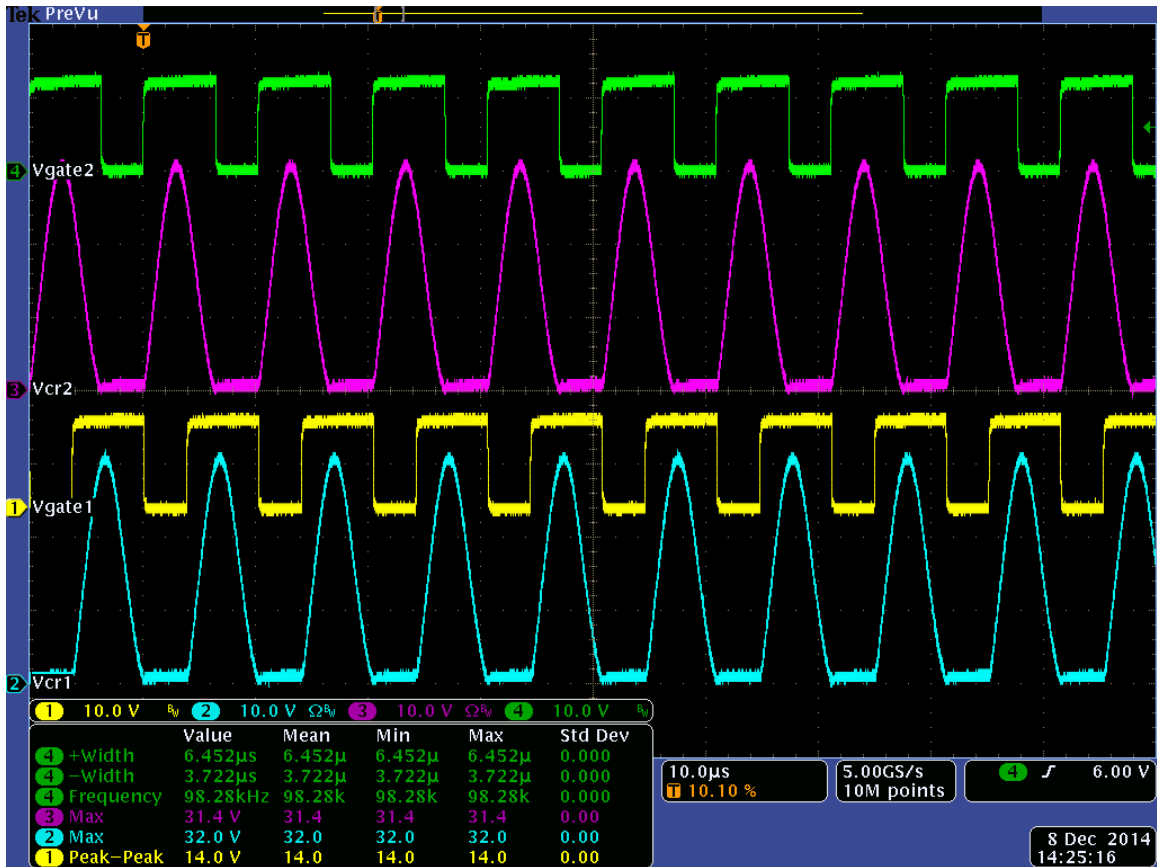


Figure 9-2: Gate Signal Comparison of Dual Phase Zero-Voltage-Switching Quasi Resonant Buck Converter at 100kHz

9.2.3 Switching Waveforms of Phase 1 and Phase 2

Figures 9-3 and 9-4 illustrate the gate signal, resonant capacitor, resonant inductor, and output voltage waveforms of phase 1 and phase 2, respectively, in an operational Two-Phase Zero-Voltage-Switching Quasi Resonant Buck Converter. It can be seen the resonant capacitor's voltage only rises above zero during the off time of the PMOS. And at the points the PMOS turns on and off, the voltage across the resonant capacitor – and PMOS – is at zero to create the zero-voltage-switching effect. The freewheeling diode is

shown to be conducting during the off time of the PMOS with its voltage near 0 V with the blue waveform at channel 2. The PMOS turns off and the voltage across the freewheeling diode slowly decreases to 0 V and remains there until the PMOS turns on. At that point in time, the voltage across the freewheeling diode will increase to the same value as the input voltage of 12 V. This mimics the exact behavior derived in Chapter 3.

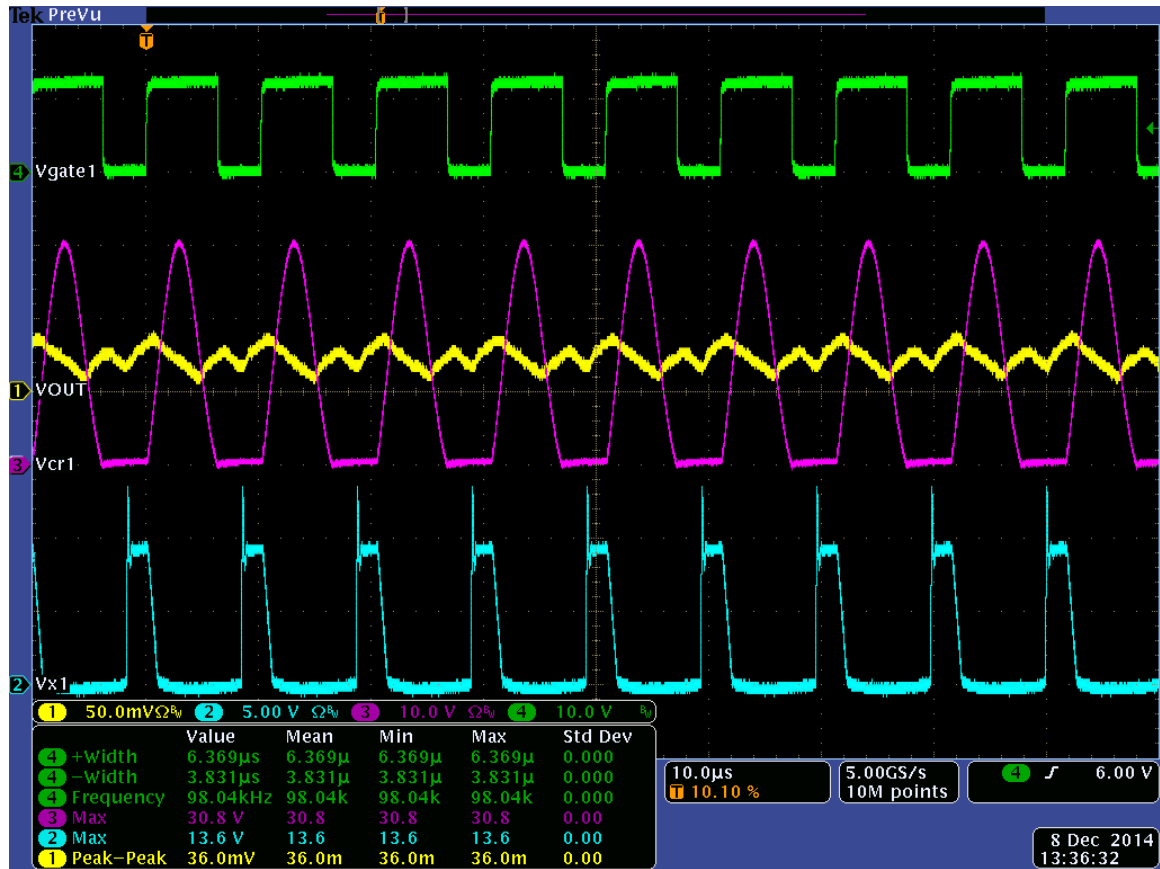


Figure 9-3: Phase 1 Waveform of Dual Phase Zero-Voltage-Switching Quasi Resonant Buck Converter at 100kHz

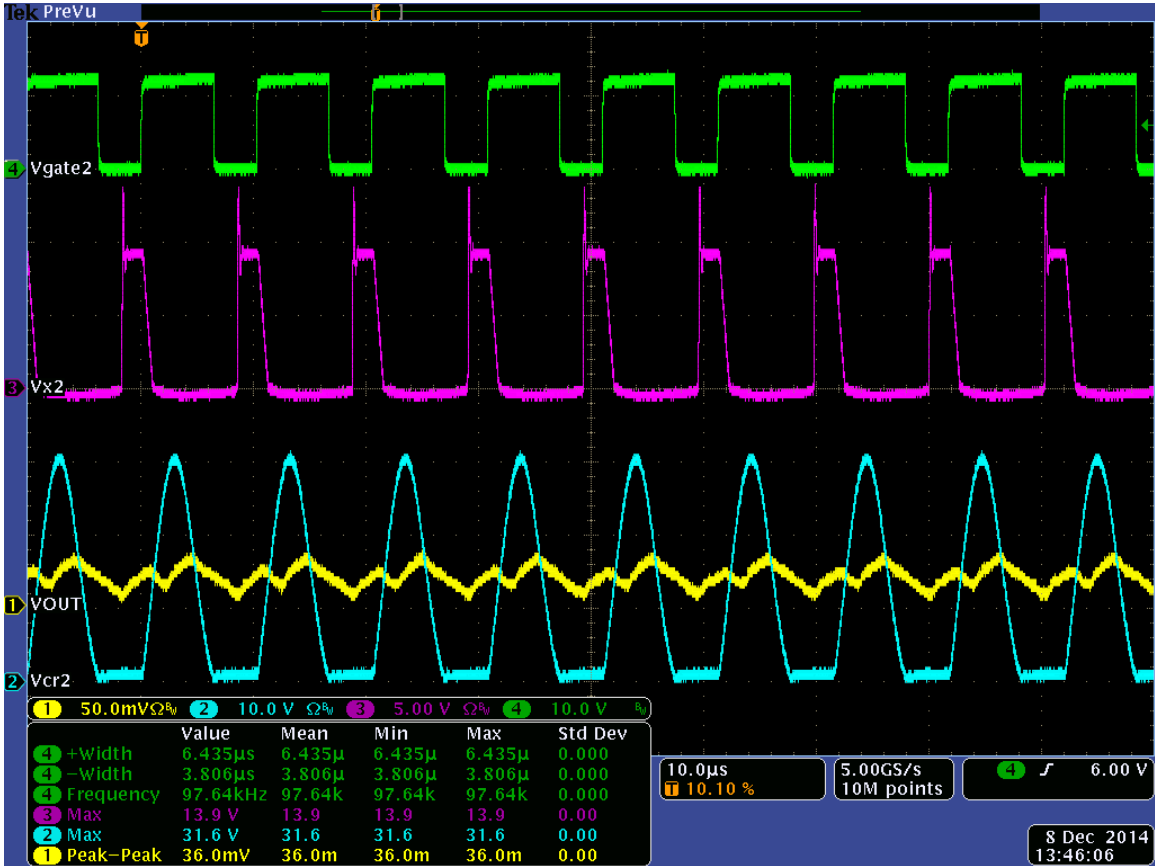


Figure 9-4: Phase 2 Waveforms of Dual Phase Zero-Voltage-Switching Quasi Resonant Buck Converter at 100kHz

9.2.4 Efficiency of Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter at 100kHz

The Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter at 100 kHz has a peak efficiency of 55.80% at 30A with an efficiency of 54.0% at full load of 40 A. This is much lower than the design requirements stated in Chapter 4 of greater than 85%. The efficiency is lower than expected because of the high current of the design. The basis of the Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter is using resonance, but that involves sinusoidal waves. This results in higher peak numbers, such as current. With higher peak numbers and more area under the curve, it results in more power loss. Also, the calculations do not take into the non-ideal and parasitic components in both the components and on the PCB. Table 9-1 lists the efficiency data

for the Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter from 13 A to 40 A. Figure 9-5 shows a graphical representation of the efficiency data from Table 9-1. It will be explained later why the output current does not maintain regulation at near no load conditions.

$$\text{Peak Efficiency} = 55.800\% @ 30A \quad (9-1)$$

$$\text{Max Load Efficiency} = 54.000\% @ 40A \quad (9-2)$$

Table 9-1: Efficiency Data for Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter at 100kHz

Load Current (A)	DMM Output Voltage (V)	DMM Input Voltage (V)	Input Current (A)	Efficiency (%)
13.008	1.524	11.987	3.952	41.843
14.004	1.522	11.987	4.029	44.133
15.008	1.520	11.987	4.109	46.303
16.008	1.518	11.987	4.214	48.109
17.008	1.517	11.987	4.333	49.672
18.008	1.515	11.987	4.465	50.974
19.008	1.515	11.987	4.600	52.243
20.008	1.515	11.987	4.755	53.179
21.008	1.512	11.987	4.924	53.830
22.008	1.513	11.987	5.113	54.315
23.008	1.512	11.987	5.308	54.667
24.008	1.511	11.987	5.516	54.845
25.008	1.510	11.987	5.704	55.216
26.008	1.509	11.987	5.918	55.309
27.008	1.509	11.987	6.097	55.756
28.008	1.510	11.987	6.344	55.601
29.012	1.508	11.987	6.564	55.610
30.012	1.507	11.987	6.762	55.798
31.012	1.507	11.987	6.998	55.719
32.012	1.505	11.987	7.247	55.463
33.012	1.506	11.987	7.474	55.498
34.012	1.505	11.987	7.733	55.222
35.012	1.505	11.987	7.975	55.131
36.012	1.503	11.987	8.224	54.911

37.012	1.501	11.987	8.504	54.510
38.012	1.502	11.987	8.754	54.400
39.012	1.502	11.987	9.017	54.214
40.016	1.502	11.987	9.283	54.003

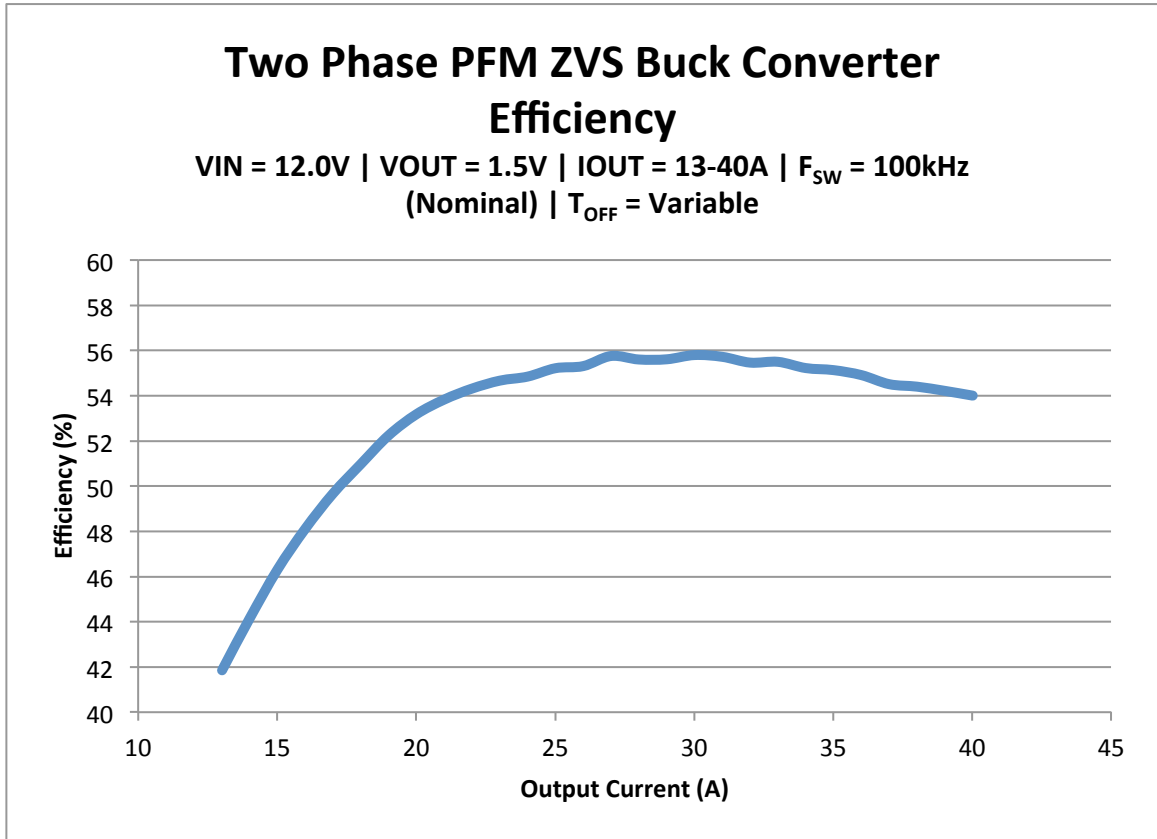


Figure 9-5: Efficiency Graph of Two Phase Zero-Voltage-Switching Quasi Resonant Buck Converter at 100kHz

9.2.5 Load Regulation of Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter at 100kHz

Since the minimum possible load current for the Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter is only 13 A, then the load regulation will be calculated with a minimum load current of 13 A instead of the typical no load condition of 0 A. Table 9-2 lists the load regulation data for the Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter from 13 A to 40 A. Figure 9-6 shows a graphical representation of the load regulation data from Table 9-2. The load regulation is slightly more than the design requirement of under 1%.

$$\text{Load Regulation} = \left| \frac{V_{I\max} - V_{I\min}}{V_{I\max}} \right| \times 100 \quad (9-3)$$

$$\text{Load Regulation} = \left| \frac{1.502V - 1.524V}{1.502V} \right| \times 100 = 1.464\% \quad (9-4)$$

Table 9-2: Load Regulation Data for Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter at 100kHz

Load Current (A)	DMM Output Voltage (V)
13.008	1.524
14.004	1.522
15.008	1.520
16.008	1.518
17.008	1.517
18.008	1.515
19.008	1.515
20.008	1.515
21.008	1.512
22.008	1.513
23.008	1.512
24.008	1.511
25.008	1.510
26.008	1.509
27.008	1.509
28.008	1.510
29.012	1.508
30.012	1.507
31.012	1.507
32.012	1.505
33.012	1.506
34.012	1.505
35.012	1.505
36.012	1.503
37.012	1.501
38.012	1.502
39.012	1.502
40.016	1.502

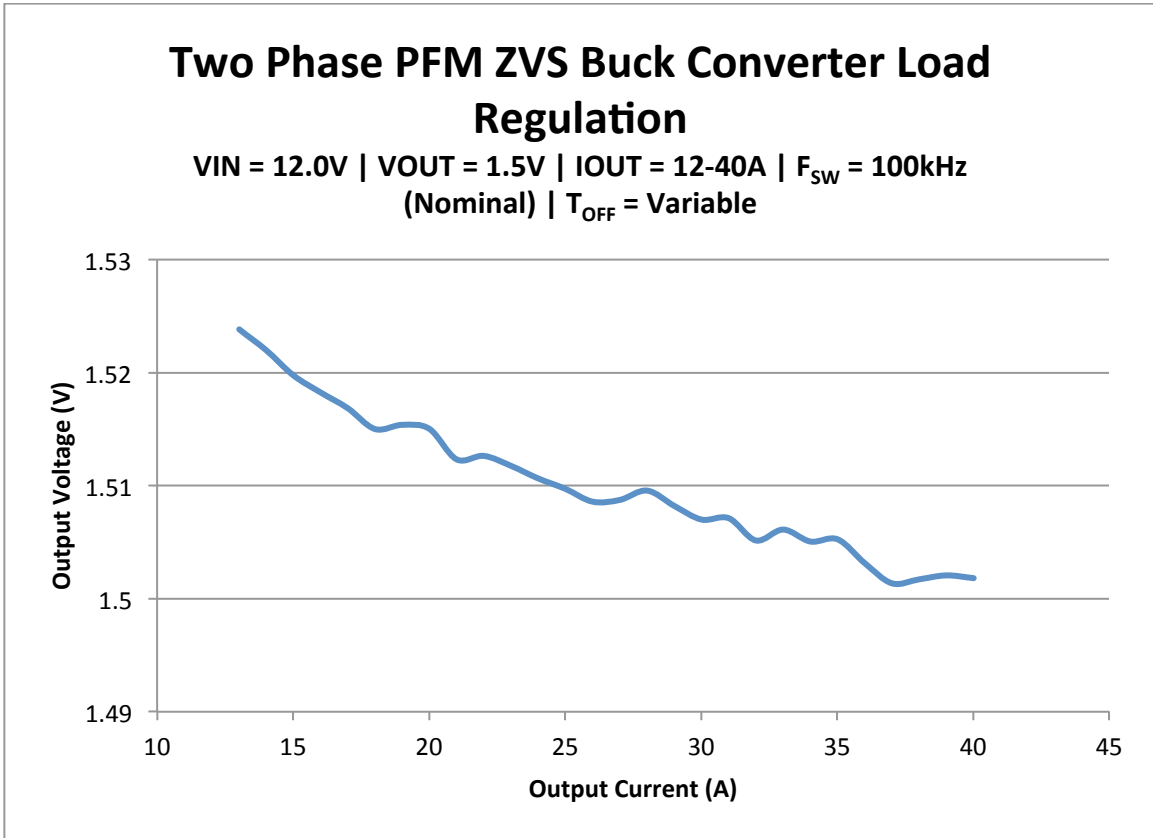


Figure 9-6: Load Regulation Graph of Two Phase Zero-Voltage-Switching Quasi Resonant Buck Converter at 100kHz

9.2.6 Line Regulation of Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter at 100kHz

Similar to the load regulation, the line regulation will be calculated with a minimum load current of 13A instead of the typical no load condition of 0A. Table 9-3 lists the line regulation data for the Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter from 10.8V to 13.2V. The line regulation is measured +10% and -10% from the nominal voltage of 12.0V, which results in 13.2V and 10.8V – respectively. Figure 9-7 shows a graphical representation of the load regulation data from Table 9-3. Unlike the efficiency and load regulation, the line regulation was well under the design requirement of 1%.

$$\text{Line Regulation} = \left| \frac{V_{Vmax} - V_{Vmin}}{V_{Vmax}} \right| \times 100 \quad (9-5)$$

$$\text{Line Regulation} = \left| \frac{1.501V - 1.502V}{1.501V} \right| \times 100 = 0.075\% \quad (9-6)$$

Table 9-3: Line Regulation Data for Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter at 100kHz

Load Current (A)	DMM Output Voltage (V)	DMM Input Voltage (V)	Input Current (A)	Efficiency (%)
40.012	1.502	13.186	8.496	53.638
40.012	1.502	12.987	8.611	53.740
40.012	1.501	12.787	8.741	53.721
40.012	1.503	12.587	8.865	53.897
40.012	1.501	12.387	8.995	53.917
40.012	1.502	12.187	9.144	53.915
40.012	1.502	11.987	9.277	54.045
40.012	1.501	11.788	9.398	54.205
40.004	1.501	11.588	9.657	53.652
40.008	1.500	11.388	9.808	53.719
40.008	1.501	11.188	9.955	53.913
40.008	1.501	10.988	10.111	54.038
40.008	1.501	10.666	10.298	54.665

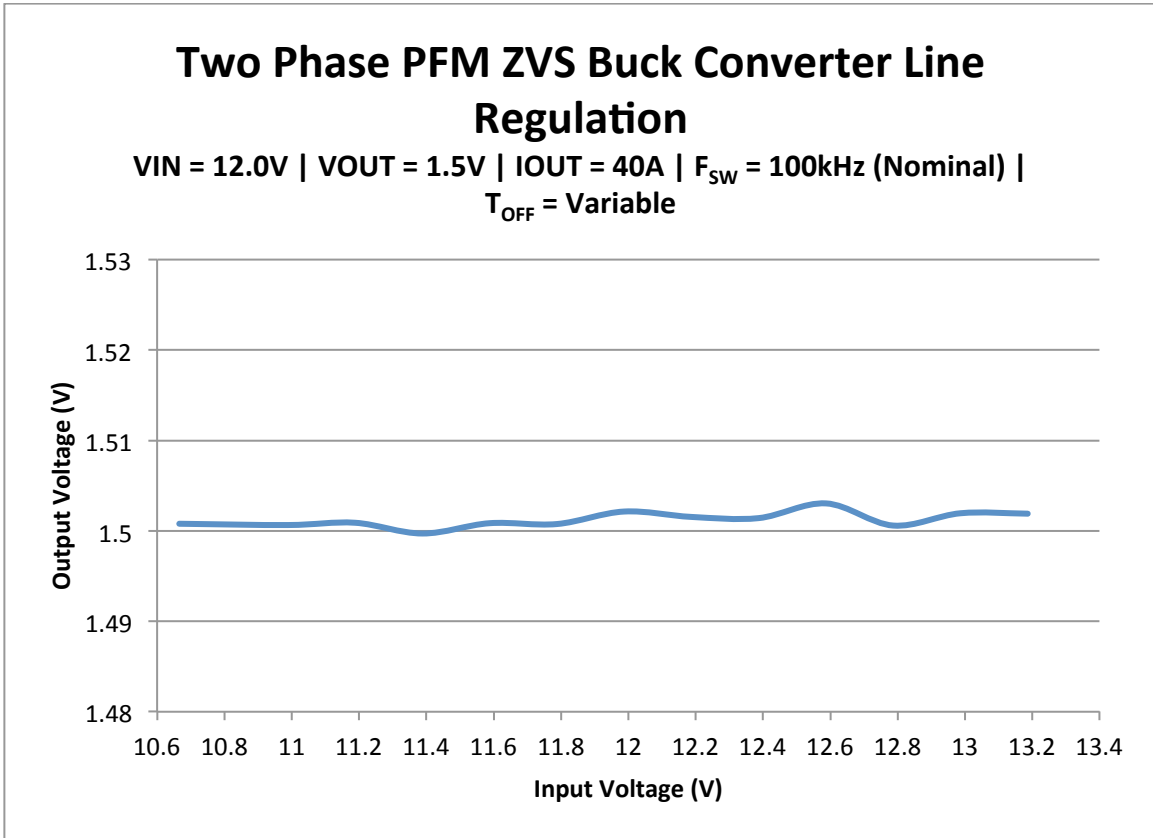


Figure 9-7: Line Regulation Graph of Dual Phase Zero-Voltage-Switching Quasi Resonant Buck Converter at 100kHz

9.2.7 Efficiency of Two-Phase PWM Buck Converter at 100kHz

For a comparison, the exact components were used for a PWM control algorithm to show any efficiency differences between the two topologies. The Two-Phase PWM Buck Converter at 100 kHz has a peak efficiency of 65.21% at 19A with an efficiency of 63.55% at full load of 40A. This is higher than the Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter. Table 9-4 lists the efficiency data for the Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter from 0A to 40A. Figure 9-8 shows a graphical representation of the efficiency data from Table 9-4.

$$\text{Peak Efficiency} = 65.21\% @ 19A \quad (9-7)$$

$$\text{Max Load Efficiency} = 63.55\% @ 40A \quad (9-8)$$

Table 9-4: Efficiency Data for Two-Phase PWM Buck Converter at 100kHz

Load Current (A)	DMM Output Voltage (V)	DMM Input Voltage (V)	Input Current (A)	Efficiency (%)
0.048	1.492	11.987	0.187	3.190
0.114	1.495	11.987	0.206	6.908
0.206	1.497	11.987	0.227	11.319
0.304	1.498	11.987	0.247	15.380
0.404	1.500	11.987	0.265	19.053
0.502	1.499	11.987	0.283	22.160
0.602	1.498	11.987	0.301	24.980
0.704	1.498	11.987	0.319	27.591
0.804	1.499	11.987	0.336	29.875
0.902	1.499	11.987	0.354	31.855
1.004	1.499	11.987	0.372	33.774
2.004	1.501	11.987	0.548	45.828
3.004	1.501	11.987	0.723	52.064
4.004	1.500	11.987	0.898	55.785
5.004	1.496	11.987	1.072	58.240
6.004	1.496	11.987	1.246	60.137
7.000	1.498	11.987	1.421	61.565
8.004	1.498	11.987	1.598	62.589
9.004	1.497	11.987	1.776	63.312
10.004	1.497	11.987	1.957	63.838
11.004	1.497	11.987	2.140	64.240
12.004	1.497	11.987	2.323	64.548
13.004	1.496	11.987	2.508	64.702
14.004	1.497	11.987	2.695	64.884
15.004	1.497	11.987	2.884	64.988
16.004	1.497	11.987	3.072	65.072
17.004	1.498	11.987	3.263	65.141
18.004	1.499	11.987	3.454	65.175
19.004	1.499	11.987	3.645	65.206
20.004	1.499	11.987	3.837	65.197
21.004	1.499	11.987	4.028	65.198
22.004	1.499	11.987	4.222	65.170
23.004	1.499	11.987	4.414	65.166
24.004	1.498	11.987	4.608	65.114

25.004	1.499	11.987	4.803	65.087
26.004	1.498	11.987	5.000	64.999
27.004	1.497	11.987	5.194	64.926
28.004	1.497	11.987	5.391	64.861
29.004	1.496	11.987	5.590	64.759
30.004	1.496	11.987	5.788	64.694
31.004	1.496	11.987	5.989	64.612
32.004	1.495	11.987	6.188	64.501
33.004	1.495	11.987	6.391	64.400
34.004	1.494	11.987	6.593	64.298
35.004	1.494	11.987	6.798	64.182
36.004	1.494	11.987	7.002	64.071
37.004	1.493	11.987	7.210	63.939
38.004	1.493	11.987	7.416	63.838
39.004	1.492	11.987	7.627	63.667
40.004	1.493	11.987	7.838	63.551

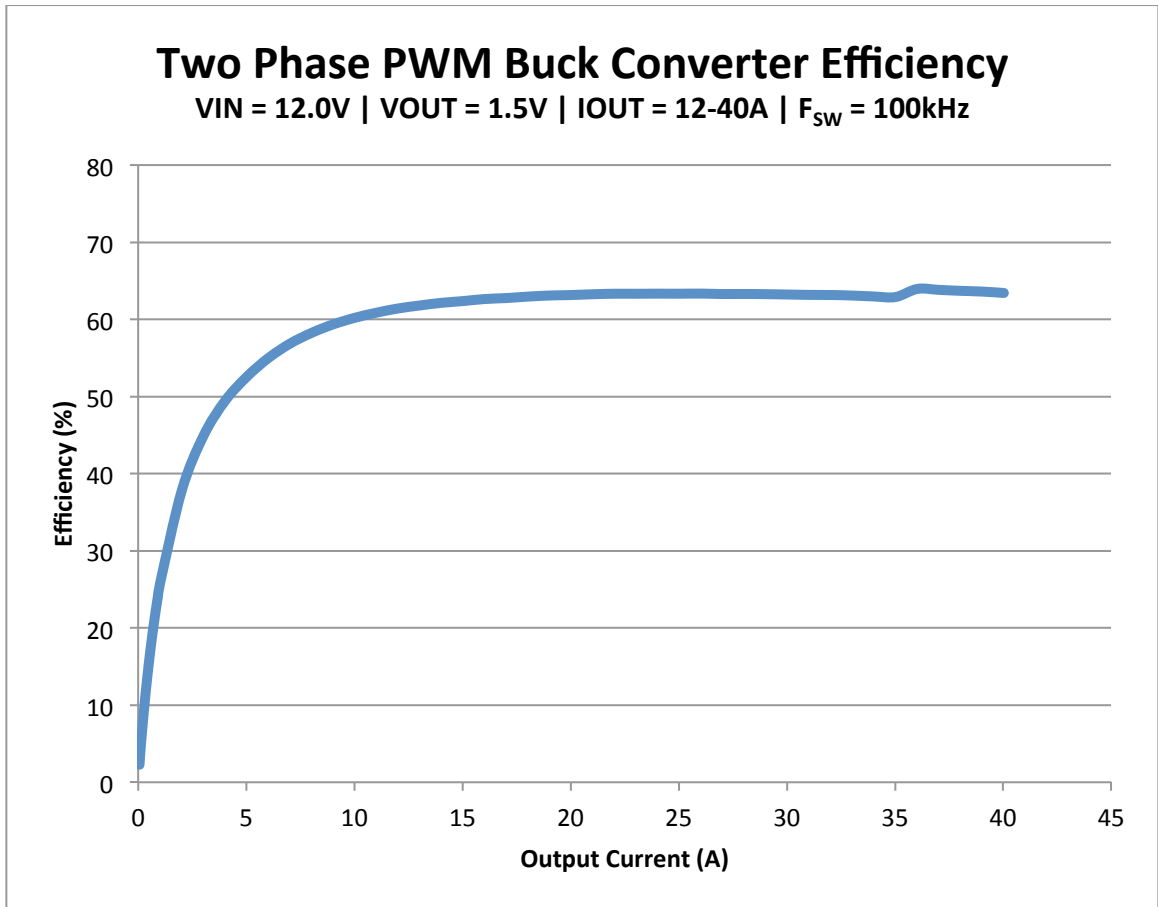


Figure 9-8: Efficiency Graph of Two Phase PFM Buck Converter at 100kHz

9.2.8 Efficiency Comparison between Pulse Width Modulation and Zero-Voltage-Switching at Switching Frequency of 100kHz

Below is the data to compare the full load efficiency of the Two Phase PWM Buck Converter and Two Phase PFM Zero-Voltage-Switching Buck Converter at a switching frequency of 100kHz. It can be seen there is approximately a 9.5% efficiency difference between the two buck converters favoring the Two Phase PWM Buck Converter. There are two main losses within a buck converter: conduction losses and switching losses. At lower frequencies, the conduction losses are the dominant of the two. However as the switching frequency is increased, the switching losses slowly become the dominant factor.

Table 9-5: Full Load Efficiency of Two Phase PWM Buck Converter at 100kHz

Load Current (A)	DMM Output Voltage (V)	DMM Input Voltage (V)	Input Current (A)	Efficiency (%)
40.004	1.493	11.987	7.838	63.551

Table 9-6: Full Load Efficiency of Two Phase PFM Zero-Voltage-Switching Buck Converter at 100kHz

Load Current (A)	DMM Output Voltage (V)	DMM Input Voltage (V)	Input Current (A)	Efficiency (%)
40.016	1.502	11.987	9.283	54.003

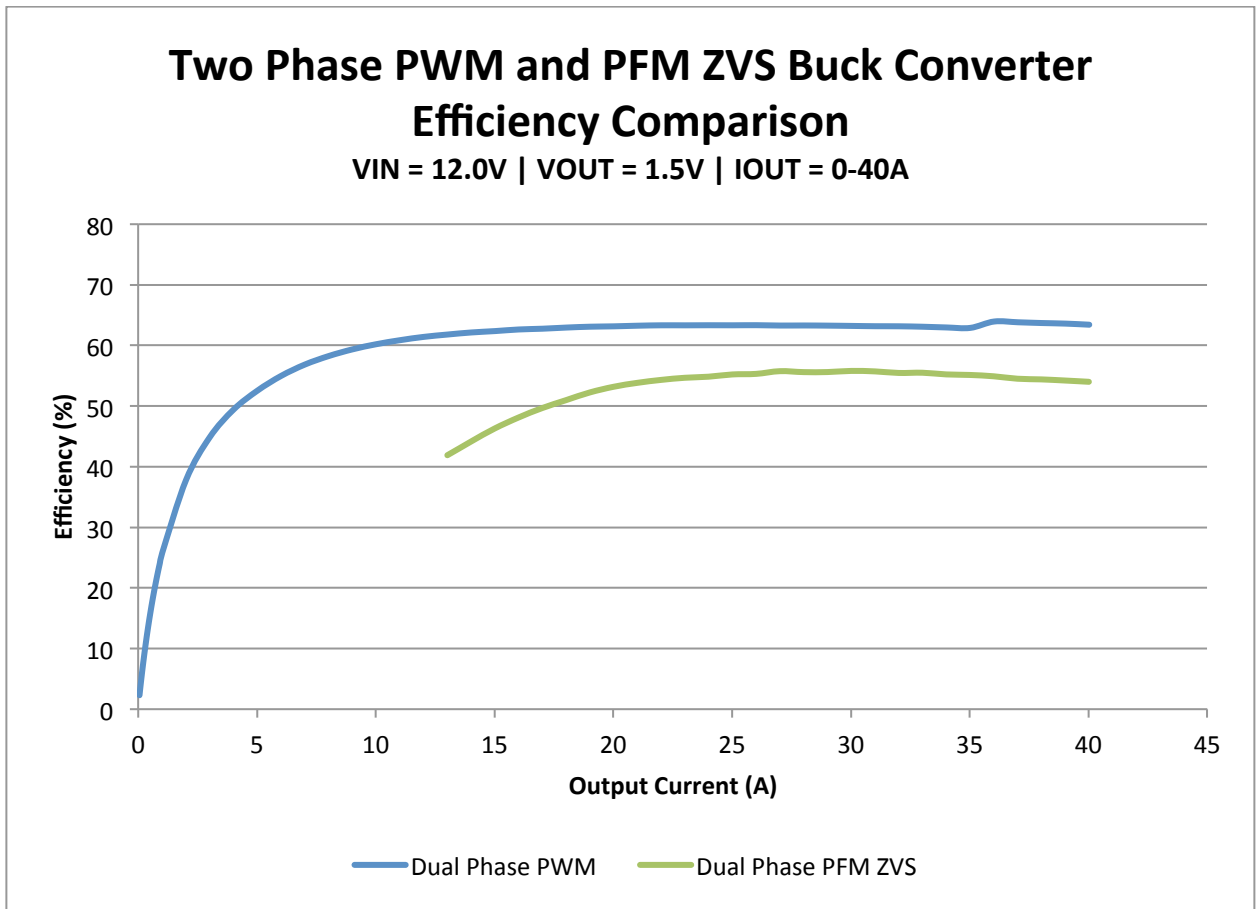


Figure 9-9: Efficiency Graph Comparison of Two Phase PWM and PFM ZVS Buck Converter at 100kHz

9.2.9 Efficiency at Various Switching Frequencies of Two Phase PWM Buck Converter

As stated in the previous sub-section, as the switching frequency increases in PWM Buck Converter, the efficiency will decrease because switching losses begin to play a larger role in the losses of the topology. With all the components the same and unchanged, only the switching frequency was increased. It can be seen in Table 9-7 that the efficiency at full load drops as the switching frequency increases. The complete efficiency curve at each switching frequency is shown in Figure 9-11. It can be seen that at each 100kHz increase of the switching frequency, there is nearly a 2% drop in efficiency with each step as shown by the trend line shown in Figure 9-11 – which is a

graphical representation of the efficiency data from Table 9-7. From 100kHz to 820kHz, the efficiency has dropped approximately 15.41%.

Table 9-7: Full Load Efficiency of Two Phase PWM Buck Converter

Frequency (kHz)	Load Current (A)	DMM Output Voltage (V)	DMM Input Voltage (V)	Input Current (A)	Efficiency (%)
100	40.032	1.493	11.991	7.858	63.421
200	40.032	1.499	11.991	8.154	61.388
300	40.032	1.500	11.991	8.492	58.949
400	40.032	1.501	11.991	8.791	57.003
500	40.016	1.506	11.988	9.285	54.158
600	40.012	1.500	11.988	9.528	52.543
700	40.036	1.496	11.991	9.757	51.194
800	40.036	1.494	11.991	10.272	48.561
820	40.036	1.495	11.991	10.399	48.009

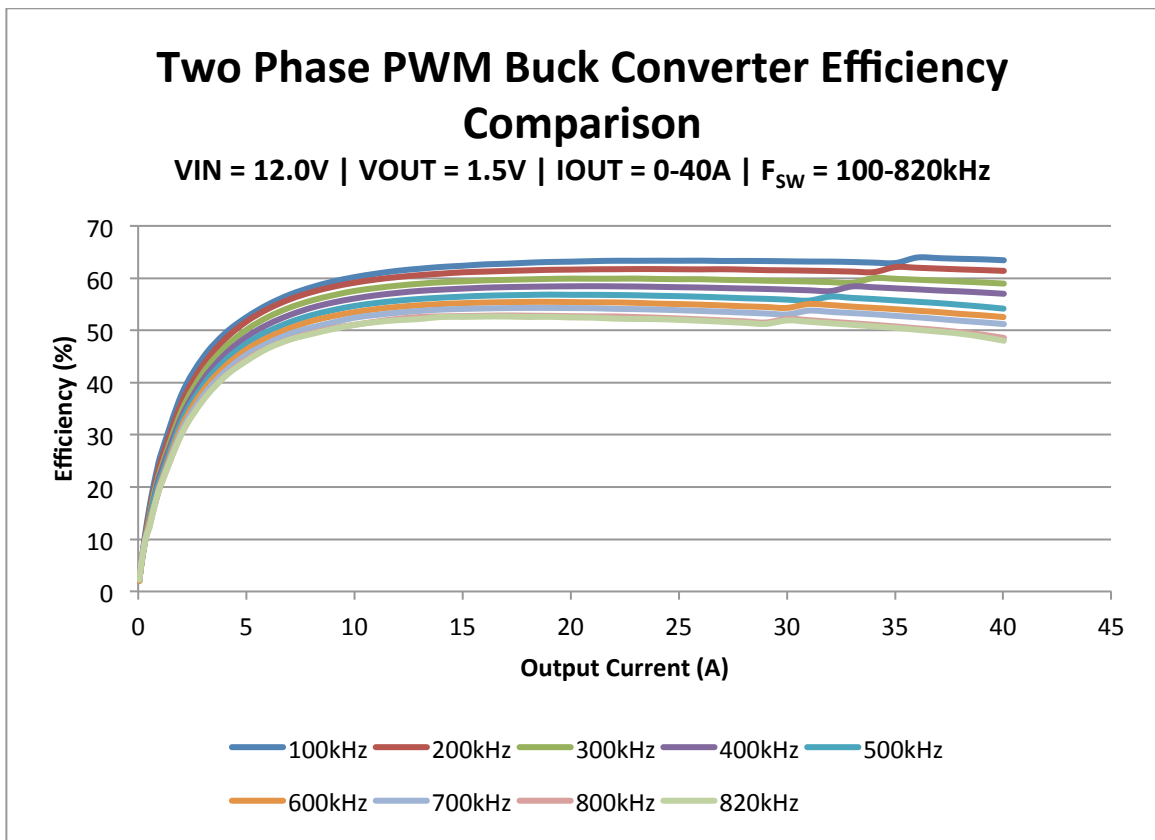


Figure 9-10: Efficiency Graph Comparison of Two Phase PWM Buck Converter at 100-820kHz

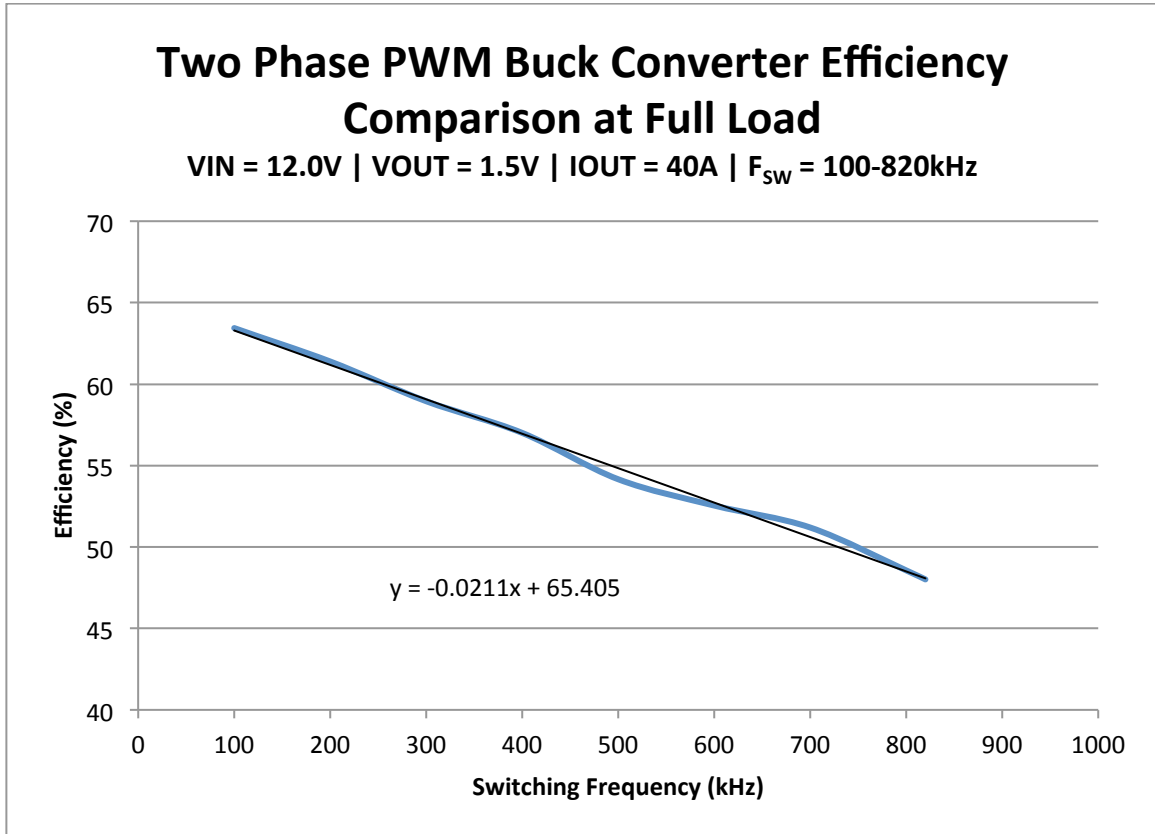


Figure 9-11: Full Load Efficiency Graph Comparison of Two Phase PWM Buck Converter at 100-820kHz

9.2.10 Efficiency at Various Switching Frequencies of Two Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter

Similar to the comparison of efficiency curves of the Two Phase PWM Buck Converter with increasing switching frequency, the same was done to the Two Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter. Unfortunately, efficiency for the Two Phase ZVS-QR Buck Converter with increasing switching frequency was much more difficult to perform so only three switching frequencies were chosen: 100 kHz, 500 kHz, and 820 kHz. The efficiency results at full load are listed in Table 9-8. The complete efficiency curve of each switching frequency is shown in Figure 9-12. The graphical representation of the data in Table 9-8 is shown in Figure 9-13. The trend line in Figure 9-13 shows from 100 kHz to 820 kHz, the efficiency is dropping approximately

0.2% per 100 kHz increase in switching frequency. From 100 kHz to 820 kHz, the efficiency has dropped approximately 1.81%. This is compared to 15.41% from the PWM Buck Converter. That is over 8.5 times the efficiency difference between the of the Two Phase PWM Buck Converter and the Two Phase PFM Zero-Voltage-Switching Buck Converter with latter proving its superiority in efficiency as switching losses increases with switching frequency.

Table 9-8: Full Load Efficiency of Two Phase PFM Zero-Voltage-Switching Buck Converter

Frequency (kHz)	Load Current (A)	DMM Output Voltage (V)	DMM Input Voltage (V)	Input Current (A)	Efficiency (%)
100	40.016	1.502	11.987	9.283	54.003
500	40.016	1.524	11.988	9.436	53.909
820	40.032	1.510	11.990	9.662	52.194

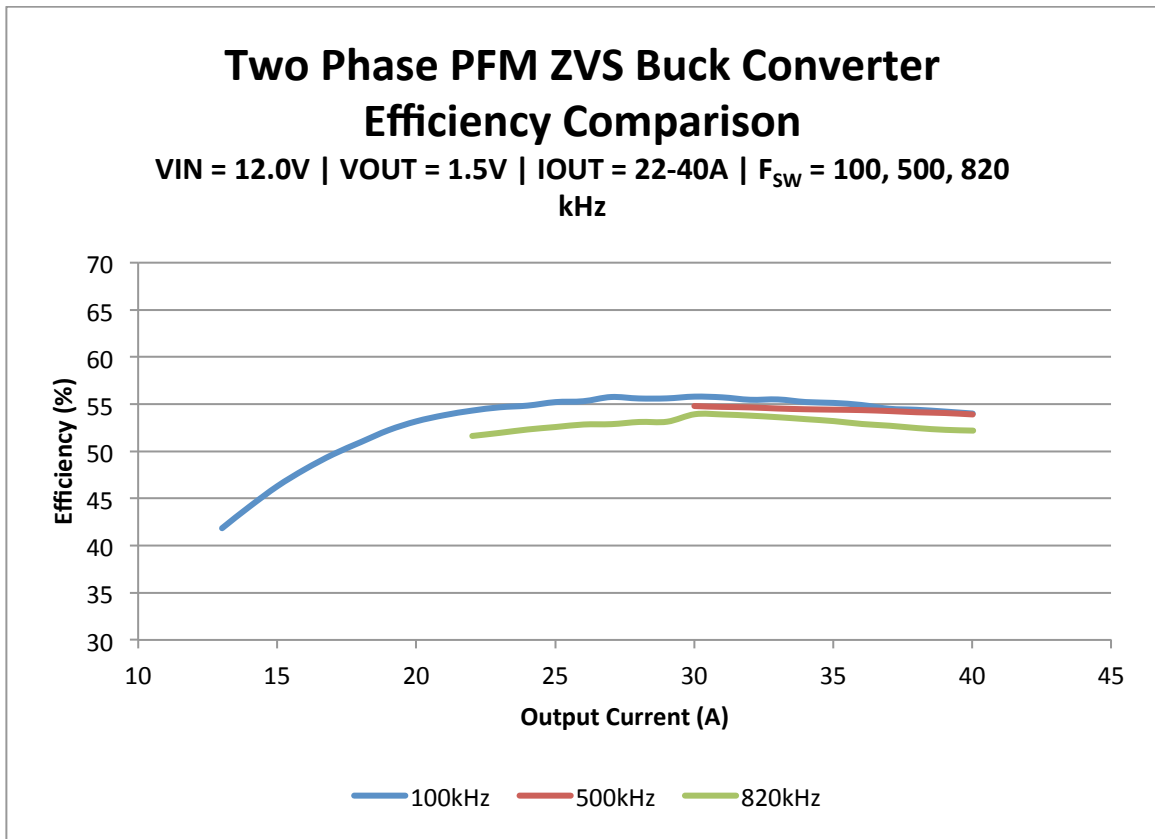


Figure 9-12: Efficiency Graph Comparison of Two Phase PFM ZVS Buck Converter at 100,500,820kHz

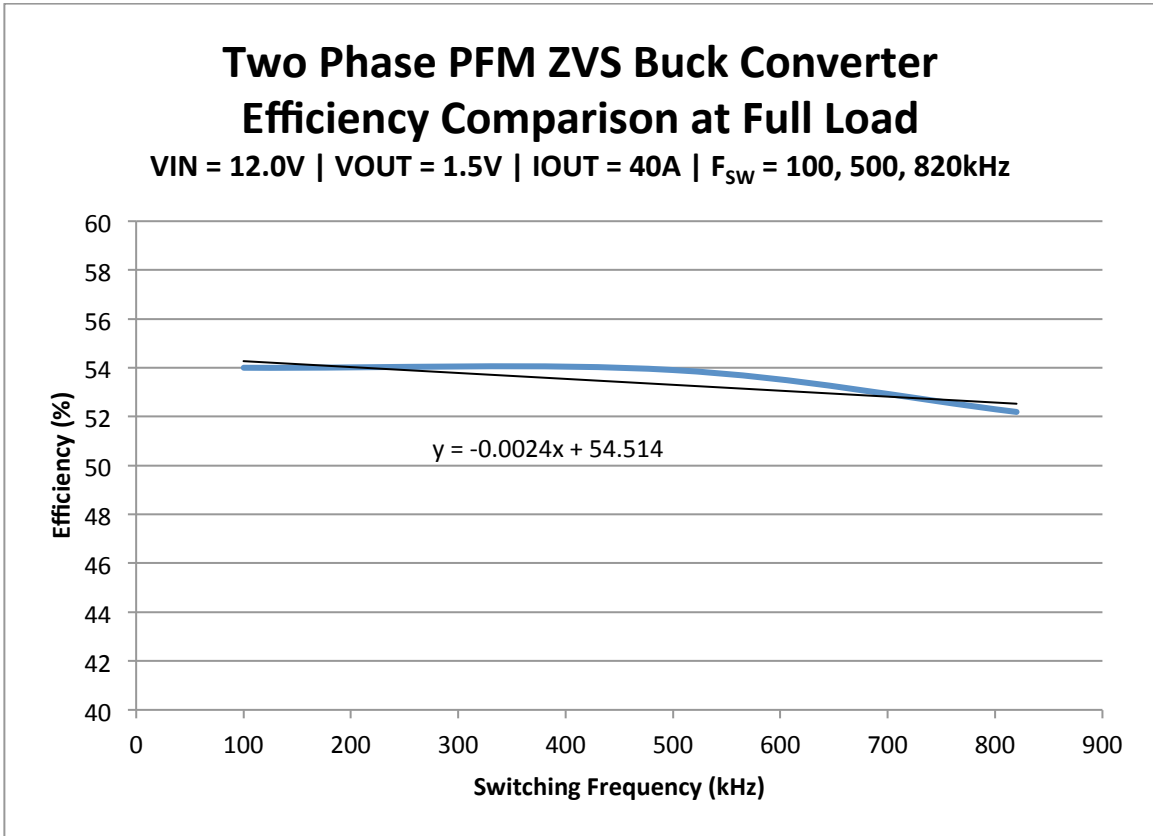


Figure 9-13: Full Load Efficiency Graph Comparison of Two Phase PFM ZVS Buck Converter at 100,500,820kHz

9.2.11 Efficiency Comparison between Pulse Width Modulation and Zero-Voltage-Switching at Switching Frequency of 820kHz

Below is the data to compare the full load efficiency of the Two Phase PWM Buck Converter and Two Phase PFM Zero-Voltage-Switching Quasi-Resonant Buck Converter at a switching frequency of 820 kHz. As shown, there is approximately a 2.1% efficiency difference between the two buck converters in favor of the Two Phase ZVS-QR Buck Converter. Figure 9-15 illustrates graphically the full efficiency curves of the two topologies at a switching frequency of 820 kHz. Unfortunately, the Two Phase PFM ZVS-QR Converter must operate at a non-zero load current. However, the current at which the Two Phase ZVS-QR Buck Converter operates, the efficiency is overall better throughout the load current range than the Two Phase PWM Buck Converter. Table 9-11

and Table 9-12 list the complete efficiency curve data for the Two Phase PWM Buck Converter and the Two Phase PFM Zero-Voltage-Switching Quasi-Resonant Buck Converter, respectively.

Table 9-9: Full Load Efficiency of Two Phase PWM Buck Converter at 820kHz

Load Current (A)	DMM Output Voltage (V)	DMM Input Voltage (V)	Input Current (A)	Efficiency (%)
40.036	1.495	11.991	10.399	48.009

Table 9-10: Full Load Efficiency of Two Phase PFM Zero-Voltage-Switching Quasi-Resonant Buck Converter at 820kHz

Load Current (A)	DMM Output Voltage (V)	DMM Input Voltage (V)	Input Current (A)	Efficiency (%)
40.032	1.510	11.990	9.662	52.194

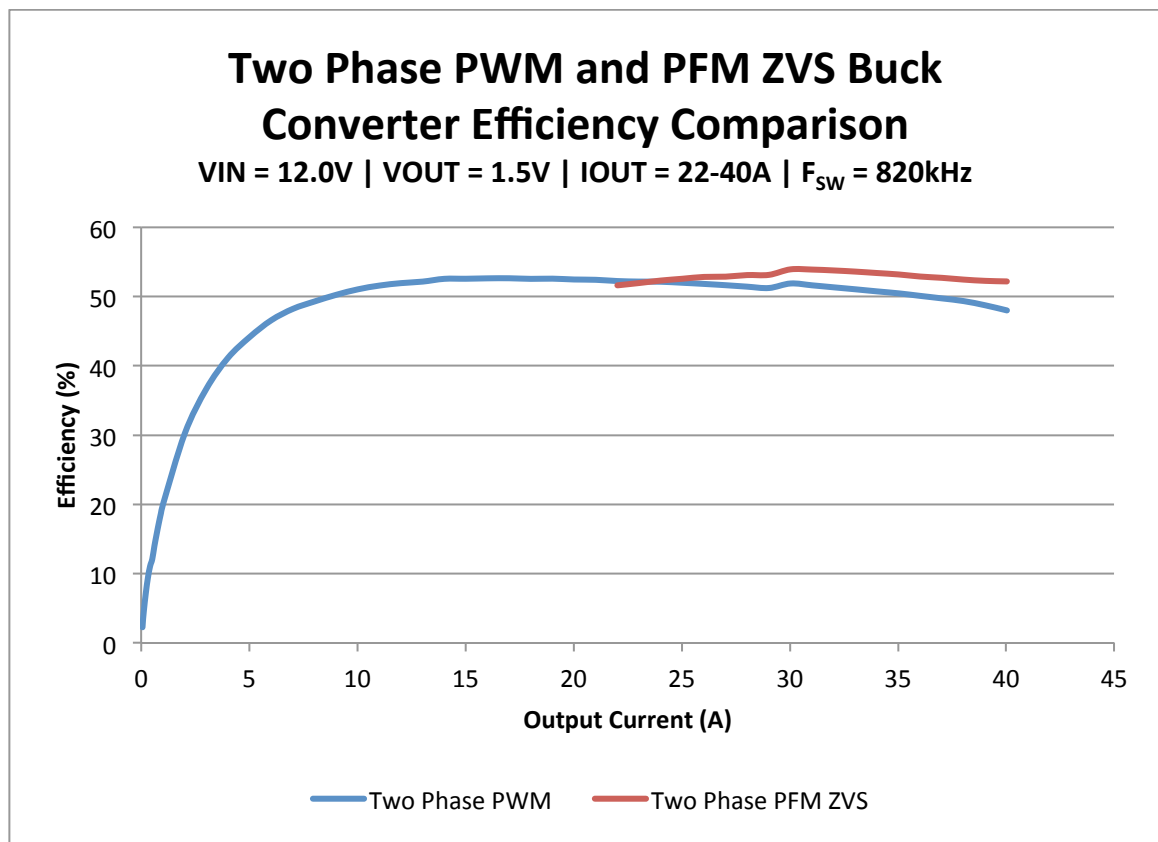


Figure 9-14: Efficiency Graph Comparison of Two Phase PFM ZVS Buck Converter at 820kHz

Table 9-11: Efficiency Data for Two Phase PWM Buck Converter at 820kHz

Load Current (A)	DMM Output Voltage (V)	DMM Input Voltage (V)	Input Current (A)	Efficiency (%)
0.056	1.494	12.015	0.307	2.269
0.124	1.492	12.015	0.334	4.607
0.216	1.492	12.015	0.372	7.203
0.314	1.492	12.015	0.413	9.444
0.414	1.489	12.015	0.463	11.089
0.514	1.486	12.015	0.525	12.112
0.614	1.493	12.015	0.544	14.012
0.714	1.491	12.015	0.565	15.673
0.814	1.494	12.015	0.586	17.262
0.914	1.492	12.015	0.606	18.717
1.014	1.492	12.015	0.628	20.055
2.016	1.491	12.015	0.827	30.227
3.016	1.491	12.015	1.020	36.691
4.016	1.492	12.015	1.211	41.158
5.02	1.488	12.015	1.407	44.170
6.016	1.492	12.015	1.604	46.588
7.02	1.489	12.015	1.803	48.234
8.016	1.493	12.015	2.021	49.297
9.02	1.493	12.015	2.229	50.259
10.02	1.496	12.015	2.445	51.049
11.02	1.496	12.015	2.660	51.596
12.02	1.496	12.014	2.881	51.947
13.02	1.493	12.014	3.101	52.169
14.02	1.493	12.014	3.314	52.568
15.02	1.492	12.014	3.549	52.579
16.024	1.493	12.014	3.783	52.639
17.024	1.492	12.014	4.017	52.650
18.024	1.493	12.014	4.260	52.564
19.024	1.492	12.013	4.492	52.592
20.024	1.491	12.013	4.737	52.471
21.024	1.492	12.013	4.982	52.427
22.028	1.490	12.013	5.230	52.247
23.028	1.490	12.013	5.476	52.172
24.028	1.491	12.013	5.718	52.146
25.028	1.491	12.012	5.972	52.000
26.028	1.491	12.012	6.231	51.833

27.028	1.491	12.012	6.496	51.648
28.028	1.490	12.012	6.759	51.436
29.032	1.490	12.012	7.029	51.244
30.032	1.490	11.991	7.190	51.896
31.032	1.490	11.991	7.469	51.629
32.032	1.491	11.991	7.757	51.340
33.032	1.491	11.991	8.045	51.055
34.032	1.491	11.991	8.339	50.756
35.032	1.493	11.991	8.644	50.472
36.036	1.493	11.991	8.958	50.102
37.036	1.496	11.991	9.290	49.743
38.036	1.499	11.991	9.631	49.353
39.036	1.496	11.991	9.989	48.745
40.036	1.495	11.991	10.399	48.009

Table 9-12: Full Load Efficiency of Two Phase PFM Zero-Voltage-Switching Quasi-Resonant Buck Converter at 820kHz

Load Current (A)	DMM Output Voltage (V)	DMM Input Voltage (V)	Input Current (A)	Efficiency (%)
22.024	1.525	12.010	5.419	51.626
23.024	1.515	12.010	5.591	51.961
24.024	1.516	12.010	5.798	52.318
25.024	1.516	12.010	6.007	52.578
26.024	1.517	12.010	6.222	52.842
27.024	1.516	12.009	6.453	52.880
28.024	1.517	12.009	6.665	53.111
29.028	1.513	12.009	6.884	53.139
30.028	1.517	11.990	7.043	53.935
31.028	1.515	11.990	7.273	53.904
32.028	1.517	11.990	7.536	53.778
33.028	1.516	11.990	7.790	53.611
34.028	1.513	11.990	8.040	53.406
35.028	1.514	11.990	8.317	53.199
36.028	1.511	11.990	8.583	52.898
37.032	1.514	11.990	8.870	52.711
38.032	1.512	11.990	9.145	52.458
39.032	1.511	11.990	9.411	52.276
40.032	1.510	11.990	9.662	52.194

9.2.12 Efficiency Comparison between Two Phase Pulse Width Modulation and Zero-Voltage-Switching at Switching Frequency from 100-820kHz

Table 9-11 and Table 9-12 contain the data to compare the full load efficiency of the Two Phase PWM Buck Converter and Two Phase PFM Zero-Voltage-Switching Buck Converter at a switching frequency of 100 kHz, 500 kHz, and 820 kHz. Increasing the switching frequency from 100 kHz to 800 kHz, the Two Phase PWM Buck Converter drops 15.41% in efficiency. Compare this to the Two Phase PFM Zero-Voltage-Switching Buck Converter dropping 1.81% in efficiency. The conclusion could be drawn that the decrease in efficiency for the Two Phase PWM Buck Converter is due to the increased switching losses because of the increased switching frequency. The Two Phase PFM Zero-Voltage-Switching Buck Converter does not suffer from this massive efficiency loss because the switching loss is minimized with the Two Phase PFM Zero-Voltage-Switching Buck Converter.

Figure 9-15 graphs the data from Table 9-13 and Table 9-14. The intersection point could prove to show that it is the point at which the conduction losses and switching losses changes its dominance over the total loss of the buck converter. It can be concluded about the total power loss for this particular PCB and component selection that buck converters with switching frequencies less than 500 kHz are dominated by conduction losses while with switching frequencies greater than 500 kHz switching losses dominate.

Table 9-13: Full Load Efficiency of Two Phase PWM Buck Converter

Frequency (kHz)	Load Current (A)	DMM Output Voltage (V)	DMM Input Voltage (V)	Input Current (A)	Efficiency (%)
100	40.032	1.493	11.991	7.858	63.421
500	40.016	1.506	11.988	9.285	54.158
820	40.036	1.495	11.991	10.399	48.009

Table 9-14: Full Load Efficiency of Two Phase PFM Zero-Voltage-Switching Buck Converter

Frequency (kHz)	Load Current (A)	DMM Output Voltage (V)	DMM Input Voltage (V)	Input Current (A)	Efficiency (%)
100	40.016	1.502	11.987	9.283	54.003
500	40.016	1.524	11.988	9.436	53.909
820	40.032	1.510	11.990	9.662	52.194

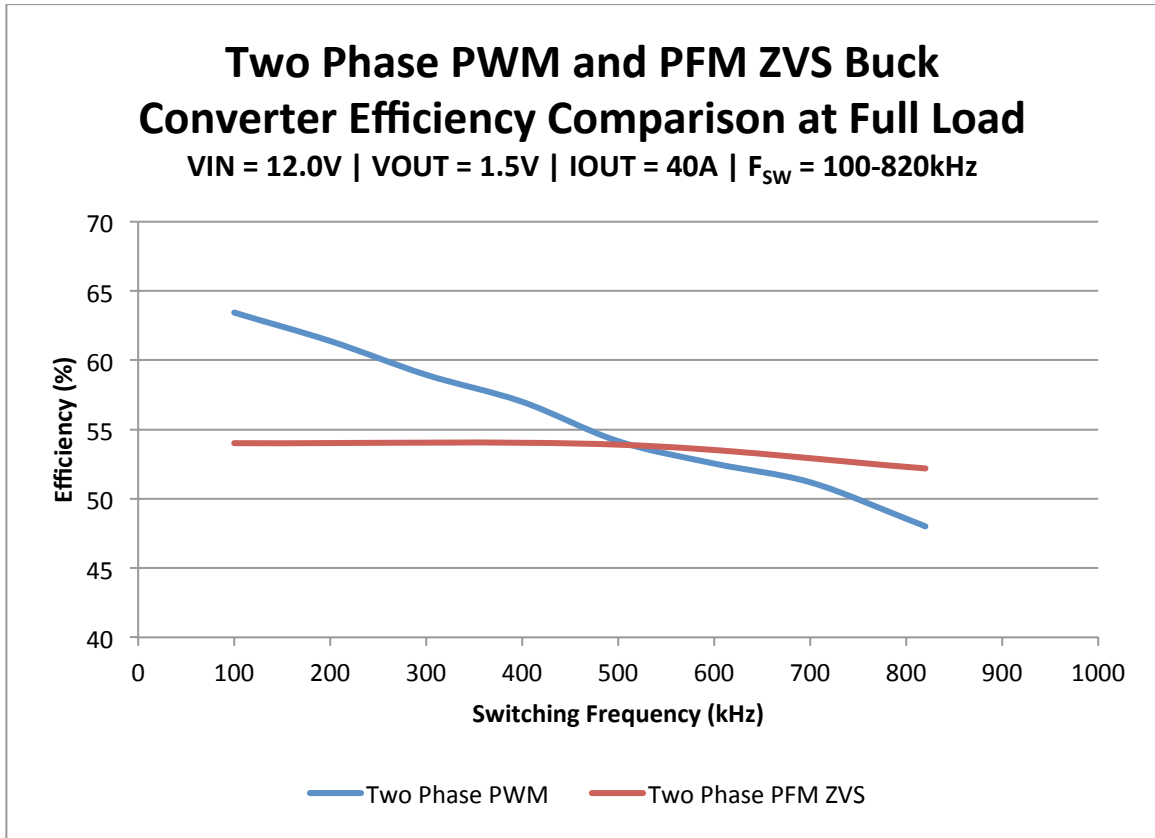


Figure 9-15: Full Load Efficiency Graph Comparison of Two Phase PWM and PFM ZVS Buck Converter at 100-820kHz

9.2.13 Load Regulation of Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter at 820kHz

Since there is a change in the switching frequency, there will also be a change in the minimum possible load current for the Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter – which is only 22 A. The load regulation will be calculated with a minimum load current of 22 A instead of the typical no load condition of 0A.

Table 9-15 lists the load regulation data for the Two-Phase Zero-Voltage-Switching

Quasi-Resonant Buck Converter from 22 A to 40 A. Figure 9-16 shows a graphical representation of the load regulation data from Table 9-2. The load regulation is slightly less than the design requirement of 1%.

$$\text{Load Regulation} = \left| \frac{V_{Vmax} - V_{Vmin}}{V_{Vmax}} \right| \times 100 \quad (9-9)$$

$$\text{Load Regulation} = \left| \frac{1.510V - 1.525V}{1.510V} \right| \times 100 = 1.002\% \quad (9-10)$$

Table 9-15: Load Regulation Data for Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter at 820kHz

Load Current (A)	DMM Output Voltage (V)
22.024	1.525
23.024	1.515
24.024	1.516
25.024	1.516
26.024	1.517
27.024	1.516
28.024	1.517
29.028	1.513
30.028	1.517
31.028	1.515
32.028	1.517
33.028	1.516
34.028	1.513
35.028	1.514
36.028	1.511
37.032	1.514
38.032	1.512
39.032	1.511
40.032	1.510

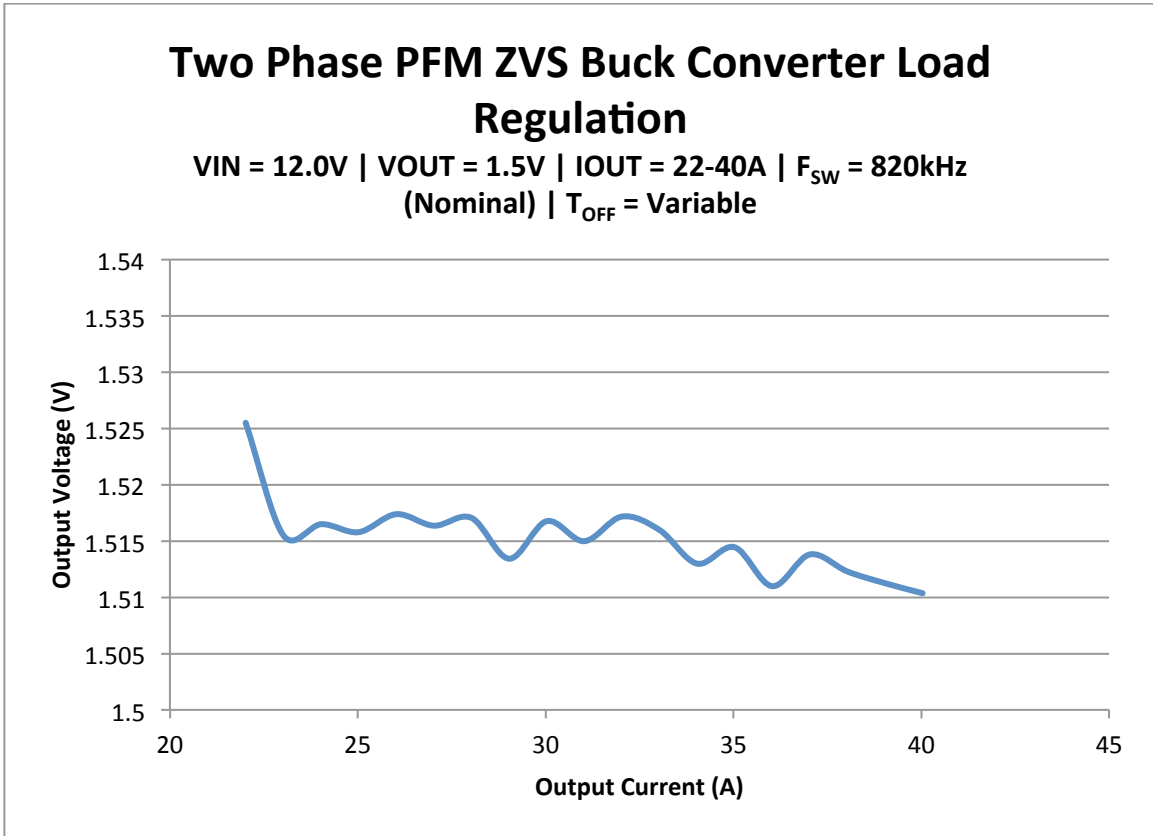


Figure 9-16: Load Regulation Graph of Two Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter at 820kHz

9.2.14 Line Regulation of Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter at 820kHz

Similar to the load regulation, the line regulation will be calculated with a minimum load current of 22 A instead of the typical no load condition of 0 A. Table 9-16 lists the line regulation data for the Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter from 10.8 V to 13.2 V. The line regulation is measured +10% and -10% from the nominal voltage of 12.0 V, which results in 13.2 V and 10.8 V – respectively. Figure 9-17 shows a graphical representation of the load regulation data from Table 9-17. Just like the line regulation for a switching frequency of 100 kHz, the line regulation is well under the design requirement of 1%.

$$\text{Line Regulation} = \left| \frac{V_{Vmax} - V_{Vmin}}{V_{Vmax}} \right| \times 100 \quad (9-11)$$

$$\text{Line Regulation} = \left| \frac{1.510V - 1.510V}{1.510V} \right| \times 100 = 0.046\% \quad (9-12)$$

Table 9-16: Line Regulation Data for Two-Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter at 820kHz

Load Current (A)	DMM Output Voltage (V)	DMM Input Voltage (V)	Input Current (A)	Efficiency (%)
40.028	1.510	10.790	10.642	52.630
40.032	1.511	10.990	10.476	52.534
40.032	1.514	11.190	10.307	52.533
40.028	1.513	11.390	10.173	52.275
40.032	1.512	11.590	10.012	52.148
40.032	1.510	11.790	9.852	52.036
40.028	1.512	11.989	9.711	51.973
40.032	1.513	12.189	9.555	51.990
40.028	1.511	12.389	9.447	51.685
40.028	1.512	12.589	9.300	51.697
40.032	1.512	12.789	9.182	51.531
40.028	1.513	12.989	9.064	51.448
40.032	1.510	13.189	8.904	51.491

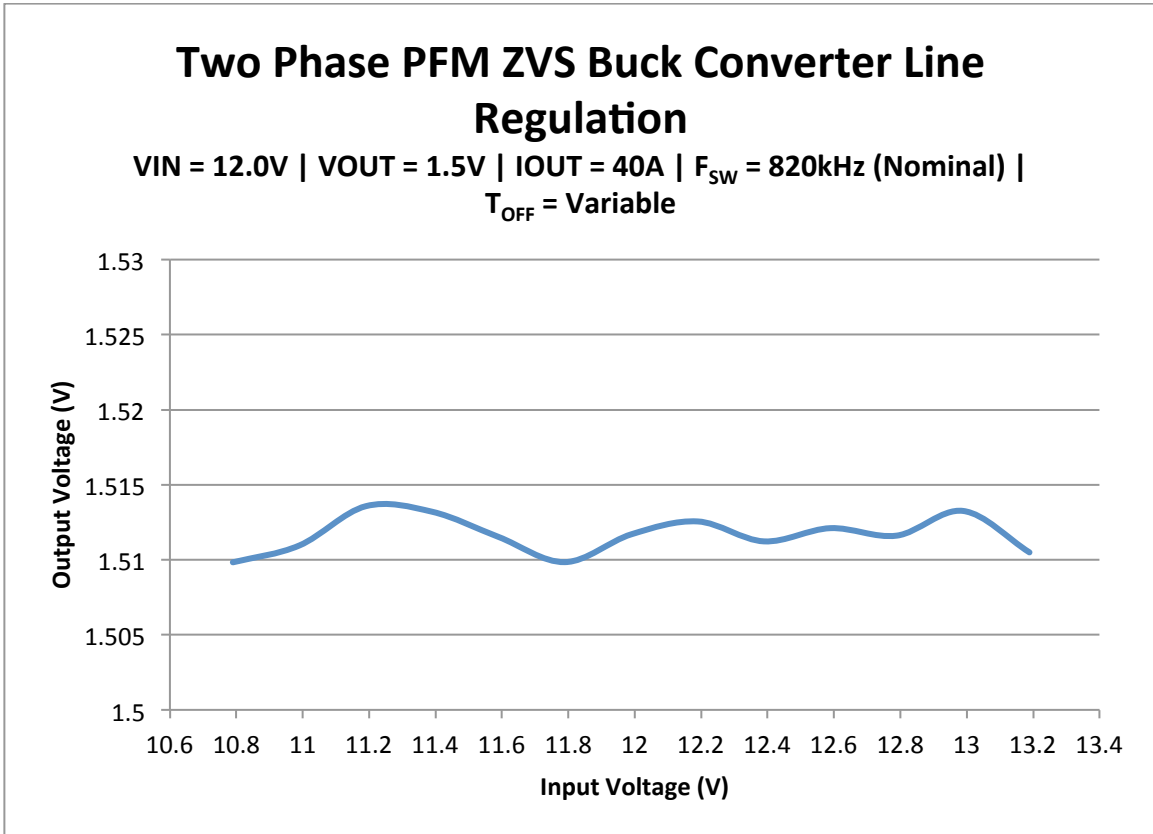


Figure 9-17: Line Regulation Graph of Two Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter at 820kHz

9.2.15 Switching Waveform and Trajectory of Phase 1 and Phase 2 for the Two Phase Zero-Voltage-Switching Buck Converter at Switching Frequency of 100 and 820kHz

Figure 9-18 and Figure 9-20 show the oscilloscope captures of the current through the high-side PMOS of phase 1 and phase 2, respectively, and the voltage across the high-side PMOS (V_{SD}) for the Two Phase Zero-Voltage-Switching Buck Converter at a switching frequency of 100 kHz. The oscilloscope captures make conceptual sense because when the high-side PMOS is on, then the V_{SD} is zero with the current through the PMOS rising linearly.

The current through the high-side PMOS was measured through a pair of 2 m Ω surface mount current sense resistors for a nominal equivalent resistance of 1 m Ω . A

differential probe was used to measure across the current sense resistors because the differential math function of two passive probes does not provide enough resolution to make any quantitative analysis. The data points were then extracted from the oscilloscope capture and the switching trajectory of the high-side PMOS of phase 1 and phase 2 were generated in Microsoft Excel.

The resultant high-side PMOS switching trajectory of phase 1 and phase 2 are shown in Figure 9-19 and Figure 9-21, respectively. The switching trajectory graphs closely mirrors what is expected above from Figure 2-3 in Chapter 2. The switching trajectory closely follows the x-axis and y-axis. The further the switching trajectory is away from the x-axis and y-axis, then the greater the power loss.

Similarly, Figure 9-22 and Figure 9-24 shows the oscilloscope capture of the current through the high-side PMOS of phase 1 and phase 2, respectively, and the voltage across the high-side PMOS (V_{SD}) at a switching frequency of 820 kHz. Unfortunately, the oscilloscope captures does not make conceptual sense because when the high-side PMOS is on, then the V_{SD} is zero but the current through the PMOS does not rise linearly. A possible explanation for this is the measurement probe's parasitic capacitance and the high switching frequency. As a result, the oscilloscope capture and switching trajectory at a switching frequency of 100 kHz is better suited for quantitative analysis.

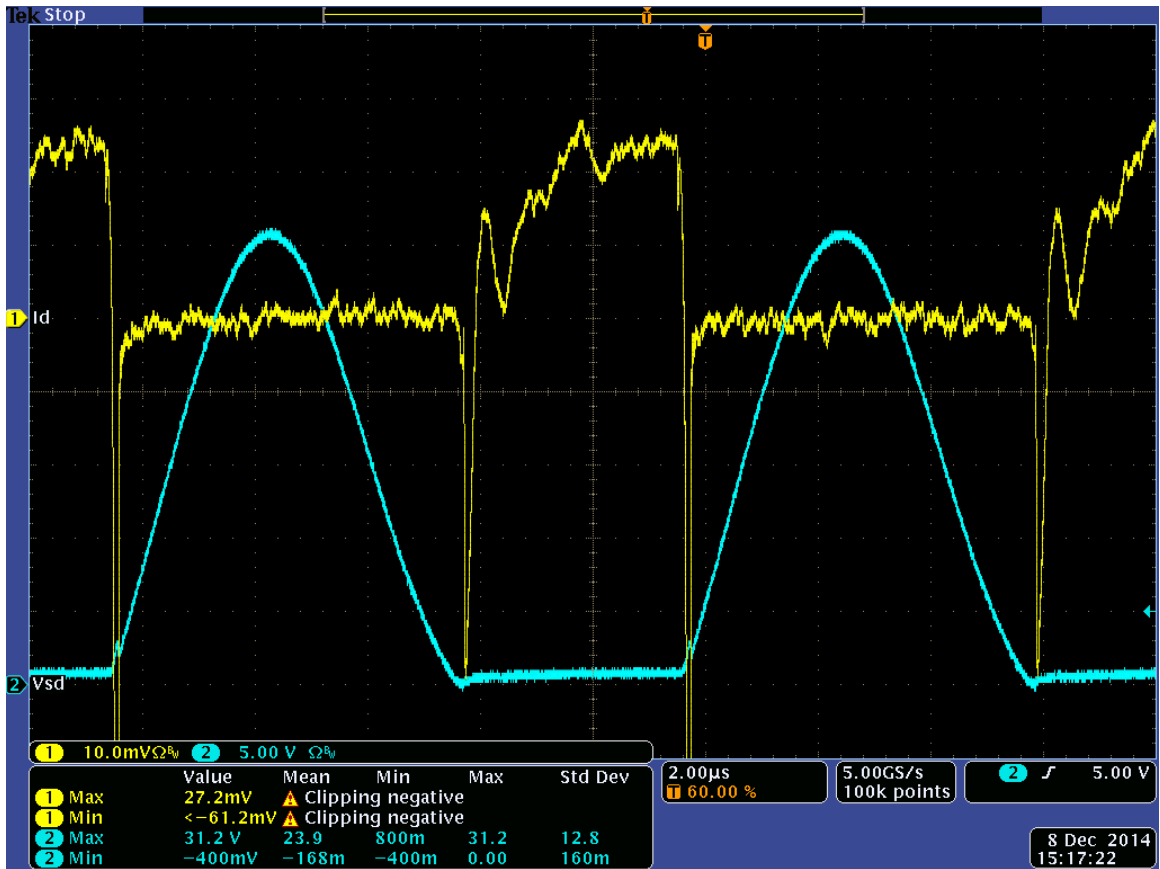


Figure 9-18: Phase 1 Switching Trajectory Waveform of Dual Phase Zero-Voltage-Switching Quasi Resonant Buck Converter at 100kHz

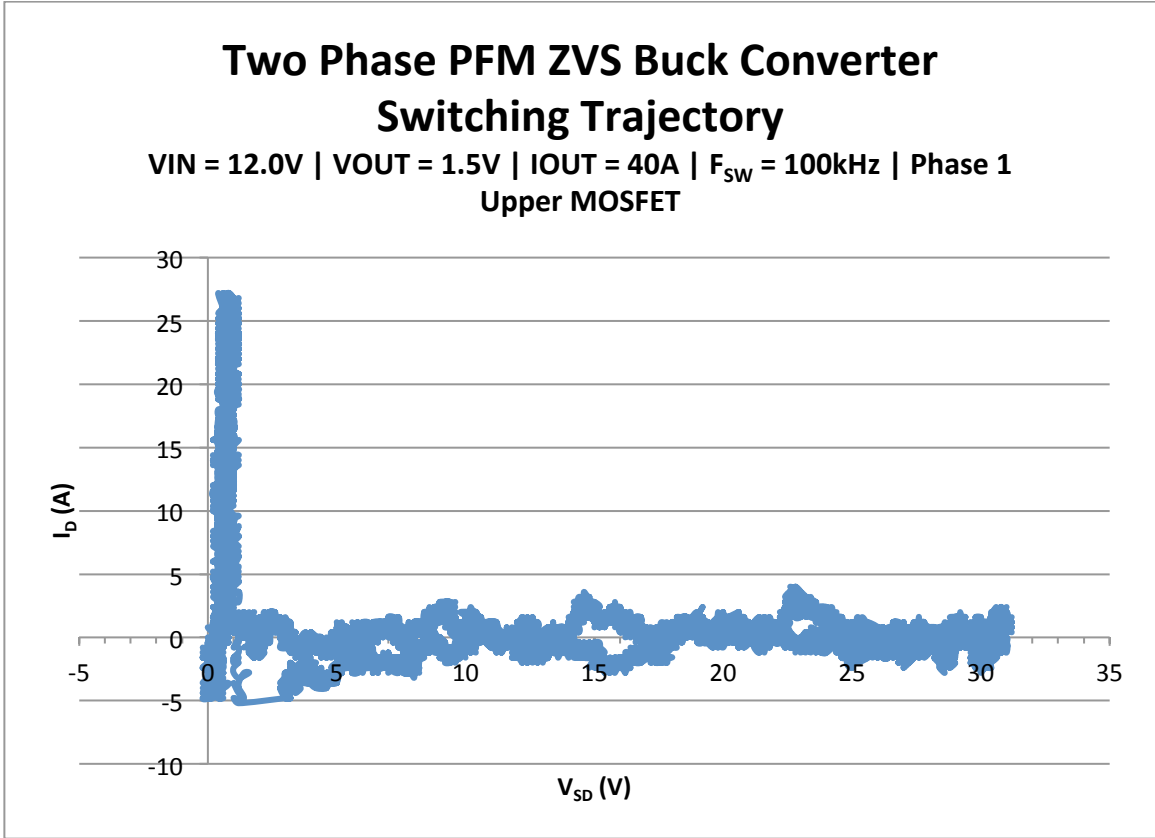


Figure 9-19: Phase 1 Switching Trajectory of Dual Phase Zero-Voltage-Switching Quasi Resonant Buck Converter at 100kHz

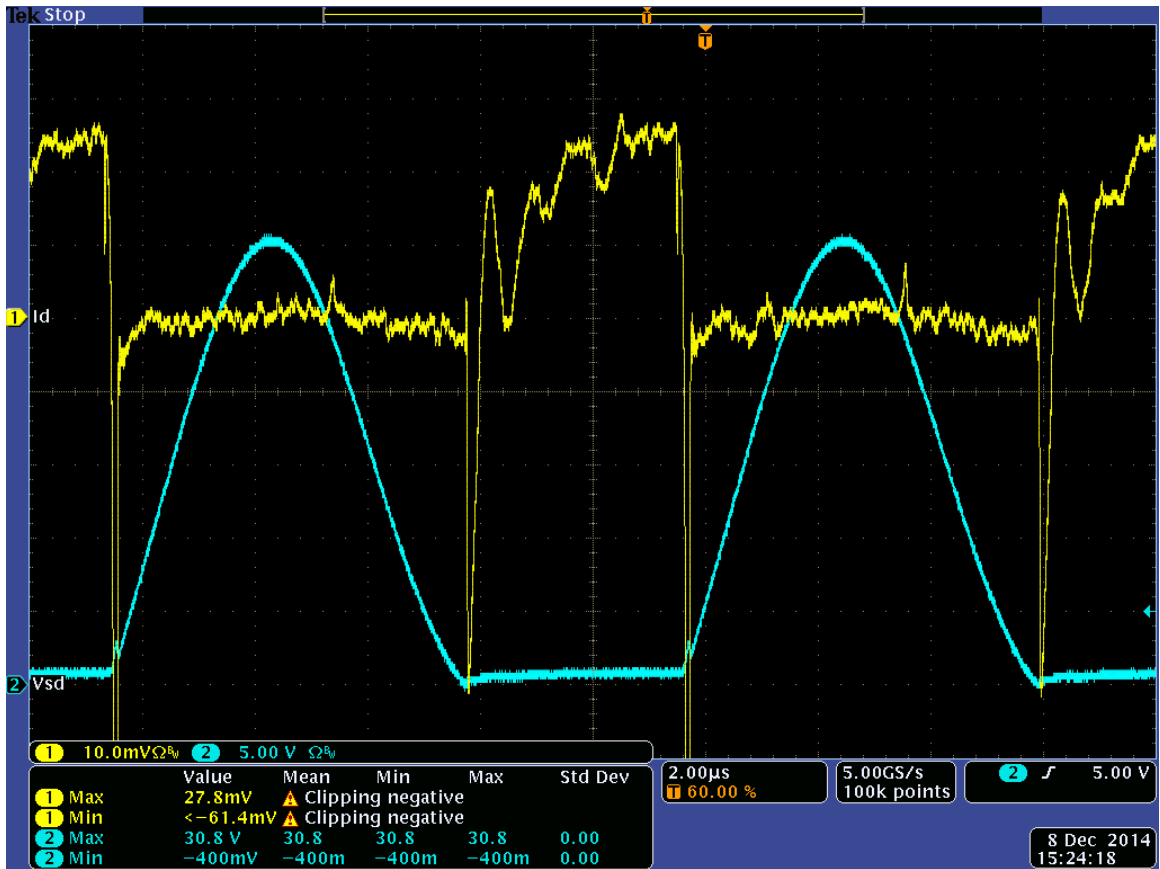


Figure 9-20: Phase 2 Switching Trajectory Waveform of Dual Phase Zero-Voltage-Switching Quasi Resonant Buck Converter at 100kHz

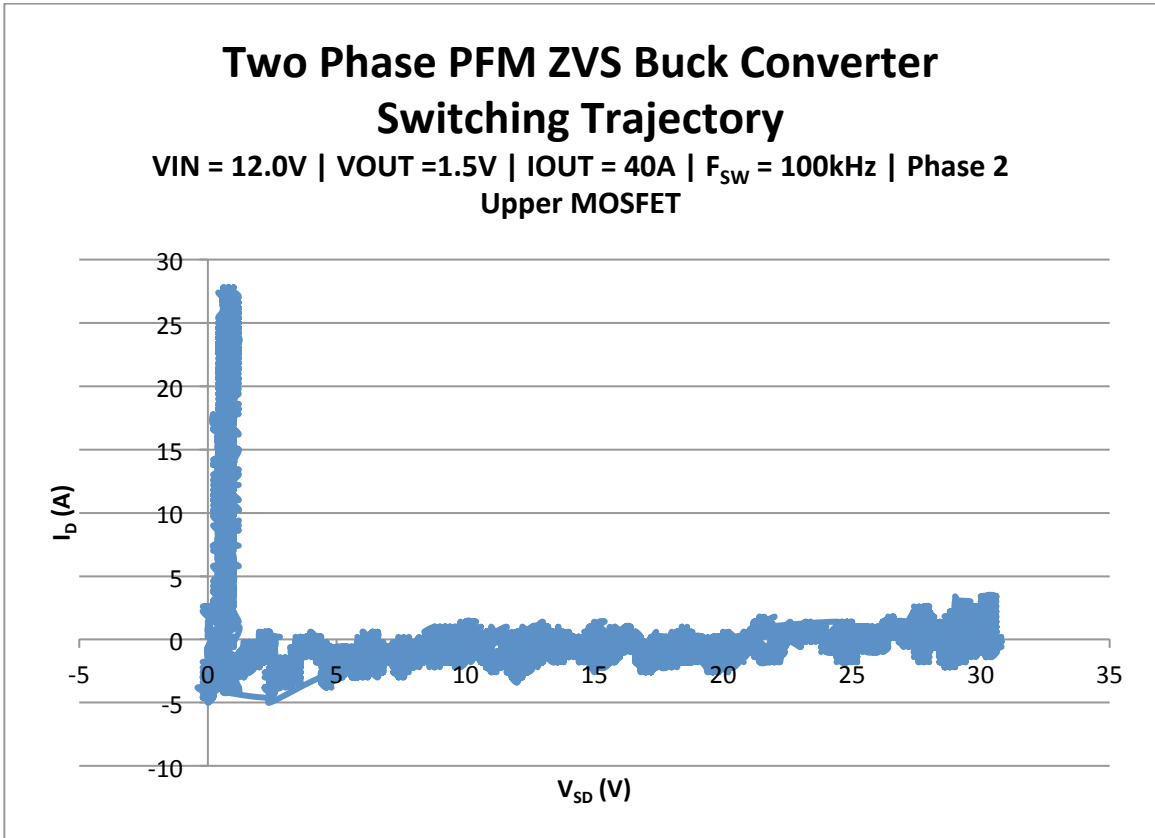


Figure 9-21: Phase 1 Switching Trajectory of Dual Phase Zero-Voltage-Switching Quasi Resonant Buck Converter at 100kHz

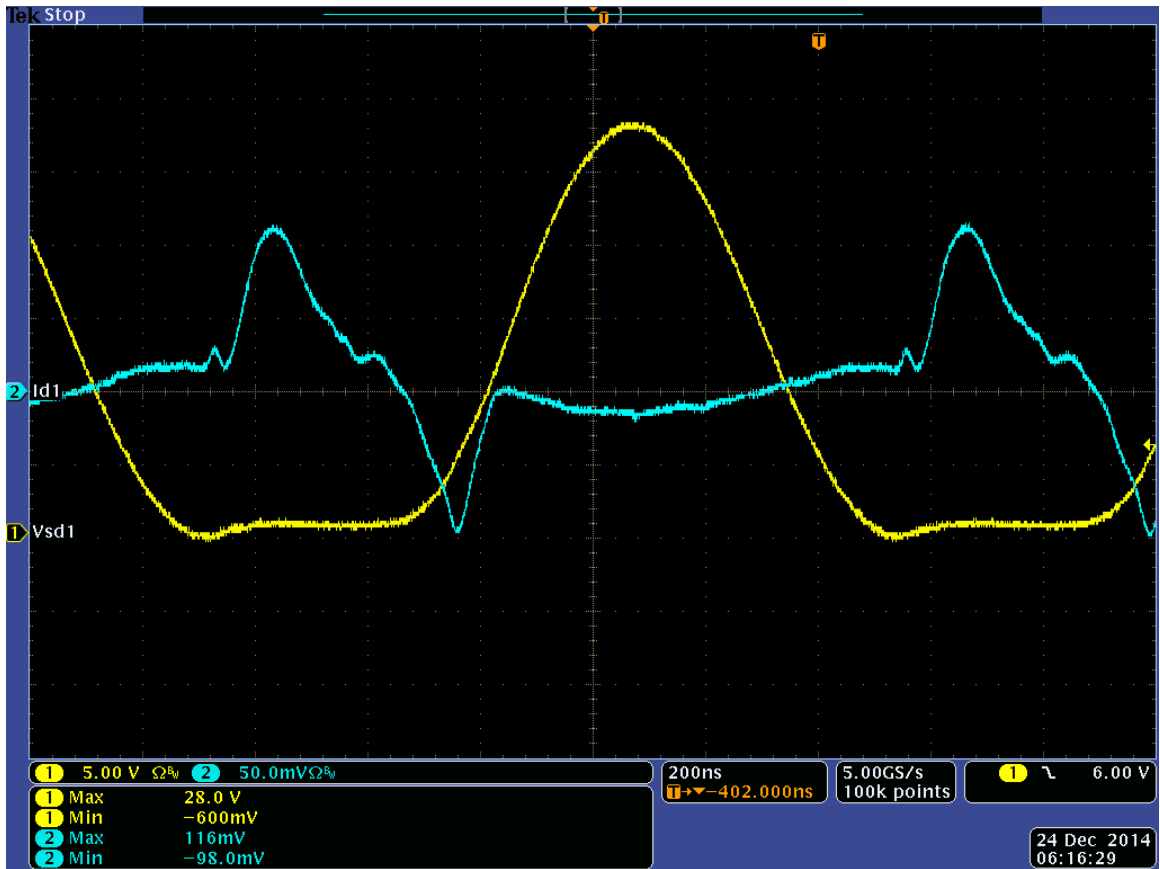


Figure 9-22: Phase 1 Switching Trajectory Waveform of Dual Phase Zero-Voltage-Switching Quasi Resonant Buck Converter at 820kHz

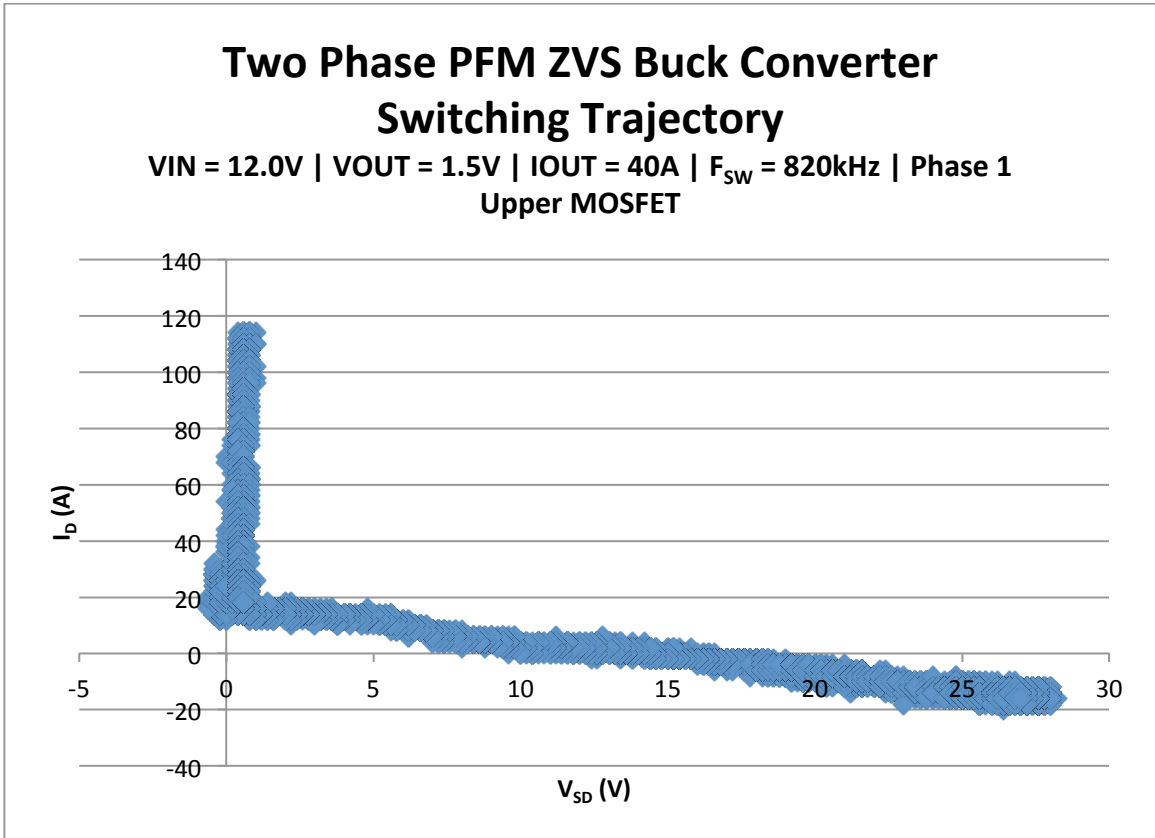


Figure 9-23: Phase 1 Switching Trajectory of Dual Phase Zero-Voltage-Switching Quasi Resonant Buck Converter at 820kHz

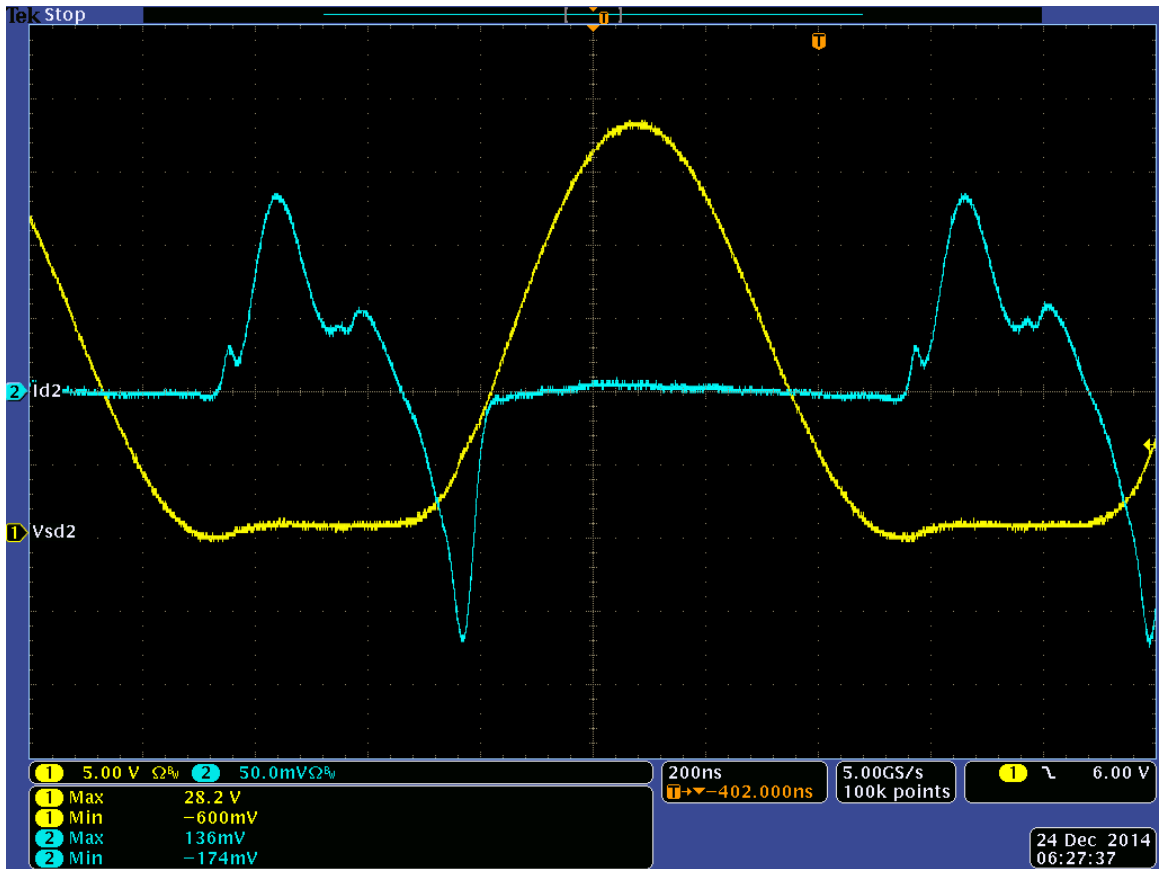


Figure 9-24: Phase 2 Switching Trajectory Waveform of Dual Phase Zero-Voltage-Switching Quasi Resonant Buck Converter at 820kHz

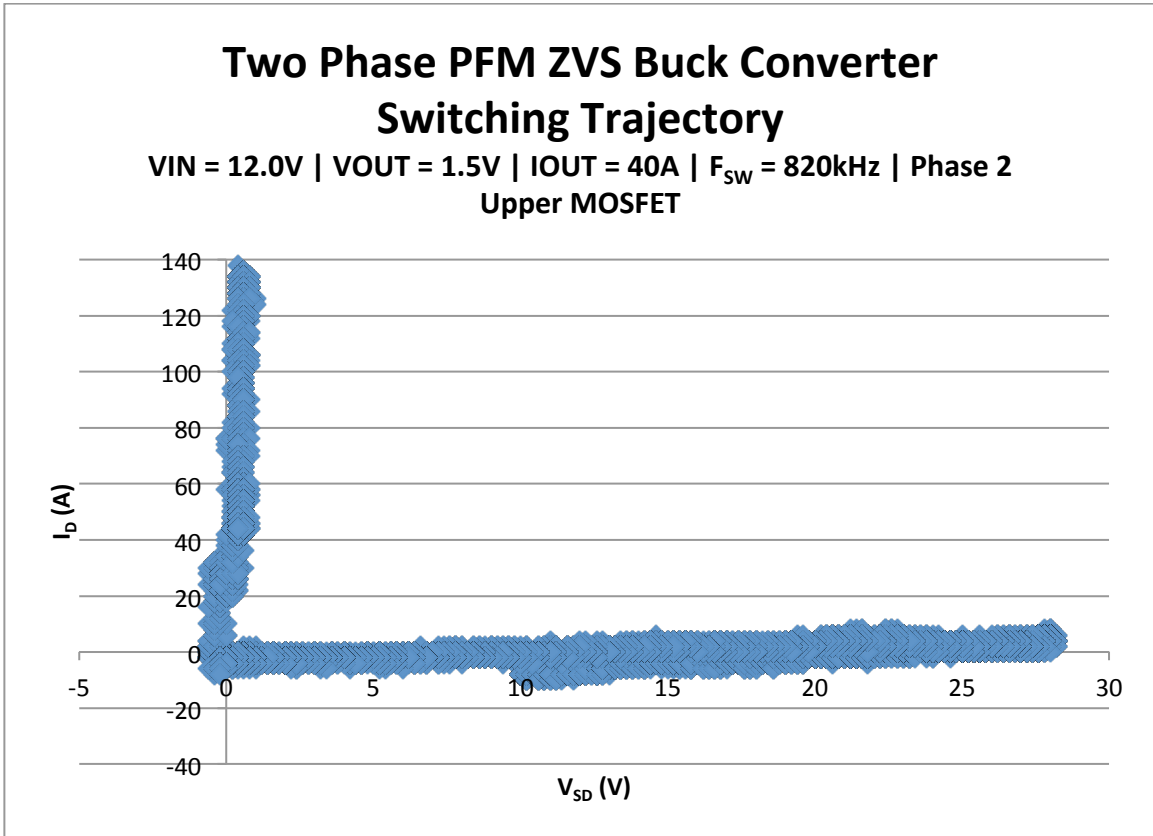


Figure 9-25: Phase 2 Switching Trajectory of Dual Phase Zero-Voltage-Switching Quasi Resonant Buck Converter at 820kHz

9.2.16 Switching Waveform and Trajectory of Phase 1 and Phase 2 for the Two Phase PWM Buck Converter at Switching Frequency of 100 kHz

Figure 9-26 and Figure 9-28 shows the oscilloscope capture of the current through the high-side PMOS of phase 1 and phase 2, respectively, and the voltage across the high-side PMOS (V_{SD}) for the Two Phase PWM Buck Converter at a switching frequency of 100 kHz. The oscilloscope captures make conceptual sense because when the high-side PMOS is on, then the V_{SD} is zero with the current through the PMOS rising linearly.

Just like the Two Phase Zero-Voltage-Switching Buck Converter, the current through the high-side PMOS was measured through a pair of 2 m Ω surface mount current sense resistors for a nominal equivalent resistance of 1 m Ω . A differential probe was used to measure across the current sense resistors because the differential math function of two

passive probes does not provide enough resolution to make any quantitative analysis. The data points were then extracted from the oscilloscope capture and the switching trajectory of the high-side PMOS of phase 1 and phase 2 were generated in Microsoft Excel.

The resultant high-side PMOS switching trajectory of phase 1 and phase 2 are shown below in Figure 9-27 and Figure 9-29, respectively. The switching trajectory graphs closely mirrors what is expected above from Figure 2-3 in Chapter 2. The switching trajectory does not closely follow the x-axis and y-axis like in the Two Phase Zero-Voltage-Switching Buck Converter. Instead, the switching trajectory makes a box outline with two of the box's side being the x-axis and y-axis of the graph. The further the switching trajectory is away from the x-axis and y-axis, then the greater the power loss because the area under the curve in quadrant 1 is the power loss of the buck converter.

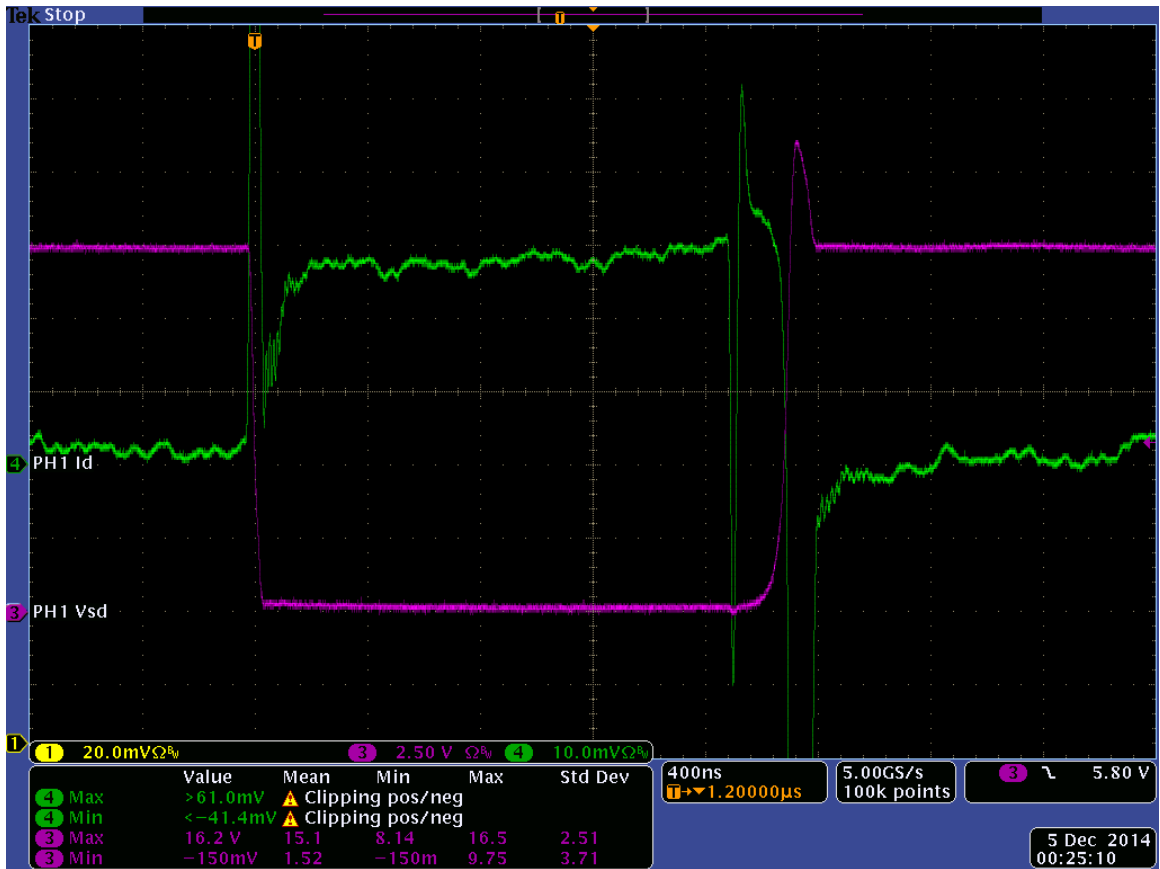


Figure 9-26: Phase 1 Switching Trajectory Waveform of Two Phase PWM Buck Converter at 100kHz

Two Phase PWM Buck Converter Switching Trajectory

VIN = 12.0V | VOUT = 1.5V | IOU = 40A | F_{sw} = 100kHz | Phase 1
Upper MOSFET

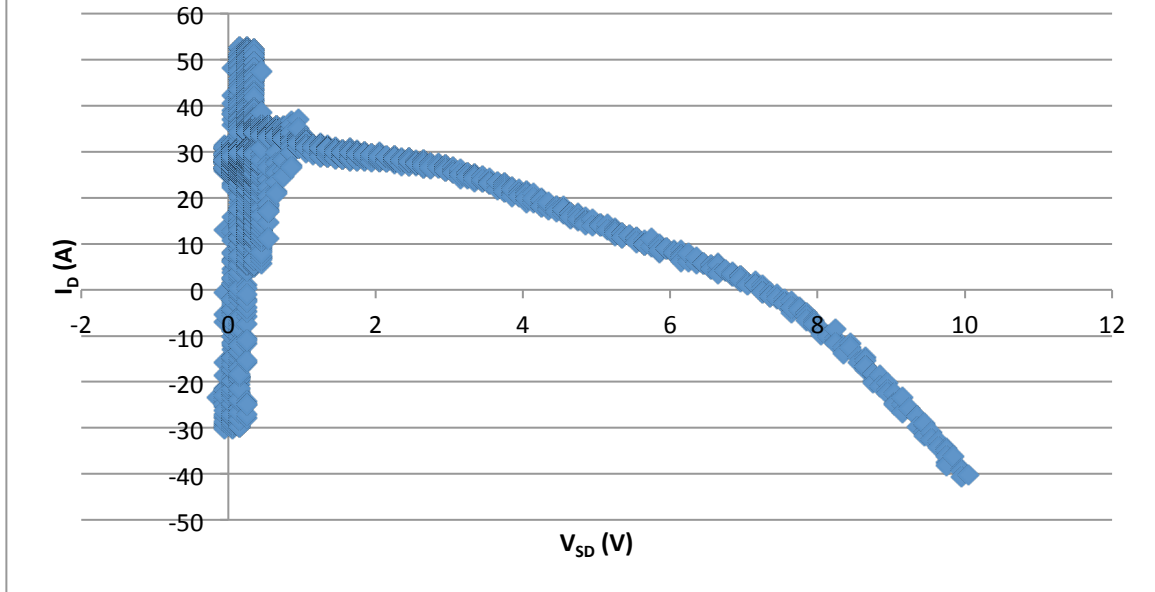


Figure 9-27: Phase 1 Switching Trajectory of Two Phase PWM Buck Converter at 100kHz

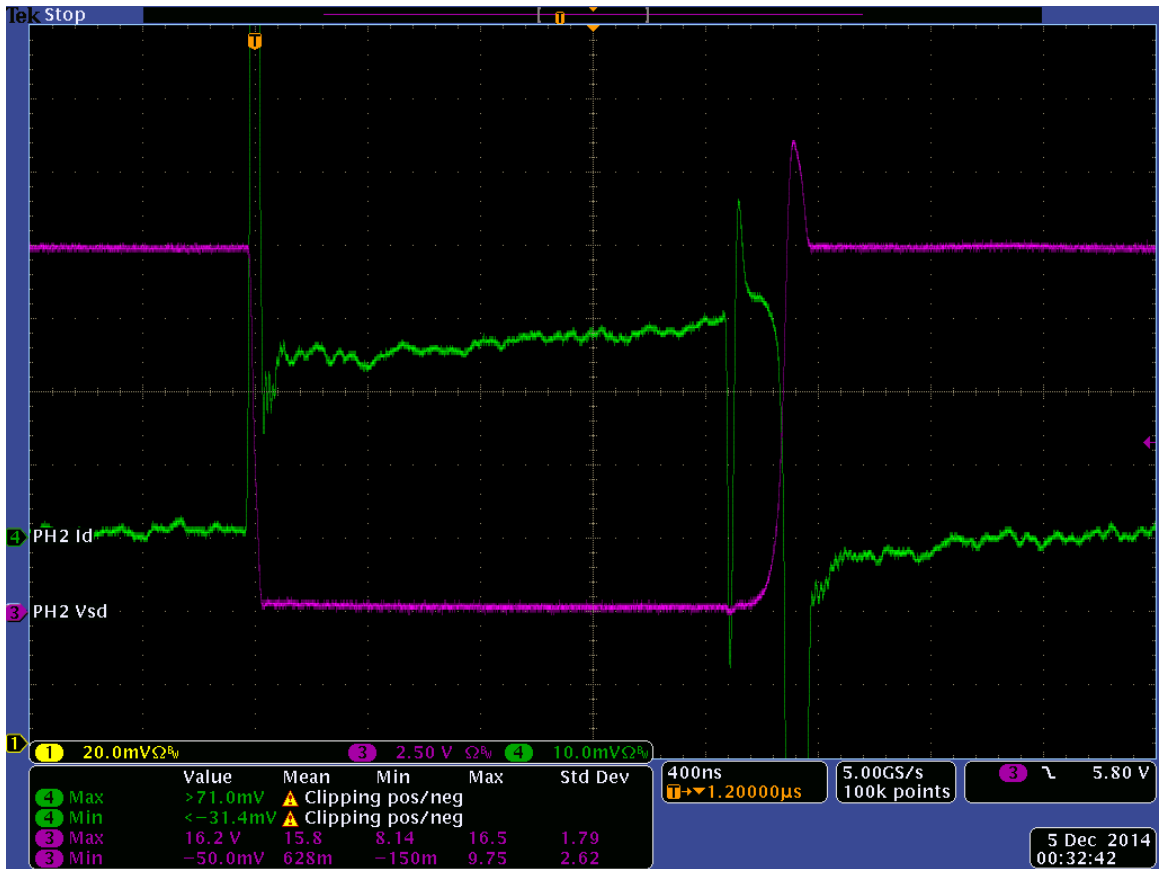


Figure 9-28: Phase 2 Switching Trajectory Waveform of Two Phase PWM Buck Converter at 100kHz

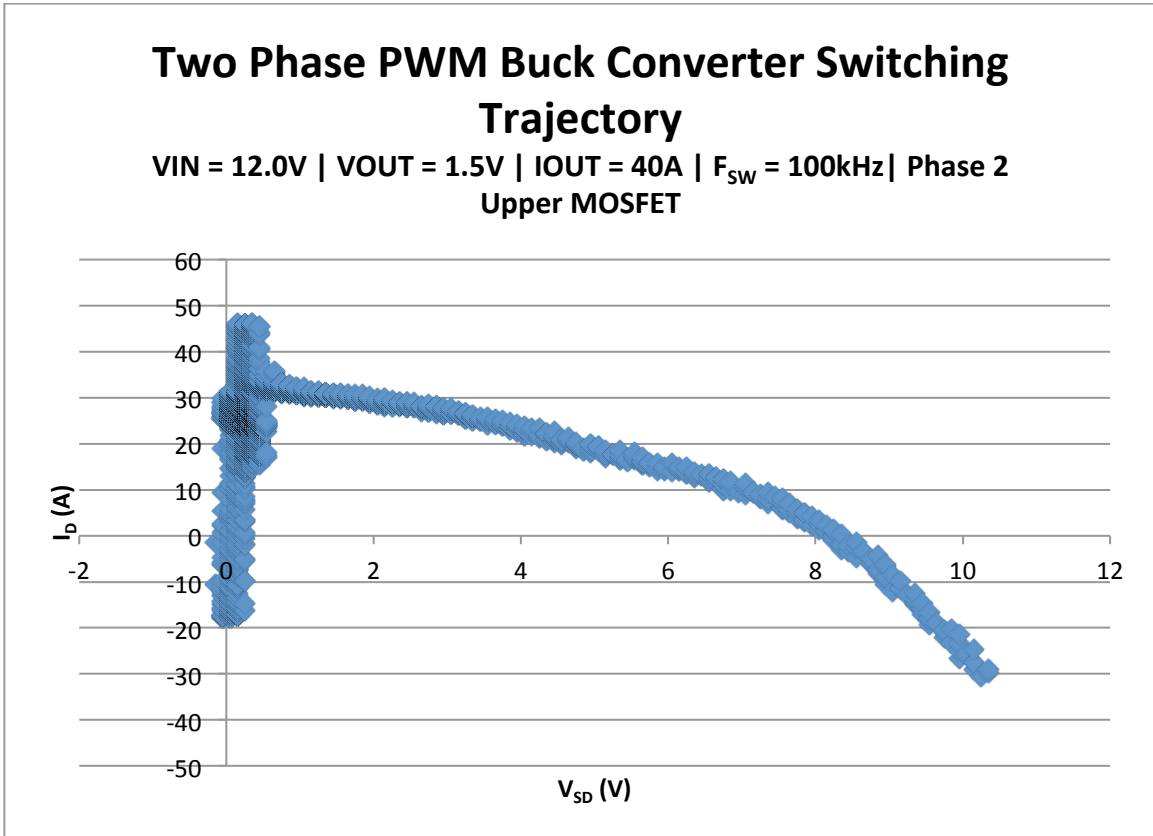


Figure 9-29: Phase 2 Switching Trajectory of Two Phase PWM Buck Converter at 100kHz

9.3 Hardware Troubleshooting

9.3.1 Minimum Required Load Current

It can be deduced from the efficiency data the Two Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter cannot maintain its output voltage for light current load conditions. From a conceptual standpoint, the important portion of the switching cycle to notice is time period 1 (T_1). It is between t_0 and t_1 that energy transfer occurs between the input and output. The resonant inductor cannot change its current flow direction instantaneously, but can only discharge its energy by continuing the flow of current to the output capacitors and the resonant capacitor. The energy is diffused between the output capacitors and the resonant capacitor. Given the large input capacitance, the large output capacitance, and lack of a soft start algorithm, the output capacitors are charged to the

same voltage as the input voltage capacitors. Typically to control the output voltage, the duty cycle can be reduced and it will limit the input current from reaching the output. Unfortunately, the dsPIC30F2020 requires at least 64 clock cycles (one clock cycle is 1.61ns) for the PID control loop to be stable. As a result, the minimum duty cycle will still have 103.04 ns of on time regardless of the frequency with higher frequencies having less effective duty cycle and vice versa. Ideally, the controller should let the output voltage drop down to its regulation voltage. However in a no load condition, the frequency has hit the minimum limit to maintain PID control loop stability for the dsPIC30F2020. Ideally, the leakage resistance of the capacitors should discharge the capacitors and reduce the output capacitance, but the operational characteristics of time period 1 and the high output capacitance will not let the output voltage drop unless a significant amount of load current is drawn from the Two Phase ZVS-QR Buck Converter.

In addition, there needs to be a minimum load current in order for the Two Phase ZVS-QR Buck Converter to maintain output voltage regulation. This is directly related to the characteristic impedance of the Two Phase ZVS-QR Buck Converter. The resonant capacitor equation will be used to determine the minimum load current.

$$C_r = \frac{1}{\omega_o Z_R} = \frac{I_{O,min}}{\omega_o V_{IN}} \quad (9-13)$$

Rearranging the coefficients to solve for the minimum load current will result in the following equation:

$$I_{O,min} = C_r \omega_o V_{IN} \quad (9-14)$$

For the 100 kHz switching frequency condition with the resonant frequency at 118 kHz, a resonant capacitor of 1.8 μF , a resonant inductor of 1.0 μH , and an input voltage of 12.0 V, the minimum load current is approximately 16.01 A.

For the 820 kHz switching frequency condition with the resonant frequency at 1.19 MHz, a resonant capacitor of 0.18 μF , a resonant inductor of 0.1 μH , and an input voltage of 12.0 V, the minimum load current is approximately 16.15 A. Keep in mind the minimum load current of 16.15 A is only per phase. As a two phase design, the minimum load current is approximately 32.0 A. As discussed previously, the ZVS-QR has demonstrated its ability to successfully maintain a good output voltage regulation down to 22 A.

9.3.2 Voltage of High-Side PMOS Current Sense Resistors

It was very difficult to obtain the voltage across the current sense resistors. The two conflicting factors were the power rating of the resistors and the resolution of the measurement. In order to obtain meaningful measurements, the resistance should be high as to gain voltage granularity, but the increased resistance will exceed the power rating of the current sense resistor.

The other option would be to insert wire loops and use a current probe that clamps around the wire with a ferrite core and measure the magnetic field of the wire to calculate the current flow. However, inserting wire loops between the input voltage plane and the source side of the MOSFET introduced so much inductance into the board that the Two Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter was no longer able to regulate the output voltage at any meaningful load current.

A current sensing op amp was also implemented to only fall short due to the timing delay from the op amp. On the oscilloscope, the current sensing op amp's output voltage was slightly slowly than what was expected with the voltage across the high-side PMOS. Thus, the current sensing op amp could not be used either.

It really narrowed back down to using a current sensing resistor. The only available surface mount current sense resistor was a 2 W 2 m Ω resistor and placing two of the resistors in parallel allowed for an equivalent 4 W 1 m Ω . At full load approximately 20A flowing through each phase, the power loss of the resistor is only 0.4 W. However, if the load current was applied too long and the current sense resistor in series with the high-side PMOS, then the high-side PMOS would somehow become electrically overstressed and cease to operate. Even though the calculations showed the current sense resistors should be able to handle the current capacity, it was oversized as a safety precaution because of the PMOS behavior when the current sense resistors were introduced into the circuit.

As for the measurement of the voltage across the current sense resistor, a differential probe must be used. The passive probes could only zoom into the waveform until it reached a maximum of a 100 mV/div. With a full expected range of 20 mV, a 100 mV/div was not enough to obtain quality data for analysis. The differential probe allowed the waveform to be zoomed in up to 10 mV/div. This allowed at least 2 divisions of useful data analysis. The only concern was the ability to discern between the noise and the actual waveform. Luckily at the lower frequencies, the parasitic components of the current sense resistor did not play a large role. This can be seen when comparing Figure 9-18 (100 kHz) and Figure 9-22 (820 kHz). Figure 9-18 shows a much cleaner voltage

equivalent current waveform than Figure 9-22. This is most likely due to the parasitic packaging series inductance and parallel capacitance. The frequency response of the non-ideal resistor is at first 0 dB gain (resistive behavior), followed by a -20 dB/dec drop (capacitive behavior), and then a +20 dB/dec ramp (inductive behavior). The 820 kHz frequency must be right at the capacitive behavior region which makes the resistor act like a low pass filter.

The measurement procedure of the current sense resistor was also immensely important. The wires connecting the differential probe to the current sense resistor must not be too long and must be twisted together as to reduce the parasitic inductance of the wire – which can greatly affect the measurements. Luckily, the current sense resistor was large enough that metal male headers were used instead so it was a two-fold benefit: it reduced the length of the measurement medium to a minimum and it eliminated any parasitic inductance from the loops two wires create. This technique is illustrated in Figure 9-30.



Figure 9-30: Method used to measure voltage across the current sense resistor with differential probes of Two Phase PWM Converter

9.3.3 RC Snubber Circuit

During the design of the buck converters, the adjustment of the gate turn on time was not taken into account. Thus, the ability to slow down the turn on time of the PMOS was not implemented into the PCB design. The reason a MOSFET may want to be slowed down is to limit phase node ringing.

Usually, this is done with a series resistor between the MOSFET driver and the gate of the MOSFET. Unfortunately, there is no gate resistor footprint allocated on the PCB, so a RC snubber must be used at the phase node to ground. The reason a power supply designer would want to limit ringing on the phase node because the ringing voltage's

peak value can be twice as much as the expected steady state voltage. Not only does the voltage have a positive peak during the turn on of the MOSFET, but it will also have a negative peak during the turn off of the MOSFET. Thus, to prevent overstressing the MOSFET and cause interference with nearby circuits and traces, an effort should be made to eliminate ringing from the phase node of a buck converter.

Below lists the steps to follow in order to properly select the resistor and capacitor values for the RC snubber.

- 1) Measure the phase ringing frequency.
- 2) Add capacitance across the freewheeling diode until the ringing frequency has dropped in half.
- 3) Calculate the parasitic capacitance by dividing the capacitance value in step 2 by 3.
- 4) Calculate the parasitic inductance from the following equation.

a.
$$L_P = \frac{1}{C_P * (2\pi f)^2} \quad (9-15)$$

- 5) Calculate the characteristic impedance from the following equation.

a.
$$Z = \sqrt{\frac{L_P}{C_P}} \quad (9-16)$$

- 6) Select a snubber resistor with a resistance value equal to the characteristic impedance.
- 7) Select a snubber capacitor with the same capacitance value used in step 2.
- 8) Calculate the power loss in the snubber resistor to ensure power rating is adequate.

a.
$$P = f_S * C_S * V^2 \quad (9-17)$$

- i. $f_S = \text{switching frequency}$

ii. $C_S = \text{snubber capacitor}$

iii. $V = \text{input voltage}$

Figure 9-31 shows the phase node ringing of the Two Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter as step 1 of the RC snubber component selection process. Figure 9-32 exemplifies the result with a capacitor chosen that satisfies step 2s criteria. Figure 9-33 illustrates the final result of the phase node with a properly selected RC snubber network. Comparing Figure 9-31 and Figure 9-33, we can see dramatic improvement of the phase node ringing. The RC snubber network which reduces the phase node ringing on the Two Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter is a 26Ω resistor and a 3300 pF capacitor.

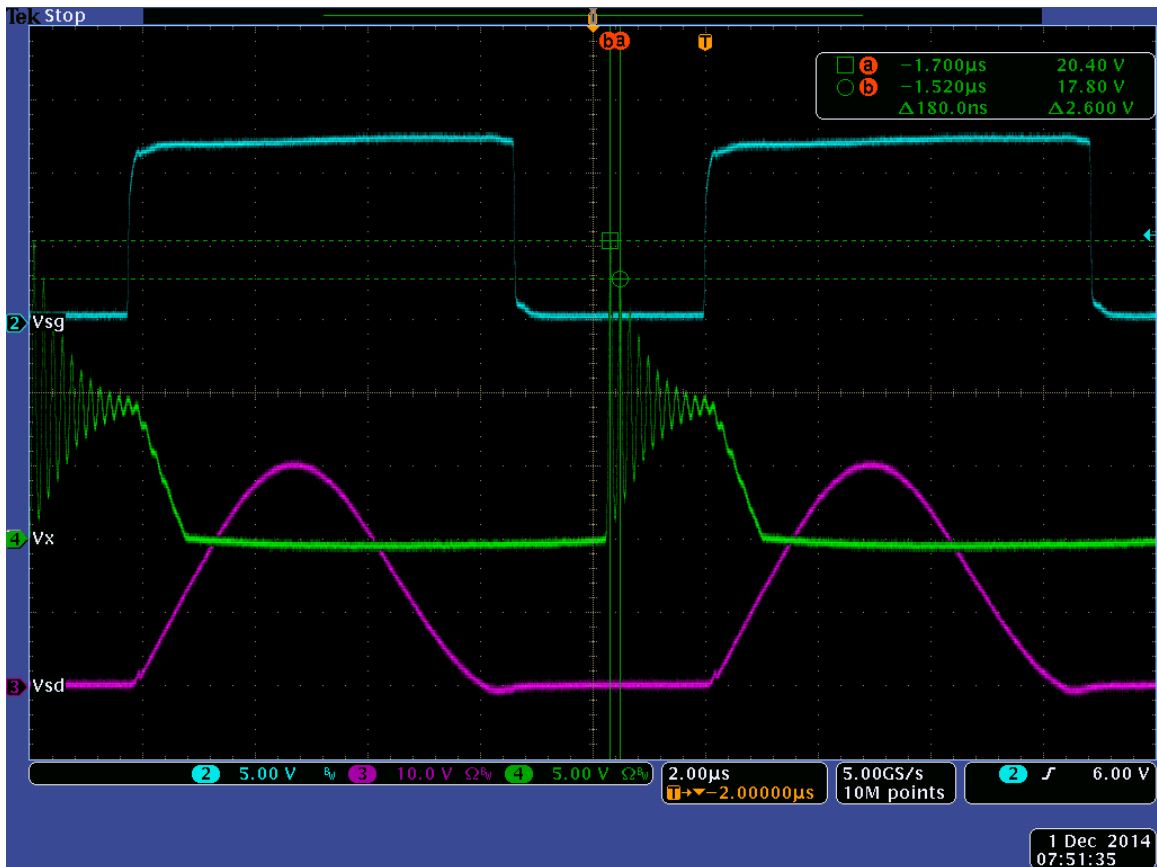


Figure 9-31: Phase Node Ringing Baseline for Two Phase PFM Zero-Voltage-Switching Quasi-Resonant Converter at 100kHz

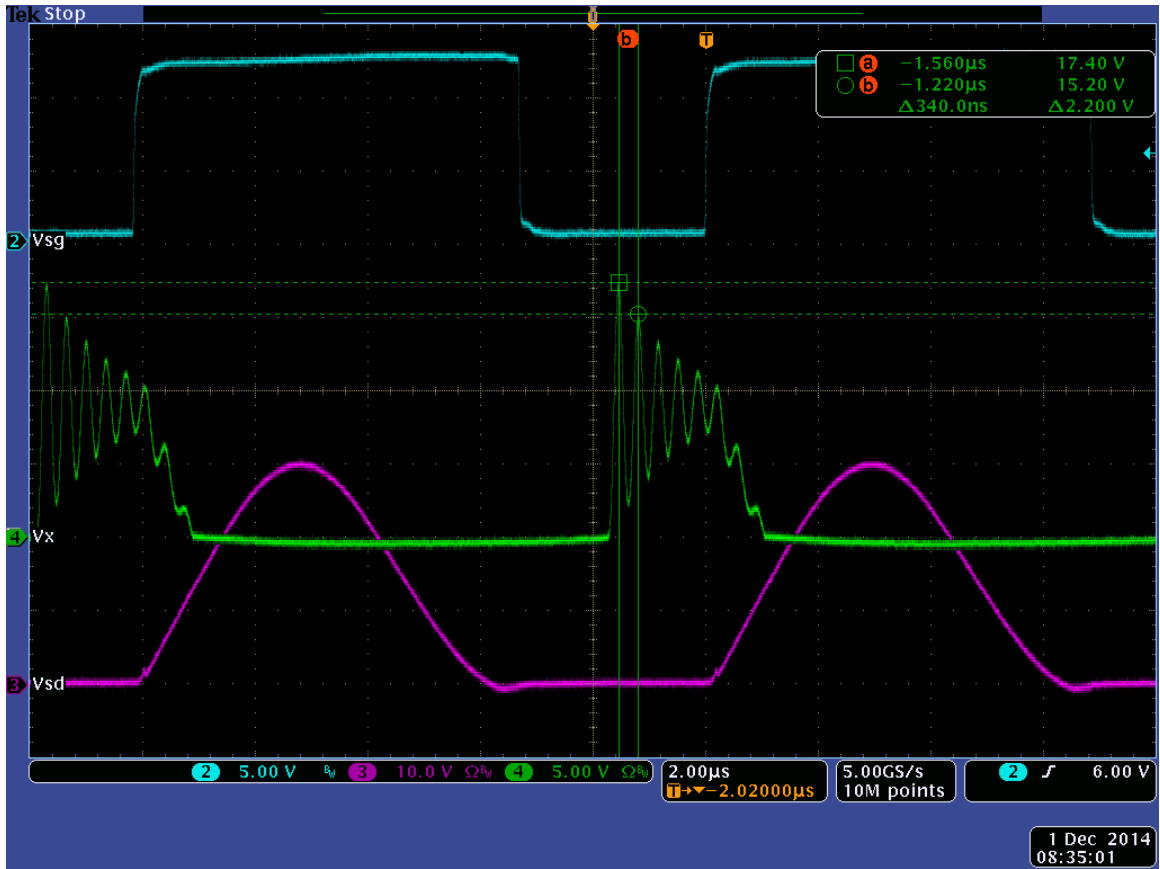


Figure 9-32: RC Snubber Tuning with 3300pF Capacitor for Two Phase PFM Zero-Voltage-Switching Quasi-Resonant Converter at 100kHz

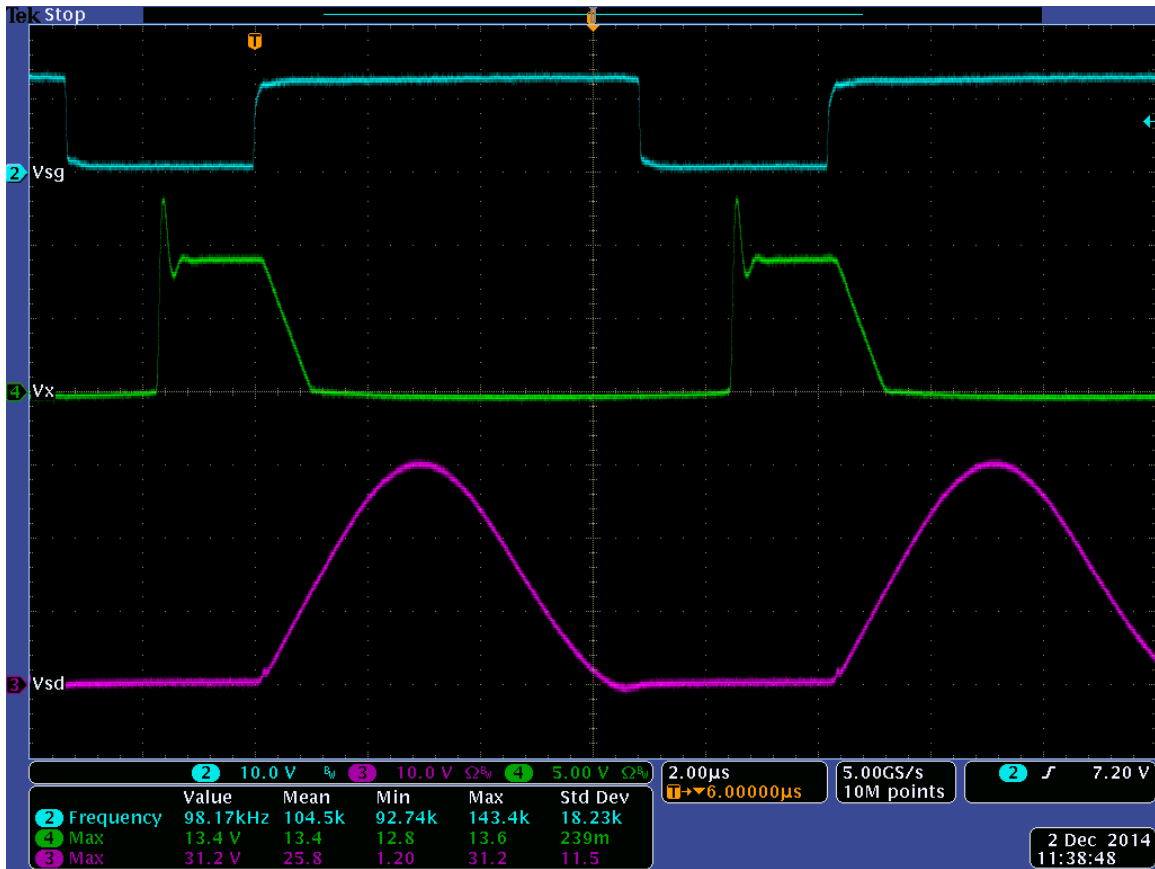


Figure 9-33: Phase Node with RC Snubber (R=16Ohm and C=3300pF) for Two Phase PFM Zero-Voltage-Switching Quasi-Resonant Converter at 100kHz

9.3.4 Component Value Selection for a Switching Frequency of 820kHz

For the Two Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter when the switching frequency is changed, the resonant components must be recalculated. Bear in mind the resonant frequency must be higher than the switching frequency. However, the selection of the components will be slightly different due to the massive increase in switching frequency. The selection of components will hinge on the ability for the Two Phase ZVS-QR Buck Converter to have a minimum output current less than the full load current and the resonant frequency has to be higher than the switching frequency. Therefore, one attempt to overcome this is by decreasing the resonant capacitor and inductor back a factor of 10. This results in a resonant capacitor of 0.18 μF and a resonant

inductor of 0.1 μH . A component decrease of a factor of 10 will result in the same characteristic impedance as the 100 kHz switching frequency components.

$$Z_o = \sqrt{\frac{L_r}{C_r}} = \sqrt{\frac{0.1\mu\text{H}}{0.18\mu\text{F}}} \quad (9-18)$$

$$Z_o = 0.74536\Omega \quad (9-19)$$

$$\omega_o = \frac{1}{\sqrt{L_r C_r}} = \frac{1}{\sqrt{0.1\mu\text{H} * 0.18\mu\text{F}}} \quad (9-20)$$

$$\omega_o = 7453559.925 \text{ rad/sec} \quad (9-21)$$

The minimum load current the Two Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter is able to sustain is given by the equation from section 9.3.1.

$$I_{o,min} = C_r \omega_o V_{IN} = 0.18\mu\text{F} * 7453559.925 \text{ rad/sec} * 12.0\text{V} \quad (9-22)$$

$$I_{o,min} = 16.09967 \text{ A/phase} \quad (9-23)$$

With a minimum load current of 16A/phase, then the first criteria stated earlier in this section is satisfied. The next criterion to satisfy is the resonant frequency.

$$f_o = \frac{\omega_o}{2\pi} = \frac{17453559.925 \text{ rad/sec}}{2\pi} \quad (9-24)$$

$$f_o = 1.18627\text{MHz} \quad (9-25)$$

The resonant inductor and resonant capacitor selection has satisfied both criteria stated earlier in this section. The next step in the design is to determine the timing parameters from equations derived in section 3 for each portion of the resonant cycle. This will provide a starting point to tune the off time to maximize the switching frequency and PMOS dead time. Completing the calculations for an 820 kHz switching frequency, the following timing parameters are found.

$$t_1 = 0.108\mu s \quad (9-26)$$

$$t_2 = 0.650\mu s \quad (9-27)$$

$$t_3 = 0.982\mu s \quad (9-28)$$

$$t_4 = 1.220\mu s \quad (9-29)$$

Figure 9-34 has the oscilloscope screen capture of the phase 1 switching waveforms with the same RC snubber network implemented from the switching frequency of 100 kHz. It shows that the Two Phase ZVS-QR Buck Converter operates at slightly higher than 820 kHz, but all the expected switching waveform behaviors are present.

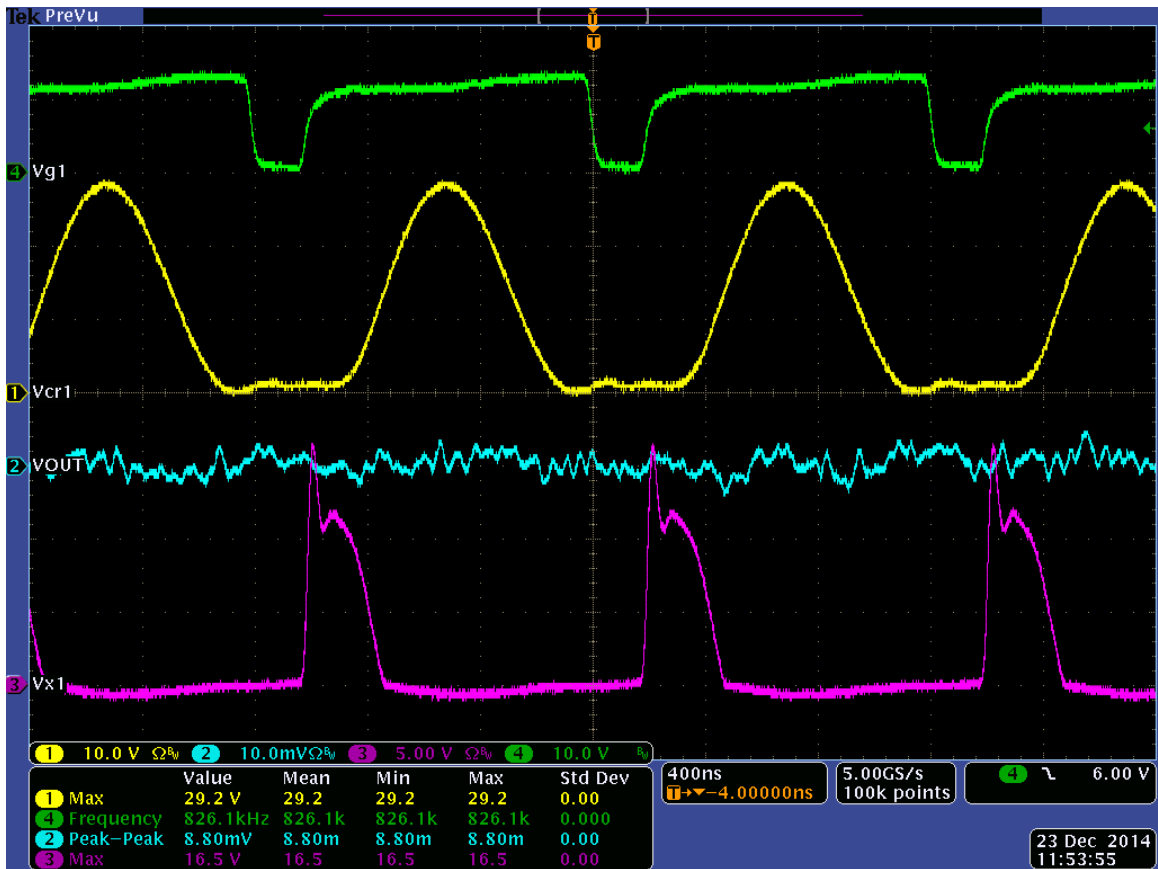


Figure 9-34: Phase 1 Switching Waveforms with RC Snubber (R=16Ohm and C=3300pF) for Two Phase PFM Zero-Voltage-Switching Quasi-Resonant Converter at 820kHz

9.3.5 Resonant Capacitor Component Selection

Although the capacitor value is determined to be 1.8 μF for a switching frequency of 100 kHz and 0.18 μF for a switching frequency of 820 kHz, the rated voltage is not the only parameter to emphasize. There are two factors which break capacitors: voltage and ripple current. In order to resist the destruction of capacitors through over voltage, the power supply designer will de-rate the capacitor by selecting a rated capacitor voltage double the expected voltage stress the capacitor will be subjected to. This allows for the capacitor to have the correct capacitance when it is operating in its desired operation conditions and to prevent over voltage electrical stress.

The second factor of excessive ripple current is solved by placing more capacitors in parallel in order to distribute the current load among multiple capacitors. The more ripple current the capacitor is subjected to, the higher the temperature the capacitor will generate. A very useful graph to pay attention towards is the Ripple Temperature Rising graph attached in Figure 9-33. This graph explains for a given ripple current in A_{RMS} and a specific switching frequency, then the capacitor's temperature will rise by a specific degree in Celsius. Referencing Figure 9-33 for a capacitor at a switching frequency of 1 MHz and a ripple current of 436 mA, the capacitor's temperature will rise by 20°C over the ambient temperature. If the ripple current is 1.744 A, then the capacitor's temperature will rise by 80°C over the ambient temperature.

Since the resonant capacitor has the tendency to have the highest component temperature on the PCB during operation, the resonant capacitor will be sized very generously. For a switching frequency of 820 kHz, the resonant capacitor is calculated to be 0.18 μF . However, the capacitor value of 0.18 μF can be obtained through a single capacitor or multiple capacitors in parallel to add up to 0.18 μF . In the case of using the

TDK CGA4J3X7R2E103K125AA, which has a capacitance of 10 nF, 18 capacitors can be placed in parallel to generate the desired 0.18 μ F resonant capacitor's value. The capacitor is a X7R temperature coefficient and has a maximum operating temperature of 125°C. If the maximum temperature is set to 125°C and the PCB is operating in a room with an ambient temperature of 25°C, then the capacitor has a margin of temperature rise of 100°C. The margin temperature rise is divided by the capacitor temperature rising and a factor of 5 is determined. This concludes for a single capacitor, it can handle 2.18 A of ripple current while having a capacitor temperature of 125°C. If the number is multiplied by the number of capacitors in parallel, then the current capacitor of the equivalent resonant capacitor is greatly increased. With 18 capacitors in parallel, the resonant capacitors are able to theoretically withstand 39.24A of ripple current while having a capacitor temperature of 125°C. Referring to Figure 3-2 during the high-side PMOS' off time, the resonant capacitor is subjected from a positive output load current value to a negative output load current value. Assuming an output load current value of 20 A for a single phase, that is 40 A of peak to peak current flowing through the resonant capacitors. However, Figure 9-35 is the ripple current in RMS and assuming a switching frequency of 1MHz – which is far greater than the switching frequency of 820 kHz, so the value to be concerned of will be much less than the expected 40 A of peak to peak current. As a result, the design of 18 TDK CGA4J3X7R2E103K125AA capacitors in parallel to create a resonant capacitor value of 0.18 μ F has the proper design.

Figure 9-36 shows the construction of the 18 capacitors in parallel. The reason for stacking so many capacitors is to save PCB real estate in the x-y plane. Due to the fact this PCB will not be manufactured in an assembly line, building components on top of

each other in the z-plane is feasible. Figures 9-37 through Figure 9-39 show the schematics of the Two Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter, while Figures 9-40 and 9-41 depict the front and back of the finished printed circuit board of the Two Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter.

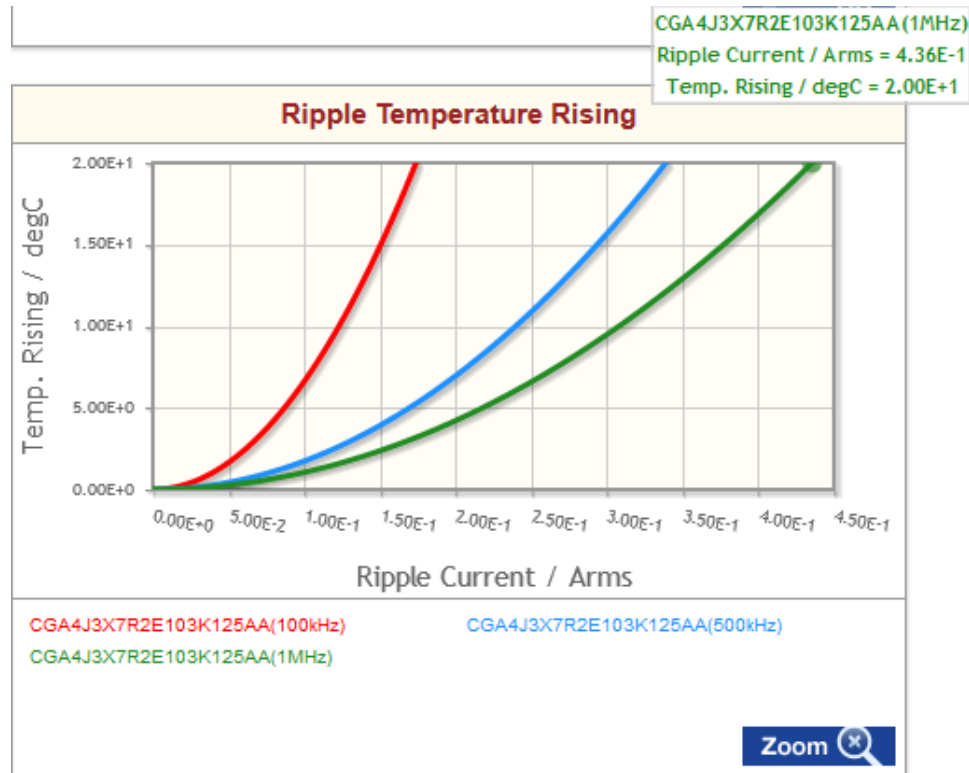


Figure 9-35: Ripple Temperature Rising chart of the TDK CGA4J3X7R2E103K1125AA operating at 1MHz

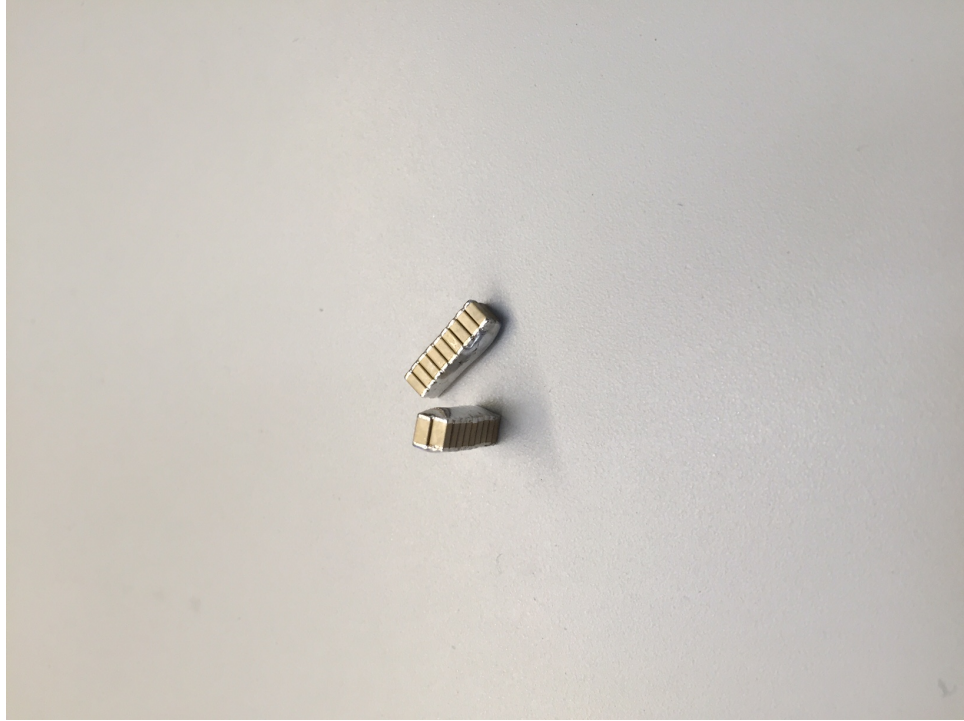


Figure 9-36: Construction of 18 TDK CGA4J3X7R2E103K1125AA capacitors in parallel to create the resonant capacitor of $0.18\mu\text{F}$

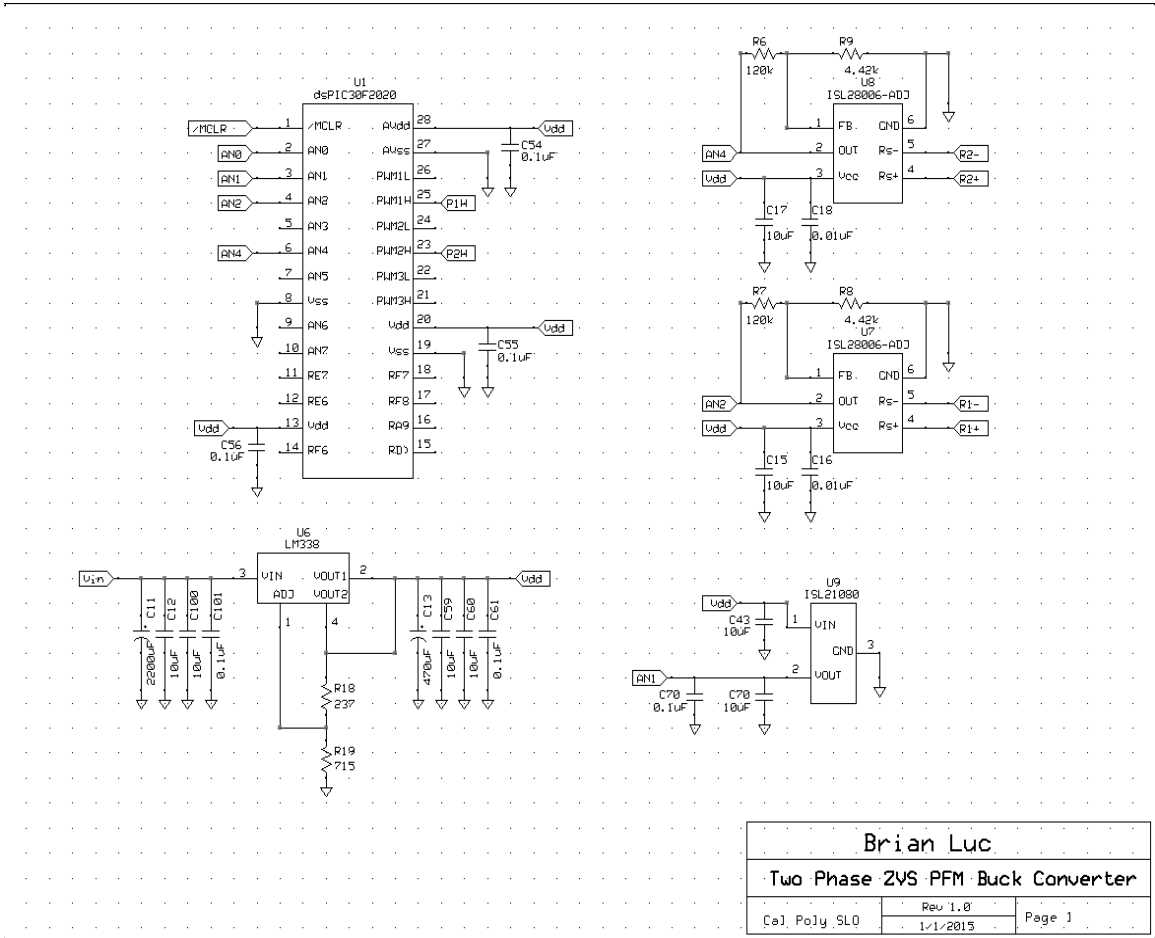


Figure 9-37: Schematic of Control PIC, Current Sense Op-Amp, Voltage Reference, and LDO (Page 1)

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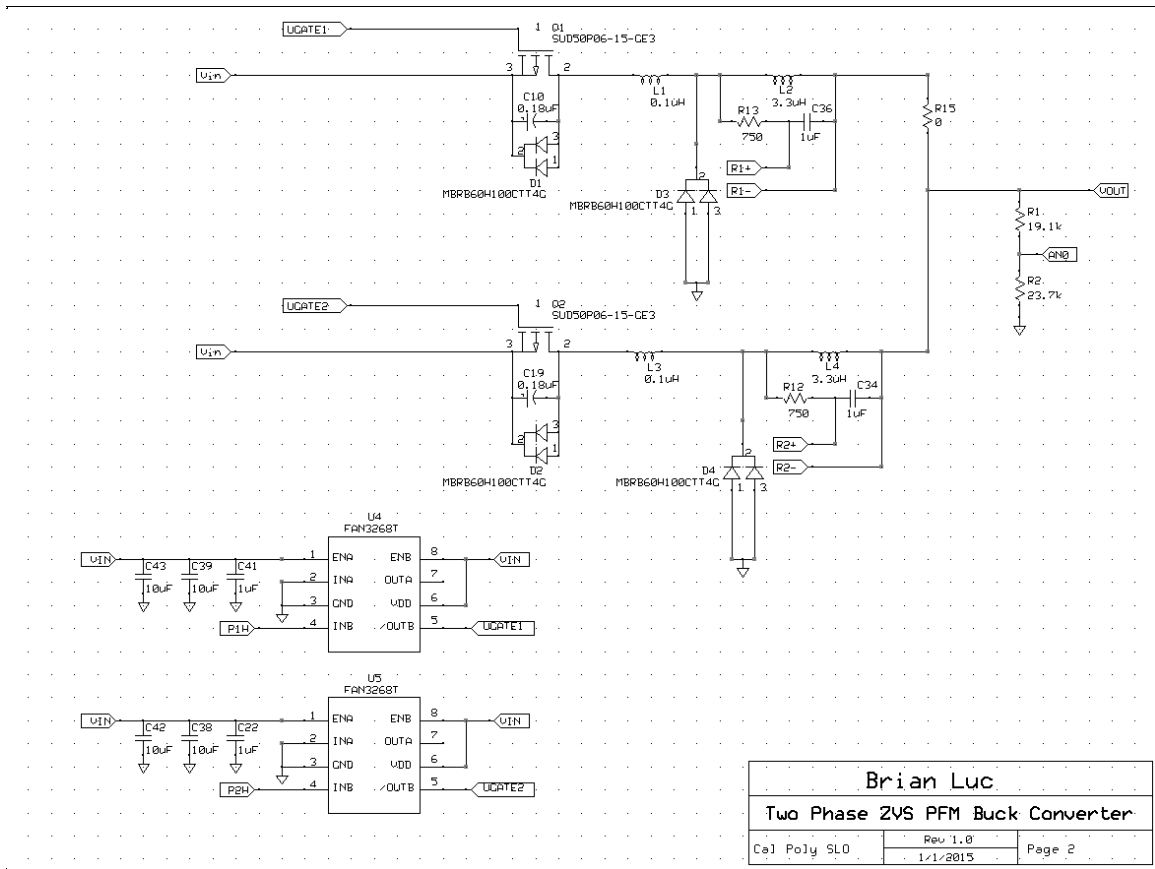


Figure 9-38: Schematic of Power Stage and PMOS High-Side Driver (Page 2)

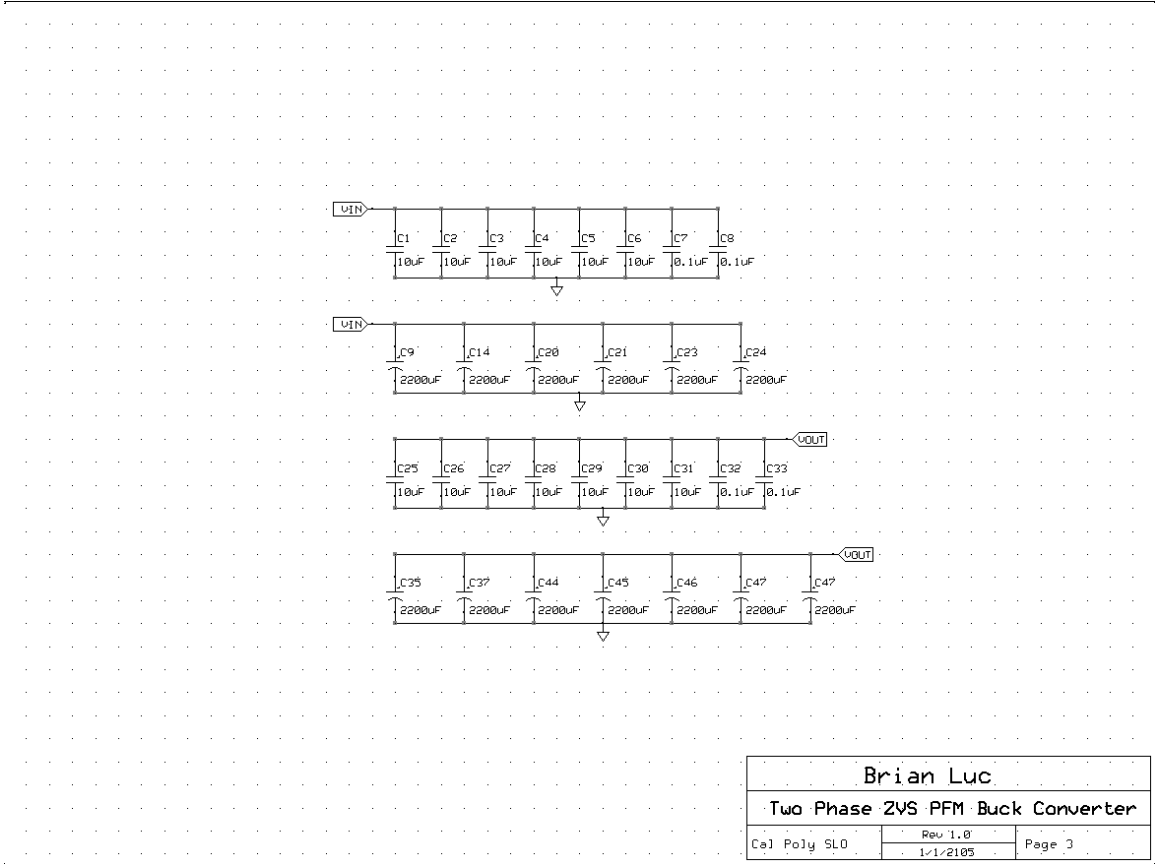


Figure 9-39: Schematic of Input and Output Capacitors of the Power Stage (Page 3)

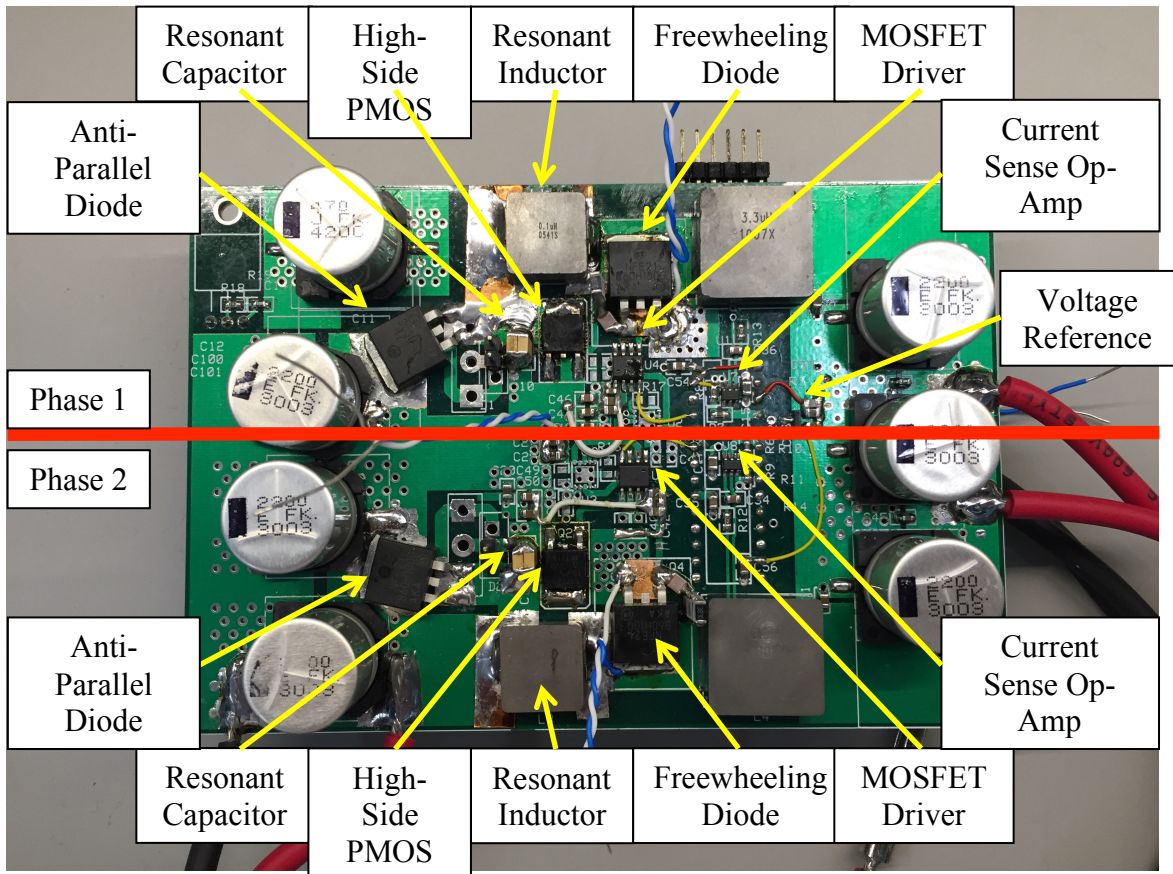


Figure 9-40: Front Picture of the Two Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter PCB

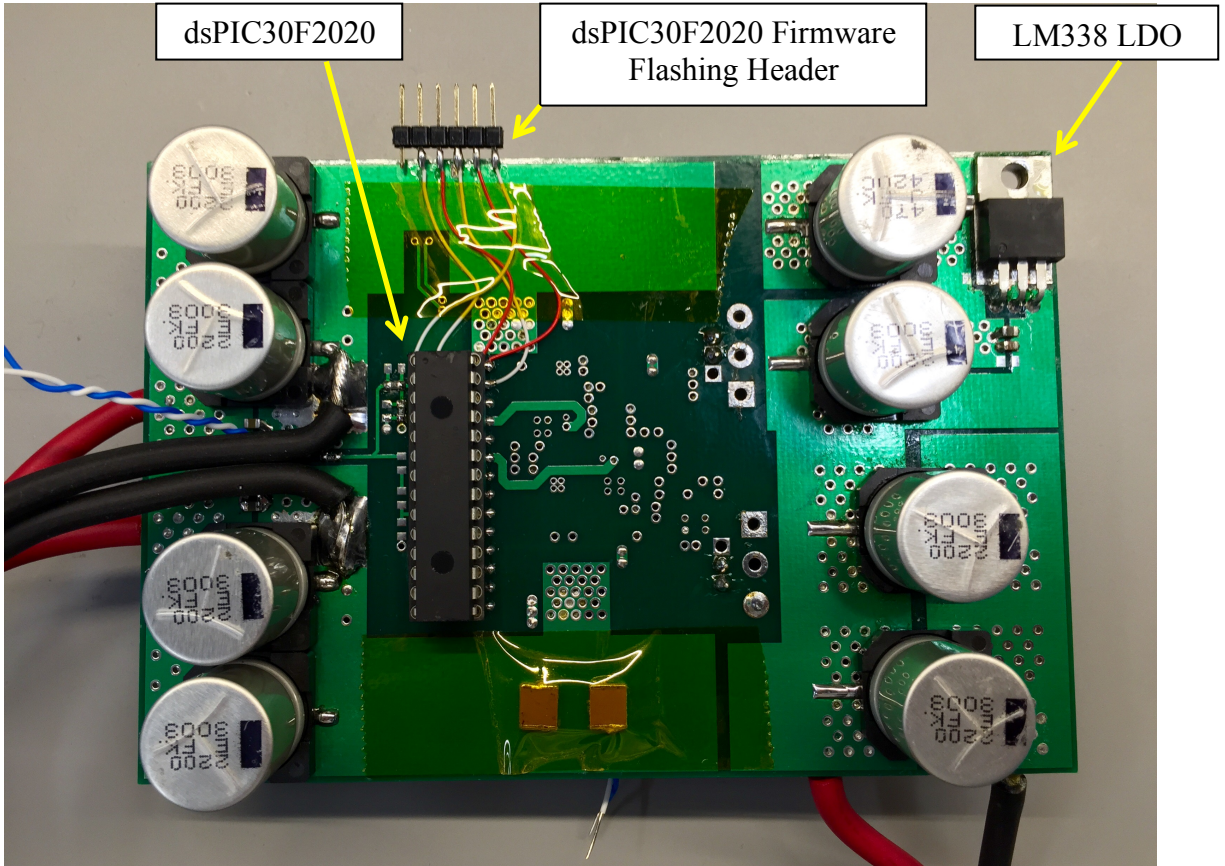


Figure 9-41: Back Picture of the Two Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter PCB

10. Conclusion and Further Work

The main goal of a power supply is to provide a stable regulated output voltage across all output load currents while maintaining maximum efficiency throughout its load condition. In general, power supply designers must compromise between cost, performance, size and efficiency. In the never ending quest towards obtaining maximum efficiency from a power supply circuit, the Two Phase Zero-Voltage-Switching Quasi Resonant Buck Converter with Digital Control implementation in this thesis was designed, built, and tested to several requirements.

Efficiency measurements conducted on the Two Phase ZVS-QR reveal the switching frequency at which the converter becomes beneficial to implement. Any switching frequencies above 500 kHz will begin to reap efficiency benefits. Many buck converters do not operate at such frequencies with high load current outputs because of the efficiency penalty of higher switching losses. It is impressive to observe that the Two Phase ZVS-QR Buck converter only loses 1.81% compared to the traditional Two Phase PWM Buck Converter of 15.41% in efficiency loss across a switching frequency from 100 kHz to 820 kHz. In addition, it completes this while maintaining less than 5% peak-to-peak voltage ripple, load regulation, and line regulation – even though the design requirements specify less than 1%. The one major downside to the Two Phase ZVS-QR Buck Converter is its inability to maintain output voltage regulation at no load condition. This means that there must always be some load current in order for the Two Phase ZVS-QR Buck Converter to maintain output voltage regulation. This lack of regulation at no load is mainly caused by the absence of resonance occurring between the resonant capacitor and inductor when the output is not pulling any current.

The next criteria to discuss are cost and size. It was found that these two criteria are where the Two Phase ZVS-QR Buck Converter has a severe disadvantage. Since the converter relies on resonant operation, the operational voltage and current waveforms are much higher than the traditional Two Phase PWM Buck Converter. Thus, the components must be rated higher than normal which directly correlates to the physical footprint size on the PCB and component costs. With higher footprint sizes comes more difficulty in finding board space to fit the solution. It can be clearly seen from the complete PCB solution, the inductors and capacitors are by far the largest and tallest components on the board – minus the PIC controller dsPIC30F2020. With the industry always looking for the smallest solution possible to reduce their final product form factor and meet their design requirements, having a large physical footprint size on the PCB is a very difficult attribute to overlook. In addition, the added cost of slightly more and higher rated components is definitely the biggest shortcoming because the increase in board solution cost will directly impact the final product's market price. With the market always striving for the most benefit from the lowest cost solution, it will be difficult to rationalize the usage unless under extreme circumstances or in any applications where cost is not the major driving factor. For most applications, designers will sacrifice efficiency in order to keep the cost of the design to a minimal because that increase in cost is passed down to the consumer in the final price of the converter.

For future improvements on the Two Phase ZVQ-QR Buck Converter, it is recommended to implement NMOS instead of PMOS high-side MOSFET switches because of its inherent lower R_{DS-on} and ability to operate much better at higher switching frequencies. This is one reason for the relatively low overall efficiency of the converters

tested in this thesis. Another solution to further reduce the R_{DS-on} is to parallel more high-side MOSFET switches because it reduces the R_{DS-on} by the number of high-side MOSFET switches. The decrease in the R_{DS-on} is crucial with this topology due to its relatively large peak switch current.

Another improvement to increase the efficiency of the Two Phase Zero-Voltage-Switching Quasi-Resonant Buck Converter is to eliminate the freewheeling diode and to implement a low-side MOSFET switch (synchronous switch). This will dramatically improve efficiency because the voltage loss across the low-side MOSFET switch is only a quarter of the voltage loss due to the forward conducting voltage of the freewheeling diode. The voltage loss across the low-side MOSFET switch will only be the current through the switch times the R_{DS-on} of the switch. Though the voltage across the low-side MOSFET switch is scaled proportionally to the current through the switch, the total voltage across the switch is lower than the forward conducting voltage of the freewheeling diode. The only caveat is the control algorithm to adjust the turn on of the low-side MOSFET switch at the beginning of t_3 .

The benefit of using a digital controller compared to using an analog controller is the flexibility and ease of adaptation for the system design parameters. Typically, there is an input for each feature of the analog controller, such as constant off time, soft start, or switching frequency. Most of the features are implemented with resistors and capacitors creating timing circuits. Unfortunately, the resistors and capacitors do take up valuable board space. In addition, for changing a feature such as the switching frequency, an analog controller requires a physical change of a resistor, but a digital controller simply requires a change in the line of code and then re-flashing the microcontroller. A

disadvantage of using the digital controller is its complexity. In order to implement the digital controller, thorough knowledge of the microcontroller is required and also the ability to construct C-code. When the digital controller does not operate as intended, there is no ability to use an oscilloscope and probe the specific building block to determine its input and output signals to find the problem and create a solution. Everything in a digital controller is code and logic based. With an analog controller, the designer is able to probe the input and output of specific building blocks to determine if the desired signal is present. An analog controller makes debugging the circuit much easier. As a result, an improvement of the digital controller would be the ability to output to a serial terminal on the host computer the status of certain bits within the microcontroller. This is similar to that of debugging regular software code with print statements to determine if the code flow is operating as intended.

One test that will be useful to perform as part of future work is to compare the noise (EMI and harmonics) produced by the Two Phase ZVS-QR Buck converter with that of the regular Two Phase Buck converter. It is expected that the resonant Buck will produce less noise and harmonics which makes it suitable for applications requiring high-efficiency and low noise power supplies.

In summary, this thesis demonstrates the viability of the Two Phase Zero Voltage Switching Quasi Resonant Buck converter as an alternative topology for the regular Two Phase Buck converter. Merits and drawbacks of the resonant buck have been discussed as observed from simulation and hardware test results. Knowing these will be a very important step for power supply designers to determine whether this resonant topology is suitable for their load or customer requirements.

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Appendices

A: C-Code Two Phase PWM Operation

```
#include "p30F2020.h"
#include "dsp.h"
#include "math.h"

/* Configuration Bit Settings */
_FOSCSEL(FRC_PLL)
_FOSC(CSW_FSCM_OFF & FRC_HI_RANGE & OSC2_CLKO & HS_EC_DIS)
_FWDT( FWDTEN_OFF & WINDIS_ON & WDTPRE_PR128 & WDTPOST_PS32768 )
_FPOR(PWRT_128)
_FGS( CODE_PROT_OFF & GWRP_OFF )
_FBS(BSS_NO_FLASH)

typedef signed int SFRAC16;

#define Q15(X) ((X < 0.0) ? (int)(32768*(X) - 0.5) : (int)(32767*(X) + 0.5))

#define MAX_DUTY_CYCLE 2965 // may be 0.4744

unsigned int scaled_val;
unsigned int duty_cycle_comp;
signed long int currentAverage;
signed long int measured_output;
extern float Fract2Float (fractional);
void setup(void);

// Constants used by the PID controller, since a MAC operation is used, the PID structure is changed
SFRAC16 ControlDifference[3] __attribute__((__space__(xmemory), __aligned__(4)));
SFRAC16 PIDCoefficients[3] __attribute__((__space__(ymemory), __aligned__(4)));

SFRAC16 ControlOutput; // Output
SFRAC16 ControlReference; // Desired value
SFRAC16 ControlFeedback; // Actual value, that will generate the error

/* Variable Declaration required for each PID controller in your application */
/* Declare a PID Data Structure named, fooPID */
tPID fooPID;
/* The fooPID data structure contains a pointer to derived coefficients in X-space and */
/* pointer to controler state (history) samples in Y-space. So declare variables for the */
/* derived coefficients and the controller history samples */
fractional abcCoefficient[3] __attribute__((section (".xbss, bss, xmemory")));
fractional controlHistory[3] __attribute__((section (".ybss, bss, ymemory")));
/* The abcCoefficients referenced by the fooPID data structure */
/* are derived from the gain coefficients, Kp, Ki and Kd */
/* So, declare Kp, Ki and Kd in an array */
fractional kCoeffs[] = {0,0,0};

void init_PWM(void)
{
    PTPER = 6250; // PWM Period = 10 usec @ 20 MIPS for 100kHz */
}
```

/ 1.05nsec for Industrial and 1.61nsec for Extended */
/* Refer to PWM section for more details */*

/ Initialize PWM Generator 1 */*

IOCON1bits.PENH = 1; */* PWM Module controls High output */*
IOCON1bits.PENL = 1; */* PWM Module controls Low output */*
IOCON1bits.POLH = 0; */* High Output Polarity is active High */*
IOCON1bits.POLL = 0; */* Low Output Polarity is active High */*
IOCON1bits.PMOD = 0; */* Complimentary output mode */*
IOCON1bits.OVRENH = 0; */* High Output Override disabled */*
IOCON1bits.OVRENL = 0; */* Low Output Override disabled */*

TRGCON1bits.TRGDIV = 0; */* Trigger on every event */*
TRGCON1bits.TRGSTRT = 0; */* Start the counting at the start */*

TRIG1 = 200; */* Trigger event at 0.214 usec from start of the PWM cycle */*

PWMCON1bits.FLTSTAT = 0; */* Clear Fault Interrupt flag */*
PWMCON1bits.CLSTAT = 0; */* Clear Current Limit Interrupt flag */*
PWMCON1bits.TRGSTAT = 0; */* Clear PWM Trigger Interrupt flag */*
PWMCON1bits.FLTIE = 0; */* Disable Fault Interrupt */*
PWMCON1bits.CLIEN = 0; */* Disable Current Limit Interrupt */*
PWMCON1bits.TRGIEN = 0; */* Disable Trigger Interrupt */*
PWMCON1bits.ITB = 0; */* Time base is read from PTMR */*
PWMCON1bits.MDCS = 0; */* Duty cycle is read from PDC */*
PWMCON1bits.DTC = 0; */* DTC=0: Postive dead time actively applied for all output*

*modes */*

PWMCON1bits.XPRES = 0; */* No extenal reset for PTMR */*
PWMCON1bits.IUE = 0; */* Immediate update to PDC */*

DTR1 = 160; */* Deadtime = DTR1*1.61nsec = 257.6nsec */*
ALTDTR1 = 160; */* Deadtime = ALTDTR*1.61nsec = 257.6nsec */*

PDC1 = 128; */* Start with a Ton value of 0.137usec */*
PHASE1 = 0; */* No phase shift */*

/ Initialize PWM Generator 2 */*

IOCON2bits.PENH = 1; */* PWM Module controls High output */*
IOCON2bits.PENL = 1; */* PWM Module controls Low output */*
IOCON2bits.POLH = 0; */* High Output Polarity is active High */*
IOCON2bits.POLL = 0; */* Low Output Polarity is active High */*
IOCON2bits.PMOD = 0; */* Complimentary output mode */*
IOCON2bits.OVRENH = 0; */* High Output Override disabled */*
IOCON2bits.OVRENL = 0; */* Low Output Override disabled */*

TRGCON2bits.TRGDIV = 0; */* Trigger on every event */*
TRGCON2bits.TRGSTRT = 0; */* Start the counting at the start */*

TRIG2 = 200; */* Trigger event at 0.214 usec from start of the PWM cycle */*

PWMCON2bits.FLTSTAT = 0; */* Clear Fault Interrupt flag */*
PWMCON2bits.CLSTAT = 0; */* Clear Current Limit Interrupt flag */*
PWMCON2bits.TRGSTAT = 0; */* Clear PWM Trigger Interrupt flag */*
PWMCON2bits.FLTIE = 0; */* Disable Fault Interrupt */*

```

PWMCON2bits.CLIEN = 0;      /* Disable Current Limit Interrupt */
PWMCON2bits.TRGIEN = 0;    /* Disable Trigger Interrupt */
PWMCON2bits.ITB   = 0;    /* Time base is read from PTMR */
PWMCON2bits.MDCS = 0;    /* Duty cycle is read from PDC */
PWMCON2bits.DTC   = 0;    /* DTC=0: Postive dead time actively applied for all output
modes */
PWMCON2bits.XPRES = 0;    /* No extenal reset for PTMR */
PWMCON2bits.IUE = 0;     /* Immediate update to PDC */

DTR2 = 160;               /* Deadtime = DTR1*1.61nsec = 257.6nsec */
ALTDTR2 = 160;           /* Deadtime = ALTDTR*1.61nsec = 257.6nsec */

PDC2 = 128;              /* Start with a Ton value of 0.137usec */
PHASE2 = PTPER/2;       /* Phase shift of half of the PWM period */

/* Intialize the ADC */

ADPCFG = 0xFFE8;        /* AN0, AN1, AN2, and AN4 are analog inputs */
ADCONbits.ADCS = 5;    /* Clock Divider is set up for Fadc/14 */
ADCONbits.FORM = 0;    /* Output in Integer Format */
ADCONbits.SEQSAMP = 1; /* Sequential Sampling Enabled */
ADCONbits.ORDER = 0;  /* Even channel first */
ADPC0bits.TRGSRC0 = 0x4; /* Trigger conversion on PWM#1 Trigger for AN0 and AN1
*/

ADCONbits.ADSIDL = 0;   /* Operate in Idle Mode */
ADCONbits.EIE = 1;     /* Enable Early Interrupt */
ADSTAT = 0;           /* Clear the ADSTAT register */
ADPC0bits.IRQEN0 = 1;  /* Enable the interrupt for AN0 and AN1 */
ADCONbits.ADON = 1;    /* Start the ADC module */

/* Set up the Interrupts */

IPC2bits.ADIP = 4;     /* Set ADC Interrupt Priority */
IFS0bits.ADIF = 0;    /* Clear AD Interrupt Flag */
IEC0bits.ADIE = 1;    /* Enable the ADC Interrupt */

PTCON = 0x8000;       /* Enable PWM Module */

while(1);
}

void __attribute__((interrupt, no_auto_psv)) _ADCInterrupt()
{
    IFS0bits.ADIF = 0; /* Clear ADC Interrupt Flag */
    ADSTATbits.PORDY = 0; /* Clear the ADSTAT bits */

    fooPID.controlReference = Q15(ADCBUF1/1024.0); /* Set the Reference which is 0.8V
from the VREF LDO */

    fooPID.measuredOutput = Q15(ADCBUF0/1024.0); /* Scale measured output
to fractional format. */

    PID(&fooPID); /* Call the PID controller using the new measured
input */
}

```

```

        if( fooPID.controlOutput > Q15(0.0) )
        {
            scaled_val = __builtin_mulsu(fooPID.controlOutput, MAX_DUTY_CYCLE) >> 15;
        }
        else
        {
            scaled_val = 0;
        }
        if( scaled_val < 64 )
        {
            scaled_val = 64; // see errata for min. duty cycle
        }

        PDC1 = scaled_val;
        PDC2 = scaled_val;
    }

int main(void)
{
    fooPID.abcCoefficients = &abcCoefficient[0]; //Set up pointer to derived coefficients */
    fooPID.controlHistory = &controlHistory[0]; //Set up pointer to controller history samples */
    PIDInit(&fooPID); //Clear the controller history and the controller output */

    kCoeffs[0] = Q15(0.4); // Kp + Ki + Kd must be < 0.99999
    kCoeffs[1] = Q15(0.2); // Kp + 2*Kd must be < 1.000
    kCoeffs[2] = Q15(0);
    PIDCoeffCalc(&kCoeffs[0], &fooPID); //Derive the a,b, & c coefficients from the Kp, Ki &
    Kd */

    init_PWM();

    while(1);
}

```

B: C-Code Two Phase PWM Operation

```

#include "p30F2020.h"
#include "dsp.h"
#include "math.h"

/* Configuration Bit Settings */
_FOSCSEL(FRC_PLL)
_FOSC(CSW_FSCM_OFF & FRC_HI_RANGE & OSC2_CLKO & HS_EC_DIS)
_FWDT( FWDTEN_OFF & WINDIS_ON & WDTPRE_PR128 & WDTPOST_PS32768 )
_FPOR(PWRT_128)
_FGS( CODE_PROT_OFF & GWRP_OFF )
_FBS(BSS_NO_FLASH)

typedef signed int SFRAC16;

#define Q15(X) ((X < 0.0) ? (int)(32768*(X) - 0.5) : (int)(32767*(X) + 0.5))

#define MIN_FREQ 12422 // lowest frequency is 50kHz at 1.61nsec clock.

```

```

unsigned int scaled_val;
signed long int measured_output;
extern float Fract2Float (fractional);
void setup(void);

// Constants used by the PID controller, since a MAC operation is used, the PID structure is changed
SFRAC16 ControlDifference[3] __attribute__((__space__(xmemory), __aligned__(4)));
SFRAC16 PIDCoefficients[3] __attribute__((__space__(ymemory), __aligned__(4)));

SFRAC16 ControlOutput; // Output
SFRAC16 ControlReference; // Desired value
SFRAC16 ControlFeedback; // Actual value, that will generate the error

/* Variable Declaration required for each PID controller in your application */
/* Declare a PID Data Structure named, fooPID */
tPID fooPID;
/* The fooPID data structure contains a pointer to derived coefficients in X-space and */
/* pointer to controller state (history) samples in Y-space. So declare variables for the */
/* derived coefficients and the controller history samples */
fractional abcCoefficient[3] __attribute__((section(".xbss, bss, xmemory")));
fractional controlHistory[3] __attribute__((section(".ybss, bss, ymemory")));
/* The abcCoefficients referenced by the fooPID data structure */
/* are derived from the gain coefficients, Kp, Ki and Kd */
/* So, declare Kp, Ki and Kd in an array */
fractional kCoeffs[] = {0,0,0};

void init_PWM(void)
{
    PTPER = 4485; // PFM Period = 7.728 usec @ 20 MIPS for 129.4kHz */
// 1.61nsec for Extended */
// 1.05nsec for Industrial and
// Refer to PWM section for more details */

/* Initialize PWM Generator 1 */

IOCON1bits.PENH = 1; // PWM Module controls High output */
IOCON1bits.PENL = 1; // PWM Module controls Low output */
IOCON1bits.POLH = 1; // High Output Polarity is active LOW */
IOCON1bits.POLL = 1; // Low Output Polarity is active LOW */
IOCON1bits.PMOD = 0; // Complimentary output mode */
IOCON1bits.OVRENH = 0; // High Output Override disabled */
IOCON1bits.OVRENL = 0; // Low Output Override disabled */

TRGCON1bits.TRGDIV = 0; // Trigger on every event */
TRGCON1bits.TRGSTRT= 0; // Start the counting at the start */

TRIG1 = 200; // Trigger event at 0.214 usec from start of the PWM cycle */

PWMCON1bits.FLTSTAT = 0; // Clear Fault Interrupt flag */
PWMCON1bits.CLSTAT = 0; // Clear Current Limit Interrupt flag */
PWMCON1bits.TRGSTAT = 0; // Clear PWM Trigger Interrupt flag */
PWMCON1bits.FLTIE = 0; // Disable Fault Interrupt */
PWMCON1bits.CLIEN = 0; // Disable Current Limit Interrupt */

```

```

PWMCON1bits.TRGIEN = 0; /* Disable Trigger Interrupt */
PWMCON1bits.ITB = 0; /* Time base is read from PTMR */
PWMCON1bits.MDCS = 0; /* Duty cycle is read from PDC */
PWMCON1bits.DTC = 0; /* DTC=0: Postive dead time actively applied for all output
modes */
PWMCON1bits.XPRES = 0; /* No extenal reset for PTMR */
PWMCON1bits.IUE = 0; /* Immediate update to PDC */

DTR1 = 160; /* Deadtime = DTR1*1.61nsec = 257.6nsec
*/
ALTDTR1 = 160; /* Deadtime = ALTDTR*1.61nsec =
257.6nsec */

PDC1 = 4255; /* Constant off time of 6.55us */
PHASE1 = 0; /* No phase shift */

/* Initialize PWM Generator 2 */

IOCON2bits.PENH = 1; /* PWM Module controls High output */
IOCON2bits.PENL = 1; /* PWM Module controls Low output */
IOCON2bits.POLH = 1; /* High Output Polarity is active LOW */
IOCON2bits.POLL = 1; /* Low Output Polarity is active LOW */
IOCON2bits.PMOD = 0; /* Complimentary output mode */
IOCON2bits.OVRENH = 0; /* High Output Override disabled */
IOCON2bits.OVRENL = 0; /* Low Output Override disabled */

TRGCON2bits.TRGDIV = 0; /* Trigger on every event */
TRGCON2bits.TRGSTRT = 0; /* Start the counting at the start */

TRIG2 = 200; /* Trigger event at 0.214 usec from start of the PWM cycle */

PWMCON2bits.FLTSTAT = 0; /* Clear Fault Interrupt flag */
PWMCON2bits.CLSTAT = 0; /* Clear Current Limit Interrupt flag */
PWMCON2bits.TRGSTAT = 0; /* Clear PWM Trigger Interrupt flag */
PWMCON2bits.FLTIEEN = 0; /* Disable Fault Interrupt */
PWMCON2bits.CLIEN = 0; /* Disable Current Limit Interrupt */
PWMCON2bits.TRGIEN = 0; /* Disable Trigger Interrupt */
PWMCON2bits.ITB = 0; /* Time base is read from PTMR */
PWMCON2bits.MDCS = 0; /* Duty cycle is read from PDC */
PWMCON2bits.DTC = 0; /* DTC=0: Postive dead time actively applied for all output
modes */
PWMCON2bits.XPRES = 0; /* No extenal reset for PTMR */
PWMCON2bits.IUE = 0; /* Immediate update to PDC */

DTR2 = 160; /* Deadtime = DTR1*1.61nsec = 257.6nsec
*/
ALTDTR2 = 160; /* Deadtime = ALTDTR*1.61nsec =
257.6nsec */

PDC2 = 4255; /* Constant off time of 6.55us */
PHASE2 = PTPER/2; /* Phase shift of half of the PWM period */

/* Intialize the ADC */

ADPCFG = 0xFFE8; /* AN0, AN1, AN2, and AN4 are analog inputs */
ADCONbits.ADCS = 5; /* Clock Divider is set up for Fadc/14 */

```

```

ADCONbits.FORM = 0;      /* Output in Integer Format */
ADCONbits.SEQSAMP = 1;  /* Sequential Sampling Enabled */
ADCONbits.ORDER = 0;   /* Even channel first */
ADCPC0bits.TRGSRC0 = 0x4; /* Trigger conversion on PWM#1 Trigger for AN0 and AN1
*/

ADCONbits.ADSIDL = 0;   /* Operate in Idle Mode */
ADCONbits.EIE = 1;     /* Enable Early Interrupt */
ADSTAT = 0;            /* Clear the ADSTAT register */
ADCPC0bits.IRQEN0 = 1; /* Enable the interrupt for AN0 and AN1 */
ADCONbits.ADON = 1;    /* Start the ADC module */

/* Set up the Interrupts */

IPC2bits.ADIP = 4;     /* Set ADC Interrupt Priority */
IFS0bits.ADIF = 0;    /* Clear AD Interrupt Flag */
IEC0bits.ADIE = 1;    /* Enable the ADC Interrupt */

PTCON = 0x8000;       /* Enable PWM Module */

while(1);
}

void __attribute__((interrupt, no_auto_psv)) _ADCInterrupt()
{
    IFS0bits.ADIF = 0; /* Clear ADC Interrupt Flag */
    ADSTATbits.PORDY = 0; /* Clear the ADSTAT bits */

    fooPID.controlReference = Q15(ADCBUF1/1024.0); /* Set the Reference which is 0.8V
from the VREF LDO */

    fooPID.measuredOutput = Q15(ADCBUF0/1024.0); /* Scale measured output
to fractional format. */

    PID(&fooPID); /* Call the PID controller using the new measured
input */

    if( fooPID.controlOutput > Q15(0.0) )
    {
        scaled_val = __builtin_mulsu(fooPID.controlOutput, MIN_FREQ) >> 15;
    }
    else
    {
        scaled_val = 0;
    }
    if( scaled_val < 4485 )
    {
        scaled_val = 4485; /* see errata for min. duty cycle of 64 and dead time. Max Fsw
= 139.514kHz */
    }

    PTPER = scaled_val;
    PHASE2 = PTPER/2;
}

```

```

int main(void)
{
    fooPID.abcCoefficients = &abcCoefficient[0]; //Set up pointer to derived coefficients */
    fooPID.controlHistory = &controlHistory[0]; //Set up pointer to controller history samples */
    PIDInit(&fooPID); //Clear the controller history and the controller output */

    kCoeffs[0] = Q15(0.4); // Kp + Ki + Kd must be < 0.99999
    kCoeffs[1] = Q15(0.2); // Kp + 2*Kd must be < 1.000
    kCoeffs[2] = Q15(0);
    PIDCoeffCalc(&kCoeffs[0], &fooPID); //Derive the a,b, & c coefficients from the
    Kp, Ki & Kd */

    init_PWM();

    while(1);
}

```