AC POWER COMBINING STRATEGY

WITH

APPLICATION TO EFFICIENT LINEAR POWER AMPLIFIERS

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ABSTRACT

AC Power Combining Strategy with Application to Efficient Linear Power Amplifiers

Rudi Matthew Bendig

With the ongoing push for wireless systems to accommodate more users and support higher data rates more efficient modulation schemes have been created that are more advanced than simple FM and AM modulation used for radio broadcasting. These modulation schemes, such as orthogonal frequency division multiplexing (OFDM), suffer from high peak to average power ratios. Standard Class A and Class AB amplifiers cannot simultaneously achieve good linearity and efficiency, and therefore there has been an increase in the development of new topologies to combat this issue. Common features to these circuits is power combining of two or more separate transistors.

In this work, we consider various ways of two-source power combining and identify four topologies of interest. We notice that linear power-efficient amplifiers reported to date are based upon two of the identified combining strategies. We believe that no amplifiers have been reported that leverage the other two alternatives. This work produces a fully-functional amplifier based on one of these alternatives. The prototypes are intended to serve as concept verification of the architecture and hence are implemented at lower (1 MHz) frequencies.

Keywords: Two-source power amplifier, Peak to Average Power Ratio, Linear Power Amplifier

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1.1 Statement of Problem

With the ongoing push for wireless systems to accommodate more users and support higher data rates more efficient modulation schemes have been created that are more advanced than simple FM and AM modulation used for radio broadcasting. These modulation schemes, such as orthogonal frequency division multiplexing (OFDM), suffer from high peak to average power ratios. Standard Class A and Class AB amplifiers cannot simultaneously achieve good linearity and efficiency, and therefore there has been an increase in the development of new topologies to combat this issue.

1.2 Document Overview

This thesis deals with power combining. First we discuss the properties of 3 ideal power sources: voltage, current and negative resistance. Next we consider various configurations allowing power combining of two sources and notice four arrangements exhibiting the same desirable property – one of the sources behaves as a “master” determining the power to the load, while the second one behaves as a “helper”. We also notice that these four configurations always leverage different type of sources, so we discuss converting AC current sources into AC voltage sources using reactive networks. The next task is to explain how to create grounded and floating current sources to support our power combining strategy. Lastly, the background provides examples of types of narrow-band amplifiers that use two-source power combing strategies.

In the Circuit Theory and Design section, we outline a single transistor resonant amplifier that will serve as the basis for our design. The type of two-source power combining technique

used in this thesis is then explained. This method involves the series combining of a current source and voltage source.

The Implementation in Software section uses LTSpice to explain the circuits used to create the overall power combining design. The main concern of which is designing a practical floating current source by means of a differential pair. Furthermore, we explain the circuits designed to create the differential pair tail current, as well as the structures which provide the voltages needed to commutate the diff. pair.

The Prototyping section introduces the two circuit designs that we created to validate our two-source power combining technique. The section covers the components selected based upon the simulations made in the previous section, and the important data that was collected from the circuits.

The Component Sizing & Circuit Dangers section elucidates the important properties of the circuit and explains how the components must be selected to achieve the desired results. The section includes both simulation results and relevant circuit theory.

Finally, the Conclusion and Future work section names the steps we must take to make this design a commercial reality. Design choices were made to make proof of concept easier, while other optimizations are more relevant in a commercial setting.

2. Background

2.1 Types of Ideal Sources

This work outlines a novel AC power combining technique and therefore the types of sources used in the design must be readily understood to understand the overall design. In this first section we discuss three different types of ideal sources: Voltage, Current, and Negative Resistance (NR).

Voltage sources are among the most prevalent type of power sources. AC and DC sources are found in every household around the world. The wall outlet can be regarded as an AC voltage source. Batteries are DC voltage sources. The key aspect of an ideal voltage source is its zero output (Thevenin) resistance. A voltage source alone will not determine the current through itself; it is the load that determines the current. [7]

Ideal current sources are the opposite of voltage sources. The current through the source is determined solely by the device, but the voltage is dependent upon the components connected with the current source. Under certain operating conditions transistors, bipolar and MOS, can be regarded as voltage controlled **current sources.**

The last source, Negative Resistance, is more complex. A NR can only be present in a circuit with active components, and a NR behaves as both a source and an element as it has a phasor diagram. [15]The phasor diagram of a resistor and a negative resistor is depicted in Figure 2.1.

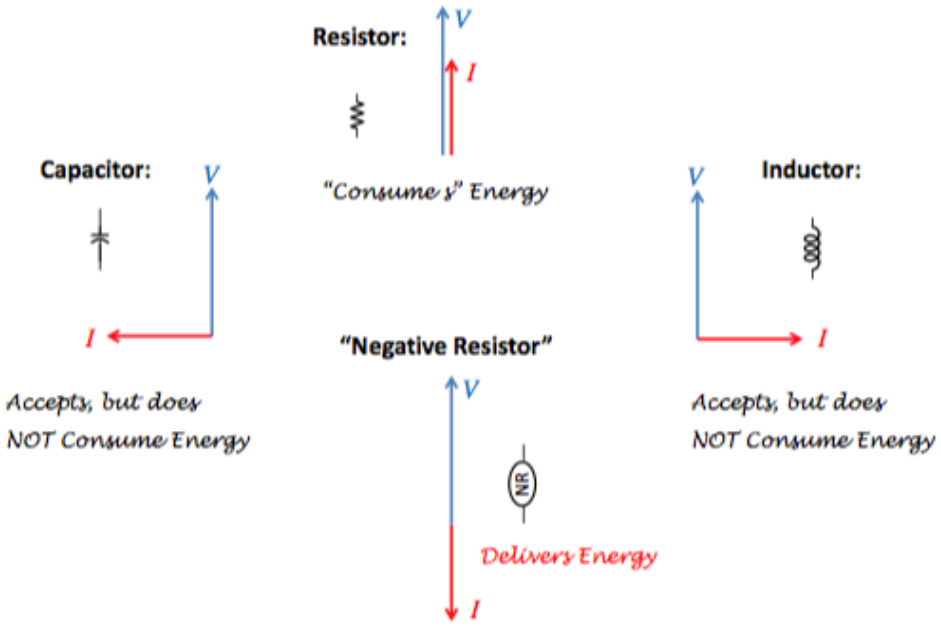


Figure 2.1: The four types of elements.NR can be shown to be both a source and an element because it can deliver power and has a phasor diagram. [15]

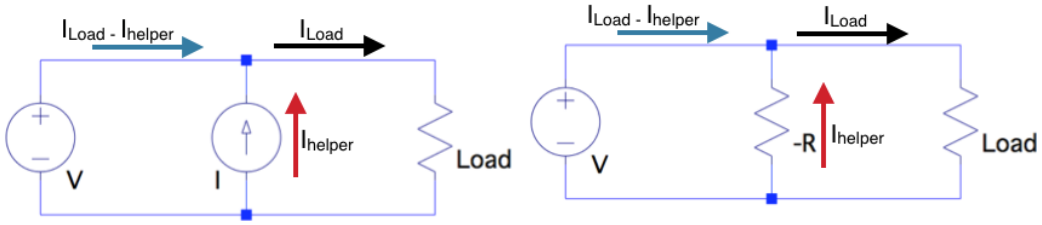
Unlike an ideal voltage or current source, a NR does not set a voltage or current, but instead provides a current when a voltage is applied. This means that a NR is dependent upon another source, and that the phase difference between the voltage and the current is 180 degrees, since the current will flow opposite to the applied voltage. Since a NR provides current in the opposite direction of the voltage, if a source is not present two possibilities arise. The first of which is no voltage is present across the negative resistance and therefore no current is sourced, and the element delivers no power. The second possibility is that some occurrence such as noise provides a voltage across the NR and in the presence of reactive components the NR sustains an oscillation. This property is thoroughly understood and used for many oscillator designs (Colpitts, Hartley).

2.2 Two-source Power Combining

Sources can be connected in series or in parallel to a load. Of the various combinations of two-sources, two combinations are disallowed: the combining of two voltage sources in parallel, as well as the combining of two current sources in series. These are disallowed because they violate Kirchoff's Voltage Law and Kirchoff's Current Law, respectively. Also, as discussed previously

networks with just negative resistors and loads will deliver zero power or oscillate with ever-increasing magnitude.

Of the remaining combinations of two sources, four are of particular interest and are shown in Figure 2.2 and Figure 2.3.In these combinations the left most source is considered the main source, and the second source is the helper source. The helper source is meant to assist the main source in power delivery *without* changing the power that the load would receive with only the main source.



a) b)

Figure 2.2: Parallel "master-helper" configurations. The master, the source that determines the power to the load, is the voltage source. See equation (2.3).

The relations governing the operation of both Figure 2.2 topologies are the same and given by:

$$V_{Load} = V \tag{2.1}$$

$$I_{Load} = V \times G_{Load} \tag{2.2}$$

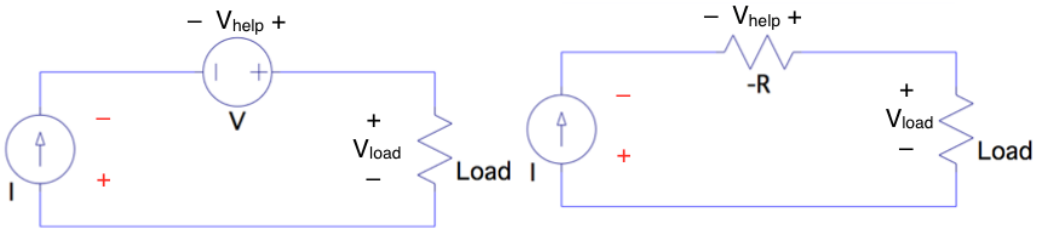
$$P_{Load} = V^2 \times G_{Load} \tag{2.3}$$

$$P_{from\,V} = V \times \left(I_{Load} - I_{help}\right) \tag{2.4}$$

For Figure 2.2 b) configuration we can also write:

$$P_{from\,V} = V^2 \times \left(G_{Load} - G_{NR}\right) \tag{2.5}$$

Here G_{NR} denotes the conductance of the negative-resistance component and G_{Load} denotes the conductance of the load.



a) b)

Figure 2.3: Series "master-helper" configurations. The master, the source that determines the power to the load, is the current source. (see expression 2.8)

The relations governing the operation of both Figure 2.3 topologies are the same and given by:

$$I_{Load} = I \tag{2.6}$$

$$V_{Load} = I \times R_{Load} \tag{2.7}$$

$$P_{Load} = I^2 \times R_{Load} \tag{2.8}$$

$$P_{from\,V} = I \times \left(V_{Load} - V_{help}\right) \tag{2.9}$$

For Figure 2.3 b) series configuration we can also write:

$$P_{from\,I} = I^2 \times \left(R_{Load} - R_{NR}\right) \tag{2.10}$$

Here R_{NR} denotes the value of the negative-resistance component and R_{Load} denotes the resistance of the load. Comparing the series configuration to the parallel configurations we notice their duality. The duality is apparent when equations 2.1, 2.2, 2.3, 2.4, and 2.5 are compared to 2.6, 2.7, 2.8, 2.9 and 2.10, respectively. In the Figure 2.2 a) and Figure 2.2 b) circuits the helper source should always deliver less current than the load demands:

$$I_{help} \leq I_{Load} \tag{2.11}$$

If the helper current exceeds the load current then the excess current will be wasted flowing through the voltage source. This condition is depicted in Figure 2.4. It is undesirable and it should be avoided.

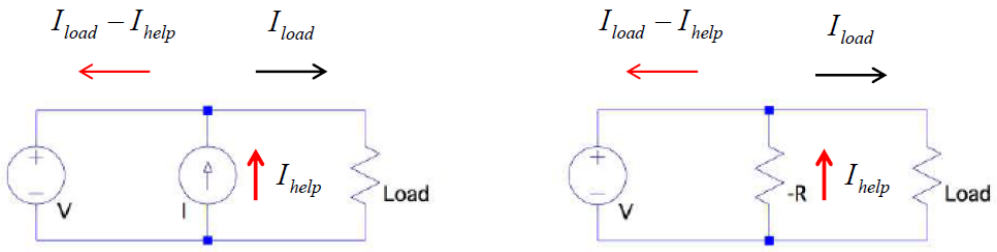


Figure 2.4: If the helper source exceeds the current demand of the load, the master source acts as a load and dissipates the excess power. This condition is highly undesirable and should be avoided.

To satisfy the current constraint (2.11), the negative conductance in Fig. 2b) must be less than the load conductance.

$$|G_{NR}| \leq G_{Load} \tag{2.12}$$

The helper source, in the Figure 2.3 circuits, should always deliver less voltage than the load demands:

$$V_{help} \leq V_{Load} \tag{2.13}$$

When condition (2.13) is violated the voltage across the master source reverses polarity. The master source then behaves as a load, dissipating excess power. This situation is illustrated in Figure 2.5.

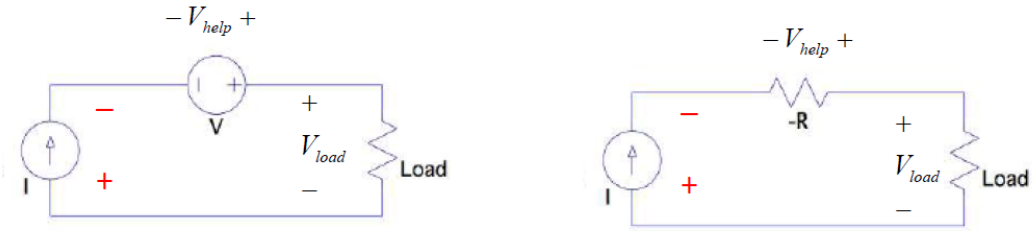


Figure 2.5: If the helper source exceeds the voltage demand of the load, the master source acts as a load and dissipates the excess power. This condition is highly undesirable and should be avoided.

To avoid polarity reversal in the Fig. 2.3b) circuit, one must keep the negative resistance small compared to the load resistance.

$$|R_{NR}| \leq R_{Load} \tag{2.14}$$

2.3 Converting an AC Current Source into an AC Voltage Source

Notice that the Figure 2.2 a) and Figure 2.3 a) topologies leverage two different sources – a voltage source and a current source. Hence, to use these topologies with a pair of voltage or a pair of current sources we must be able to convert a voltage source into a current source or vice versa. In the following, we will show that for AC sources, such a conversion is possible. The conversion requires the use of reactive components assembled into a suitable resonant network.

When a current source is placed in parallel with an impedance the voltage that develops across the resulting network is:

$$V = I_{Isource} \times Z_{impedance} \tag{2.15}$$

With the current converted to a voltage, an additional impedance is then placed in series with the parallel network to resonate out the original impedance.

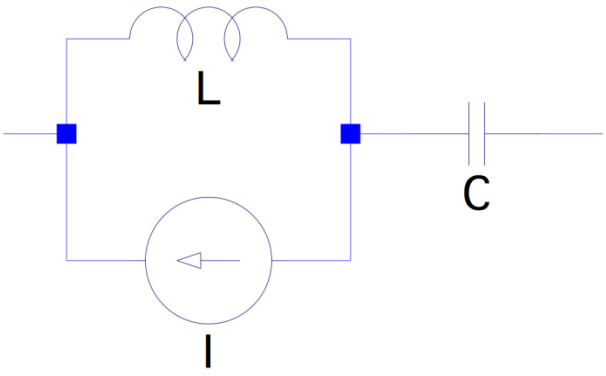


Figure 2.6: At the resonant frequency of L and C this circuit behaves as an ideal voltage source with value I × jX_L.

Figure 2.6shows an example of such a network. The inductor, L, presents an impedance of jwL to the current source and creates a voltage across its terminals with a ninety degree phase shift. The capacitor, C, is presented in series and has an impedance of -j/wC. The value of the inductor and capacitor are than chosen to create a resonant network at the desired frequency, based upon the equation:

$$f = \frac{1}{2 \times \pi \times \sqrt{LC}} \tag{2.16}$$

This network will than behave as an ideal voltage source when operated at the resonant frequency. The voltage of the source will be based upon the chosen inductance, L, and the current source. The voltage will also be ninety degree phase shifted because of the imaginary nature of the parallel impedance.

A similar network can be created for converting a voltage source to a current source. Additional designs for higher frequency can be found in [14]. Also, further study of these types of networks, termed impedance-inverting networks, can be found in [6].

2.4 Transistor-based Grounded and Floating Current Sources

In the previous section, it was shown that the floating voltage source, illustrated in Figure 2.3a), could be implemented by using a floating current source and appropriately sized reactive network. To use this implementation methods of creating current sources, both grounded and floating, must be given.

When a bipolar junction transistor (BJT) is operated in a common-emitter (CE) configuration the BJT behaves as a grounded current source, in which the current is determined by the voltage presented on the base terminal, when in forward active. This is also true for junction gate field-effect transistors (JFETs) and metal-oxide-semiconductor field-effect transistors (MOSFETs) operated in common-source (CS) configuration when kept in saturation.

A transistor in CE or CS configuration can be used for the "main" current source in the Figure 2.3 designs presented in section 2.2. A CE/CS transistor has the input voltage presented to the base/gate terminal and the voltage creates collector/drain current nearly proportional to the voltage when the device is operated in Class-A mode. For these configurations the class of single transistor amplifier is decided based upon the conduction angle of the device. More information regarding conduction angle is provided Appendix A.3. Here it is to be noted that a transistor operating in Class A or Class-AB can be regarded as a grounded AC source where the magnitude

of the first harmonic is (almost) linearly related to the amplitude of the base/gate drive. This is actually true for any conduction angle, as long as the conduction angle remains constant. [17]

Lastly, to implement a floating voltage source, as described in section 2.3, one must be capable of implementing a floating current source. It can be shown that an over-driven differential pair can be regarded as a floating AC current source where the magnitude of the source is determined by the value of the tail current and the phase is determined by the phase of the base/gate drive. This statement assumes that the magnitude of the input drive is sufficient to commutate the device.

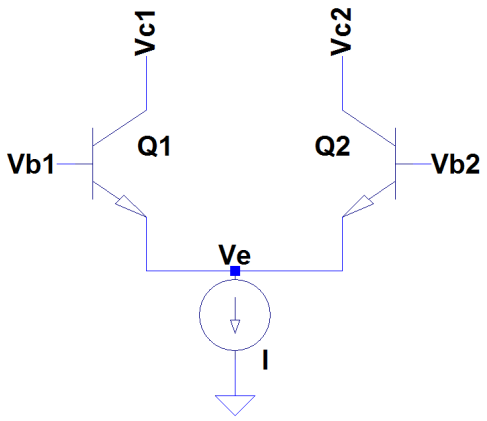


Figure 2.7: Schematic of a Bipolar Differential Pair

Figure 2.7shows a BJT differential pair with DC tail current I. By KCL:

$$I_{tail} = I_{e1} + I_{e2} \tag{2.17}$$

where I_{tail} is the tail current of the differential pair and I_{e1} and I_{e2} are the emitter currents of Q1 and Q2. This means that the magnitude of the emitter currents will always sum to equal the set tail current, as long as at least one transistor has sufficient base voltage to be conducting current. If the transistors are also matched, then the emitter currents will have an average value of half of the tail current. For small differential input drive the differential pair behaves as a linear voltage-to-current converter. However, if one of the base voltages is larger than the other, by $2V_T$ or more, the transistor with the larger base voltage will carry all of the tail current. Figure 2.8 demonstrates this property.

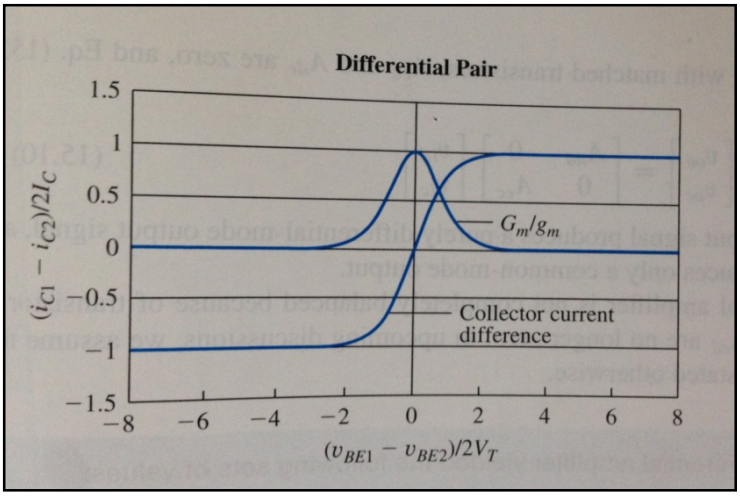


Figure 2.8: Collector current based on voltage difference between base nodes of a BJT differential pair. [7]

The V-to-I relation of a BJT diff. pair is described by a hyperbolic tangent function. As discussed in [8], this relation can be expanded in Taylor series and written in the form:

$$I_{c1} - I_{c2} = \alpha_F I_{EE}\left[\left(\frac{v_{id}}{2V_T}\right) - \frac{1}{3}\left(\frac{v_{id}}{2V_T}\right)^3 + \frac{2}{15}\left(\frac{v_{id}}{2V_T}\right)^5 - \frac{17}{315}\left(\frac{v_{id}}{2V_T}\right)^7 + \cdots\right] \qquad (2.18)$$

where I_{c1} and I_{c2} are the collector currents, α_F is the common-base current gain, I_{EE} is the tail current of the differential pair, v_{id} is the base voltage difference between the pair, and V_T is the thermal voltage. This equation shows that when an overdriven differential pair is used as a floating AC current source the created signal will also have odd order harmonics. In narrow-band amplifiers these harmonics will be removed by various filtering and impedance matching networks interfacing the transistor and the load. Further study of current switch/differential pairs can be seen in Chapter 9 & 15 of [7].

2.5 Narrow-Band Amplifiers using Two-Source Power Combining

Amplifiers that make use of the previously discussed power combing strategies are of significant interest because such topologies achieve high overall power-conversion efficiency without significant loss of linearity. Of the two-source power combining techniques described in section 2.2, some have already been implemented, and these implementations have had a variety of success.

The so-called Doherty amplifier [6] is an implementation of the power combining strategy depicted in Figure 2.2 a). In this design, both transistors operate as signal-controlled current sources, but one of them is converted into a voltage source using a suitable reactive network (this reactive network is described in Section 2.3).

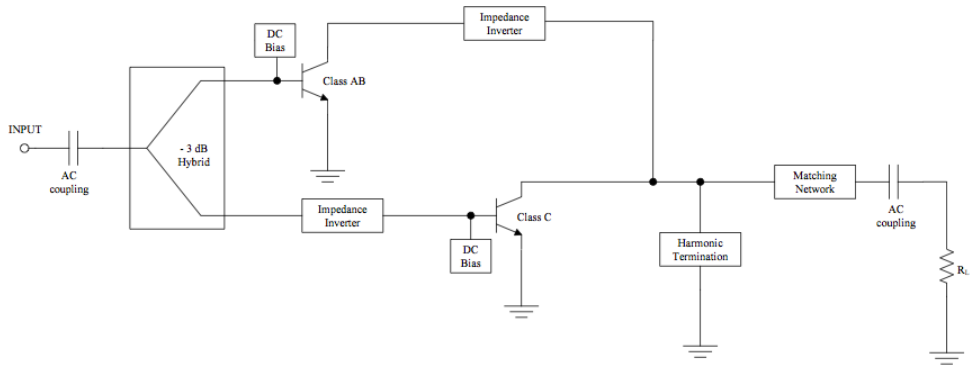


Figure 2.9: Doherty amplifier block diagram. [10]

The Doherty amplifier is also a variance of the balanced amplifier. Both, the Doherty amplifier and a balanced amplifier splits the job of power delivery between two transistors with the main transistor operated in Class-AB. In the Doherty amplifier the helper transistor is operated in deep Class C while, in other balanced amplifiers the helper transistor is usually operated in Class AB. Further information on the theory behind balanced amplifiers can be found in [12].

The amplifier topology based upon the Figure 2.2 b) combining strategy, was introduced in 2004, and a patent was awarded in 2006, see Figure 2.10[14]. The implementation was attempted by both Cody Nelson and Matt King of California Polytechnic University. The

implementation proved to be challenging as harmonic distortion created feedback to the system further increasing the high-order harmonic content [10] [13].

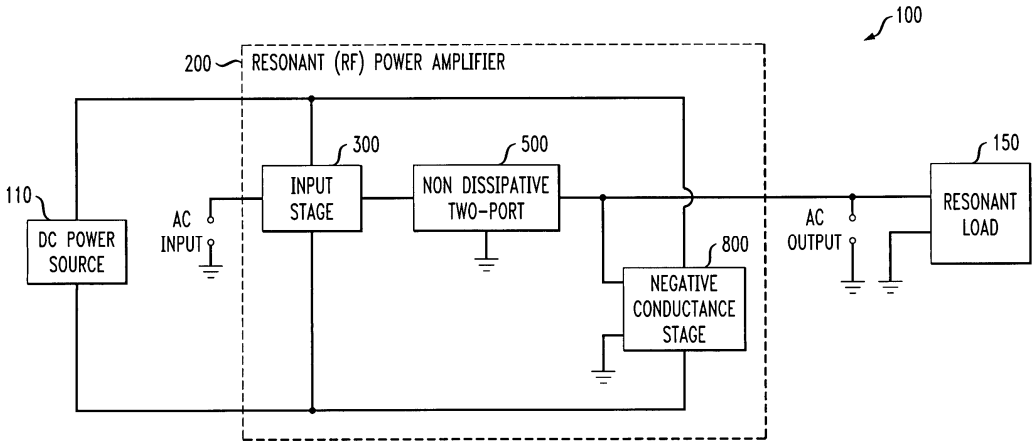


Figure 2.10: The V-parallel-NR-parallel-R_{Load} topology which was awarded a patent in 2006. [14]

Finally, this work explores the implementation of an amplifier based upon the series combining topology depicted in Figure 2.3 a). This design is considered the next step in identifying the practicality of the four two-source power combination techniques.

3. Circuit Theory and Design

3.1 Single Transistor Resonant Amplifier

Our design is based upon the single transistor narrow-band amplifier, shown in Figure 3.1. The circuit is composed of a single transistor with two resonant networks. The parallel resonant network attaches the transistor collector terminal to supply and series one from collector terminal to load. This design is simple but is limited in performance by transistor properties and resonant network imperfections. For example, the signal swing at the collector terminal equals that across the load. As the magnitude of this swing becomes commensurable to the supply voltage, Q1 is forced into saturation creating an unacceptable distortion level.

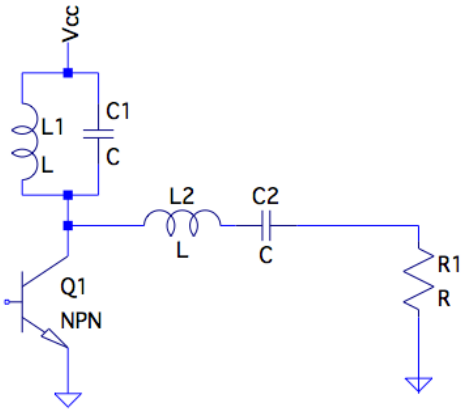


Figure 3.1: Single Transistor Resonant Amplifier. The parallel resonant network is "open circuit" at the frequency of operation while the series one is "short circuit".

The single transistor design works by converting a voltage waveform into a current waveform. In the case of a bipolar junction transistor (BJT), a voltage waveform applied to the base of a transistor is converted to a current waveform flowing between collector and emitter.

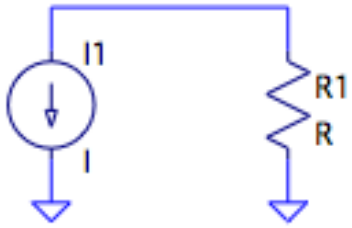


Figure 3.2: Simple circuit depicting the operation of the Fig. 3.1 resonant amplifier.

The AC component of the current is then directed into the load. This is accomplished by the series resonant network. The ratio of the base signal voltage to the collector signal current is determined by the transconductance of the transistor. By appropriately biasing and sizing a transistor, the g_m can be adjusted. Finally, the current applied to the load produces a voltage waveform. The voltage waveform created is proportional to the original voltage waveform applied to the base of the transistor.

One weakness of this design is that the voltage waveform, created by the induced current interacting with the load, can cause the transistor to exit its operating voltage range. This means that the collector voltage is either too high or too low causing the transistor to leave forward active mode. Exiting its operating range generally results in clipping of the output waveform. If the voltage waveform is clipped on either end, than the signal content is no longer preserved. To avoid this issue the load and current must be chosen carefully.

Each resonant network in this design serves a different purpose. The parallel resonant network from collector to supply behaves as an “open circuit” at the resonant frequency and therefore serves as a band-reject filter, or RF choke. This band-reject filter prevents the signal being amplified through the transistor from being shorted to ground, while simultaneously DC biasing the transistor. The DC biasing allows for the transistor to be operated in the desired active region.

The series, band-pass, resonant network connecting the transistor to the load works to prevent frequencies other than the fundamental from reaching the load. Different applications call for different Q factors and amplifier bandwidths, but the general concept of band limiting the signal applied to the load is the same.

3.2 Series-Type Power Combining

The single transistor amplifier of Figure 3.1 serves as the basis for series-type RF power combining. As described previously the single transistor amplifier must be tuned to provide maximum linearity and power output. Both of these characteristics are limited by the transistor and available supply voltage.

The goal of adding an active network between the transistor and resistor is to improve the power capability of the transistor while maintaining the linearity properties of the chosen transistor. This first step in explaining this technique is to understand the circuit of Figure 3.3.

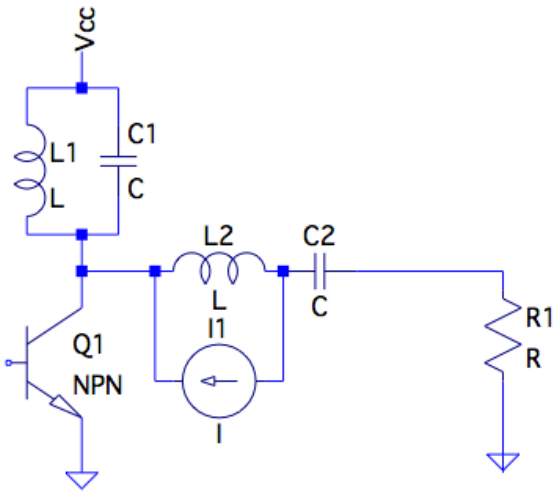


Figure 3.3: Conceptual implementation of series power combining. The BJT operates as an AC current source, while L2, C2 and I form a floating AC voltage source.

Figure 3.3 depicts the same single transistor amplifier as previously seen in Figure 3.1, but a current source has been added in parallel with the inductive component of the series resonant network. The added current source, in conjunction with the inductive impedance and the capacitance of C2, behaves as a voltage source connecting the transistor and the load. This further simplification is represented in Figure 3.4, combining the original single transistor model with the voltage source.

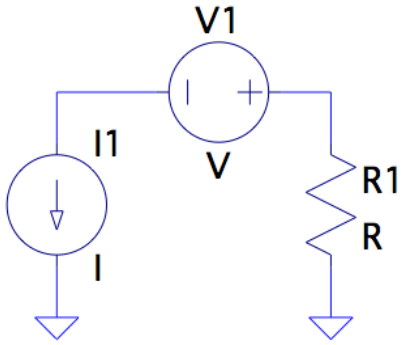


Figure 3.4: Simple circuit depicting the operation of Fig. 3.3 resonant amplifier.

This diagram illustrates the benefits of an added active element to the circuit. The current source I1, which represents the transistor, determines the gain and linearity of the overall amplifier. On the other hand, the voltage source V1 serves as a "helper". When the voltage source delivers power to the load it reduces the power demanded from the transistor. Next we will perform a few spice simulations to verify the theory.

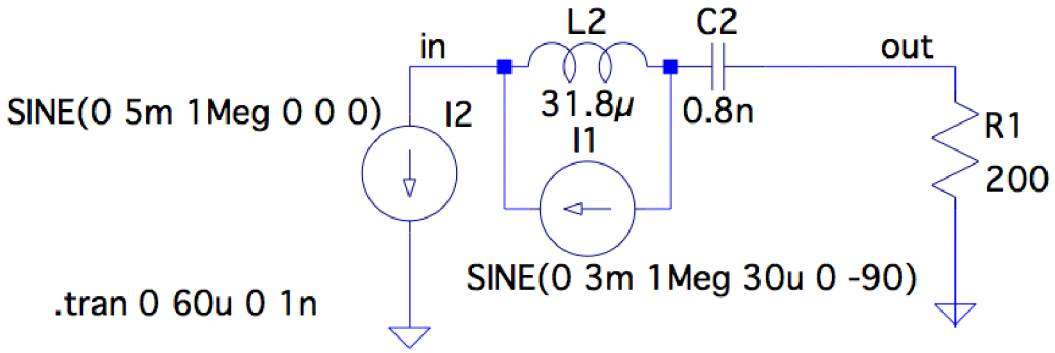


Figure 3.5: Circuit used to verify theory. L2 and C2 are resonant at 1 MHz. Both sources are purely sinusoidal with frequency of 1 MHz.

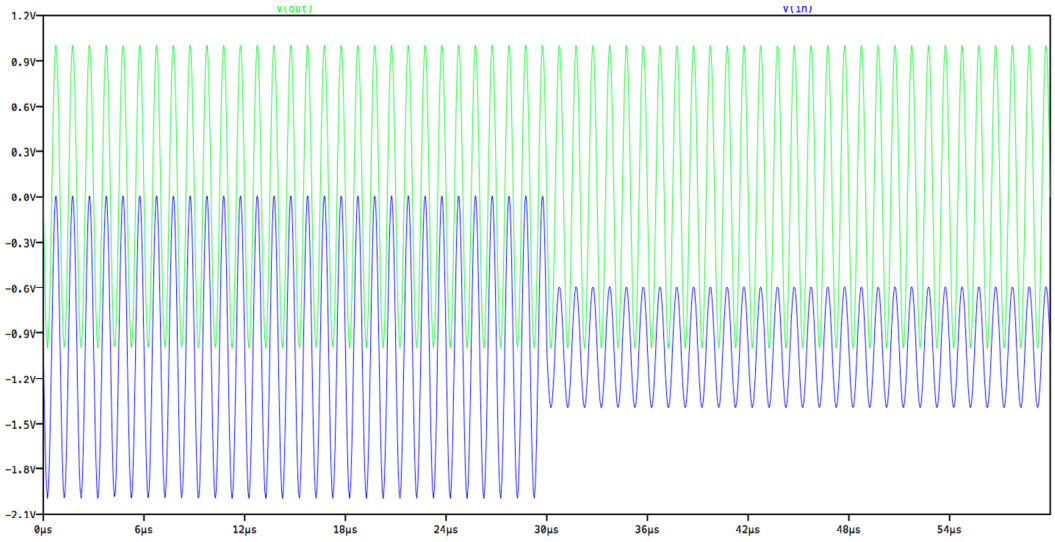


Figure 3.6: Transient simulation of the circuit in Figure 3.5. The voltage across the main current source, shown in blue, decreases when the "helper" current source is activated.

The circuit in Figure 3.5shows the effects of the helper current source. In Figure 3.5 the current source is turned on at thirty microseconds and the magnitude of the voltage waveform is halved.

$$V_{L2} = I1 \times j\omega L2 \tag{3.1}$$

$$V_{Load} = I2 \times R1 \tag{3.2}$$

$$V_{I2} = V_{Load} + V_{L2} \tag{3.3}$$

Since the waveforms are out of phase 90 degrees with each other the addition of V_{Load} and V_{L2} yields a V_{I2} of smaller magnitude. The green waveform shows that the voltage and hence the power to the load has not changed, but the power required by the main current source I2 has been reduced. The power reduction comes from the reduction in voltage across I2 without any reduction in current. The current waveform is not depicted, but can be inferred since the output voltage has remained constant.

4. Implementation in Software

4.1 LTSpice

After analyzing the theory behind the series power combining strategy, the next step is to test its validity in circuit simulation software. Circuit simulation is useful for choosing the right components and validating theory prior to implementation. For this circuit, LTspice was the chosen circuit simulation tool because of its ease of use and my familiarity with its functionality. The goal of this thesis is concept validation; hence both the simulations and subsequent implementation are carried out at low (MHz range) frequencies.

4.2 Floating Current Source

The simulation conducted in Chapter 3 used ideal AC current sources to prove that the power-combining theory was valid. This section focuses on choosing realizable components to implement every aspect of the circuit. For example, the idealized helper current source in Figure 3.5 is not a component that can be purchased. Therefore, to implement this current source a differential pair was utilized.

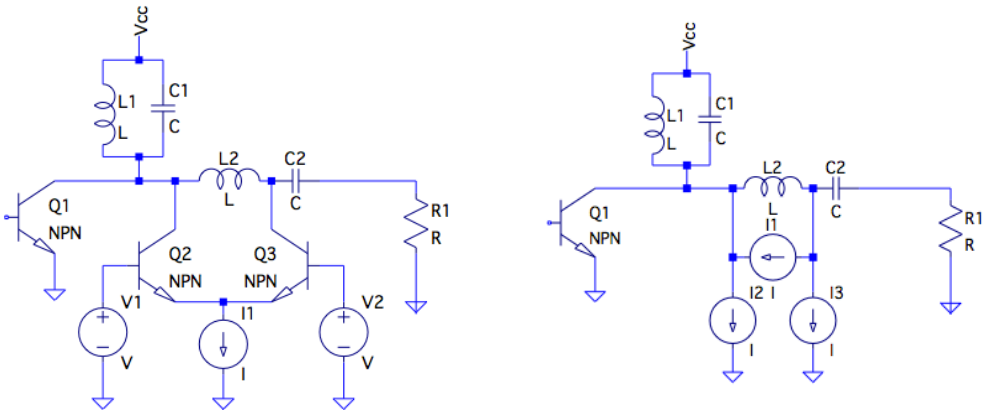
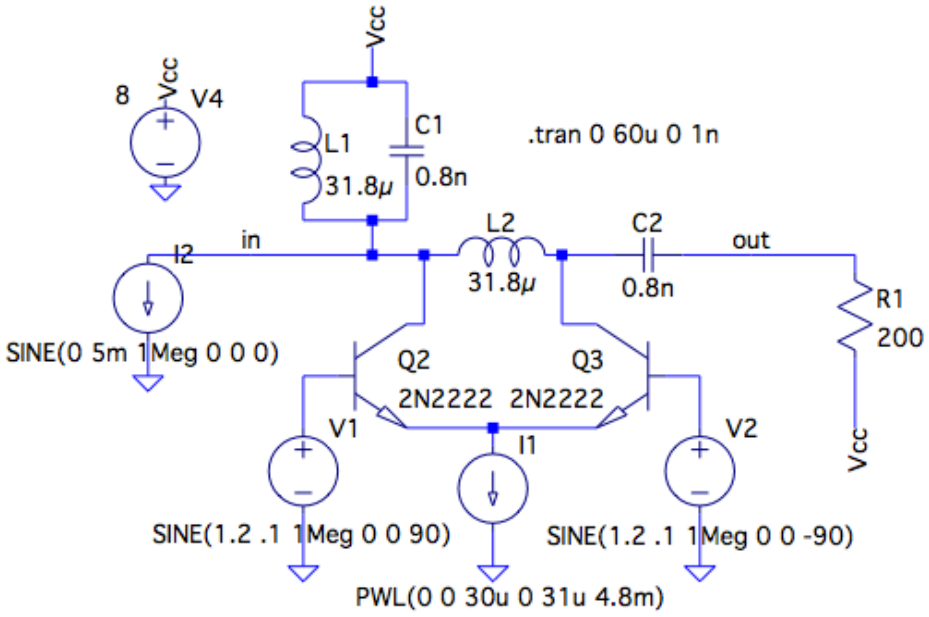
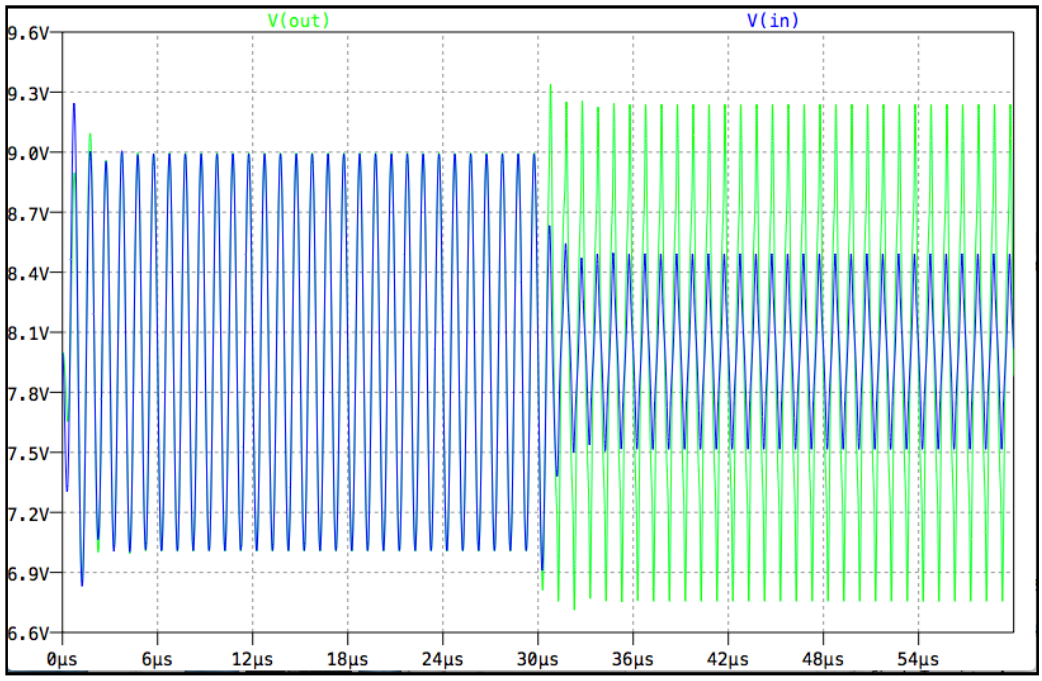


Figure 4.1: (a) Differential pair implementation of a floating current source in a series combining amplifier. (b) Equivalent circuit model for differential pair implementation.

Figure 4.1 shows the current source implemented with a differential pair. When a differential pair is commutated by a large enough voltage difference the two transistors will produce a collector current with rectangular shape and value alternating between zero and the bias current, where the bias current is Figure 4.1a current I1. This behavior can be modeled as in Figure 4.1b in which current source I1 is a square wave with a value of half the bias current. The ground facing current source will also have a value of half the bias current, but these sources are DC. Furthermore, a rectangular waveform with a magnitude of half the bias current will have a fundamental component nearing $(2/\pi)^* I_{bias}$. [3] This component is the representation for the idealized current source presented in Figure 3.5. Circuit simulation was done with the differential pair implementation of the floating current source.



(a)



(b)

Figure 4.2: (a) Floating current source implemented using a differential pair. (b) Voltage waveforms: “blue” across the main source, “green” across the load.

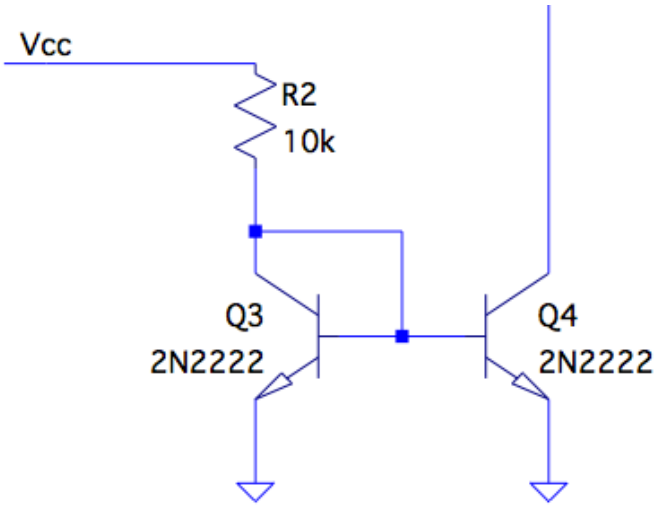
Figure 4.2a demonstrates the differential pair implementation of the floating current source. Key aspects of this implementation include appropriate commutation, both magnitude and phase, of the differential pair, and proper sizing of the tail current. Appropriate commutation of the

differential pair is achieved by ensuring that the differential pair voltage difference is high enough to force all current through only one transistor at a time. This results in a square wave. Different transistors will have different voltage ranges, but for the 2N2222, a BJT device, approximately 50mV difference was enough to ensure proper commutation. Also, since the floating current source needs to be 90 degree phase shifted with respect to the main source, the voltage sources on the base terminals of the differential pair must be shifted 90 degrees from the source. To achieve commutation, a positive and negative 90 degree phase shift was implemented for Q2 and Q3, respectively.

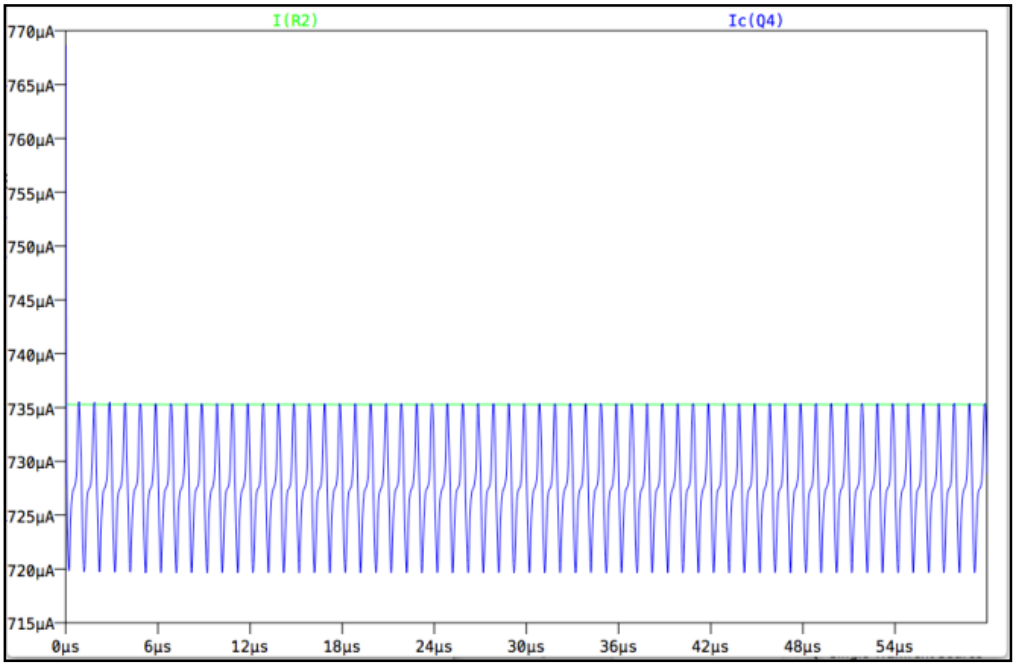
Figure 4.2b shows the input and output voltages when the tail current source of Figure 4.2a is activated at 30 us. The plot shows that before the active network is powered, the series resonant network operates as a "short" and the voltages across the main source and the load have equal magnitude and phase. However, after the circuit is activated the output voltage increases slightly, and the voltage across the main source decreases. This voltage decrease shows proper operation of the circuit. On the other hand, the increase in output voltage is undesired. The output voltage has increased because the differential pair circuit produces a square wave current not a sinusoidal one. This means that power is distributed to all odd-harmonics. Since this increase in voltage is from odd-harmonics it can be filtered out.

4.3 Differential Pair Tail Current

The next idealized component is the tail current powering the differential pair. In order to create a constant current that can be easily controlled, a current mirror was implemented.



(a)



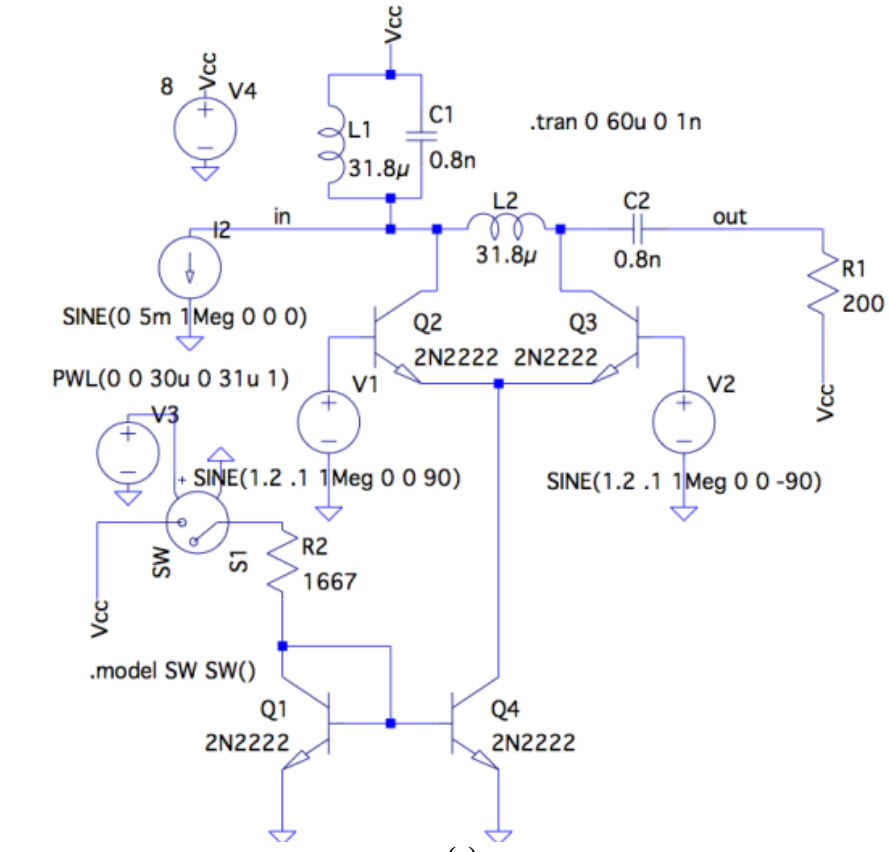
(b)

Figure 4.3:(a) Current mirror schematic implemented for simulation. (b) Plot of Q3 and Q4 Collector Current for the current mirror implemented above.

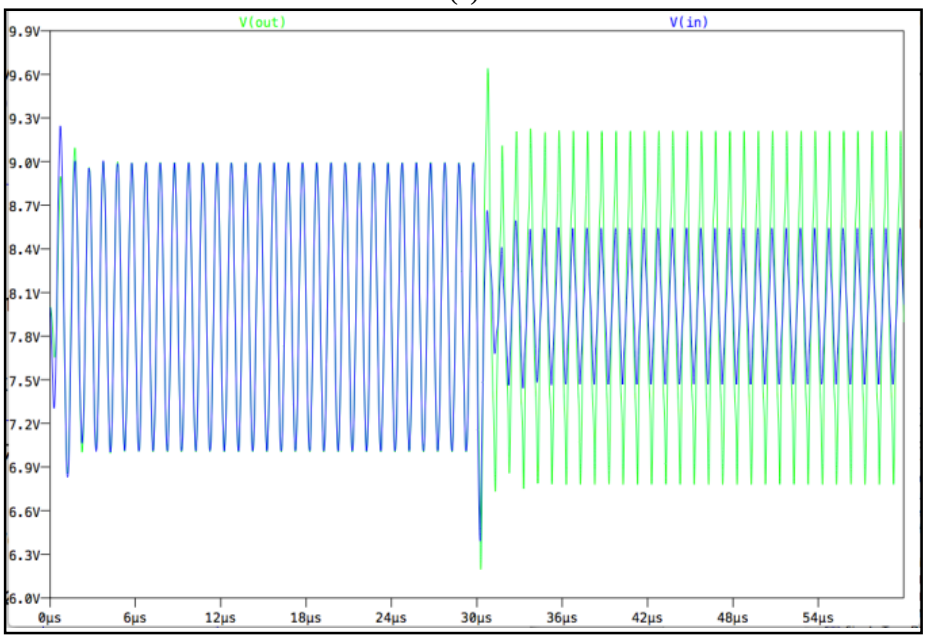
Figure 4.3a shows the circuit diagram for the current mirror. By connecting the base and collector of Q3 to the base of Q4, the V_{BE} of Q3 and Q4 are identical. As long as the two transistors are very similar, and Q4 is kept in forward active mode of operation, having the same V_{BE} will result in

nearly identical collector currents. The term similar, in this case, generally refers to the same nominal size, fabrication on the same wafer. Additional criterion to be considered is proximity of each component on the wafer, and placement in close proximity to each other with the same orientation. In Figure 4.3b the green waveform shows the collector current of Q3 and the blue waveform collector current for Q4. The collector currents are very similar with slight variations for Q4. This variation is due to loading of the Q4 transistor. This simulation, Figure 4.3, has the current mirror driving the differential pair in Figure 4.4, and the differential pair loads the current mirror when the transistors toggle, hence the observed 2 MHz ripple.

Figure 4.4 shows the operation of the circuit with the current mirror replacing the ideal current source in Figure 4.1.



(a)



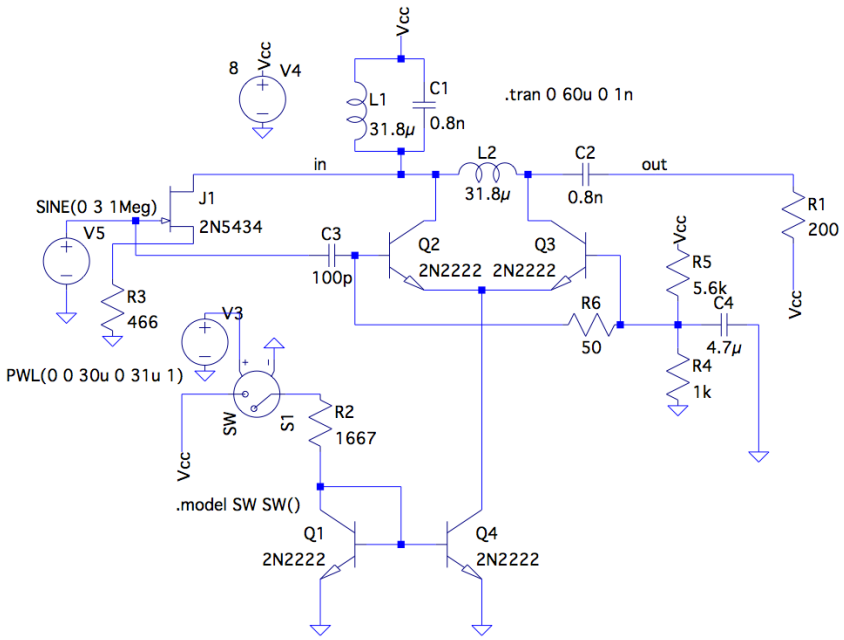
(b)

Figure 4.4: (a) Complete implementation of the current mirror and differential pair to produce the floating current source. (b) Plot showing circuit operation with Current Mirror

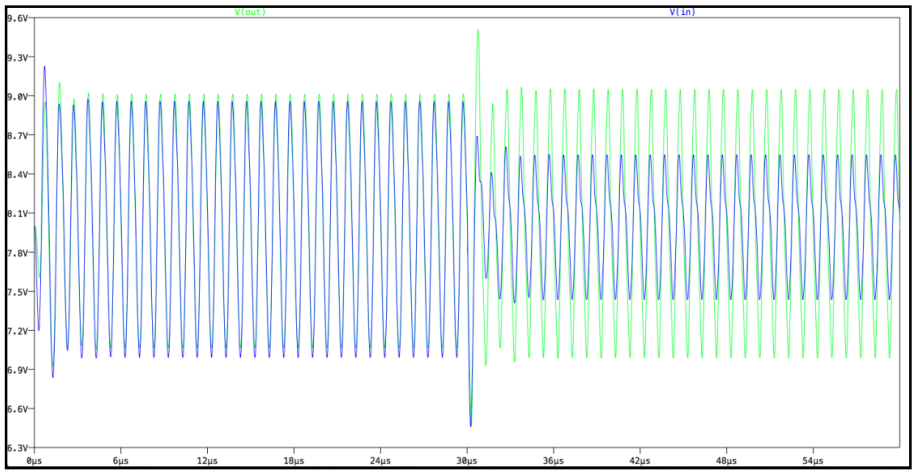
Figure 4.4 shows that circuit operation, with the current mirror in use, closely resembles that of Figure 4.2b. The current mirror is not an ideal source and therefore there are slight transients in the plot. These transients only last for a few microseconds and are therefore acceptable. Also, these transients are most likely resultant from the programmable switch being used to activate the current mirror, as opposed to circuit issues. The output variation is also present in this implementation. Again, this output voltage increase is created by the odd-harmonics generated by the differential pair implementation and can be filtered out.

4.4 Differential Pair Commutation

The final aspect of the circuit that must be addressed is the voltage waveforms that toggle the differential pair. In the section 3.2, it was explained that the current source must be ninety degrees out of phase with the AC current of the main source. The floating current source is now being implemented with the differential pair. Therefore, the differential pair must be toggled 90 degrees out of phase to achieve proper power combining. As seen in Figure 4.4a, the differential pair base terminals must be supplied with signals that are each ninety degrees out of phase with the incoming signal. To accomplish this ninety degree phase shift, a High Pass circuit was applied to the incoming voltage signal, shown in Figure 4.5.



(a)



(b)

Figure 4.5: (a) Circuit showing series power combining. The JFET transistor implements the main current source. The 90-degree drive for the diff. pair is obtained from the input signal using a RC High Pass filter operated deep into stop-band. For ease of waveform comparison the load is connected to Vcc as opposed to GND. (b) Voltage waveforms measured across the drain-source of the JFET and the load. The blue waveform is the JFET drain-source voltage and decreases when the tail current is activated, whereas the load voltage remains relatively constant.

Figure 4.5a shows the ninety degree phase shift implementation by using capacitor C3 and resistor R6. This RC combination forms a HP filter with a 32 MHz cut off. The desired signal of 1MHz falls deep into the stop-band and experiences a phase-shift of approximately 90 degrees. The plot shown in Figure 4.5b demonstrates that the properties of the proposed series power combining are

still maintained. The blue waveform is the drain terminal voltage and there is some distortion, but this is insignificant because this waveform is not being used at the output and the overall property of voltage scaling is still upheld. This distortion is most likely caused by the ninety degree phase shift circuit not providing an exact ninety degree phase shift. The circuit of Figure 10 was our first implementation. This circuit was deemed acceptable for concept verification, but has a major shortcoming—the 90-degree phase-shifting loads the input of the main amplifier. This loading could introduce additional distortion. Improved variant is shown in Figure 4.6

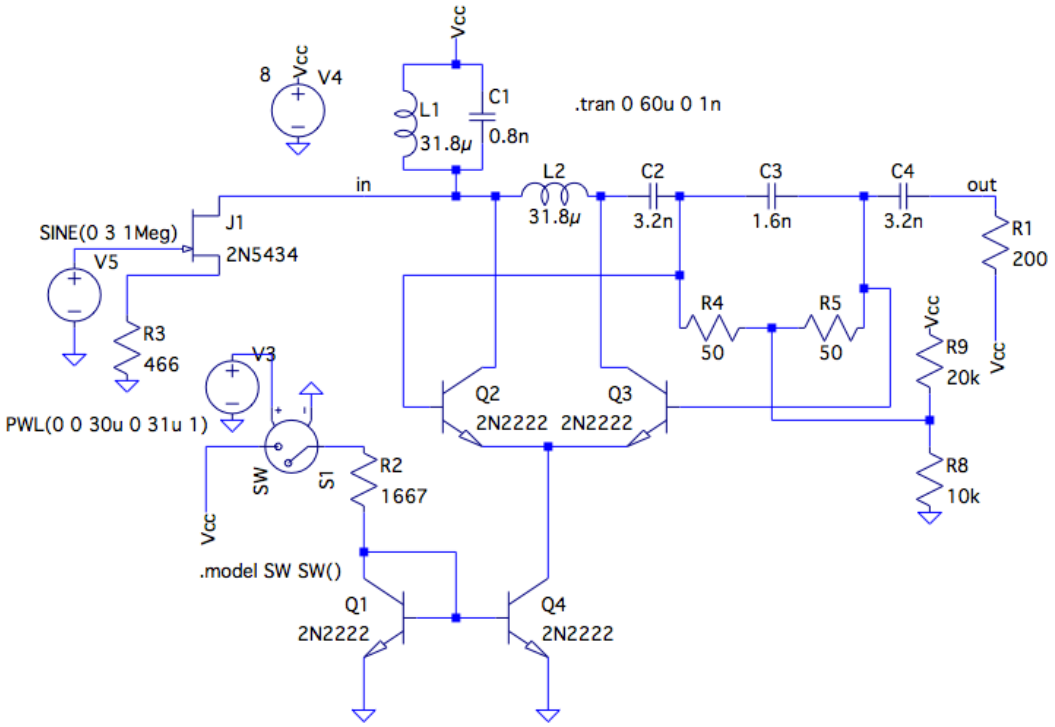


Figure 4.6: Amplifier with series power combining. Required 90-degree diff. pair drive is the voltage across C3. The capacitor voltage is 90 degree phase shifted relative to the main current conducted by C3.

The above figure shows the three capacitor design in which C2, C3 and C4 make up the series capacitor originally in place. By adding two capacitors in series with the original, the base nodes of the differential pair can be driven by its own output. By sizing the C3 capacitor the base nodes of the diff. pair are naturally driven with a 90 degree phase shift, with respect to the current flowing through the capacitor. This is because of the natural 90 degree phase shift of a capacitor. This design is used for the second implementation, and appropriate sizing of the three capacitor design is explained in section 6.3.

5. Prototyping

5.1 Supplemental Tools

The research conducted on this thesis was aided by many instruments and tools. Bench top tools such as Power Supplies, Function Generators, Oscilloscopes and Digital Multimeters were used. All of the equipment used in my thesis is owned by Cal Poly SLO and was manufactured by Agilent Technologies.

5.2 Prototype I

With the simulation provided in Figure 4.5 and Figure 4.6 the basis for the design is complete. The simulation shows a working system with one, eight volt supply and an appropriate input signal. The simulations serve as a basis for the design, and from them we chose discrete components to create a physical implementation. This section will first go through the first implementation of Prototype I and then the adjusted Prototype I. This process is necessary to explain the significance of the series resonant network.

The first step to creating this circuit is the resonant networks. The two networks, RF choke and series band-pass, do not need to have the same components. The resonant frequency and quality factor of the two networks are the main areas of interest. The quality factor of the networks should be chosen such that the desired signal is blocked from escaping to the supply, but unhindered to pass to the load. For testing purposes a high quality factor is desirable because the signal being presented to the input was chosen to be 1 MHz, and a narrow bandwidth will remove the odd harmonics from the differential pair.

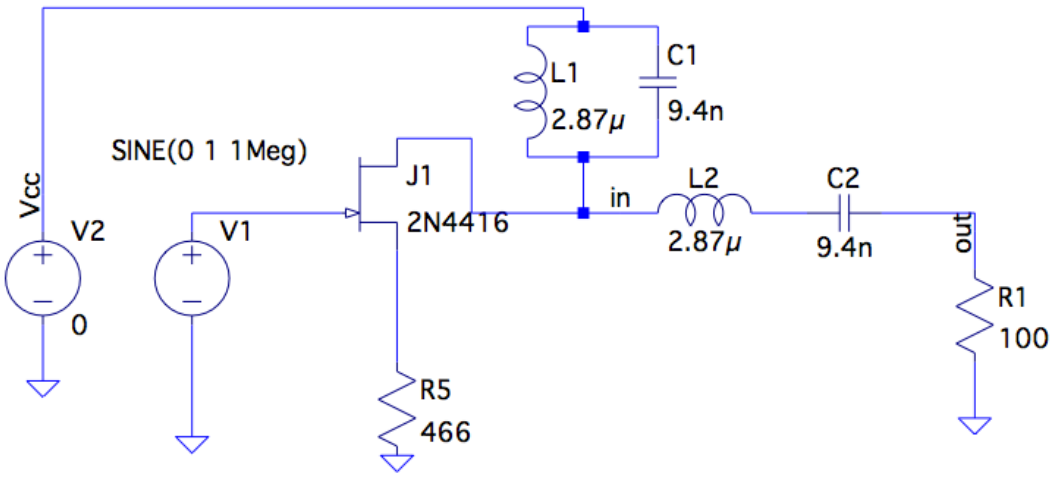


Figure 5.1: Initial structure used for Prototype I. This schematic contains the two resonant networks as well as the chosen input transistor.

The first resonant networks were implemented with the components shown in Figure 5.1. We tested this circuit for the frequencies in the vicinity of the expected resonant frequency of 1 MHz. Figure 5.2 shows the frequency plot. The center frequency was slightly shifted from the goal of 1 MHz, but 1 MHz was well within the 3dB range.

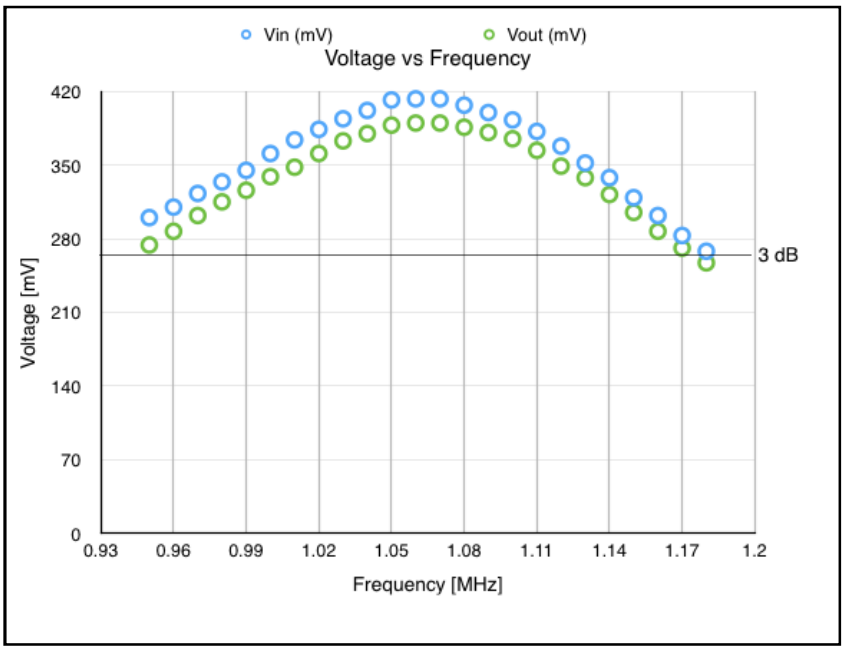


Figure 5.2: This plot shows the measured frequency response for the Figure 5.1 single-transistor amplifier.

The next task was building the active network. The components, as described in previous sections, are a current mirror, and differential pair. The topology of the current mirror can be found in Figure 4.3. We used a supply voltage of 8V and a bias resistor of 10k Ohms, this results in a current of approx. 0.8 mA. The differential pair was constructed using the same discrete chip as the current mirror. The chip, CA3086 [2], contains five NPN BJTs. The differential pair utilizes the Q1 and Q2 transistors with shared emitter. It is important that the differential pair and current mirror be implemented with components from the same wafer because both of these circuits are sensitive to variations in transistor properties. This stems from the fact that both of these designs assume that the pair of transistors have the exact same properties. Proximity is also important because these devices exhibit changes with temperature and close proximity helps to ensure that the temperature of each device is similar. The tail current of 0.8 mA set by the current mirror is chosen to be no greater than the current that should be delivered to the load by the transistor.

We used a 2N4416 [1] JFET as the input transistor. The biasing of this device is established using series-series negative feedback resistive degeneration. The JFET with source degeneration of 466 Ohms has a transconductance (g_m) of 2.9 mS. This was calculated by applying a 200 mVpp waveform to the gate of the device and measuring the peak-peak output voltage into a drain resistance of 268 ohms. After obtaining the transconductance, we can calculate the voltage that will develop across the load, given the input voltage. With the transistor characterized, the active network built, and the resonant network built, the last task is to design a ninety degree phase shift circuit for the differential pair. The ninety degree phase shift circuit we used is based on the design provided in Figure 4.5. The circuit utilizes a capacitor of 100pF and a resistor of 150 Ohms. This network provides for a 20 dB magnitude reduction and +84.6 degree phase shift. The DC bias voltage used for the differential pair is 1.2V.

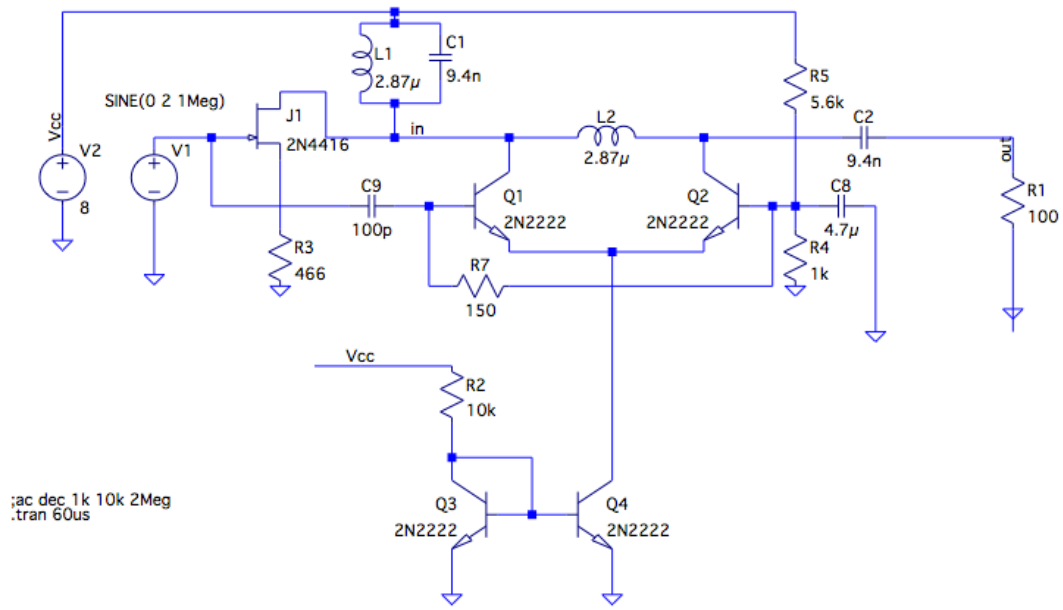


Figure 5.3: Prototype I implemented with the HP filter as a 90 degree phase shift circuit.

Figure 5.3 depicts the first circuit implementation of our series-combining amplifier topology. The figure shows the 0.8 mA current mirror providing the tail current for the differential pair, the ninety degree phase shift circuit commutating the differential pair, and the degenerated common source JFET connected to the previously tested resonant networks.

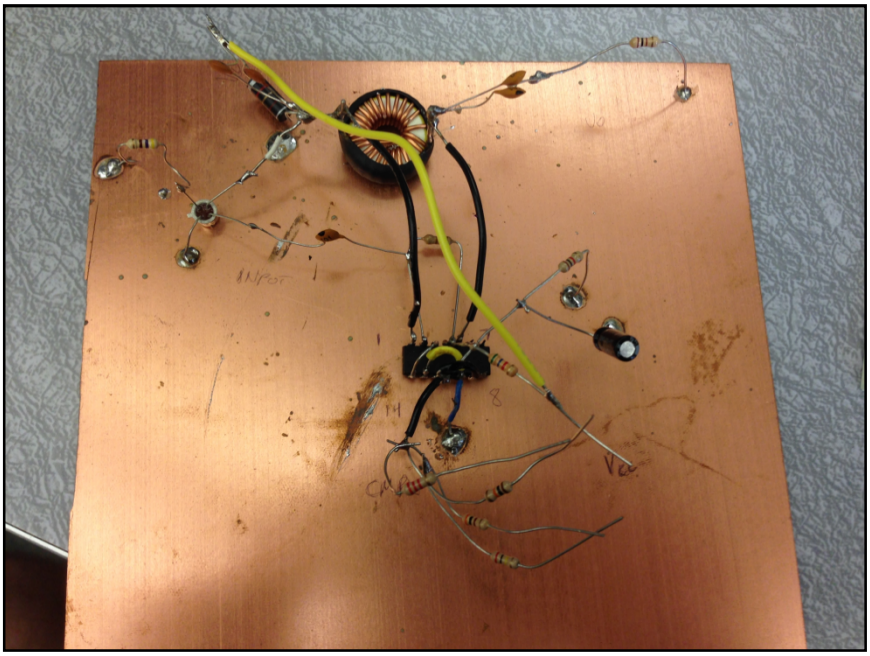
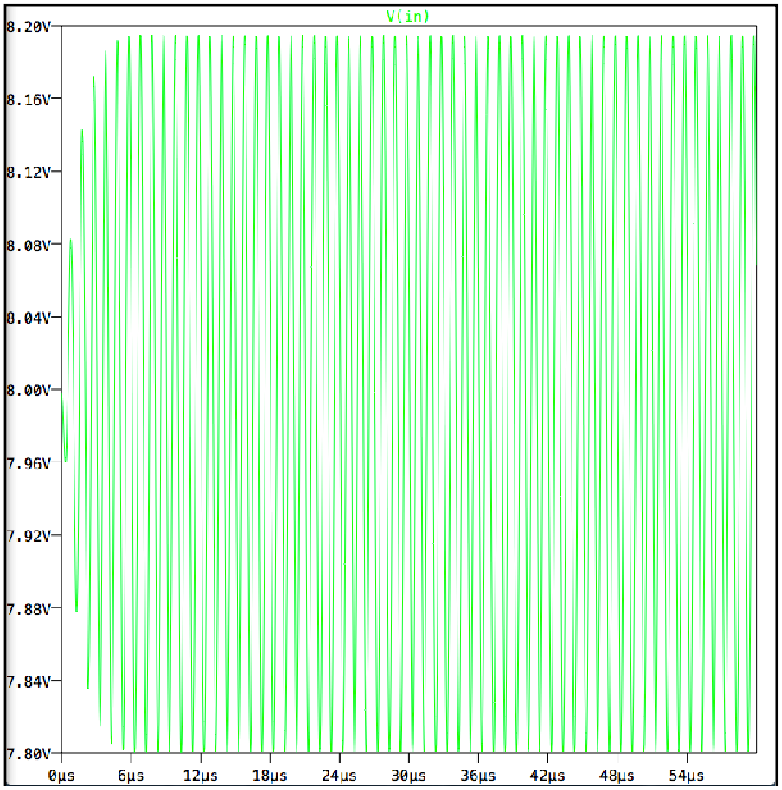
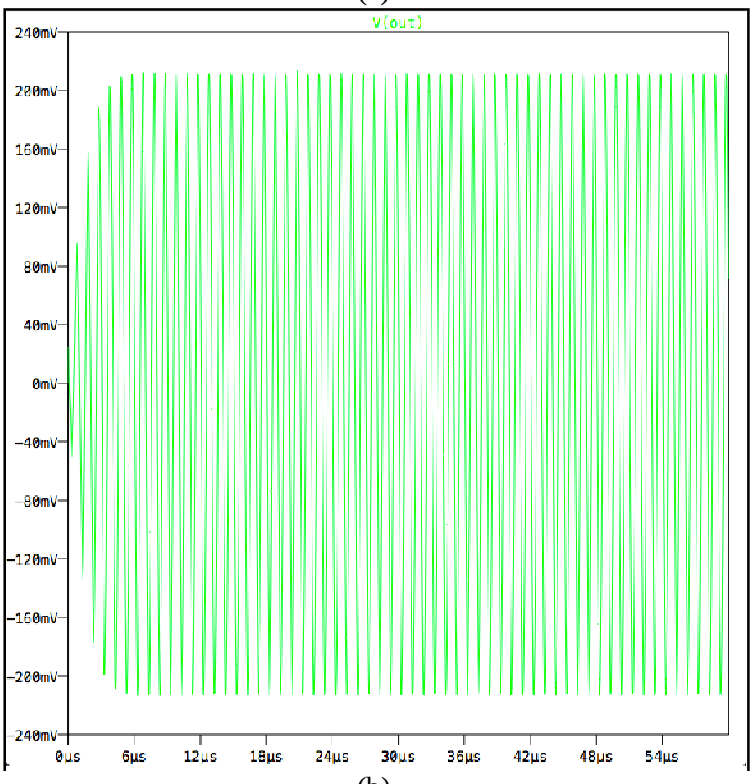


Figure 5.4: "Dead bug" construction of Prototype I.



(a)



(b)

Figure 5.5: (a) Simulated voltage waveform at the drain of the JFET for Prototype I. (b) Simulated output Voltagewaveform for Prototype I.

Figure 5.5 shows encouraging results but also deficiencies. First, one must note that in this circuit the 30 microsecond turn on does not occur for the active network. This means that the active network is on immediately. Figure 5.5b shows the output waveform is steady at 200 mV which is what is to be expected. Simple calculations with an input voltage of 2V, a transconductance of 2.9 mS and a load of 100 Ohms the expected predict an output voltage of580mVpp. The shown waveform is approx. 400 mVpp, the discrepancy is likely due to power loss in the reactive networks. In Figure 5.5a the JFET drain voltage waveform unfortuanetly does not show the expected voltage reduction. Since the active network is turned on the drain voltage of the JFET should benefit from the power provided by the active network and therefore this voltage should be lower in magnitude than the output waveform. The same issue is seen in the physical implementation of the circuit, Scope captures of the measured voltages can be seen in Figure 5.6.

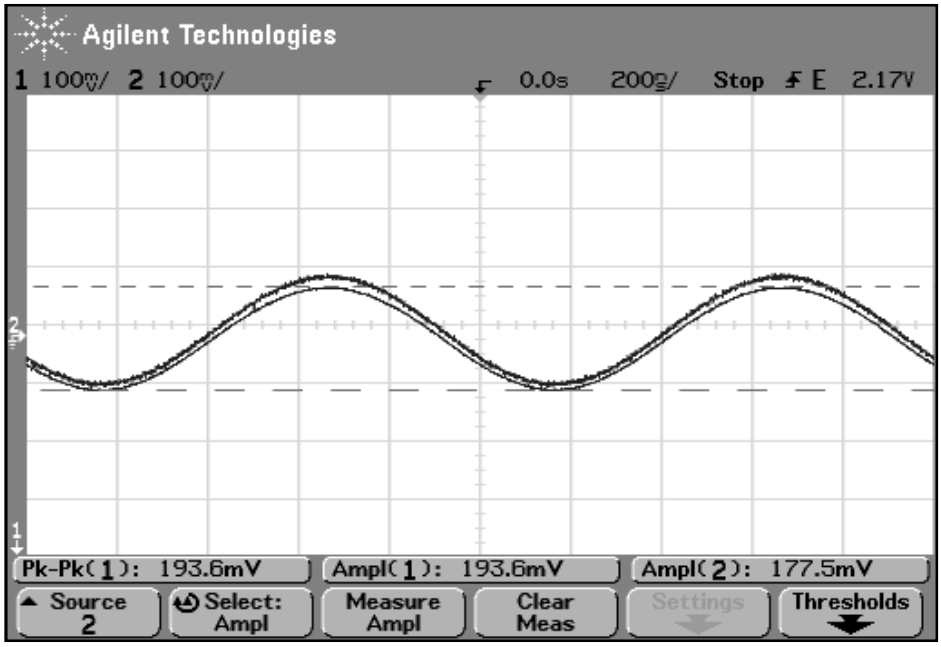


Figure 5.6: JFET drain voltage and Output Voltage Waveforms for First Circuit Implementation

The reason there is no significant voltage drop across at the transistor drain is because the inductor in Figure 5.3 is too small to provide noticeable voltage assistance. The inductor impedance in Figure 5.4, based on the inductance and frequency of operation, is 18 Ohms. This impedance, when compared to the output impedance of 100 Ohms, is 5 times smaller. This means that

eitherthe current created by the differential pair or the value of the inductor must be increased to provide a significant voltage drop across the resonant network.

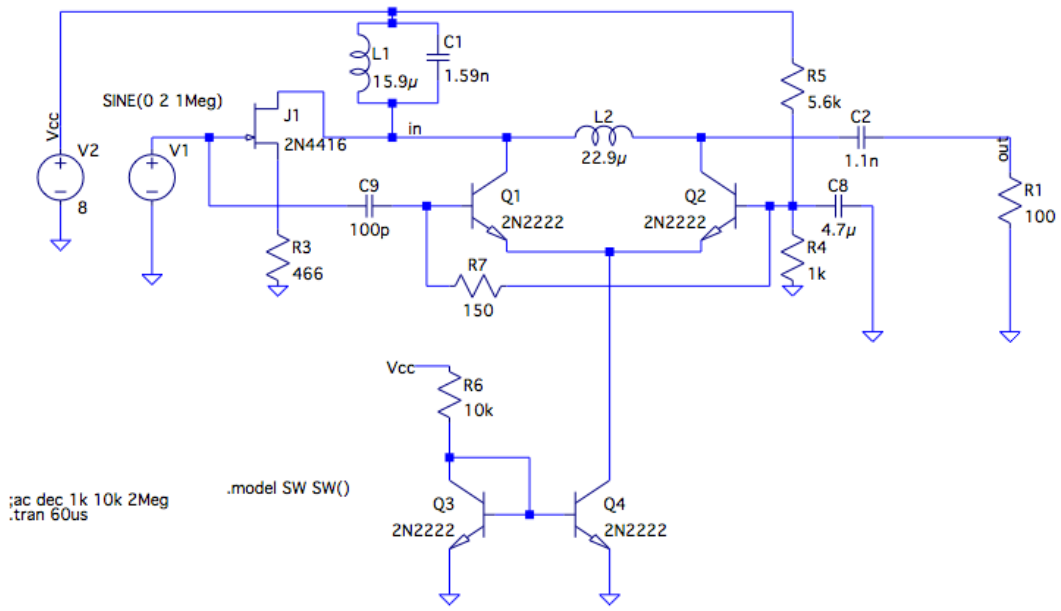
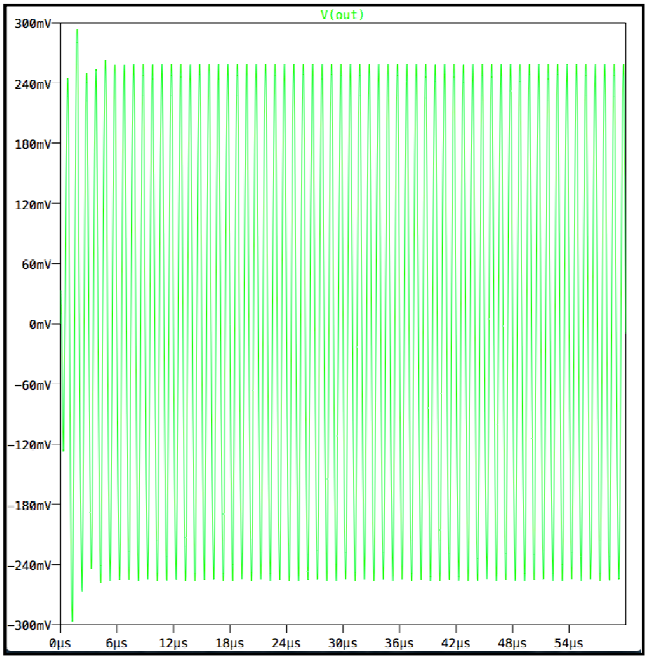
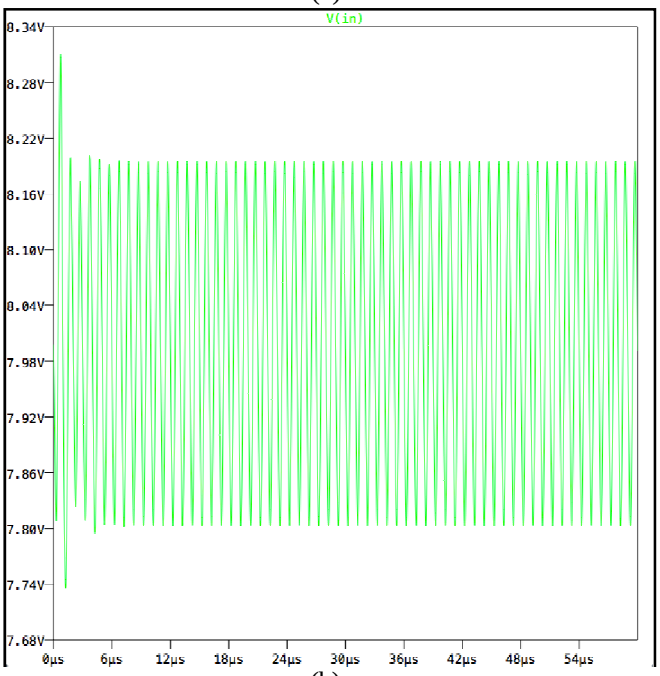


Figure 5.7: Second Implementation of Prototype I with larger inductor and adjusted capacitor.

We used Figure 5.7circuit to study the impact of the inductor L2. By making L2 larger the impedance difference between the inductor and the load diminishes, thereby increasing the voltage drop across the inductor resulting in a prominent voltage reduction, or "help" for the JFET.



(a)



(b)

Figure 5.8: (a) Simulated JFET drain voltage waveform for Prototype I with inductor correction. (b) Simulated output voltagewaveform for Prototype I with inductor correction.

In the simulation shown in Figure 5.8, one can see the voltage difference between the voltage signal at the output and the voltage at the drain of the JFET. Since the inductance value was changed from 2.87 uH to 22.9 uH the impedance increased from 18 Ohms to 143 Ohms. This

change makes the impedance of the inductor larger than the impedance of the load. Since the current through the load and inductor remains the same the voltage drop across the inductor will increase and the voltage at the transistor will be lowered, see equation 5.1.

$$V_L = jX_L \times I_L \tag{5.1}$$

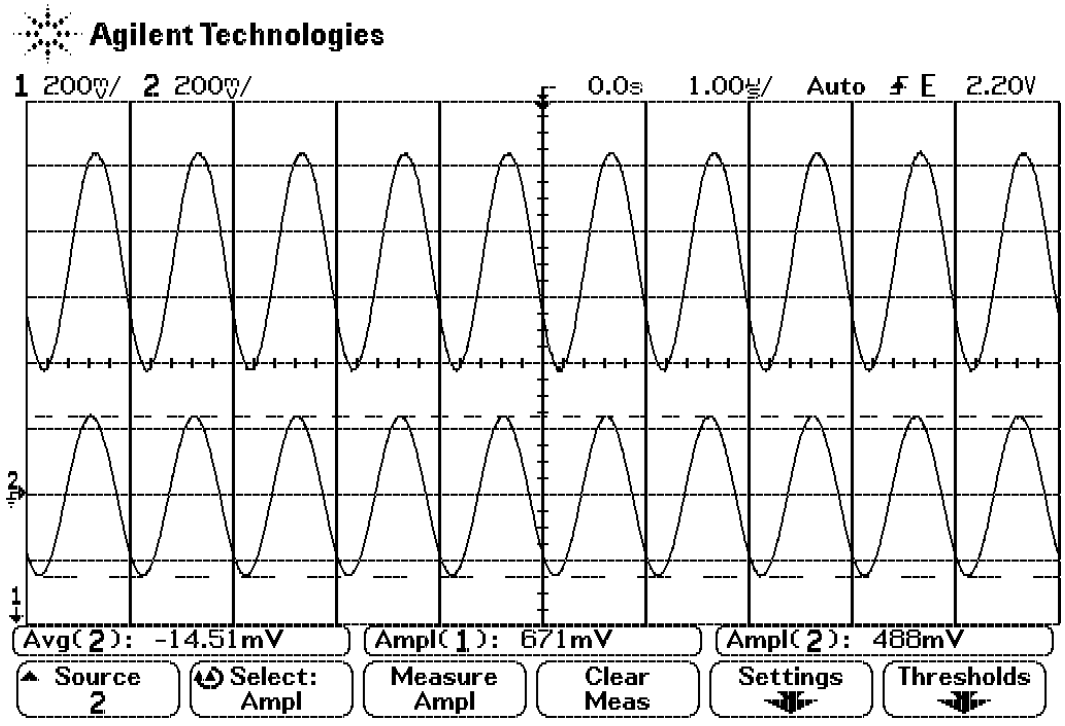


Figure 5.9: JFET drain (Channel 1) and Output (Channel 2) voltage waveforms with the current mirror disabled such that the differential pair has no tail current.

Comparing Figure 5.9 and 5.10 we see that changing the inductor makes a significant impact on the power demanded from the JFET. In Figure 5.9, when the active network is off, the JFET drain voltage is 671 mV. Whereas, in Figure 5.10, when the active network is on, the JFET drain voltage is 597 mV. Concurrently, the voltage at the output, Ampl(2), remains relatively constant. These images show that the design works, and the properly sizing the inductor is crucial to achieve desired "helper" power.

Figure 5.11 demonstrates that the HPF is properly commutating the diff. pair.

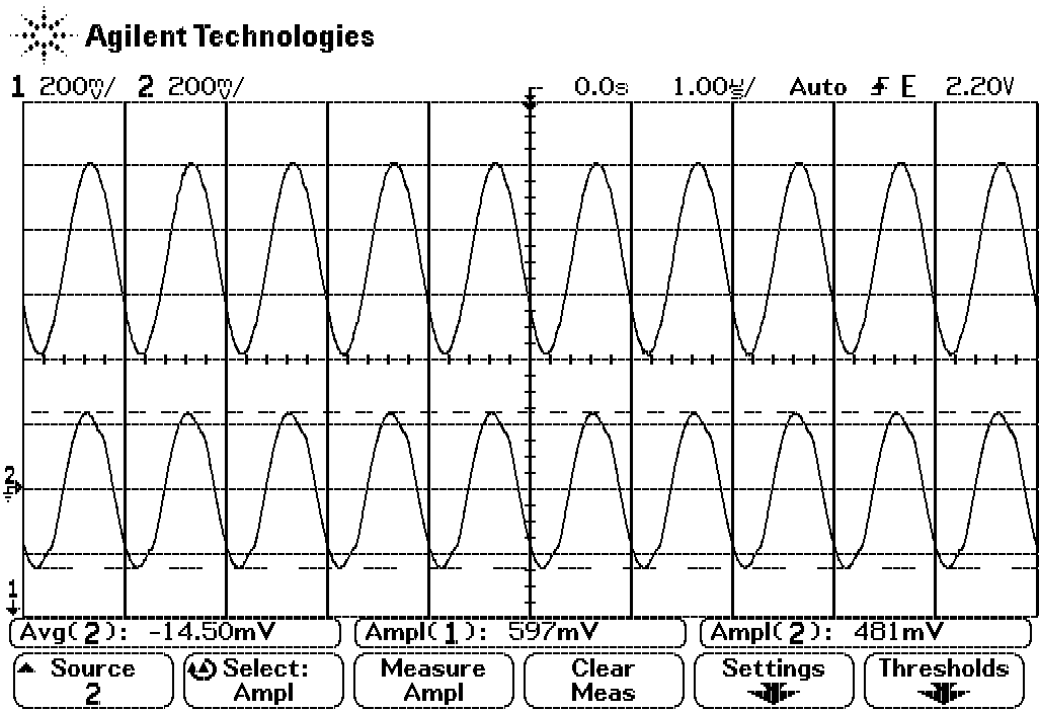


Figure 5.10:JFET drain (Channel 1) and Output (Channel 2) Voltage Waveforms with the current mirror resistor set to 2.2k Ohms for a tail current of 3.3 mA.

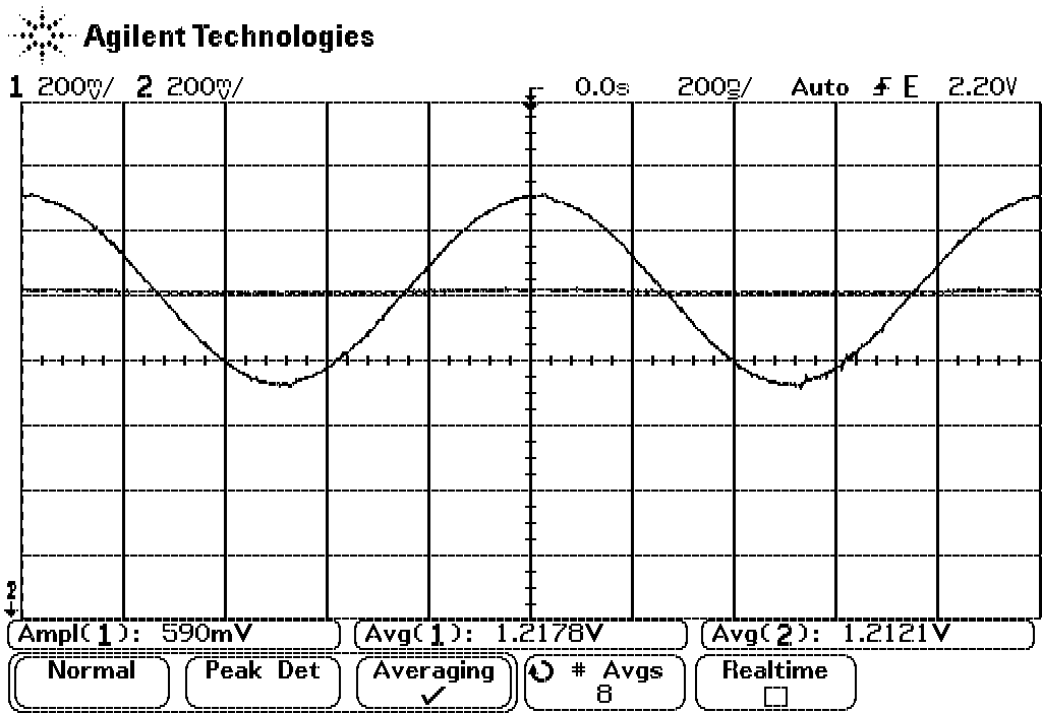


Figure 5.11: Ch. 1 and Ch. 2 show the voltage at the base terminals of the Q1 and Q2 transistors (see Figure 5.7). The base of Q2 is set to a DC voltage of 1.2V while the base terminal of Q1 is driven to achieve the needed commutation.

5.3 Prototype II

The second prototype utilizes a self driven topology to create the floating current source. This design is an important change from the first one because Prototype I loaded the input to drive the diff. pair. The design introduces two DC-blocking capacitors in series with the original series reactive network. These two capacitors allow for the voltage across the center capacitor to be DC shifted to a common-mode level agreeable to the differential pair. Figure 5.12 shows the overall topology. The value of the center capacitor is chosen such that the AC voltage magnitude is large enough to commutate the diff. pair. Connected to each end of the capacitor is a DC voltage of 1.2V which elevates the AC voltage to a range in which the the lowest possible voltage will keep the base of both transistors above their turn off voltage. This ensure proper operation of the differential pair. Also, by using each end of the capacitor as the voltage for each base, the design ensures that the base voltage is ninety-degree phase shifted from the current delivered to the load. This is because a capacitor is naturely a 90 degree phase shifter because of the reactive nature of its impedance.

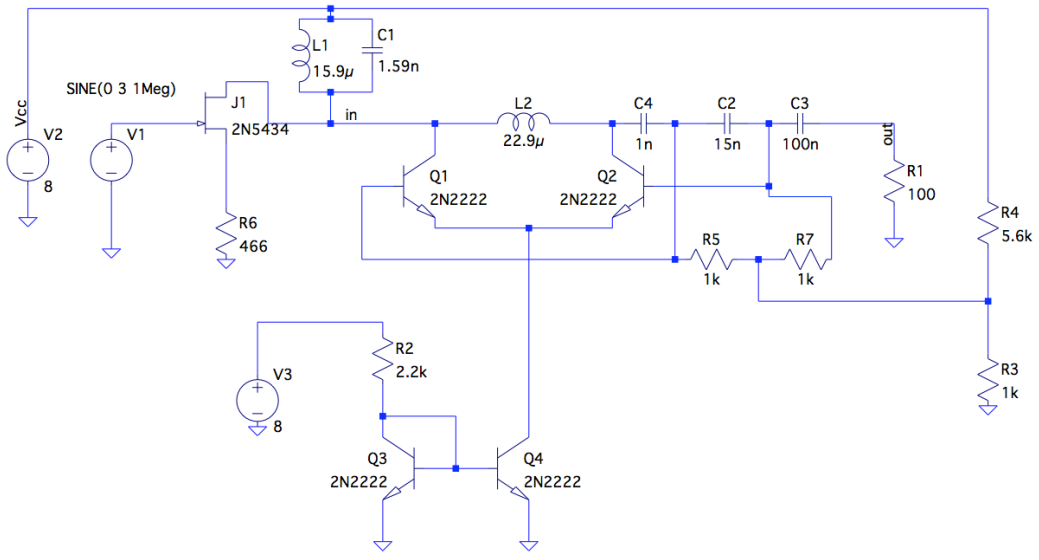


Figure 5.12: Prototype II schematic.

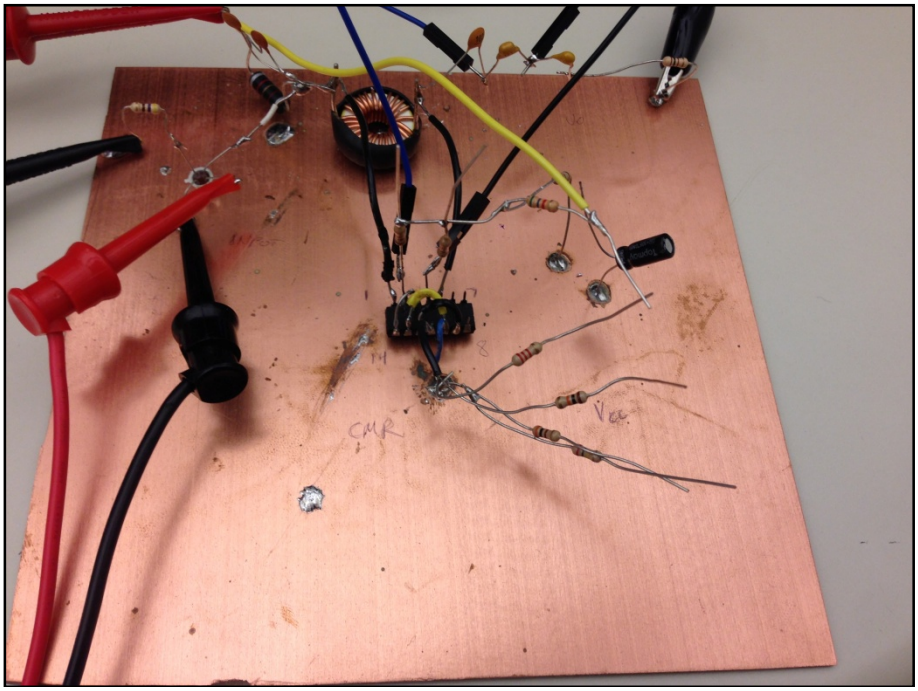


Figure 5.13: Prototype II physical circuit utilizing the three capacitor self-driven design.

Figure 5.13 shows the actual "dead bug" implementation of the Prototype II circuit, which uses the three capacitor self-driven design to commutate the diff. pair.

Figures 5.14 and 5.15 show circuit operation with the three capacitor structure. Similar, to the Prototype I adjusted design, this circuit shows a voltage drop across Ampl(1) when the active network is turned on. Ampl(1) of Figures 5.14 and 5.15 show the JFET drain voltage, while Ampl(2) in the Figures shows the relatively unchanging load voltage. The small voltage change of 49 mV at the load is present because of the odd order harmonics generated by the diff pair implemented floating current source. This voltage difference can be filtered out.

Figure 5.16 shows the diff. pair base voltages, and the MATH subtraction of the two. The out of phase, lower magnitude, signal is the subtraction of the two base signals and shows that the differential pair is being properly commutated.

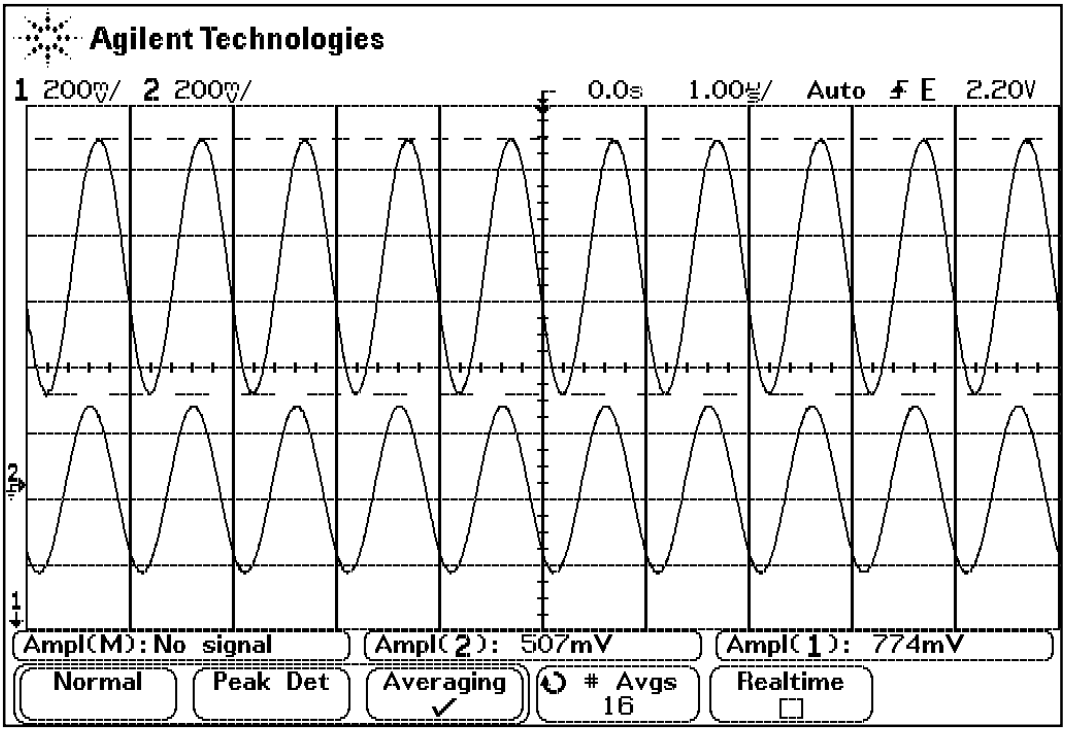


Figure 5.14: JFET drain (Channel 1) and Output (Channel 2) Voltage Waveforms with the current mirror disabled such that the differential pair has no tail current.

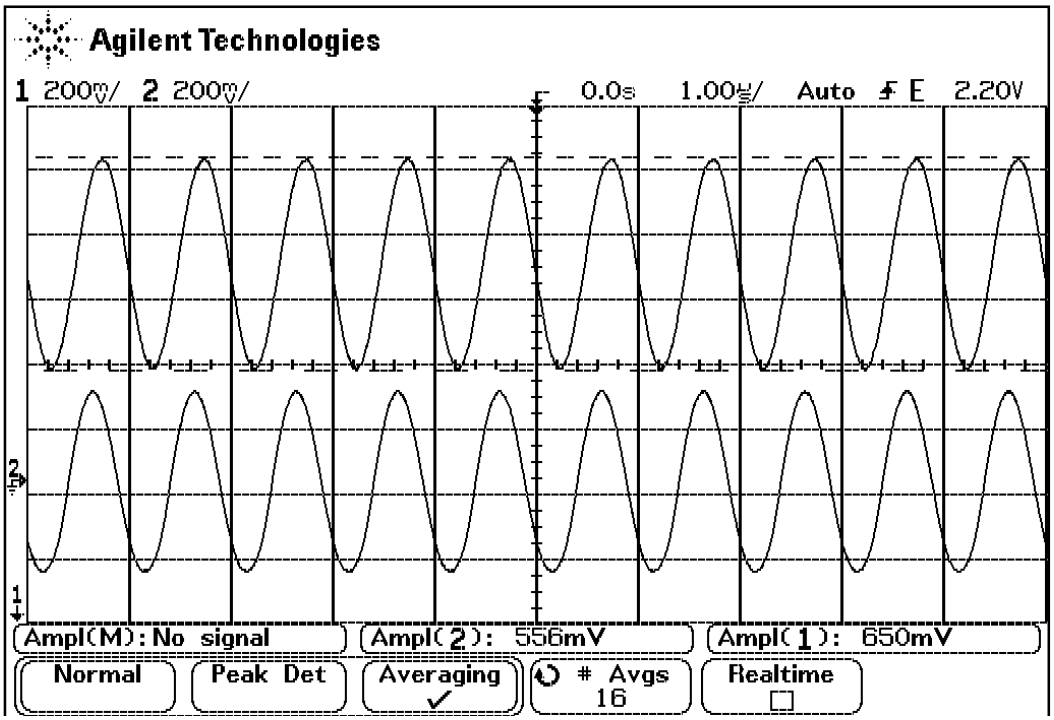


Figure 5.15: JFET drain (Channel 1) and Output (Channel 2) Voltage Waveforms with the current mirror resistor set to 2.2k Ohms for a tail current of 3.3 mA.

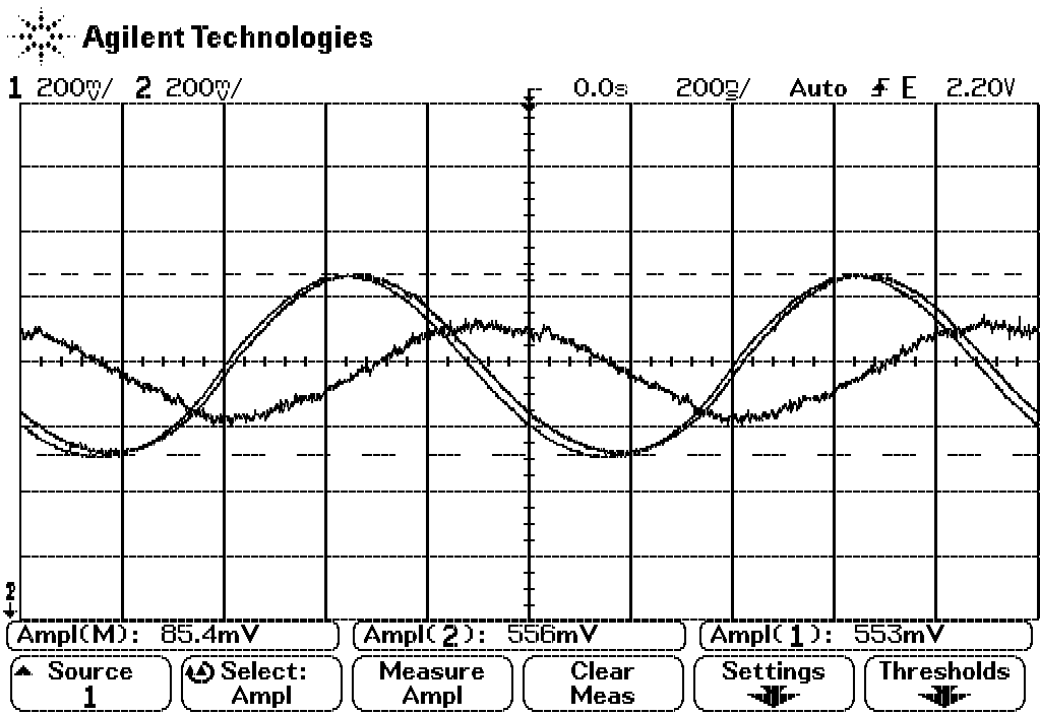


Figure 5.16: Ch. 1 and Ch. 2 show the voltage at the base terminals of the Q1 and Q2 transistors (see Figure 5.12). The math subtract function shows the difference between these two waveforms. This difference is what commutates the differential pair.

6. Component Sizing & Circuit Dangers

Appropriate selection of component values and source magnitudes is paramount to our design. In this chapter, we will discuss important component-related issues and their implications. These issues were skipped in the software implementation and prototyping sections to allow for the bigger picture to dominate the design. Here we discuss the benefits and drawbacks of more subtle design changes.

6.1 Input Transistor

The first component chosen for this design is the input transistor. This component should be the easiest to choose because the user should have specifications that they must meet, and therefore can choose a transistor that satisfies these parameters. These parameters should be gain, linearity and bandwidth. The active circuitry added to the system is intended to allow for high PAPR and therefore this is the one parameter that does not need to be addresses by the input transistor.

6.2 RF Choke

The RF choke circuit is the simplest circuit and requires little to no design effort. The designer must solely be mindful of the bandwidth of the circuit. The RF choke is meant to prevent any portion of the desired signal, coming from the transistor, from shunting to ground. Therefore, depending on the application of this design the notch bandwidth will vary.

6.3 Series Resonant Network

The next circuit to be examined is the series resonant network. The capacitance of this network is solely chosen based on the inductor, and therefore should be chosen second. The inductor should be chosen based upon impedance. The impedance of the inductor must have a proper ratio with the load to get a sufficient voltage reduction when the floating source is activated. The larger the impedance of the inductor the more voltage drop will be experienced across the inductor. This means that the voltage difference between the output voltage and transistor collector/drain voltage is dependent upon proper selection of the inductor. This value will change based on the voltage limitations of the transistor and the desired output voltage at the load. For example, if the designer would like to have an 8V swing on the output but a 4V swing on the transistor then the inductor impedance must have twice the value of the load impedance.

Second, once the inductor value has been chosen the overall capacitance must be chosen to satisfy equation 2.16. This value is therefore set based upon the desired frequency of the series resonant network and the inductor. For the three capacitor implementation the next step is choosing the value of the three capacitors. The middle capacitor must be chosen first. The middle capacitor is used to commutate the differential pair. The impedance of the capacitor must be chosen such that the current through the capacitor multiplied by the impedance of the capacitor will give a large enough voltage to commutate the differential pair. For example, in the case of a 1 MHz frequency, an average load current of $4.5mA_{p\text{-}p}$ and a desired commutation voltage of $50mV_{p\text{-}p}$ a capacitor value of 14nF is determined using the equation:

$$V_C = I_C \times \frac{1}{j\omega C} \tag{6.1}$$

where ω is angular frequency.

The additional two components must be chosen two create the series resonance at the frequency of interest and therefore infinitely many combinations exist. Capacitors in the following equations are labeled based on Figure 5.12.

$$C_{total} = C_4 \,||\, C_2 \,||\, C_3 \tag{6.2}$$

To decide which combination of these two capacitors is "best" we must recall what purpose they serve. The center capacitor is sized to create a voltage difference large enough to commutate the differential pair. This voltage alone is not sufficient because the base nodes of the differential pair must be DC biased so that the diff. pair transistors are in forward active mode of operation. This means that the base nodes of the transistors are DC biased up to some DC voltage and then driven out of phase. The magnitude of the differential drive is set by the center capacitor, but the magnitude of each individual voltage waveform is set by the side capacitors. If the voltage magnitude of the transistor base nodes is too large than the base node voltage could swing too low, causing the transistor to turn off, or swing too high, causing the base node to have a higher voltage magnitude than the collector. Therefore, the side capacitors must be chosen to minimize the common-mode voltage swing experienced by the diff. pair.

It is best to make the capacitor furthest from the load,C4 in Figure 5.12,smallest (in terms of capacitance). This means that the impedance of C4 is largest, due to the inverse relation between capacitance and capacitive reactance. This is ideal because the large voltage magnitude present on the collector of Q2 will be dropped significantly. Subsequently, C3 must be as large as possible, in terms of capacitance. This makes the C3 impedance as small as possible so that the magnitude of the voltage from the load to the center capacitor minimized. The following equations show the suggested relations (note C_2 is fixed by 6.1 and the total is set by 6.2):

$$C_4 \geq C_{total} \tag{6.3}$$

$$C_4 << C_3 \tag{6.4}$$

6.4 Tail Current

Tail current is another important consideration for our design. As tail current is increased power delivery is shifted from the transistor to the active network. Recall that the diff. pair under commutation emulates a floating current source with rectangular shape and magnitude of one-half

the tail current. Such a waveform has fundamental component of magnitude (2/π) I_{tail}. To avoid voltage reversal at the drain of the main device (previously covered in section 2.2), we must satisfy the follow relationship under all operating conditions:

$$I_{main} \times R_{load} > \left[\frac{2}{\pi} \times I_{tail}\right] \times X_L \qquad (6.5)$$

Here I_{main} is the magnitude of the current delivered by the main device, the JFET in our case. I_{tail} is the bias current of the diff. pair – a DC but adjustable quantity and X_L is the reactance of the series inductor.

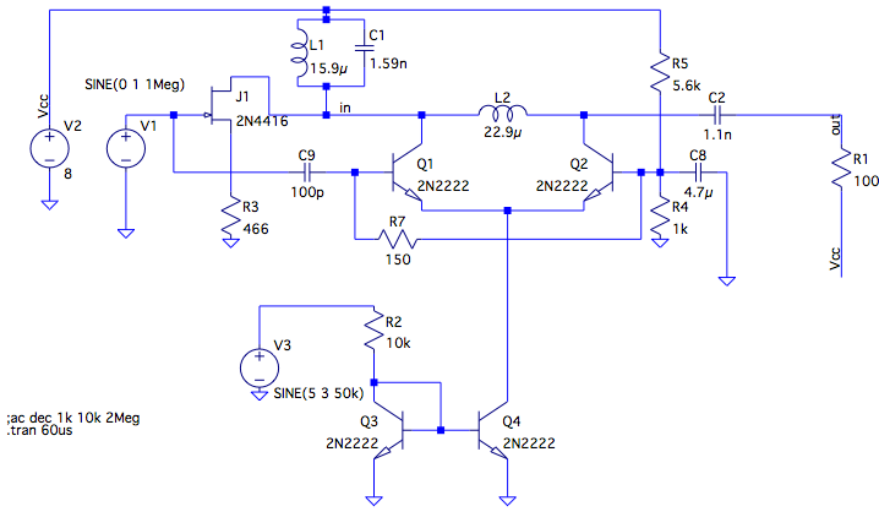


Figure 6.1: The circuit can be regarded as a controlled resonant amplifier. The control, V3, is used to change the tail current of the diff. pair modifying the amount of "help" it provides to the main device.

Figure 6.1 and 6.2 show how modifying the tail current affect the voltage at the transistor and therefore contribute to the robustness of this design. If the system can predict the input signals than the circuit can self-adjust to keep the transistor in the correct operating range without affecting the output gain or linearity. Again the plot shows slight variation in output voltage but these are caused by the odd harmonics that can be removed by proper filtering.

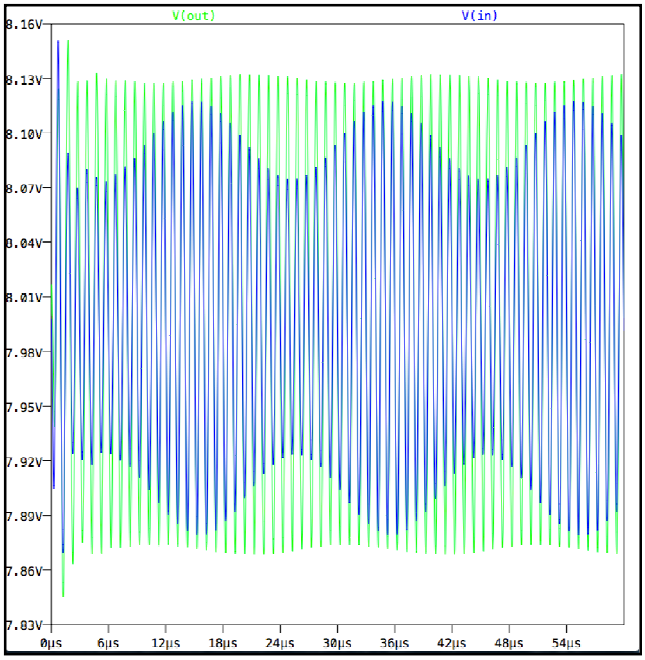


Figure 6.2: Tail Current Modulation Plot

6.5 Differential Pair Commutation

Lastly, the commutation of the differential pair is an important part of this circuit. If the differential pair is commutated at the wrong phase offset from the original signal than the voltage at the transistor could be increased instead of decreased. The differential pair is attempting to replicate the signal exactly on either side of the inductor with a phase shift to cause destructive interference on the transistor side. This means that if the phase is incorrect than the voltages can constructively interfere causing the opposite effect. An example of this is shown in Figure 6.3 and 6.4.

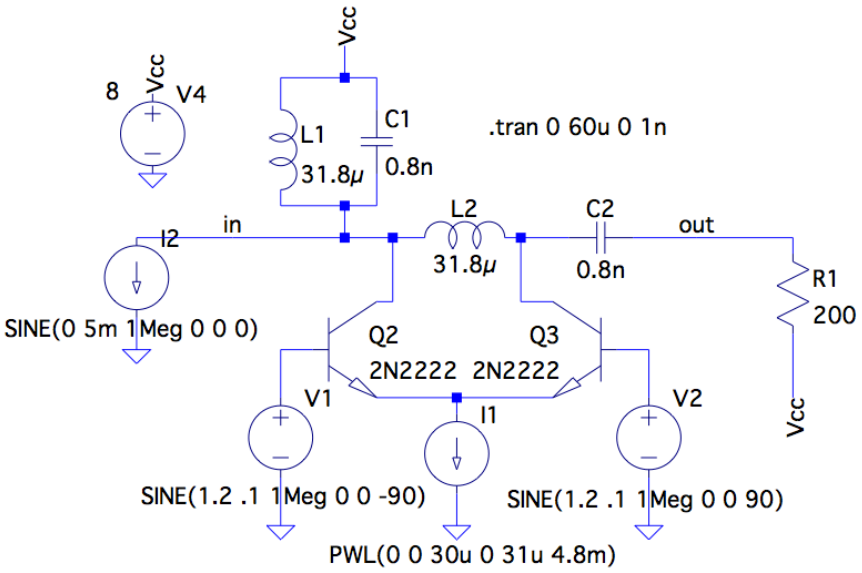


Figure 6.3: Schematic used to demonstrate diff. pair toggled with the wrong phase difference.

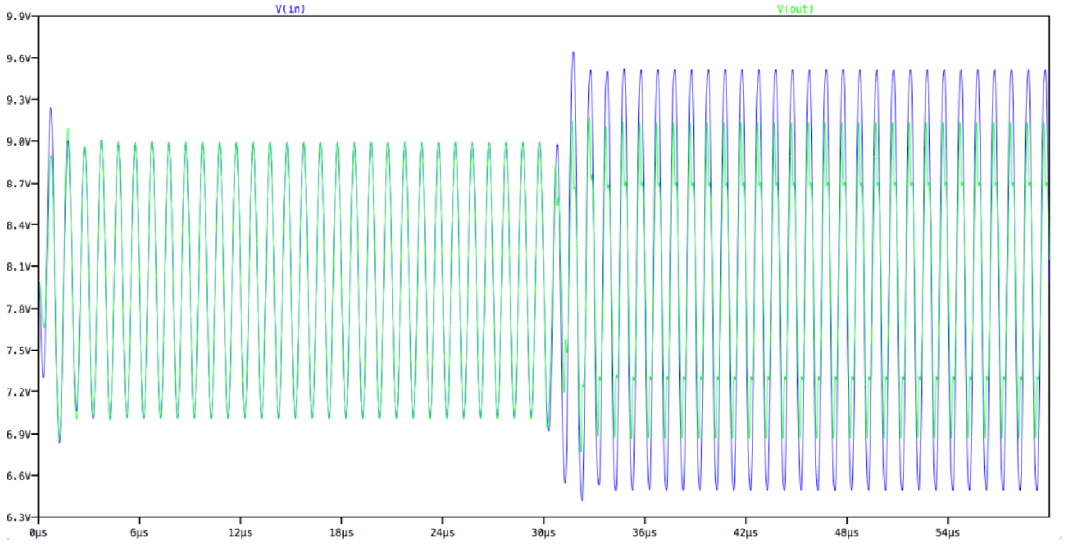


Figure 6.4: Plot of diff. pair commutated to increase the voltage at the load, rather than maintain the gain of the input transistor.

7. Conclusions & Future Work

7.1 Conclusions

This work proves that series power combining of a current source with a “helper” voltage source is possible. Our design shows how to synthesize a voltage source with the required 90-degree phase shift and a magnitude controlled by a DC signal. The design also shows that the odd order harmonics, generated by the diff. pair commutation, will distort the signal at the load, but these odd order harmonics are significantly smaller than the fundamental and can be filtered out. Also, this work uses practical components to implement the design proving that the circuit should work in a real world design. The current mirror is the only component that must be changed for commercial design. A current mirror consumes twice the power that is necessary for circuit operation since the current setting branch consumes the same current as the delivery branch. This component can be easily replaced with more power efficient designs.

This work also shows that the floating voltage source circuit can be self-driven. The initial design shown in Prototype I derives the commutation signal from the input of the amplifier, which may introduce loading and potentially increase the distortion of the overall amplifier. However, in Prototype II, we show that proper selection of three capacitors at the output allows for the differential pair to drive itself. This design was the pivotal step in demonstrating that our combination strategy is practical for real world application.

7.2 Two Source Topology Comparison

There are four distinct methods of two source power combining. These topologies were presented in Figures 2.2 and 2.3. The Doherty amplifier, Figure 2.9 was presented as an example of a parallel combination two source strategy. The two source topology used is a voltage source "main" and current source "helper", presented in Figure 2.2a. The upper branch of the Doherty amplifier is the "main" source. The input voltage is converted to a current by the Class AB amplifier and then converted back into a voltage by the impedance inverter. This creates a voltage controlled voltage source with a 90 degree phase shift. In the other branch, the input voltage passes through an impedance inverter to match the 90 degree phase shift of the upper branch. This voltage is then converted into a current to serving as the "helper" source. This design loads the input voltage twice to create the two-source power combining technique, and utilizes a Class C amplifier as its helper source. This means that the design has two sources of distortion that can be improved.

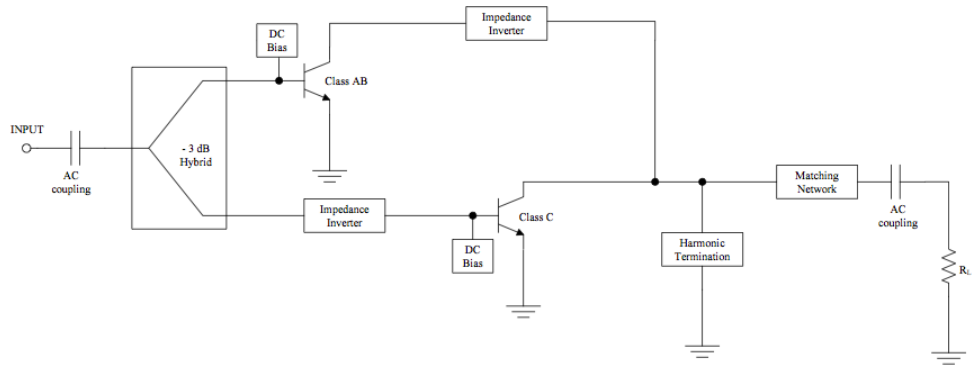


Figure 7.1: Doherty amplifier block diagram. [10]

Matt King and Cody Nelson both worked to create a better design by modifying the Doherty amplifier. Their designs detach the Class C amplifier and attempt to replace it, with a negative resistance. This converts the design into a voltage source in parallel with negative resistor topology, presented in Figure 2.2b. This design was unsuccessful because the harmonics created by the negative resistor caused the overall structure to oscillate. Further study is needed to determine the merits of this two source topology.

This work is focused on the dual of the Doherty design. The topology, presented in Figure 2.3a, is a current source "main" in series with a voltage source "helper". This design was challenging because of the need for a floating voltage source, but utilizing a differential pair and resonant network a floating voltage source was created. The tail current used by the differential pair and the impedance of the inductor were determined to be the two variables needed to determine the magnitude of the helper voltage source. This means that if the tail current can be controlled then the magnitude of the helper voltage source can be adjustable. This means that this design can compensate for High Peak-to-Average Power Ratios (PAPR) without the need for loading the input twice. Also, Class C amplifiers can be avoided.

7.3 Future Work

The next step is to redesign the circuitry for cellular technology implementation. While our design was used to test the theory, this design is not helpful for application in the cellular or other wireless markets. High PAPR is common in cellular technology modulation schemes and it is this market where the two-source power combining technique will be most advantageous. The combining technique presented can also be used in the 802.11 (WiFi) family of standards. Those use OFDM signaling to have large PAPR.

The first task for making the design ready for the cellular market is to test the design at higher frequencies. One megahertz was a reasonable frequency to test the theory and practicality of this circuit, but much higher frequencies are used for the cellular market. [4]

We envision creating a linear power amplifier with digitally-controlled helper activation. The cellular market uses digital signal processing to create the complex modulation schemes used for wireless data transmission and therefore is capable of determining when the high peaks will occur in the signal. This means that the DSP circuits are capable of "knowing" when to turn on or increase the tail current in our design. As discussed in section 6.4, variation of the tail current adjusts how much power the helper source will add to the circuit. This means that the tail current

circuit, currently a current mirror, would benefit from being an adjustable current source. If the DSP can control the current value and when it is on, then the design can be optimized for high PAPR signals. The use of DSPs to assist power amplifier efficiency has been studied before and can be seen in [19]. Therefore, addition work should be done to incorporate a more controllable and power efficient tail current source. Figure 7.1 shows the digital control implementation for commercial application.

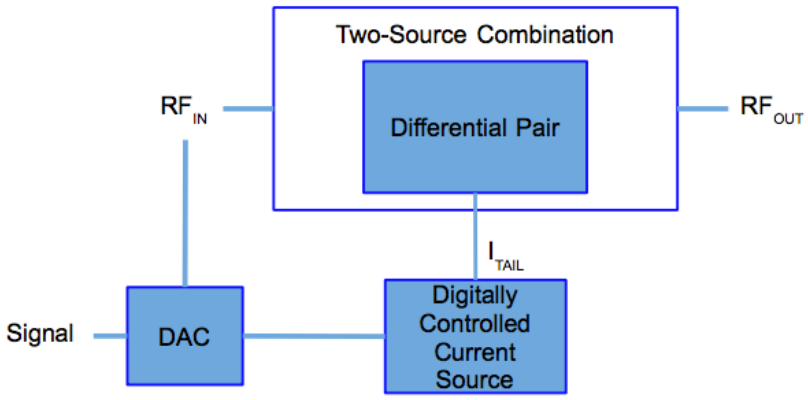


Figure 7.2: Commercial Top Level Schematic

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Appendices

A.1 Peak-to-Average Power Ratio (PAPR)

With the ongoing push for wireless systems to accommodate more users and support higher data rates more efficient modulation schemes have been created that are more advanced than simple FM and AM modulation used for radio broadcasting. One of these modulation schemes is *Orthogonal Frequency Division Multiplexing* (OFDM) which is used in 4G long-term evolution (LTE) wireless systems[11]as well as 802.11 a/g Wireless LANS[11]. OFDM is a wideband communication scheme in which baseband data is modulated into multiple orthogonal subcarriers, which are then summed together for transmission. The subcarriers have different frequencies, magnitudes and phases leading to constructive and destructive interference. The resulting baseband signal exhibits large magnitude variation and when up-converted to RF creates wireless signal with large crest factor. Signals with large crest factor are said to have high *peak-to-average power ratios*(PAPR)[1]. PAPR is defined as:

$$C = \frac{|P|_{peak}}{P_{rms}} \qquad \text{(A.1)}$$

where $|P|_{peak}$ is the peak amplitude of the signal, and P_{rms} is the RMS (root-mean-squared) of the signal. To demonstrate this phenomenon, a simple example is given in Figure A.1[13], which shows how the combination of multiple sinusoids can create one sinusoid with a high PAPR.

[1]Also known as *crest factor* (C)

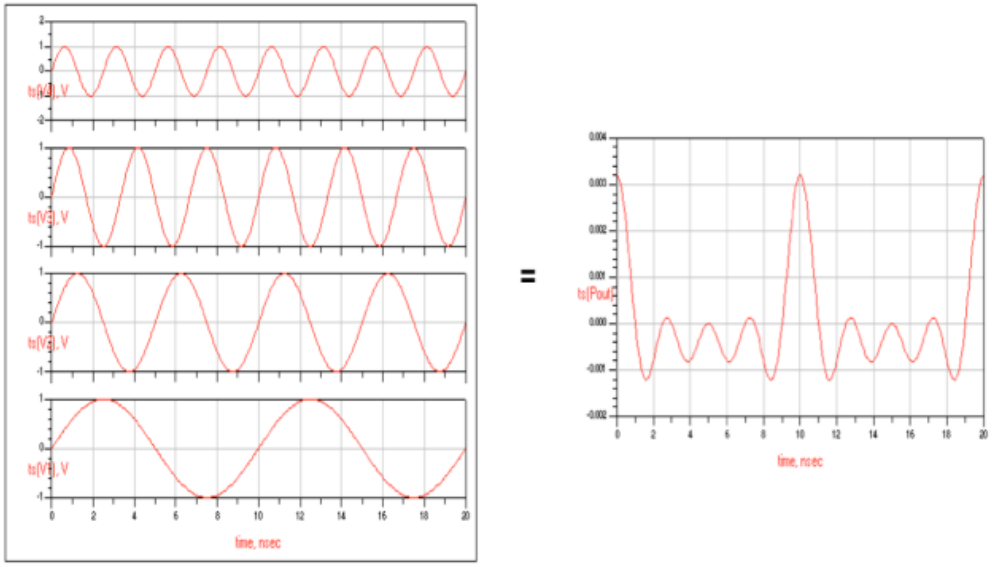

Figure A.1: Summation of signals with varied amplitude and phase forming a high PAPR signal.[13]

A real example of an OFDM signal found in an LTE system is shown below in Figure A.2 the high PAPR in practical modulation schemes. Further study of PAPR can be found in [18].

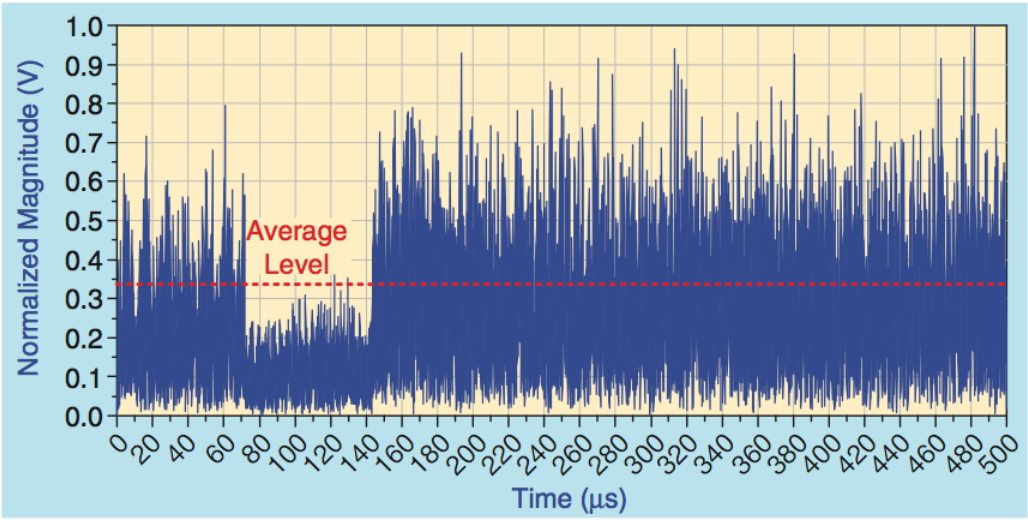

Figure A.2: Actual time-domain waveform of an LTE OFDM modulated signal. [9]

A.2 Linearity and Efficiency Tradeoffs in Power Amplifier Design

OFDM, WCDMA, and WiMAX signals are all examples of high PAPR modulation schemes. Because of their large amplitude variation, such signals are difficult to amplify efficiently. The two equations used to calculate the efficiency of a power amplifier are:

$$PE = \frac{P_{out}}{P_{DC}} \tag{A.2}$$

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{A.3}$$

Power efficiency (PE), given by (A.2), is a measure of the percentage of DC power drawn from the power supply that is converted into useful RF output power. Power-added efficiency (PAE), given by (A.3), uses a ratio of the power gain of the amplifier to the DC power drawn from the supply. A typical PAE curve for a conventional Class AB amplifier is shown in Figure A.3.

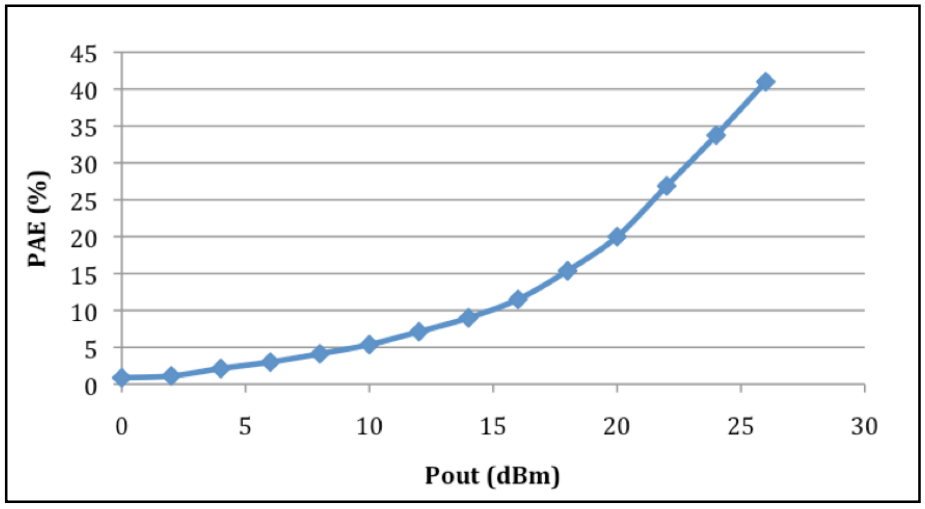

Figure A.3: Typical PAE curve for conventional Class AB amplifier. [10]

When a signal has a high PAPR the input power to the amplifier, and hence the output power, must be reduced in order to avoid saturation, but Figure A.3 shows that as one reduces the output power, the PAE is reduced. Therefore, a linear and power efficient design is needed to replace the current conventional Class AB amplifier. Linear amplifiers that have both good

linearity and good PAE have been a topic of active research in the last 10-15 years. Several such topologies are known [6], [7] ,[14], and all of them are complex multi-transistor architectures.

A.3 Power Amplifier Classes of Operation

A brief overview of the linear, or *current-mode*, classes of operation for a power amplifier is required, since power amplifiers are the focus of this thesis. Other modes such as Class D, Class E, and Class F, are covered extensively in other works—see [5] and[16]—but are omitted from the discussion here.

Figure A.4 shows the conduction angles associated with the different linear classes of operation using an ideal (piece-wise linear) transistor I-V characteristic. In Class A, the bias point of the transistor is set such that the transistor will conduct for the full cycle of the input signal, thus resulting in a conduction angle of 2π. A Class B amplifier has the bias point set at the "knee" of the transistor I-V characteristic, thus the transistor is off for the negative portions of the input signal. This bias results in a conduction angle of π. Any amplifier with a conduction angle which is less than π is defined as Class C. Class AB amplifiers (not shown in Figure A.4) operate with a conduction angle between π and 2π, although the Class AB amplifier is often placed near the knee of the I-V characteristic.[2] A summary of the conduction angles and their theoretical efficiencies is presented in Table A.1.

PA Class	Conduction Angle	Max. Theoretical Efficiency
Class A	$\theta = 2\pi$	50%
Class AB	$\pi < \theta < 2\pi$	78.5%
Class B	$\theta = \pi$	78.5%
Class C	$\theta < \pi$	100%

Table A.1: Conduction angles and theoretical maximum efficiencies for current-mode amplifiers. [10]

[2]These classes of operation were defined during the prevalence of vacuum tubes, which operated at somewhat ideal characteristics. An ideal Class B bias point is difficult to obtain using modern solid-state devices (which do not operate with ideal I-V characteristics), and therefore most designs that target this mode of operation technically operate in Class AB.

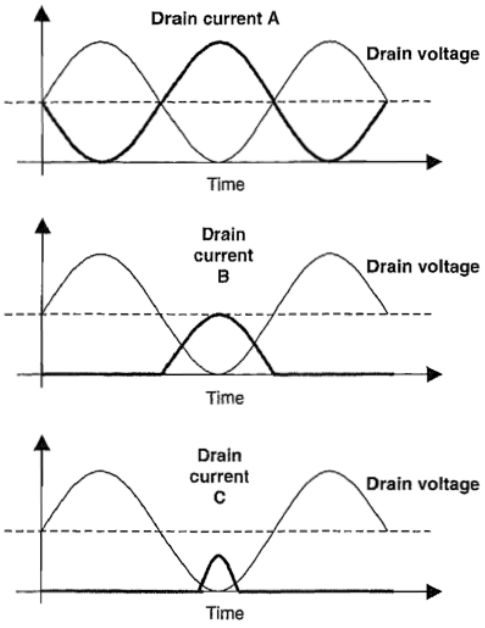

Figure A.4: Definition of conduction angle for Class A, B, and C operation. [10]

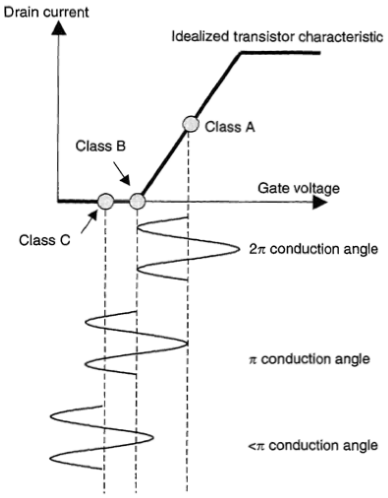

Figure A.5: Voltage and current waveforms for Class A, B, and C operation.[10]