TELKOMNIKA Telecommunication, Computing, Electronics and Control
Vol. 18, No. 5, October 2020, pp. 2618~2627
ISSN: 1693-6930, accredited First Grade by Kemenristekdikti, Decree No: 21/E/KPT/2018
DOI: 10.12928/TELKOMNIKA.v18i5.14034

A power efficient delta-sigma ADC with series-bilinear switch capacitor voltage-controlled oscillator

D. S. Shylu[1], P. Sam Paul[2], D. Jackuline Moni[3], J. Arolin Monica Helan[4]
[1,3]Department of Electronics and Communication Engineering, Karunya Institute of Technology and Sciences, India
[2]Department of Mechanical Engineering, Karunya Institute of Technology and Sciences, India
[4]Department of Electronics & Communication Engineering, Karunya Institute of Technology and Sciences, India

Article Info

Article history:

Received Sep 3, 2019
Revised Mar 28, 2020
Accepted Apr 24, 2020

Keywords:

Amplifier
Continuous-time (CT)
Delta-sigma (ΔΣ)
Loop filter
Switch capacitor circuits
Voltage-controlled oscillator
(VCO)-based ADCs

ABSTRACT

In low-power VLSI design applications non-linearity and harmonics are a major dominant factor which affects the performance of the ADC. To avoid this, the new architecture of voltage-controlled oscillator (VCO) was required to solve the non-linearity issues and harmonic distortion. In this work, a 12-bit, 200MS/s low power delta-sigma analog to digital converter (ADC) VCO based quantizer was designed using switched capacitor technique. The proposed technique uses frequency to current conversion technique as a linearization method to reduce the non-linearity issue. Simulation result show that the proposed 12-bit delta-sigma ADC consumes the power of 2.68 mW and a total area of 0.09 mm² in 90 nm CMOS process.

Corresponding Author:

D. S. Shylu,
Department of Electronics and Communication Engineering,
Karunya Institute of Technology and Sciences,
Karunya Nagar, Coimbatore-641114, Tamil Nadu, India.
Email: mail2shylu@yahoo.com

1. INTRODUCTION

The Delta-sigma (ΔΣ) ADC were widely used for signal acquisition and processing applications. Hence such types of ADCs were used as codec and hearing aids which require large dynamic range for signal paths [1-4]. When compared with the Nyquist rate converters, ΔΣ ADC is easier to design as they do not require analog components with stringent parameters. Oversampling converter samples the input signal bandwidth and the need for an anti-aliasing filter is eliminated. With medium oversampling ratio and by increased sampling rate high-resolution ADC can be designed. This efficiently reduces the entire power consumption while maintaining the required resolution [5]. Scaling of voltage is applicable to digital circuit design in reducing the heat dissipation at the trade-off of speed factor.Several techniques have been reported to address this problem such as body-driven circuits, SAR operation, sub-threshold operation [6-9] and zero crossing circuits [10, 11] and the performance of these circuits were very less.The delta-sigma ADC is a very efficient structure with oversampling and noise shaping properties.The process scaling factor and bandwidth has been improved in continuous ΔΣADC. High performance analog circuits include op-amp less pipelined ADC [12, 13], energy efficient successive approximation register (SAR) ADC [14, 15] and digital calibrated technique [16, 17]. To process the signal in time domain voltage-controlled oscillators (VCO) play a major role [18-24]. The VCO outputs introduce quantization error in VCO when the flip-flops are synchronized.

Several existing techniques in ΔΣ ADC architecture reduce the power consumption at the cost of speed [25-29]. Hence the performance of ADC can be improved by transferring the signal processing task to digital domain and by applying proper scaling methodology. In the proposed design, series-bilinear switch capacitor based VCO Quantizer is used to eliminate the harmonic distortion and non-linearity by frequency to current conversion-based linearization technique. The non-linearity of the developed and accomplished VCO based quantizers is improved by frequency to current conversion method. This paper is organized as follows. The conventional ΔΣ ADC architecture, circuit designs with its layout are shown and explained in section 2. Section 3 describes the proposed work of series-bilinear based VCO. Section 4 describe the 4 result and discussion. Section 5 describes the conclusion.

2. CIRCUIT DESIGN OF CONVENTIONAL DELTA-SIGMA ADC

2.1. Two stage differential operational amplifier

Op-amp is the most important block of ADC and in CMOS technology the design of operational amplifiers is a challenge as the transistor channel length and voltage reduces. The advantages of the two-stage op-amp are the good gain, high output swing, low noise and good bandwidth over folded cascade op-amp [25]. The differential gain structure consists of M_1, M_2, M_3, and M_4 against the structure of the conventional operational amplifier as in Figure 1. The input stage of the op-amp is constructed using M_1 and M_2 NMOS transistors. For the active load of input differential stage, M_3 and M_4 transistors are used. M_7 is a load and M_6 is a driver for current sink load inverter. The output of the M_2 transistor was boosted using current source represented as M_6 transistor [26].

The performance of two-stage CMOS op-amp is based on the width and length of the transistor. Care must be taken to assure that the transistors are operating in the saturation region and not in the triode region. This is because the triode region causes the transistor to behave in a non-linear fashion leading to poor transient response as well as the reduction of the overall gain [27]. The layout of the two-stage amplifier is shown in Figure 2. The obtained area is 75.79*65.1µm² which has a total area of about 4933.9µm². The physical design steps including DRC check, LVS check, QRC Check and Post-layout simulation was done for the two-stage amplifier.

2.2. Loop filter

The loop filter of ΔΣ ADC provides the noise-shaping property. It suppresses the nonlinearity present in the VCO. To achieve a higher order noise shaping, the order of the loop filter must be increased. In this work, RC topology is chosen for its excellent linearity. In order to suppress the distortion, a high gain loop filter is required [28]. Figure 3 shows the first order loop filter integrator. It is used because of its linearity and it is a fully differential circuit that converts square wave input into a triangular waveform. The input is given to the coupling capacitor. The high value of transconductance is achieved by adjusting the W/L ratio of the transistors. The circuit of the loop filter is shown in the Figure 3. Figure 4 shows the layout of the loop filter. The obtained area of the loop filter integrator is 59.06*137.94µm² which has a total area of about 8111.3µm². GDS-II file is also obtained for the layout.

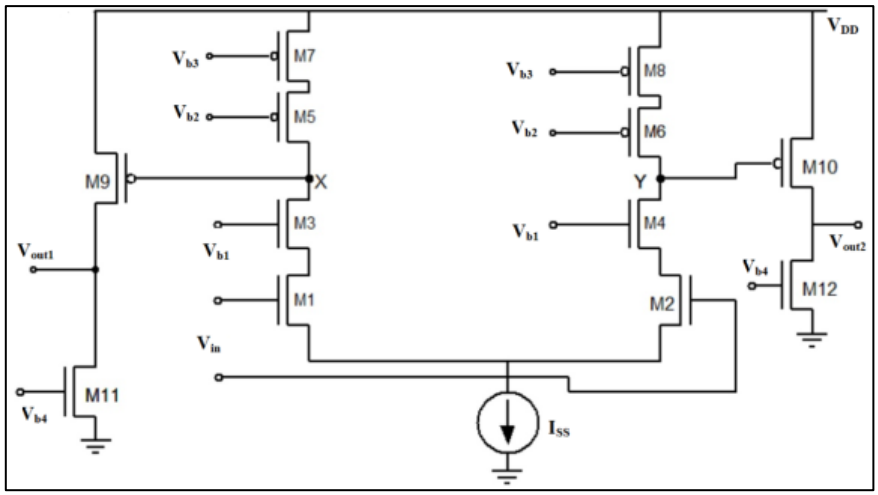

Figure 1. Circuit diagram of two-stage differential amplifier

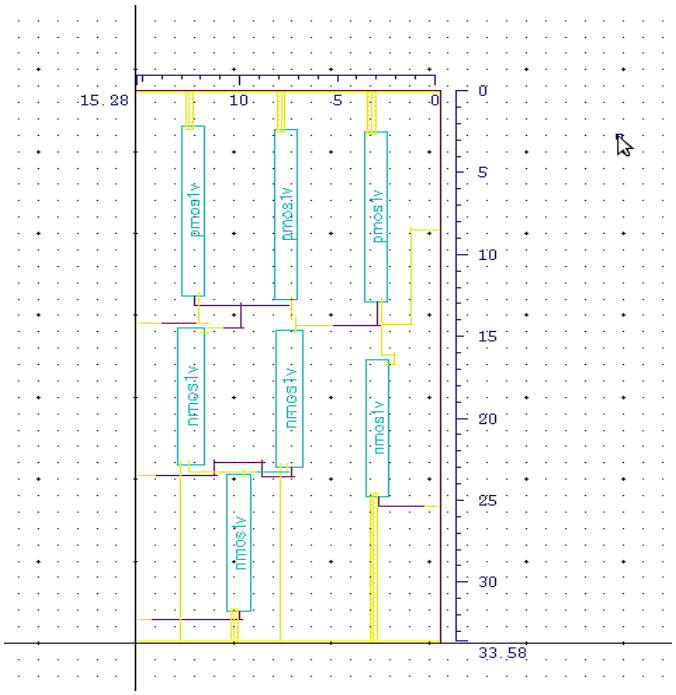

Figure 2. Layout for the two-stage amplifier

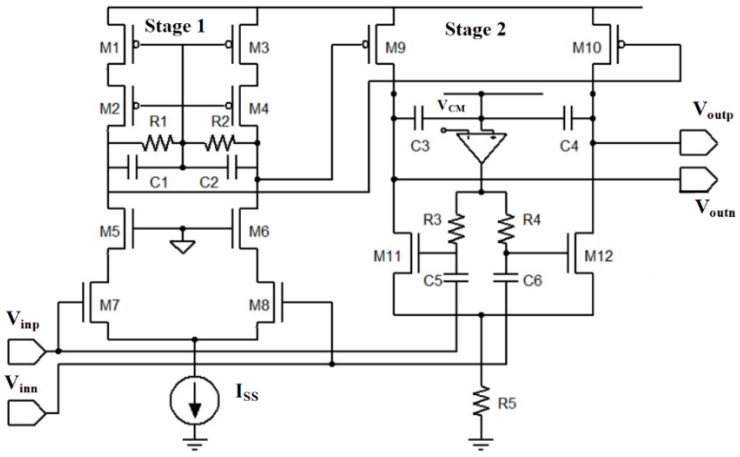

Figure 3. Op-amp used in the loop filter integrator

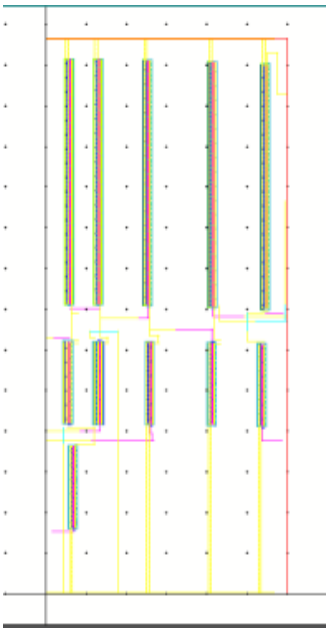

Figure 4. Layout of the loop filter

2.3. Dynamic latch comparator

In dynamic latch comparators, two cross-coupled CMOS inverters are used for regeneration as in Figure 5. A clock is used to set the comparator in active or standby mode. The reset operation is achieved through the shorted transistor M_6 between the two cross-coupled inverters. When the enable signal goes low, the circuit enters into the comparison phase. By adjusting the W/L ratio of the transistors, the high value of transconductance can be achieved [29, 30]. The major drawback of the dynamic latch comparator is the offset error caused by transistor mismatch and unbalanced charge residues [30]. Figure 6 shows the layout of the dynamic latch comparator. The obtained area is 22.095*46.74 µm² which has a total area of about 1032.7 µm.

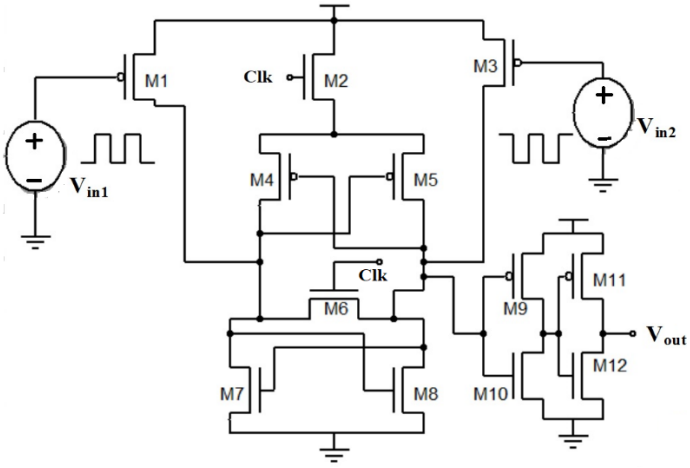

Figure 5. Dynamic latch comparator

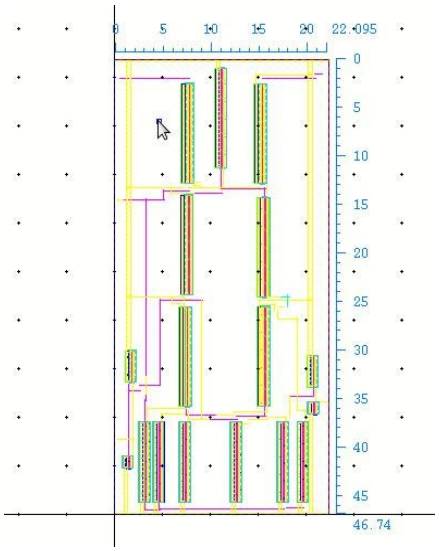

Figure 6. Layout of the dynamic latch comparator

2.4. Voltage controlled oscillator based quantizer

The most important building block of ADC is labelled as VCO based Quantizer. VCO produces a continuous time placed signal whose frequency is precisely corresponding to the input analog signal. The large value of transconductance is accompanied by regulating the W/L ratio of the transistors [31, 32]. It quantizes the signal on the individual stage and achieves the comparable digital output [33]. There are mainly two types of building blocks for VCO placed ADCs named as counter based architecture and phase detector-based architecture [34]. The VCO quantizer comprises of the multistage ring oscillator (RO), two arrays of DFFs and an array of XOR as shown in Figure 7. The power consumption obtained for VCO quantizer is 408.7µW. The layout of the VCO Quantizer is shown in Figure 8. The obtained area is 150.02*229.03 µm² which has a total area of about 34359 µm².

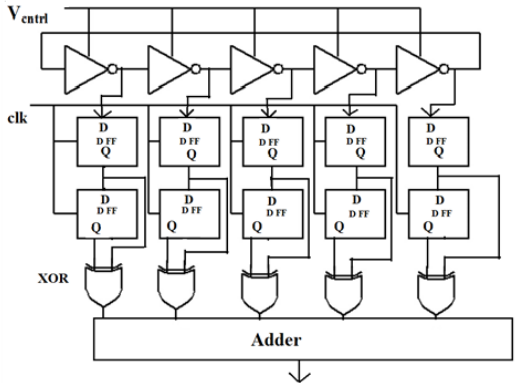

Figure 7. VCO Quantizer based on multistage ring oscillator

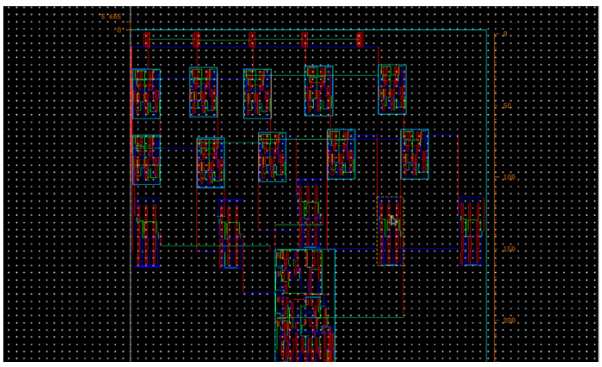

Figure 8. Layout of VCO quantizer

2.5. Digital to analog converter (DAC)

The essential operation of DAC is to cause the digital output of ADC balanced to the analog input. Delta-sigma ADC uses multi-bit quantizer and multi-bit digital-to-analog (DAC) block to fix up the analog signal [35, 36]. Figure 9 shows that the layout of the Digital to Analog Converter (DAC). The obtained area is 15.28*33.58 µm² of which the total area is about 513.1024 µm².

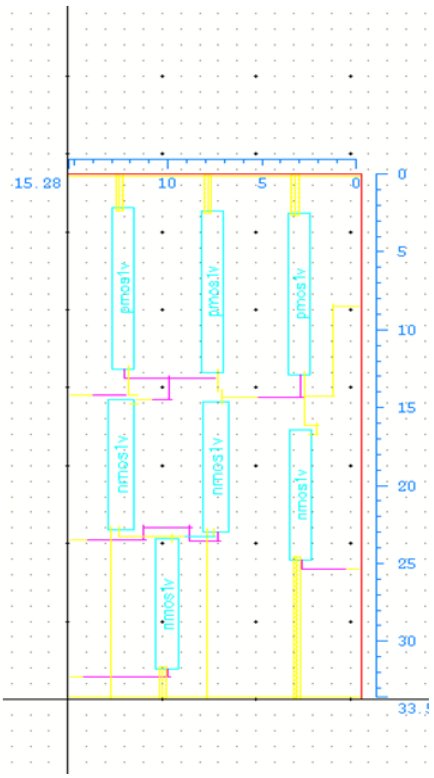

Figure 9. Layout of the DAC

3. PROPOSED SERIES -BILINEAR SWITCH CAPACITOR VCO BASED QUANTIZER

Switched capacitor circuits are used in the discrete signal processing applications [37]. The operation of the switch capacitor circuit is based on the charging and discharging of charges in capacitors. The switched capacitor emulates the resistor and classified into three types named as parallel, series, and bilinear techniques. Switch capacitors are mainly used to minimize the chip area [38]. Figure 10 shows the series-bilinear switch capacitor circuit. The proposed work used is the integration of a series capacitor switch and bilinear capacitor switch to reduce the non-linearity and harmonic distortion. The significance of the switch capacitor technique is to have a good dynamic range and accurate frequency. Accuracy is obtained from filter coefficients which are determined by capacitance ratio. In order to reduce the non-linearity, clock phases are introduced for charge transfer and non-overlapping clock phases. In the previously reported work, the VCO Quantizer is affected by linearity issues and noise distortion. In order to reduce the noise distortion, series-bilinear switched capacitor technique is proposed. The main difficulty in VCO-based Quantizer is the nonlinearity. Linearization technique used in this proposed work is FCC technique [39] (Frequency to the current converter) in which the harmonic distortions are reduced. The proposed VCO-based Quantizer uses two parasitic capacitances and two switches and it is insensitive to the applied voltage and current. Switched capacitor reduces the non-linearity issues using the linearization method. The proposed work consists of 4 switches. S_1, S_4 are odd Switch and S_2, S_3 even switches. Figure 11 shows the proposed circuit diagram of series-bilinear switch capacitor based low voltage integrator.

The series-bilinear transformation which is the simple continuous mapping from the S-plane to the Z-plane by the (1).

$$S = 2(1 - Z^{-1})/T(1 + Z^{-1}) \quad (1)$$

In the proposed work X_2 and X_3 are resistors; unswitched capacitors X_5, X_4, X_1 perform as capacitive elements. During Φ2, capacitors X_2, X_3 are discharged. During Φ1, X_5, X_4, X_1 are charged and not losing the charge during Φ2. The equivalent resistance of the series-bilinear switch capacitor circuit is (2).

$$R = \frac{T}{4C_1 + C_2} \quad (2)$$

Where R is the resistance and C1 and C_2 is the capacitance of the Series-Bilinear switch capacitor circuit. The flip-flops used in the VCO quantizer changes the VCO output at every clock edges. The output frequency of the VCO is sampled and is converted to current and is compared with the input current. The converted current is integrated to the loop filter. The layout of the 12-bit Delta-sigma ADC is shown in Figure 12. The obtained area is 136.7*143.2µm² of which the total area is 19575µm².

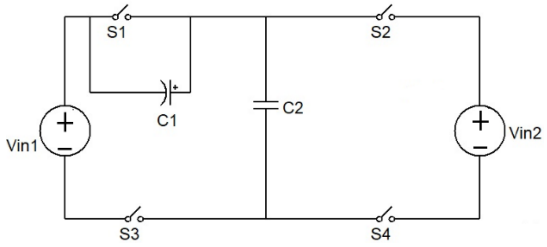

Figure 10. The series-bilinear switch capacitor circuit

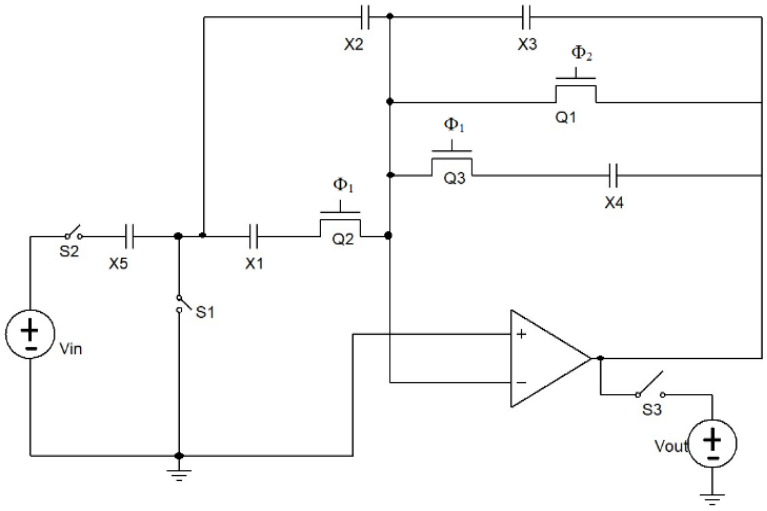

Figure 11. Proposed series-bilinear switch capacitor using low voltage integrator

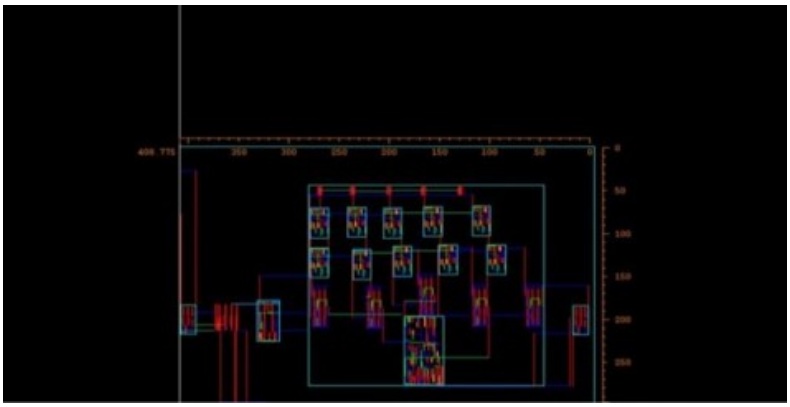

Figure 12. Layout of the proposed 12-bit delta-sigma ADC

4. RESULT AND DISSCUSSION

A conventional delta-sigma analog to digital converter is simulated in a 90nm CMOS process using a cadence tool. The open loop gain of the designed op-amp is 41 dB. A high-speed VCO quantizer is designed using 5-stage Ring oscillator with arrays of DFFs and XOR. The obtained power consumption of VCO

quantizer is 408.7 µW with a sampling frequency of 100 kHz and a V_{p-p} of 1.2 V. The ADC is designed in a 90nm CMOS process and achieves 71.54 dB SFDR, 80.63 SNR, 11.56 ENOB, 2.68 mW power consumption for a 0.6 V_{p-p} differential input signal from a 1.2 V supply voltage. Figure 13 shows that the various specification parameters obtained for 12-bit Delta-sigma ADC. Table 1 shows performance comparision of proposed delta-sigma ADC with prior works [39-44]. The power of 12-bit incremental delta-sigma ADC is reduced up to 65% when compared with conventional ADCs [45-47].

Table 1. Performance comparision of proposed delta-sigma adc with prior works

Parameter	This work	[39]	[40]	[41]	[42]	[43]	[44]
Process Technology(nm)	90	180	180	90	90	90	90
ENOB	11.56	11	13.7	-	-	-	-
Input Frequency	1GHz	150 MHz	350MHz	80MHz	40-240MHz	80-320MHz	
Sampling Frequency	200 MSPS	-	200 MSPS	80	80	90	33.3
Supply Voltage(V)	1.2	3.3	3.3	1	1.2	1.2	1.2
Input Voltage(p-p_{diff})	0.6 V	2.5V	3V	2mV	-	0.8	
SFDR (dB)	71.54dB	87	82	-	-	79-83	
SNR (dB)	80.63dB	84	86	76	68	65.5-77	76.30
Power consumption(mW)	2.68	4.8	16	6.98	5.35	3.43-6.83	6.74

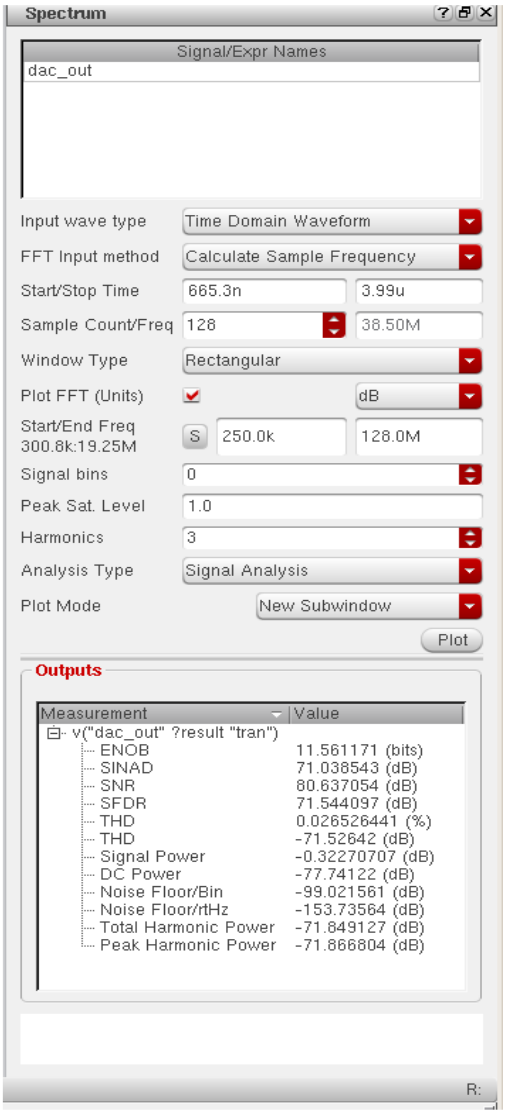

Figure 13. Various specification for 12 -bit delta-sigma ADC

5. CONCLUSION

The proposed Delta-sigma ADC is used for high-resolution gain and stability of the quantizer. The designed op-amp achieves the gain of 41dB and consumes the power of 51.11μW from a 1-V supply. The ADC saves power by sharing a two-stage amplifier to perform signal summation. The loop filter produces the integrated output, which depends on the operational amplifier. The VCO quantizer is used as comparator circuit which quantizes the signal from the filter. The total power consumption of 12- bit ADC is 2.68mW. Simulation result shows that the proposed work 12-bit ΔΣ ADC consumes the power of 2.68mW and the total area occupied is 0.12mm^2. The Post Layout simulation is done for all the blocks and GDS-II file format has been obtained for 12-bit incremental delta-sigma ADC .Based on the other reported ADCs in the literature it is found that the designed 12-bit Delta-sigma ADC with the new proposed VCO has less power consumption and less core area which make it suitable for various applications

ACKNOWLEDGEMENTS

We would like to give sincere thanks to the VLSI Lab of ECE Department, School of Engineering & Technology, Karunya Institute of Technology & Sciences for providing the cadence software tool to complete this work.

REFERENCES

[1] Gray Meye R. G., "MOS operational amplifier design—A tutorial overview," *IEEE J. Solid-State Circuit*, vol. 13, no. 3, pp. 969-982, December 1978.
[2] Min Tan, Qianneng Zhou., "A two-stage amplifier with active miller compensation," *IEEE J. Solid-State Circuits*., vol. 59, no. 6, pp. 201-204, June 2011.
[3] Shedge D. K., et al., "CMOS telescopic cascode operational amplifier," *2013 International Conference on Green Computing, Communication and Conservation of Energy (ICGCE)*, 2013
[4] Chong S., Chan P. K., "Cross feed forward cascode compensation for low-power three-stage amplifier with large capacitive load," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2227-2234, Septemer 2012.
[5] Baker R. J., et al., "CMOS Circuit Design, Layout, and Simulation, Chapter 26," *Piscataway, NJ: IEEE Press*,1998.
[6] Shikata A., et al., "A 0.5 V 1.1MS/sec 6.3 fJ/conversion-step SAR-ADC with tri-level comparator in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 1022-1030, April 2012.
[7] Harpe P., et al., "A 2.2/2.7 fJ/conversion-step 10/12 b 40 kS/s SAR ADC with data-driven noise Reduction," *IEEE Int. Solid-State Circuits*, vol. 48, no. 12, pp. 3011-3018, December 2013.
[8] Liou C. Y., Hsieh C. C., "A 2.4-to-5.2 fJ/conversion-step 10 b 0.5-to-4 MS/s SAR ADC with charge-average switching DAC in 90 nm CMOS," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech.Papers*, pp.280–281, 2013.
[9] Tai, Hu Y. S., Chen H.W. Chen H. S., "A 0.85 fJ/conversion-step 10 b 200 kS/s sub ranging SAR ADC in 40 nm CMOS," *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, pp.196–197, February 2014.
[10] Fiorenza J. K., et al., "Comparator-based switched-capacitor circuits for scaled CMOS technologies," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2658-2668, December 2006.
[11] Lee S., et al., "A 12 b 5-to-50 MS/s 0.5-to-1 V voltage scalable zero-crossing based pipelined ADC," *IEEE Solid-State Circuits*, vol. 47, no. 7, pp. 1603-1614, July 2012.
[12] Murmann B., Boser B. E., "A 12 b 75MS/s pipelined ADC using open-loop residue amplification*," Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 328-497, February 2003.
[13] Hu J., Dolev N., Murmann B., "A 9.4-bit, 50-MS/s, 1.44-mWpipelined ADC using dynamic residue amplification," *2008 IEEE Symposium on VLSI Circuit*, June 2008.
[14] W. Hegong, et al*., "*A 0.024 mm 8 b 400 MS/s SAR ADC with 2/b cycle and resistive DAC in 65 nm CMOS," *2011 IEEE International Solid-State Circuit Conference*, February 2011.
[15] Yip M., Chandrakasan A. P, "A resolution-reconfigurable 5-to-10b 0.4-to-1 V power scalable SAR ADC*," 2011 IEEE International Solid-State Circuit Conference*, pp.190–192, February 2011.
[16] Nakajima Y., et al*.,* "A self-background calibrated 6 b 2.7 GS/s ADC with cascade- calibrated folding-interpolating architecture," *IEEE Symp.VLSI Circuits,* pp. 266-267, June 2009.
[17] Verma A, Razavi B, "A 10 b 500 MHz 55 mW CMOS ADC," *Proc. IEEE Int. Solid-State Circuits Conference*, pp.84-85, February 2009.
[18] Kim J., Cho S. H, "A time-based analog-to-digital converter using a multi-phase voltage-controlled oscillator," *Proc. IEEE Int. Symp. Circuits Syst,* pp. 3934-3937, 2006.
[19] Yoon Y., et al., "A time-based band pass ADC using time-interleaved voltage-controlled oscillators," *IEEE Trans. Circuits Systems. I,* vol. 55, no. 11, pp. 3571-3581, December 2008.
[20] Kim J., et al., "Analysis and design of voltage-controlled oscillator based analog-to-Digital converter," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 1, pp. 18-30, January 2010.
[21] Daniels J., et al., "A 0.02 mm 65 nm CMOS 30 MHz BW all-digital differential VCO-based ADC," *2010 Symposium on VLSI Circuits*, pp. 155–156, June 2010.
[22] Taylor G., Galton I., "A mostly-digital variable-rate continuous time Delta-Sigma modulator ADC," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2634-2646, December 2010.
[23] Cao Y., et al*.,* "A 1.7 mW 11 b 1-1-1 MASH time-to-Digital converter," *IEEE International. Solid-State Circuits Conferenc*e, pp. 480-482, February 2011.

[24] Konishi T., et al., "A 40-nm 640 m 45-dB op-ampless all-digital second -order MASH ΔΣ ADC," *IEEE Int. Symp. Circuits Syst.,* pp. 518-521, 2011.
[25] Li Huang, et al., "A new algorithm for an incremental sigma-delta converter reconstruction filter," *32nd Symposium on Integrated Circuits and Systems Design* (*SBCCI*), August 2019.
[26] Adi Xhakoni, *et al*., "PTC-based sigma-delta ADCs for high-speed, low-noise imagers", *IEEE Sensors Journal*, vol. 14, no. 9, pp. 2932-2933, September 2014.
[27] Pere Llimos Muntal, et al., "34.3 fJ/conv.-step 8-MHz bandwidth fourth-order pseudo-differential ring-amplifier-based continuous-time delta–sigma ADC in 65 nm", *IEEE Solid-State Circuits Letters*, vol. 1, no. 10, pp. 198-201, 2018.
[28] Johannes Wagner, et al., "On the signal filtering property of CT incremental sigma–delta ADCs," *IEEE Transactions on Circuits and Systems II*: Express *Briefs*, vol. 66, no. 11, pp. 1780-1784, 2019.
[29] Mohamed A. Mokhtar, et al., "A 94.3-dB SFDR, 91.5-dB DR, and 200-kS/s CT incremental delta–sigma modulator with differentially reset FIR feedback," *IEEE Solid-State Circuits Letters*, vol.2, no. 9, pp. 87-90, 2019.
[30] Shylu D. S., Jackuline Moni D, "Design of low power dynamic comparator with reduced kick back noise using clocked PMOS technique," *Journal of Electrical Engineering* (JEE), vol.16, no. 3, pp.1-10, January 2016.
[31] Shylu D. S., et al., "Design and power optimization of high-speed pipelined ADC with programmable gain amplifier for wireless receiver applications," *Wireless Personal Communication*, vol. 90, no. 2, pp. 657-678, January 2016.
[32] Shylu D. S., Jackuline Moni D, "A 1.8V 22mW 10 bit 165 MSPS Pipelined ADC for video applications," *WSEAS Transactions on Circuits and systems*, vol.13, pp. 343-355, January 2014.
[33] Gray P. R., et al., "Analysis and design of analog integrated circuits," Forth Edition. *John Wiley* &Sons, Inc, 2001.
[34] Anchal Verma, et al., "Design of two-stage CMOS operational amplifier," *International Journal of Emerging Technology and Advanced Engineering*, vol. 3, no. 12, pp.102-106, 2018.
[35] Leslie T. C., Singh B., "Improved sigma-delta modulator architecture," *IEEE Int. Symp. Circuits and Systems (ISCAS),* vol. 1, pp. 372-375, May1990.
[36] Zhaohui Huang, et al., "An adaptive analog-to-digital converter based on low-power dynamic latch comparator," *IEEE International conference*, May 2005.
[37] McCarroll, et al., "A high-speed CMOS comparator for use in an ADC," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 1, pp. 159-165, February 1988.
[38] Carlos J Solis, et al., "High resolution low power 0.6μm CMOS 40MHz dynamic latch comparator," *53rd IEEE International Midwest Symposium on Circuits and Systems*, pp.1045-1048, Aug. 2010.
[39] Baschirotto A., et al., "A 15 MHz 20 mW BICMOS sppwitched-capacitor biquad operating with 150 Ms/s sampling frequency," *IEEE J. of Solid-State Circuits*, vol. 30, pp.1357-1365, 1995.
[40] Hosticka B. J., et al., "MOS sampled data recursive transistors using switched-capacitor integrators," *IEEE Journal Solid-State Circuits*, vol. 12, no. 6, pp. 600-608, January1978.
[41] Harish Balasubramaniam, Klaus Hofmann, "Calibrated switched capacitor integrators based on current conveyors and its application to delta sigma ADC," *10th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, pp.1-4, July 2014.
[42] Morgado, et al., "A 100kHz–10MHz BW, 78-to-52dB DR, 4.6-to-11mW flexible SC ΣΔ modulator in 1.2-V 90-nm CMOS," *Proceedings of the ESSCIRC*, pp.418-421, September 2010.
[43] L. Bos, et al., "Multirate cascaded discrete-time low-pass ΔΣ modulator for GSM/bluetooth/UMTS," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1198-1208, June 2010.
[44] Chunhui Pan, Hao San, "A 6th-order complex bandpass ΔΣAD modulator using dynamic amplifier and noise coupling SAR quantizer," *International Symposium on Intelligent Signal Processing and Communication Systems* (ISPACS), November 2018.
[45] Wonsik Yu, et al., "A Time-Domain High-Order MASH ΔΣ ADC Using Voltage-Controlled Gated-Ring Oscillator," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol.60, no. 4, pp. 856-866, April 2013.
[46] Xing, et al., "Design of power- efficient highly digital analog-to-digital converters for next-generation wireless communication systems," *Signals and Communication Technology*, Springer, 2018.
[47] Johannes Wagner, et al., "On the signal filtering property of CT incremental sigma-delta ADCs". *IEEE Transactions on Circuits and Systems II: Express Briefs(Early Access),* vol. 66, no. 11, pp. 1780-1784, January 2019.

BIOGRAPHIES OF AUTHORS

D. S. Shylu is working as an Associate Professor in ECE Department, Karunya Karunya Institute of Technology & Sciences. She received her BE degree from M.S. University, Tirunelveli and M. Tech in VLSI Design from SASTRA University, Thanjavore. She obtained her Ph.D. degree in ECE Department at Karunya Deemed University. She has 16 years of teaching experience. She has published more than 50 papers in National and International Journals and conferences. Her areas of interest are Analog VLSI Design, Device modeling, Low Power VLSI Design.

P. Sam Paul received his Bachelor degree in Mechanical Engineering in 1999 from Manonmonium Sundaranar University and Master degree in CAD in 2001 from Madras University, India. He obtained his Ph.D. degree in Mechanical Engineering at Karunya Deemed University. At present he is working as a Professor in Department of Mechanical Engineering in Karunya Deemed University. His research interests include Vibration and Finite element analysis. He has published papers in many refereed international journals and conferences for his highest level of achievement.

D. Jackuline Moni working as a Professor in ECE Department, Karunya University. She did her B. Tech in Electronics Engineering at Madras Institute of Technology, Anna University, M.E in (Applied Electronics) from Government College of Technology, Coimbatore, and her Ph. D in (VLSI Design) from Anna University, Chennai. She has over 30 years of teaching experience. She has presented and published more than 90 papers in National and International Journals and conferences. Her areas of interest are CAD VLSI Design, Device modeling, Low Power VLSI Design, analog VLSI Design.

J. Arolin Monica Helan completed Bachelors in Electronics Engineering from Karpagam Institute of Technology, Coimbatore. She completed M. Tech in VLSI Design from Karunya Institute of Technology and Sciences. Her area of interest is CMOS VLSI Design, Analog VLSI Design and Testing and Testability.