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Fabrication of a Few-Layer Graphene Electrodes for Molecular Electronics Devices

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We report on the fabrication of a molecular transistor based on a single molecule trapped in a few-layer graphene nanogap. The device is pre-patterned with He-ion beam milling or oxygen plasma etching prior to nanogap formation. Pre-patterning helps to localize the gap, and to make it narrower, so that only a few or a single molecule can be trapped in it. The nanogap is formed by an electroburning technique at room temperature. In order to test the functionality of the device we deposited diamino-terphenyl molecules in the nanogap. Three-terminal electrical measurements showed an increase of the current after deposition, and a gate voltage dependence at low temperatures. Hence, pre-patterned few-layer graphene junctions can be used for electron transport measurements through a terphenyl molecule with a future prospective towards more complex molecular configurations.

Keywords: Nanoscale devices, Three-terminal transistors, Graphene electrodes, Electroburning.

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1. INTRODUCTION

One of the open questions in molecular electronics is how to measure electron transport through a single molecule at ambient conditions. In order to do so, devices should possess certain requirements. First, the spacing between source and drain electrodes must be small enough to place a single molecule, which is typically of the order of a few nm.

Up to now, several techniques such as mechanically controlled breakjunctions [1], nanolithography [2], electromigration [3] and others [4], [5] have been used to obtain nanoscale spacing between electrodes. A second important requirement is device stability at room temperature. Gold is the most common material for electrodes because of its noble character, but Au electrodes show instability at room temperature because of the high atomic mobility [6]. For this reason, most of the single-molecule measurements with gold electrodes are performed at cryogenic temperatures. Nevertheless operation at ambient temperature is crucial for future applications [7]. Graphene, a two-dimensional honeycomb lattice of carbon atoms shows exceptional electronic, mechanical and thermal properties that can be exploited for molecular electronics. Atomically thin graphene, or a few-layer graphene to avoid gating of the electrodes [8], can increase the gate coupling in molecular transistors, compared with bulky Au electrodes. Covalent binding of the carbon atoms in the lattice minimizes atomic mobility at room temperature resulting in stable electrode geometries. Also graphene enables a variety of anchoring groups that can be used for molecule attachment [9]. All these make few-layer graphene (FLG) a promising material for room temperature molecular devices.

In this proceeding we show the fabrication approach for molecular three-terminal transistors using FLG flakes as electrodes, its electrical characterization before and after molecule deposition, and the detection of molecular transport.

2. DEVICE FABRICATION

2.1 Nanofabrication

The three-terminal transistors are fabricated on a heavily doped Si substrate coated with 285-nm thick SiO_2. The Si substrate is used as a common back-gate electrode. The surface is cleaned with ozone in order to minimize contamination and to maximize the adhesion of the flakes to the surface. FLG flakes are transferred onto the clean substrate by mechanical exfoliation using nitto tape. Suitable flakes [8] are selected by optical contrast under the microscope or by an AFM scanning. Two gold leads contact the graphene flake, as shown in the Figure 1, and are used for biasing the device.

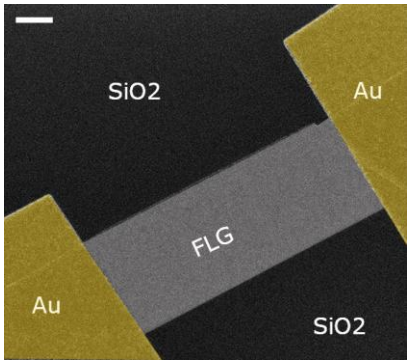

Fig. 1 – Scanning electron microscope (SEM) colored top view of the device after fabrication. The FLG flake is located between two Au electrodes on insulating SiO_2. Scale bar 500 nm.

The next step is to open the gap in FLG flake by using the electroburning technique [see 8 for more information] that allows to create a gap of a few nm. During electroburning the gap appears along the whole width of the flake, as seen in Fig. 2, which is about 3 μm wide. The probability of having several molecules in the gap increases because of the micrometre width of the flake. Moreover, the gap may appear close to one of

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the gold electrodes resulting in the partial shielding of the gate voltage.

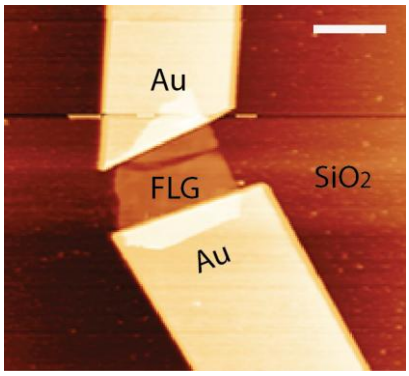

Fig. 2 – Atomic force microscopy (AFM) image of a device after electroburning. The gap appears along the whole flake in close proximity to the top electrode, which may result in shielding of the gate field. Scale bar 2.5 µm.

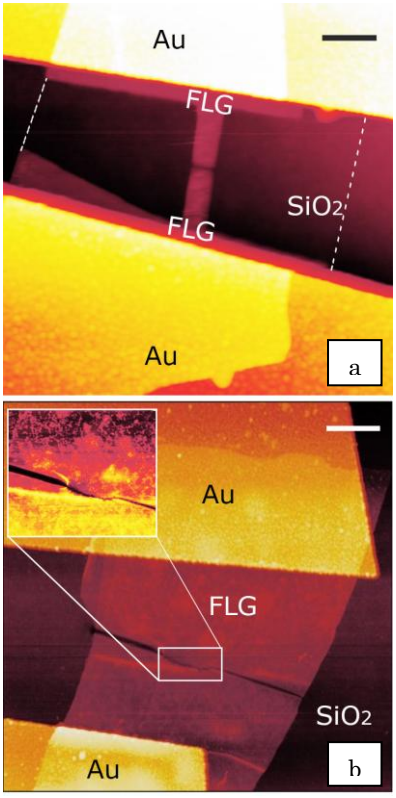

Fig. 3 – AFM image of a device pre-patterned with (a) a combination of EBL and OP RIE. Dashed white lines indicate the flake size before etching. Scale bar 500 nm. (b) He-ion beam. After electroburning of the pre-patterned device the nanogap appeared in the middle of the bridge, as shown in the inset. Scale bar 100 nm.

In order to overcome this issue a pre-patterning fabrication step is added prior to electroburning. The goal is to fabricate narrow FLG bridges. Two different approaches: 1) Electron-beam lithography (EBL) in combination with oxygen plasma etching (OP RIE), 2) He-ion beam (HIM) milling. Briefly, for the EBL approach the chip is covered with a positive resist (PMMA) and exposed to the electron beam in such a way that the mask pattern for the etching is defined. Afterwards the resist is developed in MIBK:IPA (1:3) for 90 seconds and rinsed with IPA. Next, 1 min of the oxygen plasma etching is employed with a RF power of 20 W, a gas flow of 25 sccm O_2 and a pressure in the chamber of 50 µbar. In this step, the parts of the flakes that were not shielded by the resist are removed. The result is shown in the AFM image in Fig.3(a). Using this technique many devices can be processed simultaneously.

As an alternative to oxygen plasma etching, a He-ion beam microscope can be used. It is an universal nanofabrication tool that besides various applications [10,11,12] can perform ion-beam milling with nanometer resolution. The device is placed into the loading chamber of a Zeiss Orion HIM. The acceleration voltage for imaging is set to 25 kV in order to prevent charging effects on the surface of the chip. An internal pattern generator is used for pre-patterning, while the acceleration voltage in this case increases to 30 kV, enabling a beam current of 1 pA at a dose of 120 nC/cm. The patterned trenches, of about 10 nm wide, are narrower than with plasma etching, resulting in shorter bridges. For imaging after pre-patterning the acceleration voltage is reduced. A complete device is shown in Fig. 3(b).

2.2 Feedback-controlled electroburning

After pre-patterning, feedback-controlled electroburning is used to create a nanoscale gap in the FLG flake. Electroburning is performed by ramping a high bias voltage (5 – 9 V) across flakes with initial resistances of kOhms and ohmic behavior in the current-voltage characteristics. At high current densities the flake heats up by the Joule effect and carbon atoms become mobile at the hottest areas in the pre-patterned channel. Feedback controlled software keeps track on the conductance of the device, and once it drops by 10%, the voltage is ramped back to the starting point (0.2 V), to prevent the uncontrollable breaking of the flake under high voltages. After ramping back, a new voltage sweep starts and the process is repeated until the device reaches a resistance in the range of GOhms, which indicates that a nanogap has been formed. Figure 3 shows AFM images of electroburned devices that were pre-patterned with the two fabrication approaches mentioned above. The gap is opened in the center of the bridge, thus realizing control over the localization of the nanogap formation.

Figure 4 presents the current while sweeping the bias voltage of a device after electroburning. The shape of this current-voltage characteristics resembles the one expected for single-barrier tunneling. The width of the gap can be estimated from a Simmons model (red dashed line in Fig. 4). From the fit, with an area A = 1100 nm^2 (width of the FLG bridge W = 100 nm, length L = 11 nm) we extract a barrier height φ = 0.6 eV and a gap size d = 2.2 nm. The inset in Figure 4 shows the current as a function of the applied back-gate voltage at V_b = 0.3 V at room temperature. The absence of gate-dependent transport indicates that the gap is empty before molecular deposition. This observation combined with the small size of the gap makes the device suitable for molecular deposition and as a three-terminal molecular transistor.

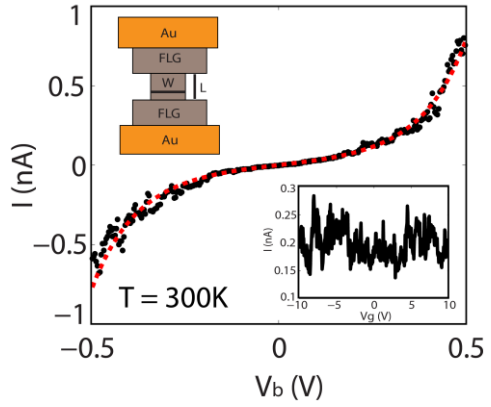

Fig. 4 – Current-voltage characteristic of a pre-patterned device after electroburning. Bias voltage sweep V_b = ± 0.5 V shows tunneling curve (black dots). The Simmons fit (dashed red line) is plotted on top along with the tunneling curve. Bottom inset: Current vs gate voltage taken at V_b = 0.3 V; top inset: schematics of the device.

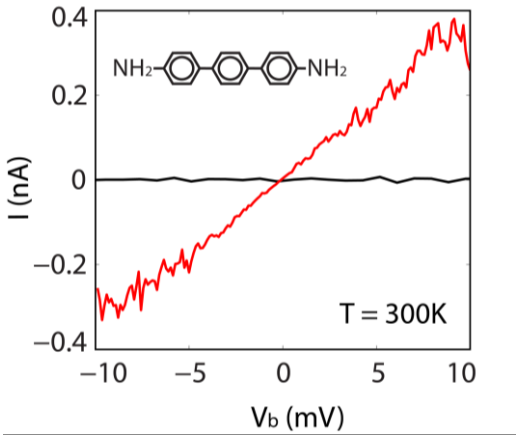

Fig. 5 – Current-voltage characteristic at room temperature of a FLG gap before (black line) and after (red line) molecule deposition.

3. MOLECULE DEPOSITION

To test the functionality of the fabricated devices we have performed deposition of diamino-terphenyl molecules on the electroburned FLG junctions. 1-Ethyl-3-(3-dimethylaminopropyl) carbodiimide (EDAC) has been used as a catalyst to form a covalent bonds between the NH_2 anchoring groups of the molecule and the carboxylic groups present at the edges of the gap. The chip with electroburned junctions was put in pyridine solution that contains a 1 mMol of terphenyl and 2 mMol of EDAC, and kept in this solution for 15 hours to let the molecules assemble on the surface and form the covalent N-C bonds in a chemical reaction. After taking the chip out from the solution it is dried naturally. At room temperature I-V measurements were performed. As Fig. 5 shows, the current increases dramatically (red line) when compared to the current level before deposition (black line).

To characterize gate-dependent transport measurements were performed at 4 K. The gate sweep shown in Fig. 6 taken at V_b = 0.2 V displays that the current is dependent on the gate voltage after the molecule deposition.

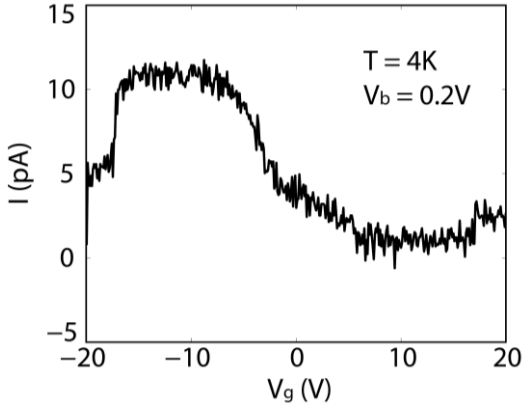

Fig. 6 – Current as a function of the applied gate after the deposition of 1mMol of terphenyl molecules. Measurements taken on a sample that is different from the one shown in Fig.5.

To conclude, we have studied the fabrication of nanogaps in pre-patterned FLG bridges using the electroburning technique. The pre-patterning of the flake enables localization of the gap, and reduces its length. To test the functionality of our device diamo-terphenyl molecule has been deposited to the gap. The I-Vs after molecule deposition show an increase of the current level and gate dependence. These devices can be used to perform measurements on more complex molecules, or can be viewed as a first step towards more complicated molecular circuits involving more than one junction.

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