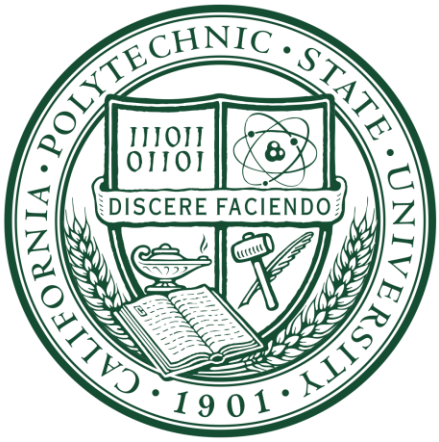

Electrical Engineering Department

California Polytechnic State University

Senior Project Final Report

Solar Panel with Embedded Electronics

June 10, 2020

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Abstract

Currently, inverters are needed to utilize solar panels for applications that require AC power. Unfortunately, these inverters are very costly and decrease power efficiency. In this work, two alternatives to using inverters are explored. The first method combines a buck converter with a buck-boost converter to create a sine output. The second method uses switches to change the connections of the solar cells, producing a stepped AC output. Both methods involve embedding the solar cells along with the additional electronics into a solar panel, thus eliminating the need for a separate inverter. Simulations were performed using SIMPLIS, and both methods were compared with a focus on feasibility and cost. Results of the simulation demonstrated that the DC-DC converter method performs better than the multiple switch method. More specifically, the quality of the sinusoidal output voltage from the DC-DC converter method is better than the stepped sine wave produced by the multiple switches. Furthermore, the use of many switches to produce a sine wave like output makes the multiple switch method not practical due to the complexity of circuit as well as cost. Therefore, through these comparisons, we recommend that future projects should focus on implementing prototypes for the DC-DC converter method using buck buck-boost converter.

Chapter 1. Introduction

Renewable energy is the fastest growing source of electricity and is projected to account for 38% of electrical generation in the United States by 2050 [1]. These projections come from the U.S. Energy Information Administration, which also predicts solar energy to constitute the largest source of renewables. Solar is expected to grow from 15% in 2020 to 46% in 2050 which is good especially considering the depleting oil and gas reserves. As solar energy for electricity is becoming more prevalent, we face new challenges in developing technologies that will make the use of solar panels more reliable, efficient, and economical.

Currently all commercially available solar panels produce direct current (DC) voltages at various voltage and power levels. However, nearly every home and industrial applications require alternating current (AC) voltages to power their appliances and other electrical devices. Thus when used for these applications, the solar panel or photovoltaic (PV) systems will require a device that must be capable of converting the DC voltage from the solar panels to an AC output voltage to match and meet load requirements.

Through the application of power electronics, a device known as the inverter makes it possible to convert a DC input voltage into an AC output voltage. Provided the inverter is designed well, it is also capable of performing the energy conversion efficiently by minimizing the power loss in the conversion process. There are several types of inverters for various applications; thus, it is imperative to choose the most suitable inverter technology based on the application. Two common commercially available inverters for PV systems are the string inverters and microinverters.

String inverters are the most widely adopted method for energy conversion in PV systems. The main requirement of this type of inverter is that it requires solar panels be strung in

series to provide the proper input voltage to the inverter. The main drawback of this method relates to the reduced performance in one panel, for example due to shading. When a panel is covered by a tree for instance, the performance of the remaining solar panels in the same string will be degraded to the lowest performing panel. However, an advantage of string inverters is the overall system cost because only one centralized inverter is required for the PV system. In contrast, microinverters face a higher cost because each panel has their own smaller inverter. The advantage of doing this is that it prevents the performance of one panel to significantly affect the overall system performance [2]. Furthermore, the use a local more distributed smaller inverter yields a much more robust and reliable PV system.

The two methods described above require at minimum two stages of power conversion. The first stage is a DC-DC converter which either steps up or steps down the output of the solar panel while the second stage inverts the DC voltage to a single-phase AC voltage [3]. While the two-stage approach is well understood and implemented in practice, it possesses several drawbacks such as complexity, size, weight, and cost of the overall converter system. It will therefore be useful and interesting to look into other ways of producing the AC voltage from the DC voltage. One such method involves directly converting the DC voltage into AC voltage; thus, allowing the use of only one stage in the conversion process.

Chapter 2. Background

Solar panels currently are only capable of producing DC voltage output; and thus, for a PV system to be viable for household and most industrial applications, the output must be inverted into an AC voltage. Unfortunately, the cost of a conventional inverter for a solar panel system is not negligible but is instead rather costly [4]. String inverters are cheaper than microinverters; however, they tend to have a lower life expectancy due to having to deal with higher power than microinverters. Furthermore, the efficiency of a system with string inverters is strongly influenced by its weakest link (or the least-efficient solar panel). Since string inverters require the solar panels to be connected in series, one underperforming solar panel negatively affects the rest. So, if one panel experiences more shading than other panels for whatever reason, all of the other panels would produce an output as if they were also shaded.

On the other hand, microinverters seem to be a direct upgrade over string inverters in terms of energy production for the system. Since each microinverter is connected to one solar panel, it allows the solar panels to be connected in parallel to the load. This means that each inverter is dealing with a smaller amount of power and heat, increasing its lifespan. Most string inverters have a warranty of 10-12 years while microinverters have warranties as long as 25 years, which is around the same for a solar panel. Additionally, the parallel connection means that the system as a whole is not as heavily affected by a single underperforming panel. However, current microinverters do face some disadvantages. They are significantly more expensive than string inverters, and they are more difficult to perform maintenance on. String inverters can be installed in a separate area from the solar panels, whereas microinverters are installed directly underneath the solar panels, which in turn are usually installed on rooftops [5].

Irrespective of whether these inverters are used in a string inverter or micro inverter configuration, there are a few different topologies to consider. The three considered here are the two-stage, multilevel inverters, and single-stage.

The popular choice for an inverter in a PV system is a two-stage topology: the first stage boosts the PV voltage and the second stage inverters the input and generates the AC sinusoidal output waveform. The topology is well understood and is shown in Figure 2.1.

The drawbacks to such a topology are high cost and a requirement for each stage to have high efficiency so that the overall system efficiency is high [8]. For example, if the DC-DC boost stage has an efficiency of 90% and the inverter also has an efficiency of 90%, the overall efficiency would be 90% * 90% = 81%.

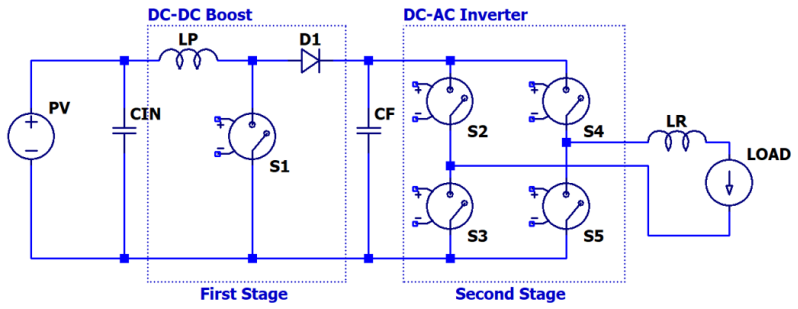

Figure 2-1: Two Stage DC-AC Inverter

Multilevel inverter is another topology explored to see whether it could reduce cost or complexity. Multilevel inverters provide an output waveform composed of several voltage steps that ideally would look like a discrete form of a sinusoidal wave. Multilevel topologies and their design considerations are discussed in [6-7]. The total harmonic distortion on a multilevel inverter can be reduced by increasing the number of output voltage steps; however, the trade-off is an increase in switches and increased complexity in switch gate driving.

A single-stage DC-AC topology would normally be thought of as an inverter with no boost or bucking capability. Solar cells are low voltage produced cells and the conventional way

of increasing the output voltage is by connecting the cells in series. Unfortunately, connecting more solar cells in series has diminishing returns due to variation in operating conditions between each cell. It then becomes necessary to boost the output voltage of the series connected solar cells.

The single-stage topology presented in [8, 9] is based on a full-bridge DC-AC inverter that includes two additional diodes and one input inductor to implement two boost converters. The topology reduces the number of switches by having the boost and inverter functionalities share the power transistors. A reduction in the number of switches assists in minimizing switching losses and reduces the switching control complexity. Furthermore, it is possible to control the AC output voltage and frequency in this topology.

The project will focus on simulating and comparing the multilevel and single-stage topologies. The intention is that the findings in this work may provide a good base for future projects of solar panels with embedded electronics.

Chapter 3. Design Requirements

This chapter details the design requirements necessary for the project regarding electrical performance and mechanical considerations.

Technical Requirements

- **Input Voltage Range**

  The input source will comprise a combination of series and parallel solar cells whose open voltage must be rated for at least 5V and short circuit current of at least 100 mA. Solar cells produce varying output voltage based on the type of materials used, and operating conditions such as temperature and shading. The IXOLARTM SolarBit, a typical surface mounted solar cell, produces 1.67V at its maximum power point as an example [10].

- **Fixed AC Output**

  The output voltage shall be a nominal of 10VAC peak running at 60Hz. The output current shall be 100mA at full load.

- **Power Efficiency**

  The efficiency of the solar cells will be dependent on the manufacturers. However, the efficiency of the embedded electronics should be above 90%. This should be achievable as the conversion is performed in a single stage instead of two stages. Physical constraints and component physical sizing must be considered.

- **Use of Existing Controller**

  The controller used for this product should be already commercially available, instead of designing a new controller. Using an existing controller reduces the complexity of the overall project. It also improves the scalability of this product, since it is easier to implement an already existing controller than implementing the individual components required in a new controller. Thus, this will ease production of numerous products.

- **Board Layout**

  The converter shall be designed onto a printed circuit board. The number of layers of the PCB should be minimized to reduce production complexity and cost. Components shall be surface mounts, whenever possible. This will create a low-profile board design capable of being closely integrated to the solar cells.

- **Compact Board Dimensions**

  The printed circuit board shall fit within the size of solar cells used. For the project to be viable as an embedded alternative, the PCB must not be larger than an individual solar cell.

Block Diagrams

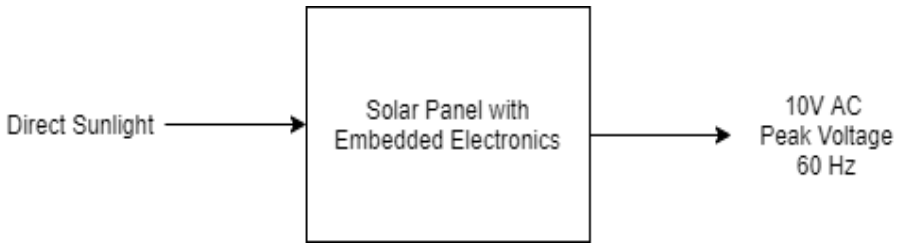

Figure 3-1: Level 0 Block Diagram

The level 0 block diagram shows that the system consists of a single input and a single output. The single input is considered to be direct sunlight. The single output is a 10VAC peak voltage operating at 60Hz with 100mA output current at full load.

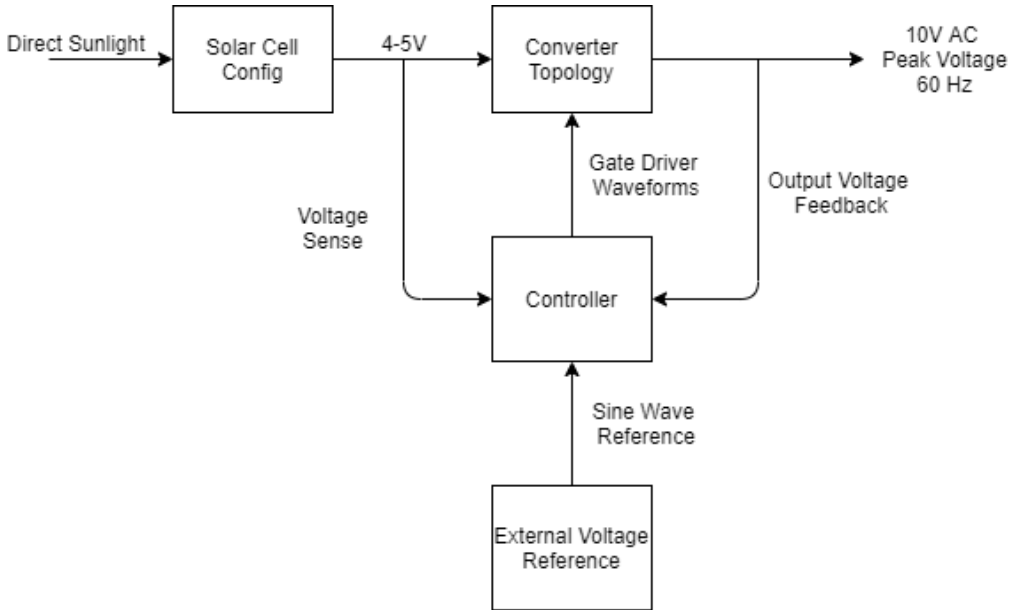

Figure 3-2: Level 1 Block Diagram

The level 1 block diagram shows the connection of the embedded electronics in more detail. The controller utilizes a feedback signal to achieve the desired voltage. The controller should have a sinusoidal or a rectified sinusoidal voltage reference, instead of the typical DC reference, to produce a sinusoidal output voltage waveform. Table 3-1 summarizes the design requirements for the project.

Table 3.1: Requirements List

Requirement	**Value**
Input Voltage Range	4-5V
Output Voltage	10V peak AC at 60 Hz
Input Power	0.5W
Full Load Current	100mA
Converter Efficiency	>90%
Board Dimensions	Within the size of the solar cells
Board Layout	Minimal

Chapter 4. Design Requirements

Figure 4-1 shows the Level 2 Block Diagram for the proposed DC converter method. The following pages will explain the purpose and functionality of each block in Figure 4-1. However, the gate drivers and references will be discussed here.

The gate drivers will provide the necessary gate voltage to drive the main switch and four other switches that reconfigure the power stage between two different topologies: Buck and Buck-Boost. Originally the gate drivers were going to implement bootstrapping capacitors but for the purposes of simulation tests, voltage sources will be used to clearly define the high and low side of the gate drivers

The sinusoidal reference will be -5 to 5 volts. Preliminary tests and simulations have shown that for the positive half cycle of the reference sine, the Buck will follow the reference. Buck-Boost can be shown to work for the negative half cycle, but further design and simulation is required. The sawtooth reference, fed into the pulse width modulator, will set the switching frequency. The switching frequency selected was 200kHz. This is a typical switching frequency and is below the gain bandwidth product of 1MHz of most generic operational amplifiers. Since this design is a proof of concept, no large switching frequencies were considered to reduce the complexity of the control part of the converter.

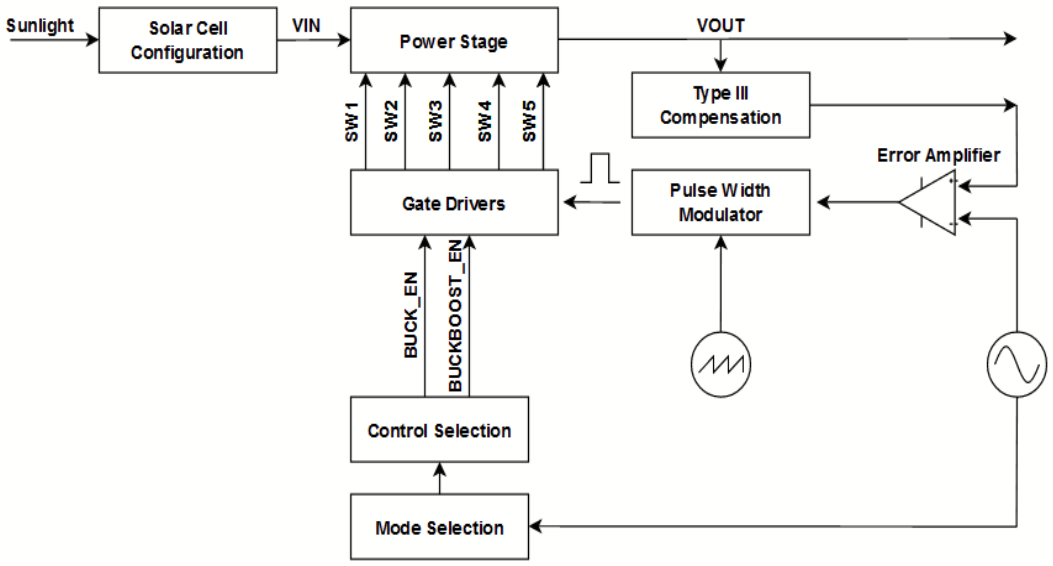

Figure 4-1: Level 2 Block Diagram for DC Converter Method

Power Stage

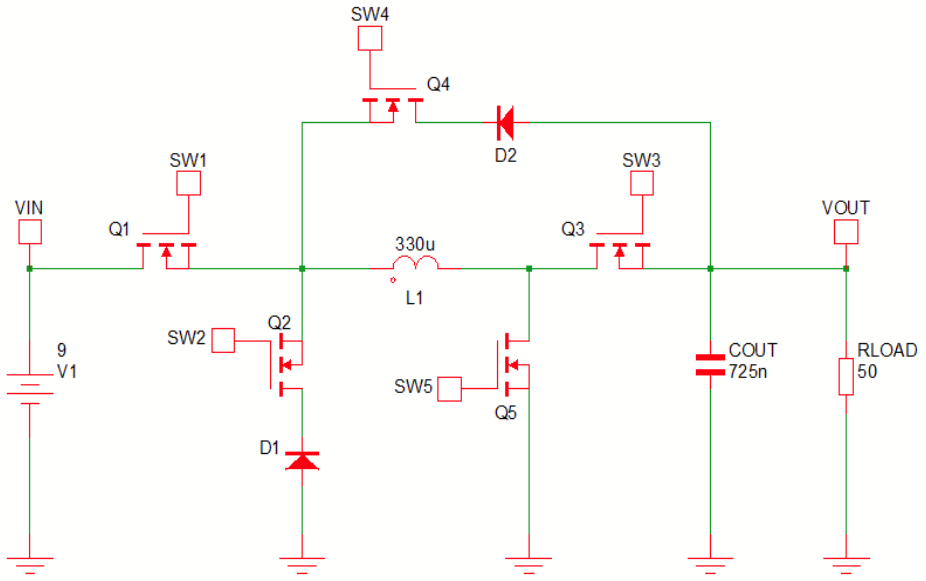

Figure 4-2: Combined Buck and Buck-Boost Topology.

Figure 4-1 depicts the proposed power stage topology which will implement a buck and buck-boost converter. From power electronics theory, a Buck converter can provide a positive output voltage that is proportional to the input voltage by duty cycle *D*. The Buck converter is one of the most understood topologies, and there exist several documents in the design of the converter. Essentially, the Buck converter portion provides the positive half cycle of our output voltage. To obtain a negative half cycle, the Buck-Boost topology was chosen as it inherently provides negative output voltage.

For the system to function as desired, it must be capable of switching between two different topology configurations. Fortunately, the Buck and Buck Boost topology have a commonality, the location of their main switch. The main switch is located at the front of both topologies. This is another reason that a Boost and Buck-Boost configuration would not work without very complex circuitry. For instance, the Boost and Buck-Boost topology share the position of the diode but not the direction of the diode. Even if this were overcome, different main switch positions would require two separate controllers as the "main" switch would be alternating.

To enter Buck mode, switches Q2 and Q3 must be closed while Q3 and Q4 must be opened. Similarly, to enter Buck-Boost mode, switches Q3 and Q4 must be closed while Q2 and Q3 must be opened. Q1 will always serve as the main switch and it will be receiving the modulated PWM signal from the control loop. From the topology one can observe that only one inductor and one output capacitor is used. Thus, the design must take these into account and selection must be performed around the worst-case values.

Type III Compensator

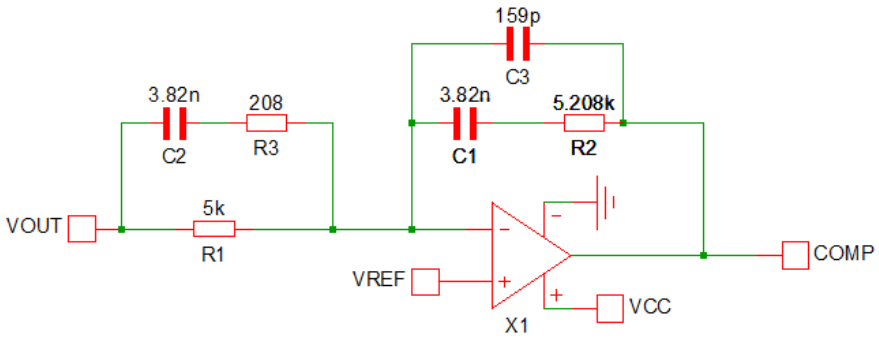

Figure 4-3: Type III Compensator

The purpose of the Type III compensator as shown in Figure 4-3 is to provide stability and control to the power stage. A Type III compensator was chosen due to its ability to provide a maximum phase boost of 180 degrees, if necessary. As shown in the following pages in the calculations section, a Type III compensator is necessary at the very least for the Buck converter portion. Provided that the phase margin is constrained to roughly larger than 60°, the system should be stable.

The selected switching frequency for the system is 200kHz. For the purposes of designing a compensator, one must select a crossover frequency, this is typically selected a decade lower than the switching frequency or 1/5 the switching frequency. The crossover frequency chosen was 40kHz. To design the compensator, one must observe the gain and phase of the open-loop response at the desired crossover frequency. The goal of the compensator is to set the gain at the crossover frequency close to zero dB and allow sufficient phase margin of the closed-loop system. Figure 4-4 shows a sample transfer function plot of a type III compensator. The figure originates from Texas Instruments' Application Report "Demystifying Type II and Type III Compensators Using Op-Amp and OTA for DC/DC Converter".

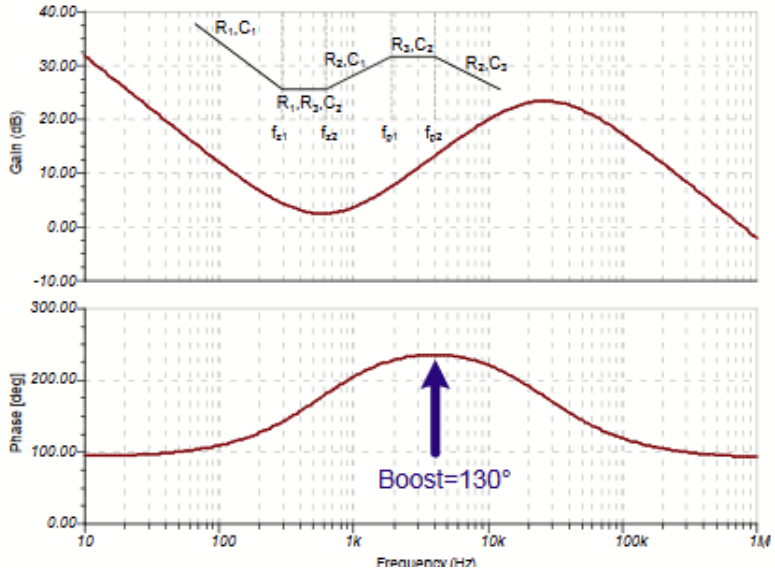

Figure 4-4: Compensator Gain and Phase Plots

As shown above, the compensator introduces two zeros and three poles (one pole approximately at the origin). Selection of these frequencies will ultimately affect the shape and location of both the gain and phase plots. For example, the phase boost of a Type III compensator can be increased by increasing the separation of the poles and zeros, but this will reduce the gain of the system. Further discussion regarding the design of the compensator will be introduced in the calculations section of this chapter.

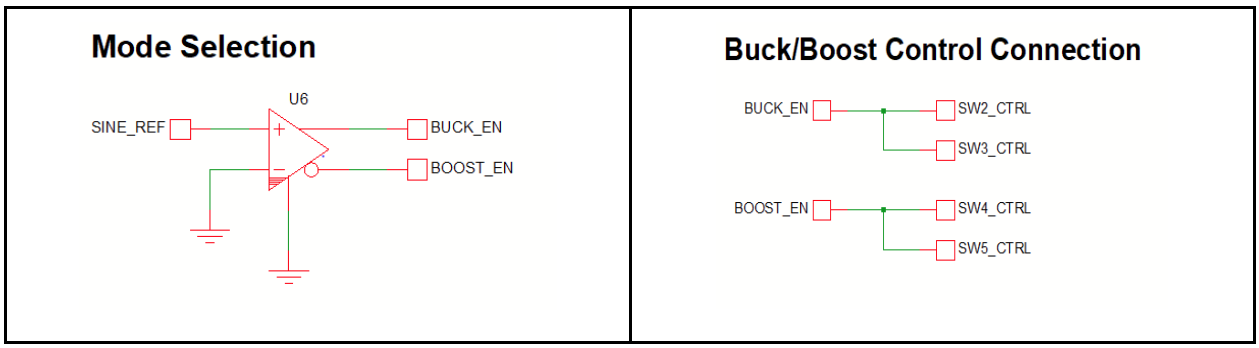

Figure 4-5: Mode Selection and Control Connections

The mode selection and the control connect (labeled control selection in the Level 2 block diagram) provide a method for the system to transition between Buck and Buck-Boost mode. The op-amp configured as comparator will accept a sinusoidal reference with a zero offset. Every time the sinusoidal reference crosses zero volts, the op-amp comparator will either set the Buck enable signal or the Buck-Boost enable signal. These signals will ultimately control a pair of switches in the power stage that will transition the system between buck and buck-boost mode.

Error Voltage Polarity

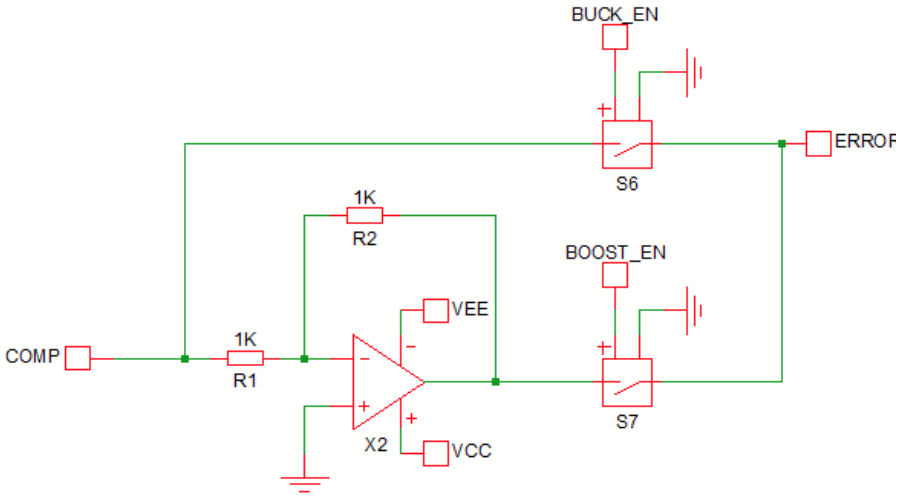

Figure 4-6: Error Voltage Polarity

The Error Voltage polarity circuit adjusts the polarity of the compensated error voltage from the control loop. The polarity of the error voltage is adjusted such that during the Buck mode, the error voltage is positive and during the Buck-Boost mode, the error voltage is negative.

Modulator

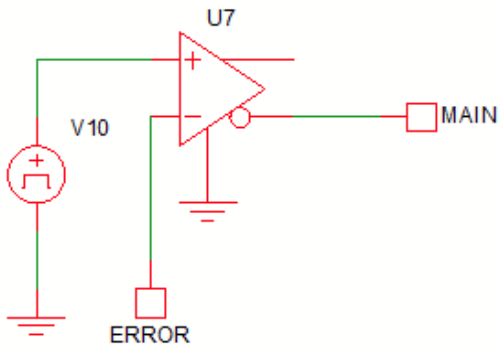

Figure 4-7: Modulator

The modulator is effectively a comparator. The comparator in the schematic provides a logic level non-inverting and inverting output, however the only inverting output is used per the recommended SIMPLIS guidelines. The output is delivered to the main switch to control the duty cycle of the main switch.

Calculations

The following pages discuss calculations involved with selecting the main component ratings in the power stage as well as the passive components used to create the Type III compensator. The first calculations performed are the power stages for both the Buck and Buck-Boost comparator. Their open-loop transfer functions will determine the design of the Type III compensator.

Buck Converter - Power Stage - Main Component Ratings

Parameters:

$V_{IN} := 9\ V$ $V_O := 5\ V$ $I_{OMAX} := 0.1\ A$ $f := 200\ kHz$

$I_{OCCM} := 20\% \cdot I_{OMAX}$ $\Delta V_O := 5\% \cdot V_O$ $V_{RIP} := 0.05$

Solution:

$$D := \frac{V_O}{V_{IN}} = 0.556$$

Inductor:

$$L_{CRIT} := \frac{(1-D)}{2 \cdot f} \cdot \frac{V_O}{I_{OCCM}} = 277.778\ \mu H$$

$$L_{SAFETY} := L_{CRIT} \cdot 1.3 = 361.111\ \mu H$$

Choose: $L := 330\ \mu H$

$$I_{SAT} := I_{OMAX} + \frac{V_O \cdot (1-D)}{2 \cdot L \cdot f} = 0.117\ A$$

MOSFET:

$$V_{DS} := V_{IN} = 9\ V$$

$$I_D := D \cdot I_{OMAX} = 0.056\ A$$

Diode:

$$V_{RRM} := V_{IN} = 9\ V$$

$$I_F := (1-D) \cdot I_{OMAX} = 0.044\ A$$

Capacitor

$$V_{CMAX} := V_O + \frac{\Delta V_O}{2} = 5.125\ V$$

$$C := \frac{(1-D)}{8 \cdot L \cdot f^2} \cdot \frac{1}{\frac{\Delta V_O}{V_O}} = 84.175\ nF$$

Choose: $C := 85\ nF$

Simulation Load Resistance

$$R_{LOAD} := \frac{V_O}{I_{OMAX}} = 50\ \Omega$$

Figure 4-8: Design Calculations for Buck Converter Power Stage

Buck-Boost Converter - Power Stage - Main Component Ratings

Parameters:

$V_{IN} := 9\ V$ $V_O := -5\ V$ $I_{OMAX} := 0.1\ A$ $f := 200\ kHz$

$I_{OCCM} := 20\% \cdot I_{OMAX}$ $\Delta V_O := 5\% \cdot |V_O|$ $V_{RIP} := 0.05$

Solution:

$$D := \frac{V_O}{V_O - V_{IN}} = 0.357$$

Inductor:

$$L_{CRIT} := \frac{(1-D)^2 \cdot |V_O|}{2\ f \cdot I_{OCCM}} = 258.291\ \mu H$$

$$L_{SAFETY} := L_{CRIT} \cdot 1.1 = 284.12\ \mu H$$

Choose: $L := 330\ \mu H$

$$I_{SAT} := \frac{V_{IN} \cdot D}{(1-D)^2 \cdot \frac{|V_O|}{I_{OMAX}}} + \frac{V_{IN} \cdot D}{2 \cdot L \cdot f} = 0.18\ A$$

MOSFET:

$$V_{DS} := V_{IN} + |V_O| + \Delta V_O = 14.25\ V$$

$$I_D := \frac{D}{(1-D)} \cdot I_{OMAX} = 0.056\ A$$

Diode

$$V_{RRM} := V_{IN} + |V_O| + \Delta V_O = 14.25\ V$$

$$I_D := I_{OMAX} = 0.1\ A$$

Capacitor

$$V_{CMAX} := |V_O| + \frac{\Delta V_O}{2} = 5.125\ V$$

$$C := \frac{D}{\frac{\Delta V_O}{|V_O|} \cdot f \cdot \frac{|V_O|}{I_{OMAX}}} = 714.286\ nF$$

Choose: $C := 725\ nF$

Figure 4-9: Design Calculations for Buck-Boost Power Stage

Recalling that the output capacitor and inductor are shared between the alternating topologies, one must compromise the final selection such that the components will work in both cases. Therefore, the output capacitance was chosen to be 725nF to account for the Buck-Boost ripple. A higher capacitance on the Buck topology will only minimize its output ripple. No detrimental effect in selecting the higher 725nF capacitance. The inductance was chosen to be 330µH because it will exceed the critical inductances in both cases. Additionally, at this value, the inductor is available in a surface mount package. The next largest available inductor size would be 470µH and this was deemed too high of a value.

After determining the inductor and capacitor values, an AC analysis is performed on both the buck and buck-boost topologies in open-loop to observe the transfer functions. The goal is to observe the gain and the phase at the crossover frequency of 40kHz. A reference voltage is applied to the PWM comparator such that the output is set to 5V or -5V accordingly. Figures 4-9 through 4-12 summarize the circuits used for open-loop tests.

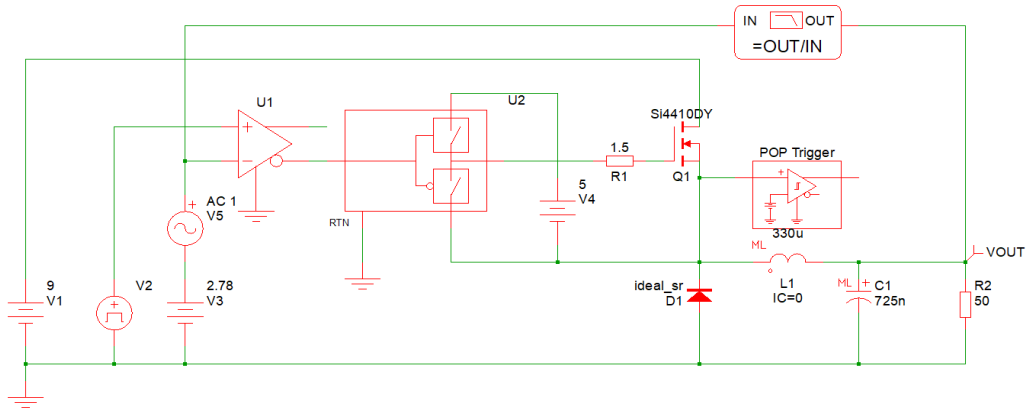

Figure 4-10: Buck Converter Open-Loop Test Configuration

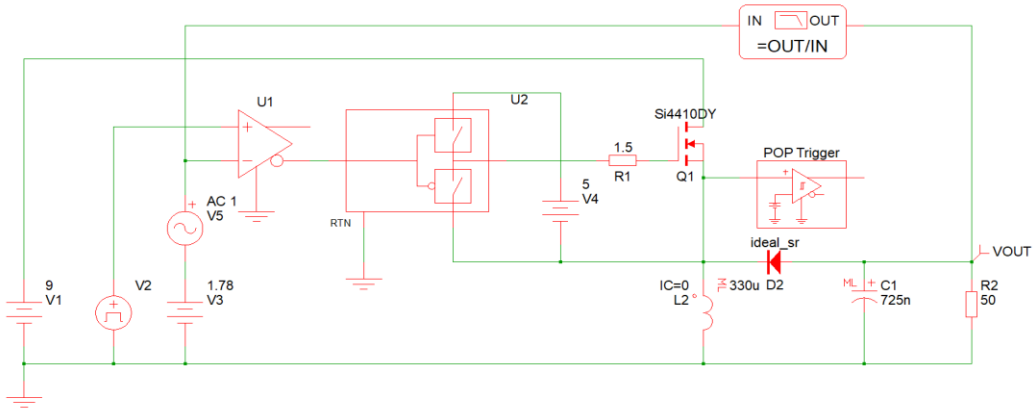

Figure 4-11: Buck-Boost Converter Open-Loop Test Configuration

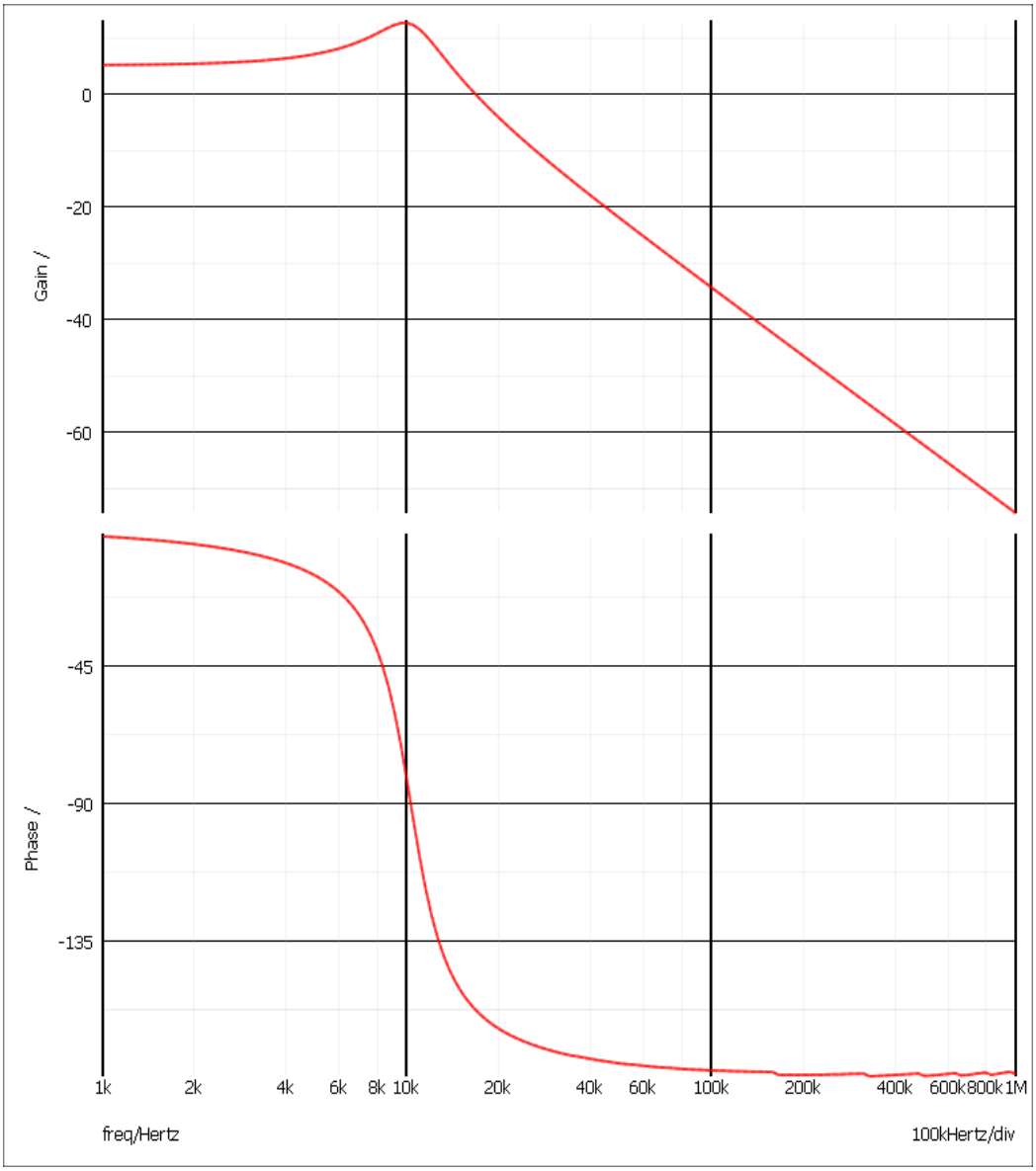

Figure 4-12: Buck Converter Bode Plot (-17dB, -173°) at crossover frequency

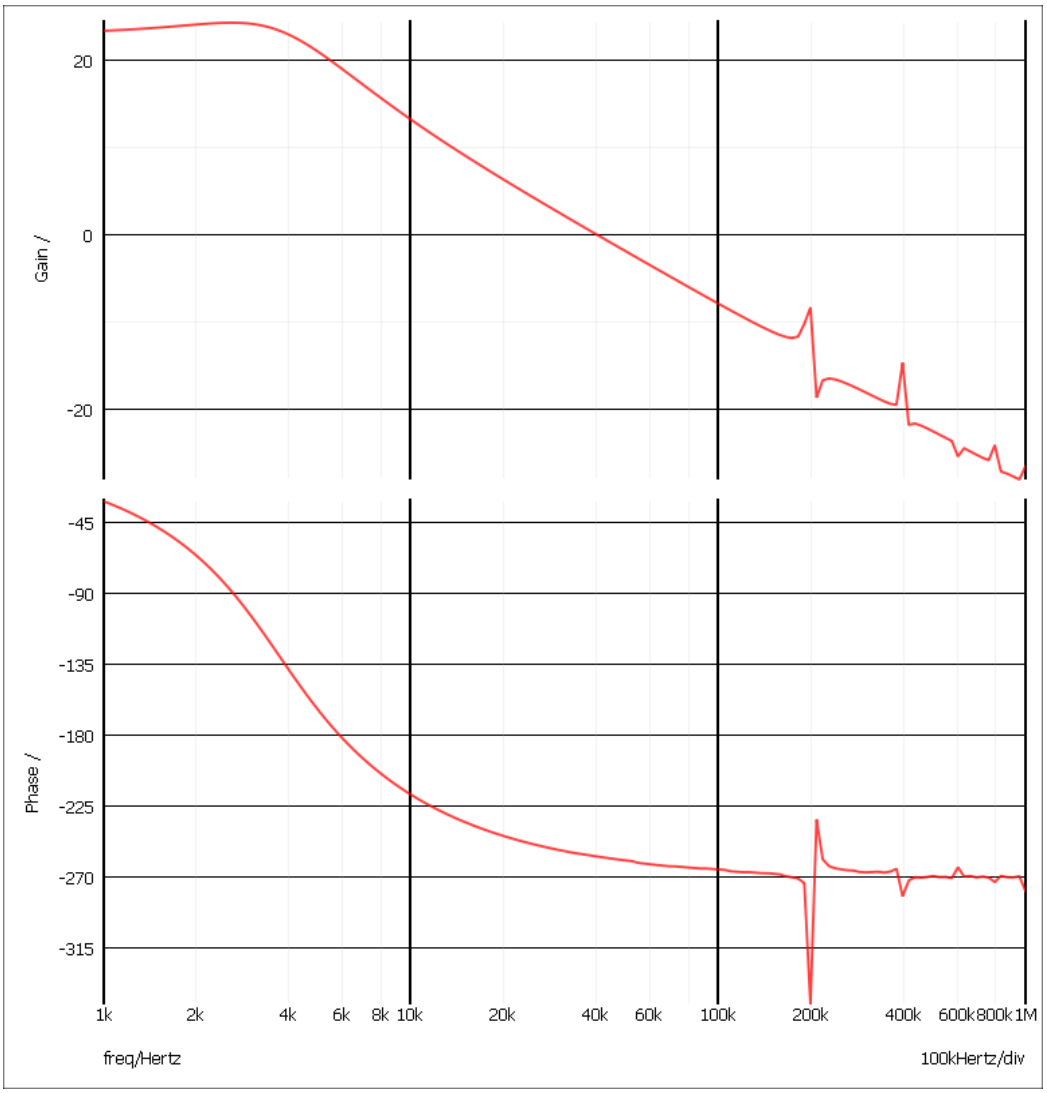

Figure 4-13: Buck Converter Bode Plot (-14dB, -256°) at crossover frequency

From the transfer function plots, it becomes clear that a compensator is needed to boost the phase. The following equations were pulled from Texas Instruments' Application Report "Demystifying Type II and Type III Compensators Using Op-Amp and OTA for DC/DC Converter". The design is performed by selecting the location of the poles and zeros. General guidelines are to set the locations of the zeros a decade below the desired crossover frequency. The second guideline is to set the location of the poles a decade above or at the switching frequency. One must arbitrarily set R1 so that the other components can be solved for.

Iterative analysis and calculations should be performed such that the desired gain and phase boost occur at the desired crossover. The following page shows the transfer function plot of the Type III compensator designed on this page. The page also verifies that the compensator will meet the phase margin criteria and thus stabilize the system.

Type III Compensator Design Equations

Parameters:

$f_{p1} := 200\ kHz$ $f_{p0} := 8\ kHz$ $f_{z2} := 8\ kHz$

$f_{p2} := 200\ kHz$ $f_{z1} := 8\ kHz$ $R_1 := 5\ k\Omega$

Component Equations

$$C_1 := \frac{(f_{p2} - f_{z2})}{2\ \pi \cdot R_1 \cdot f_{p0} \cdot f_{p2}} = 3.82\ nF$$

$$C_2 := \frac{(f_{p1} - f_{z1})}{2\ \pi \cdot R_1 \cdot f_{p1} \cdot f_{z1}} = 3.82\ nF$$

$$C_3 := \frac{f_{z2}}{2\ \pi \cdot R_1 \cdot f_{p0} \cdot f_{p2}} = 0.159\ nF$$

$$R_2 := \frac{(R_1 \cdot f_{p0} \cdot f_{p2})}{(f_{p2} - f_{z2})\ f_{z2}} = 5.208\ k\Omega$$

$$R_3 := \frac{(R_1 \cdot f_{z1})}{f_{p1} - f_{z1}} = 0.208\ k\Omega$$

Figure 4-14: Type III Compensator Design Equations

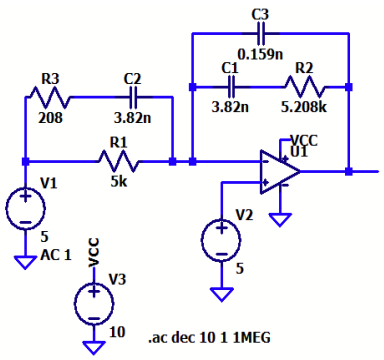

Figure 4-15: Type III Compensator Simulation Results

The following summarizes the results:

Desired Crossover Frequency:	40kHz
Gain at Crossover Frequency:	14dB
Phase at Crossover Frequency:	223 degrees
Effective Phase Boost:	223 deg - 90 deg = 133 degrees
Buck Phase Margin:	(-173+133) = 50 degrees
Buck-Boost Phase Margin:	(-226+133) = 93 degrees

Figure 4-16 implements the designed type III compensator error amplifier to the Buck converter. This effectively closes the loop of the Buck converter and provides stability control. Table 4-1 shows the Bill of Materials for the components used in the converter method.

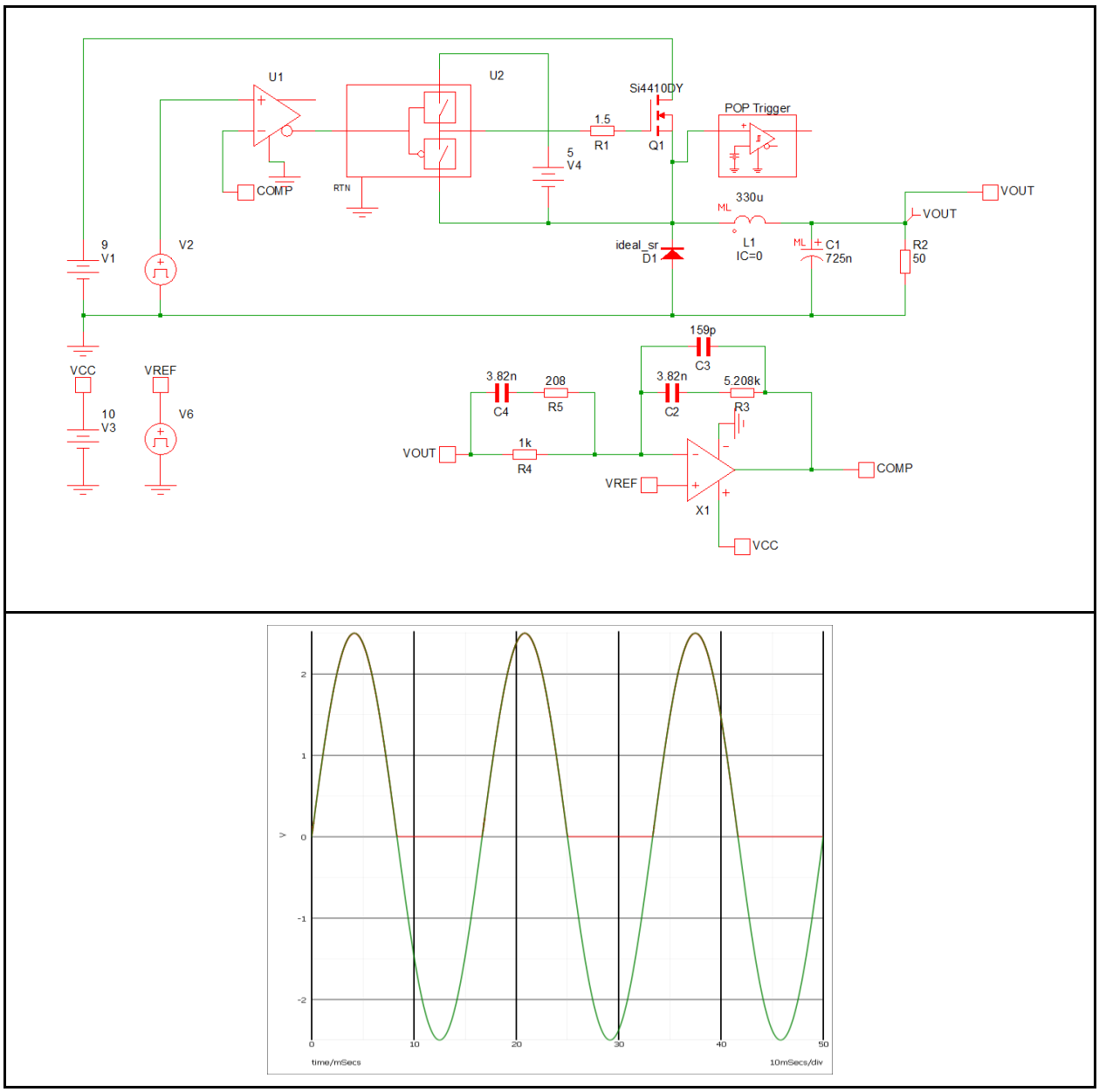

Figure 4-16: Type III Compensator Implementation to Buck Converter

Table 4-1: Bill of Materials for Converter Method

Count	RefDes	Value	Description	Size	Part Number	Manufacturer	Per Unit Cost $
1	C1	3.9nF	CAP CER 4300PF 50V C0G/NP0 0805	0201 (0603 Metric)	GRM2165C1H432JA01D	Murata Electronics	$0.25
1	C2	3.9nF	CAP CER 4300PF 50V C0G/NP0 0805	0201 (0603 Metric)	GRM2165C1H432JA01D	Murata Electronics	$0.25
1	C3	150pF	CAP CER 150PF 10V C0G/NP0 0805	0805 (2012 Metric)	885012007005	Würth Elektronik	$0.10
1	Co	725nF	RES SMD 49.9 OHM 0.1% 1W 0805	0805 (2012 Metric)	TCJP105M025R0500	AVX Corporation	$1.70
1	R2	5.23k	RES SMD 5.23K OHM 1% 1/2W 1210	1210 (3225 Metric)	ERJ-14NF5231U	Panasonic Electronic Components	$0.25
1	R3	205	RES SMD 205 OHM 1% 1/2W 1210	1210 (3225 Metric)	ERJ-14NF2050U	Panasonic Electronic Components	$0.23
1	RL	50	RES SMD 49.9 OHM 0.1% 1W 0805	0805 (2012 Metric)	PCAN0805E49R9BST5	Vishay Thin Film	$0.23
1	L	330uH	FIXED IND 330UH 2.8A 150 MOHM TH	Through Hole	1433428C	muRata Electronics	$2.49
1	U1	TL5002	Switching Controllers PWM Controller	SOIC-8	TL5002CDR	Texas Instruments	$2.20
7	Q1 - Q9	SI4410DY	MOSFET N-CH 30V 10A 8-SOIC	SOIC-8	SI4410DY	ON Semiconductor	$35
1	U2	MCP1416T-E/OTVAO	Gate Drivers Tiny 1.5 AMP Mosfet Driver	SOT-23-5	MCP1416T-E/OTVAO	ON Semiconductor	$0.65
1	D1, D2	NSRLL30XV2T5G	Diodes - General Purpose, Power, Switching SWITCHING DIODE, SOD 523	SOD-523-2	NSRLL30XV2T5G	ON Semiconductor	$0.27
							$48.62

Multilevel Switching Method:

This method primarily uses switches to periodically change the connection of the solar cells so that the output voltage will be a stepped sine wave. Figure 4-17 shows each cell is modeled as an ideal voltage source, while each switch is an ideal switch powered by an ideal pulse wave.

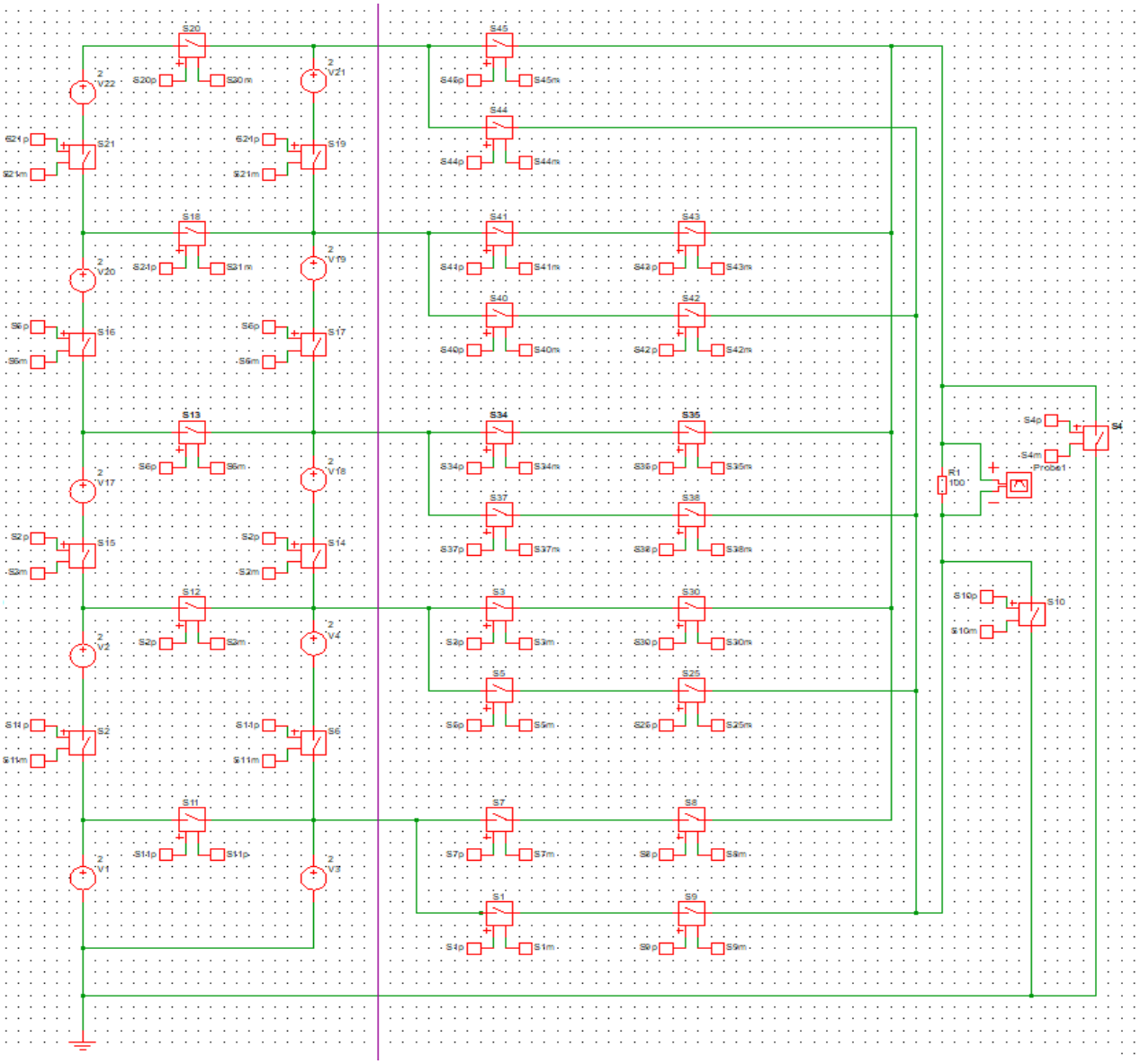

Figure 4-17: Switching Method with 10 Solar Cells

In Figure 4-17, everything to the left of the purple line is the connection of solar cells with other solar cells. This handles changing the steps of the output voltage by connecting the cells in series or connecting them in parallel. Every additional parallel network of solar cells will require two switches per cell, while every additional "step" (series network) of solar cells will require three switches and two cells. On the right of the red line are switches that handle switching between the positive half cycle and negative half cycle of the output. Every additional parallel network of solar cells will require two switches per cell, while every additional "step" (series network) of solar cells will require three switches and two cells. This configuration requires a total of 31 switches. Figure 4-18 shows the first level of a connection of solar cells while Figure 4-19 shows the first level of switches that connect the solar cells to the load. Table 4-2 shows the Bill of Materials for the switch approach.

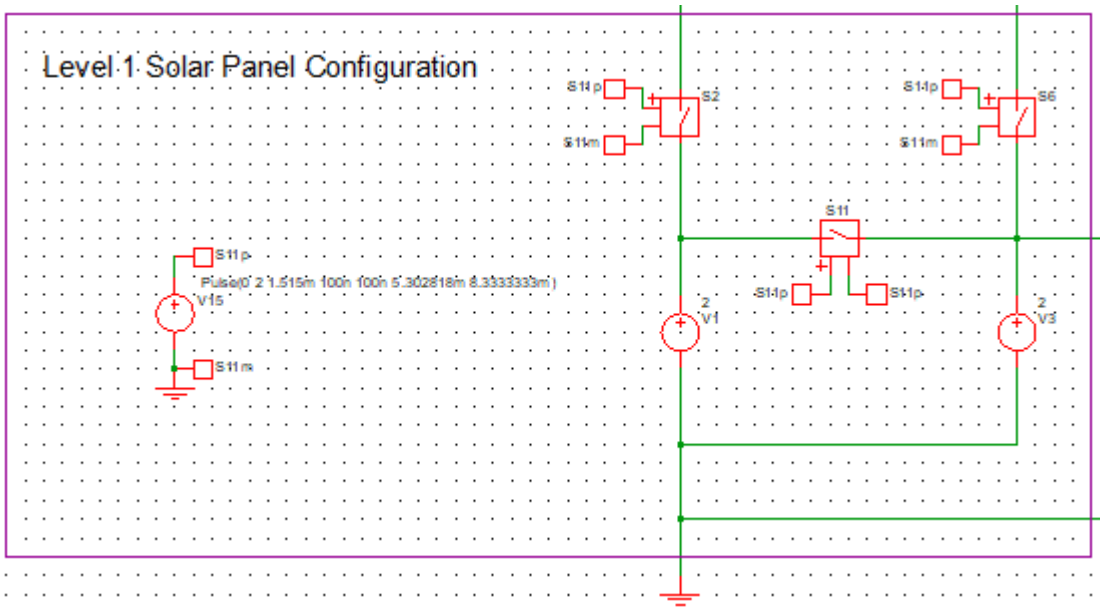

Figure 4-18: Level 1 Solar Panel Configuration

In Figure 4-18, the pulse wave controls all three of the switches. Switch S2 and S6 start open, while switch S11 starts closed. V1 and V2 are the solar cells.

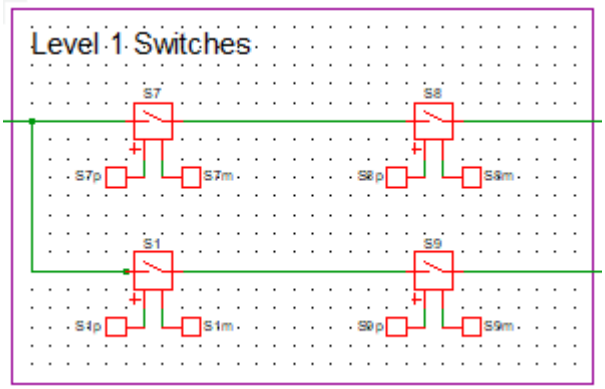

Figure 4-19: Level 1 Switches

In Figure 4-19, switches S7 and S1 start open, while switches S8 and S9 start closed.

Figure 4-20 shows the pulse waves that control the switches.

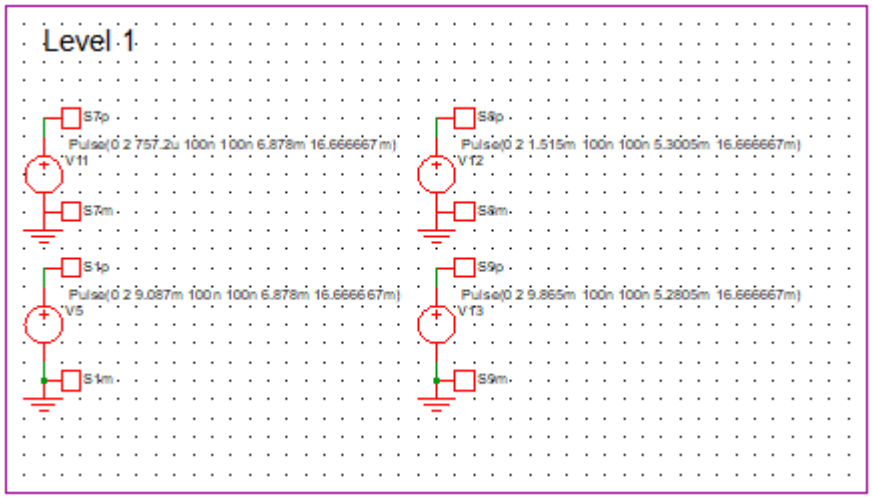

Figure 4-20: Level 1 Switch Controllers

Figure 4-21 shows the switches and their controllers that control the positive and negative half cycles. Both switches start open.

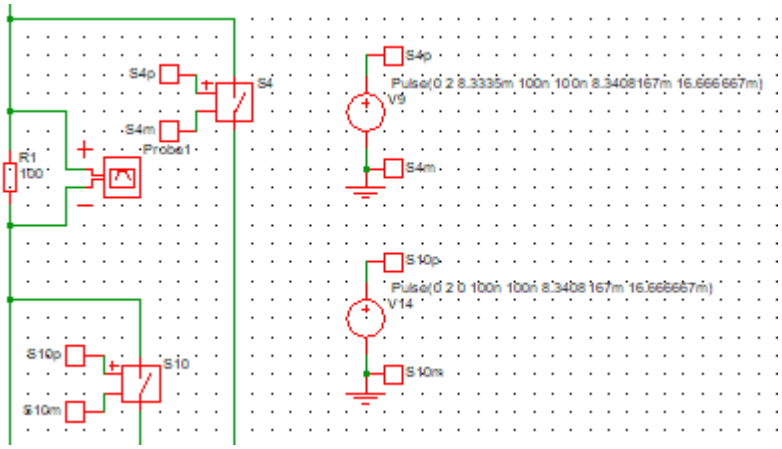

Figure 4-21: Switches for Positive and Negative Cycles

Figure 4-22 shows the switch controllers for levels 2-5. Note that each level has the same setup as seen through Figure 4-18 through Figure 4-20, the main differences are the different values.

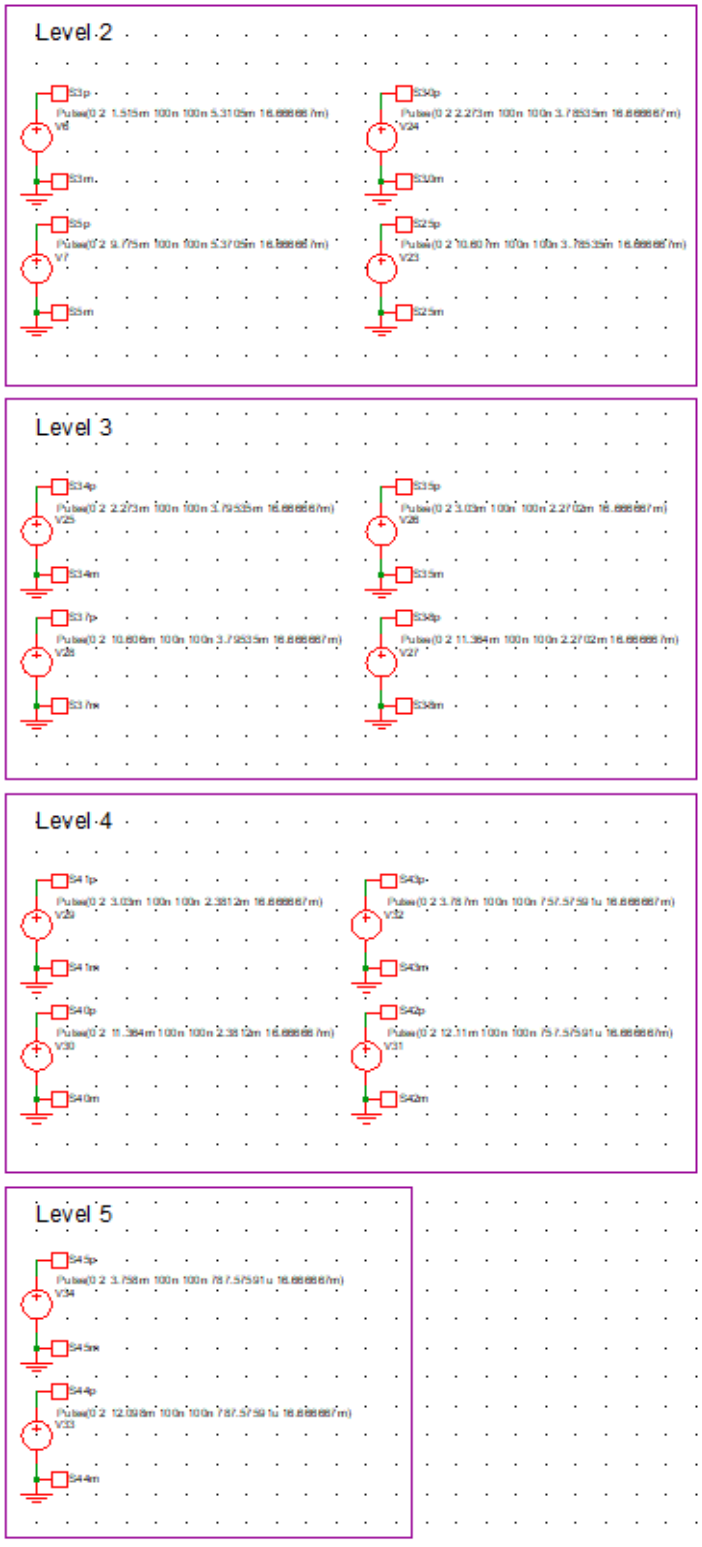

Figure 4-22: Switch Controllers for All Levels

Table 4-2: Bill of Materials for Switching Method

Count	RefDes	Description	Size	Part Number	Manufacturer	Per Unit Cost $
31	S#	MOSFET 56mOhm, SMD	2.9mm x 1.3mm	IRLML0040TRPBF	Infineon Technologies	$0.47
10	V#	AOSHIKE - B01NCQRCQR - 32110000	7.6 x 5.2 x 3.11 inches	B01NCQRCQR - 32110000	AOSHIKE	$0.16
						$16.17

Chapter 5. Simulation Results

Chapter 5 discusses the simulation aspects of the project. Rationale for the simulation software choice and simulation setup are discussed. Simulation results are provided and discussed in detail.

Software Choice

Simulation is a critical process in the development of new hardware designs. Through simulations, the designer can verify whether their designs will work. There exists several circuit simulation software, the most popular being based around the SPICE engine. These SPICE based simulators include programs such as OrCAD and LTSPICE. An alternative to the SPICE engine is MATLAB's Simulink. However, the programs listed are considered general purpose and are not necessarily optimized for power electronics. Instead, we decided to use a software tool known as SIMPLIS which is optimized specifically for switch mode power supplies. SIMPLIS is capable of performing up to ten to fifty times faster than SPICE based simulators by modeling devices via a series of straight-line segments instead of solving nonlinear equations.

SIMPLIS offers the accuracy of SPICE based simulators, an industry standard, while providing faster performance. For the purposes of adjusting and fine tuning the compensator discussed in Chapter 4, a fast simulator would be ideal for quickly selecting component values that increase stability. It is possible to import SPICE models such as diodes, MOSFETs, IGBTs, into SIMPLIS via a conversion process. In addition, SIMPLIS provides adjustable digital and analog models for developing or simulating controller schemes.

Simulation Setup for Converter Topology

The five points of interest for simulation results are the input voltage, output voltage, output current, output power and voltage reference waveforms. SIMPLIS voltage and current probes are placed into these locations. The current probe and power probe are attached to the load resistor on the node labelled VOUT. Voltage probes are placed in their respective location of interest.

For the purposes of simulation, a nominal 9V input supply is assumed. The control scheme operates on voltage control mode; therefore, the controller requires a voltage reference. The voltage reference used is sinusoidal with zero DC offset with an amplitude of 5V; thus, swinging from -2.5 to 2.5V. The sinusoidal voltage reference operates at 60Hz. It should be noted that the voltage reference amplitude can be reduced, but it will require readjusting the voltage divider network into the compensator network to appropriately scale down the output voltage.

Simulation Results

The waveform plots and frequency measurements show successful sinusoidal output from a DC input. The output voltage and output current waveforms as shown in Figure 5-1 are successfully following a scaled version of the sinusoidal voltage reference. Table 5-1 summarizes the simulation results.

It is possible to reduce the amplitude of the voltage reference; however, this requires adjusting the resistor divider network on the error voltage compensator. For convenience, the error voltage compensator is shown in Figure 5-2. One simply needs to adjust R4 and R5 shown below such that the voltage divider produces a voltage comparable to the voltage reference

amplitude from the output voltage. For example, the 5V output and the 2.5V amplitude voltage reference require resistors of equal value to produce a 0.5 ratio.

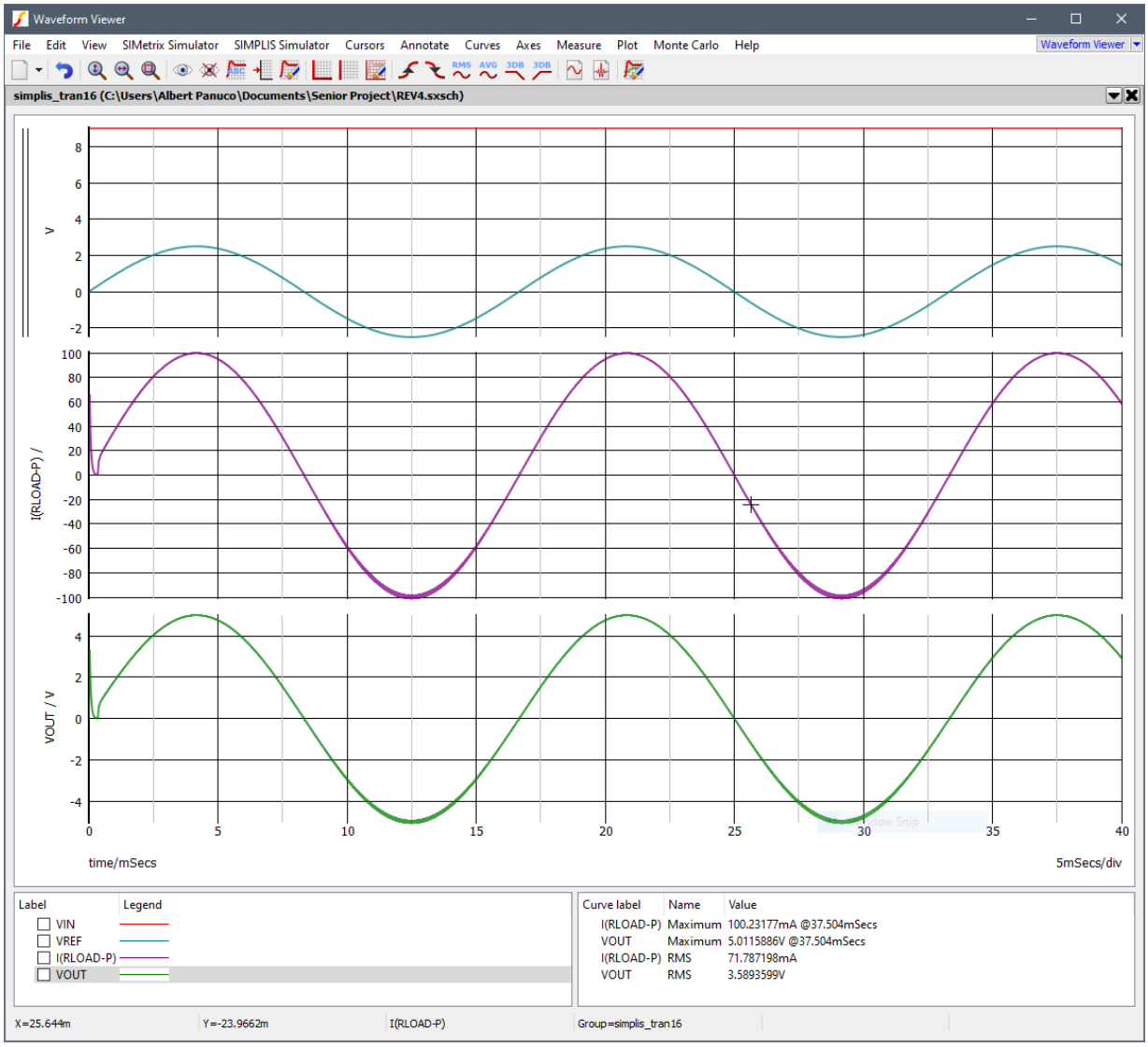

Figure 5-1: Simulation Waveforms (Descending Order of Waveforms)
Input Voltage (Blue)
Voltage Reference (Teal)
Load Current (Purple)
Output Voltage (Green), Note: Vertical Scaling is in 20mA/division

Table 5-1: Tabulated Measurements of Simulation Waveforms

Waveform	Amplitude	Frequency	RMS Measurement	Desired RMS
Input Voltage	9V	0 Hz	N/A	N/A
Voltage Reference	2.5V	60 Hz	1.768 V	N/A
Output Voltage	5.011V	60 Hz	3.589 V	5V
Output Current	100.23mA	60 Hz	71.876 mA	100mA

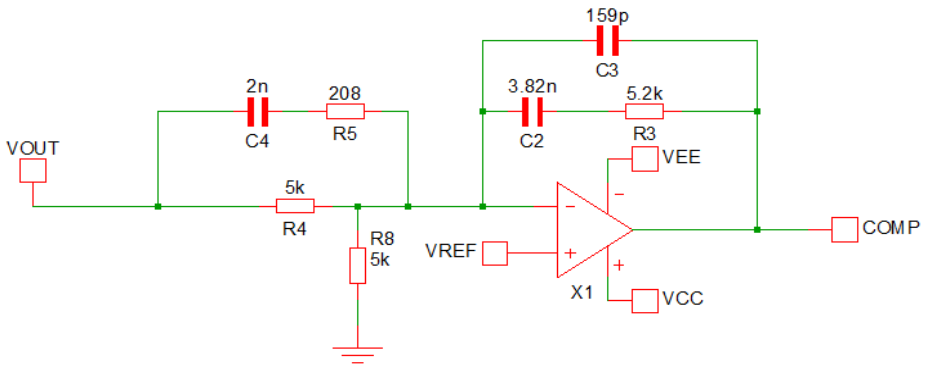

Figure 5-2: Error Voltage Compensator Network

One important measurement for an AC inverter output is the Root-Mean-Squared (RMS) of the AC output waveform. Neither the output voltage nor the output current meets the desired RMS values. Instead, the peak or amplitude values meet the desired RMS values. This ultimately means that the design equations and considerations were incorrect in that the equations used are intended to DC-DC converters that establish DC outputs with ripple. The solution to the problem is to increase the amplitude of the output voltage, and the output current is root two times the desired RMS value. To accomplish this, one must scale the voltage reference by root two times. For completeness, one should recalculate the maximum duty cycle achieved by the new output voltage amplitude; it may be possible to reduce the size of the inductor and output capacitor

provided one is willing to recalculate the compensator values. A simulation run with a higher voltage reference will be shown to confirm the method described above.

Present in both the output voltage and output current waveforms is higher frequency distortion during Buck-Boost mode (otherwise known as the negative half cycle). One possibility for the higher frequency distortion is that the design implements a single compensator that is used in both modes. The Buck mode appears to have tighter control than the Buck-Boost mode. A suggestion could be to test different values for the compensator to reduce the distortion. This is better than having two compensators (one for each mode) since the design would introduce far more complexity. The following sections will examine the output voltage ripple during Buck mode and Buck-Boost mode as well as the output current ripple.

Output Voltage Ripple - Buck Mode

The design equations described in Chapter 4 accounted for an output voltage ripple of 5%. This equates to a voltage ripple of 25mV.

The output voltage ripple in buck mode is within specifications as shown in Figure 5-3 and Table 5-2. In fact, the ripple is a tenth of the ripple accounted for. Recall that the topology switches between buck and buck-boost mode. Yet in both modes, it must share the inductor, the main switch, and the output capacitor. The buck-boost mode required a larger capacitor than the buck mode, therefore the buck mode has significantly smaller output voltage ripple. One can expect that the output voltage ripple for the buck-boost mode will be significantly higher and closer to the 5% design consideration.

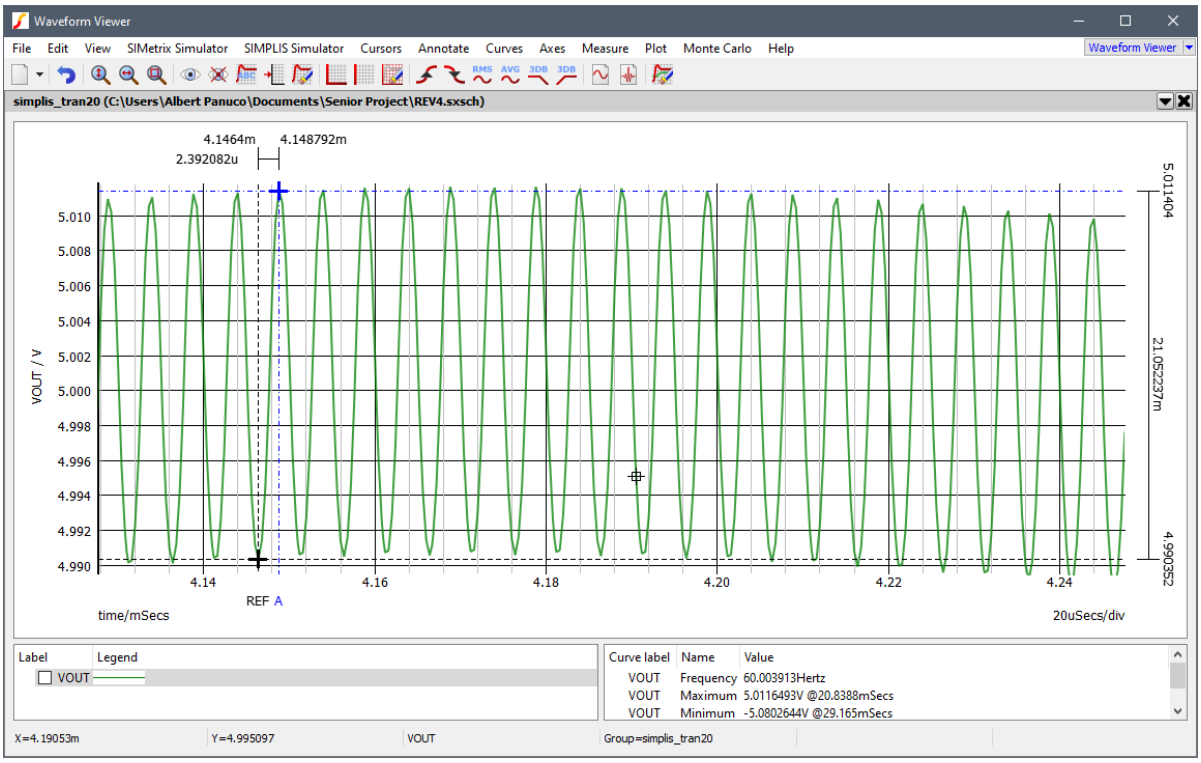

Figure 5-3: Output Voltage Ripple Buck Mode Waveform

Table 5-2: Tabulated Output Voltage Ripple Buck Mode

Cursor One	Cursor Two	Measured Ripple	Desired Ripple
4.990352V	5.011404V	21.062mV	250mV

Output Voltage Ripple – Buck-Boost Mode

The design equations described in Chapter 4 accounted for an output voltage ripple of 5%. This equates to a voltage ripple of 25mV.

The output voltage ripple in buck-boost mode is within specifications as depicted in Figure 5-4 and Table 5-3. As previously discussed, the measured output ripple is significantly higher in buck-boost mode than in buck mode. This is a result of the buck-boost mode requiring a larger output capacitance than the buck mode; therefore, the buck-boost mode output voltage ripple is much closer to the desired ripple.

The conclusion is that the distortion present in the simulation waveforms was a result of the output voltage ripple differences between Buck and Buck-Boost mode and not of the compensator. The ripple can potentially be reduced further by increasing the output capacitance; however, this will require adjusting the compensator network. Since both modes operate within specification, no recommendation is given to increase the output capacitance prior to a hardware construction and test.

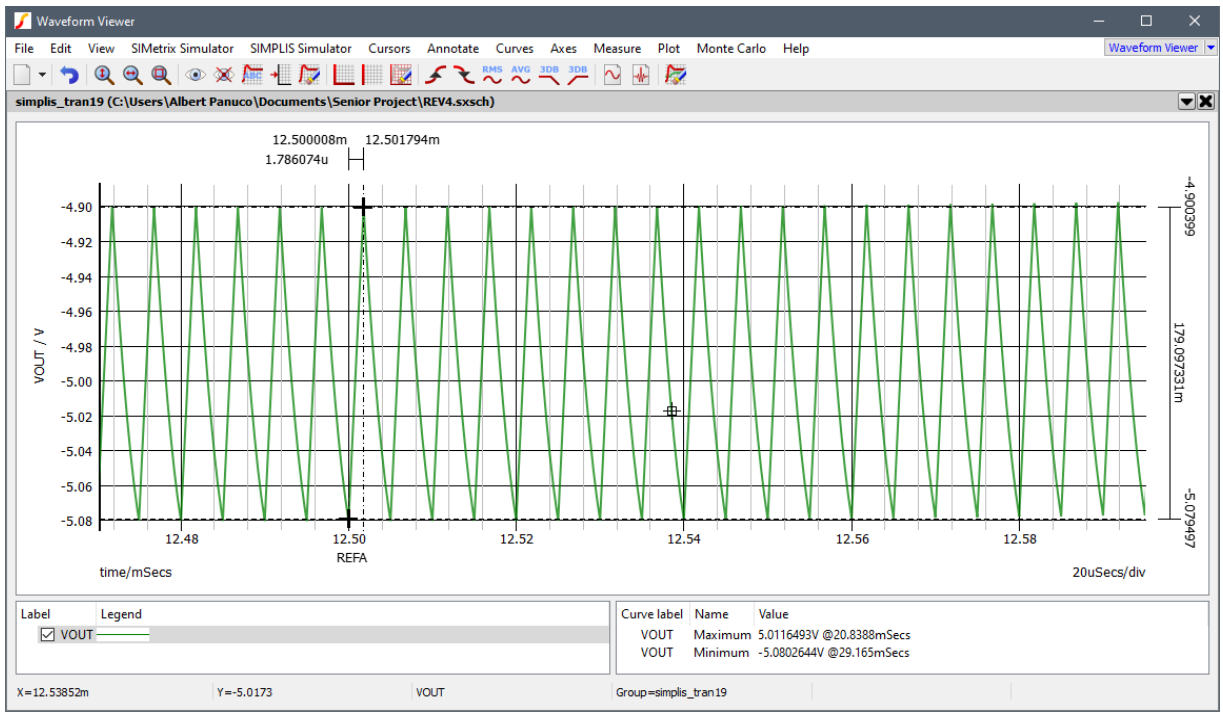

Figure 5-4: Output Voltage Ripple Buck-Boost Mode

Table 5-3: Tabulated Output Voltage Ripple Buck-Boost Mode

Cursor One	Cursor Two	Measured Ripple	Desired Ripple
-4.900	-5.079	179mV	250mV

Output Current Ripple

The output current ripple is within specifications. The measured ripple is an order of magnitude lower than the desired ripple as depicted in Figure 5-5 and Table 5-4. This opens the possibility of reducing the inductor size. However, if one chooses to decrease the inductor size, then a recalculation of the output filter and the compensator will be required. Furthermore, for an AC inverter, it may be more desirable to have less ripple in general since that will produce a waveform closer to a pure sinusoid. No recommendation is given to reduce the inductor size until an analysis with hardware is performed to see the impact of the current ripple on a device such as an electronic load.

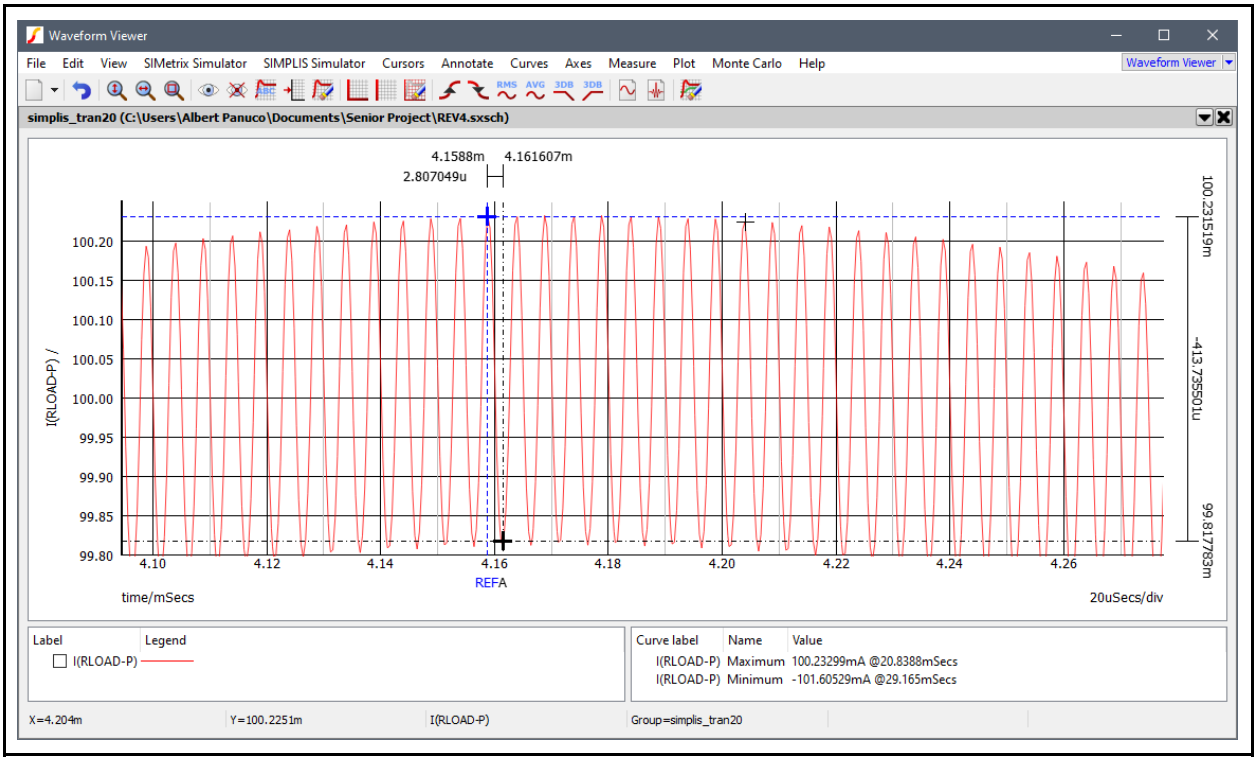

Figure 5-5: Output Current Ripple Waveform

Table 5-4: Tabulated Output Current Ripple

Cursor One	Cursor Two	Measured Ripple	Desired Ripple
100.231mA	99.817mA	413uA	5mA

Output Power

For the purposes of developing a low wattage AC inverter for solar cell applications, the measurement of interest from the output power measurements is the average output power measurement. As expected, distortion present in Buck-Boost mode is also present in the output power waveforms.

As expected, and as shown in Figure 5-6 and Table 5-5, the average output power did not meet the desired 500mW output power. Again, the conclusion that can be drawn was that the voltage reference was set to establish a peak output voltage and a peak output current. For an AC inverter, this approach was incorrect. The following pages provide a simulation in which the voltage reference was increased by root two times. This is done to verify if scaling the voltage reference will lead to the desired RMS output voltage, output current, and average (mean) output power.

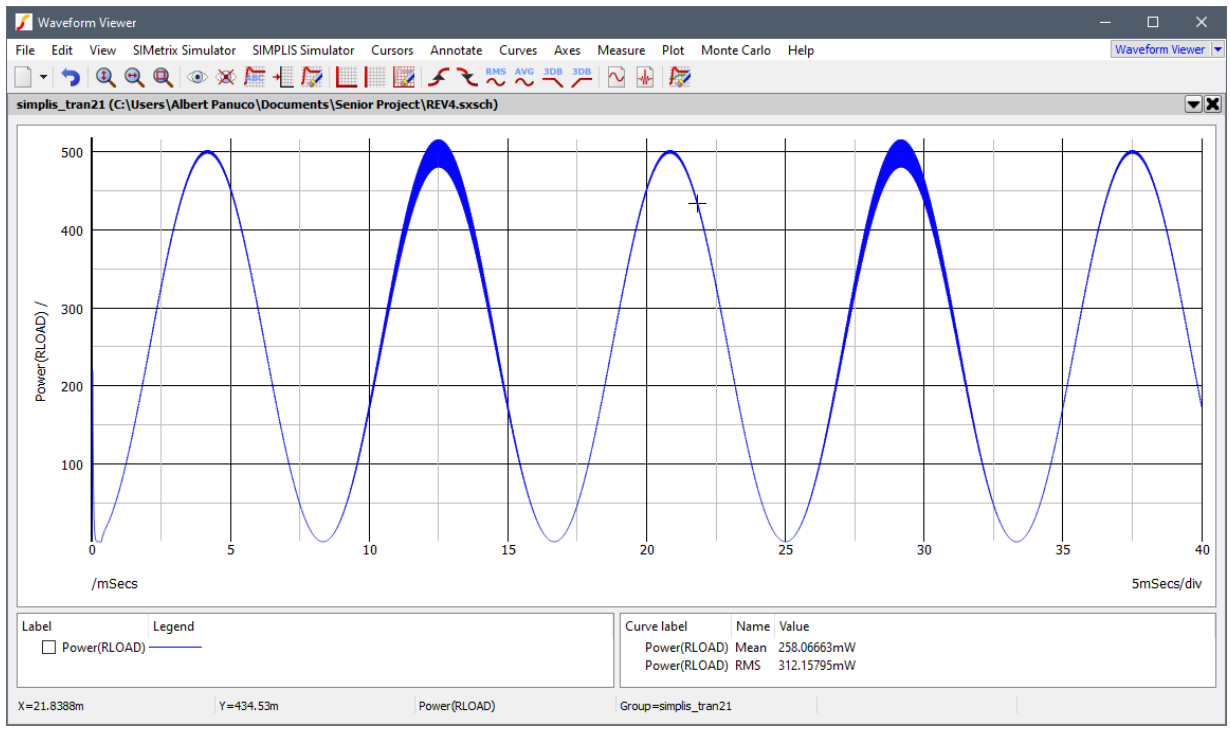

Figure 5-6: Output Power Waveform

Table 5-5: Tabulated output power measurements

Measured Average Output	Desired Average Output
312mW	500mW

Simulation Waveforms with Adjusted Voltage Reference

Once again, successful sinusoidal output was produced in the output voltage and output current. This is illustrated in Figure 5-7 and tabulated in Table 5-6. Adjusting the voltage reference amplitude set the RMS values to their desired values and are now within specification. However, consequently the input voltage had to be increased further. The design would not operate properly in buck-boost mode at the lower 9V input voltage.

If the design cannot operate at the 9V input, this will require configuring solar cells such that a higher voltage can be produced which will require more cells and physical space. This is the only single solution to the problem; it may be possible to operate at the lower voltage if one is willing to reconfigure the control loop. Recall that duty cycle is resolved by setting the desired input and output voltages. Duty cycle determines the component sizing requirements for the inductor and output capacitor, thus affecting the control loop.

Future simulations are recommended to determine, via incremental trial and error, at which input voltage the topology fails to produce the desired sinusoidal output and calculate the duty cycle at these increments. These new duty cycle values can later be used to generate new component values such that a new control (compensator) can be designed.

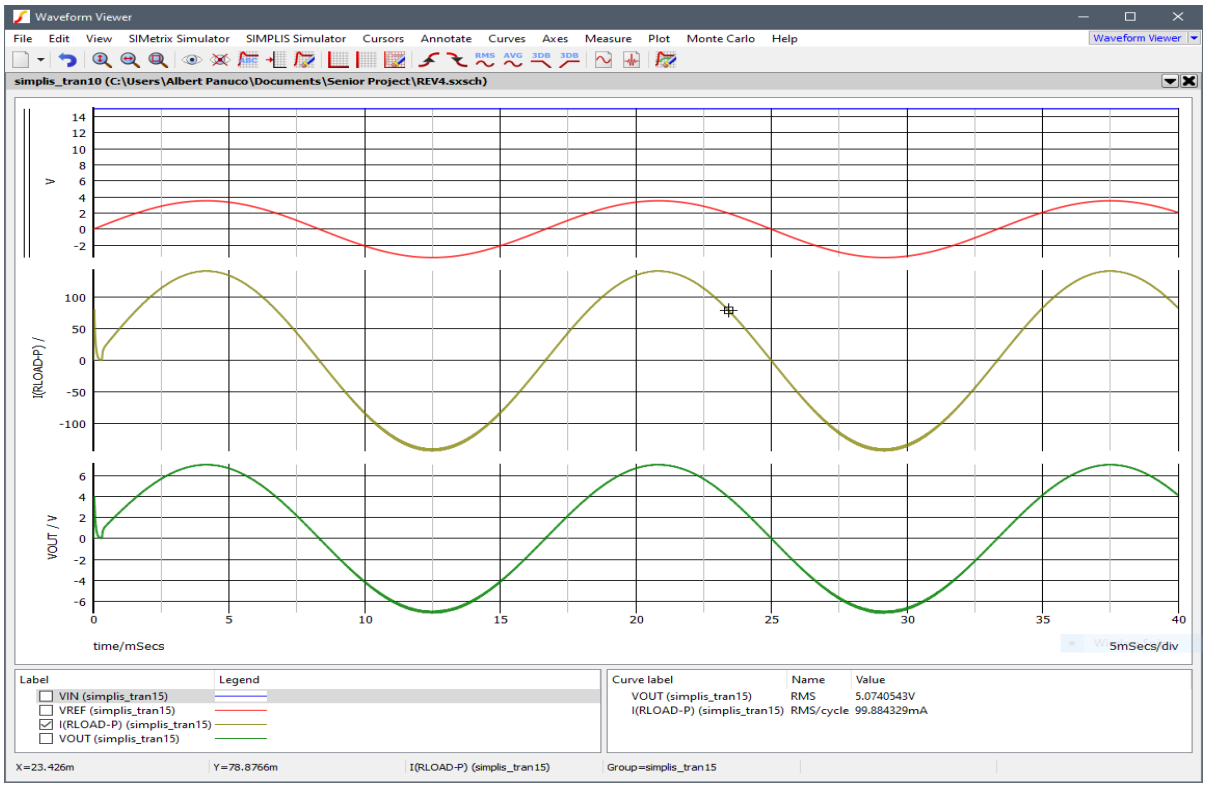

Figure 5-7: Simulation Waveforms
Input Voltage (Blue), Voltage Reference (Red), Load Current (Yellow)
Output Voltage (Green), Note: Vertical Scaling is in 20mA/division

Table 5-6: Tabulated Measurements of Simulation Waveforms

Waveform	Amplitude	Frequency	RMS Measurement	Desired RMS
Input Voltage	15V	0 Hz	N/A	N/A
Voltage Reference	3.53V	60 Hz	2.5V	N/A
Output Voltage	7.175V	60 Hz	5.074V	5V
Output Current	141.257mA	60 Hz	99.884mA	100mA

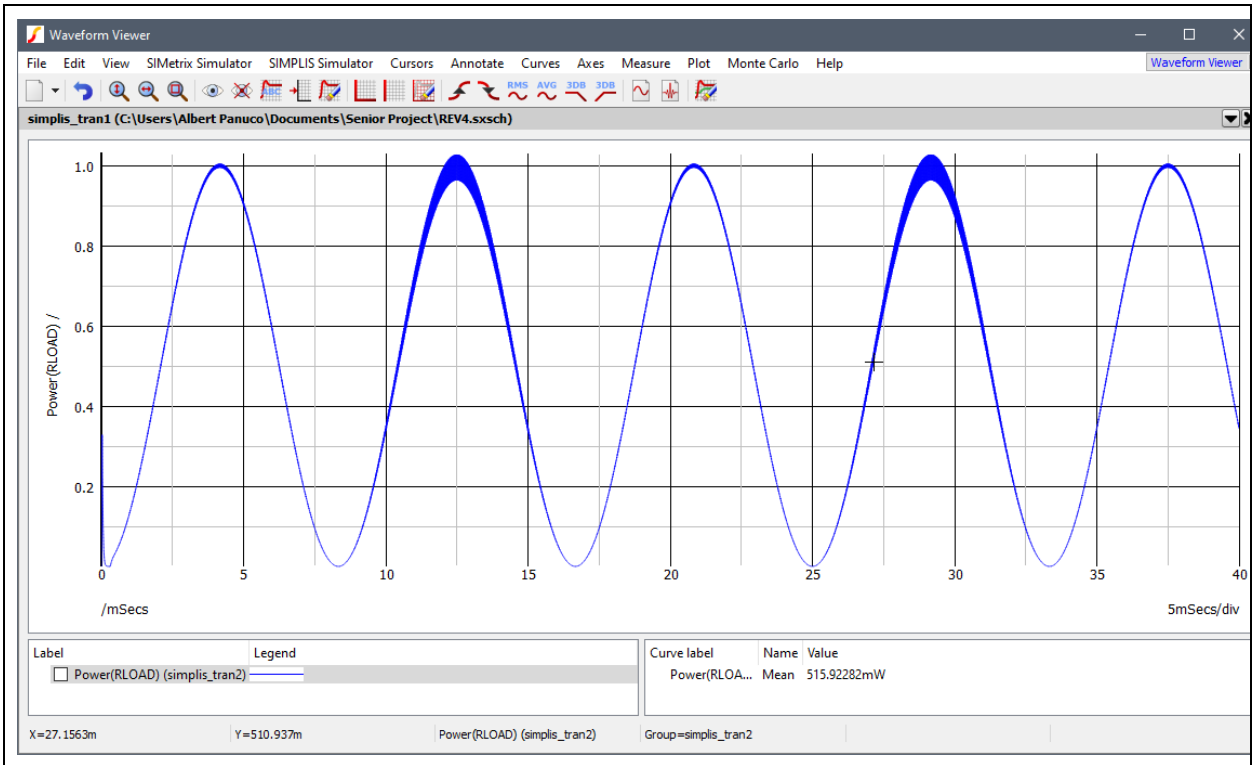

Figure 5-8: Output Power Waveform

Table 5-7: Tabulated output power measurements

Measured Average Output	Desired Average Output
515.92mW	500mW

Simulation Setup for Multilevel Switch Topology

Another method is to use switches that are configured and connected to output a multi-step AC waveform. In the simulation, all components used were ideal. 2V DC sources were used in place of solar panels. A transient simulation was run for 50ms (3 periods at 60 Hz). A 100 Ω resistor was used as the load. A voltage probe was placed across the load to measure the output waveforms.

In Figure 5-8, the voltage waveform successfully steps up to +10V, then down to -10V in steps of 2V. Notice that the 2V is the same as the solar panel (DC sources) voltage. In order to avoid spikes to 0V, the timing of the switches had to be layered so that no two switches on the same node would transition at the exact same time. This required 18 switch drivers (which were ideal pulse waveforms). The output current waveform is shown in Figure 5-9. The waveform follows the output voltage exactly. This is expected since only ideal voltage sources and ideal switches with resistive load were used.

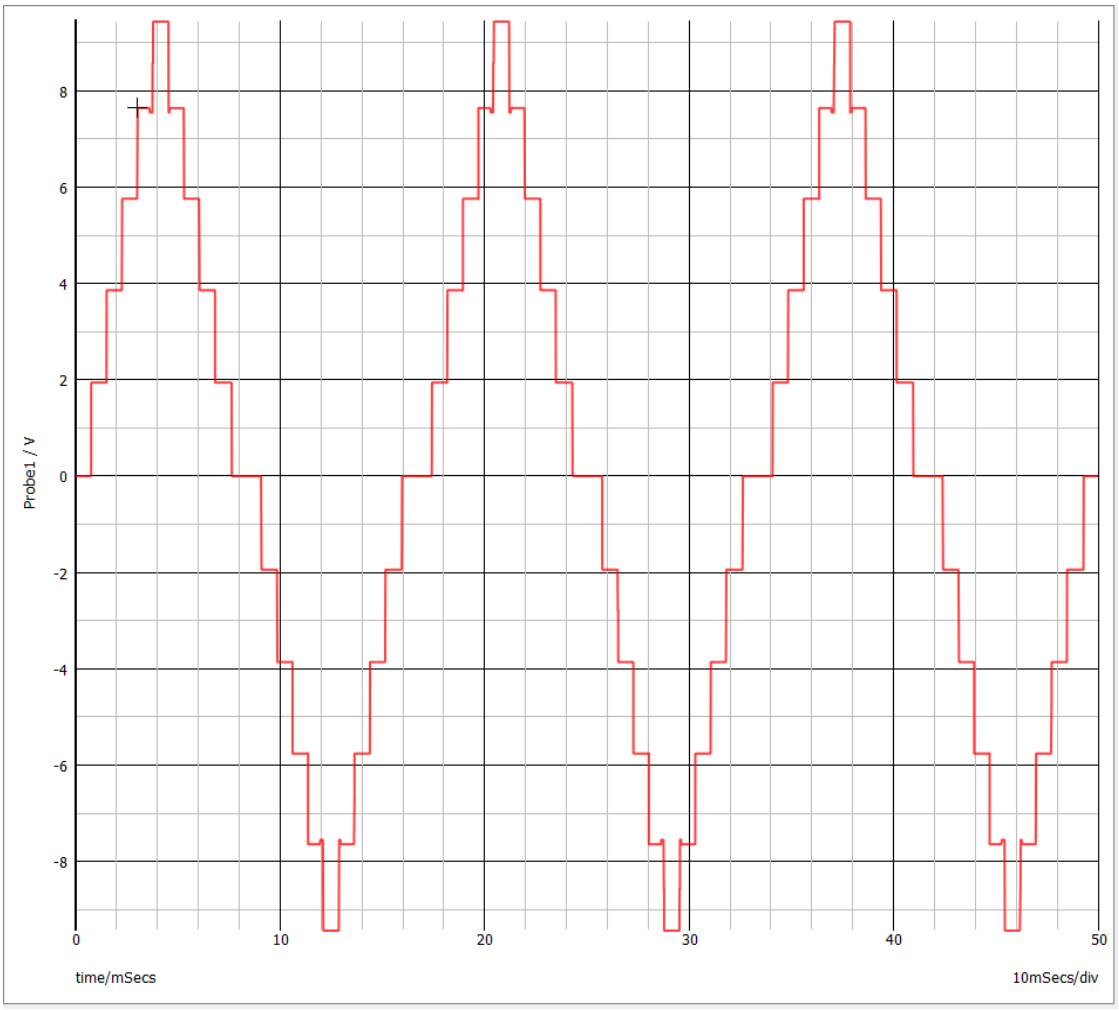

Figure 5-9: Voltage Waveform for Switching Topology Simulation
Output Voltage (Red)

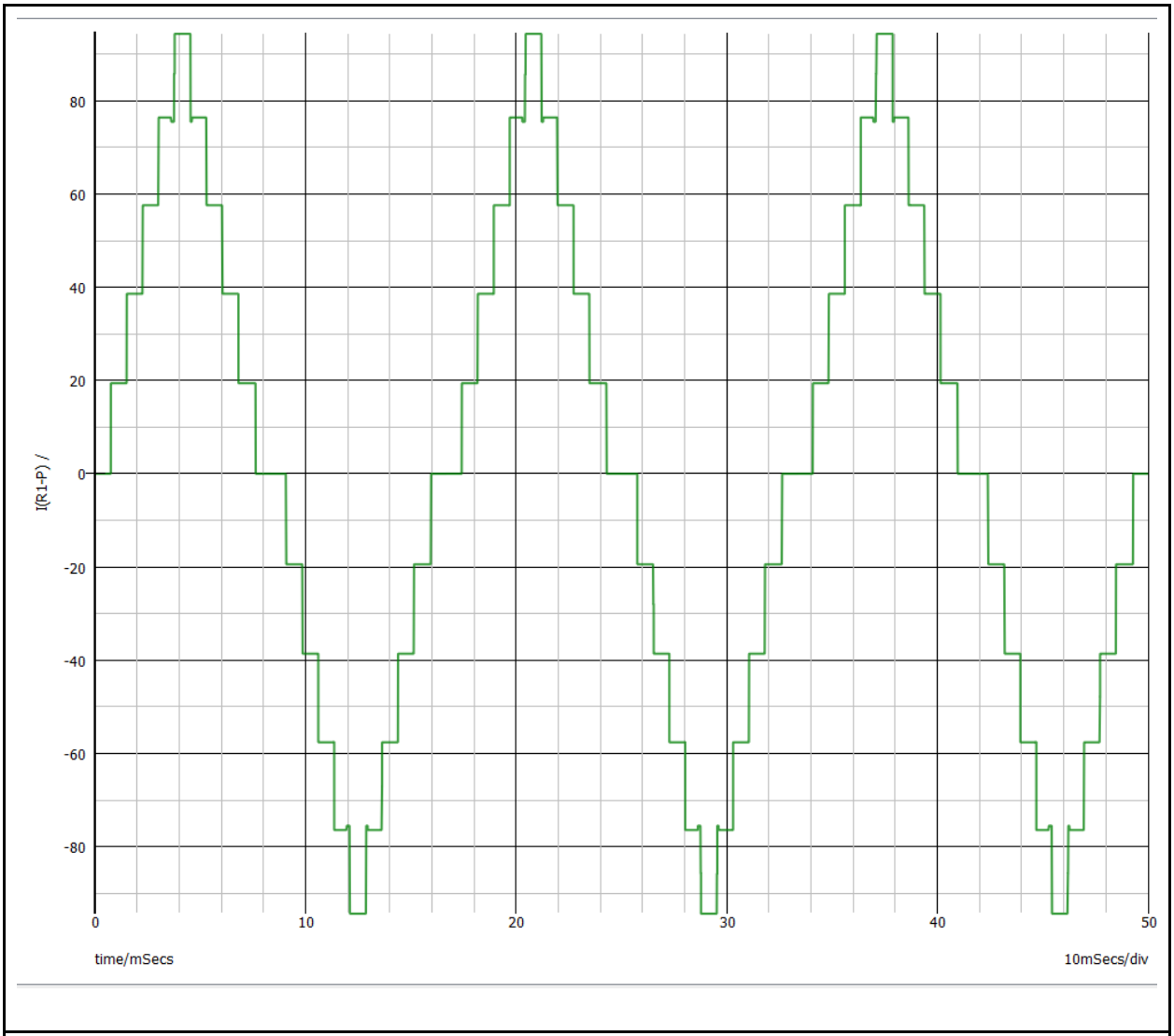

Figure 5-10: Current Waveform for Switching Topology Simulation
Output Current in mA (Green)

Chapter 6: Conclusion

This project focuses on developing an embedded electronics solution for creating solar cells capable of alternating output current.

Initially, the project involved design and simulation followed by a hardware implementation step. Unfortunately, due to the COVID-19 pandemic, access to university resources and laboratory equipment were limited or shut down entirely. Thus, no hardware implementation or testing was performed. Due to the scheduling changes the pandemic caused, the project proceeded with simulation implementations and results only. In addition, a second topology involving switches to achieve a multilevel inverter was simulated and compared to the original topology.

Converter Topology

The concept for the topology discussed in Chapters 3 and 4 is applying an external sinusoidal voltage reference to the feedback control of a switch mode power supply such that the output waveform will follow the reference. Thus, the system will perform as an inverter a DC input voltage. Simulation results presented in Chapter 5 verify that this concept is successful; however, there is a critical flaw with the approach taken in this project.

An inverter must be capable of producing both a positive half cycle and a negative half cycle. Therefore, the approach taken was to implement a design that would switch topologies such that output voltage was positive during the positive half cycle and negative during the negative half cycle of the sinusoidal reference. The design must be capable of switching between topological modes at the zero-voltage crossing of the sinusoidal waveform. To simplify the design, a single control scheme should be used between both modes. To achieve this goal, the

main switch in both topologies must be shared. Furthermore, rather than implementing a boost topology for generating the positive half cycle voltage output, a buck topology was chosen because it shares the location of the main switch with buck-boost topology; the buck-boost topology is the simplest topology for generating a negative output voltage.

Since buck topology was chosen for generating the positive half cycle, the output will be scaled down from the input. Therefore, this topology will not be able to step up the listed 5V DC input into a 10V AC RMS output. In all other regards, such as power and ripple output voltage, the topology is successful. However, for the purposes of scaling the design for household applications that require 120V AC RMS, this design could still be utilized by combining all solar cell small AC outputs into a single AC bus and then use a centralized transformer to get the desired level of the AC voltage.

An additional challenge presented with the design is the lack of a commercially available controller to achieve the combined modes. If one were to pursue a hardware implementation, one would need to construct the feedback controller from individual components. For example, one could configure the TL5002 *Pulse-Width Modulation Control Circuit* from Texas Instruments to implement such a controller [12]. This is the recommended hardware approach to take rather than attempting to provide a sinusoidal reference to a commercially available controller.

Multilevel Switch Topology

The simulations in Chapter 5 show that it is possible to combine switches and solar cells so that a stepped sine wave is created. The topology demonstrated is easily modifiable for expansion through increasing the number of levels, thus increasing the peak voltage, as well as adding more solar cells in parallel, hypothetically increasing the amount of current that can be supplied. However, unless the output voltage is at a peak, there will be some cells that are not connected to the load, resulting in some "unused voltage".

Cost Comparisons:

The sinusoidal voltage reference solution requires a total of seven switches, with five of those switches should be rated for power applications; each would require its own gate driver. While it is possible to find power management ICs (PMICs) that are dual channel for both the switch and gate driver such as the *CSD87333Q3D* and the *BM60212FV-C* available from Texas instruments, cost does play a crucial role in design. As an example, one would need four of each for a hardware implementation. Table 6-1 provides a simple cost analysis with regards to the PMICs listed above.

Table 6-1: Switch and Gate Driver Cost for Converter Topology

Component	Quantity	Cost Per Unit
Switch	4	1.20
Gate Driver	4	4.80
Total Cost:		22.48

The multilevel switch topology requires a total of 33 switches. 25 of these switches will require their own gate driver. Using the same costs as seen in Table 6-1, Table 6-2 shows an example of cost for implementing this approach using the same switches and gate drivers.

Table 6-2: Switch and Gate Driver Cost for Multilevel Switch Topology

Component	Quantity	Cost Per Unit
Switch	33	1.20
Gate Driver	25	4.80
Total Cost:		159.6

It is important to keep in mind that the multilevel switch topology is not complete, as it will likely need some sort of filter, thus increasing its total cost.

Moving Forward

The sinusoidal voltage reference solution which implements a buck and buck-boost mode topology provides a less distorted sinusoidal output than the alternative multilevel switching inverter presented. However, as previously discussed, this particular design requires a higher input voltage than the desired output voltage. This can be problematic if the desired AC output voltage is high, such as the 120V AC found in households. Moving forward, future projects should explore the possibility of implementing a boost and buck-boost mode topology instead; to reiterate, this may require selectively controlling which switch serves as the main switch. If not, one could mitigate the low AC output voltage by using a transformer.

The multilevel switching inverter solution on the other hand, does allow for the output voltage to be higher than any of the individual solar cell voltage inputs. However, disadvantages are the “unused voltage” as well as a less smooth sine wave. Hardware testing will be required to observe the effects of constantly changing the solar cell connections, as well as the necessity of a filter.

Recommendations

The sinusoidal reference converter topology should be further explored using a boost buck-boost combination, otherwise one should consider using a transformer to increase the AC output voltage. The control scheme presented in the converter topology would be less complex than implementing control for the multilevel switch topology; timing for each switch needs to be precise and this can potentially prove to be difficult to implement in hardware. The output of the multilevel switch topology does not compare well to a pure sinusoid while the converter topology shows promise. From a cost perspective, the converter topology requires fewer switches and therefore potential gate drivers. Future projects should focus on implementing the hardware necessary to create the sinusoidal reference converter topology.

References

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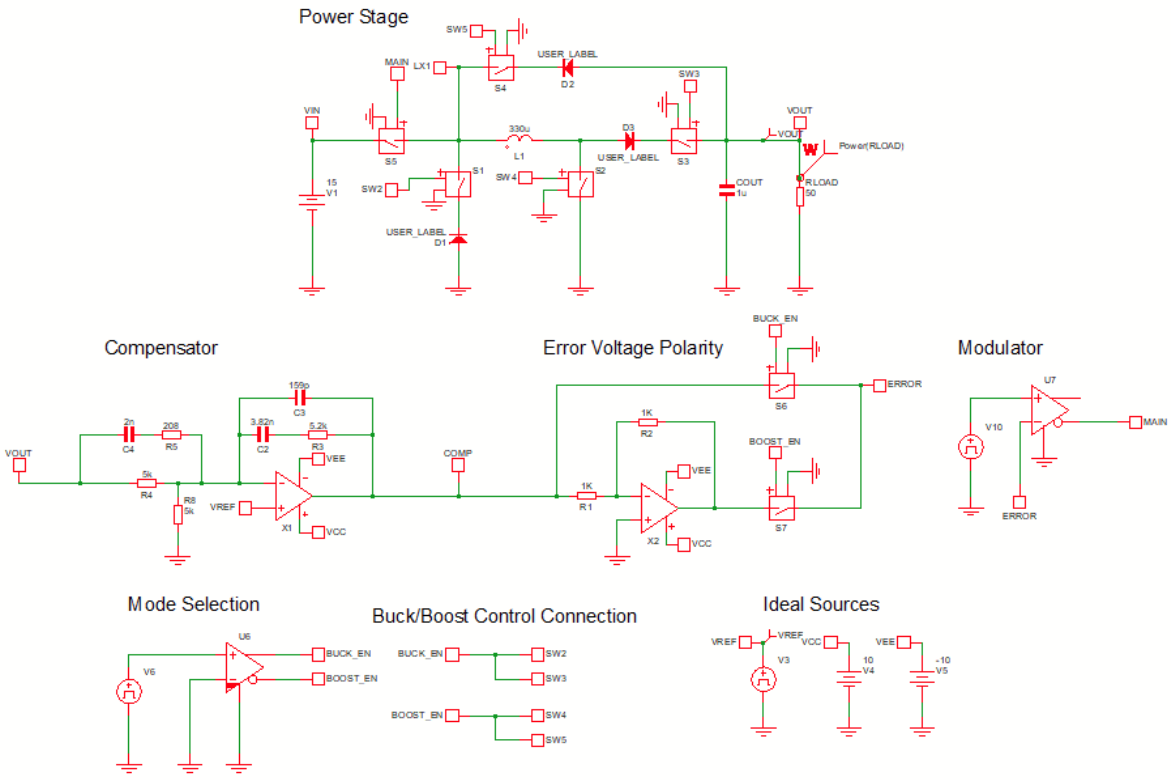
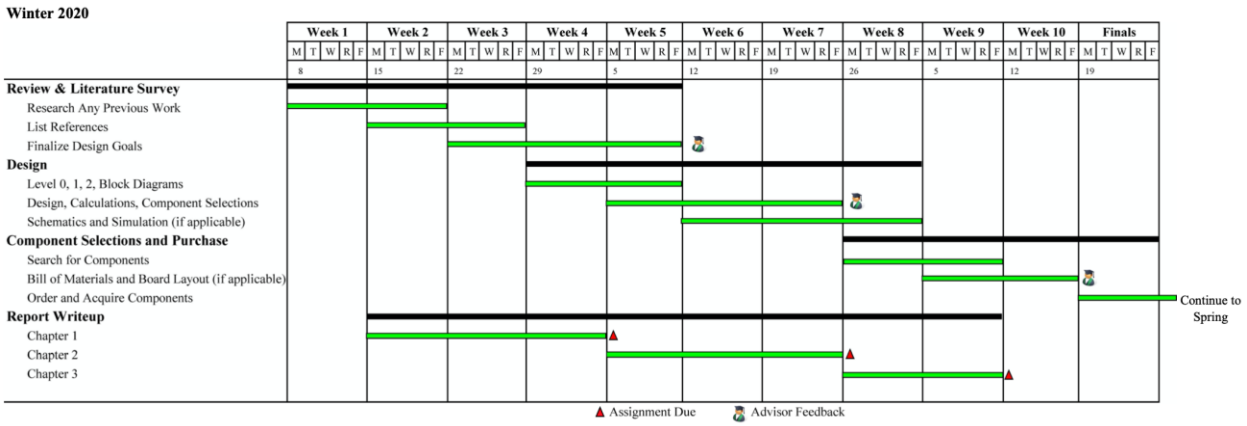
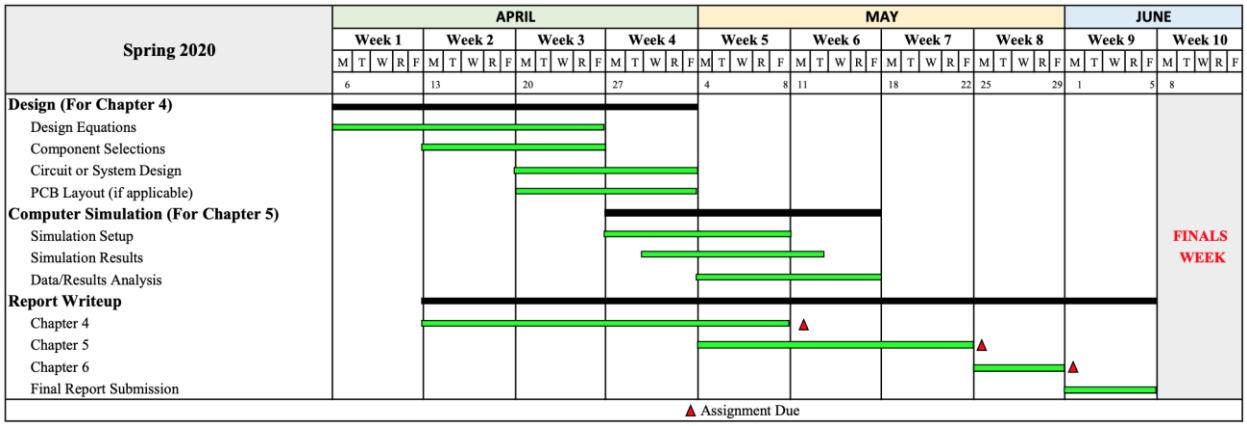
A. Final Schematic for



B. Project Schedule





C. Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	Manufacturer	Per Unit Cost $
1	C1	3.9nF	CAP CER 4300PF 50V C0G/NP0 0805	0201 (0603 Metric)	GRM2165C1H432JA01D	Murata Electronics	$0.25
1	C2	3.9nF	CAP CER 4300PF 50V C0G/NP0 0805	0201 (0603 Metric)	GRM2165C1H432JA01D	Murata Electronics	$0.25
1	C3	150pF	CAP CER 150PF 10V C0G/NP0 0805	0805 (2012 Metric)	885012007005	Würth Elektronik	$0.10
1	Co	725nF	RES SMD 49.9 OHM 0.1% 1W 0805	0805 (2012 Metric)	TCJP105M025R0500	AVX Corporation	$1.70
1	R2	5.23k	RES SMD 5.23K OHM 1% 1/2W 1210	1210 (3225 Metric)	ERJ-14NF5231U	Panasonic Electronic Components	$0.25
1	R3	205	RES SMD 205 OHM 1% 1/2W 1210	1210 (3225 Metric)	ERJ-14NF2050U	Panasonic Electronic Components	$0.23
1	RL	50	RES SMD 49.9 OHM 0.1% 1W 0805	0805 (2012 Metric)	PCAN0805E49R9BST5	Vishay Thin Film	$0.23
1	L	330uH	FIXED IND 330UH 2.8A 150 MOHM TH	Through Hole	1433428C	muRata Electronics	$2.49
1	U1	TL5002	Switching Controllers PWM Controller	SOIC-8	TL5002CDR	Texas Instruments	$2.20
7	Q1 - Q9	SI4410DY	MOSFET N-CH 30V 10A 8-SOIC	SOIC-8	SI4410DY	ON Semiconductor	$35
1	U2	MCP1416T-E/OTVAO	Gate Drivers Tiny 1.5 AMP Mosfet Driver	SOT-23-5	MCP1416T-E/OTVAO	ON Semiconductor	$0.65
1	D1, D2	NSRLL30XV2T5G	Diodes - General Purpose, Power, Switching DIODE, SOD 523	SOD-523-2	NSRLL30XV2T5G	ON Semiconductor	$0.27
							$48.62

D. Analysis of Senior Project Design

Project Title: Solar Panel with Embedded Electronics

Students: Albert Panuco

Timothy Z. Chen

Advisor: Taufik

Summary of Function Requirements:

The prototype solar panel should show a finalized version will maintain all the benefits of current AC solar panel layouts, with the added benefit of bypassing an inverter. The solar panel needs to be efficient and easy to install so that customers are more inclined to buy and use the new solar panels. Since this solar panel will be more complex than current solar panels, an improved data acquisition system will be needed to monitor energy production. The prototype solar panel will be small; however, the solar cell layout will be such that a larger solar panel can be created easily based on our design.

Primary Constraints:

This project is entering a relatively new area of DC-AC voltage conversion. Currently, nearly all DC-AC conversions are done using an inverter. Bypassing the inverter (the crux of our project) is definitely the largest issue. We are also limited by the speed of the switches and the size of the buck converters (inductors and capacitors) we will use. Other limitations will also be exposure to sunlight; however, we do not predict this to be a problem during testing since we live in a sunny climate. The overarching issue of shading on solar panels is not within the scope of our project.

Economics:

A viable marketable implementation of the AC Solar Panel will result in human capital involved within the processes of manufacturing, assembly, distribution, and marketing. To extend beyond a prototype, the product will require financial capital in order to further develop the product to viability. Viability will require the product to be made to compete with existing solutions; this will require hiring additional engineers and supportive staff. The current team does not have the necessary capital to begin this project; venture capital or external financial support would need to be sought. The solar cells and the embedded electronics production consume natural resources and place strain on manufactured capital.

The product is not a complete system solution; the product is a small collection of solar cells capable of outputting alternating current directly. Additional costs accrue via additional devices to create a useful power system from the consumer; examples include additional panels, inverters, and converters. Benefits that the product creates are reduction in complexity, and lack of inverters per solar panel.

The project, as it stands, will not produce monetary profit. The beneficiaries of the project are university, and the public. A successful proof-of-concept can potentially lead to the development of a viable product. The project is not expected to accrue maintenance or operation costs. Current projections anticipate the project to exist for a minimum of one year.

Commercial Basis:

The project is a prototype; the device will not be sold per year. The estimated manufacturing cost for each device based on a preliminary cost analysis was $5000 including labor. A competing product which employs micro-inverters costs $450. Our estimate for material was $270. Thus, with comparable capacity to a large-scale manufacture, the estimated profit per panel is potentially $180. If the product were viable, the typical user would be a homeowner. American homes typically require an average of 28 solar panels to achieve full power capacity. Typical solar panel lifecycles are 25 years. Thus, the user is expected to pay approximately $13,000 over 25 years, assuming a loan or payment plan is used to pay for the panels. The table below is the estimated component cost per unit. The total is approximately $270.

Component	Estimated Cost per Unit
Solar Cell	$75.00
Tabbing Wire	$8.00
Bus Wire	$5.00
Flux Pen	$5.00
Encapsulation Kits	$30.00
Power Diode	$10.00
Aluminum Frame	$45.00
Resistors	$2.50
Capacitors	$5.00
Inductors	$25.00
Power Zener Diodes	$4.50
Power Diodes	$5.50
Bay Area Circuits Manufacturing	$30.00
Soldering Wire Spool	$7.00
Aluminum Plate	$10.00

Environmental

The environmental impacts associated with the product stem from the components and the printed circuit board and enclosure manufacturing processes. Semiconductor devices often use heavy metal elements that are environmentally harmful if not disposed of properly. The metals must be mined and this can impact the ecosystem of living organisms that live in the area of the mine. Mining also increases externalities of human activity such as higher greenhouse gas emissions. The product will require the manufacture of printed circuit boards. This process will use hydrocarbons and directly contribute to greenhouse gas emissions; there are other potential hazardous fumes released during the process. A clean, sustainable manufacturer should be chosen instead of the lowest bidder.

Manufacturability

Possible issues with manufacturing the device come from competition in sourcing components. More and more manufacturers are entering the solar panel market and thus there will be increased competition in obtaining the necessary power diodes, and manufacturing capacity. Scarcity of these necessary production levels may lead to an increase in cost. Suppliers may not have the necessary components available and this can result in a high lead time to source critical components. This could potentially range anywhere from a few weeks to a few months.

Sustainability

Aside from manufacturing, the product's only input should be direct sunlight. Maintenance required for the panels should be limited to dust removal and the occasional visual check for any possible weather damage. The design should be such that the product is self-sustaining in normal operating conditions, free from damage from external factors. Upgrades to the design will include increased compatibility to industry standards and higher efficiency in power conversion. These upgrades are engineering challenges but should otherwise be achievable.

Ethics

One large concern is the use of this project for personal or monetary reasons. Since this is a rather uncharted area, it is tempting to try and create a patent from the outcome of the project. However, this project was requested by Manhattan2, which is a non-profit R&D organization (IEEE code of ethics #2). Another concern is dishonesty when stating claims or estimates from data (IEEE code of ethics #3). Since this is among the first AC solar panels, it is definitely tempting to try and overstate the data, or to make the project sound better than it actually is.

Health and Safety

Health and safety concerns arise with the manufacture of the product. Although the project will be limited such that no high voltage or high current is outputted or produced, accidents are still possible. The design should be done as if high voltage and high current were present anyway; this will minimize the chance of accidental damage during manufacturing and testing. A market viable product will realize high voltage of 120VRMS, and thus the product will need to conform to power safety regulations before it can be installed in any customer's home or application.