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Conducted and Radiated EMI Measurements of Parallel Buck Converters Under Varying Spread Spectrum Parameters

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Table of Contents

List of Figures

List of Tables

Acknowledgments

Thank you to our senior project advisor, Dr. Taufik, for promoting this project research idea and supporting the SSFM team throughout the entire year. We ran into a major barrier this quarter due to COVID-19 which led to the Cal Poly campus shutdown. Although this senior project was meant to be very hardware dependent, Dr. Taufik met with us and helped direct our project in a new way such that we could complete an analysis using purely simulation. His expertise and willingness to assist both contributed to the overall success of this project. We will most definitely take the well-rounded skills we learned from this project and our undergraduate years at Cal Poly and the Electrical Engineering Department with us as we move into the working industry. We would also like to express our appreciation to our families for their support throughout our time at Cal Poly, and for allowing us the opportunity to learn at one of the most respected engineering institutions in the nation.

Abstract

The Conducted and Radiated EMI Measurements with Parallel Buck Converters Under Varying Spread Spectrum Parameters research senior project aims to explore the effects from Spread Spectrum Frequency Modulation (SSFM) on the input electromagnetic interference (EMI) or noise of a switching power supply, specifically with LM53601MAEVM hardware. The input EMI is important as the main input bus needs to be clean to provide a reliable source for other sensitive devices connected to it. SSFM can replace a conventional EMI filter and save weight, space, and cost. This project provides a basis in terms of the impacts of variable SSFM in simulation in order to provide an idea for its best application in future hardware implementations. The input voltage requirement for the buck converter is from 5V to 42V with output voltage of 3.6V and maximum output current of 1A. The buck converter should vary the percent modulation of the SSFM for up to +/-4%. Auxiliary circuits that will produce the necessary control signals for varying the percent modulation of SSFM were developed. Simulating LM53601MAEVM hardware with SSFM was not efficient as it required a significant amount of time and computational power. Overall, in terms of EMI, none of the simulations passed automotive CISPR standards, which is one of the potential LM53601 applications. The best results in simulation were at lower input voltages, mid-range loads, and low percentage of SSFM spread. Since EMI depends on layout, physical hardware measurements could provide further insight into the impact of variable SSFM.

Chapter 1: Introduction

Every circuit needs some sort of power or energy source in order to operate. In most cases, such power either comes from an external power source (e.g. wall outlet) or a built-in energy storage unit (e.g. portable battery). That said, not every electronic/application can take the exact supply ratings from the available sources. One scenario could be that only a $12V_{DC}$ battery source is available to power a circuit that can only handle four or six volts DC on the input. Another scenario could be that an electronic device requires multiple voltage levels to operate. For instance, a $5V_{DC}$ powered device needs $3V_{DC}$, $1.8V_{DC}$, and $1.5V_{DC}$ to fully operate. In terms of numerical voltage or current conversion, an easy fix can be to simply implement a voltage divider using two resistors. However, this will pose issues in application: power loss for high supply ratings and longer operation times. In fact, the efficiency of the voltage divider circuit when used as a power supply is the exactly the ratio of output voltage to the input voltage. This implies that the efficiency goes down as the difference between input and output voltages is bigger. A 5V source supplying power to a load at 4V, for example, will give 80% efficiency. If the power supplied by the source is 10W then the power loss in the circuit is 20% of 10W or 2W. However, the picture can easily get worse when the load is operating at let say 1V and the same 10W. This now yields circuit's efficiency of 20% which consequently forces power loss of 80% or 8W. The significant drawback of the voltage divider due to power loss in real world would translate to the cost as well as overall size of the circuit associated with getting rid of the heat from the power loss. Another major technical issue with voltage divider has to do with loading the circuit. Another major drawback for voltage divider is its inability to provide an output

voltage that is higher than its input voltage. Therefore, a different method has to be utilized if the 5V input source in the previous example must supply power to a 12V load.

In the case of using wall outlets as the energy source, there is a need to convert the supply AC voltage into some DC voltage that most electronics can take. The vice versa applies for solar panels — the need to take a solar panel generated DC voltage and convert it into usable AC electricity to power a home. The AC voltage might also need to be converted to a different level of AC based on the applications using it. All these examples show the point where power electronics come into the picture. Power electronics is an enabling technology that allows us to take any available power and convert it efficiently into a form that the load requires. Nominal voltage conversion within the same type of power (AC or DC) can also be completed by stepping up or down the input power. Voltage and current type conversion can be done in one of four ways: DC to AC, AC to AC, AC to DC, or DC to DC [1]. In general, depending on the application, power electronic circuits can be tuned to provide specific output voltage, output current, or output frequency [1]. Due to the high demand for power conversion technology, power electronics can be found in sub-fields such as systems and controls, power and energy, and electronics and devices. In everyday items, power electronics can be found in household appliances, air conditioners, electric vehicles, laptops, cell phones, chargers, TVs, speakers, and much more. There are many of these items in existence and many more being produced each day, which both show the importance and breadth of power electronics.

As mentioned previously, there are four categories of electric power converters. The DC to AC power conversion would require a power circuit called an inverter. There are switched-mode square and modified square wave inverters available in half and full bridge topologies, as well as pulse-width modulated (PWM) bipolar, unipolar, and high-low unipolar inverters. Both

serve the same general purpose but do the conversion differently. Switch mode inverters alternate the polarity of the DC signal to provide the AC signal. PWM inverters have a reference signal that dictates output frequency in addition to the carrier signal which regulates switching frequency.

AC to DC conversion uses one of three types of rectifiers: uncontrolled, semi-controlled, and controlled rectifiers. Uncontrolled rectifiers convert single or three phase AC voltage to a fixed DC voltage using diodes. Controlled rectifiers convert single or three phase AC voltage to a variable DC voltage using thyristors. Finally, semi-controlled rectifiers use a combination of diodes and thyristors. All three types can be configured in either mid-point or bridge topologies, depending on the desired DC output.

AC to AC conversion uses AC voltage controllers and cycloconverters. AC voltage controllers typically use integral cycle control, which is on-off control, or phase control to change the AC voltage on the output. With this method, only the AC voltage level can be converted. Cycloconverters, on the other hand, can change both the voltage and the frequency but it requires very complex circuitry and it is only used for large power applications. A very common AC to AC conversion consists of two stages: AC to DC or rectifier stage, and then DC to AC or inverter stage in which voltage level and frequency can be adjusted.

DC to DC converters include resistive voltage dividers, linear regulators, and switching regulators. As mentioned previously, resistive voltage dividers contribute to significant power loss when dealing with higher power; and thus, they are not usually used for power supply. Linear regulators use some type of a controllable device to decrease or increase the amount of current delivered to the load to produce the desired voltage. Like voltage divider, they have a high efficiency only when the output is close to the input. This is the reason why they are being

used only in very low power applications. Higher overall efficiency can be achieved using switching mode DC-DC converters. However, switching DC-DC converters suffer from inherent noise both at its input and output stages. Switching DC-DC converters are categorized into isolated and non-isolated topologies. Isolated topologies make use of a transformer in between the input and output stages. Their basic topologies include the push-pull, forward, and flyback configurations. Basic non-isolated topologies include buck, boost, and buck-boost converters. Moreover, DC-DC converters also operate differently based on the switching technique used such as PWM, soft-switching, and zero-current and zero-voltage resonant switching topologies.

Each DC-DC converter topology has its advantages and disadvantages. The type of converter is chosen based on the level of power and input/output voltage needs of the specific application. Higher power often corresponds to larger sizes of components used in the circuits. Converter size, component selection, and build cost also need to be considered for the application, especially given marketing or cost limitations. Furthermore, different topologies produce different levels of signal quality and amounts of noise called electromagnetic interference (EMI) noise. This is important to know since some applications might need to match certain electromagnetic compatibility (EMC) standards; and hence, the necessity for choosing the proper topology. However, very often the choice of topologies is limited and so the other option is to find ways to minimize the EMI noise level generated by the DC-DC converter.

Chapter 2: Background

DC to DC converters are a major growing area in power electronics. Due to the switching nature of DC to DC converters, their efficiencies are relatively high. Although efficiency is the main focus of power electronics, the electromagnetic interference or EMI from the switching transitions of DC to DC converters need to be taken into consideration for practical implementations. Undesired noise not only affects efficiency but also the reliability due to potential interference with other surrounding systems. In many applications, multiple DC to DC converters are connected to the same main input DC bus among all the other devices in the system. A practical example of this is an electronic device that requires various voltage levels to fully operate the system from a single voltage battery system. Therefore, it is important to keep the DC to DC converters from corrupting the DC bus, because each connected converter will generate some noise that would contribute to the overall EMI of the DC bus. If EMI is not suppressed well enough for DC to DC converters, the DC bus EMI levels can potentially get large and significantly degrade the quality of the DC bus input which in turn affects the performance the entire DC system.

Noise in electronics can be measured and quantified in two ways: conducted and radiated EMI [2]. Conducted EMI is noise that gets created through current flow through circuit wires or copper traces. Furthermore, common mode (CM) and differential mode (DM) are the two types of conducted EMI [3]. Common mode is when the noise is superimposing on itself, while differential mode is when the noise is caused by its relative variation on different nodes. Radiated EMI, on the other hand, is noise that gets generated via induction and transmitted through air. In electromagnetism, electric and magnetic fields are induced when voltage or

current changes, respectively. These changes result in the intensity increase of EMI. However, when energy flow variation occurs, the frequency range of the electromagnetic fields change [4]. For example, the larger the energy flow variation, the larger the electromagnetic bandwidth will be, which causes the electromagnetic interference breadth to increase in turn as well. In electrical engineering terms, EMI originates from ripples at the switching frequency and sharp signal transitions, both of which have frequency content higher than the fundamental switching frequency [5]. Since this senior project focuses on reducing overall EMI on the input DC bus, conducted and radiated measurements will be made on the buck DC to DC converter because it introduces significant input EMI compared to other the basic non-isolated DC to DC converter topologies. Such high input EMI of the buck converter is due to the input signal feeding into a fully controllable switch at the front end of the buck converter. A good quality DC signal is constant, but the switch causes the input current to swing from zero to a positive value in a very short moment of time, producing a series of pulsating input current responsible for producing the EMI noise. Therefore, if the worst-case input EMI of the buck converter can be mitigated, then the methods used should prove effective.

The simplest and conventional way to help decrease the EMI is to use an input filter, which can be either passive or active. A capacitor in parallel with the input is the fundamental passive input filter. The capacitor, an energy storage device, helps the input supply the necessary energy demanded by buck converter during the fast switching transitions with less of an effect on the input voltage DC bus, consequently reducing ripple by smoothing out the waveform. Since the capacitor conducts the AC component of the signal, it needs to be large in value and ratings with low ESR to minimize the ripple, which increases its physical size and cost [6]. To reduce the requirements for the capacitor and catch the common mode conducted EMI that passes

through the capacitor, a common mode choke can be added on the line before the converter to provide a series impedance to the noise. It would keep the noise at the switching node and prevent it from reflecting to the input DC bus. From the perspective of the bus, the current changes would be slower, so there would be less demand on the supply. Also, the leakage inductance on the choke helps the capacitor with filtering the differential mode conducted EMI. However, the choke has a limited effect because at high frequencies it is shorted out by the capacitor. Furthermore, passive filters require more space because of the component sizes. A possible option for a smaller footprint is to use an active filter [3]. One example of an active filter creates and injects a signal to cancel out the noise from the ripple through the use of a R and C sensing feedback for the ripple and input current, an operational amplifier, and a current injector implemented with a transformer [3]. Since the feedback is based on the ripple, high frequency noise from transitions is not attenuated well. Another example is using a power semiconductor on the boundary between linear and saturation modes for the active filter [7]. The implementation includes voltage feedback to keep the semiconductor in the correct mode and current feedback into its base to control the input current as a type 2 proportional integral (PI) compensator. It functions as an LC filter, but the components required are significantly smaller. Overall, both passive and active input filters are more effective in reducing conducted EMI rather than radiated EMI.

Another way to reduce EMI on the input is to implement a multiphase buck converter configuration. An example of a simplified multiphase buck implementation is shown in Figure 2-1. Multiple phase buck converters all operate at the same frequency with one converter switch opening while another closes. This in turn will spread the current draw more evenly within a single switching period, thus reducing input current and voltage ripple [8]. In other words, EMI

will be reduced because the energy demand from the source will be less drastic due to minimized transitions as the buck converters will constantly need an input provided. Additionally, ripple reduction and increased effective ripple current in theory is proportional to the number of phases [9]. The multiphase buck converter operates on the concept that each buck converter operates at the same switching frequency but starts at different phases. A period in a switching cycle consists of 360°, so the difference in phases for each converter in parallel would be one cycle in degrees divided by the number of the converters used [10]. For example, if two buck converters are implemented in the multiphase configuration, then the phase difference between the two converters would be 360°/2 = 180°. The phase offset for each converter is set via each switching control signal for each of the power stage MOSFETs.

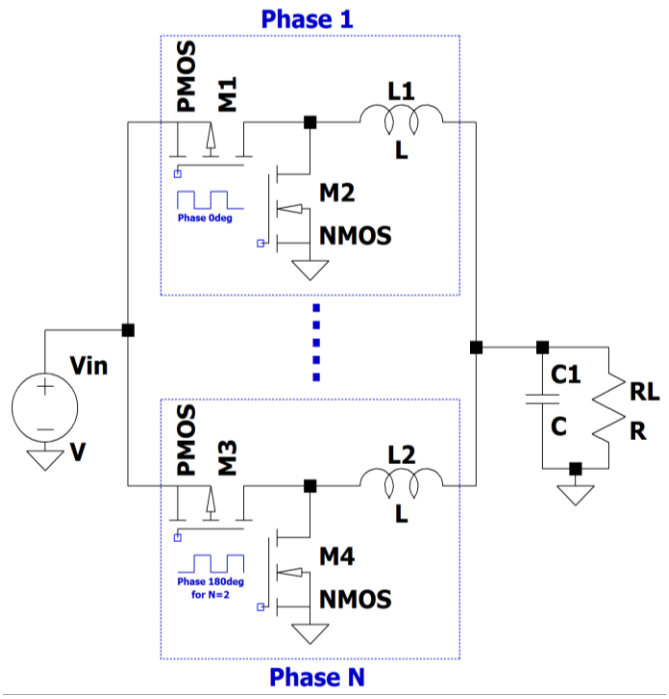

Figure 2-1. Basic Multiphase Buck Converter Configuration with Switching Waveforms Adapted from [11]

There are several different multiphase topologies, each having different benefits and tradeoffs. With the standard multiphase buck converter, transient response can be improved but at the cost of ripple cancellation, because a small inductance is required to have a large voltage step-down [12]. To obtain a fast-transient response and ripple reduction, the multiphase tapped-inductor buck converter can be used. The multiphase tapped-inductor topology is identical to a standard buck, except the output inductor is defined as the number of windings in series with the main switch divided by the number of windings in series with the low-side switch. However, the inductor coupled windings will have leakage and cause severe voltage spikes, thus introducing EMI. To address these spikes, an active clamping circuit can be applied to the tapped-inductor topology leading to the multiphase coupled buck converter topology. The clamping circuit consists of a capacitor MOSFET series connection between the main switch and low-side switch in an interleaving channel method so that the clamping capacitors can hold charge to compensate for any energy leakage [12]. The multiphase coupled buck converter topology can also be simplified into other versions to reduce the number of components.

Part of the multiphase exploration for this senior project will follow the 2018 Cal Poly SLO *Analysis of Improved Multiphase Buck Converter* senior project, which covers output voltage ripple improvement, efficiency, line and load regulation, and voltage regulator modules [10]. That project, however, goes into more advanced multiphase techniques with interleaving of the switching sequences, while this *Conducted and Radiated EMI Measurements of Parallel Buck Converters Under Varying Spread Spectrum Parameters* project will start with a more simple multiphase configuration to explore the combination with SSFM.

EMI can also be reduced through the type of switching signal used. Many ways exist to reduce the undesired characteristics of the switching that is causing the noise. First of all, the

transitions can be slowed down, which would reduce EMI, through soft-switching techniques [13]. This method is typically more effective for high frequencies. However, EMI reduction is not possible for some soft-switching topologies because of resonance characteristics and more components. Another, newer method is to spread the frequency spectrum of the pulse width modulated (PWM) signal driving the switch. A 2018 Cal Poly SLO senior project called *Spread Spectrum Buck Converter* utilized the LTC8609 to implement a buck converter with spread spectrum to minimize the EMI with successful results [14]. Then, the 2019 Summer Undergraduate Research Program (SURP) project, *Effectiveness of Spread Spectrum Frequency Modulation on Parallel Buck Converters*, measured and analyzed the conducted EMI from two bucks placed in parallel using the LM53601MAEVM. The noise characteristics, however, did not look as expected because of the way the noise floor was curved. Different types of implementations exist: adding randomness to the frequency of the PWM, frequency modulating the PWM, modulating the PWM with a randomness added to the carrier frequency, modulating the PWM based on a unpredictable but deterministic carrier signal (i.e. chaotic modulation), using hysteretic control by running the converter without an external switching signal, and using delta sigma modulation to move the noise spread to higher frequencies [15]. The latter types of spread spectrum frequency modulation (SSFM) add increased complexity, which is only valuable for some cases depending on how many control variables are desired. Adding more randomness to the modulation could also increase the output ripple, which might then need to be counteracted with feedback. In essence, all these spread spectrum technologies reduce EMI by limiting the amount of energy stored in a single band of frequencies for a significant length of time [16]. This method effectively dampens any high energy noise harmonics and creates a larger band of noise frequencies with substantially lower magnitudes, as shown in Figure 2-2.

This frequency band spectrum shape would depend mostly on the type of carrier signal used for the modulation [17]. Since the advanced techniques would be excessive for the study on EMI of variable SSFM as compared to the regular parallel buck topology, this project just focuses on frequency modulating the switching signal.

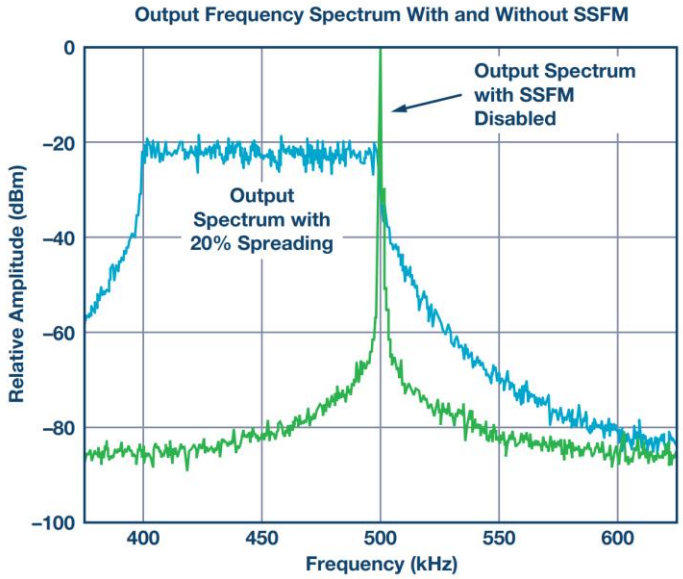

Figure 2-2. Output Frequency Spectrum Showing with and without SSFM [15]

Many techniques are developed to reduce the EMI of DC to DC converters to fit the specifications of the applications using these converters. One such application is the multimedia console in automotive vehicles. Many vehicles now feature on-board "computers" that can provide maps, different types of audio players, even software applications that are normally used on mobile devices. These multimedia centers can operate from a different voltage than what is supplied by the car, which can be provided by the DC to DC converter, but the EMI has the potential of interfering with surrounding systems. This means that the converter needs to satisfy certain electromagnetic standards if it is to be used for an application in a sensitive or

commercial system. The EMI standard for electromagnetic compatibility for automotive applications is under CISPR 25. The test to meet this standard measures the conducted noise from 150kHz to 108MHz in frequency bands relevant to AM, FM, and mobile service with the limits set by the peak, quasi-peak, and average values [18]. The limits ranging from 18dBµV to 70dBµV, corresponding to 7.94µV and 3.16mV, respectively, means that the noise tolerated is relatively low. For multimedia, the EN 55022/CISPR 22 and the newer CISPR 32/EN55032 standards are used. The measurement techniques are the same, but CISPR 25 has more specifications to meet, such as the wider range of frequencies. Compliance testing can be typically done with 5µH/50Ω artificial networks or 5µH/50Ω V-type line stabilization networks. The method chosen for measurement depends on the application and the desired accuracy of the measurement results.

Studying SSFM and multiphase effects could lead to new ways of reducing EMI. To explore those effects, the *Conducted and Radiated EMI Measurements of Parallel Buck Converters Under Varying Spread Spectrum Parameters* senior project will analyze the conducted and radiated EMI measurements without and with SSFM for the LM53601MAEVM, a synchronous buck converter evaluation board. The project will also look at the quality of the buck converters' input DC in terms of the EMI levels. Combinations of different bucks in parallel operating at different modulations could yield results with lower EMI. Since the *Effectiveness of Spread Spectrum Frequency Modulation on Parallel Buck Converters* SURP prompted further research to conclusively verify the results, measurements will be made under four testing situations to study the effectiveness on EMI reduction techniques: parallel buck converters with a regular output filter and no SSFM for a benchmark test, parallel buck converters with variable SSFM, a multiphase buck converter without variable SSFM, and a

multiphase buck converter with variable SSFM. Combinations of different bucks in parallel operating at different modulations could yield results with lower EMI. Since the synchronous buck converter evaluation board modules for this senior project use buck controllers with internal switches, there will not be a research emphasis on the circuit theory behind the generation of multiple phases. There will, however, be insight into the procedure for synchronizing each buck converter module to one another for multiphase and a study of the effects. The analysis for the noise would include preliminary testing for interference with FM radio as well as how useful SSFM or multiphase SSFM can be in reaching the automotive standards. Of the four testing situations, the standard capacitive output filter case and the SSFM only case will be compared to each other and a cost-benefit analysis will be performed in order to provide a reference for deciding which method to use. After gathering data on all four test setups, an analysis will be completed to determine the advantages and disadvantages of each configuration.

Chapter 3: Design Requirements

This project focuses on studying the effect of utilizing the Spread Spectrum Frequency Modulation (SSFM) technique with varying parameters on parallel Buck converters. In particular, this project will specifically investigate the impact on conducted and radiated electromagnetic interference (EMI). Therefore, this project entails measurements of mainly the electrical aspects of the parallel Buck converters, and the mechanical specifications as well as physical dimensions will not be relevant. These electrical aspects include power efficiency, degree of SSFM spread, input voltage range capability, input EMI reduction, and output power specifications.

Power Efficiency > 90%

Since one of the main objectives of power electronics is efficiency, it is important to keep the efficiency of the buck converters within the expected range for switching regulators [1]. Higher power efficiency helps save energy, lower heat dissipation, and reduce costs. SSFM and multiphase features that are added to the standard buck should not significantly degrade the overall efficiency.

SSFM Spread Variation = ± 4%

The SSFM spread is a controller limited function from the hardware used for this project, which is the LM53600MAEVM [19]. This project is taking advantage of using different SSFM modulation percentages within the maximum spread of ± 4% available for this specific controller. The project goal is to incorporate SSFM as one technique to reduce input EMI [16].

Input Voltage Range of 5V – 42V

The input voltage range capability is dictated by the LM53600MAEVM hardware used for this project [19]. By selecting an input capability of 5V to 42V, the buck converter configuration can be used in many step-down applications. Specifically, buck converters can be connected to a battery source rather than a generator (e.g. power supply or wall outlet), as in automotive applications. Since there are a variety of battery options with varying voltage levels, it is important that that buck converter configuration can operate under a large input range.

Input EMI Reduction > 40%

Reduced EMI is required to maintain low interference with other signals and surrounding systems. The input EMI can superimpose on itself when multiple devices are connected to the same input bus and corrupt the signal quality of that bus. Minimizing this effect is especially important when used in automotive radio/communication system applications, as any interference can impact the vehicle reliability [19]. For the case of the standard buck converter, input EMI needs the most reduction as the input waveform has the most amount of ripple due to the main switch turning on and off. A reduction of 40% is desired as the goal is for the buck converter configuration to eventually meet EMC standards governed by CISPR and IEC, which pertain to automotive and multimedia applications.

Maximum Output Power of 6W

The LM53600MAEVM hardware used for this project provides an average of 3V and a maximum of 1A on the output per buck converter, which corresponds to 3W each [5]. Since two buck converters will be implemented in parallel, the output power supply available adds to a

maximum of 6W possible, which is a standard amount of power needed for automotive radio and multimedia center applications.

Figure 3-1: SSFM Multiphase Buck Converter Level 0 Functional Block Diagram

The high-level functional block diagram of this project is depicted in Figure 3-1. The multiphase and SSFM features are chosen to be implemented with the intent to achieve input EMI reduction such that the converters do not require costly input filters. This configuration is designed to take an input voltage range of 5V to 42V, as well as phase and modulation control signals. The large input range is helpful for potential implementation for many applications. The modulation and phase control signals help tune SSFM spread and buck converter phase synchronization, respectively. The SSFM spread needs to be adjustable to study the effects of various spread percentage combinations on the input EMI. At the output, each converter can supply 3V and 1A for a total of 3W maximum per converter for the application powered by this system.

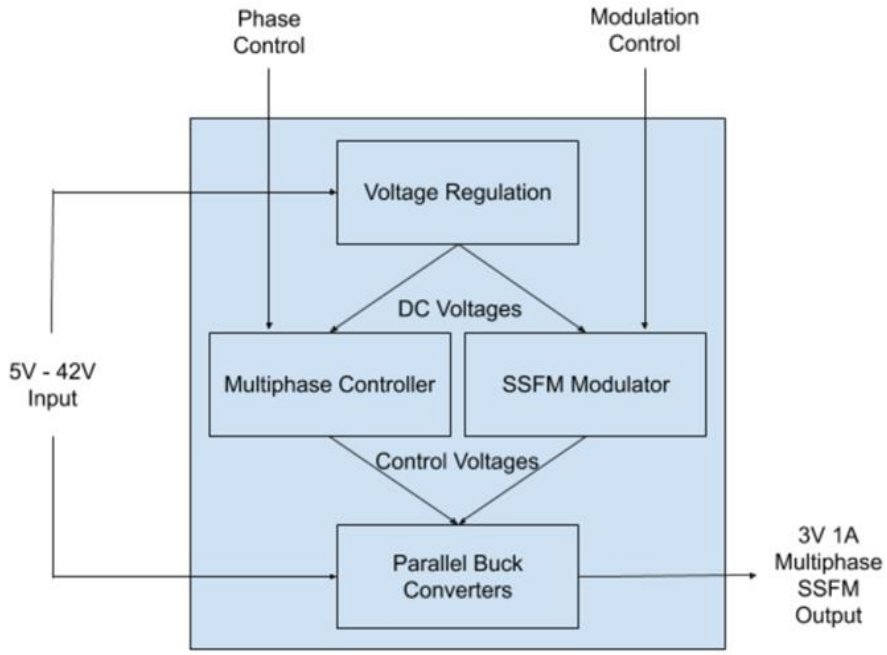

Figure 3-2: SSFM Multiphase Buck Converter Level 1 Functional Block Diagram

Figure 3-2 shows a more detailed functionality and system architecture of the SSFM buck converter configuration that will studied in this project. Since the modulator and phase controllers need to be powered by a fixed DC voltage, voltage regulation would be needed to provide that power from the variable input. The voltage regulation block takes in the input voltage range and outputs the needed power to supply the buck converters and SSFM modulation controllers in voltages and currents within their relative ratings. In addition, multiphase and SSFM modulation blocks need to be distinguished as they are separate circuits providing those distinct features. The multiphase controller takes in the phase control signal and provides the desired phase to the switching voltage signals for the buck converter configuration [8]. The multiphase voltage signal would, for example, be a PWM signal going into the gate of the switching MOSFET. The SSFM modulation controller takes in the modulation control signal with a spread of up to +/- 4% and outputs the control signals delivering the necessary voltage signal to the parallel buck converters to achieve the desired variable SSFM for each buck. The

buck converters are connected in parallel, and at least two are needed in order to incorporate multiphase capabilities. They take in the input voltage ranging from 5V to 42V, the multiphase control voltage signal, the SSFM control voltage signal, and provide the 3W output per buck. Their function is to step-down the input voltage to the desired output voltage while incorporating the additional multiphase and SSFM features to improve input EMI while preserving the general efficiency. The level 2 functional decomposition with the detailed component level design is not necessary at this point because the evaluation board used for this project is already provided.

Table 3-1: SSFM Multi-Phase Buck Converter Requirements and Specifications

Required Specification	**Value**
Power Efficiency	> 90%
SSFM Spread Variation	± 4%
Power and output	Supply total 6W of power (3W each converter x 2 converters with 3V output and 1A output max)
Buck Converter Input Voltage Range	5V - 42V
Input EMI Level Reduction	By up to 40%

Overall, Table 3-1 shows a summary of the technical specifications used for this project. As an outcome of this project, results of the measurements from this project will hopefully provide some guidelines on utilizing SSFM for parallel buck converters to reduce EMI noise. The goal is to find a combination of SSFM and multiphase that will effectively reduce input EMI noise.

Chapter 4: Design

Due to COVID-19 and the consequent shutdown of the Cal Poly campus starting March 25th, 2020, along with Cal Poly University and Electrical Engineering Department policies, this senior project will not discuss any hardware testing because of the inability to access necessary equipment to conduct such tests. With the new change, this chapter will now cover the process of coming up with a simulation design that best emulates the LM53601-MAEVM evaluation board that was intended for analyzing conducted and radiated EMI measurements in hardware.

Before developing a solid simulation model, simultaneous analyses were conducted between two spice simulation design software: Cadence Allegro PSpice Designer and LTspice. The objective was to determine if both pieces of software could successfully simulate the required design framework and to determine which of the two software would perform better in terms of ease of use, simulation quality, and simulation time. For Cadence's PSpice software, the benefit would be its greater capability and potential in terms of quicker runtimes and access to additional complex features. For LTspice, however, the benefit would be the ease of access. LTspice is free to download, whereas Cadence Allegro PSpice Designer requires a rather expensive license to use the software. For the purposes of this senior project, software access was given with the procedure of needing to remote desktop connect into a Cal Poly campus lab computer using a Cal Poly VPN provider. Answers and tutorials can be found online on software use assistance, so this was not considered in the comparison. For both simulations, the LM53601 model does not include the automatic SSFM operation internal to the converter. Only a basic PWM option is available internally in the model. Therefore, in simulation, the SSFM would need

to be provided exclusively with an external signal. The paragraphs below detail the simulation differences between the two pieces of software.

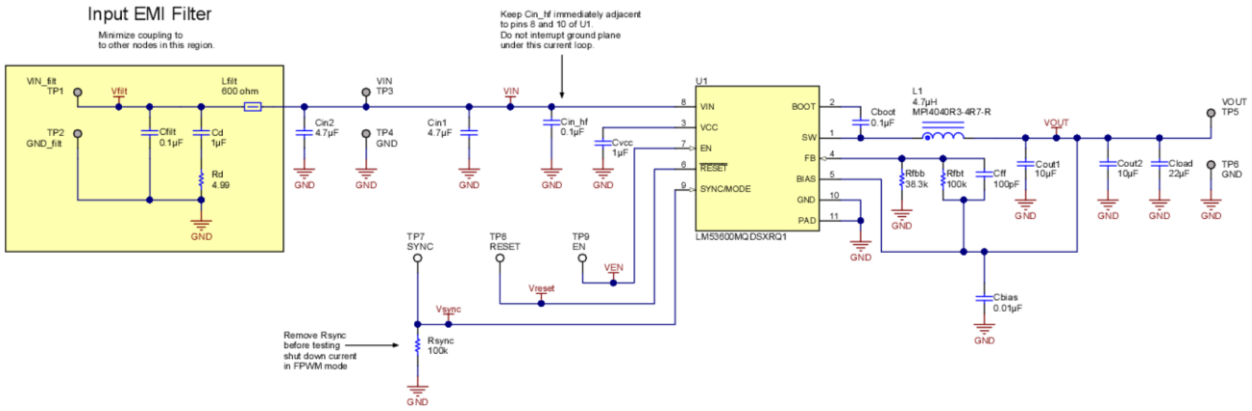

Figure 4-1: Schematic of LM53601-MAEVM Provided by Texas Instruments [20]

Using Cadence Allegro PSpice Designer, a design attempt was made to simulate the evaluation board circuit by the Texas Instruments as shown in Figure 4-1. The Cadence circuit schematic is shown in Figure 4-2. To utilize simulation ideality, all four output capacitances shown in Figure 4 were combined in parallel. In addition, the input is an ideal DC voltage source which means input capacitances were not necessary to include. The automotive SSFM capable buck converter chip also has three select signals: Enable, !Reset, and Sync/Mode. At this point, the objective was to successfully simulate a working evaluation board regardless of which operating mode. This design was thus configured to switch at the internal clock frequency of 2.1MHz in forced pulse width modulation (FPWM) mode by tying Sync/Mode and Enable pins to the input and !Reset to the output [21]. With the completed schematic as described, the simulation attempted to run but faced convergence issues. To address this issue, the simulation profile was adjusted using two methods. The first method was to directly use PSpice's auto

convergence function. Working in a similar manner, the second method was to manually reduce the relative and absolute voltage and current tolerances: RELTOL, ABSTOL, VNTOL, and GMIN [22]. Specifically, RELTOL was reduced from 0.001 to 0.01, ABSTOL from 1e-12 to 1e-09, VNTOL from 1e-6 to 1e-3, and GMIN from 1e-12 to 1e-09. Despite both methods to reduce runtime issues, simulations still took a minimum of 20-30 minutes to complete.

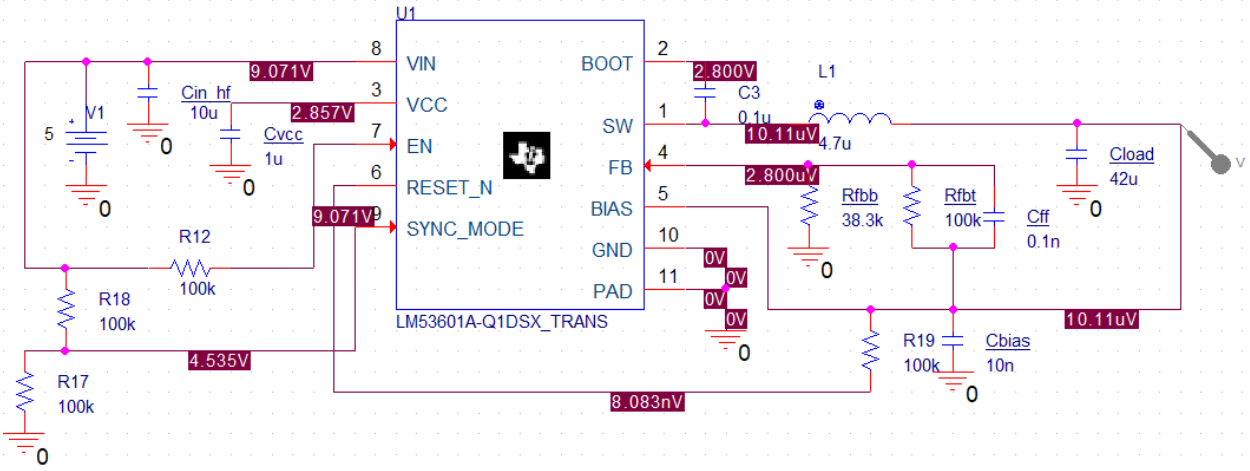

Figure 4-2: Schematic of LM53601-MAEVM in FPWM Mode Using Cadence PSpice

Regardless of runtime speeds, the simulations conducted using Cadence proved unsuccessful. At best, the input signals Vin, Vcc, Enable, and Sync/Mode were outputting their designated voltage levels. It is important to note that the fully working input for this design did not make use of the input EMI filter shown in the LM53601 User Guide. This is because the EMI filter contains a 600Ω ferrite bead tied to the output; the ferrite bead was not available on the list of components nor was it easily understood how to import a model of one with the correct specifications. The output, however, was reading around 10µV with the !Reset pin reading 8 nV as shown in Figure 4-2. As previously mentioned, the !Reset pin is the only one of the three select signals that when high is tied to the output, unlike both Enable and Sync/Mode that are

tied to the input when they are in high state. Furthermore, the LM53601 datasheet describes that a low output on !Reset indicates a regulator fault [21]. Why !Reset and the output are both low may have caused the other to fail are unanswered questions.

LTSpice was investigated as the other simulation software to be used for testing the effects of variable SSFM on input EMI. A major benefit of the LTSpice software is that it is readily available and does not require special remote access. The simulation is targeted at examining the behavior of the available LM53601-MAEVM hardware. The schematic was constructed as per LM53601-MAEVM schematic, shown in Figure 4-1. However, the simulation ran into significant convergence issues with simulation time getting stuck in the fs/sec. The first approach to improve the situation with the convergence issues in the simulation calculations was to merge the output capacitors into one. When connected in parallel, the total capacitance is 42µF. Another change was to adjust the simulation options, which meant decreasing the accuracy and precision of the simulation to achieve convergence in a realistic time. The options changed consist of gmin, abstol, reltol, and trtol. Gmin is the conductance added to semiconductor junctions to help the calculation converge faster with a default of 1e-12; abstol is the absolute current error tolerance with a default of 1pA; reltol is the relative error tolerance with a default of 0.001; and trtol is the transient error tolerance given by the overestimation factor for truncation errors with a default of 1 [23]. Changing the options to gmin=1e-10, abstol=1e-10, reltol=0.003, trtol=7 improved the simulation time and results were obtained in hours, but only for open circuit conditions. However, this simulation time was still not realistic for the many other circuit conditions especially with limited computers to carry out the simulations. In contrast though, simulating with the input filter and no load only took several

minutes. Nevertheless, simulation without the input filter is needed to fully analyze the operation and EMI characteristics of the buck with SSFM.

Furthermore, when the load was added the simulation ran into significant convergence issues again. The next step was to reduce the transients happening in the simulation, especially since the project focuses on steady-state analysis. The input voltage is seen as a step from 0V in the beginning of the simulations. Sharp transients take longer to calculate. Therefore, the input voltage was ramped up more slowly. This change, along with further decrease of the accuracy with another increase in the options to gmin=1e-8, abstol=1e-8, reltol=0.003, trtol=7, yielded simulation results with the load in about an hour. This timing was more reasonable and provided expected waveforms as a result.

Another way to slightly improve the time the simulation takes is to only start saving the data when steady state occurs, which constitutes the time of interest [24]. This was achieved by setting the .tran command followed by the step size, the stop time, and the time to start saving waveform data. The step size is determined based on the frequency of the converter, which is set to 2.1MHz on default, in order to be small enough to capture all the necessary information; it is about a couple orders of magnitude less than the period of the switching. In addition, the .save command can be used to specify the particular nodes for which the data is to be saved. These two changes did not contribute to much improvement, so their inclusion is not essential, but can be helpful. Since the simulations involving SSFM would be without the input filter connected, the input capacitors can be decreased and even removed because the input voltage is ideal. This change also does not improve the simulation time significantly, but it does simplify the circuit. At this point, the simulations took slightly under an hour to run.

Once the simulation time was reasonable, the operation of the buck converter and the controller simulation model were verified. The pins, as mentioned in the PSpice description, configuring the converter controls were set. First, the enable pulled up to input voltage, active-low reset pulled up to a steady 3.6V corresponding to the desired output, and the sync/mode pin pulled down to verify converter was then verified with the internal frequency of 2.1MHz [20]. The run was successful. Next, the FPWM, requiring an external signal to be applied to the sync/mode pin, was also successfully verified. This is the desired mode of operation. The set-up for this mode has the sync/mode pin pulled up to the input voltage. A signal in the same frequency range as before was used to test.

For the external signal to be frequency modulated for the SSFM operation, LTSpice has two options to consider. One simpler way could be using the single-frequency frequency modulation source and setting the needed modulation index, carrier, information signal, and voltage [23]. Another way would be to use the VCO-based FM-AM generator. The AM pin would be disconnected, while the FM pin would accept the information signal. The “mark” parameter corresponds to the highs of a signal and is used to specify the higher frequency and “space” is used for the lower one. However, this method is more of a frequency shift key modulation, rather than a classic FM. Both methods seem to have sinusoidal carriers that cannot be changed to a different type of waveform. Therefore, to change the carrier from a sinusoid to a triangular wave in the simulation, which could provide better results as mentioned in Chapter 2, a signal conditioning circuit would be needed. Ideal components would be used for the signal conditioning since it is only for simulation purposes. In practical implementation, however, the carrier can be set to a triangular waveform. This method was chosen as adding another chip in order to get the necessary SSFM would increase the simulation time which is already very slow.

After debugging and changes, the final decision was to use LTspice as the simulation software for this senior project. As previously explained, the simulations in LTSpice finally converged and were able to provide results. Final schematic selected for further use is shown in Figure 4-3.

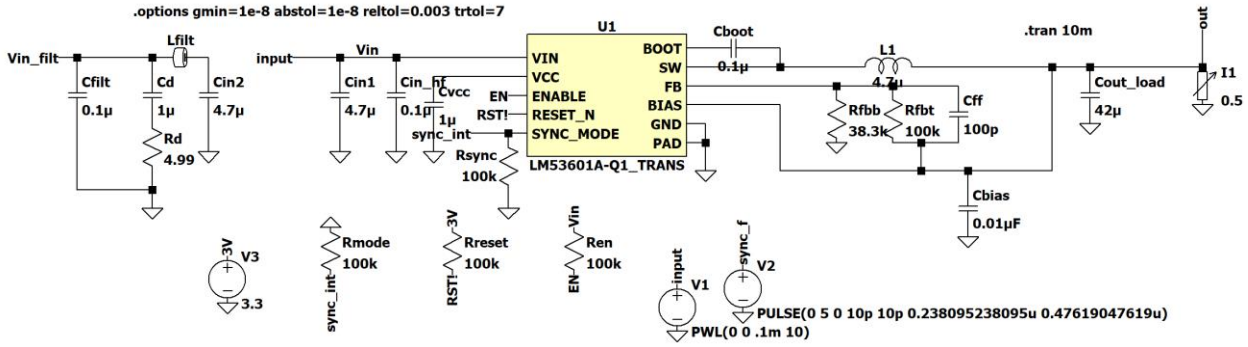

Figure 4-3: Schematic of LM53601-MAEVM in Auto Mode Using LTspice

With a working LTspice simulation set to switch at the internal clock frequency in auto mode, changes to the inductor, the output capacitance, and input voltage were separately made to further analyze the capability of the LM53601A buck converter. From the working version shown in Figure 4-3, an attempt was made to reduce the output capacitance from its combined 42µF in half twice. The goal here was to observe the simulation while monitoring the amount of output ripple increase. The three simulation runs confirmed the increase in output voltage ripple as output capacitance decreases. The output ripple was 933µV at worst case with the original output capacitance. With this in mind, an output ripple of less than 1% is desired with the decrease in capacitance for simulation time improvement. While at ¼ reduction, with a 10µF output capacitance, the ripple was 3.8mV at worst case, corresponding to 0.1%. Besides the ripple, slight oscillation due to the control loop was also observed. This could also be attributed

to stopping the simulations with less than 1ms of steady-state data due to their long run times. Further decreases of output capacitance were not explored as the datasheet suggests not to decrease the output capacitance below 20µF in order to meet load transient requirements [21].

A trial was also done to lower the inductance value in order to determine when the converter will reach boundary and discontinuous conduction modes. This information mainly shows how much the current can be changed while still keeping the converter in continuous conduction mode operation. In doing so, simulation shows that reducing the inductance to 1.2µH will cause the inductor current to reach boundary and further discontinuous conduction modes. Theoretically, this value can be checked from calculating the critical inductance, which is the inductance giving the boundary condition [1]. The maximum input of 42V should be used as it gives the worst-case scenario. The change in inductor current Δi_L, measured in the simulation, is about 0.4A. Since the output voltage is known to be 3.6V, and the switching frequency is 2.1MHz, all the variables are available to calculate the critical inductance:

$$L_c = \frac{(V_{in} - V_{out}) * (V_{out}/V_{in})}{\Delta i_L * f_{sw}} = \frac{(42V - 3.6V) * (3.6V/42V)}{0.4A * 2.1MHz} \approx 4\mu H \quad (4\text{-}1)$$

There is a definite discrepancy in the measured and calculated values, which can be attributed to the added non-idealities of the converter in the simulation. The inductance used in the simulation is 4.7µH, which should be sufficient as shown by theory and simulation. That said, it is also important to note that the LM53601 datasheet specifies that an inductance between 4-10µH should be used to allow the current mode compensator to be stable [21].

With the information about how much certain parameters can be changed to improve the simulation while not degrading the overall converter operation, tests of varying SSFM in a buck

can be successfully carried out in LTSpice. The simulation would provide an insight into the hardware tests and measurements in a follow up project at a later time when the COVID pandemic conditions improve.

Chapter 5: Simulation Results and Analysis

The final schematic selected was adapted for use in simulation. The simplifications and options discussed in Chapter 4 were applied to have a reasonable simulation time. The input filter was not used to simplify the schematic and just explore the differences between no SSFM and varying SSFM. The schematic for no SSFM is shown in Figure 5-1. A step size of 0.03µs was chosen to have enough points for the fastest switching signal of 2.1MHz in this case.

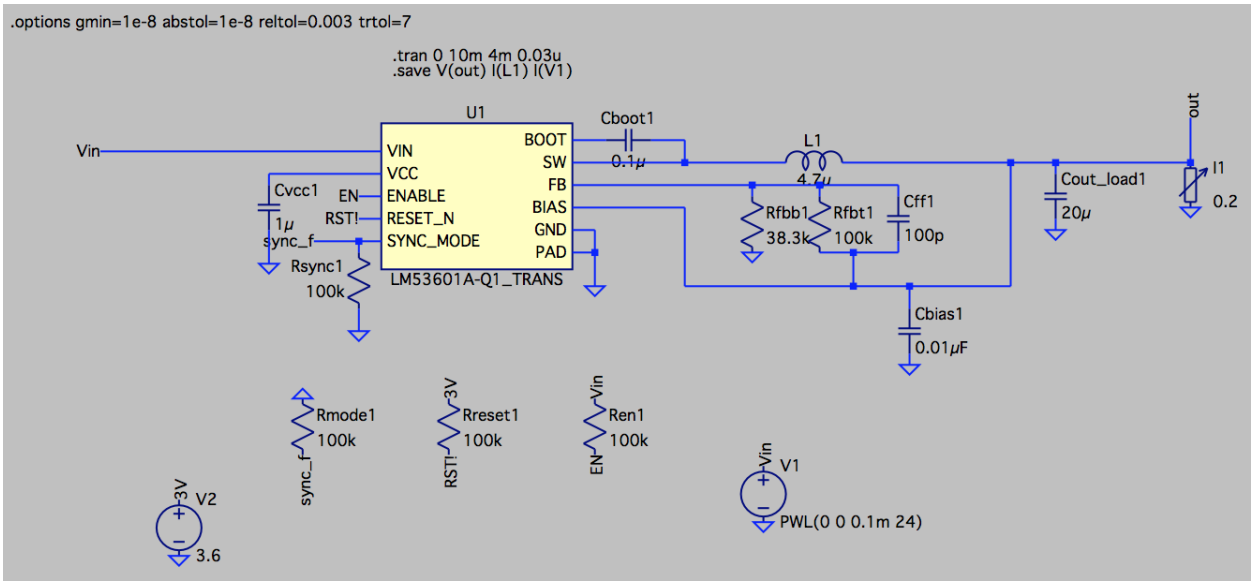

Figure 5-1: LM53601MAEVM Schematic for Simulations with no SSFM

The schematic for testing with SSFM is shown in Figure 5-2. The step size needed to be decreased to 0.001µs to accommodate the faster signals around 100MHz and not miss the required information. The FM modulator was chosen as a square wave representing the PWM could be specified as the message signal. However, the output Q of the modulator has a swing of

-1V to 1V regardless of the input. Therefore, it needed to be shifted up to swing between the voltage the SYNC/MODE pin is pulled-up and ground, to be within the pin's specifications for FPWM [21]. Thus, the voltage-controlled voltage source E1 was used to adjust the swing by introducing the necessary offset and gain.

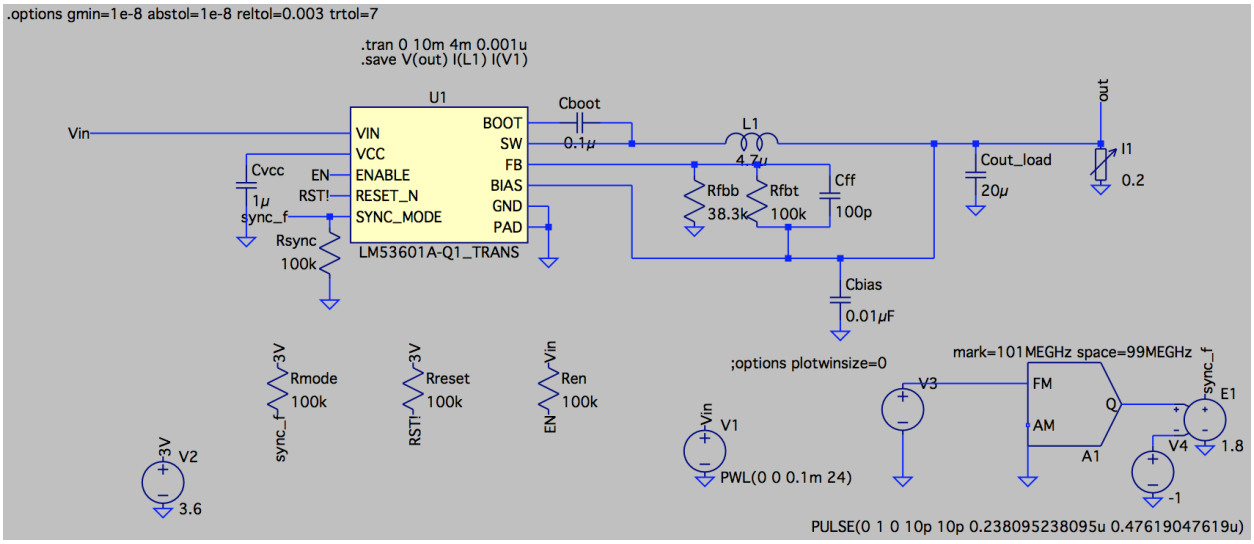

Figure 5-2: LM53601MAEVM Schematic for Simulations with SSFM

To simulate all the cases, the input voltage V1 was changed between 12V and 24V, the percent of SSFM spread was changed between ±1% which corresponds to 101MHz mark and 99MHz space and ±4% which corresponds to 104MHz mark and 96MHz space, and the load I1 was changed between 0.2A to 1A in 0.2A steps with each input voltage and spread percentage.

As previously mentioned, the completed simulations consist of 30 different test cases. One third of these cases are tested without spread spectrum frequency modulation; the other two thirds are tested with SSFM. Hence, the fundamental evaluation board circuit design was configured into two different modes: auto mode and forced pulse width modulation (FPWM) mode, respectively, to test without and with SSFM. This is because the LM53601 can override

and disable built-in spread spectrum if either an external clock is applied to the chip or if the chip is configured into auto mode specifically for this simulation model [21]. To test with SSFM, an external signal is applied to the SYNC/MODE pin of the chip such that the signal voltage is above its threshold of 1.5V [21]. The reason for not using internal spread spectrum for these simulations is because Texas Instruments does not provide a simulation model file for a chip with the internal SSFM capability. Figure 5-1 depicts the circuit configuration for buck converter testing without SSFM. To configure the chip in auto mode, R_{MODE} is tied to ground and no external clock signal is applied to the SYNC/MODE pin.

Figure 5-2 depicts the circuit configuration for buck converter testing with SSFM. To configure the chip in FPWM mode, R_{MODE} is tied high to a 3.6V source and an external clock signal is applied to the SYNC/MODE pin. The reason for choosing the 3.6V source rather than the input voltage as stated in the LM53601MAEVM User Guide is because the steady DC source was already made available for simulation purposes [20]; the source is one that can be used to provide SYNC/MODE with a valid synchronization signal level above the minimum threshold. In addition, the SYNC/MODE pin also sees an external clock from the output of the voltage dependent source given the FSK modulated 2.1MHz internal clock switching frequency as mentioned earlier in this chapter.

When simulating with SSFM, the maximum step size had to be reduced to an extremely small value to accommodate for the high modulation frequency and obtain enough data samples per period. As previously discussed, the internal 2.1MHz switching frequency was modulated in the FM range up to ±4% spread with a center frequency of 100MHz. Accounting for the shortest period scenario of 9.6ns (1/104MHz), the maximum step size for all SSFM simulations were set to 1ns which allows a minimum collection of nine samples per period. Since the internal clock

frequency is running at 2.1MHz or approximately 0.5µs per period, there also needs to be a long enough simulation time to capture sufficient data. Hence, the final simulation parameters were set to ".tran 0 10m 4m 1n". Although this means only the 6ms of steady state data will be saved, there will be six million (6ms/1ns) data points calculated and recorded per node and component. In other words, the SSFM simulations will take an extremely long time to run. To expedite the process, a couple more simulation parameters were altered. First, a ".save" operating command was added to only calculate and save the data for output voltage, inductor current, and input voltage current. In addition, the LTspice control panel parameter Engine solver was changed from "normal" to "alternate". If applicable, depending on the version of LTspice, the thread priority could also be changed from "medium" to "high". The simulation also reduced the preciseness of absolute and relative voltage and current tolerances to increase simulation speed as mentioned in the previous chapter. Note that even with these adjustments, SSFM simulations still took upwards of three hours to complete.

Figures 5-3, 5-4, and 5-5 respectively show the output voltage, inductor current, and input current switching starting at 4.5ms for a 12V input, 60% load, and no SSFM case. Figure 5-3 shows a small dip on the output voltage at 4.506ms, but the overall range swings around 3mV to show an average voltage of 3.61V. The 3.61V output voltage is dictated by the adjustable output voltage divider configured for this senior project and as specified by Texas Instruments. Figure 5-4 shows the inductor current operating in CCM with a peak to peak current of approximately 300mA from 450mA to 750mA. Figure 5-5 shows the input current switching signal as seen from the input voltage source. Since the chip is running on auto mode and using its internal clock frequency, the main switch should be operating at 2.1MHz. Figure 5-5 verifies this as four periods can be seen per two microsecond increments. Note that the input current spikes

going above the peak current and below 0A are not attributed to the actual performance but rather simulation. Further discussion on this will be done later in the chapter.

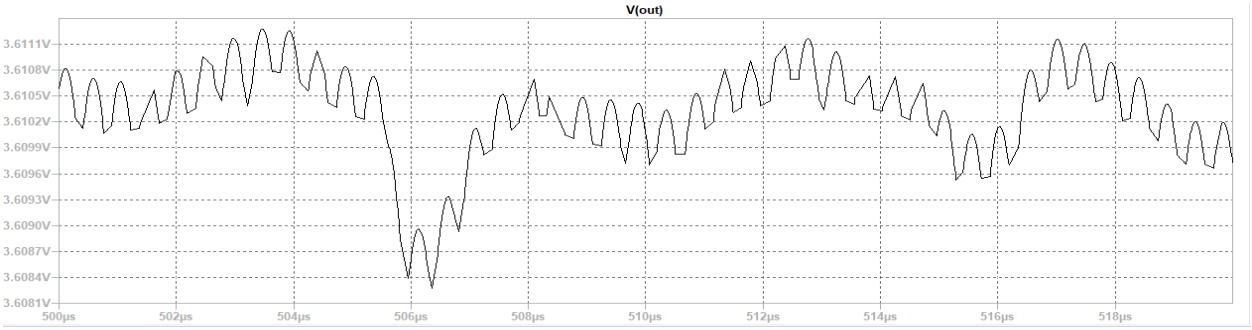

Figure 5-3: V_o from 4.5ms to 4.52ms (S-S) for 12V input at 60% Load with no SSFM

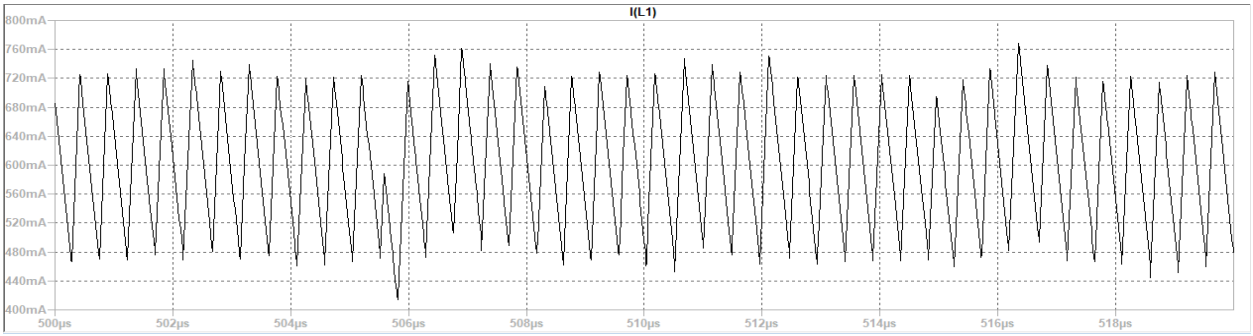

Figure 5-4: $I_L = I_o$ from 4.5ms to 4.52ms (S-S) for 12V input at 60% Load with no SSFM

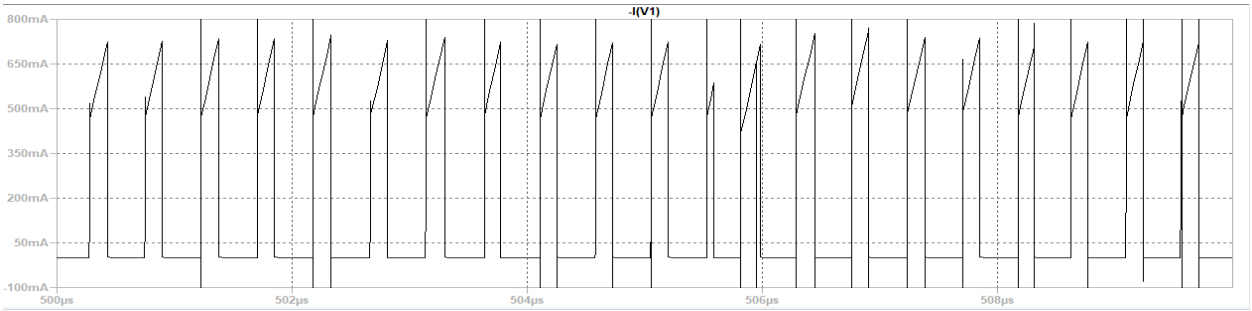

Figure 5-5: I_{IN} from 4.5ms to 4.51ms (S-S) for 12V input at 60% Load with no SSFM

Figures 5-6, 5-7, and 5-8 respectively show the output voltage, inductor current, and input current switching starting at 4.5ms for a 12V input, 60% load, and with ±4% SSFM. Figure

5-6 shows a small dip on the output voltage at 4.519ms, but the overall swing is less than no SSFM by 1mV. Figure 5-7 shows the inductor current operating in CCM with a peak to peak current of approximately 300mA from 450mA to 750mA. This current waveform is nearly identical to the case without SSFM in Figure 5-4. Figure 5-8 shows the input current switching signal as seen from the input voltage source. Like Figure 5-5, Figure 5-8 shows four periods per two microsecond increments. Although Figure 5-8 is shown in a 20µs window instead of a 10µs window, it can be observed that the input switching with SSFM looks cleaner than that without SSFM. Overall, however, the time domain plots between SSFM and no SSFM are very similar in terms of shape. Regardless of SSFM or no SSFM, a difference can be spotted depending on the percent load. The higher the percent load, the larger the peak current value.

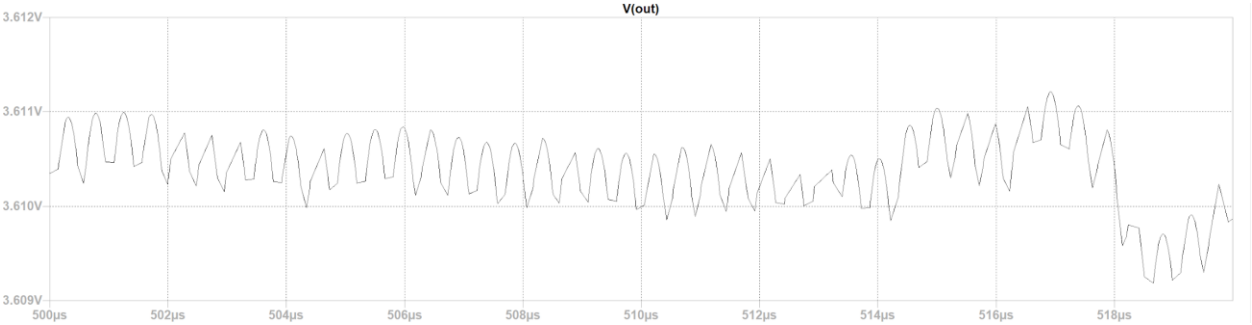

Figure 5-6: V_o from 4.5ms to 4.52ms (S-S) for 12V input at 60% Load with ±4% SSFM

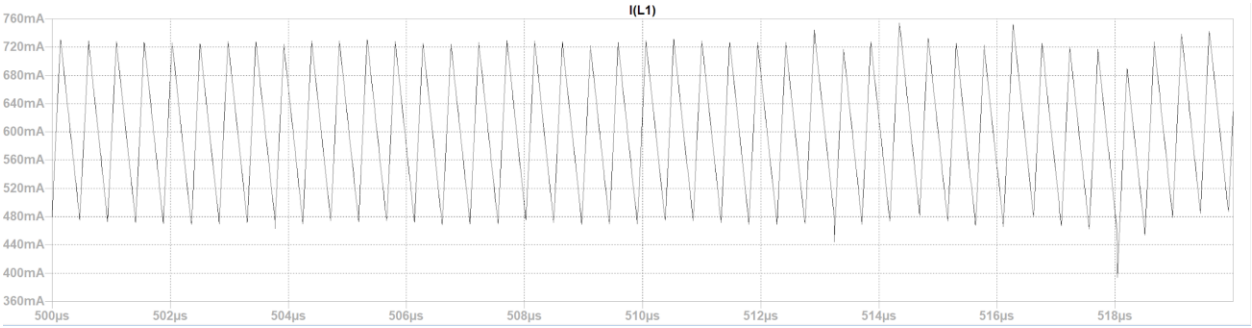

Figure 5-7: $I_L = I_o$ from 4.5ms to 4.52ms (S-S) for 12V input at 60% Load with ±4% SSFM

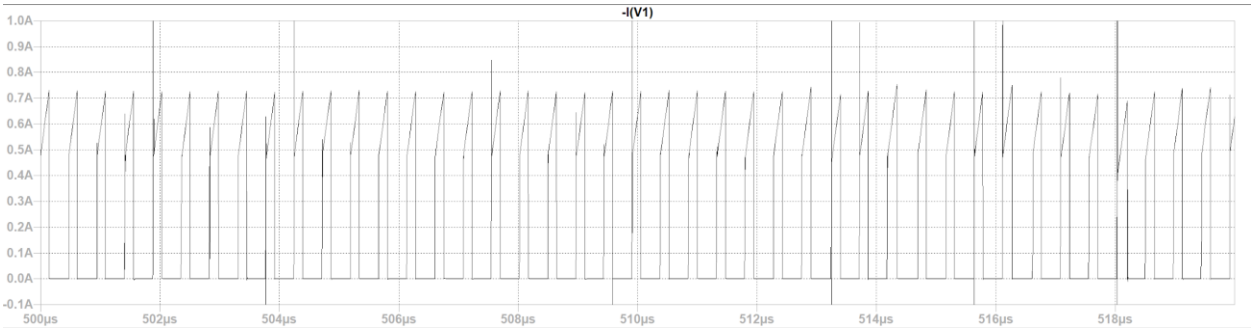

Figure 5-8: I_{IN} from 4.5ms to 4.52ms (S-S) for 12V input at 60% Load with ±4% SSFM

As briefly mentioned, spikes can be observed on the input current waveforms. Figure 5-9 shows the input source current in a 200µs window with around 15 spikes reaching up to 13kA. However, Figures 5-5 and 5-8 show that these spikes only occur at some rise and fall transitions of the input current switching. These spikes can be attributed not to the performance of the chip, but rather simulation calculation errors. The simulation input current spikes can also be observed on the FFT plots below since they are not in smooth and linear forms. For more input current spike captures, refer to Appendix A.

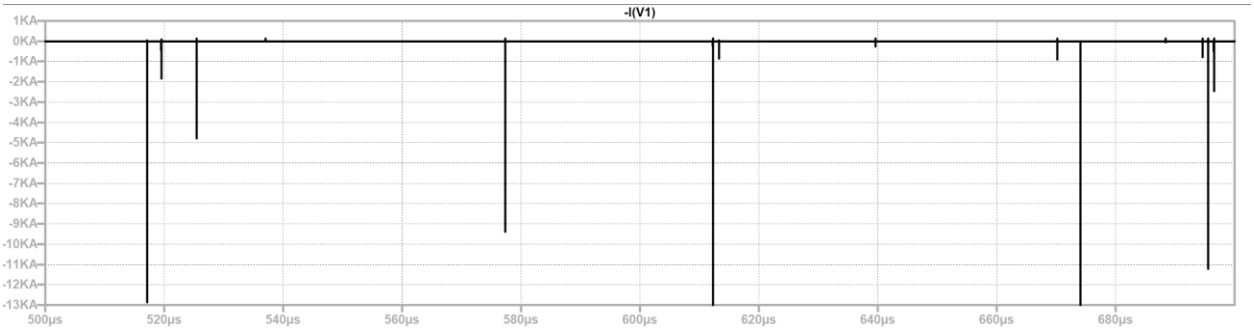

Figure 5-9: I_{IN} from 4.5ms to 4.7ms (S-S) for 12V input at 40% Load with ±4% SSFM

Figures 5-10, 5-11, and 5-12 respectively show the FFT plots for the input source current with a 12V input at 20% load with none, ±1%, and ±4% SSFM. For all FFT plots captured, the

frequency range was set from 100kHz to 110MHz. This range is to ensure that frequency content can be captured for frequencies at least one decade less than the internal clock frequency as well as frequencies in the FM broadband (88MHz to 108MHz). An initial observation among these three plots is that the maximum noise level sits around 10dB lower when using SSFM. The peak is around -7dB without SSFM and around -17dB with SSFM regardless of the percent spread. All three FFTs have similar shapes and noise ranges around 65dB ± 5dB.

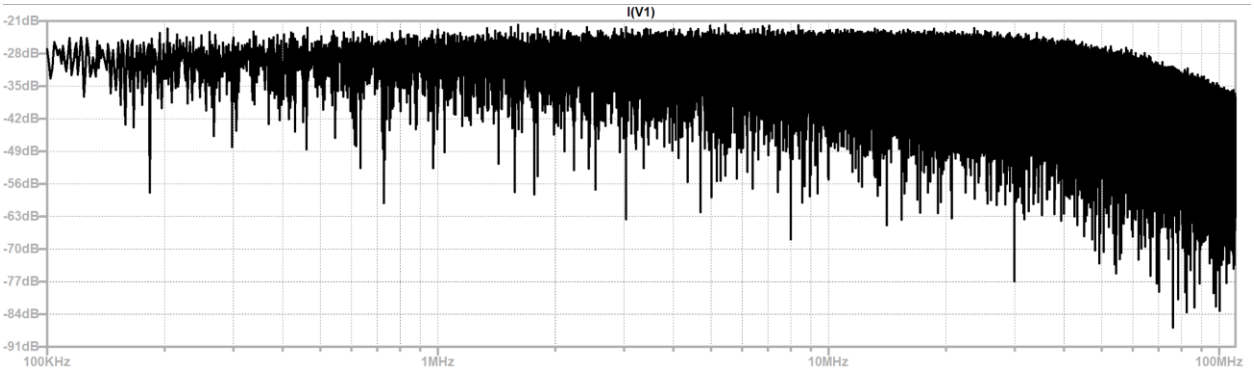

Figure 5-10: FFT of I_{IN} from 4ms to 5ms (S-S) for 12V input at 20% Load with no SSFM

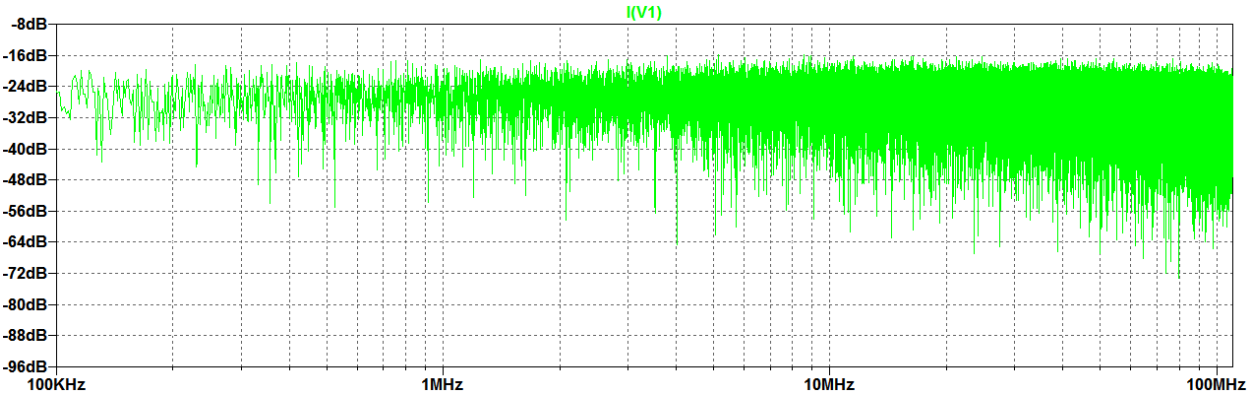

Figure 5-11: FFT of I_{IN} from 4ms to 5ms (S-S) for 12V input at 20% Load with ±1% SSFM

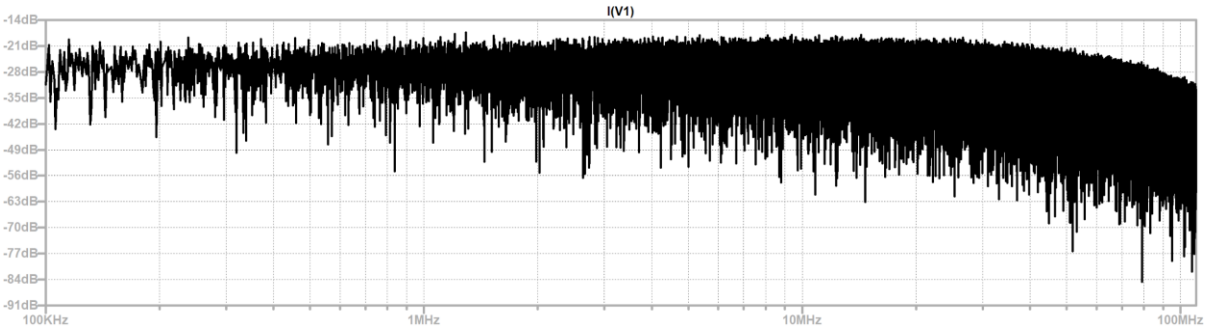

Figure 5-12: FFT of I_{IN} from 4ms to 5ms (S-S) for 12V input at 20% Load with ±4% SSFM

Figures 5-13, 5-14, and 5-15 respectively show the FFT plots for the input source current with a 12V input at 60% load with none, ±1%, and ±4% SSFM. Just like at 20% load, the maximum noise level sits lower when using SSFM. The noise peak is still around -7dB without SSFM. With ±1% spread the noise peak is around -30dB, and for ±4% spread the noise peak is around -22dB. All three FFTs again have similar shapes; however, there are some interesting differences in terms of range and minimum noise. The ±1% spread had the lowest recorded noise level at -95dB, but the ±4% spread had a noise range over 10dB smaller than the ±1% spread as well as with no SSFM.

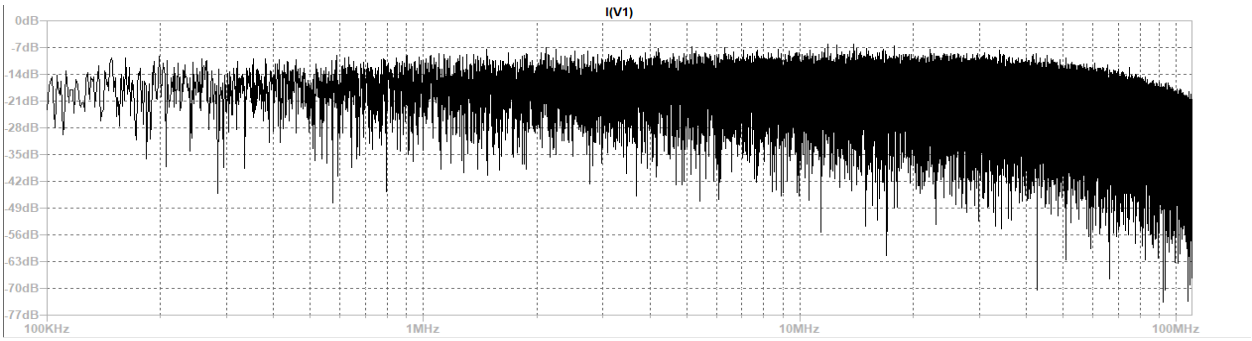

Figure 5-13: FFT of I_{IN} from 4ms to 5ms (S-S) for 12V input at 60% Load with no SSFM

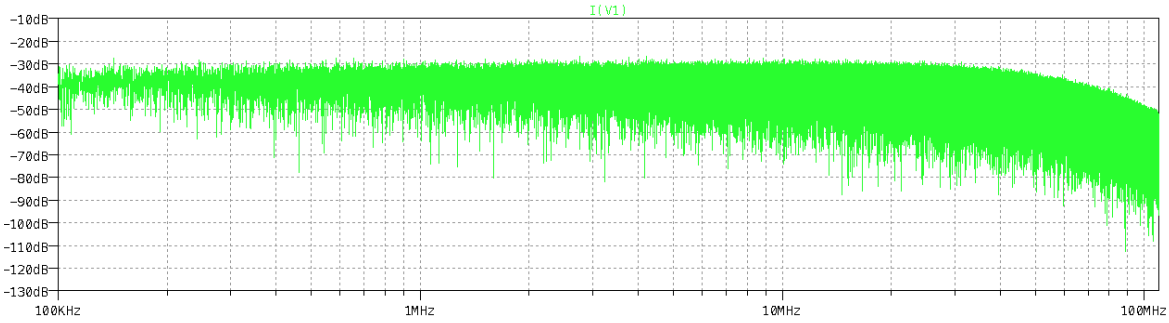

Figure 5-14: FFT of I_{IN} from 4ms to 5ms (S-S) for 12V input at 60% Load with ±1% SSFM

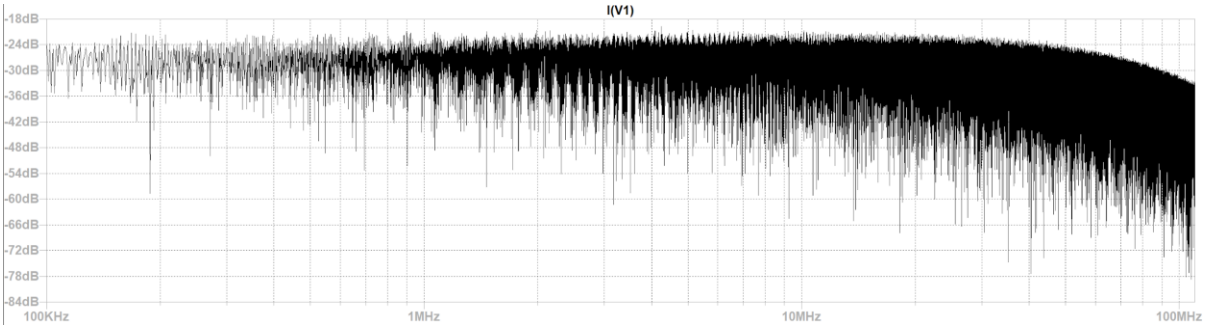

Figure 5-15: FFT of I_{IN} from 4ms to 5ms (S-S) for 12V input at 60% Load with ±4% SSFM

Figures 5-16, 5-17, and 5-18 respectively show the FFT plots for the input source current with a 12V input at 100% load with none, ±1%, and ±4% SSFM. In Figures 5-10, 5-13, and 5-16, it can be observed that overall shape, peak, and minimum noise levels do not change very much in the no SSFM cases regardless of percent load. At full load; however, the effect of spread spectrum can be more easily observed. The smoothness of the FFT curves increases and majority noise range decreases as SSFM percent modulation increases. Looking at the average peak and minimum values, the noise range for no SSFM is approximately 45dB (from -10dB to -55dB). With ±1% spread, the noise range is approximately 25dB (from -35dB to -60dB). With ±4% spread, the noise range is approximately 5dB (-35dB to -40dB). Looking at the ±4% spread FFT in Figure 5-18, spikes at certain frequencies can be easily distinguished. The ±1% spread FFT in Figure 5-17 shows a couple of these spikes as well. While the overall maximum and minimum

noise levels numerically are similar (±10dB) among the 12V full load test cases, these spikes can be attributed to particular frequencies at which the converter is operating at. For instance, the most prominent spike in Figure 5-18 can be attributed to the internal clock frequency at 2.1MHz.

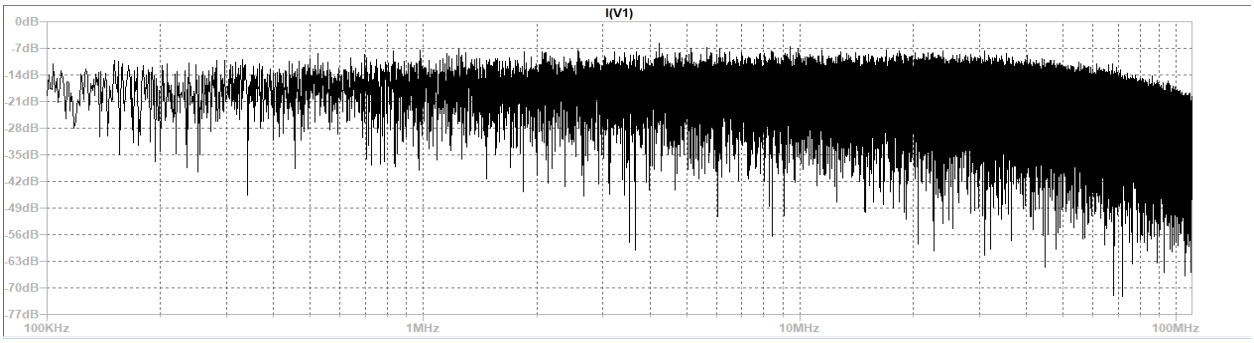

Figure 5-16: FFT of I_{IN} from 4ms to 5ms (S-S) for 12V input at 100% Load with no SSFM

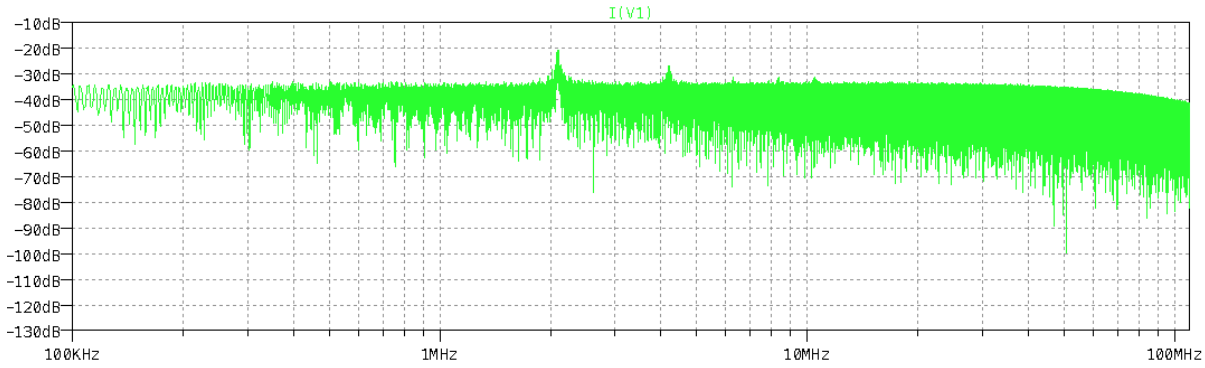

Figure 5-17: FFT of I_{IN} from 4ms to 5ms (S-S) for 12V input at 100% Load with ±1% SSFM

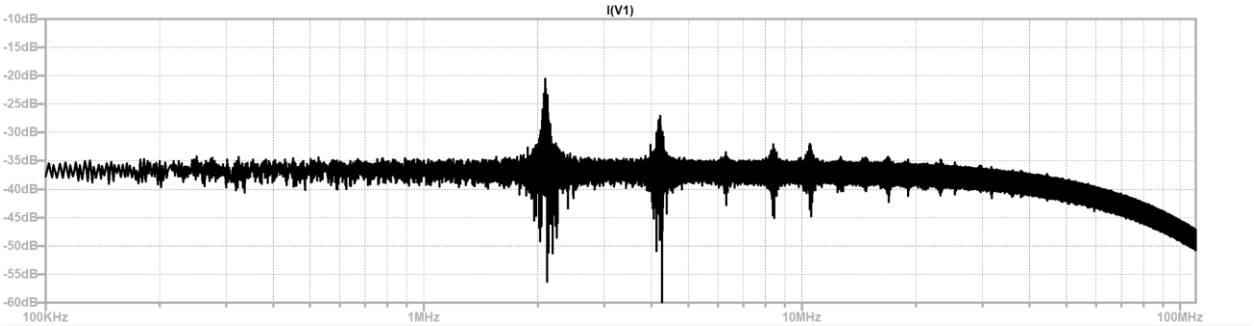

Figure 5-18: FFT of I_{IN} from 4ms to 5ms (S-S) for 12V input at 100% Load with ±4% SSFM

Next, the LM53601EVM was tested with the 24V input. The no SSFM case provided results as expected from a regular buck converter as shown in Figures 5-19, 5-20, and 5-21. The waveforms for the 100% load case. The output was around 3.61V, the inductor current ranged from 1.25A to 0.76A, and the inductor current was trapezoidal following the inductor's charging current going up to 1.25A. The time-domain waveforms for the other load cases look very similar. The main difference is that at lower loads, the inductor current peak and DC component are lower, which makes the input current lower as well.

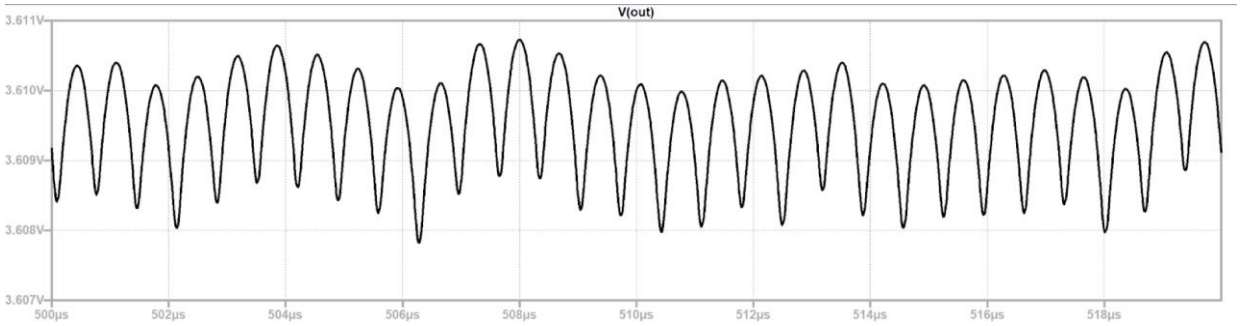

Figure 5-19: V_o from 4.5ms to 4.52ms (S-S) for 24V input at 100% Load with no SSFM

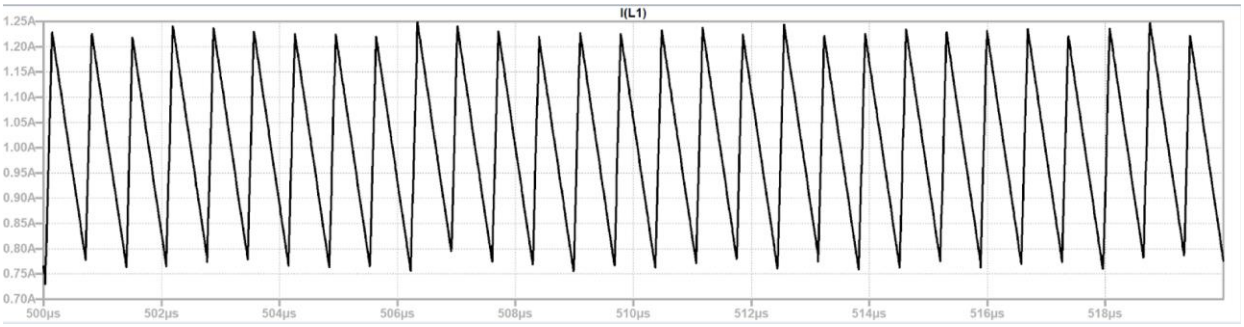

Figure 5-20: $I_L = I_o$ from 4.5ms to 4.52ms (S-S) for 24V input at 100% Load with no SSFM

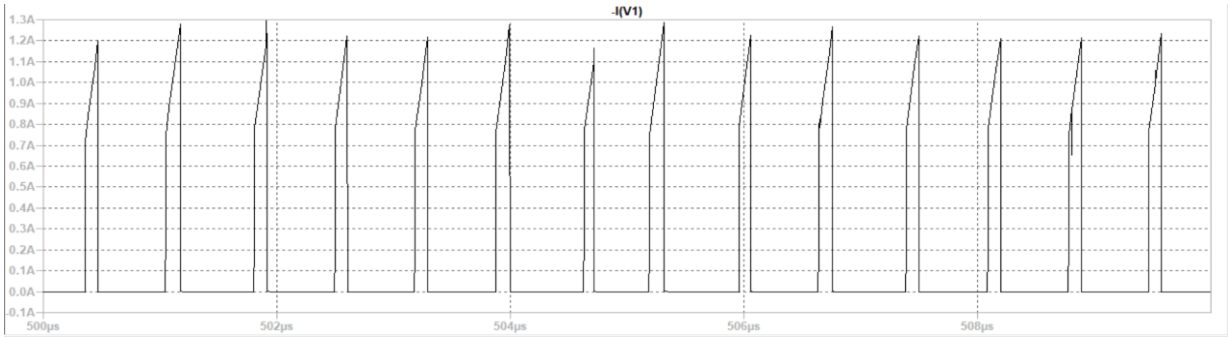

Figure 5-21: I_{IN} from 4.5ms to 4.51ms (S-S) for 24V input at 100% Load with no SSFM

When SSFM is introduced with the 24V input; however, the inductor current hits DCM. This is demonstrated by the 20% load case at ±4% SSFM as shown in Figures 5-22, 5-23, and 5-24. The input current is sinusoidal like the switching SSFM FPWM signal before it becomes trapezoidal as it follows the inductor current's positive charging slope. The input current shown here is measured going into ground, so that is the reason the polarity is reversed in Figures 5-23 and 5-24. Figure 5-23 shows one of the larger trapezoids from Figure 5-24 zoomed in. The shape of the input current is significantly different than what is seen in the previous cases. The change can be attributed to the inductor current reaching DCM. The shape can be described through the function of the current mode controller [21]. Current mode implies a Type 3 slope compensation. Therefore, the comparator in the feedback has three pins, watching for overall current peak limit and the maximum slope limit. As seen from Figures 5-23 and 5-24, the larger trapezoids have the same peak due to the current limit, but the smaller trapezoids have increasing slopes until they reach the slope limit, where the slopes become approximately the same. Furthermore, the inductor current reaches DCM because the controller transitions to PFM for better efficiency at lighter loads because only a small current is needed, so the frequency can be reduced. This also

contributes to a discrepancy in the output voltage with the average rising to 3.85V instead of the expected 3.6V.

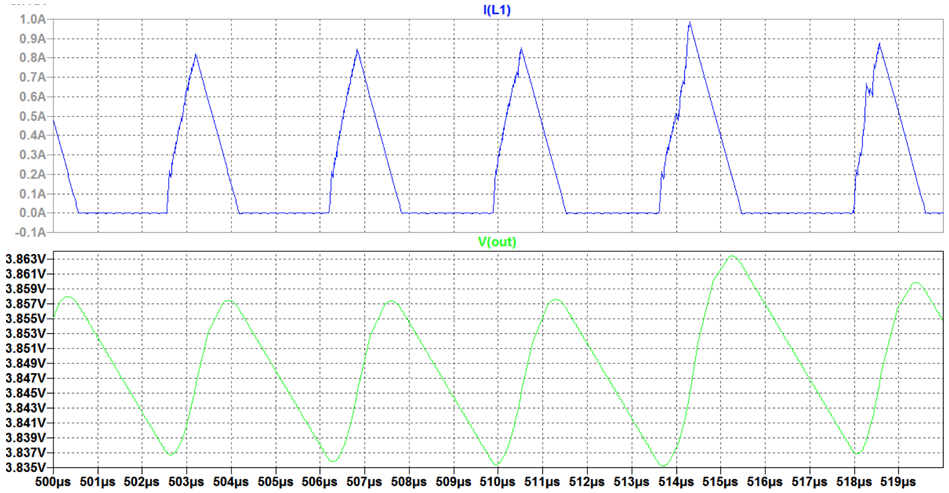

Figure 5-22: V_o and I_L for 20µs (S-S) for 24V input at 100% Load with ±4% SSFM

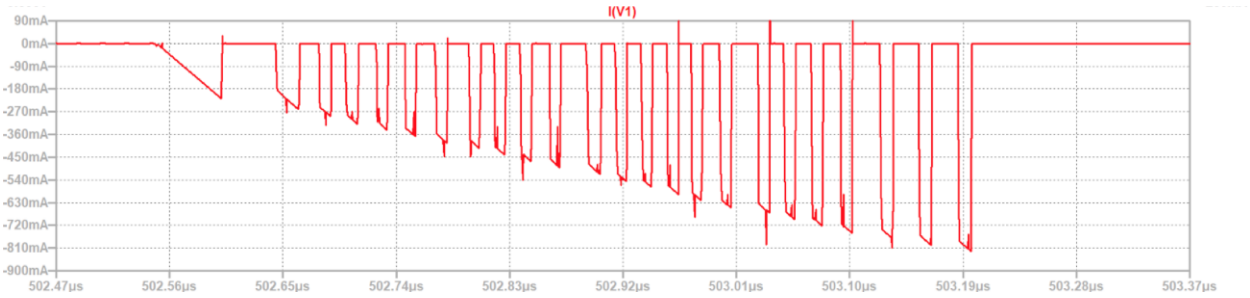

Figure 5-23: I_{IN} for 1µs (S-S) for 24V input at 100% Load with ±4% SSFM

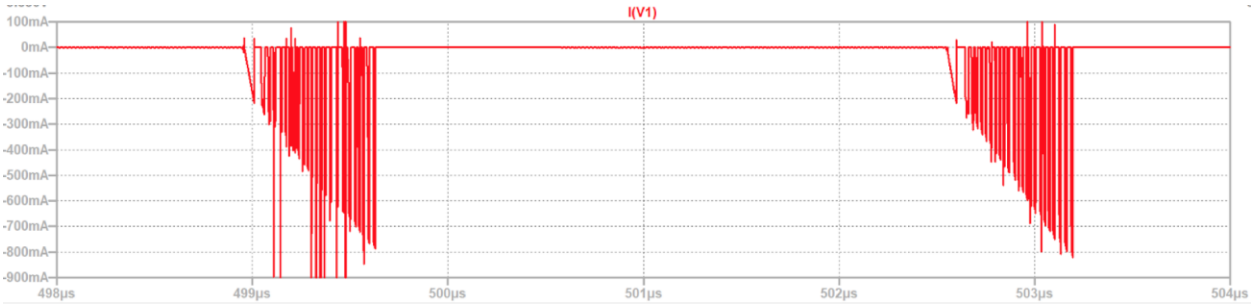

Figure 5-24: I_{IN} for 5µs (S-S) for 24V input at 20% Load with ±4% SSFM

The full-load case for the 24V input at ±4% SSFM is provided in Figures 5-25 and 5-26 to show the differences happening in the time-domain. As previously explained, DCM happens due to transition to PFM at lower loads. Hence, as the load increases, the durations of the inductor current at 0A decrease. Transitions happen more often, which could increase the noise. At the 100% load case, the inductor current does not always stay in DCM, as shown by Figure 5-25. The PFM behavior happens consistently with all loads for ±4% SSFM and ±1% SSFM as well. DCM, however, occurs for a longer period in the ±1% SSFM cases, as compared to the ±4% SSFM cases. The other time-domain waveforms are not presented in this chapter, as they are similar, and can be found in Appendix A.

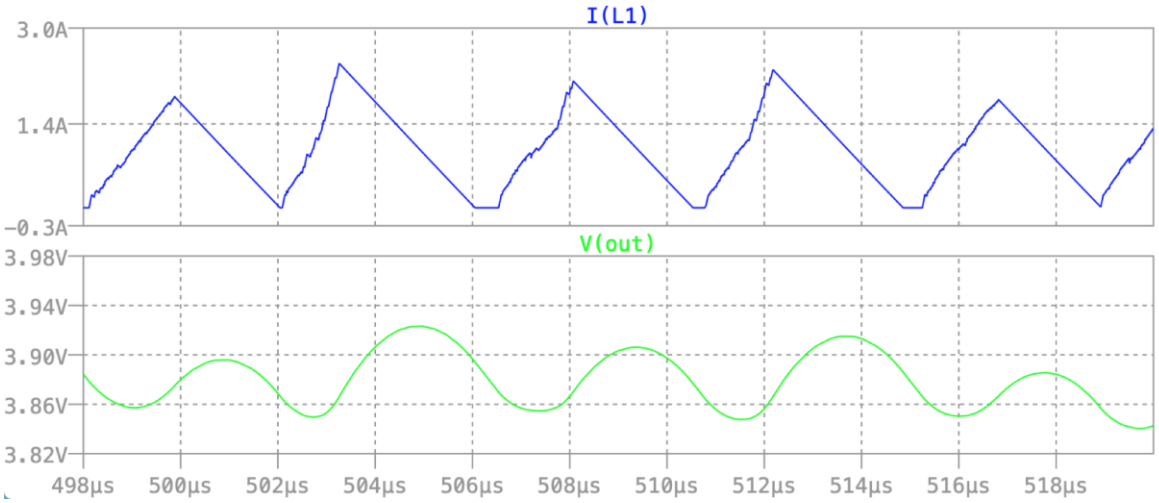

Figure 5-25: V_o and I_L for 20µs (S-S) for 24V input at 100% Load with ±4% SSFM

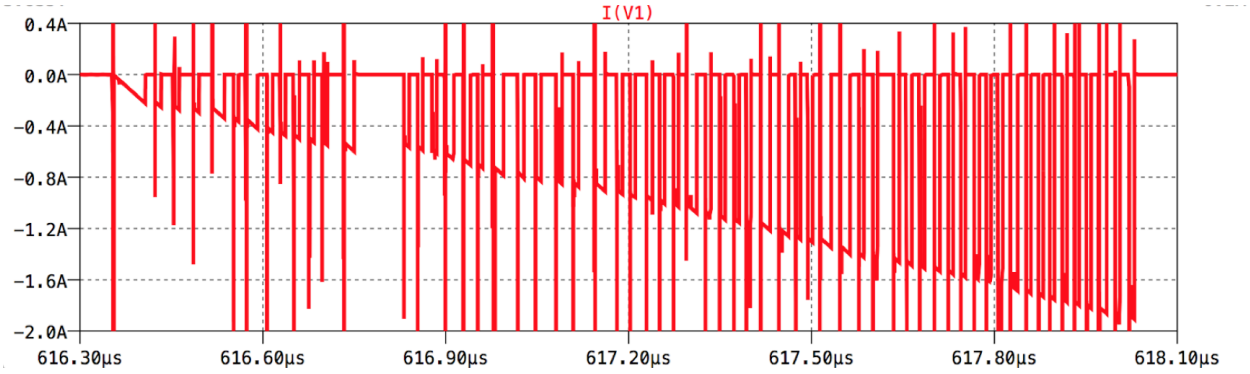

Figure 5-26: I_{IN} for 2µs (S-S) for 24V input at 100% Load with ±4% SSFM

Regarding the noise analysis, all the 24V cases exhibit higher noise content as compared to the 12V cases. Higher noise occurs for higher inputs because the inductor slope is higher. The inductor is directly proportional to the voltage across the inductor, which is the difference between the input voltage and the output voltage. Therefore, more di/dt noise is introduced as the input follows the charging portion of the inductor waveform. Only the 20%, 60%, and 100% load cases are presented as they show the characteristic differences that happen at edge cases and mid-range.

Figures 5-27, 5-28, and 5-29 show the FFT of the input current at 100% load for no SSFM, ±1% SSFM, and ±4% SSFM, respectively. The no SSFM case ranges from -7dB to -63dB, the ±1% SSFM case ranges from -7dB to -75dB, and the ±4% SSFM case ranges from 4dB to -72dB. The ±1% SSFM does not provide a significant improvement at this load. The noise reaches lower levels due to simulation spikes, but the envelope does not change substantially. The ±4% SSFM case gives worse noise around 220kHz. This lower frequency noise could be attributed to the PFM mode, which lowers the frequency for better efficiency. This peak is only seen at full load, which could be because the transitions are higher due to load demands and happen slightly more often due to decreased DCM operation than at the lower loads, so their noise is seen within the range.

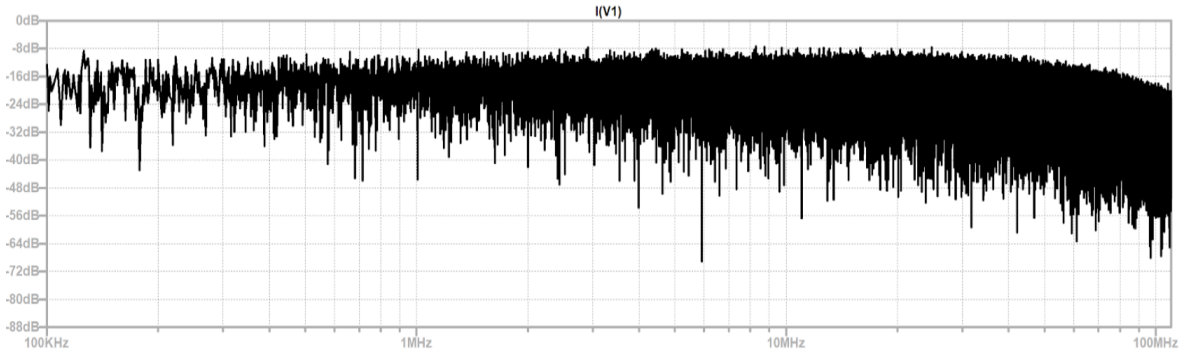

Figure 5-27: FFT of I_{IN} from 4ms to 5ms (S-S) for 24V input at 100% Load with no SSFM

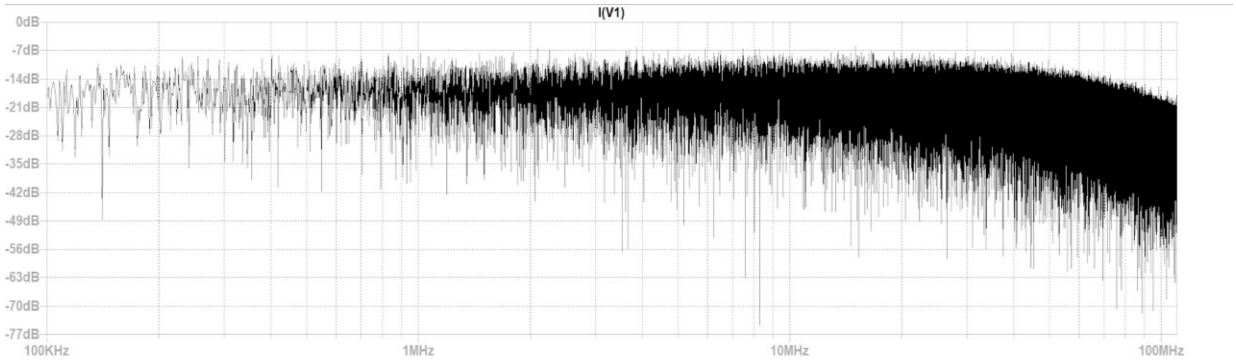

Figure 5-28: FFT of I_{IN} from 4ms to 5ms (S-S) for 24V input at 100% Load with ±1% SSFM

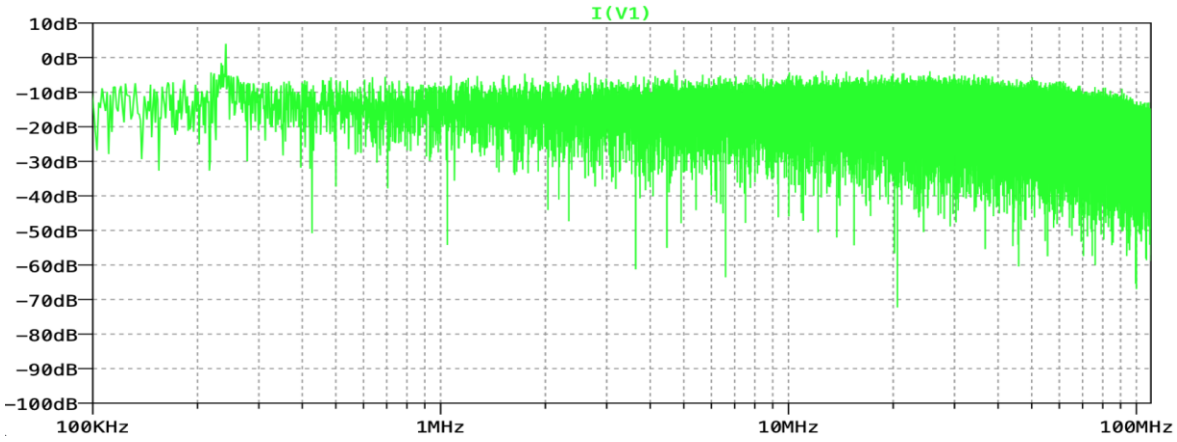

Figure 5-29: FFT of I_{IN} from 4ms to 5ms (S-S) for 24V input at 100% Load with ±4% SSFM

Figures 5-30, 5-31, and 5-32 show the FFT of the input current at 60% load for none, ±1%, and ±4% SSFM, respectively. The no SSFM case ranges from -2dB to -90dB, the ±1% SSFM case ranges from -7dB to -77dB, and the ±4% SSFM case ranges from -10dB to -60dB.

As seen by the figures and ranges, both cases of SSFM for the 60% load provide a reduction in noise with the ±4% SSFM showing better improvement. Also, the ±4% SSFM case is more uniform, as shown in Figure 5-32, throughout all frequencies. This is expected as larger percentages correspond to more spread in frequency in SSFM. The 80% load cases also have an improvement in noise with both ±1% and ±4% SSFM, which are about the same, but less than the 60% load cases.

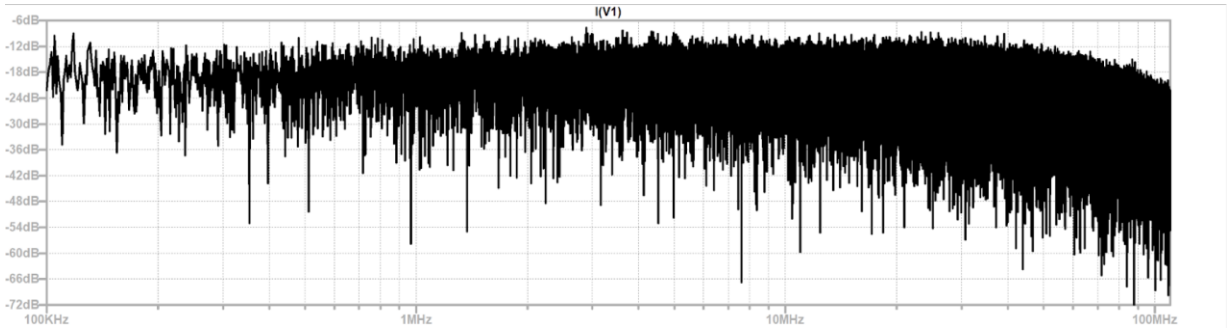

Figure 5-30: FFT of I_{IN} from 4ms to 5ms (S-S) for 24V input at 60% Load with no SSFM

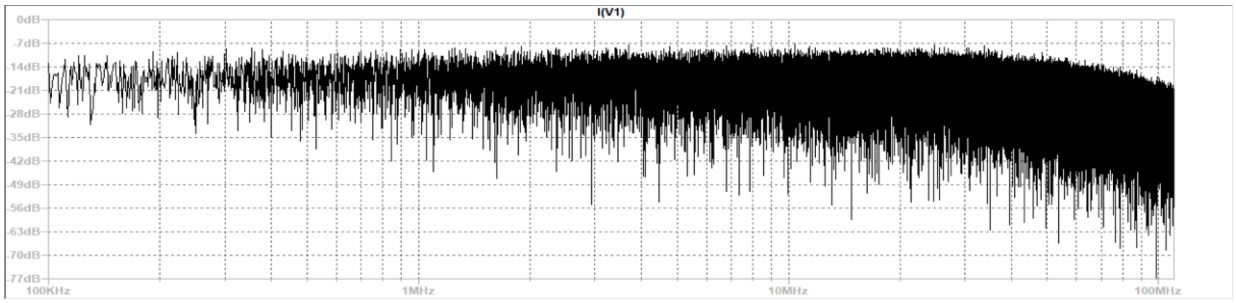

Figure 5-31: FFT of I_{IN} from 4ms to 5ms (S-S) for 24V input at 60% Load with ±1% SSFM

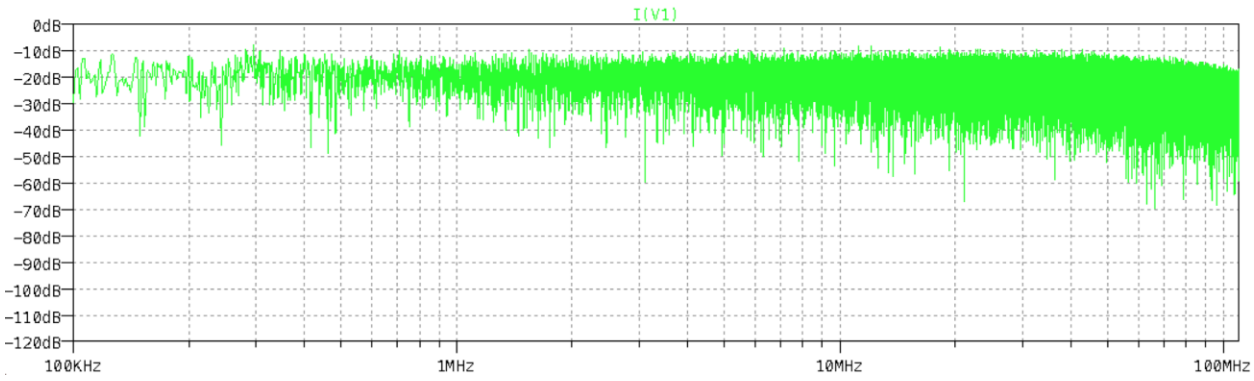

Figure 5-32: FFT of I_{IN} from 4ms to 5ms (S-S) for 24V input at 60% Load with ±4% SSFM

Figures 5-33, 5-34, and 5-35 show the FFT of the input current at 20% load for no SSFM, ±1% SSFM, and ±4% SSFM, respectively. The no SSFM case ranges from -7dB to -63dB, the ±1% SSFM case ranges from -10dB to -dB, and the ±4% SSFM case ranges from -8dB to -68dB. Both the ±1% and ±4% SSFM cases provide results that are worse than the case with no SSFM, even though the SSFM is supposed to help with input EMI reduction. This can be attributed to the higher input voltage increasing the inductor slope and the switching noise, as well as the PFM operation deviating from CCM and PWM. As in the previous cases the ±4% SSFM provides more uniform noise across the frequency range. The 40% load cases provide similar results.

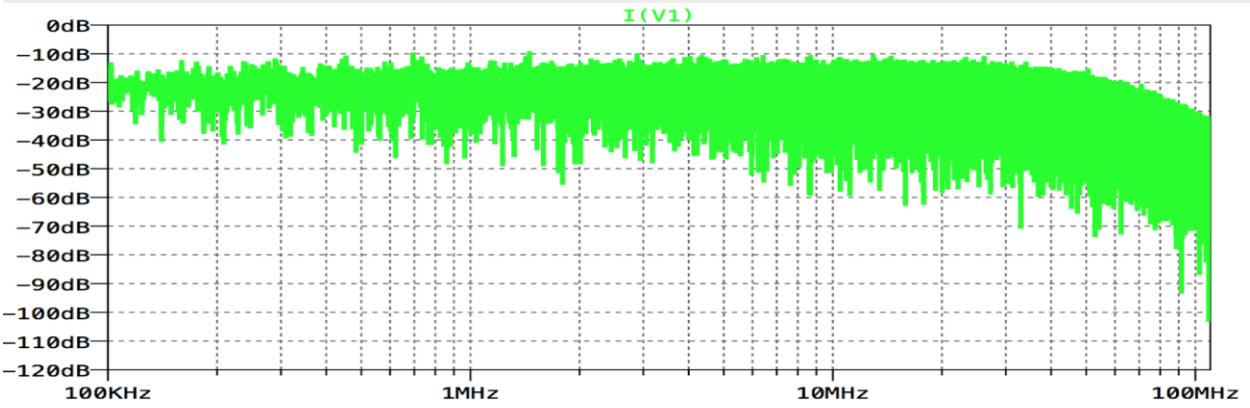

Figure 5-33: FFT of I_{IN} from 4ms to 5ms (S-S) for 24V input at 20% Load with no SSFM

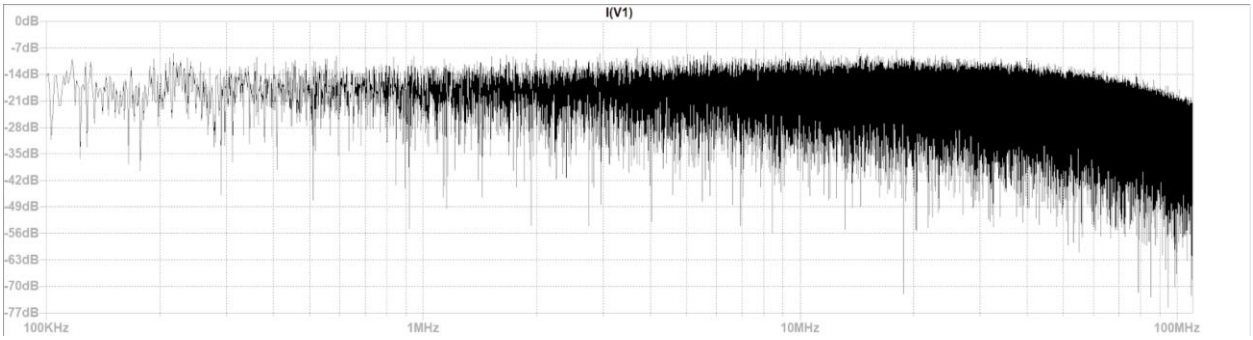

Figure 5-34: FFT of I_{IN} from 4ms to 5ms (S-S) for 24V input at 20% Load with ±1% SSFM

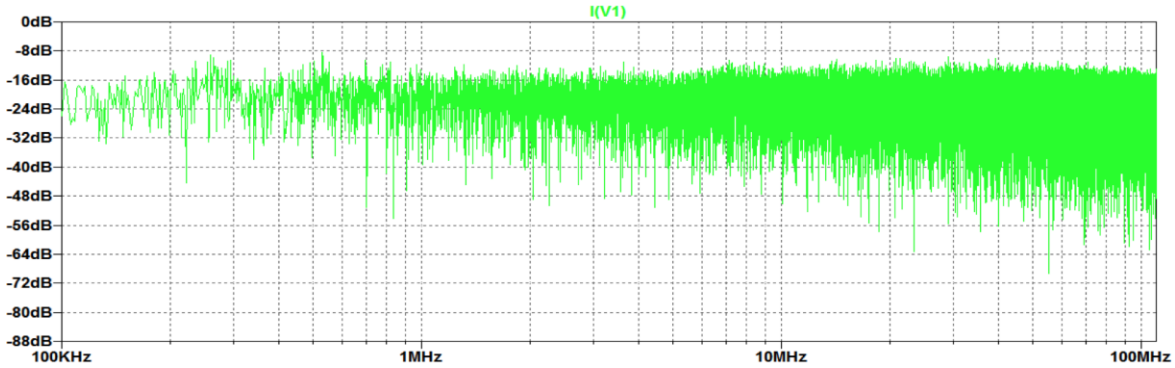

Figure 5-35: FFT of I_{IN} from 4ms to 5ms (S-S) for 24V input at 20% Load with ±4% SSFM

A summary of all cases is shown in Table 5-1 in terms of the input current EMI for a basic general comparison. The range of noise generated by the buck converter on the input is shown for additional information about the overall noise profile, even though only the peak noise is considered in CISPR standards. For simulation captures that were not shown in this chapter, please refer to Appendix A.

Table 5-1: Range of Noise Levels for all 30 Test Cases

Percent Load (%)	12V No SSFM Noise Range	12V ±1% SSFM Noise Range	12V± 4% SSFM Noise Range	24V No SSFM Noise Range	24V ±1% SSFM Noise Range	24V ±4% SSFM Noise Range
20	-7dB to -65dB	-18dB to -73dB	-17dB to -84dB	-10dB to -90dB	-8dB to -64dB	-8dB to -68dB
40	-12dB to -70dB	-25dB to -100dB	-19dB to -63dB	-13dB to -90dB	-8dB to -75dB	-10dB to -74dB
60	-7dB to -70dB	-30dB to -95dB	-22dB to -72dB	-2dB to -90dB	-7dB to -77dB	-10dB to -60dB
80	-10dB to -64dB	-22dB to -72dB	-21dB to -75dB	-7dB to -66dB	-8dB to -80dB	-8dB to -65dB
100	-7dB to -71dB	-20dB to -80dB	-20dB to -60dB	-7dB to -63dB	-7dB to -75dB	+4dB to -72dB

Chapter 6: Conclusion

Overall, SSFM in the 12V cases was more successful at reducing the EMI levels. Both input voltage cases performed best at 60% load, regardless of the SSFM spread. Looking at the 12V input only, all cases showed noise improvements when using SSFM regardless of percent load or spread with the noise peaks at least 7dB below its respective percent load with no SSFM. Based on input voltage and percent spread, noise level was the worst at 20% load for both ±1%, which reached a maximum of -18dB, and ±4% spread with a maximum of -17dB. Noise level was the best at 60% load for both percent spreads. Broadening the scope to look only at 12V inputs again, the worst cases by peak noise is the 20%, 60% or full load cases for no SSFM at -7dB. The best case within the same scope is the 60% load with ±1% spread which has a peak at -30dB. For the 24V input, the 60% load also yielded the best results with both ±1% and ±4% spread. While the ±4% spread provided 3dB more EMI reduction reaching peak of -10dB at the 60% load, it also provided the worst case that happened at 100% load, where the EMI peaked up to 4dB, which was much worse than no SSFM. At full load for ±1% spread; however, the SSFM performed about the same as no SSFM in terms of peak noise. The ±1% spread was more consistent regardless of the load. At light loads, for both percentages of spread, the cases with SSFM tended to do worse than using no SSFM. Comparing the performance of the input voltages, the 24V best case did not perform nearly as well as the worst case for the 12V input.

Since the LM53601 is a step-down converter intended for automotive purposes, noise levels measured were compared to the CISPR-25 and CISPR-32 standards to determine whether the converter passes automotive and multimedia EMI ratings. The CISPR-25 standard dictates a maximum noise level of 70dBμV at long wave broadband (150kHz to 300kHz) [2]. This range is

within the scope of the collected FFT data and also the range with the least strict EMI requirements. To convert dBμV to the dBV as shown on the FFT plots, the following conversion can be used:

$$dBV = 20\log\left(10^{\frac{\text{dBuV}}{20}}\left(10^{-6}\right)\right) \quad (6\text{-}1)$$

Applying Equation 6-1 with 70dBμV gives -50dBV. Notice in Table 5-1 that the best test case for all thirty shows a peak of -30dBV. Hence, it can be concluded that none of the recorded test cases will meet the CISPR-25 standard. At the long wave range, the CISPR-32 standard has a noise threshold of 79dBμV [2]. This, however, converts to -41dBV which is still below our best test case. Therefore, none of our simulations meet either applicable CISPR standards. Noise levels observed from this senior project; however. do pass the CISPR-11 standard. CISPR-11 is the international product standard for EMI disturbances from industrial, scientific, and medical (ISM) radiofrequency (RF) equipment [2]. The strictest requirement for Class A Group 2 HP is a quasi-peak of 115dBμV for frequencies above 5MHz, which translates to -5dBV. All thirty cases tested, even those without SSFM, pass CISPR-11 Class A Group 2 HP except for the 24V full load ±4% spread.

Having observed that all the simulated test cases do not pass the CISPR-25 nor CISPR-32 standards, the notion of whether or not SSFM is worth implementing comes into question. For 12V input test cases, all loads showed at least a 7dB attenuation regardless of ±1% or ±4% spread. Yet, the amount of attenuation is not enough to meet CISPR-25 or CISPR-32 EMI standards. Furthermore, the difference between using and not using SSFM is rather noticeable. Incorporating the modulator adds additional complexity to the simulation. When operating in FPWM to use external SSFM, simulation times take longer and require more computing power

to process. In terms of physical hardware, it would also mean adding more complexity and capability to the buck converter design. This will effectively result in more time in terms of design and set-up as well as more space required, which will lead to higher production costs. An additional trade-off, specifically regarding the 24V case, is that using SSFM changes the operation of the controller causing DCM for higher efficiency, so the output increases by 300mV instead of staying at the expected 3.6V. Therefore, since the 24V SSFM cases provide only several dB improvements with mid-range loads, SSFM with the 24V input will be useful only if that slight reduction is absolutely necessary and the offset in output can be tolerated.

In conclusion, the simulated test case data from Chapter 5 shows that SSFM improved the noise response for all 60% load cases regardless of input voltage and percent spread. In terms of consistency, however, SSFM proved to be the most successful at low input voltages as our simulation showcased that SSFM improved EMI levels for all 12V cases. Also, the 1% spread showed more consistent noise reduction, especially for the lower voltage input cases. A preliminary recommendation based on the simulation results is to use SSFM at lower input voltages, lower percent spread, and mid-range loads for best results.

However, further work can be done in order to obtain better results. First of all, more simulations would help determine the effects of SSFM on input current EMI reduction more clearly. More simulations could include more input voltage cases, more percent spread cases, and more load cases. Since simulations take a long time to complete, higher computing power or a faster simulation software would be beneficial. In addition, different waveforms for modulation carriers, besides the sinusoid used here, can be explored for further possible reduction in EMI. The most important next step; however, would be to do the measurements in hardware, especially since EMI depends substantially on the layout. Exploring the effects in hardware

could provide more insight into the practical implications of the effects of variable SSFM. Furthermore, the analysis of how well hardware results correlate with simulation results could prove to be interesting.

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Appendix A: All Simulation Results

Case 1: 20% Load No SSFM at V_{IN} = 12V

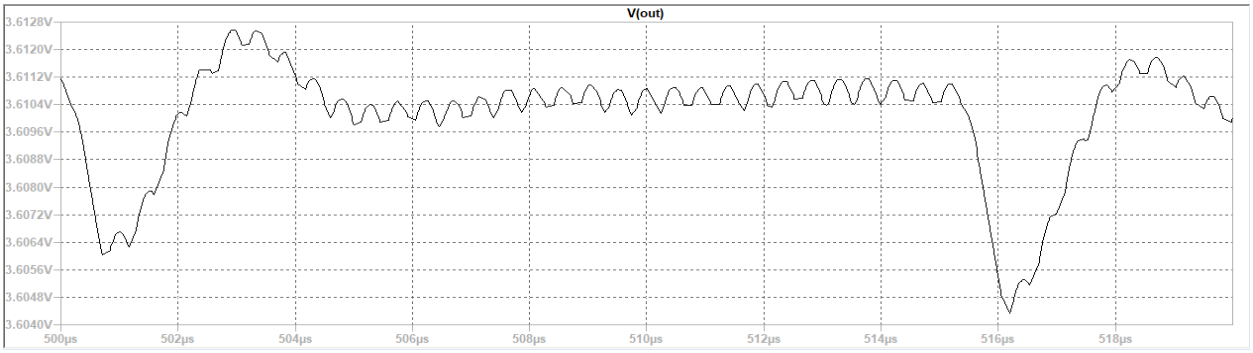


Figure A-1: V_o from 4.5ms to 4.52ms (S-S)

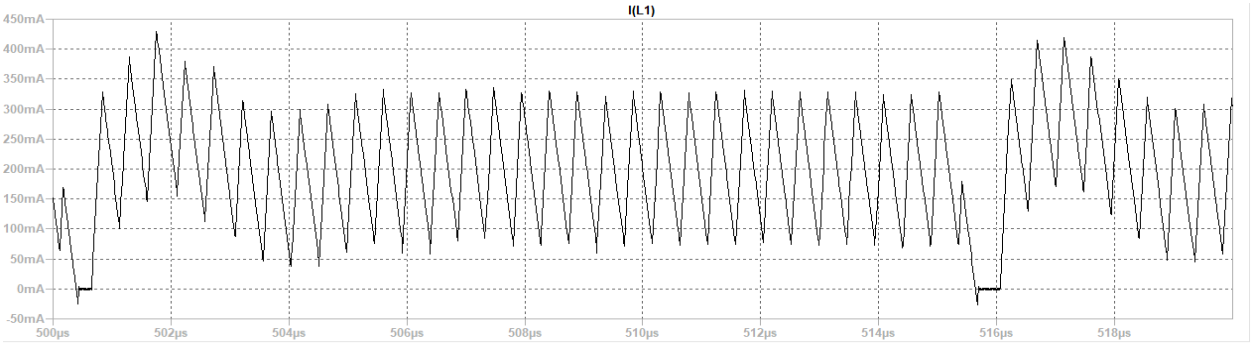


Figure A-2: $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

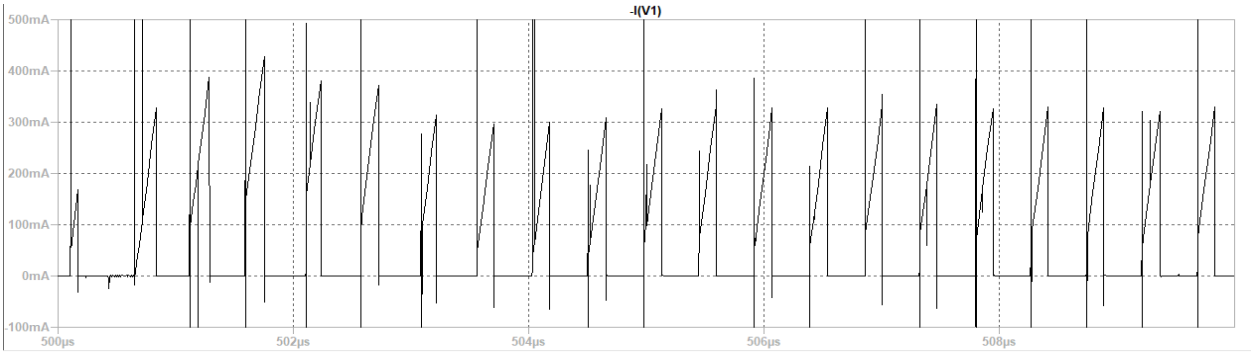


Figure A-3: I_{IN} from 4.51ms to 4.52ms (S-S) Showing Input Current Switching

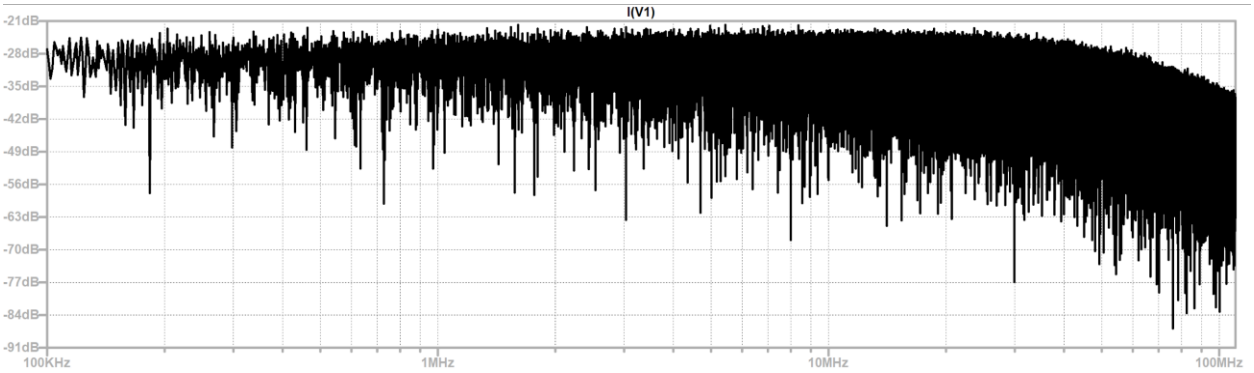


Figure A-4: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 2: 40% Load No SSFM at V_{IN} = 12V

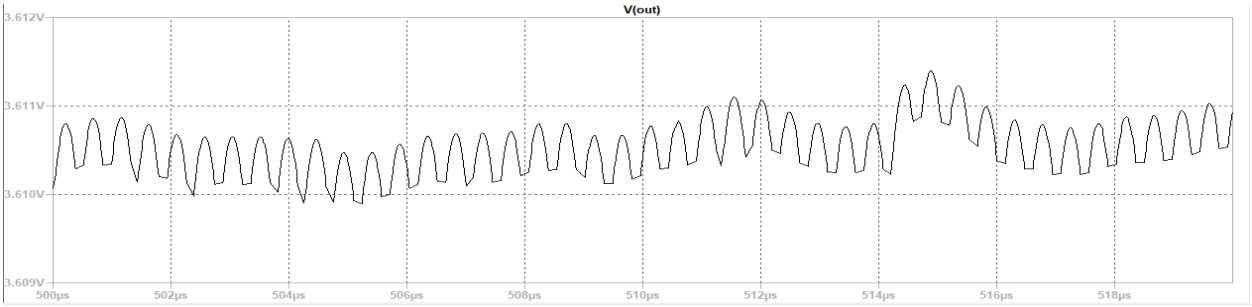


Figure A-5: V_o from 4.5ms to 4.52ms (S-S)

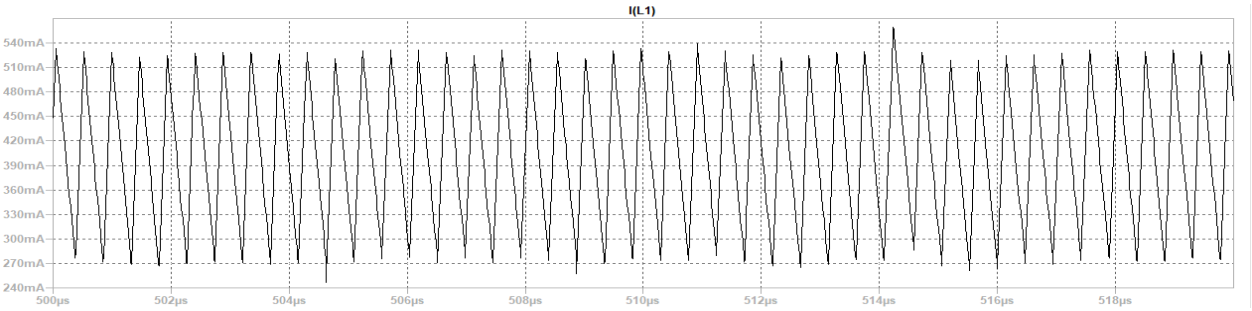


Figure A-6: $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

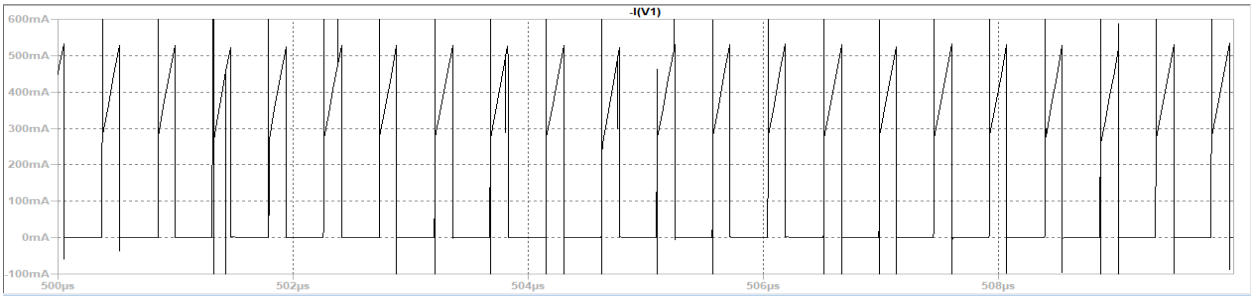


Figure A-7: I_{IN} from 4.5ms to 4.51ms (S-S) Showing Input Current Switching

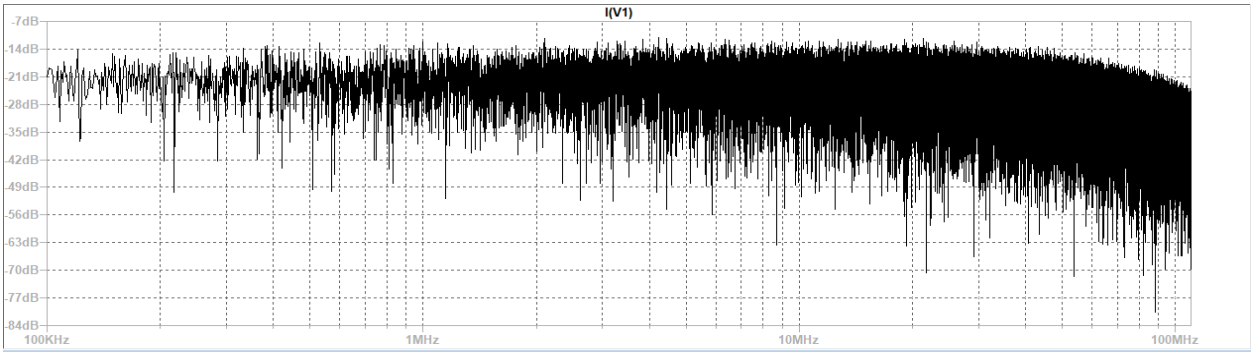


Figure A-8: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 3: 60% Load No SSFM at V_{IN} = 12V

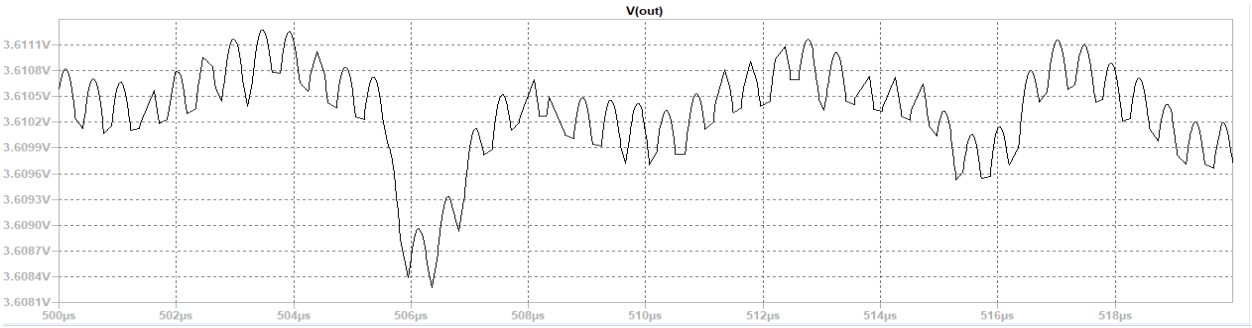


Figure A-9: V_o from 4.5ms to 4.52ms (S-S)

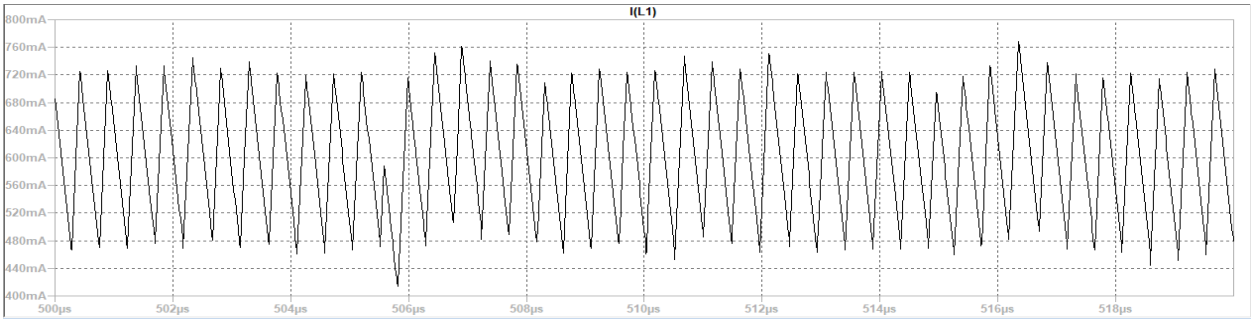


Figure A-10: $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

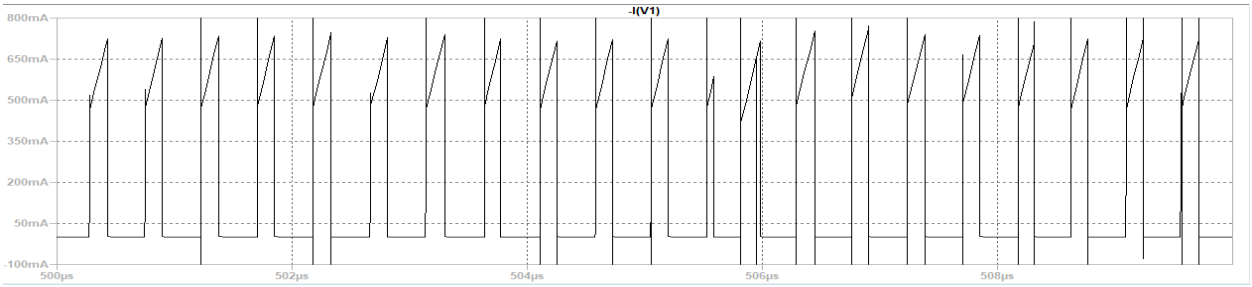


Figure A-11: I_{IN} from 4.5ms to 4.51ms (S-S) Showing Input Current Switching

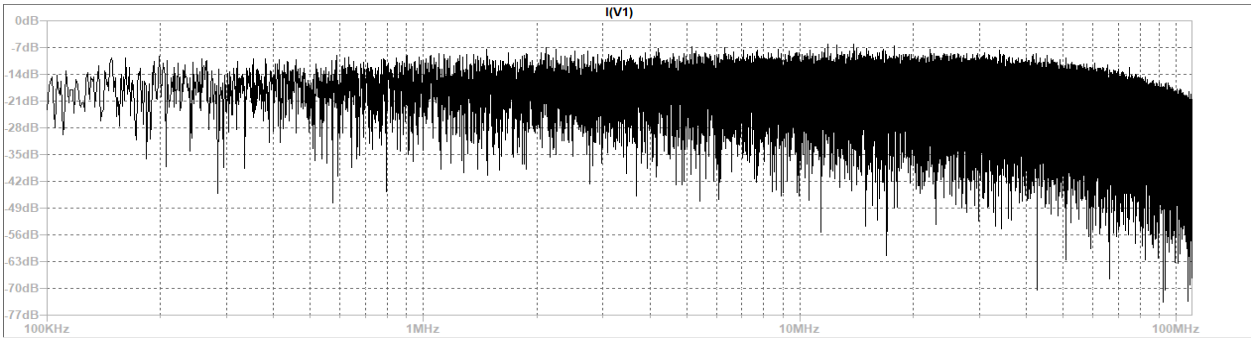


Figure A-12: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 4: 80% Load No SSFM at V_{IN} = 12V

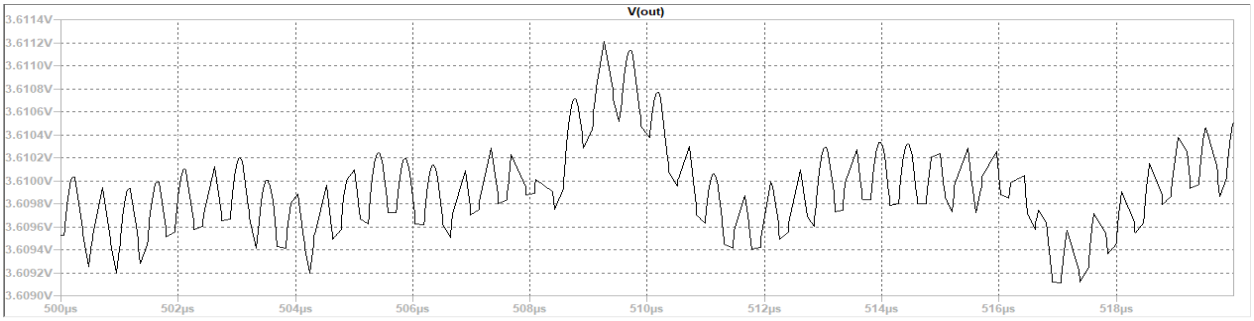


Figure A-13: V_o from 4.5ms to 4.52ms (S-S)

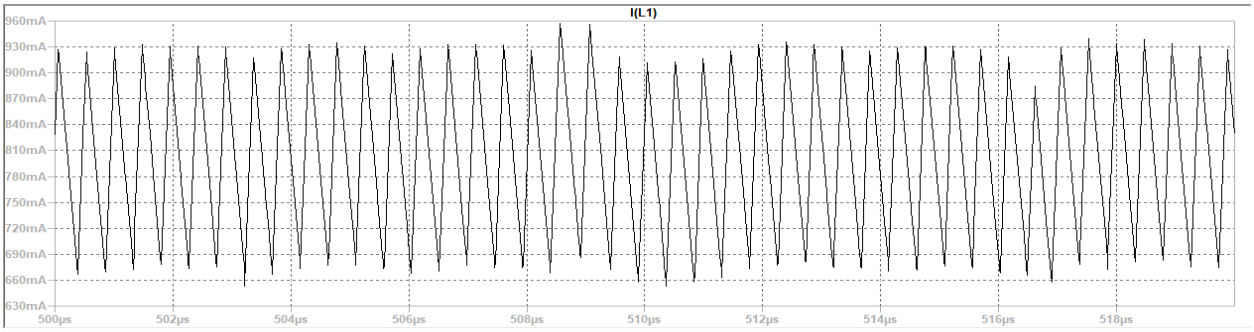


Figure A-14: $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

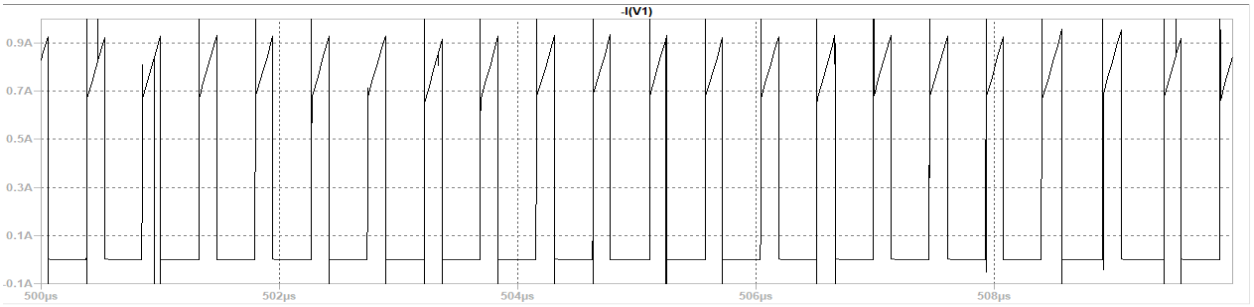


Figure A-15: I_{IN} from 4.5ms to 4.51ms (S-S) Showing Input Current Switching

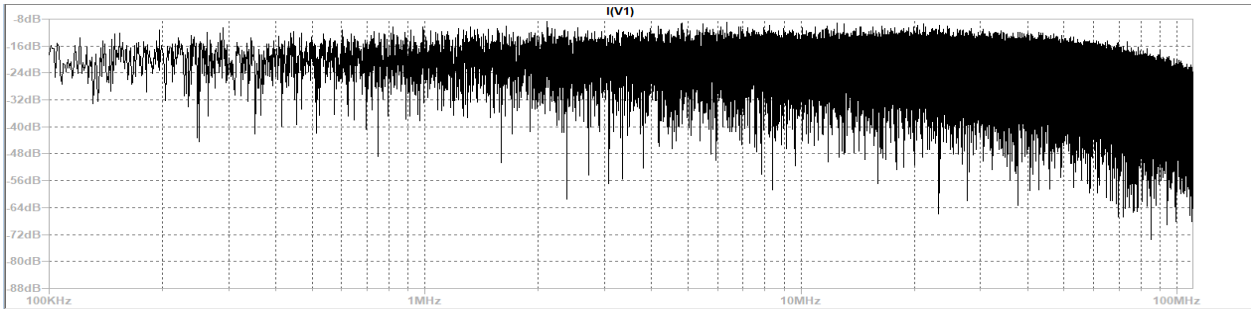


Figure A-16: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 5: Full Load (1A) No SSFM at V_{IN} = 12V

Figure A-17: V_o from 4.5ms to 4.52ms (S-S)

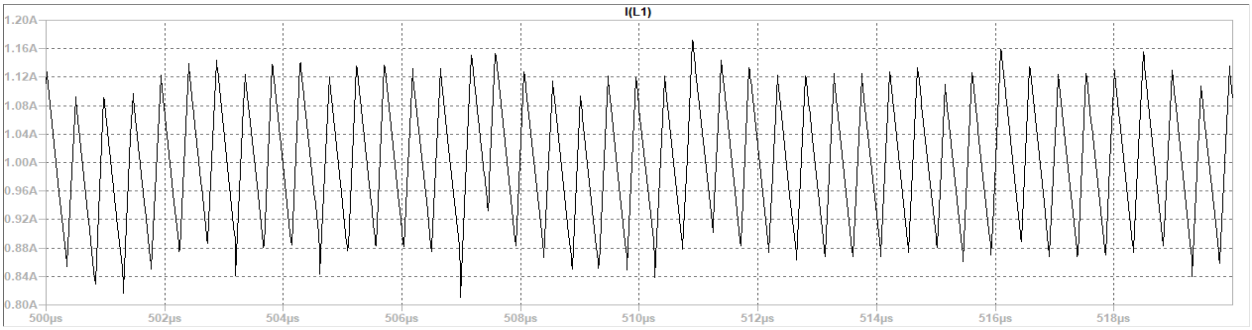


Figure A-18: $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

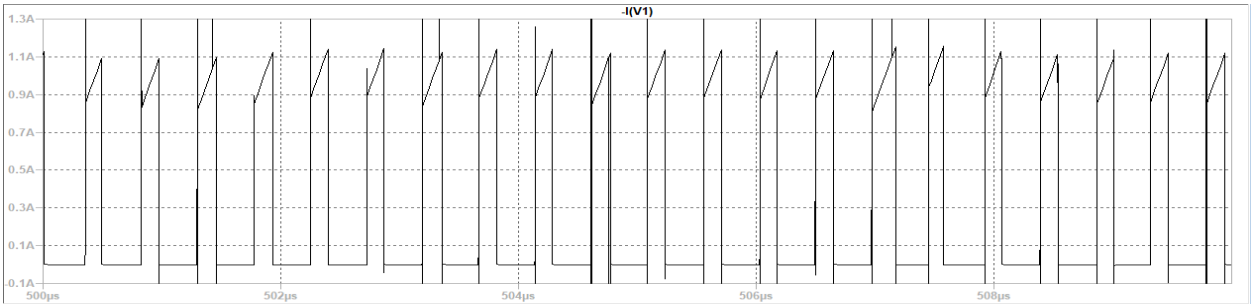


Figure A-19: I_{IN} from 4.5ms to 4.51ms (S-S) Showing Input Current Switching

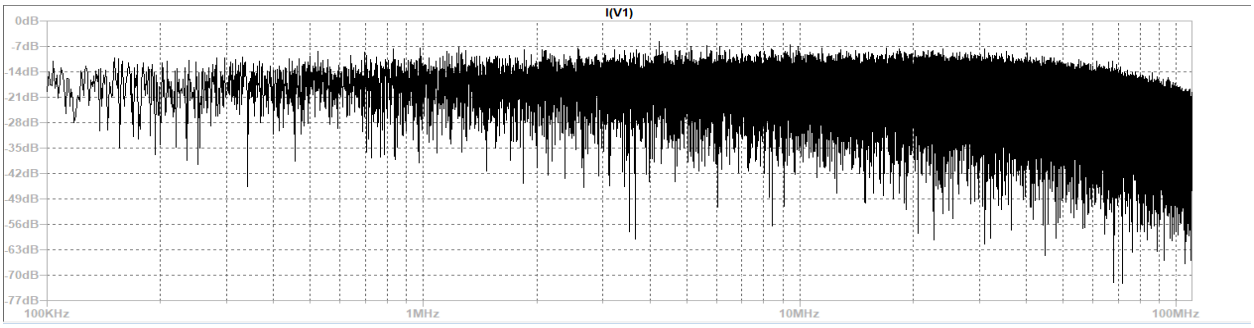


Figure A-20: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 6: 20% Load +/- 1% SSFM at V_{IN} = 12V

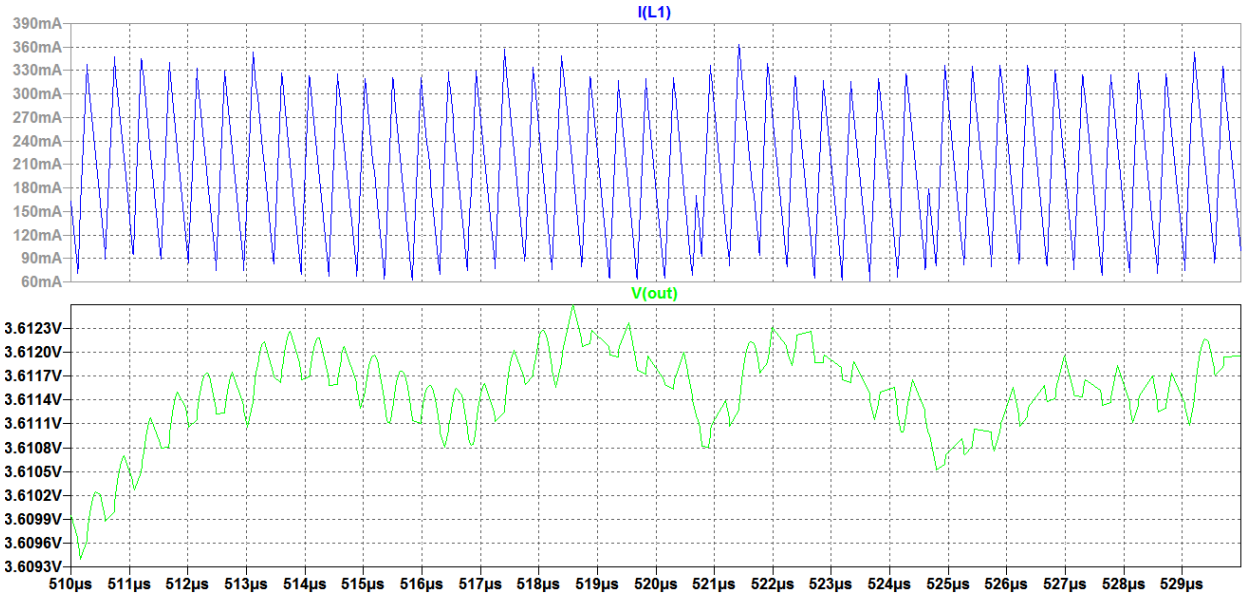


Figure A-21: V_o and $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

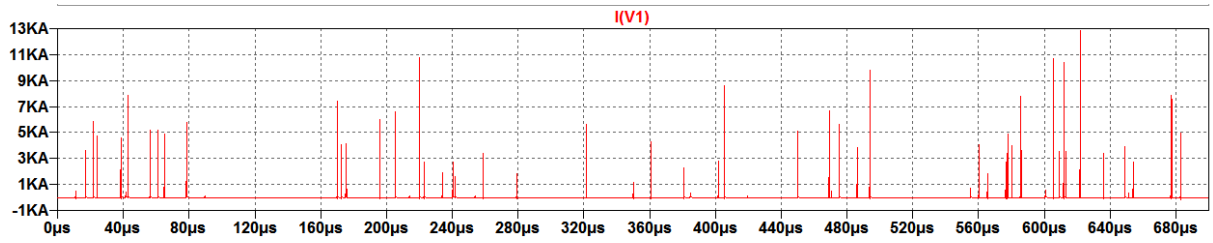


Figure A-22: I_{IN} from 4.5ms to 4.7ms (S-S)

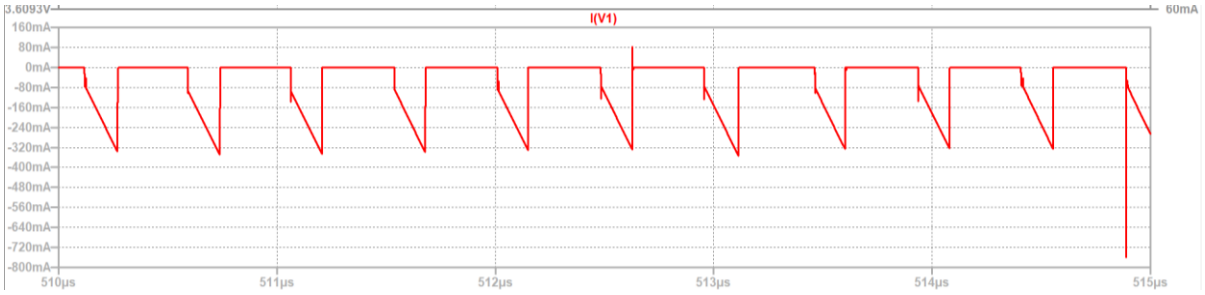


Figure A-23: I_{IN} from 4.51ms to 4.52ms (S-S) Showing Input Current Switching

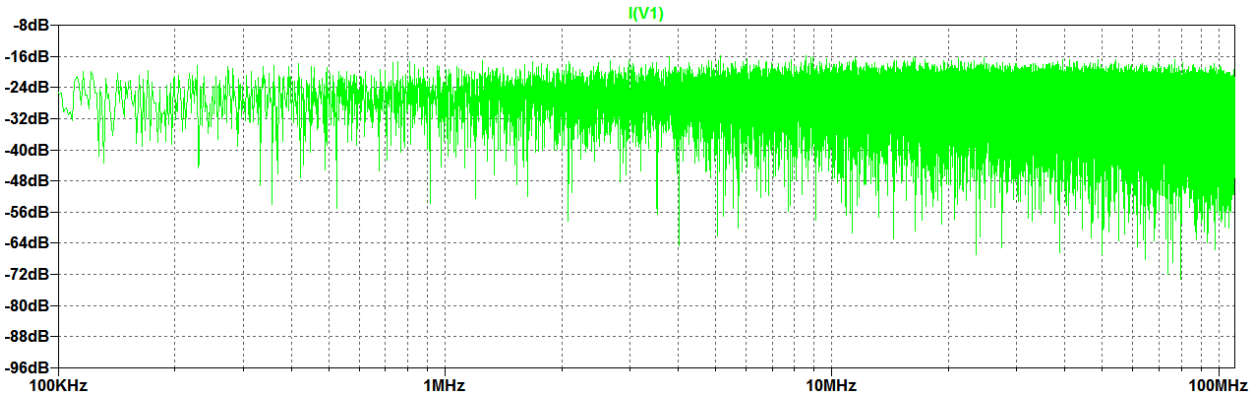


Figure A-24: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 7: 40% Load +/- 1% SSFM at V_{IN} = 12V

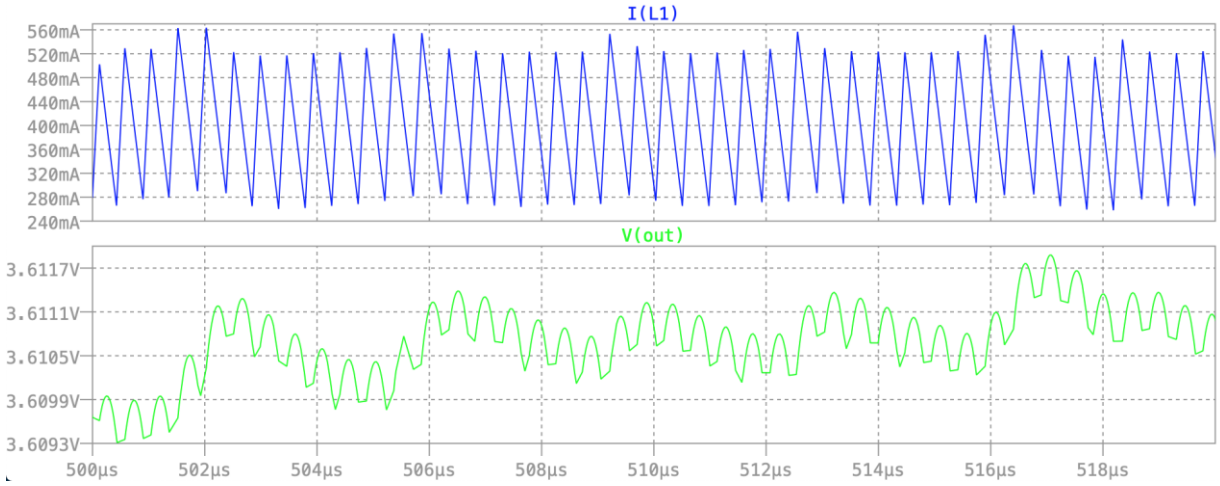


Figure A-25: V_o and $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

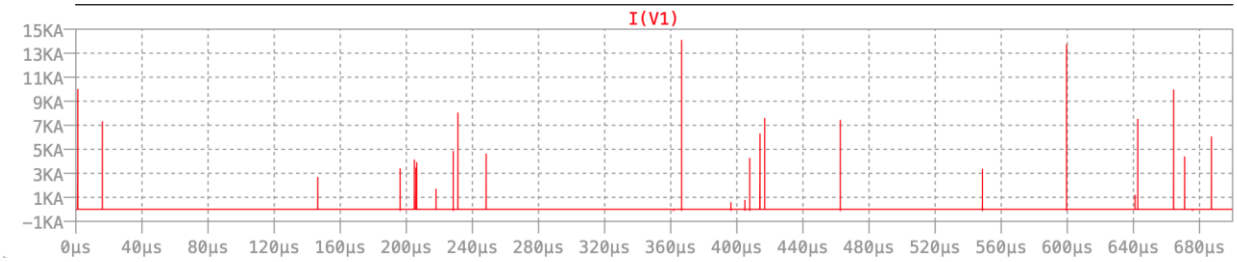


Figure A-26: I_{IN} from 4.5ms to 4.7ms (S-S)

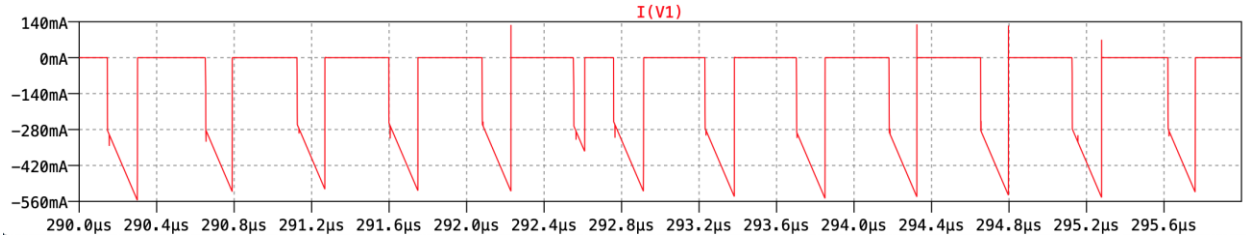


Figure A-27: I_{IN} from 4.51ms to 4.52ms (S-S) Showing Input Current Switching

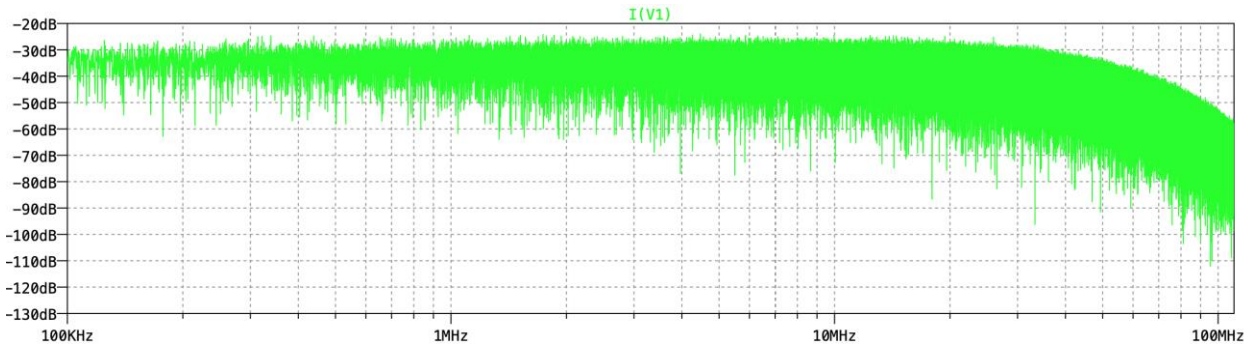


Figure A-28: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 8: 60% Load +/- 1% SSFM at V_{IN} = 12V

Figure A-29: V_o and $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

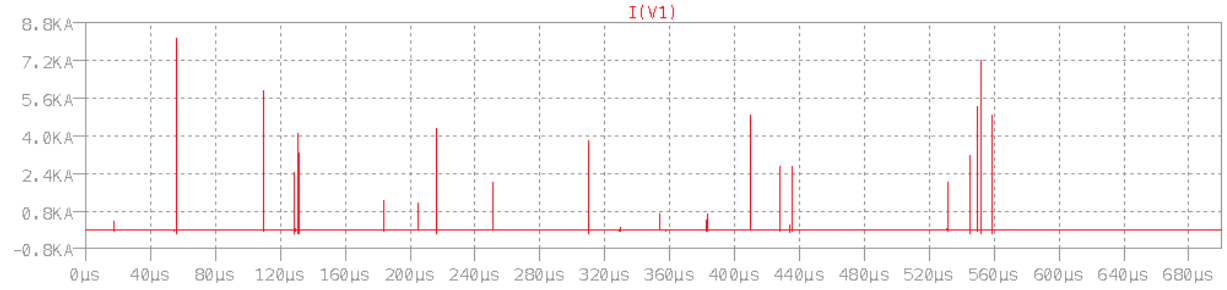


Figure A-30: I_{IN} from 4.5ms to 4.7ms (S-S)

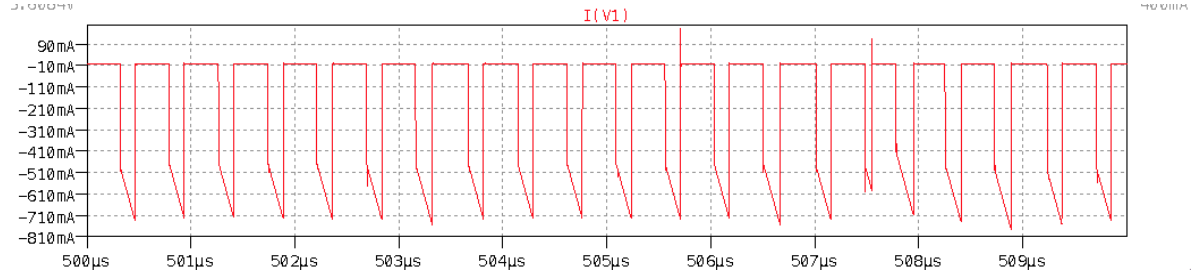


Figure A-31: I_{IN} from 4.51ms to 4.52ms (S-S) Showing Input Current Switching

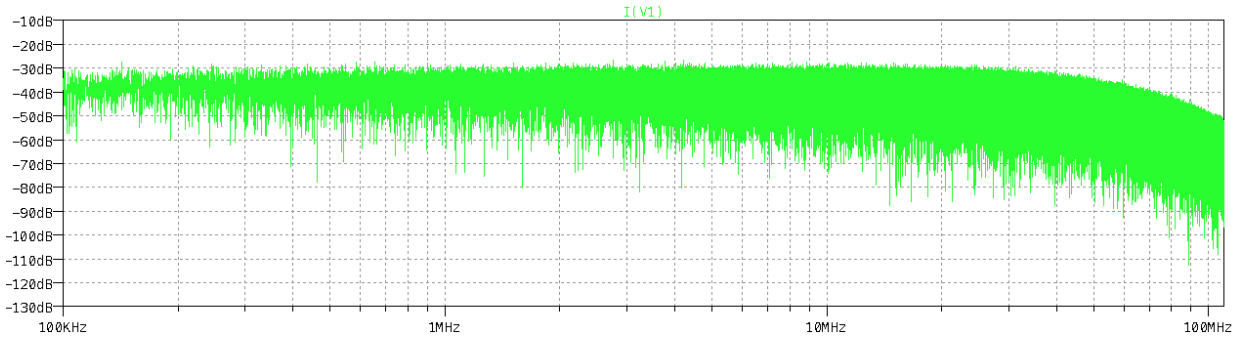


Figure A-32: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 9: 80% Load +/- 1% SSFM at V_{IN} = 12V

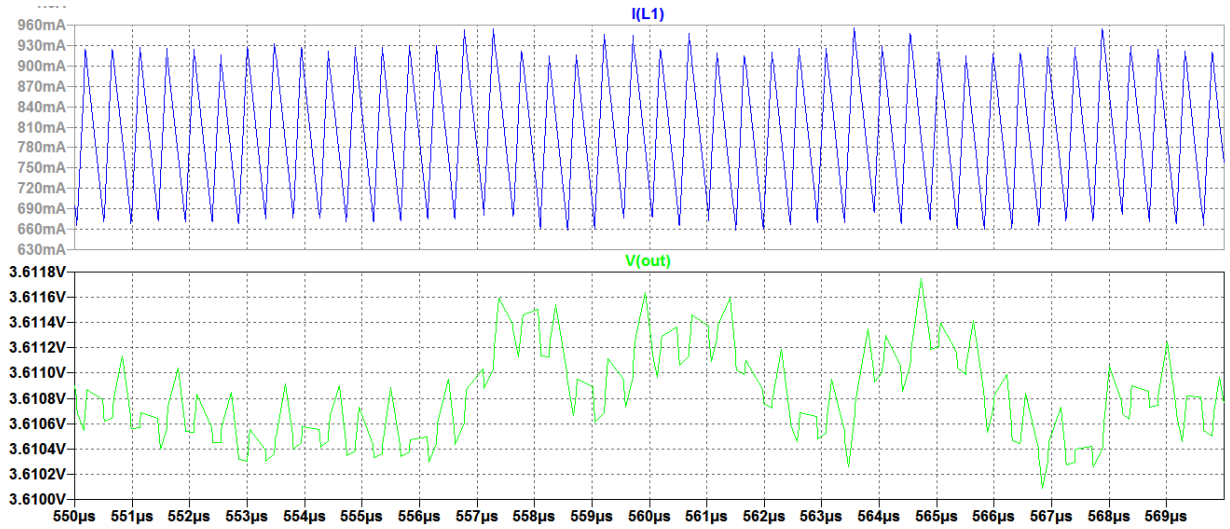


Figure A-33: V_o and $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

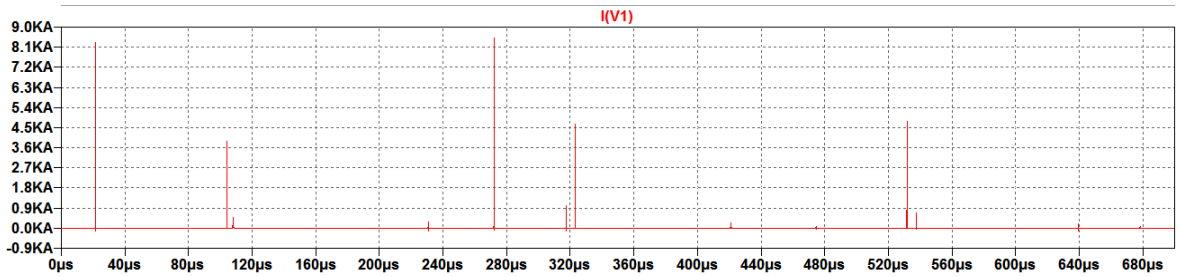


Figure A-34: I_{IN} from 4.5ms to 4.7ms (S-S)

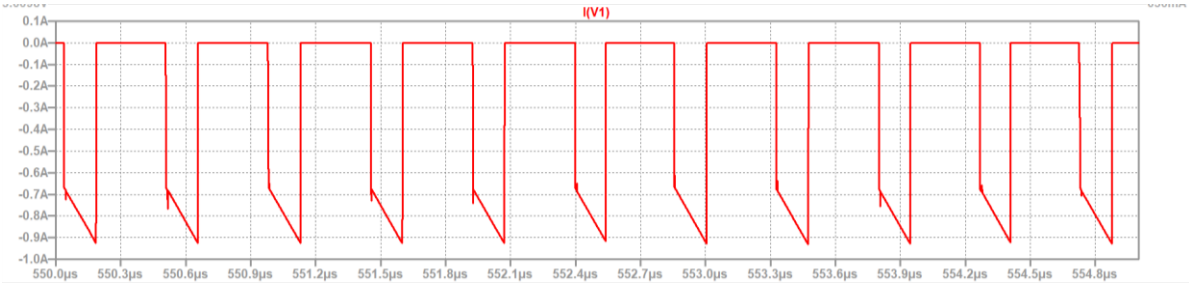


Figure A-35: I_{IN} from 4.51ms to 4.52ms (S-S) Showing Input Current Switching

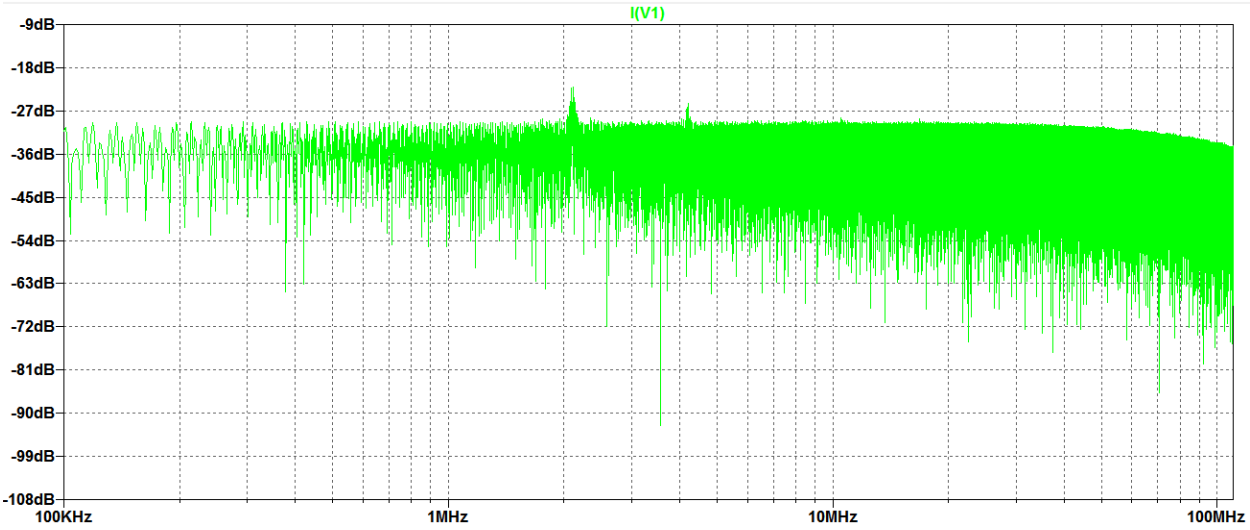


Figure A-36: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 10: Full Load (1A) +/- 1% SSFM at V_{IN} = 12V

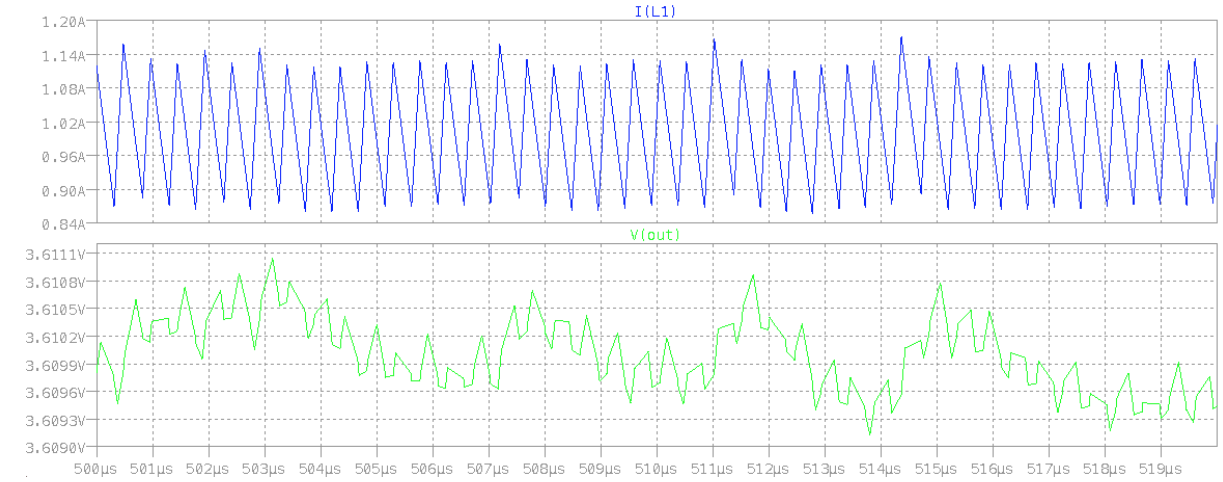


Figure A-37: V_o and $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

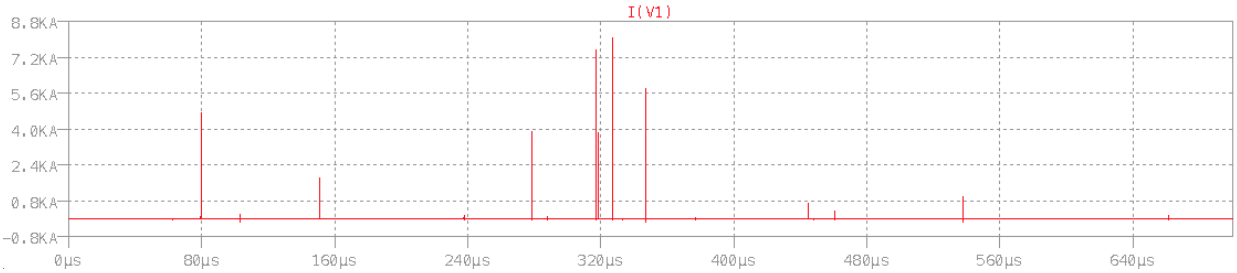


Figure A-38: I_{IN} from 4.5ms to 4.7ms (S-S)

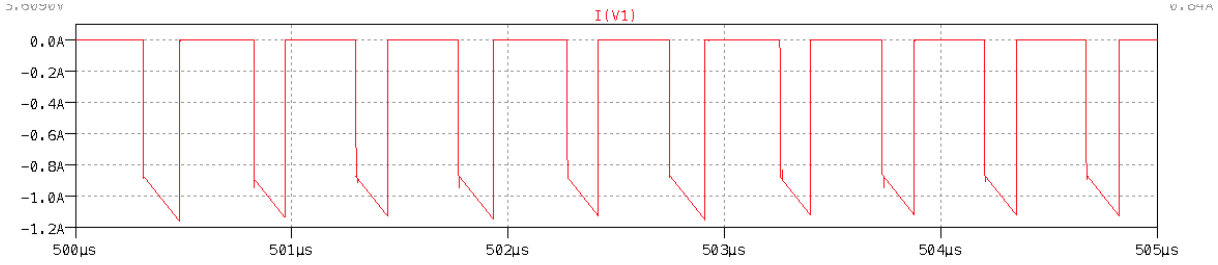


Figure A-39: I_{IN} from 4.51ms to 4.52ms (S-S) Showing Input Current Switching

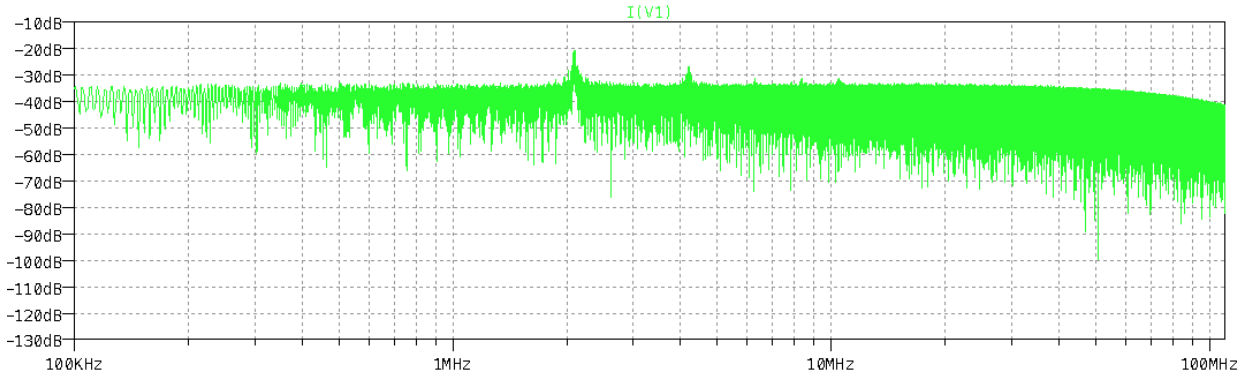


Figure A-40: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 11: 20% Load +/- 4% SSFM at V_{IN} = 12V

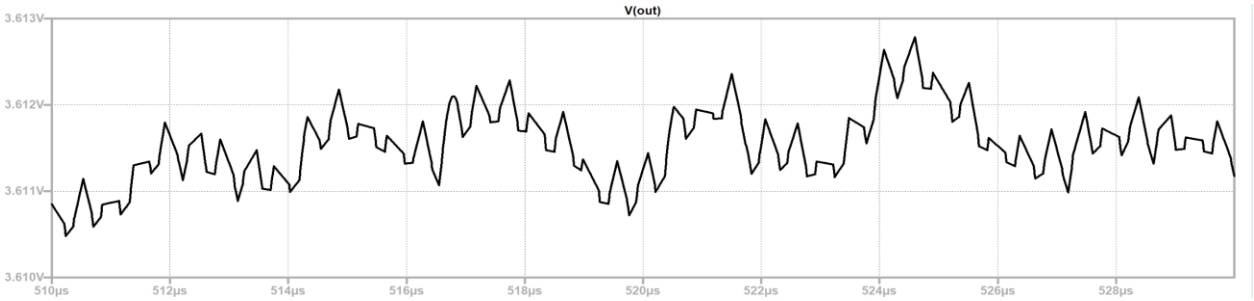


Figure A-41: V_o from 4.5ms to 4.52ms (S-S)

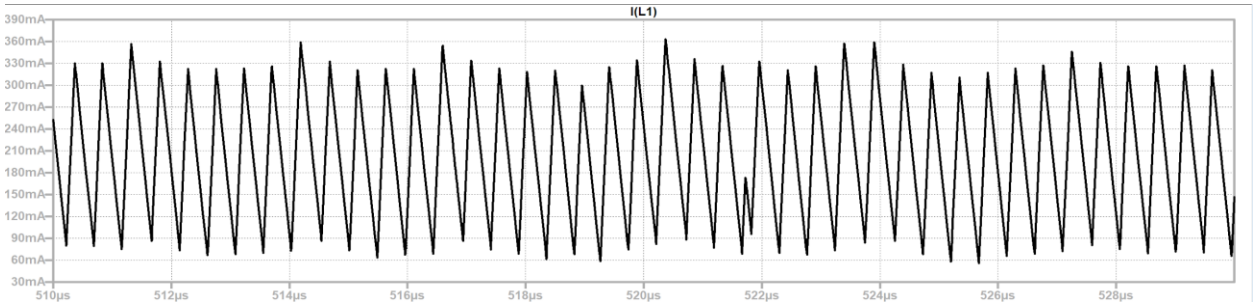


Figure A-42: $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

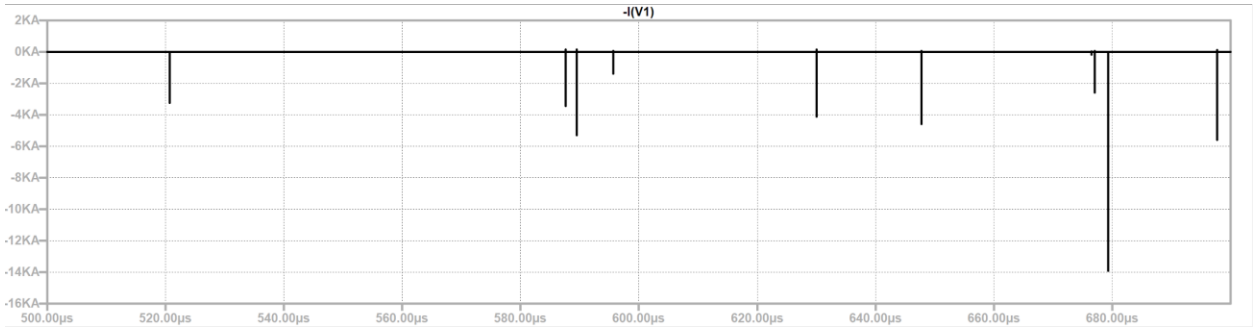


Figure A-43: I_{IN} from 4.5ms to 4.7ms (S-S)

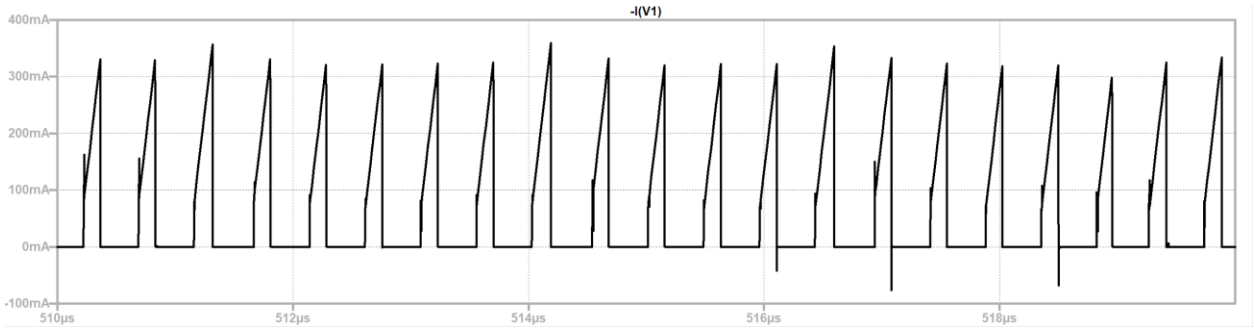


Figure A-44: I_{IN} from 4.51ms to 4.52ms (S-S) Showing Input Current Switching

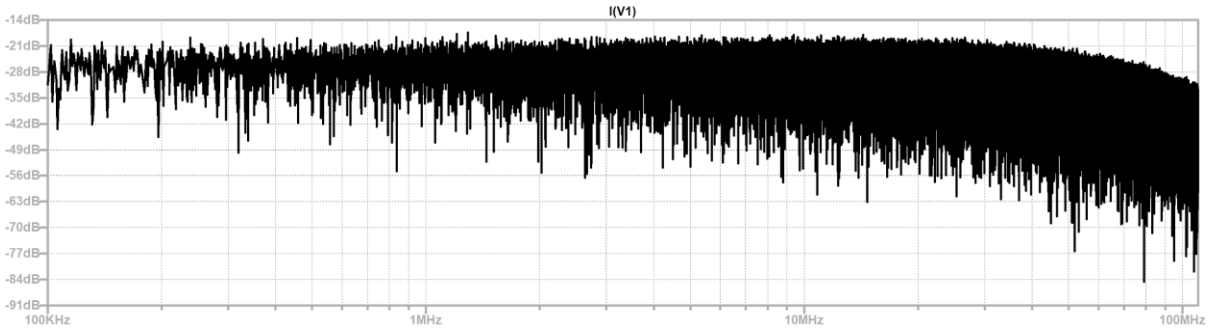


Figure A-45: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 12: 40% Load +/- 4% SSFM at V_{IN} = 12V

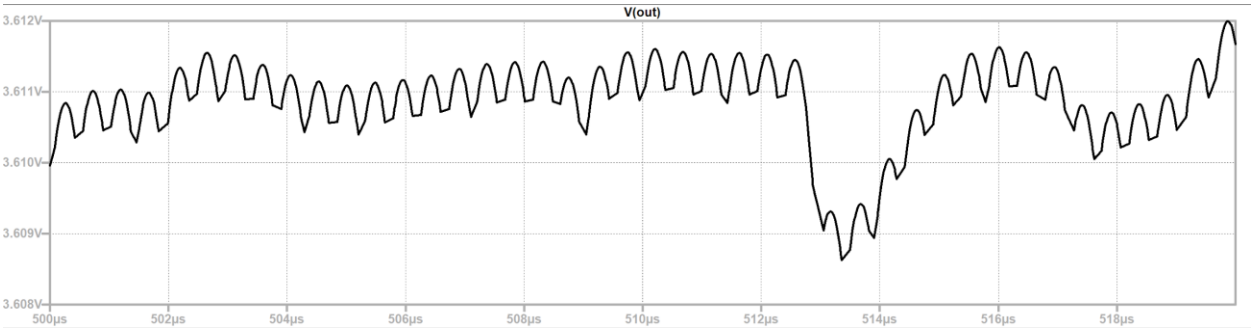


Figure A-46: V_o from 4.5ms to 4.52ms (S-S)

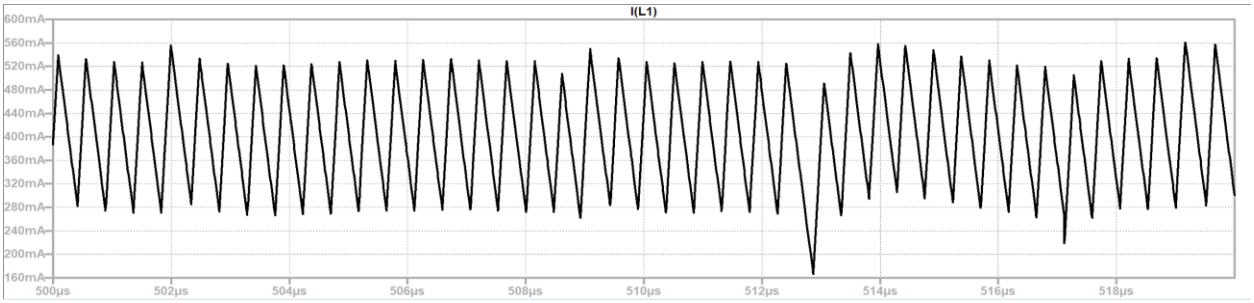


Figure A-47: $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

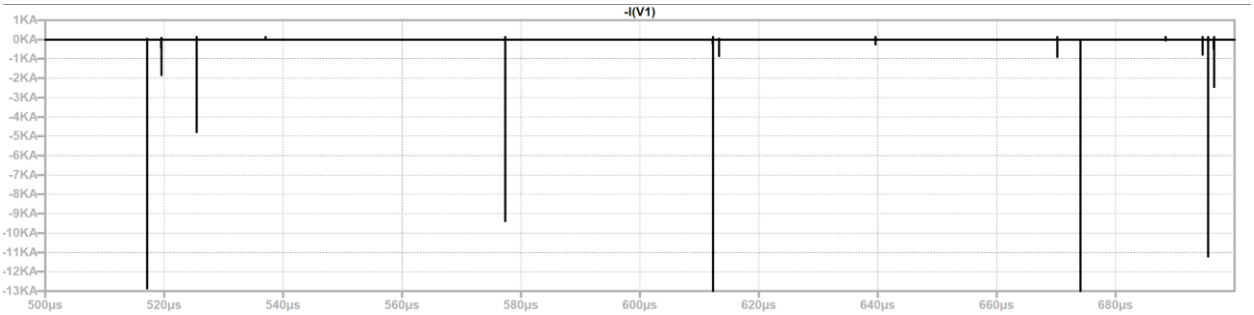


Figure A-48: I_{IN} from 4.5ms to 4.7ms (S-S)

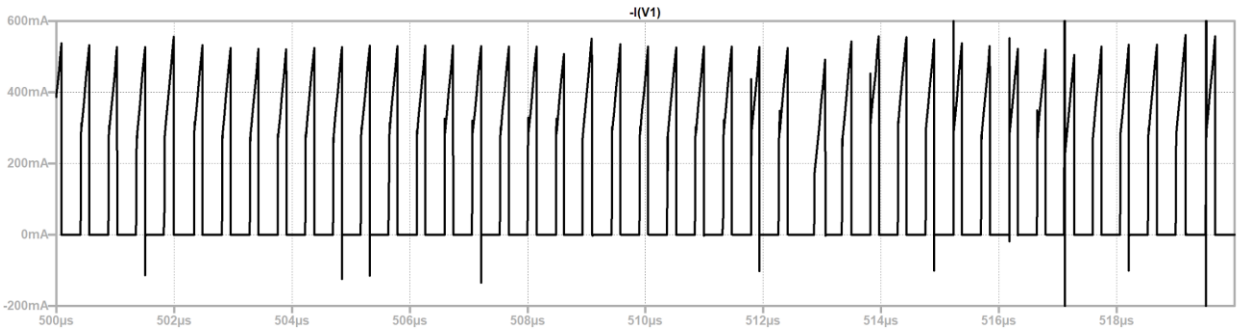


Figure A-49: I_{IN} from 4.5ms to 4.52ms (S-S) Showing Input Current Switching

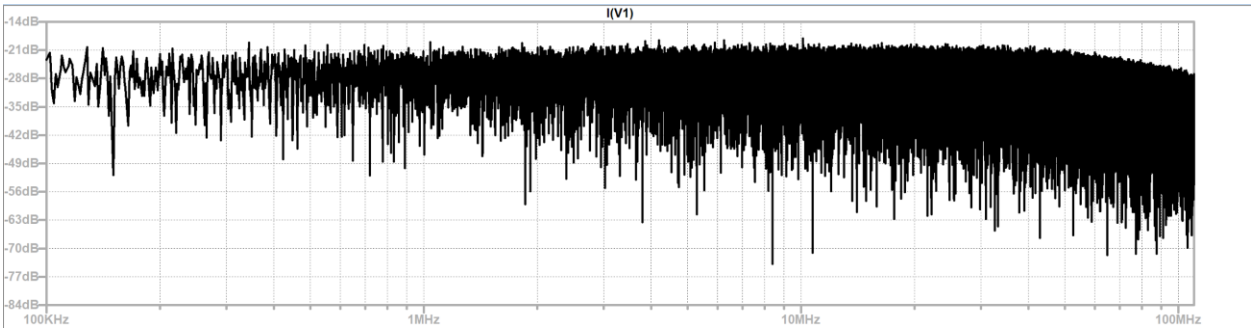


Figure A-50: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 13: 60% Load +/- 4% SSFM at V_{IN} = 12V

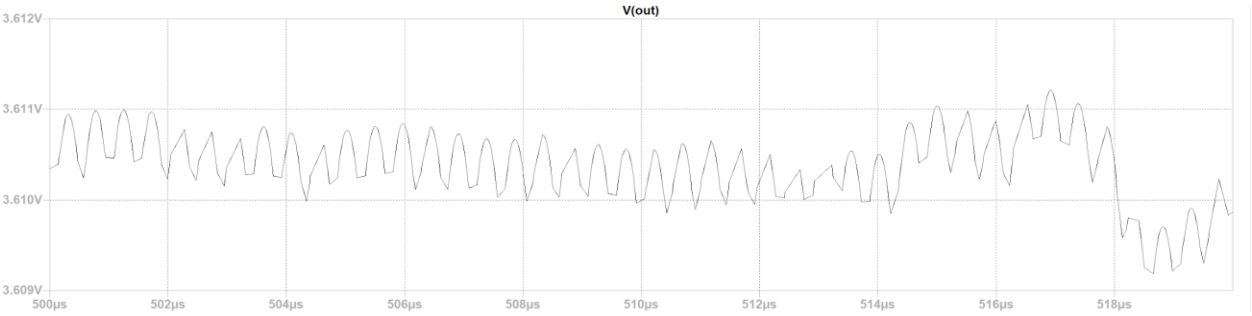


Figure A-51: V_o from 4.5ms to 4.52ms (S-S)

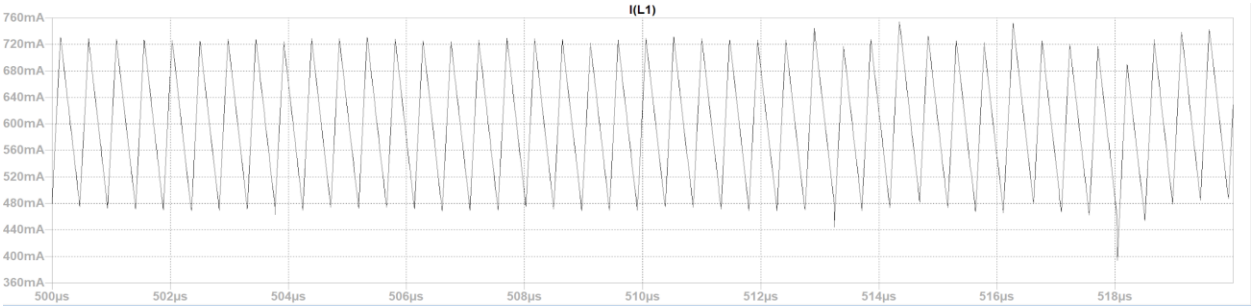


Figure A-52: $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

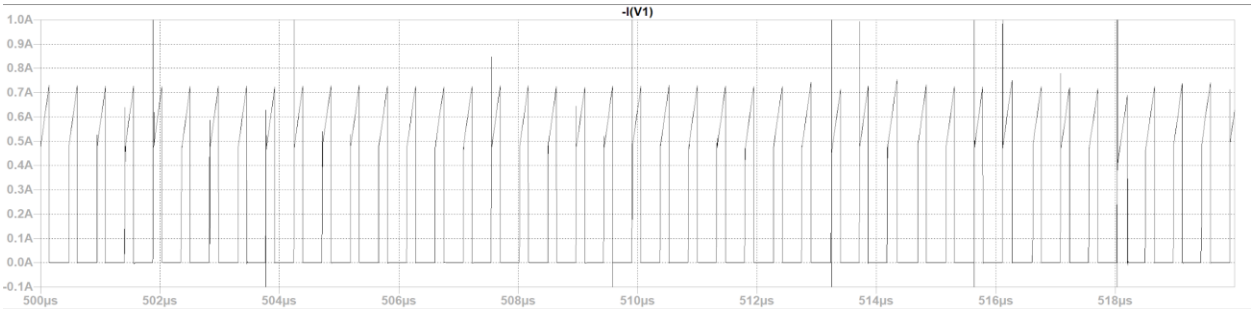


Figure A-53: I_{IN} from 4.51ms to 4.52ms (S-S) Showing Input Current Switching

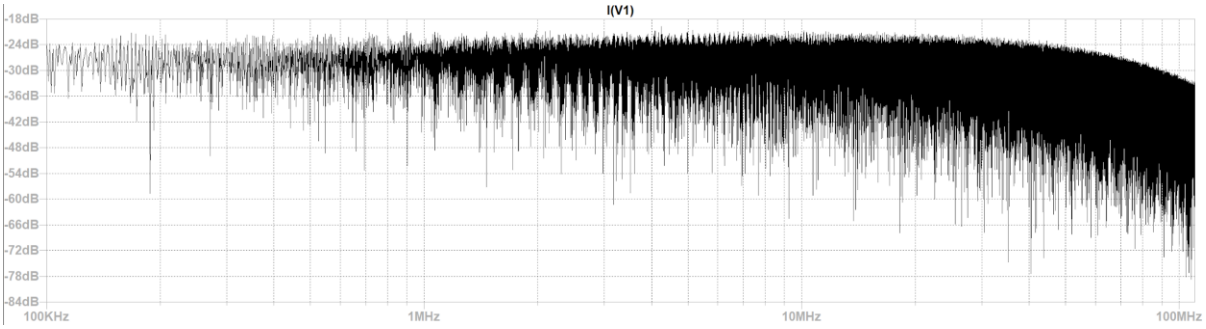


Figure A-54: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 14: 80% Load +/- 4% SSFM at V_{IN} = 12V

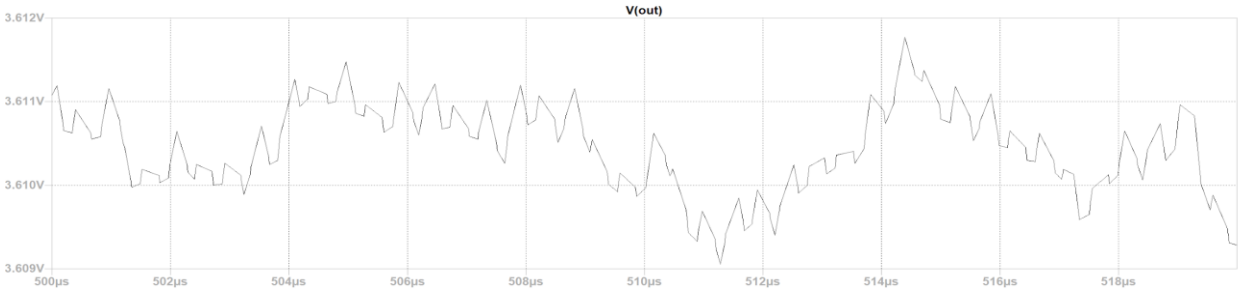


Figure A-55: V_o from 4.5ms to 4.52ms (S-S)

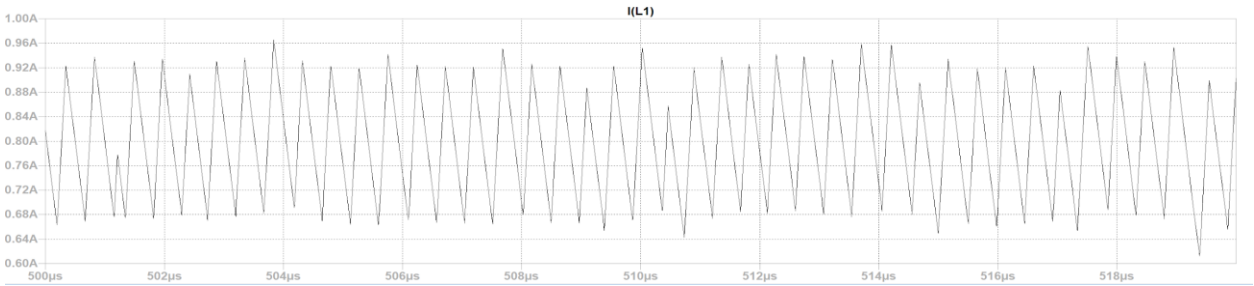


Figure A-56: $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

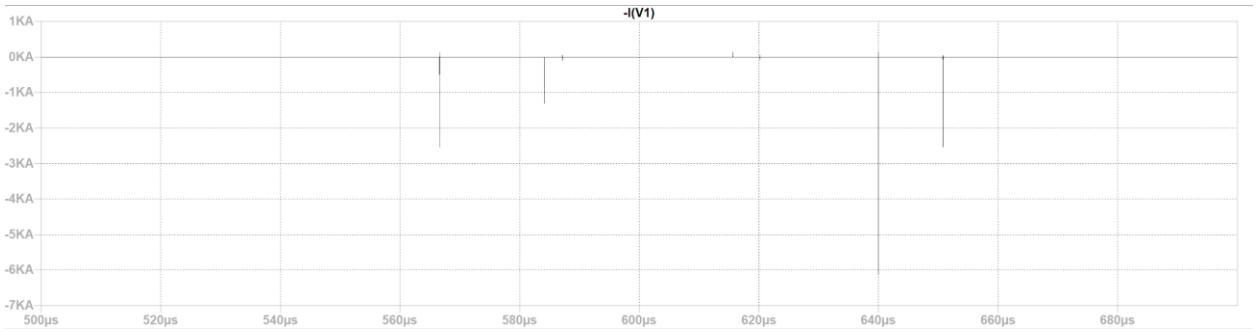


Figure A-57: I_{IN} from 4.5ms to 4.7ms (S-S)

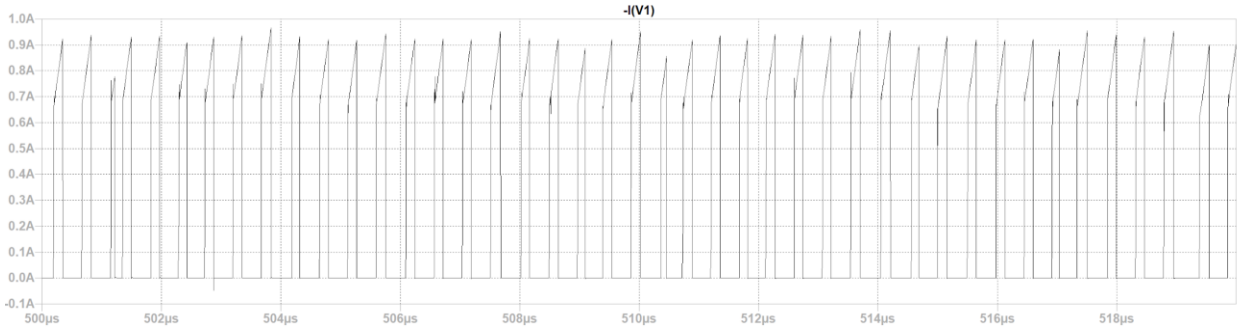


Figure A-58: I_{IN} from 4.5ms to 4.52ms (S-S) Showing Input Current Switching

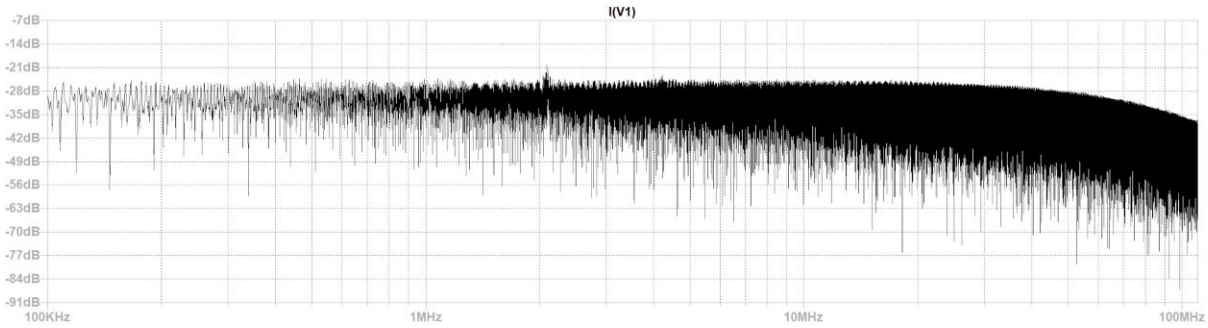


Figure A-59: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 15: Full Load (1A) +/- 4% SSFM at V_{IN} = 12V

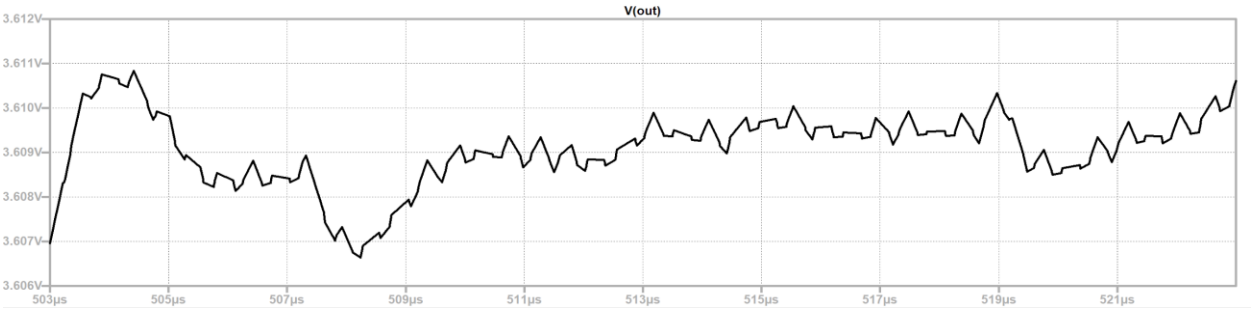


Figure A-60: V_o from 4.5ms to 4.52ms (S-S)

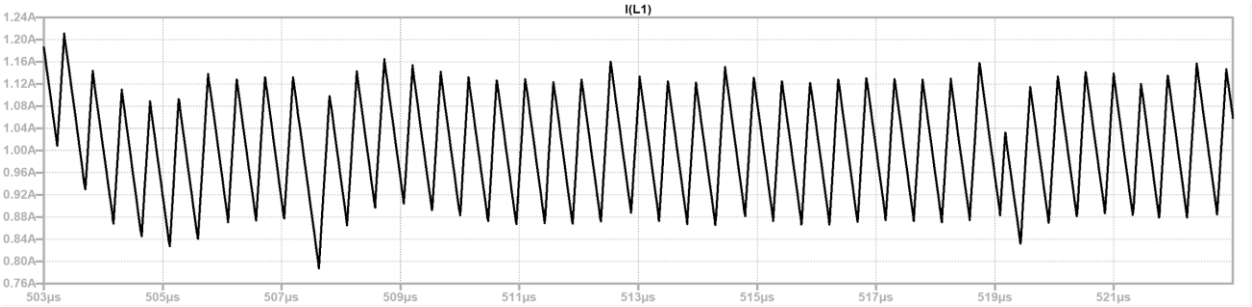


Figure A-61: $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

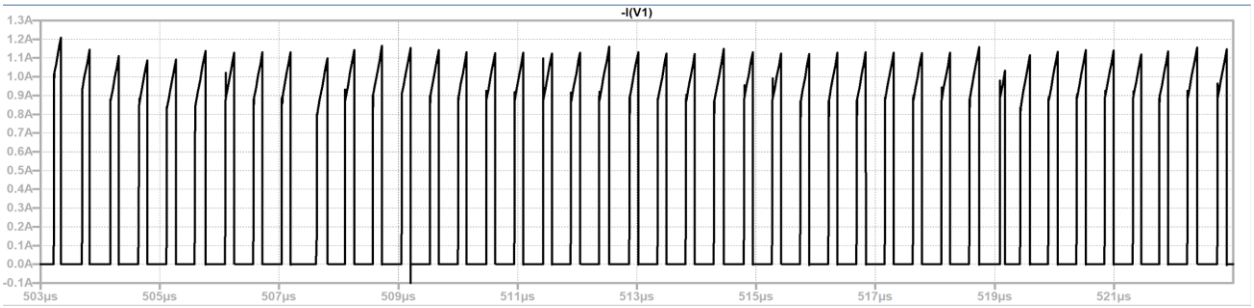


Figure A-62: I_{IN} from 4.5ms to 4.52ms (S-S) Showing Input Current Switching

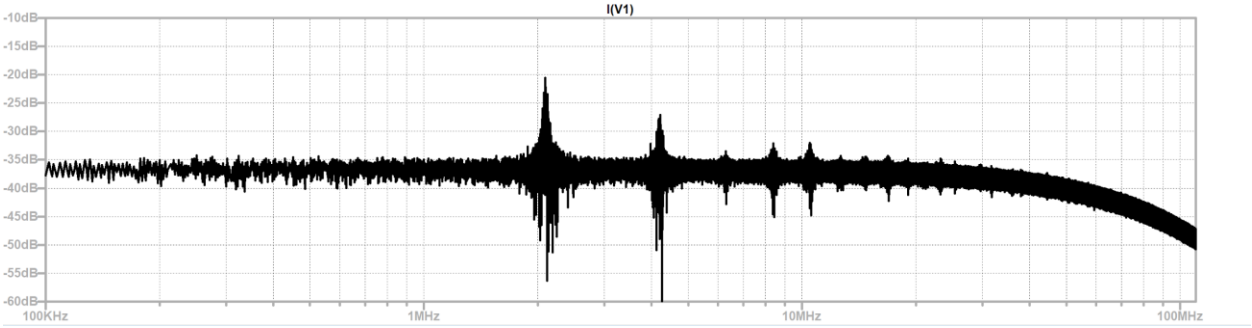


Figure A-63: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 16: 20% Load No SSFM at V_{IN} = 24V

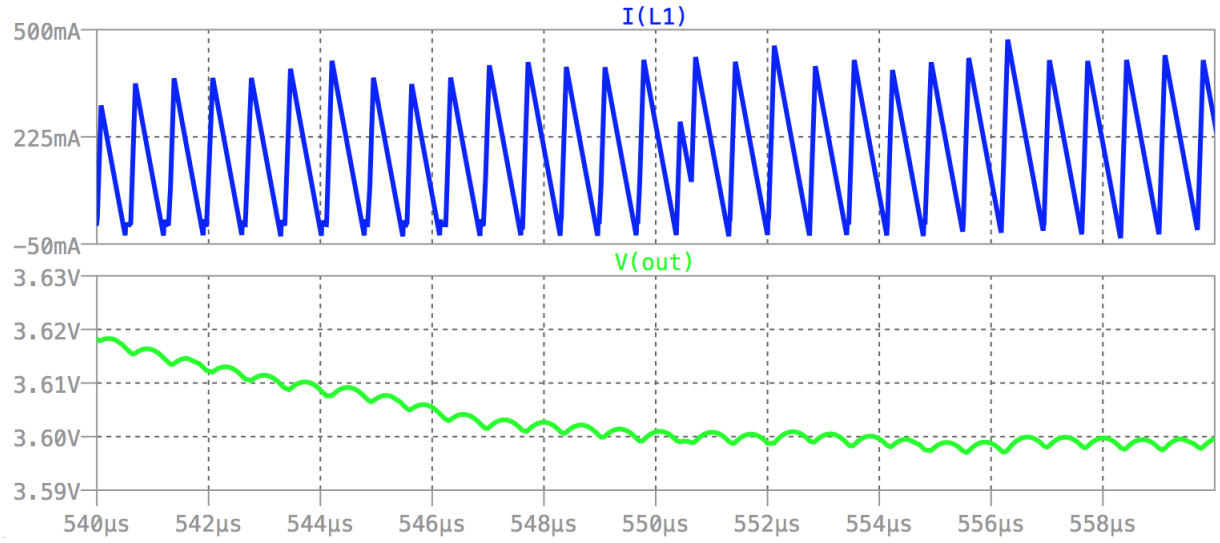


Figure A-64: V_o and $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

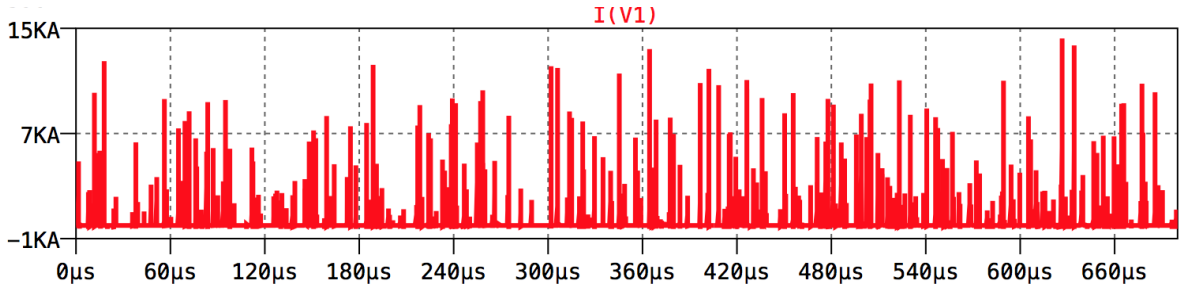


Figure A-65: I_{IN} from 4.5ms to 4.7ms (S-S)

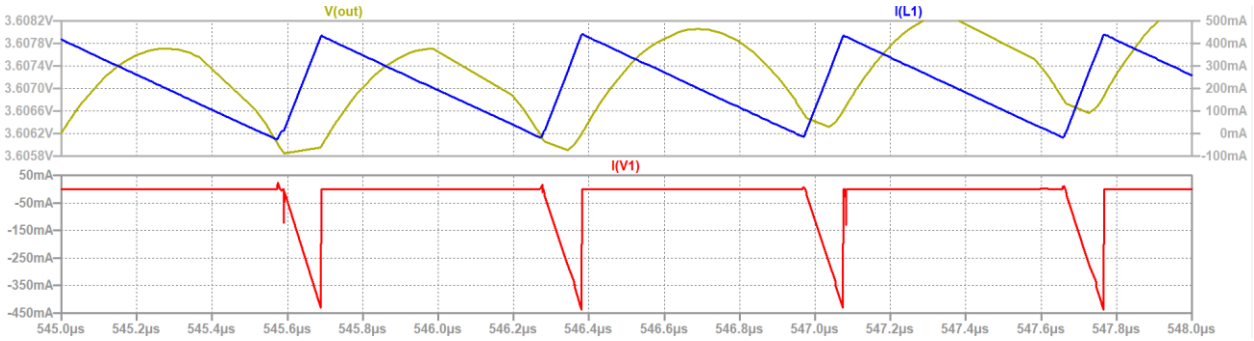


Figure A-66: I_{IN} from 4.51ms to 4.52ms (S-S) Showing Input Current Switching

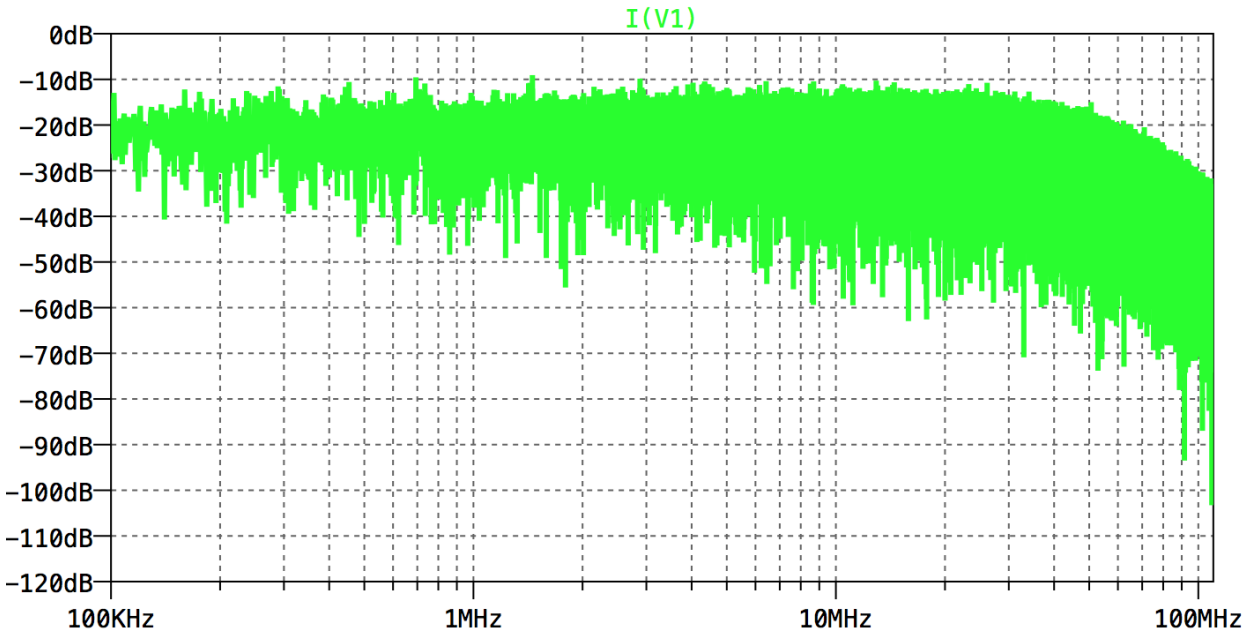


Figure A-67: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 17: 40% Load No SSFM at V_{IN} = 24V

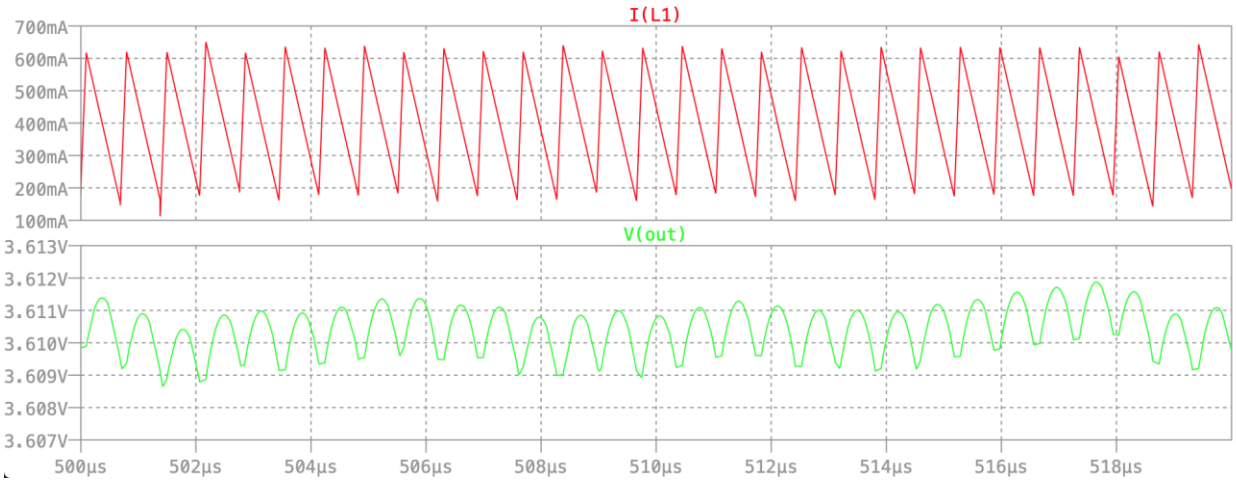


Figure A-68: V_o and $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

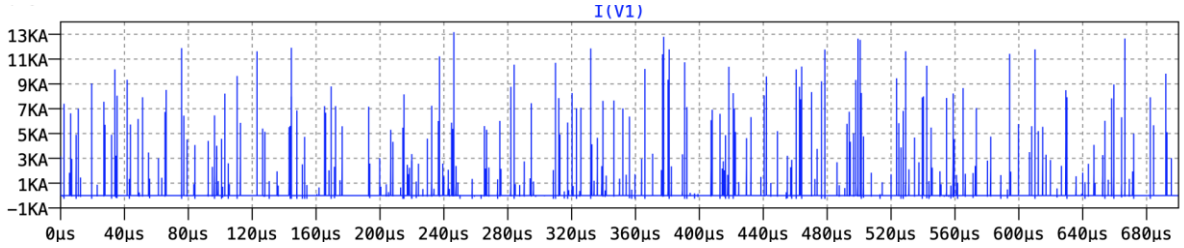


Figure A-69: I_{IN} from 4.5ms to 4.7ms (S-S)

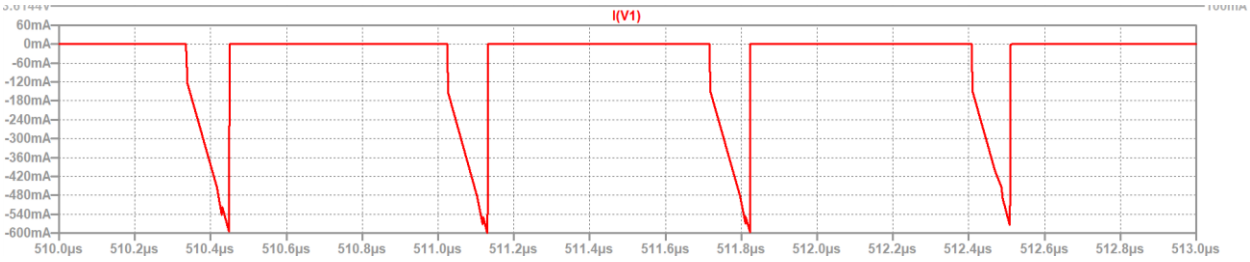


Figure A-70: I_{IN} from 4.51ms to 4.52ms (S-S) Showing Input Current Switching

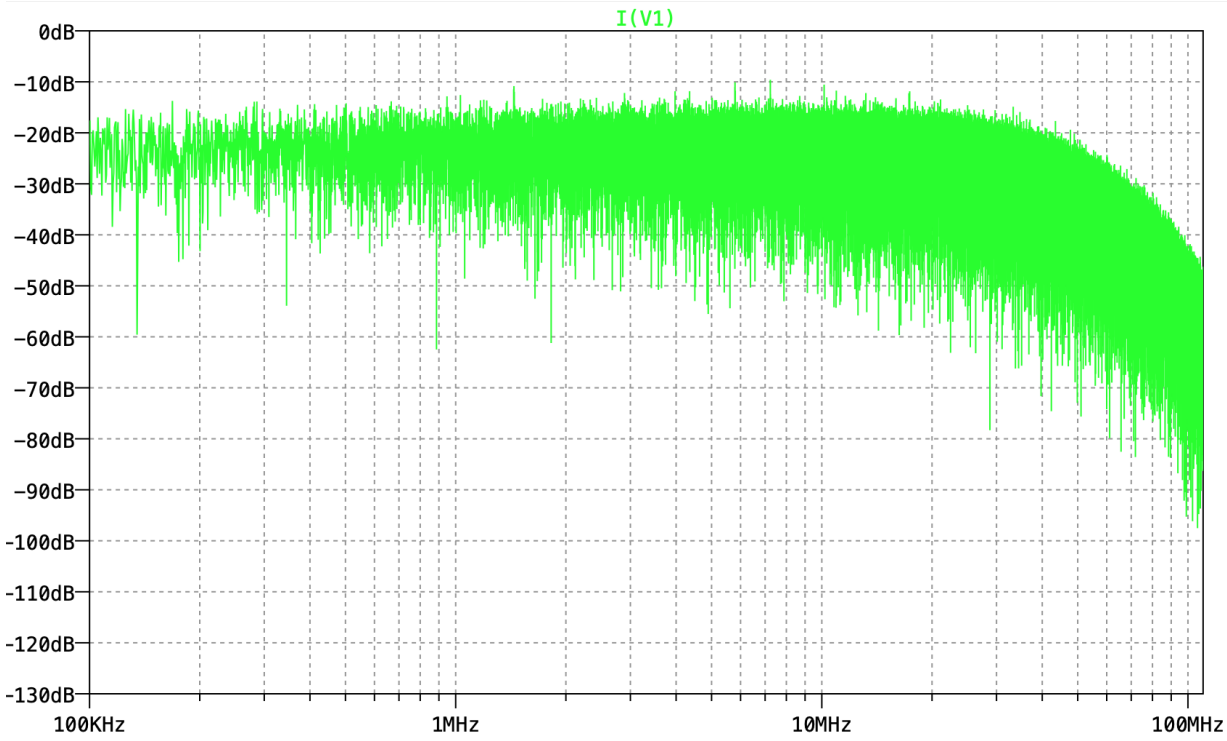


Figure A-71: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 18: 60% Load No SSFM at V_{IN} = 24V

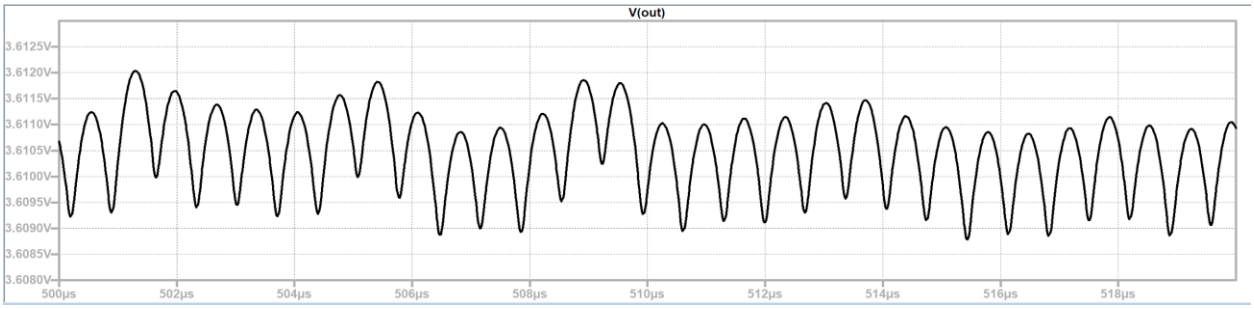


Figure A-72: V_o from 4.5ms to 4.52ms (S-S)

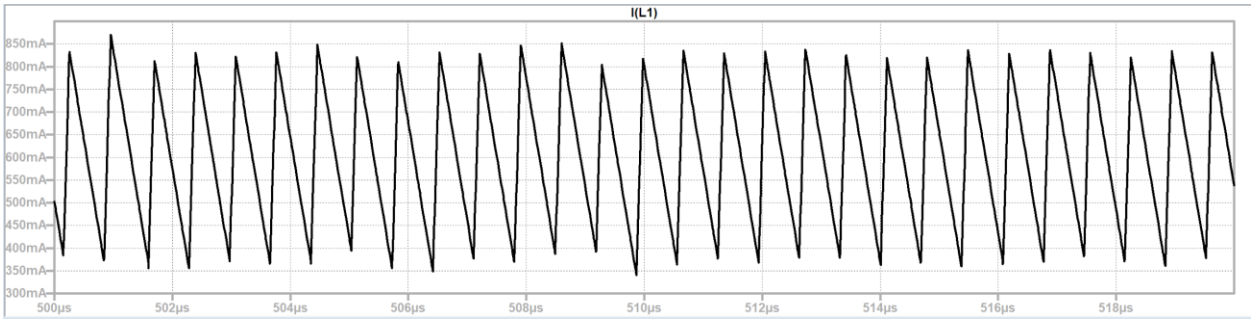


Figure A-73: $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

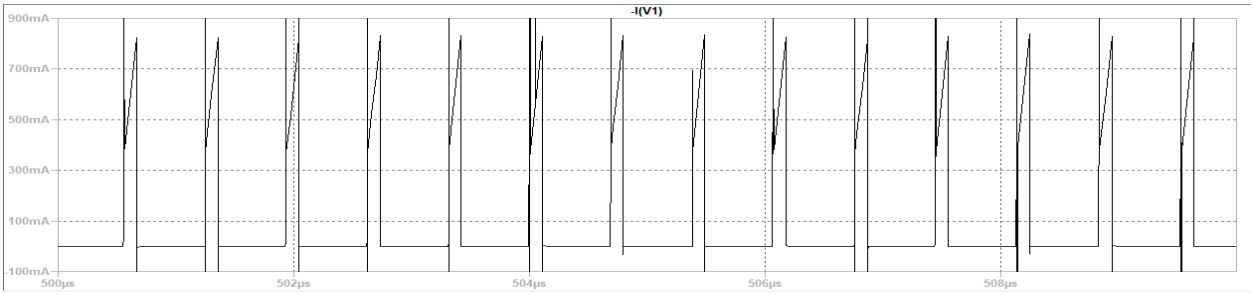


Figure A-74: I_{IN} from 4.5ms to 4.51ms (S-S) Showing Input Current Switching

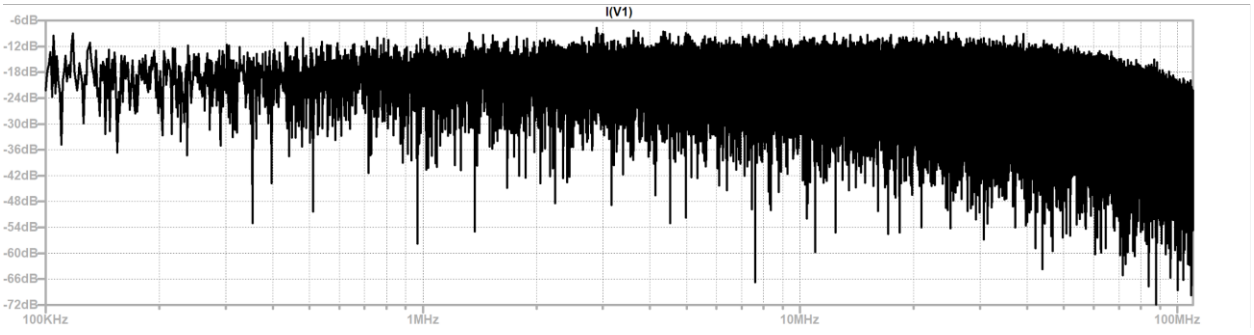


Figure A-75: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 19: 80% Load No SSFM at V_{IN} = 24V

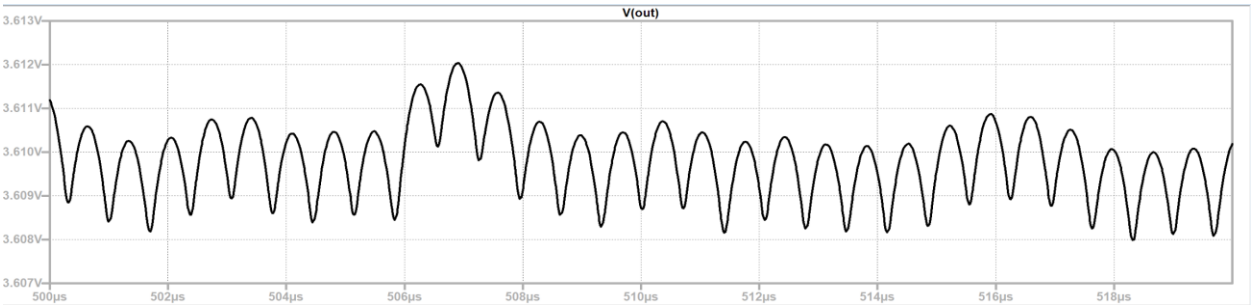


Figure A-76: V_o from 4.5ms to 4.52ms (S-S)

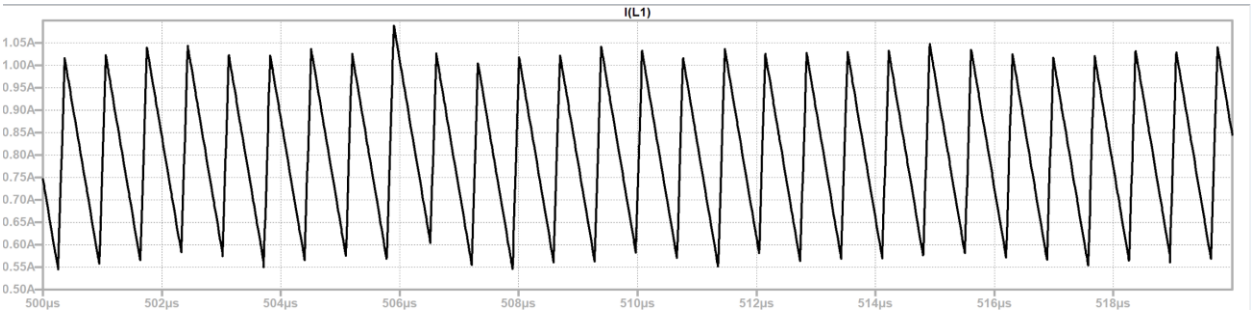


Figure A-77: $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

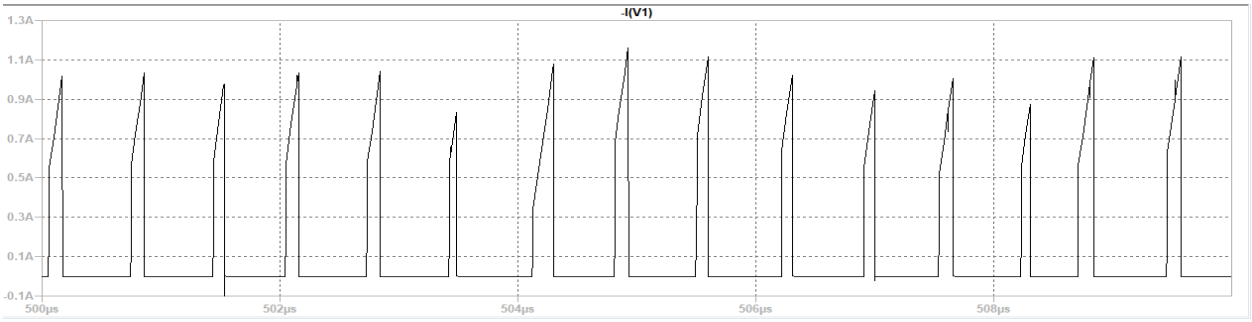


Figure A-78: I_{IN} from 4.5ms to 4.51ms (S-S) Showing Input Current Switching

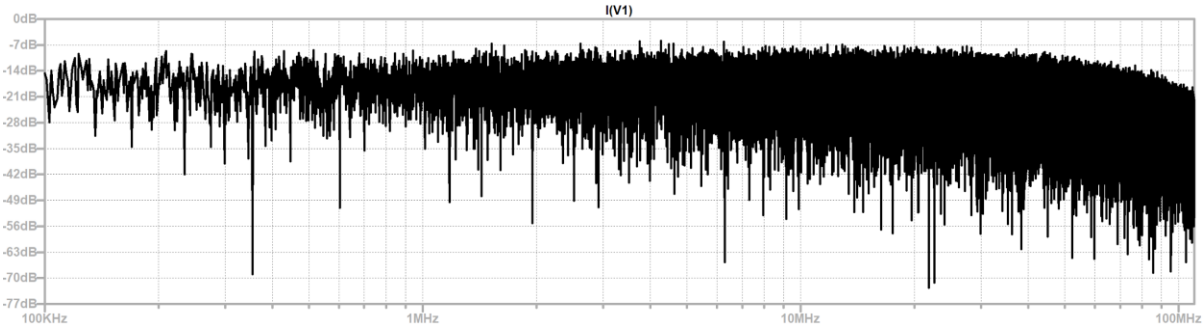


Figure A-79: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 20: Full Load (1A) No SSFM at V_{IN} = 24V

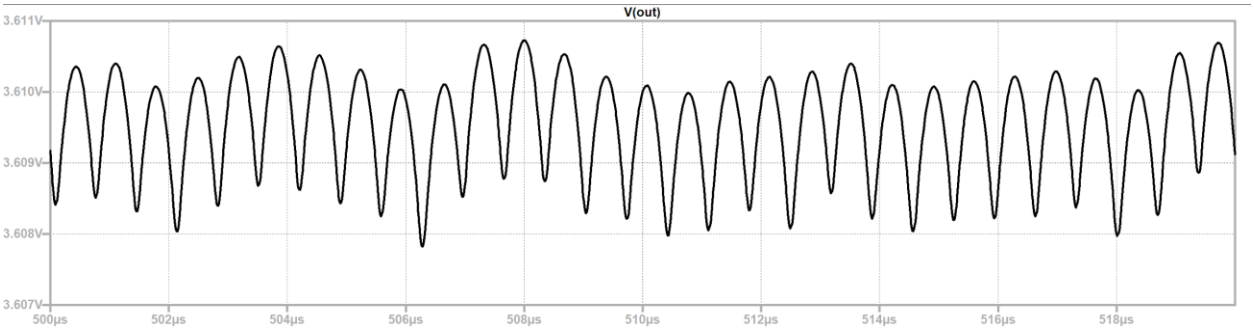


Figure A-80: V_o from 4.5ms to 4.52ms (S-S)

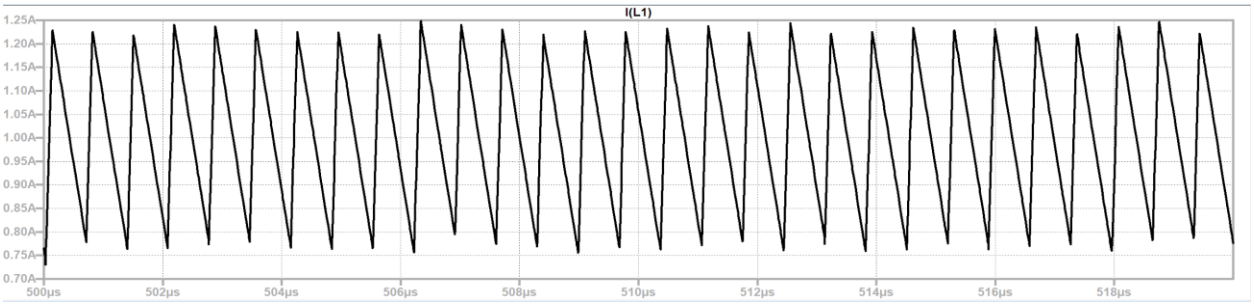


Figure A-81: $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

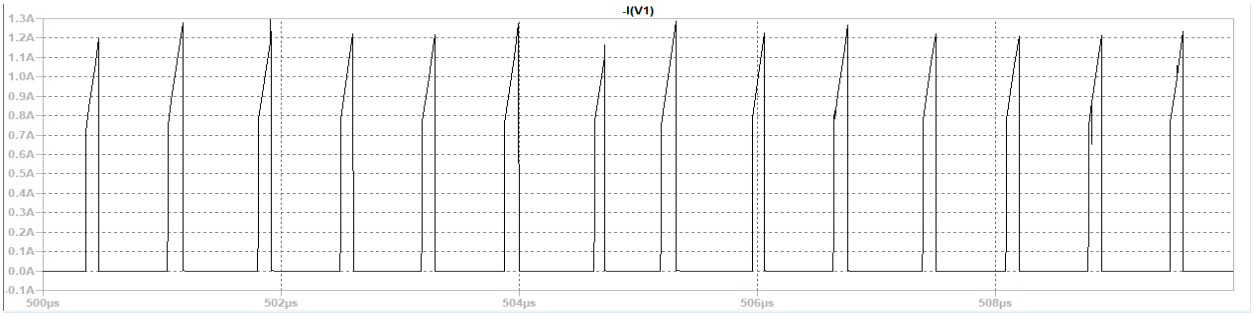


Figure A-82: I_{IN} from 4.5ms to 4.51ms (S-S) Showing Input Current Switching

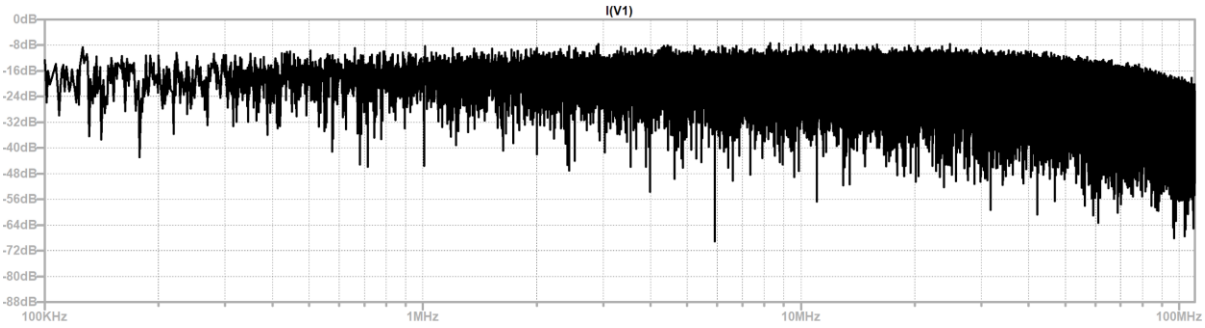


Figure A-83: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 21: 20% Load +/- 1% SSFM at V_{IN} = 24V

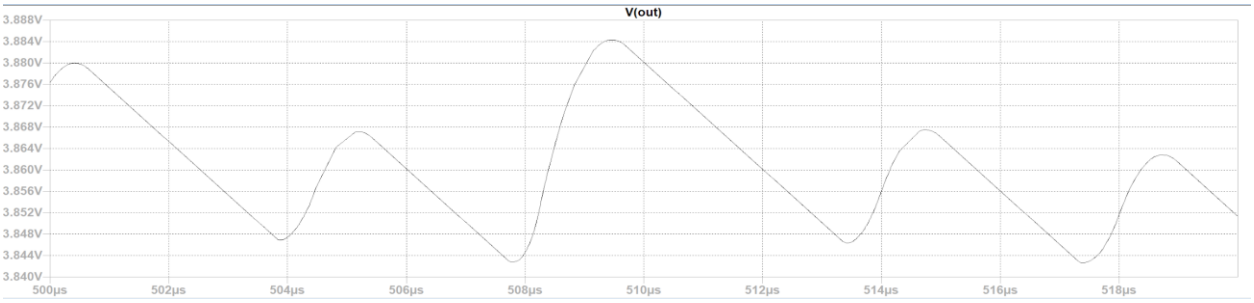


Figure A-84: V_o from 4.5ms to 4.52ms (S-S)

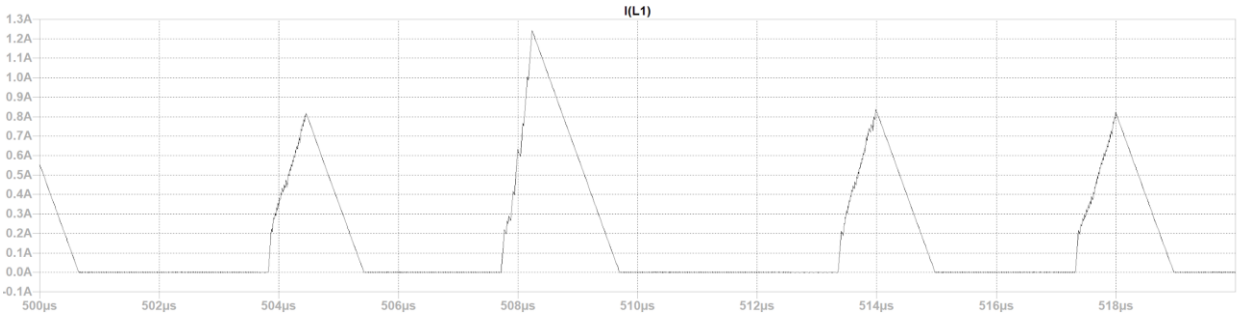


Figure A-85: $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

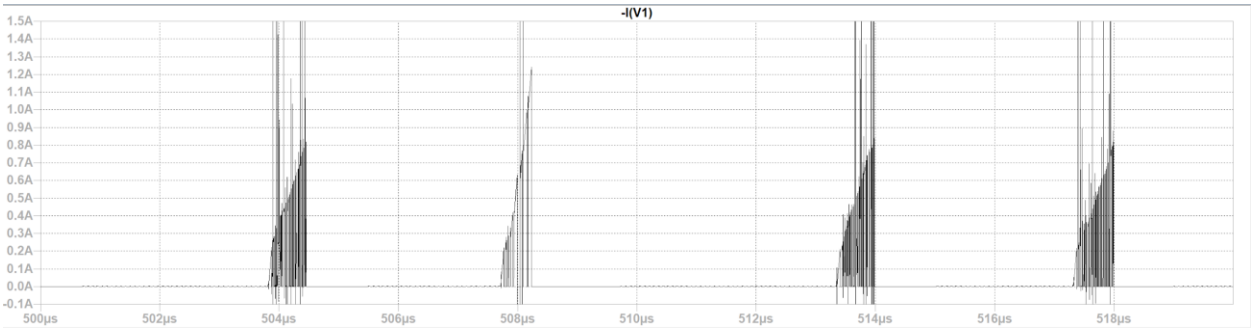


Figure A-86: I_{IN} from 4.5ms to 4.52ms (S-S) Showing Input Current Switching

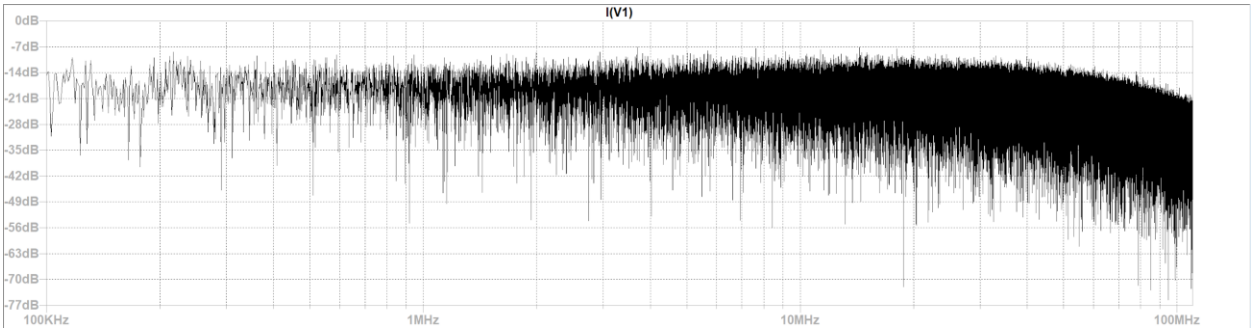


Figure A-87: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 22: 40% Load +/- 1% SSFM at V_{IN} = 24V

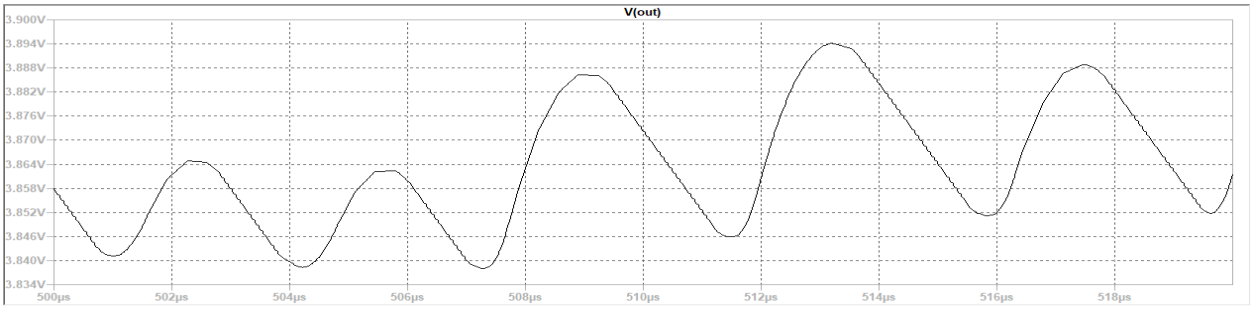


Figure A-88: V_o from 4.5ms to 4.52ms (S-S)

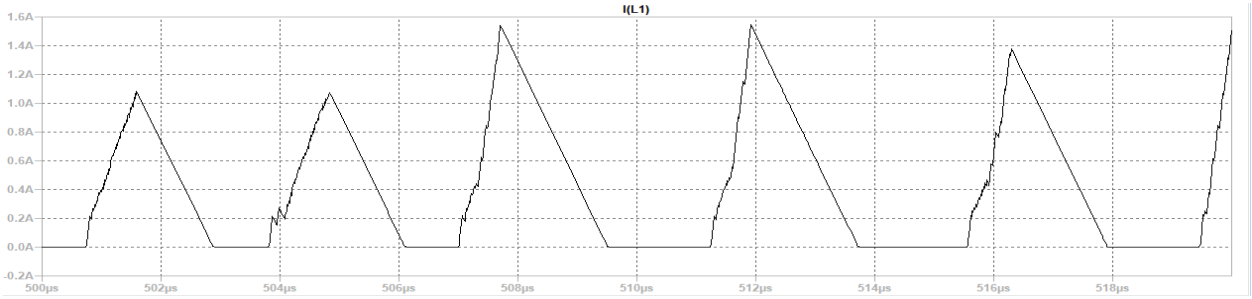


Figure A-89: $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

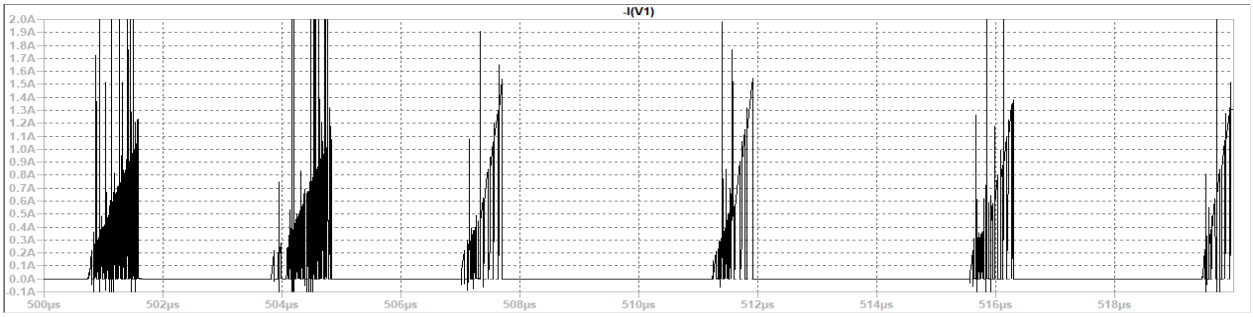


Figure A-90: I_{IN} from 4.5ms to 4.52ms (S-S) Showing Input Current Switching

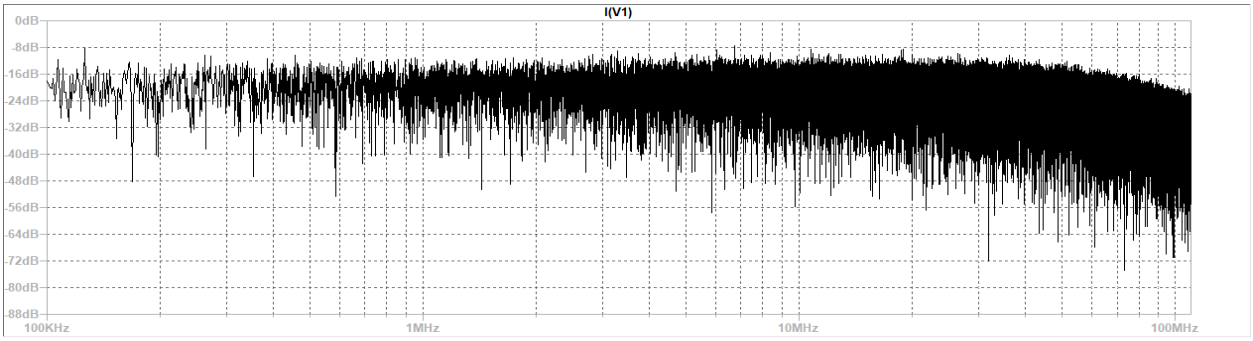


Figure A-91: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 23: 60% Load +/- 1% SSFM at V_{IN} = 24V

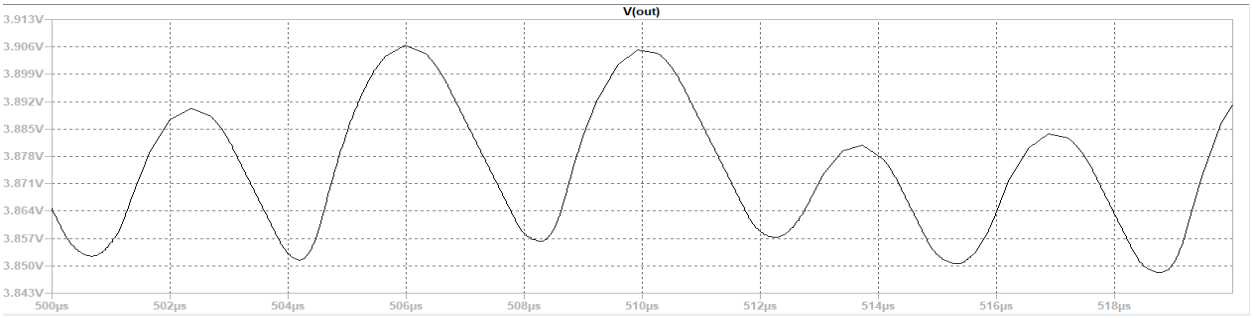


Figure A-92: V_o from 4.5ms to 4.52ms (S-S)

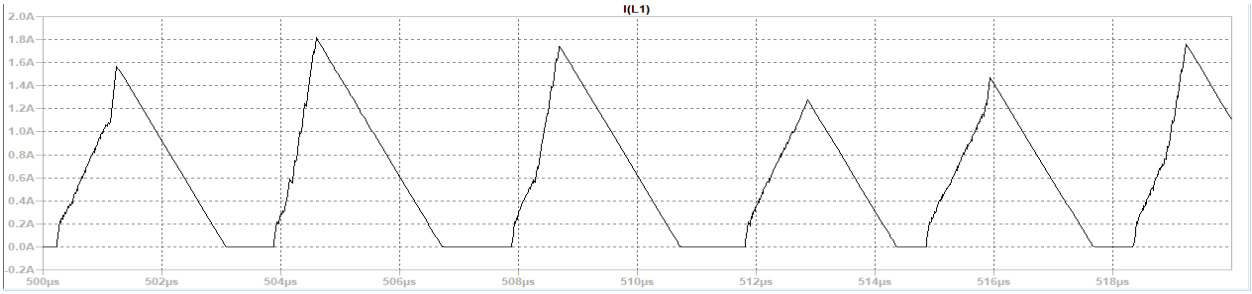


Figure A-93: $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

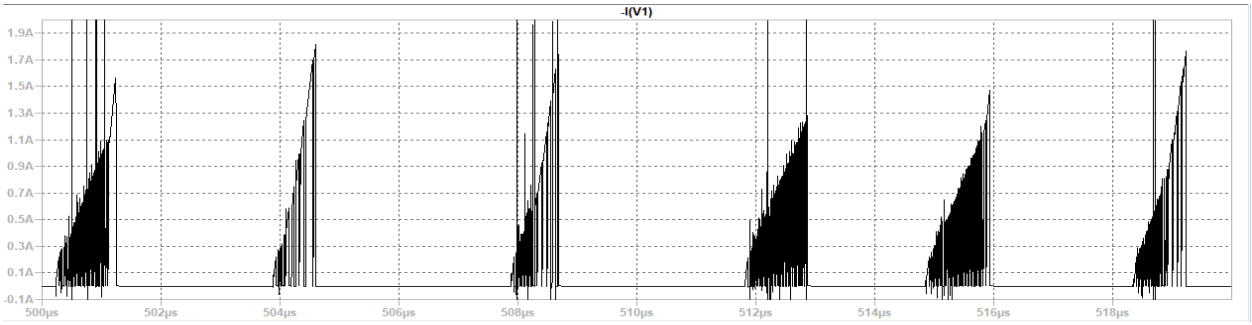


Figure A-94: I_{IN} from 4.5ms to 4.52ms (S-S) Showing Input Current Switching

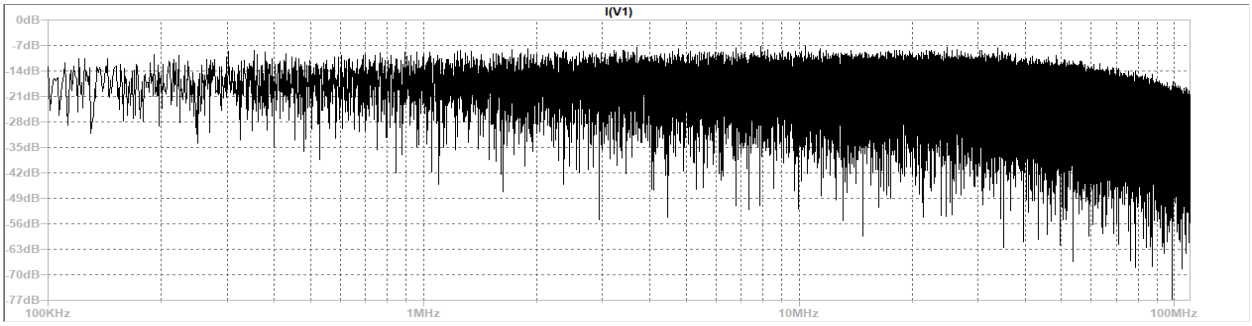


Figure A-95: FFT of I_{IN} from 4ms to 5ms (S-S) 60% 24V 1%

Case 24: 80% Load +/- 1% SSFM at V_{IN} = 24V

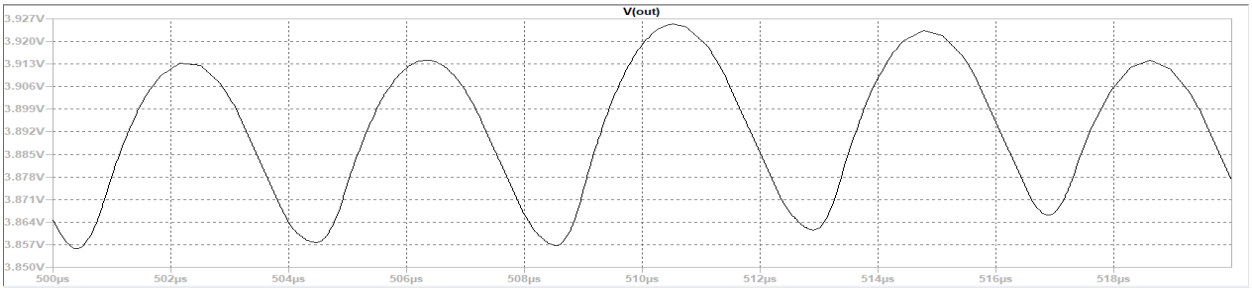


Figure A-96: V_o from 4.5ms to 4.52ms (S-S)

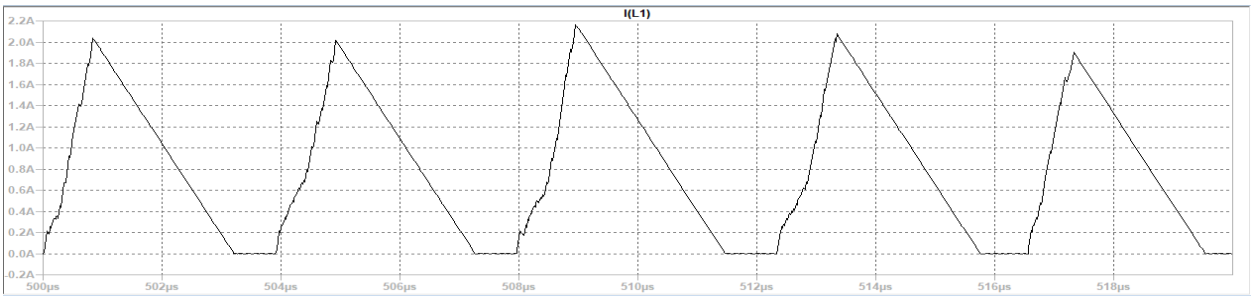


Figure A-97: $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

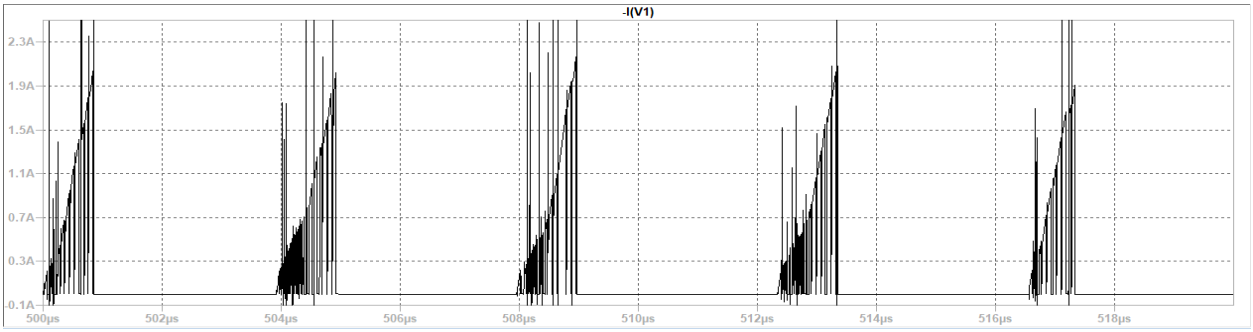


Figure A-98: I_{IN} from 4.5ms to 4.52ms (S-S) Showing Input Current Switching

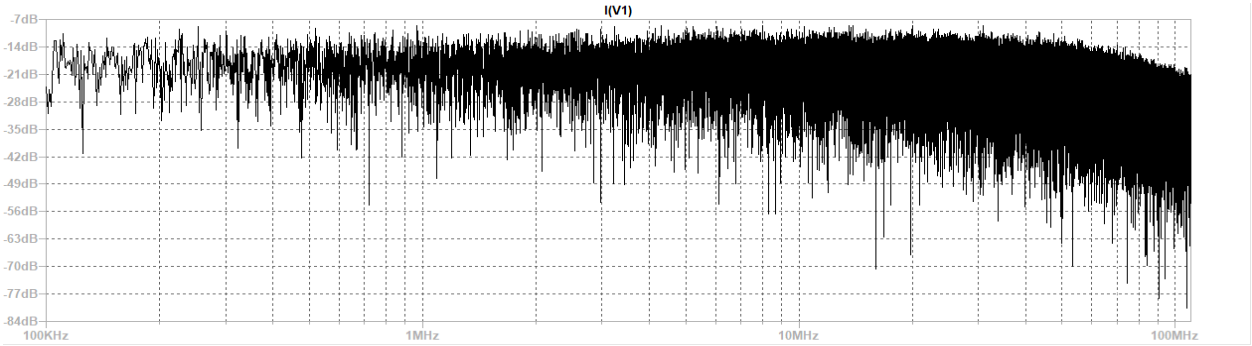


Figure A-99: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 25: Full Load (1A) +/- 1% SSFM at V_{IN} = 24V

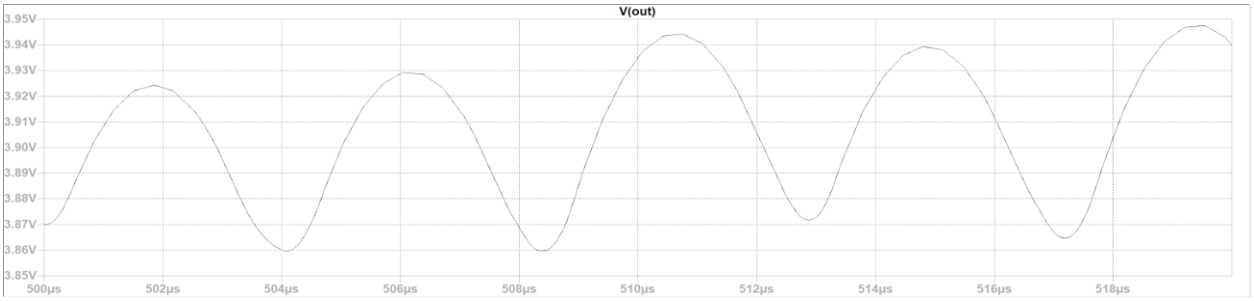


Figure A-100: V_o from 4.5ms to 4.52ms (S-S)

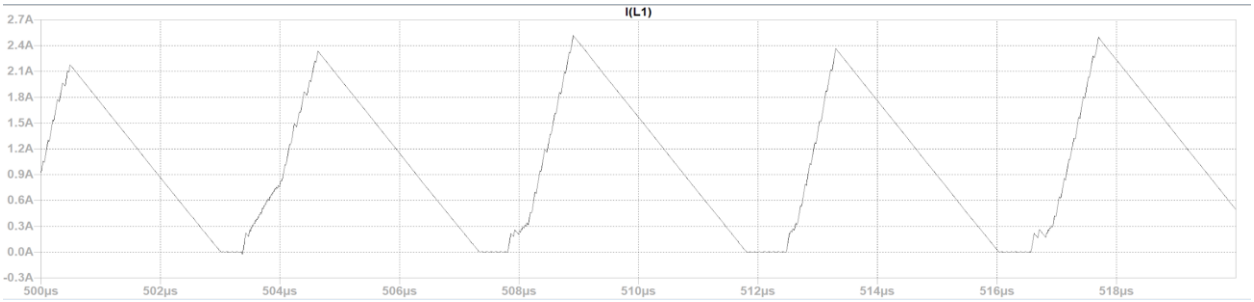


Figure A-101: $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

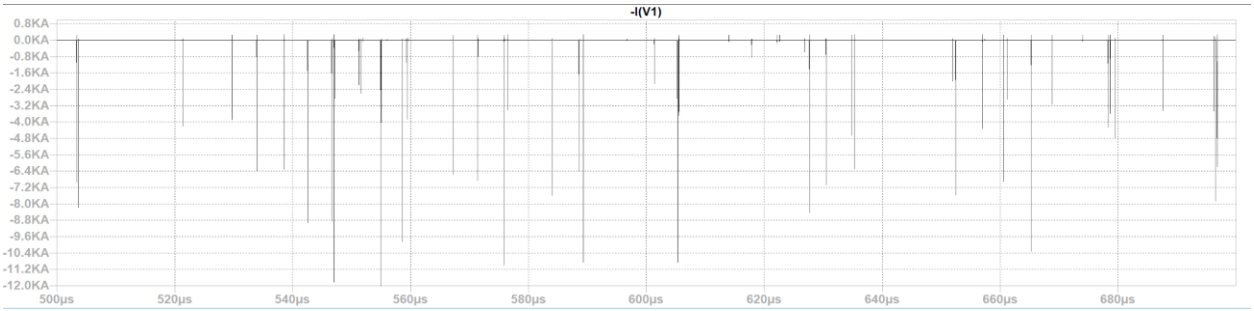


Figure A-102: I_{IN} from 4.5ms to 4.7ms (S-S)

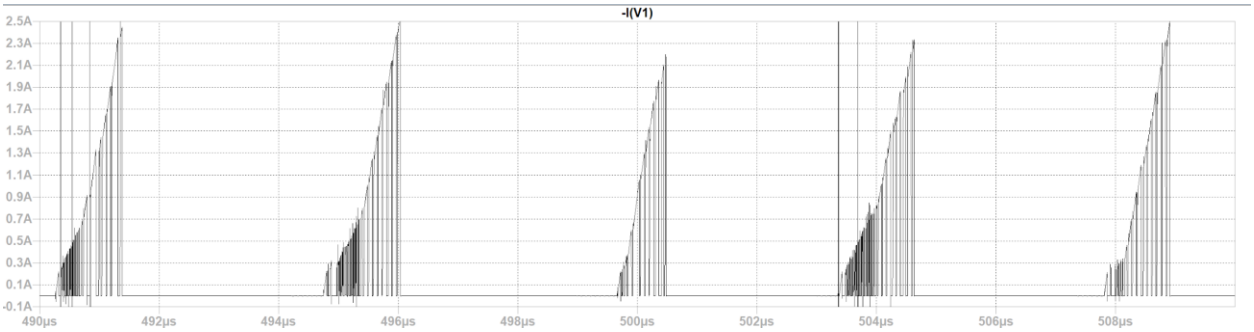


Figure A-103: I_{IN} from 4.49ms to 4.51ms (S-S) Showing Input Current Switching

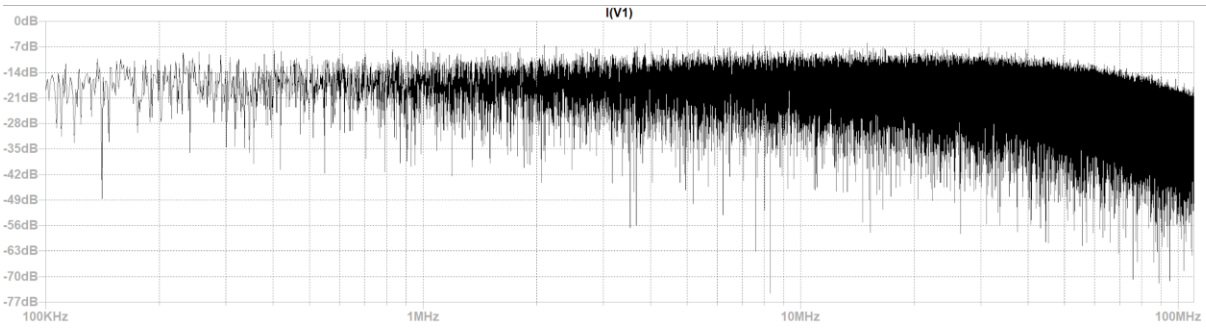


Figure A-104: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 26: 20% Load +/- 4% SSFM at V_{IN} = 24V

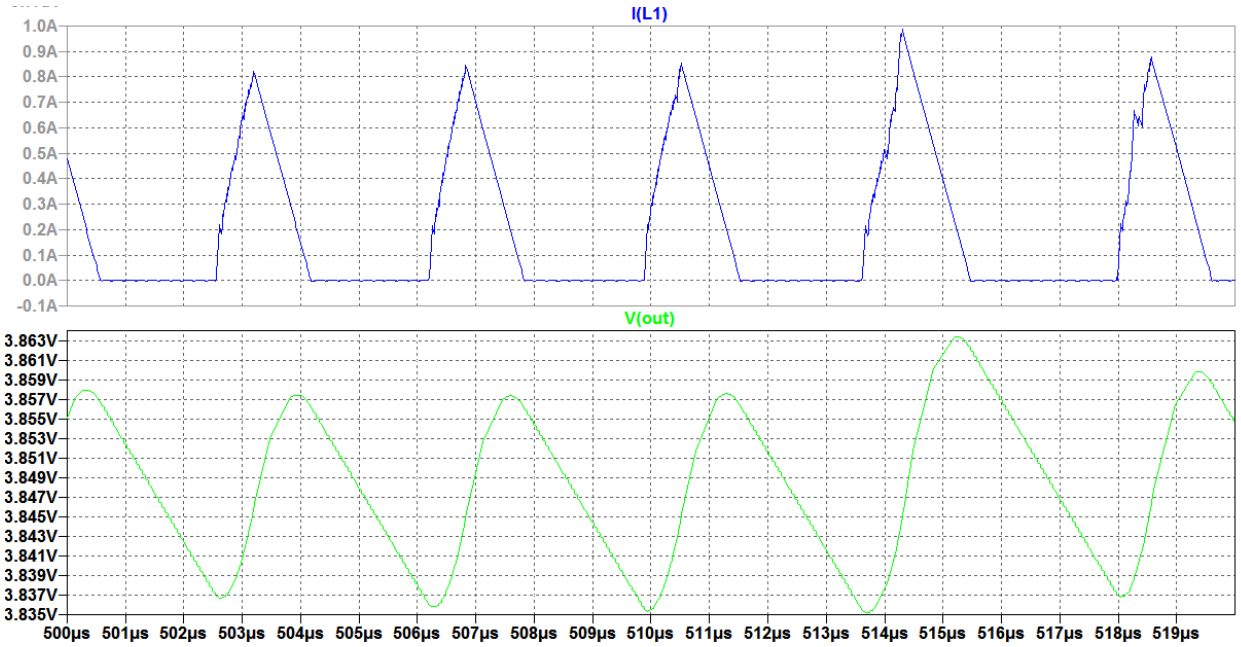


Figure A-105: V_o and $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

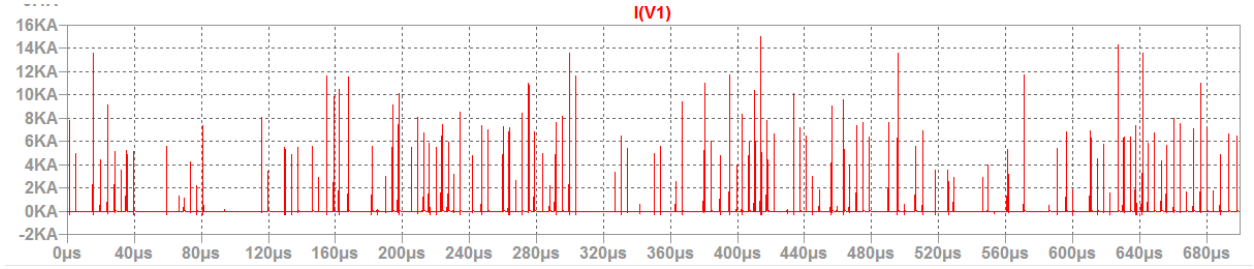


Figure A-106: I_{IN} from 4.5ms to 4.7ms (S-S)

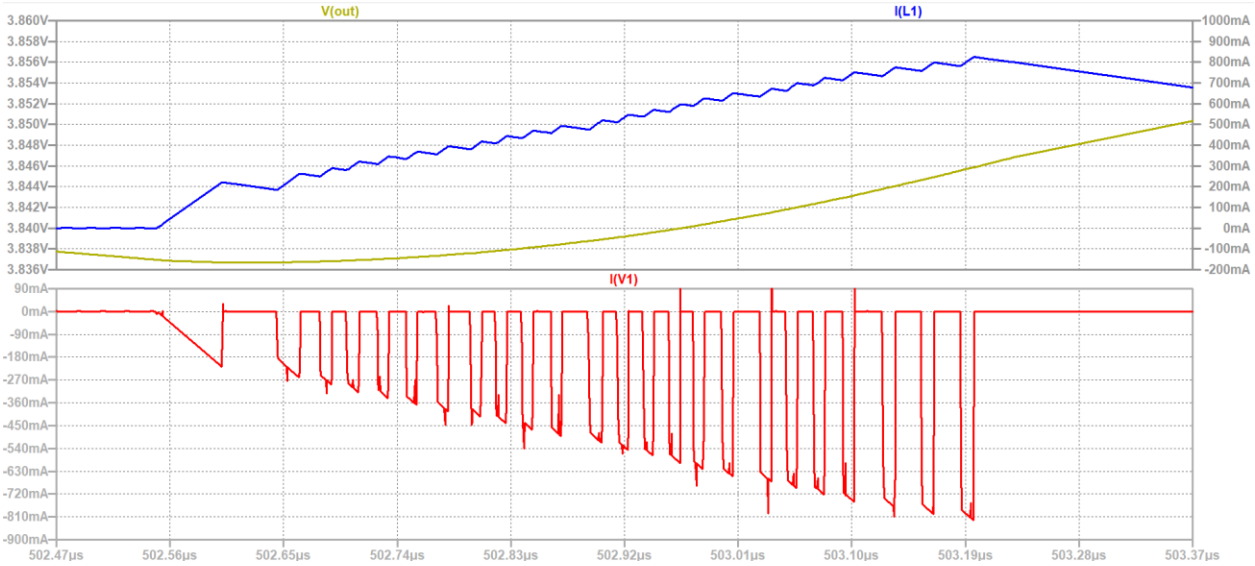


Figure A-107: I_{IN} Zoomed in Showing Input Current Switching with corresponding V_o and I_L

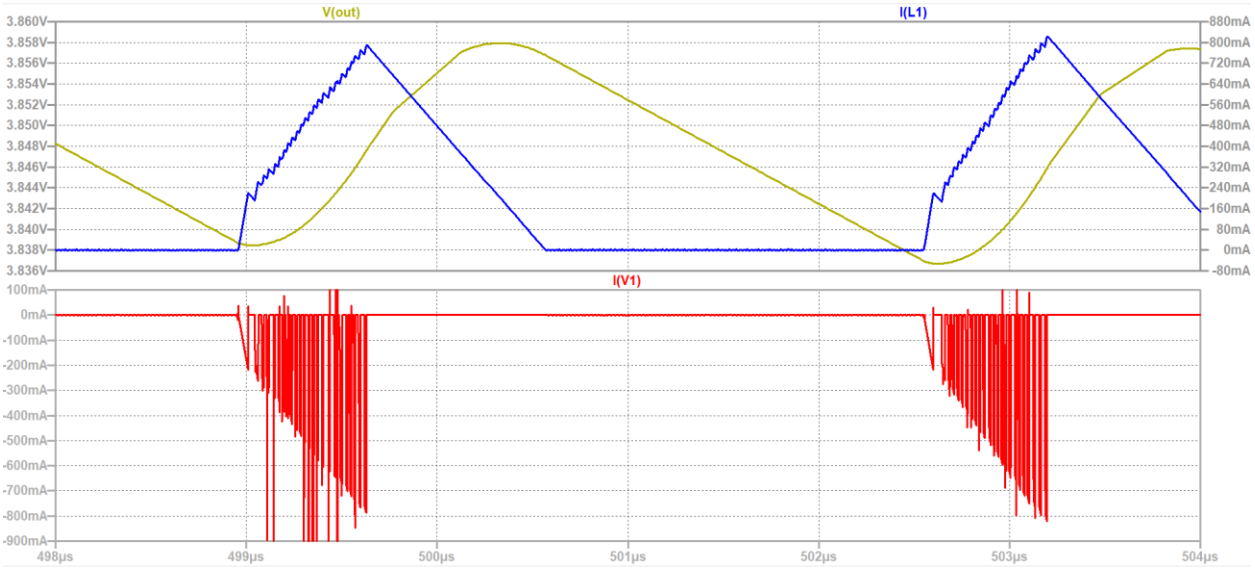


Figure A-108: I_{IN} Showing Input Current Switching with corresponding V_o and I_L

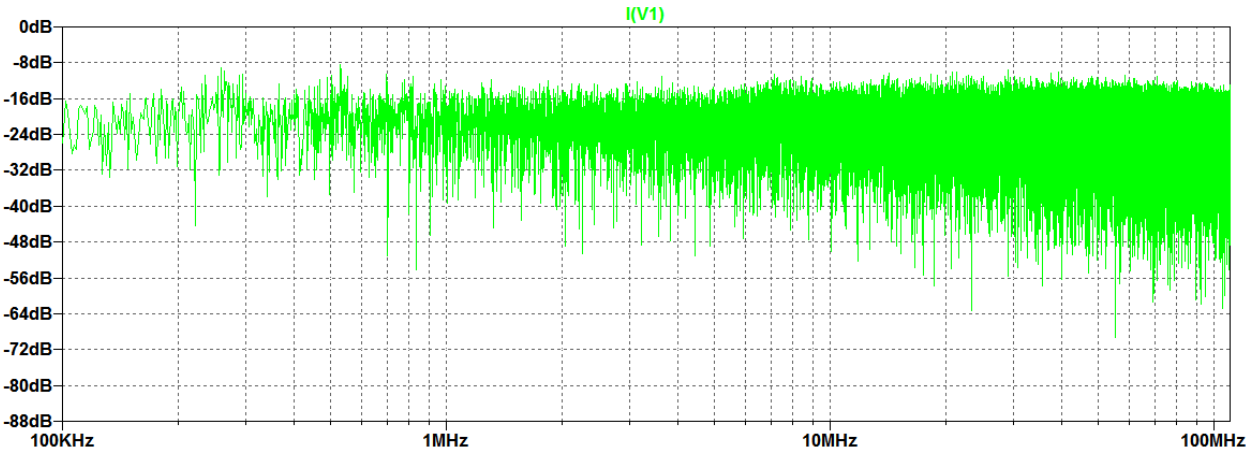


Figure A-109: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 27: 40% Load +/- 4% SSFM at V_{IN} = 24V

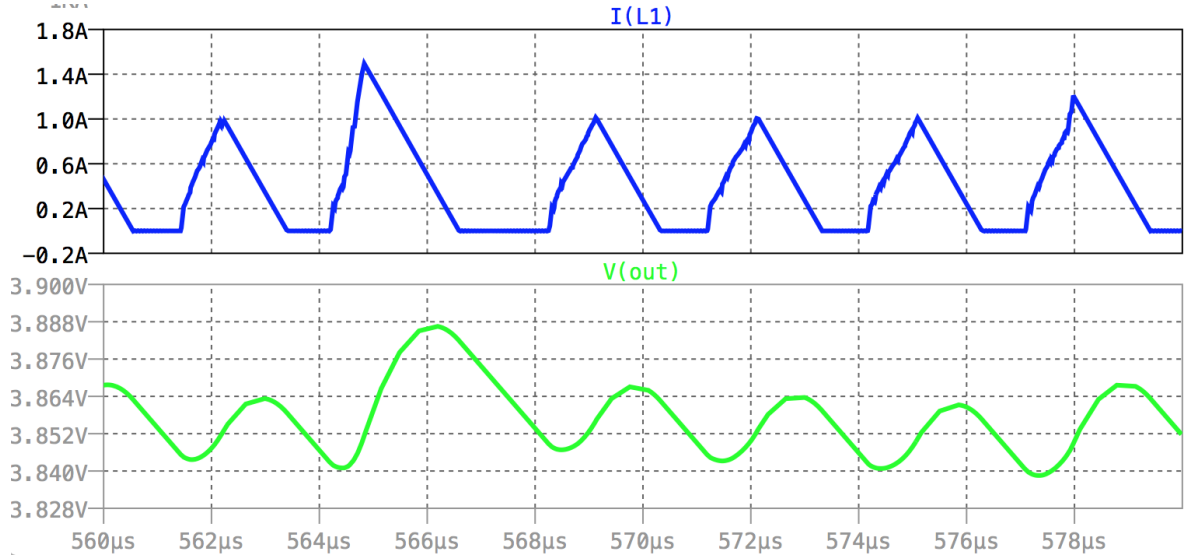


Figure A-110: V_o and $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

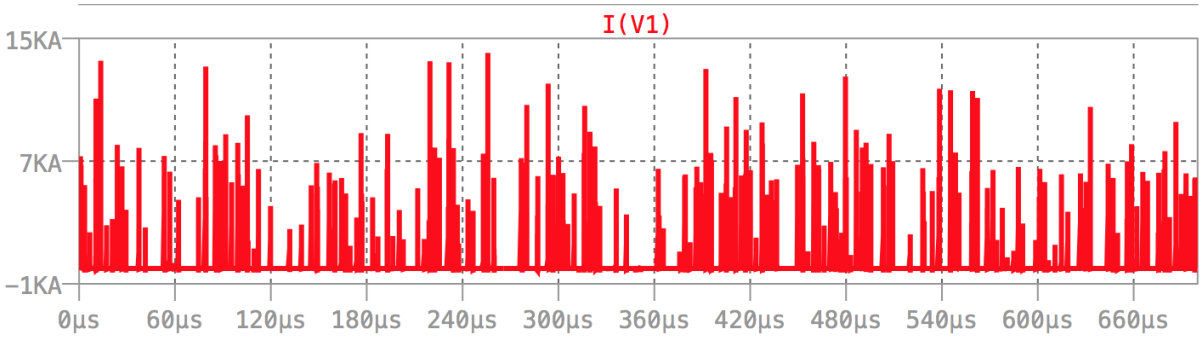


Figure A-111: I_{IN} from 4.5ms to 4.7ms (S-S)

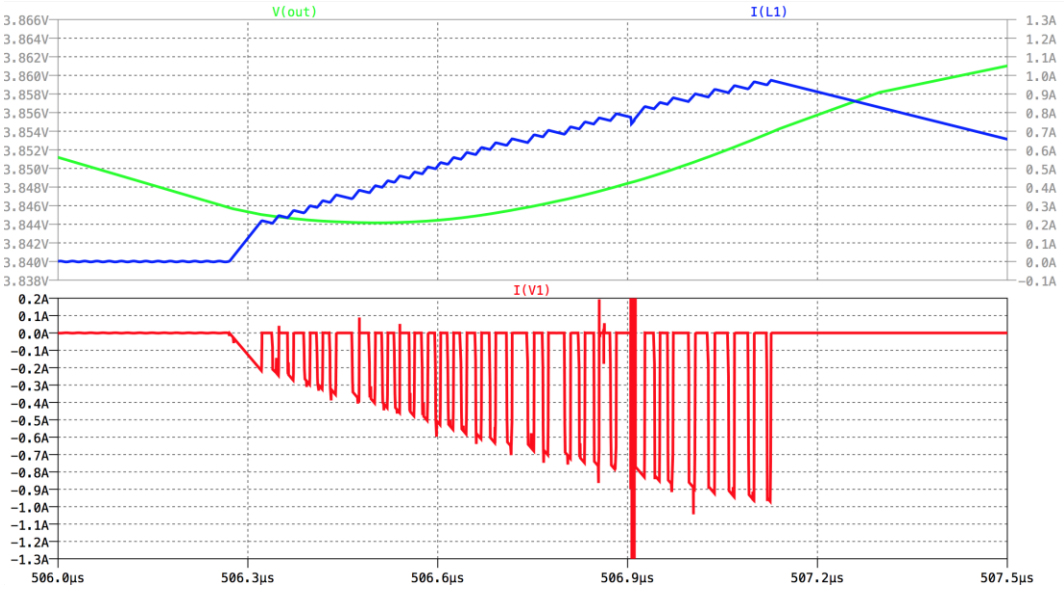


Figure A-112: I_{IN} Zoomed in Showing Input Current Switching with corresponding V_o and I_L

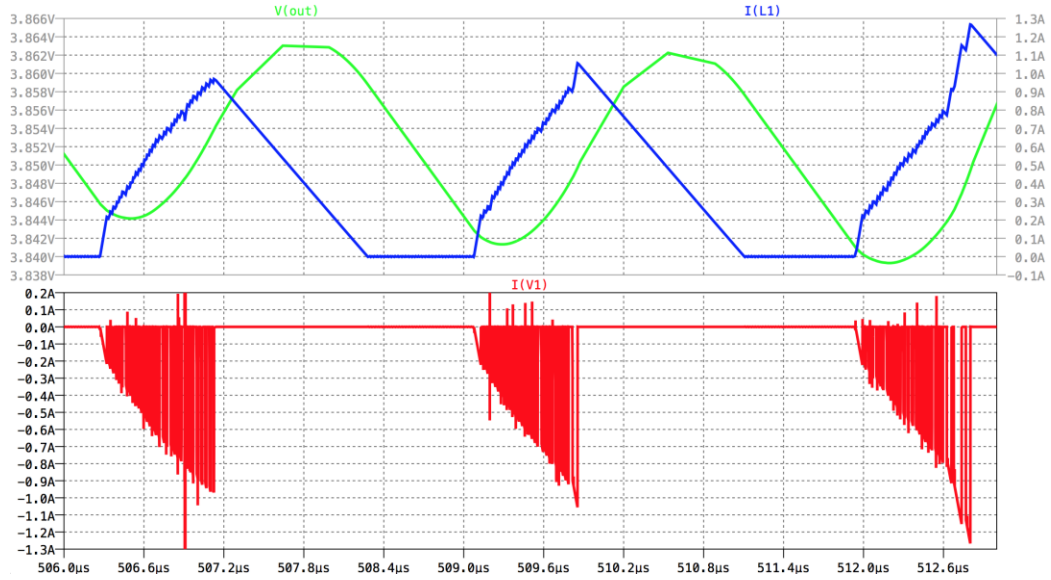


Figure A-113: I_{IN} Showing Input Current Switching with corresponding V_o and I_L

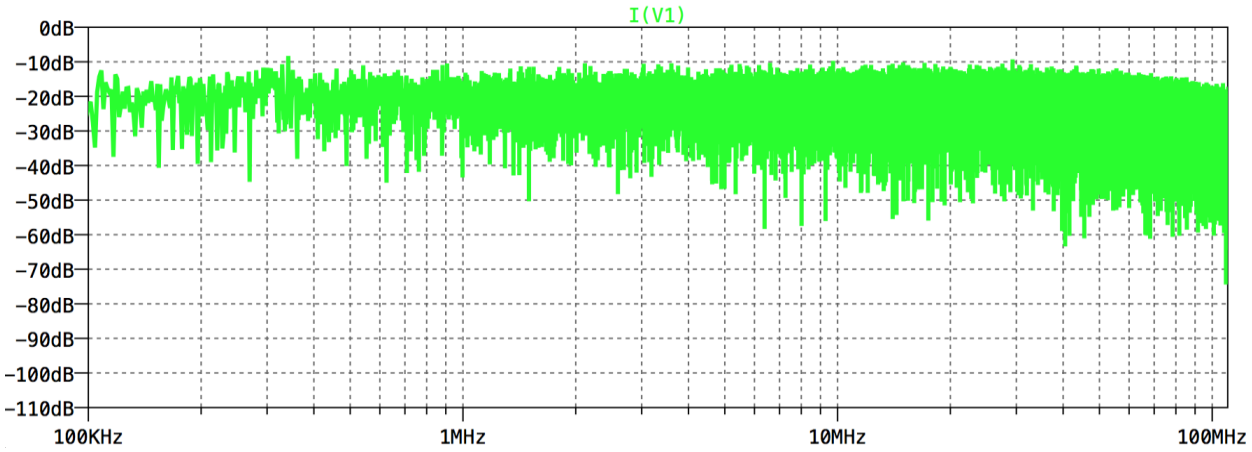


Figure A-114: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 28: 60% Load +/- 4% SSFM at V_{IN} = 24V

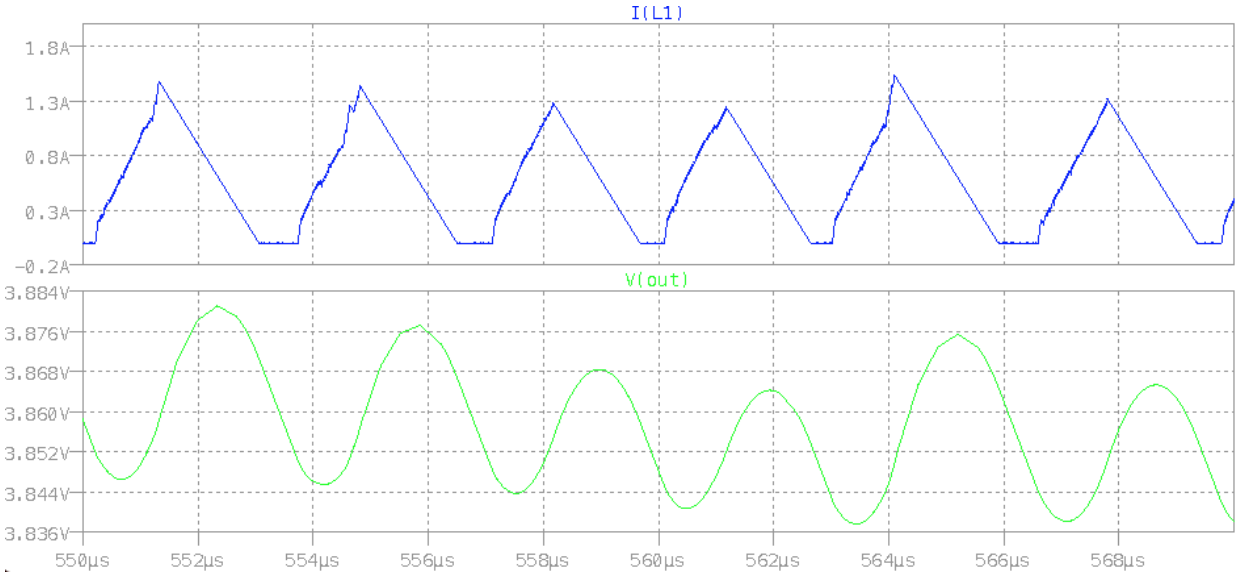


Figure A-115: V_o and $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

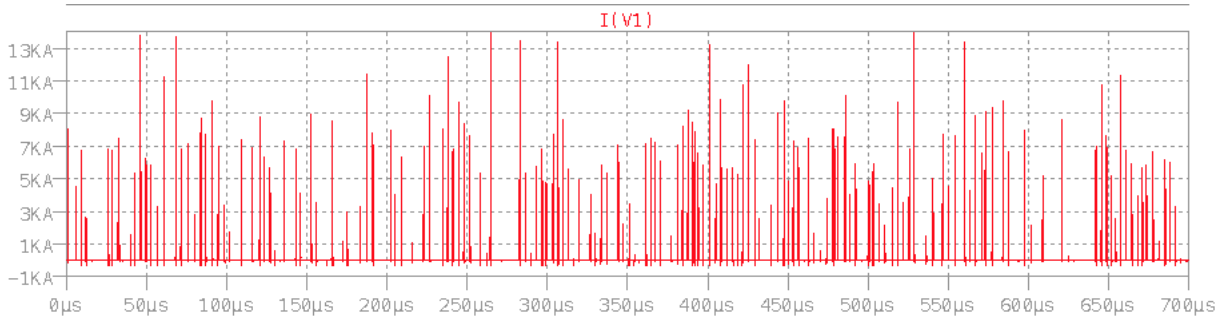


Figure A-116: I_{IN} from 4.5ms to 4.7ms (S-S)

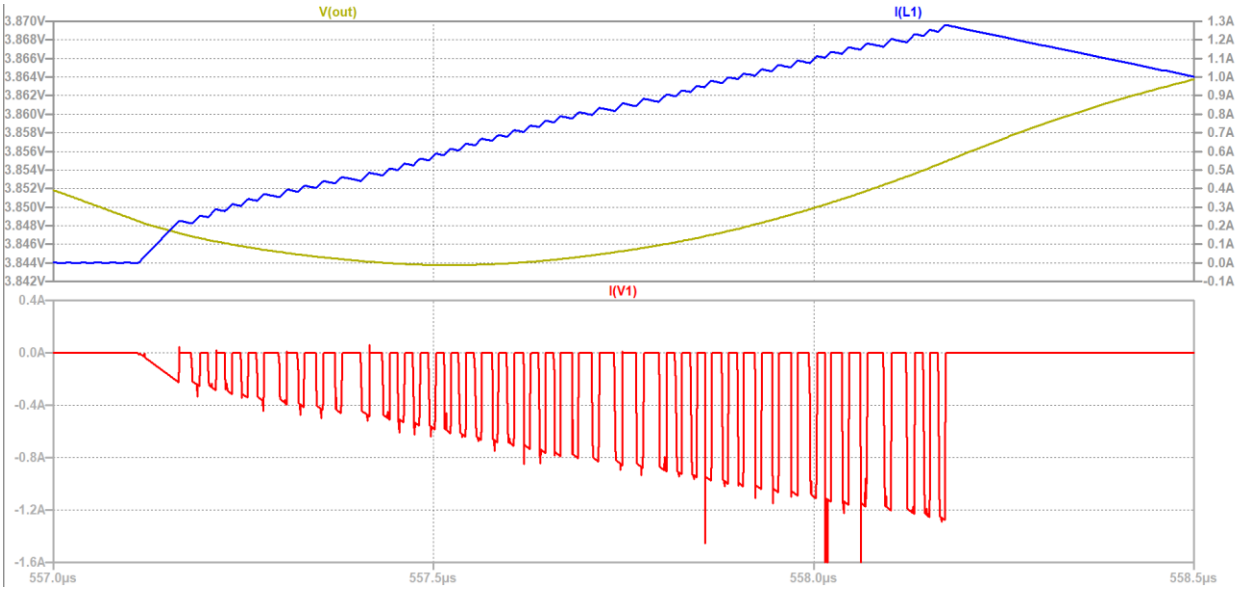


Figure A-117: I_{IN} Zoomed in Showing Input Current Switching with corresponding V_o and I_L

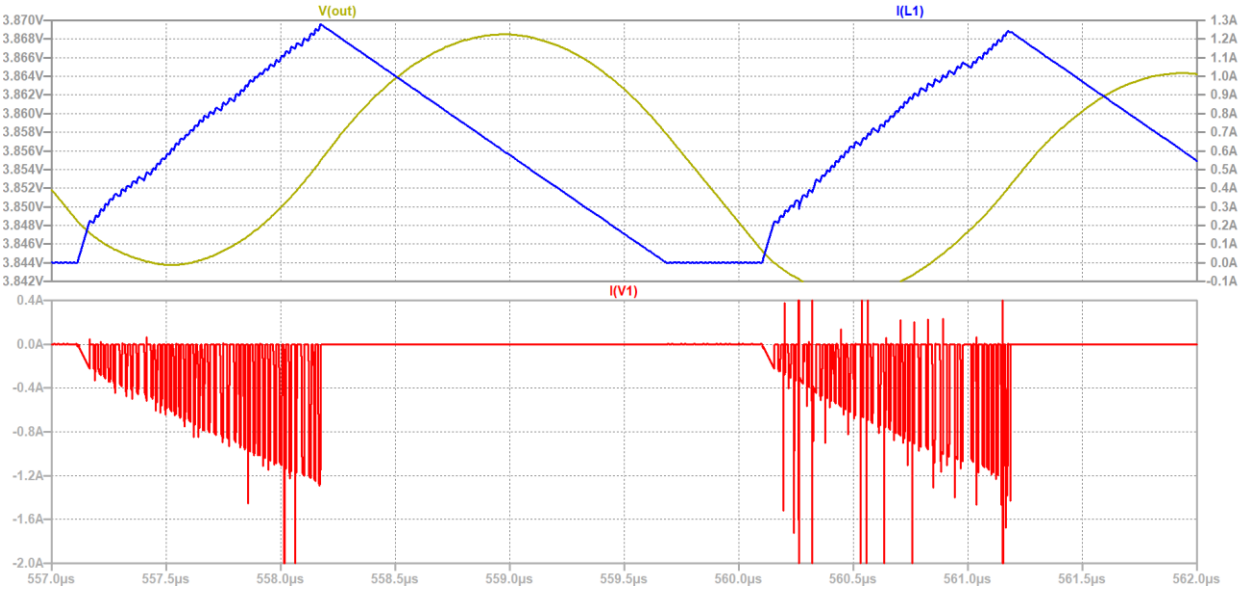


Figure A-118: I_{IN} Showing Input Current Switching with corresponding V_o and I_L

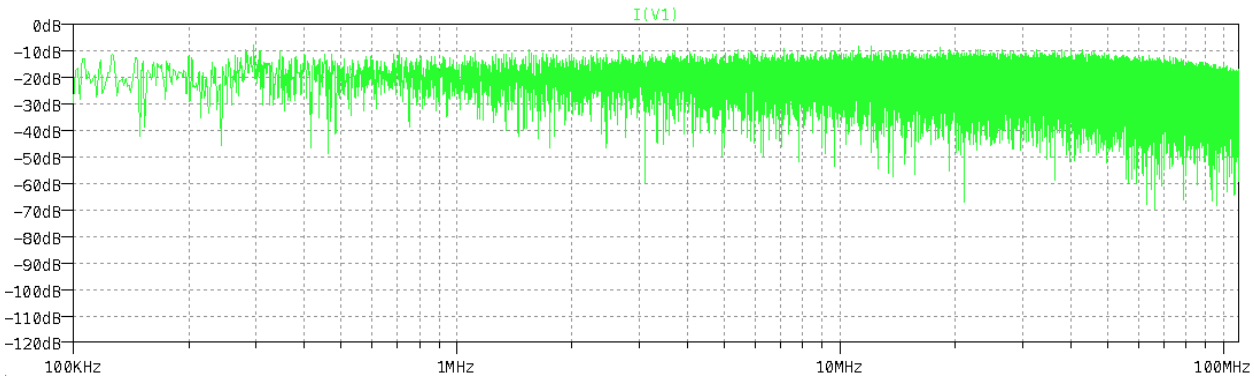


Figure A-119: FFT of I_{IN} from 4ms to 5ms (S-S) 60% 24V 4%

Case 29: 80% Load +/- 4% SSFM at V_{IN} = 24V

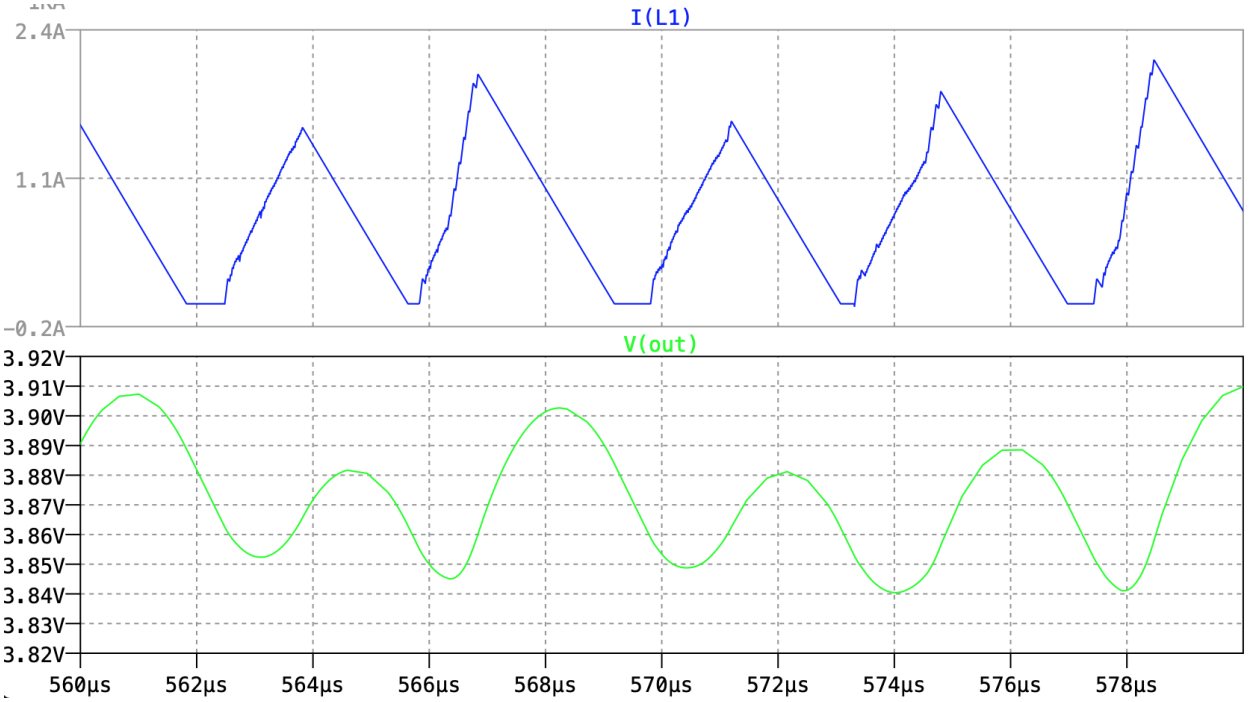


Figure A-120: V_o and $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

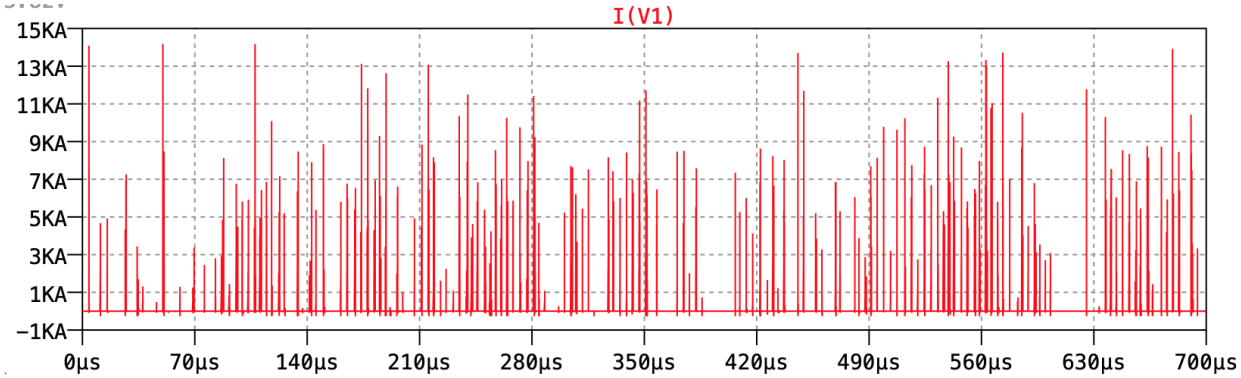


Figure A-121: I_{IN} from 4.5ms to 4.7ms (S-S)

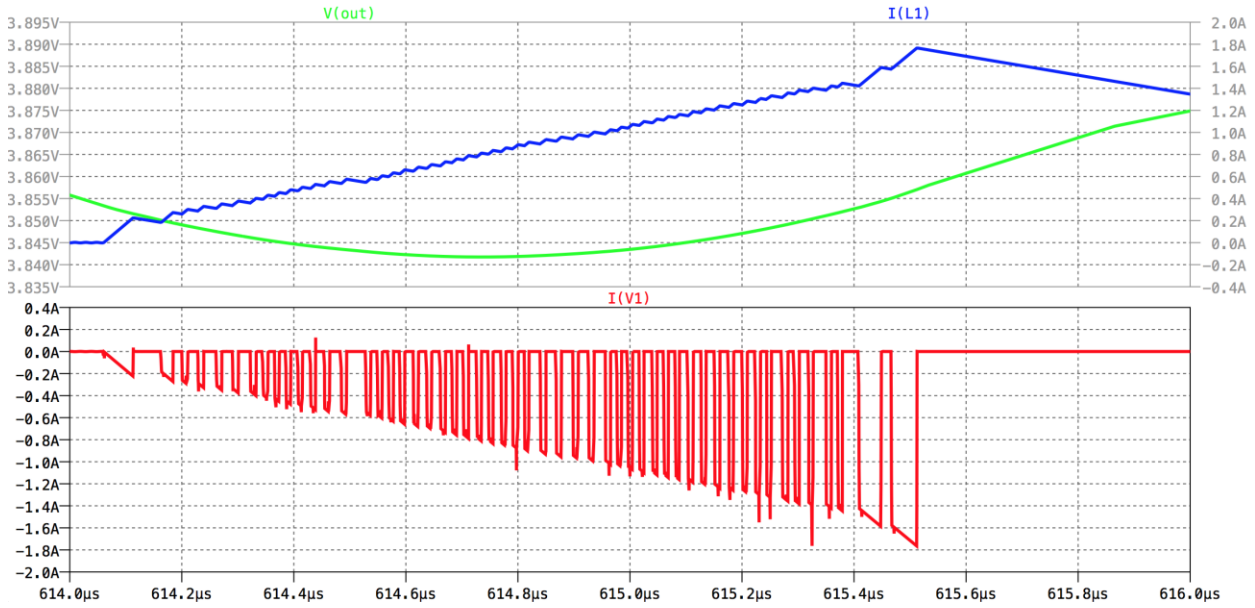


Figure A-122: I_{IN} Zoomed in Showing Input Current Switching with corresponding V_o and I_L

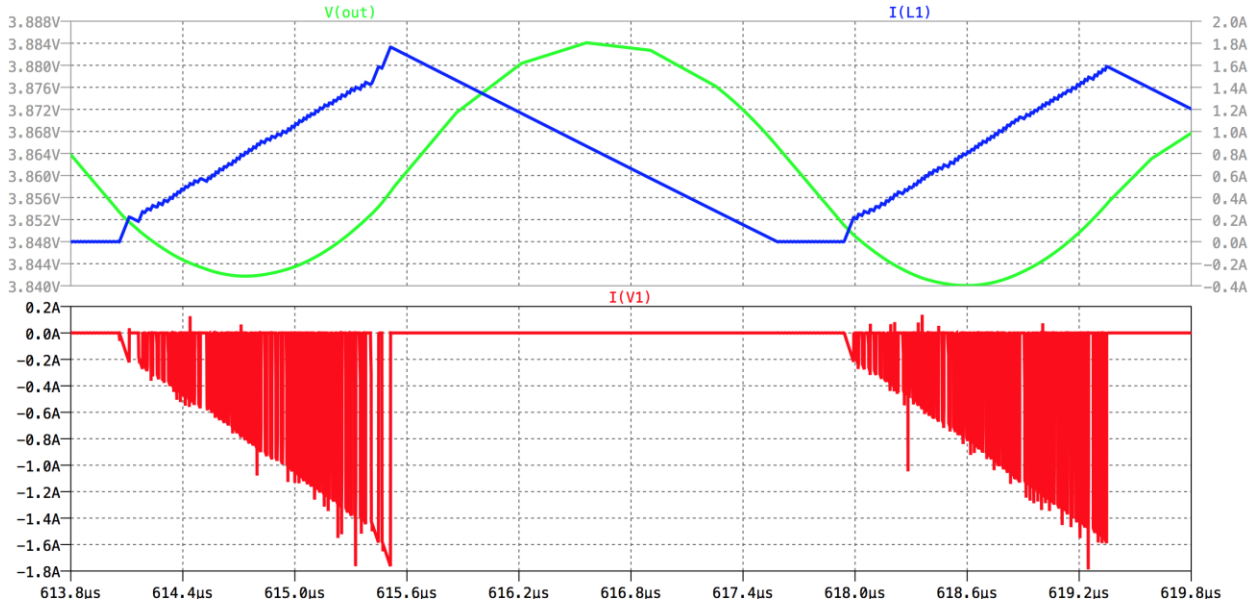


Figure A-123: I_{IN} Showing Input Current Switching with corresponding V_o and I_L

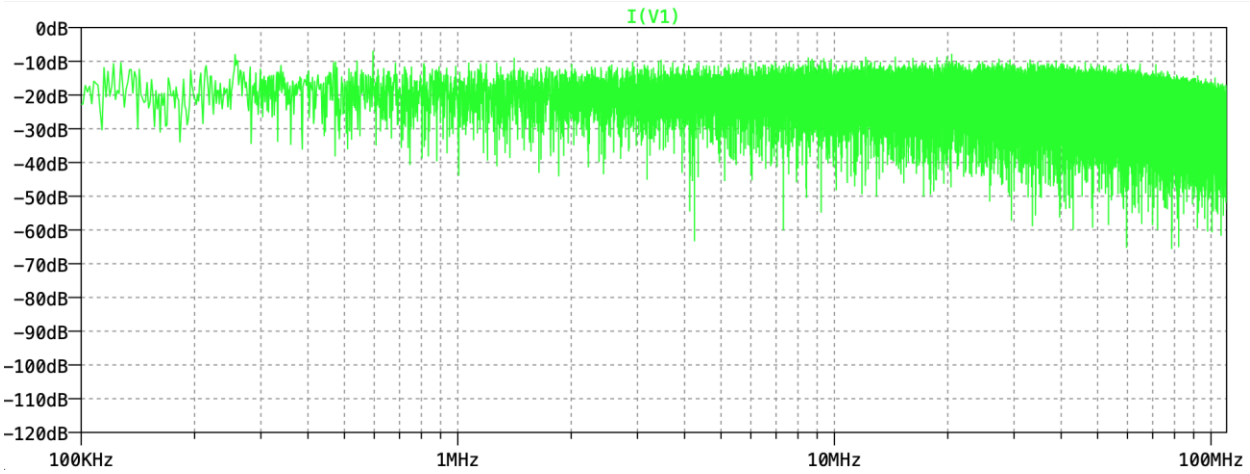


Figure A-124: FFT of I_{IN} from 4ms to 5ms (S-S)

Case 30: Full Load (1A) +/- 4% SSFM at V_{IN} = 24V

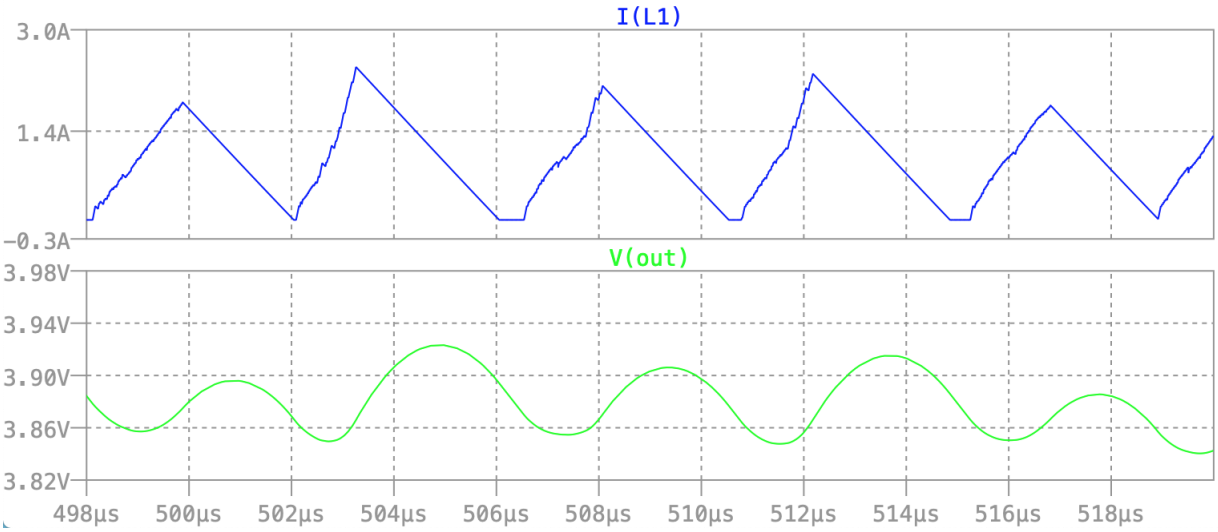


Figure A-125: V_o and $I_L = I_O$ from 4.5ms to 4.52ms (S-S)

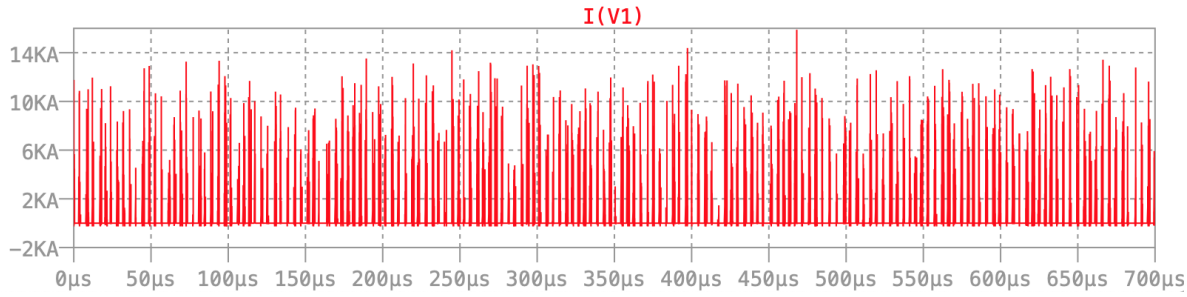


Figure A-126: I_{IN} from 4.5ms to 4.7ms (S-S)

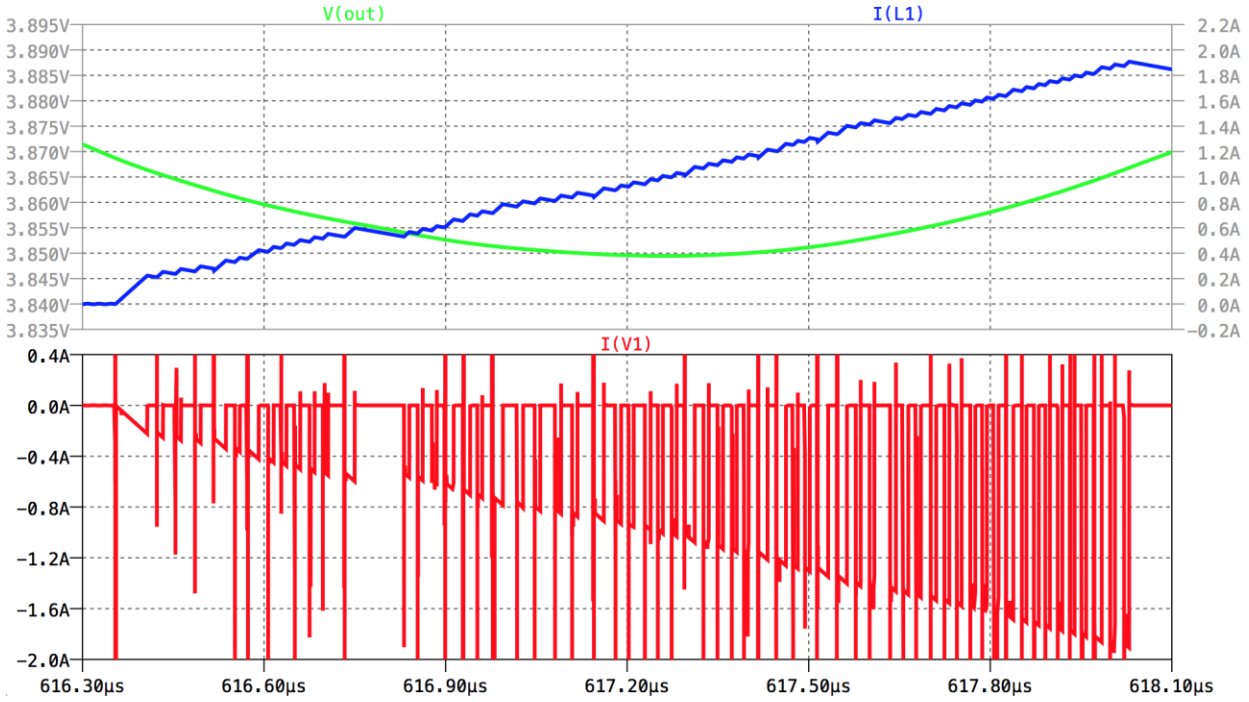


Figure A-127: I_{IN} Zoomed in Showing Input Current Switching with corresponding V_o and I_L

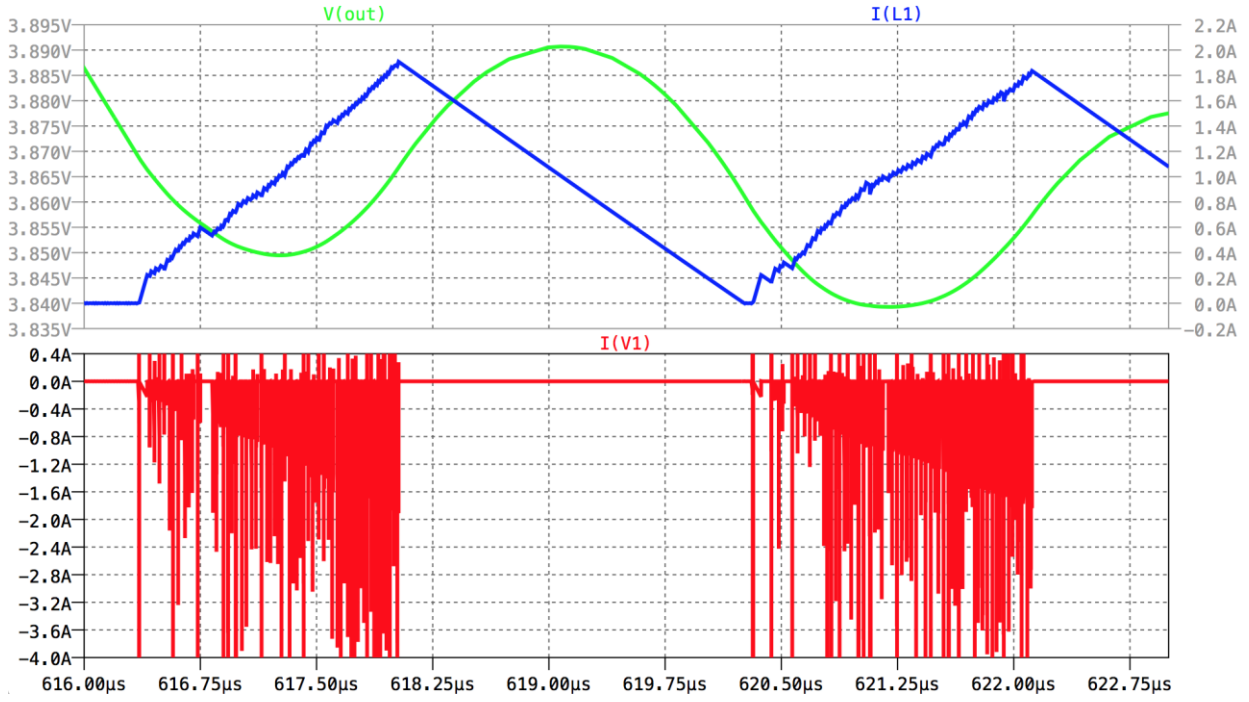


Figure A-128: I_{IN} Showing Input Current Switching with corresponding V_o and I_L

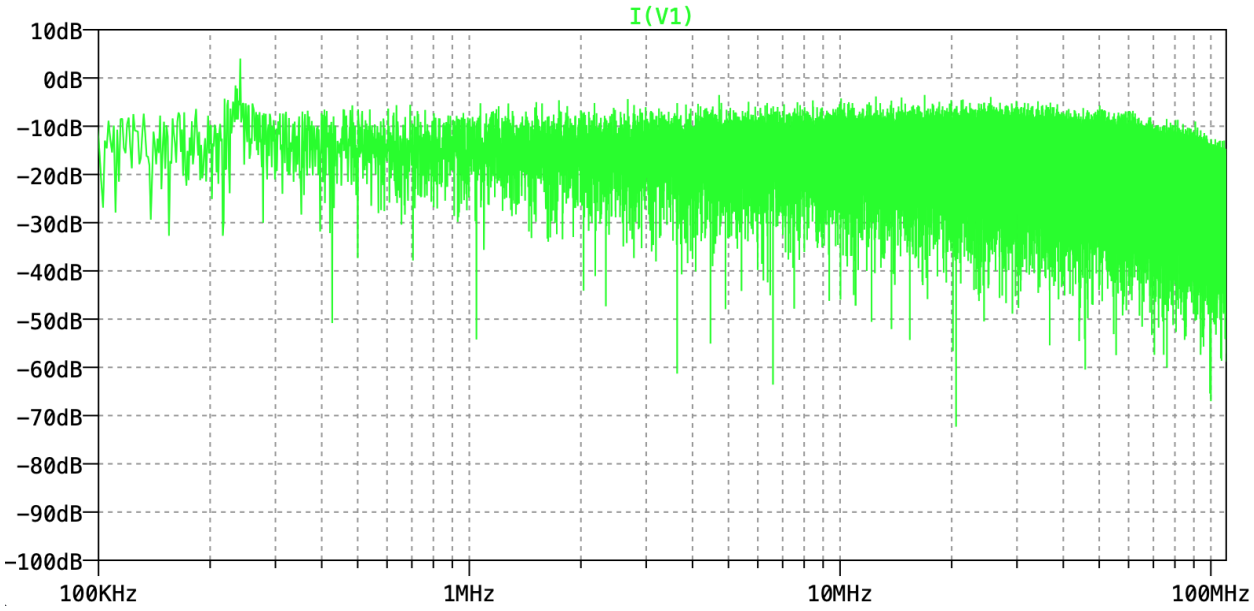
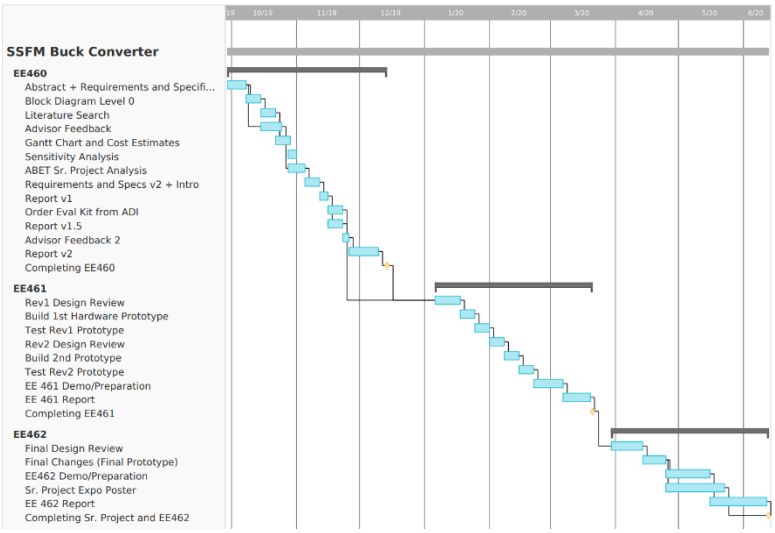
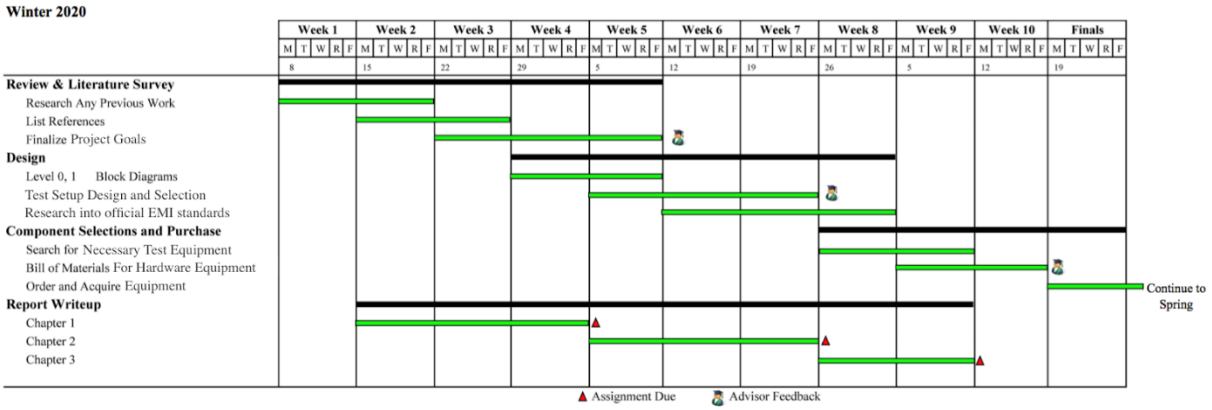
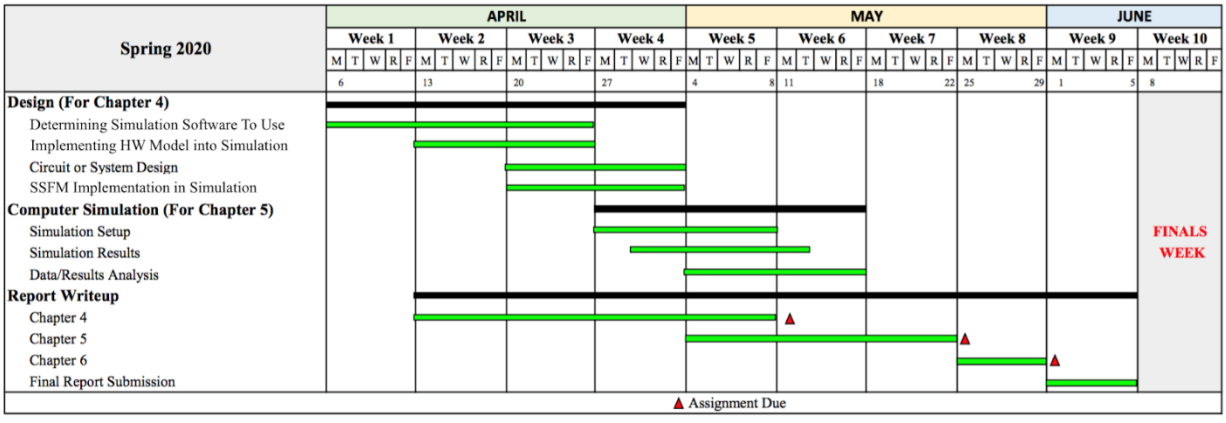


Figure A-129: FFT of I_{IN} from 4ms to 5ms (S-S)

Appendix B: Timeline of Tasks and Milestones







Appendix C: Analysis of Senior Project Design

Project Title: Conducted and Radiated EMI Measurements of Parallel Buck Converters Under Varying Spread Spectrum Parameters

Student Name(s): Elena Postupalskaya and Nathan Wang

Student Signature(s): ___EPP___, ___NW___

Advisor's Name: Dr. Taufik

1. Summary of Functional Requirements

The benefit of Spread Spectrum Frequency Modulation (SSFM) in minimizing electromagnetic interference (EMI) noise in a single buck converter has been known. This project investigates the effectiveness of SSFM in reducing EMI noise when applied in different variations. The noise of the parallel buck configuration needs characterization in order to analyze the circuits in comparison to each other. This was done through probing the input current in simulation and performing an FFT on the data in order to compare the noise spectra, specifically to look at the effects within the FM range. A commercially available buck module that has an LTSpice model available with SSFM capability is utilized in this project. Auxiliary circuits that will produce the necessary control signals for varying the percent modulation of SSFM are developed. After accomplishing proper operation in simulation, SSFM is applied in the buck converter with different combinations of percent modulation, loads, and inputs. The EMI noise levels at the input of the buck converter is measured and compared with the EMI noise obtained without any SSFM. The input voltage requirement for the buck converter is from 5V to 42V with output voltage of around 3V and maximum output current of 1A. The buck converter should vary

the percent modulation of the SSFM for about +/-4%. The conditions simulated were at 12V and 24V inputs, +/-1% and +/-4% spread in modulation, and load from 20% to 100% in 20% steps.

2. Primary Constraints

One of the issues associated with our project involves SSFM. The purpose of implementing SSFM and multiphase concepts into a buck converter are to reduce EMI. However, incorporating SSFM technology could cause an increase in interference with FM radio. Thus, there has to be a proper balance between EMI and FM audio. Exploring different variations in SSFM provides further possibilities to evaluate a new design approach.

3. Economic

The resulting creation of this project idea would be a combination of SSFM and multiphase. This development can increase consumer cost in the short run and become negligibly priced long term. This stems from the idea that new technology is improved and more efficient, also requiring R&D to develop the new product. Once new technology comes out, this project will become increasingly obsolete and hit the end of its life cycle. Obviously, the mass production of electronic devices requires a tremendous amount of energy to produce. However, the creation of this project will not significantly impact the trend in resource usage.

For the scope of this senior project, the sole benefit will be the investigation and testing of a functioning variable SSFM buck converter. In order to develop working prototype products, this project will undergo lots of research, testing, and prototyping. In short, this project will accrue more cost and then it will benefit. This project is very much research based rather than practical based. Project funding will come from Texas Instruments, our project sponsor, the Cal

Poly Electrical Engineering department, as well as our advisor, Dr. Taufik. Additional needed funding will be the responsibility of Elena Postupalskaya and Nathan Wang.

The initial plan for this project only requires a component cost of $58.33. This cost will go toward an ADI development board that has the capability of adjusting SSFM percent modulation while being a multiphase buck converter. In terms of equipment cost, all necessary lab machines are available for the team to access. New equipment has been purchased to complete hardware measurements, but since the focus of the project shifted to simulation due to the COVID-19 pandemic, this is not applicable to the senior project itself anymore as the hardware will be done at a later time.

For the purpose of this project, there will be no source of revenue or profit as this is purely a research project. As outlined in the project Gantt chart shown in Figure C-1, the goal is to measure the variable SSFM effects on the LM53601MAEVM by June 2020. The goal of coming up with a functioning model for a product is to be able to take that data and make it available to industry to develop a more efficient and better performing buck converter to be used in a wide range of applications. Other than further R&D costs, manufacturing and operation costs should remain unchanged. Depending on the project status by June, the result from this year's team determines the course of action for students who choose to continue with this project. The team would be the same, and the plan is to complete hardware measurements before the end of 2020 if the health situation permits.

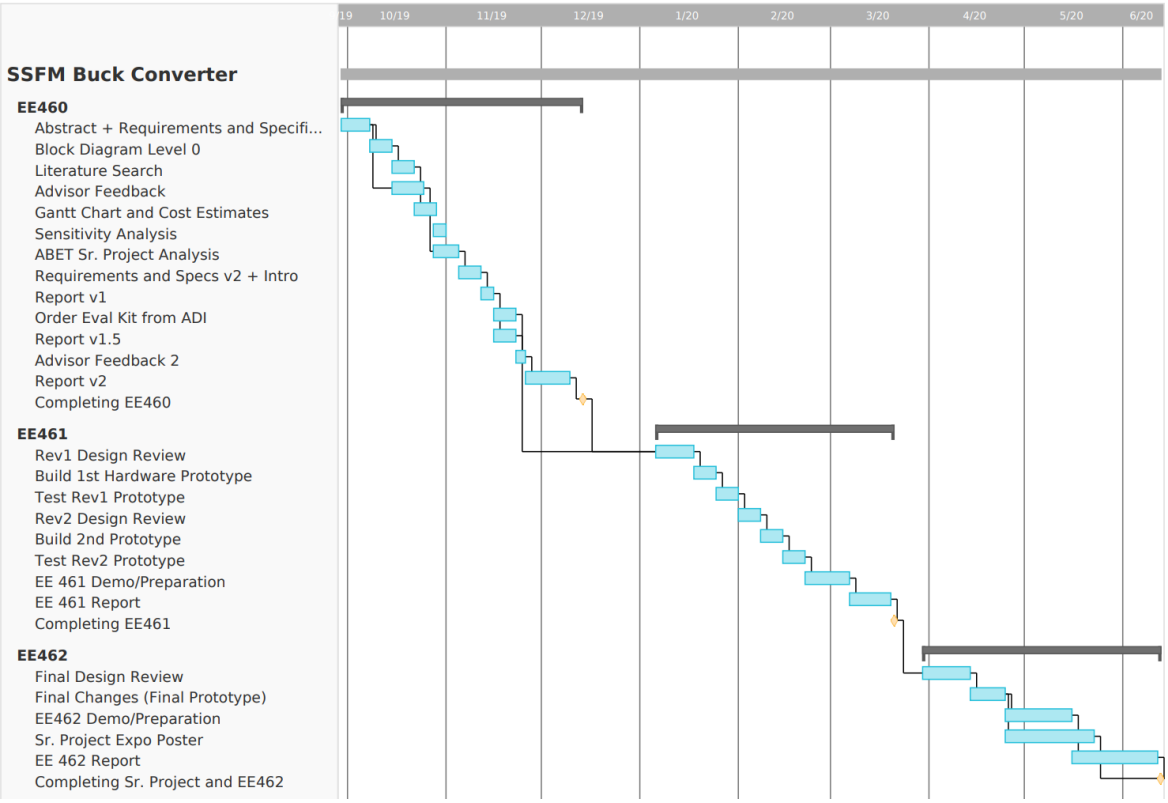


Figure C-1: Economic Timing as Shown by Gantt Chart

4. If manufactured on a commercial basis:

If the working converter makes it into mass production, we can anticipate the production of approximately 10 million modules a year, based on the estimate that one tenth of the cars manufactured per year would potentially incorporate this type of buck converter. The estimated cost of a standard buck converter is $20 on average when developed in mass based on a comprehensive search for buck converters from various vendors. In order to support operating costs, the buck converter would be sold to customers at $30. Thus, we would be looking at a $10 profit for each buck converter, which translates to an estimated $100 million profit from this buck converter alone annually. For an average consumer, they would not be directly impacted by the cost to operate the buck converter. One reason is that the proposed buck converter is targeted for above 90% efficiency. Another reason is that the end customer will not be directly interacting

with the buck converter itself. Rather, the effect on the customer will be seen through a malfunctioning car multimedia unit when used in automotive applications.

5. Environmental

An effect of the SSFM buck converter is expanding the potential electronics that can be used in cars. It further expands the DC applications within cars. There is potential it could help reduce the use of gas in cars and perhaps the pollution from it too. However, a buck converter is a switching DC to DC converter, and semiconductors are used for the transistor that carries out the switching. Also, the buck converter we are using is a chip, and that is also a semiconductor material. Semiconductor manufacturing is detrimental to the environment and uses lots of hazardous chemicals. Data exists of the workers manufacturing semiconductors experiencing health problems due to the exposure. The externalities would include all the people affected by the pollution. The pollution manifests in the air, water, and soil. Pollution would also affect plants, animals, and the world's ecosystems, hereby affecting species besides humans because of human actions.

6. Manufacturability

A manufacturability aspect does not exactly exist for this project since it is a research and development project. The evaluation boards that we are using are already manufactured in a company; therefore, there would not be any significant changes in manufacturability of the hardware. Perhaps, if our project yields promising results, the only change would just be added functionality to the chips or boards, which would not be a major change in the way the existing boards and chips are manufactured.

7. Sustainability

From an economic perspective, like any other new technological development, releasing the newly developed buck converter introduces new competition to the electronics industry. Thus, certain stakeholders and companies would be affected by seeing a decline in the purchase of their existing product. However, introducing new technology into circulation allows for healthy competition and economic prosperity. The goal in the long run is to produce an improved product at a lower cost. The development and production of our buck converter will, however, have a short life cycle as new technology will replace it in the future. To beat the competition, people would strive to create a better product compared to each other, driving sustainability.

Environmentally, like any generic electronics, buck converters are composed of numerous kinds of materials, some of which are rather hard to harvest naturally. In addition, there is a rise in global awareness surrounding the issue of electronic waste. Socially, electronic waste pollution detracts from the quality of life around the world. Introducing this buck converter into production and to customers will contribute to the electronic waste already in existence. Therefore, it is important to have the design be fully ROHS compliant at least. A challenge would be to have a design of this buck converter to be more environmentally friendly.

8. Ethical

An ethical implication with this buck converter is the balance between having an FM radio feature to entertain and broadcast information to drivers, while ensuring that they are not distracted from the driving itself. As the IEEE Code of Ethics states, it is important to hold paramount the safety and health of the public. The system needs to be reliable enough to not malfunction on drivers at critical moments, interfere with critical systems, nor provide a sense of distraction as drivers are on the road.

9. Health and Safety

An important safety concern with the product is to ensure that the operation of the buck converter does not interfere with the FM radio in an automobile. This is important because it is possible that FM radio can potentially be used to broadcast important information worldwide in the event of an emergency. Another safety concern is that we want the buck converter to work reliably in order to sustain a car multimedia system. In addition, this converter needs to work in a relatively independent environment to not interfere with other electronics in an automobile.

10. Social and Political

Considering the social and political effects could make sense in a broad sense of the impacts and implementation of this research and development project further carried into production. The main effect from this senior project would be on the automotive companies as well as the chip and power designers and manufacturers, since the SSFM buck converter in hardware would directly concern these stakeholders. Those companies would have the main interest in such a potential project due to the nature of their business. The secondary stakeholders would be the ones affected by these companies. These would include the consumers of automobiles from those automotive companies, for example. Another instance would be the ones experiencing the impact of the pollution of the manufacturing companies. The areas in the world with higher skilled jobs requiring more knowledge would feel more of the profits of having the proprietary information of the design. Many areas outsource. The areas with a larger infrastructure or manufacturing sectors would feel more of an impact from the pollution. However, pollution can be limited with restrictions sourced from the political power placed in

regulation. Thus, the nature of the economy in a certain area could create inequities compared to other areas.

11. Development

This project could help the development of buck DC to DC converter chips with variable SSFM and multiphase, which are difficult to come across in the typical market available for DC to DC converters. SSFM provides an interesting alternative to conventional EMI filters. The SSFM with multiphase combination could bring about new advances in switching regulator and controller technologies. It could be incorporated and more widespread in chips. This project will also contribute to the self-development of the future electrical engineers working on this project, Nathan Wang and Elena Postupalskaya. SSFM significantly reduces the noise of the switching buck converter providing better DC to DC overall. The buck SSFM converter involves different areas of electrical engineering providing experience in power electronics, RF, signal processing, and some aspects of communications. The power electronics portion is incorporated with the buck DC to DC converter. The RF and communications are included with the measurements and analysis of the conducted and radiated EMI and EMC, as well as investigating the interference with FM radio and signals. The signals come into play when controlling the waveform shapes. Since this is a relatively new area of research, there will be much insight into electrical engineering from different perspectives. The development progress can be seen in the preliminary literature search shown below:

[1] K. Scott and G. Zimmer, "Spread Spectrum Frequency Modulation Reduces EMI," *Analog Devices*. [Online]. Available: https://www.analog.com/en/technical-articles/spread-spectrum-frequency-modulation-reduces-emi.html. [Accessed 18 Oct. 2019].

1. We chose this source because the article gives a broad overview on how SSFM technology reduces EMI. The article also discusses applications that use SSFM technology, as well as how Linear Technology chips could assist those applications.

2. This source informs the project by giving description and visual overviews of SSFM analysis. This information can be used as a basic example which we can base our initial SSFM analysis on for our project.

3. This source is credible because Analog Devices is a renowned company. Kevin Scott graduated from Stanford University, which is well known for its engineering, and worked in the industry for 26 years. Greg Zimmer graduated from UC Berkeley, which is also well known for its engineering, and has a broad range of product experience such as the SSFM buck converters.

[2] G. Aulagnier, K. Abouda, E. Rolland, M. Cousineau, and T. Meynard, "Benefits of multiphase Buck converters in reducing EME (Electromagnetic Emissions) Analysis and application to on-chip converters for automotive applications," *2015 IEEE International Symposium on Electromagnetic Compatibility (EMC)*, 2015, pp. Xx-xx. [Online]. Available at: https://ieeexplore-ieee-org.ezproxy.lib.calpoly.edu/document/7256140. [Accessed 17 Oct. 2019].

1. We chose this source because the paper discusses multi-phase buck converter designs and analyzes EMI reduction benefits compared to standard topology. The paper also discusses applications for such a converter, including automotive technologies.

2. This source informs the project by providing the context to our goals of our converter incorporated in an automotive application, which is an end goal for our research. This source

provides details about the automotive application aspects of multi-phase bucks that we can reference for our project.

3. This source is credible because the article was published by IEEE. In addition, author Aulagnier received his Ph.D. in power electronics in France and works as an Analog Circuit Design Engineer at NXP Semiconductors. Co-author Cousineau also received his Ph.D. in Electrical Engineering at the Institut National Polytechnique de Toulouse.

[3] *LM53600MAEVM and LM53601MAEVM User's Guide*. (2015). Accessed: Oct. 17, 2019. [Online]. Available at: http://www.ti.com/lit/ug/snau190/snau190.pdf.

1. We chose this source because the guide provides an overview of features available on a SSFM buck converter laid out on a development board for testing.

2. This source informs the project because the user guide is for the SSFM buck converter development board that we are using for our senior project. We can reference this to learn more about the features of the development board.

3. The source is credible because the guide was produced by Texas Instruments' engineers. Texas Instruments is a well-known and trusted company, and the user's guide is for the development board they made for their own component, the LM53600-Q1.

[4] Texas Instruments, "LM53600/01-Q1, 0.65A/1A, 36V Synchronous, 2.1MHz, Automotive Step-Down DC-DC Converter," LM53600-Q1, LM53601-Q1 datasheet, Jun. 2015 [Revised Feb. 2016]. [Online]. Available at: http://www.ti.com/lit/ds/symlink/lm53601-q1.pdf.

1. We chose this source because the datasheet provides technical specifications and values for an automotive step-down converter that uses SSFM.

2. This source informs the project because this datasheet corresponds to the buck converter on the development board used for this senior project.

3. Source is credible because Texas Instruments' engineers wrote this datasheet. Texas Instruments is a well-known and trusted company, and the datasheet is for their own product, which they know thoroughly.

[5] B. Choi, "Chapter 3: Buck Converter," in *Pulsewidth Modulated DC-to-DC Power Conversion Circuits, Dynamics, and Control Designs*, Hoboken, NJ: John Wiley & Sons, Inc., 2013, ch 3 pp. 71-122. [Online]. Available at: https://onlinelibrary-wiley-com.ezproxy.lib.calpoly.edu/doi/pdf/10.1002/9781118772188. ch3. [Accessed 17 Oct. 2019].

1. We chose this source because the book discusses PWM DC-DC power conversion. Chapter 3 of the book specifically discusses PWM power conversion specific to buck converter topologies.

2. This source informs the project by breaking down the fundamentals of buck converter with modulation technology.

3. The source is credible because this book was published by the IEEE Press in print as well as edited by the IEEE editorial board of 2013. IEEE is a highly regulated technical authority on these subjects. Furthermore, this book had been technically reviewed by peers. Also, Dr. Choi

has over 50 research publications on converters. In addition, the book is relatively recent, which means the information is relevant to the times.

[6] F. Biziitu, et al. "Buck Voltage Converter." U.S. Patent 20180375434A1, Dec. 27, 2018. [Online]. Available at: http://appft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&p=12&u=%2Fnetahtml%2FPTO%2Fsearch-bool.html&r=582&f=G&l=50&co1=AND&d=PG01&s1=%22buck+converter%22&s2=Dc&OS=%22buck+converter%22+AND+Dc&RS=%22buck+converter%22+AND+Dc.

1. We chose this source because the patent discusses a topology used by Infineon Technologies, specifically the effects of the poles and zeros in the transfer function on the response of the converter.
2. This source informs the project by telling us how we change the function of our buck converter by influencing the control loops to provide the desired output.
3. The source is credible because Infineon sponsored this patent, and Infineon is a renowned company. Furthermore, this patented technology is used in their products, which proves this is a valid and applicable patent.

[7] S. Park, H. A. Huynh and S. Kim, "Analysis of EMI reduction methods of DC-DC buck converter," 2015 10th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo), Edinburgh, 2015, pp. 92-96. [Online]. Available at: https://ieeexplore-ieee-org.ezproxy.lib.calpoly.edu/document/7358337. [Accessed 17 Oct. 2019].

1. We chose this source because the paper presents several EMI reduction techniques for a DC-DC converter, as well as methodology to analyze EMI levels.

2. This source informs the project by giving examples on how to conduct EMI testing for development boards as well as our final SSFM buck converter.

3. The source is credible because IEEE published the paper. Co-author Hai Au Huynh is pursuing his Ph.D. in this area, so he is knowledgeable in this area. Co-author Sanghyeok Park has an MSEE degree and works for the renowned company of Samsung. Co-author So Young Kim received her M.S. and Ph.D. degrees at Stanford University in Electrical Engineering and worked at Intel Corporation and Cadence Design Systems before becoming Associate Professor at Sungkyunkwan University in Suwon, South Korea.

[8] D. Sokolov, V. Khomenko, A. Mokhov, A. Yakovlev, and D. Lloyd, "Design and Verification of Speed-Independent Multiphase Buck Controller," 2015 21st IEEE International Symposium on Asynchronous Circuits and Systems, 2015, pp. Xx-xx. [Online]. Available at: https://ieeexploreieee.org.ezproxy.lib.calpoly.edu/document/7152688. [Accessed 18 Oct. 2019].

1. We chose this source because the paper describes the design and verification for a multi-phase buck controller. It focuses specifically on how the speed independent phases perform better compared to traditional synchronous designs.

2. This source informs the project by explaining how our project can incorporate the multi-phase aspect to a SSFM buck converter.

3. The source is credible because IEEE published the paper. In addition, all authors hold Ph.D. degrees in electrical and computing fields.

[9] Z. Li and D. Pommerenke, "EMI Specifcs of Synchronous DC-DC Buck Converters," Proceedings of the 2005 International Symposium on Electromagnetic Compatibility, 2005. EMC 2005, Institute of Electrical and Electronics Engineers (IEEE), Jan 2005, pp. 711-714. [Online]. Available at: https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber =1513616. [Accessed 17 Oct. 2019].

1. We chose this source because the paper analyzes the radiated EMI issues associated with standard buck converters. The paper also addresses solutions to reduce EMI for buck converter topologies.
2. This source informs the project by providing information on how to measure and analyze radiated EMI measurements, which is one of two EMI measurements needed for our senior project.
3. This source is credible because IEEE published it. Also, Professor David Pommerenke has a Ph.D. in this field, worked at Hewlett Packard, authored or co-authored more than 200 papers, and has 13 patents. Li is his co-researcher at Missouri University of Science and Technology.

[10] M. R. Yazdani and H. Farzanehfard, “Conducted electromagnetic interference analysis and mitigation using zero-current transition soft switching and spread spectrum techniques,” *IET Power Electronics*, vol. 5, no. 7, pp. 1034–1041, Jan. 2012. [Online]. Available at: https://ieeexplore.ieee.org/document/6336928. [Accessed 19 Oct. 2019].

1. We chose this source because the IEEE journal article addresses spread spectrum methods by pseudo random modulation for a flyback DC-DC converter. More specifically, the paper talks about the reduction in EMI via conducted EMI measurements.

2. This source informs the project by providing information on how to take and analyze conducted EMI measurements, which is one of the two analysis methods needed for our EMI measurements.

3. This source is credible because the article was published by IEEE. The authors are also respectable and have experience in the area. Yazdani got his Ph.D. at the Sciences and Research Branch of Azad University in Tehran, Iran in this area. Farzanehfard got his Ph.D. from Virginia Polytechnic Institute and State University and authored or coauthored more than 150 published papers.

[11] J. Balcells, A. Santolaria, A. Orlandi, D. Gonzalez, and J. Gago, "EMI Reduction in Switched Power Converters Using Frequency Modulation Techniques," *IEEE Transactions on Electromagnetic Compatibility*, vol. 47, no. 3, pp. 569–576, Aug. 2005. [Online]. Available at: https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=1516228. [Accessed 19 Oct. 2019].

1. We chose this source because the paper brings up the idea of spread spectrum technology on a buck converter using frequency modulation.

2. This source informs the project by helping us understand the overall scope as we try to understand, improve, and develop a SSFM buck converter with a minimum of two phases.

3. This source is credible because IEEE published the paper. Also, Balcells has his Ph.D. in power electronics, has been a professor at Universitat Politècnica de Catalunya in Barcelona, Spain, was head of R&D in power electronics at a GE company, worked as a consultant, participated in EU projects, and was an editor for IEEE for 11 years. Santolaria got his Ph.D. from the Polytechnic University of Catalonia in Barcelona, Spain, worked with nuclear power plants as well as R&D, and later worked for Siemens and Bosch.

[12] K. S. Kostov, et al., "Prediction of the Conducted EMI from DC-DC Switched-Mode Power Converters." Power Electronics and Motion Control Conference. Riga, Latvia. 2-4 Sept. 2004. [Online]. Available at: https://pdfs.semanticscholar.org/1b43/471a8ebc3ad89863ec3bbb6e8f13837919b8.pdf. [Accessed 18 Oct. 2019].

1. We chose this source because the paper addresses the EMI from a switching mode power supply, which can be applied to a switching buck DC-DC converter. The article also touches on theoretical and measured EMI levels for common mode and differential mode.
2. This source informs the project by giving our project a guideline on how to predict and measure common and differential mode EMI levels relating to the switching of DC-DC converters.
3. This source is credible because the authors are from the Power Electronics Laboratory at the Helsinki University of Technology in Finland and the Institute of Power Electronics at the Tampere University of Technology. The authors have also been cited on many occasions: K. S. Kostov has been cited 247 times, J. Kyyrä has an h-index of 13, and T. Suntio has an h-index of 31.

[13] "Pulse-Width Modulated DC-DC Power Converters, 2nd Edition." *ProtoView*, Jan. 2016. *Gale Academic Onefile*, [Online]. Available at: https://link.gale.com/apps/doc/A439057474/AONE?u=calpolyw_csu&sid=AONE&xid=09e183e7. [Accessed 21 Oct. 2019].

1. We chose this source because the review discusses PWM DC-DC power converters. The paper also compares EMI levels between a standard converter and one that uses PWM technology.
2. This source informs the project by providing an overview on PWM DC-DC converters, which we are attempting to design, verify, and test to incorporate SSFM and eventually multiple phases.
3. This source is credible because there are multiple editions, which signifies that the material is relevant and demanded. Furthermore, it is recent, meaning the information is relevant today. Also, Dr. Kazimierczuk is a University Distinguished Professor at Wright State University with research specifically in converters and their signals, was an IEEE Associate Editor for various journals and won the Best Paper Award from IET Power Electronics in 2012.