Current Protection
For the Energy Harvesting from Exercise Machines (EHFEM) Project

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Abstract

The Energy Harvesting from Exercise Machines (EHFEM) project intends to create an exercise machine that recycles the energy expended by an athlete operating the machine by sending it to the electric grid. The work done by the user goes through a DC-DC converter and an inverter in order to prepare it for delivery to the grid. A protection circuit ensures that the inverter does not try to pull too much current from the DC-DC converter. The project implements a current protection system that ensures the system doesn't experience an overcurrent condition.

1 Introduction

The Energy Harvesting for Exercise Machines (EHFEM) project seeks to create an exercise machine that harvests the energy generated by operating an exercise machine and transfers the energy to the local grid [5]. This project consists of various subprojects that each deal with individual aspects of the EHFEM, such as designs for a DC-DC converter, an inverter, and an input protection system [5]. This particular project seeks to improve upon and complete the designs for a current protection circuit that Eric Funsten and Cameron Kiddoo completed for their senior project [6]. This current limiting circuit depends on an input protection circuit design worked on by Dr. Braun.

The Enphase Micro-Inverter's startup period causes current and voltage accumulation in open load conditions that input protection seeks to prevent from causing damage [3.] The current protection circuit seeks to deliver only as much power as the inverter can convert. Current limiting improves efficiency between the DC-DC converter and inverter as while as protecting the DC-DC converter.

Concurrent with this project, students Calvin Abshier and Calvin Xu developed an input protection circuit focused on limiting voltage. Their design seeks to improve upon the DC-DC converter input protection circuit design Ryan Turner and Zack Weiler completed for their senior project [14]. Filtering out high frequency and transient responses using capacitive filtering and decoupling techniques ensures a clean DC signal [14]. Both this overvoltage protection circuit and the overcurrent protection circuit rely on a microcontroller, which contains four ADCs and two DACs to drive the current limiter.

This project intends to further Eric Funsten and Cameron Kiddoo's attempts to provide the necessary protection for the DC-DC converter while still allowing the converter to draw the proper amount of power from the elliptical for maximum efficiency. Input current protection seeks to minimize efficiency loss to preserve the benefits of the EHFEM.

This report contains a design and testing results for a module necessary for the current limiting circuit, identifying two modules that definitively work. The report documents issues encountered while working with the embedded systems used in the current limiting system and it concludes by integrating the current liming system together.

2 Customer Needs, Requirements and Specifications

Customers need a safe exercise machine with the potential to pay itself off. Customers want a machine similar in operation and size but more affordable and economically friendly. Customer needs originate by understanding that a customer wants a more environmentally friendly and cost-effective machine that doesn't put them in danger or take up more space than a standard exercise machine would.

Requirements and specifications derived from the DC-DC converter and inverter specifications, and the protection circuit prototyped previously by Eric Funsten and Cameron Kiddoo [6]. Table 3-1 consists of marketing requirements and the engineering specifications derived to meet the marketing requirements.

Table 2-1: Current Protection System Requirements and Specifications

Marketing Requirements	Engineering Specifications	Justification
1, 5	Current drawn by DC-DC converter limited to 6.4A.	Current Four-switch Buck-Boost technology for the converter supports a maximum DC input current of 6.4A at 51V input.
2, 3	Machine pays itself off after 35,000 hours of use with PG&E rates and 70 W-hr. per hr.	The total system must operate for 35,000 hours to reach a zero lifecycle cost.
2, 3	Average machine operates for 10 years without maintenance of energy harvesting electrical components.	10 years equates to about 35,000 hours or the amount of time needed for the machine to pay itself off.
4	Protection circuit has a volume no greater than 6" by 3" by 3".	Smaller circuitry means a smaller overall system. A PCB for circuit protection should not take up more space than 6"

		by 3" by 3"
1, 3	Current protection system reacts to overcurrent conditions within 100µs.	If the protection circuit doesn't react fast enough overcurrent conditions could damage the overall system.
1, 6	Current protection circuit diverts current greater than 6.4A to a load that can dissipate the additional power safely.	The extra current has to go somewhere and in order for the system to remain safe it must regulate current dissipation.
5	Input protection circuit connects to DC-DC converter through female banana plugs.	The current protection system needs input from the current DC-DC converters
2	Current protections costs (components and labor) must not exceed $25.	The previous input protection circuit design managed a $25 dollar budget and this project seeks affordability.

Marketing Requirements
1. The protection circuit must prevent overcurrent conditions.
2. Cost-effective
3. Durable
4. Spatially conservative design
5. Compatible with inverter and DC-DC converter
6. The protection circuit must divert extraneous power safely.

The following table outlines the delivery dates for the primary reports and demonstrations related to this EHFEM project.

Table 2-2: Deliverables

Delivery Date	Deliverable Description
1/7/15	EE 460 update
3/20/15	Design Review
4/15/15	EE 461 demo
3/17/15	EE 461 report
6/4/15	EE 462 demo
10/30/14	ABET Sr. Project Analysis
5/29/15	Sr. Project Expo Poster
6/5/15	EE 462 Report

3   Functional Decomposition (Level 0 and Level 1)

3.1   Level 0 Block Diagrams

Figure 3-1 depicts a high-level black box diagram of the input protection circuit as a whole; a high-level block diagram pertaining to the current protection system, specifically, follows the diagram of the input protection system as a whole. The former diagram seeks to clarify how the latter diagram fits in the system as a whole. The current protection black box diagram seeks to display that the system has two inputs and one output. The table breaks the inputs down into one component from the elliptical machine, one from the DC-DC converter, and a single output to the micro-inverter. The functionality of the system, specified in the table, seeks to satisfy the known specifications of the DC-DC converter and the inverter.
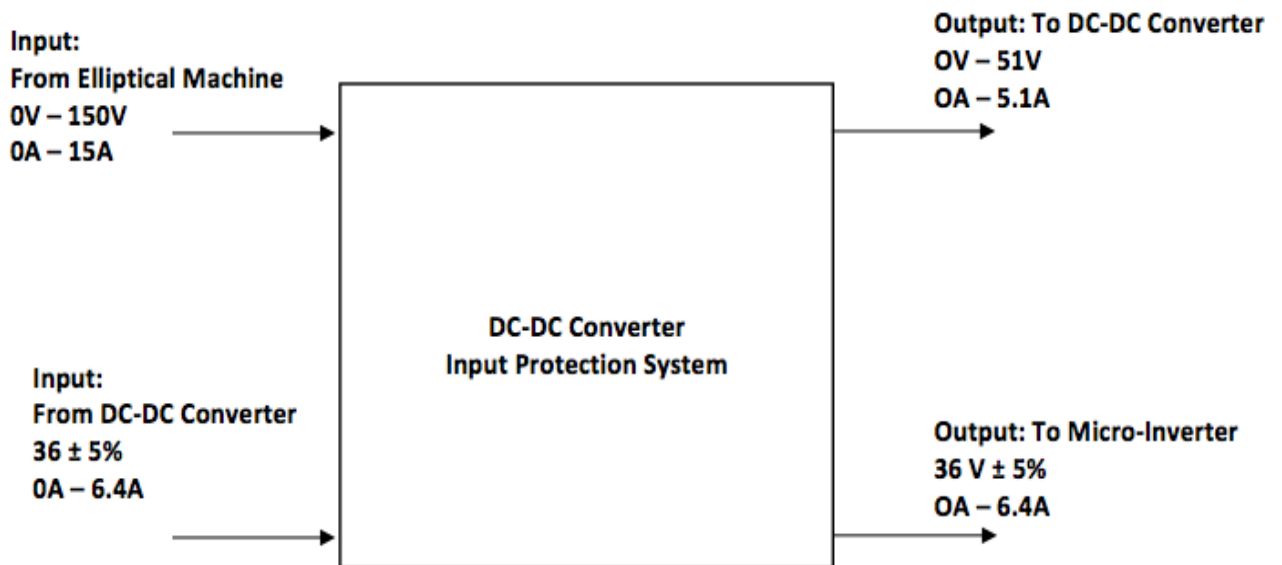
Figure 3-1: Protection System Level 0 Block Diagram
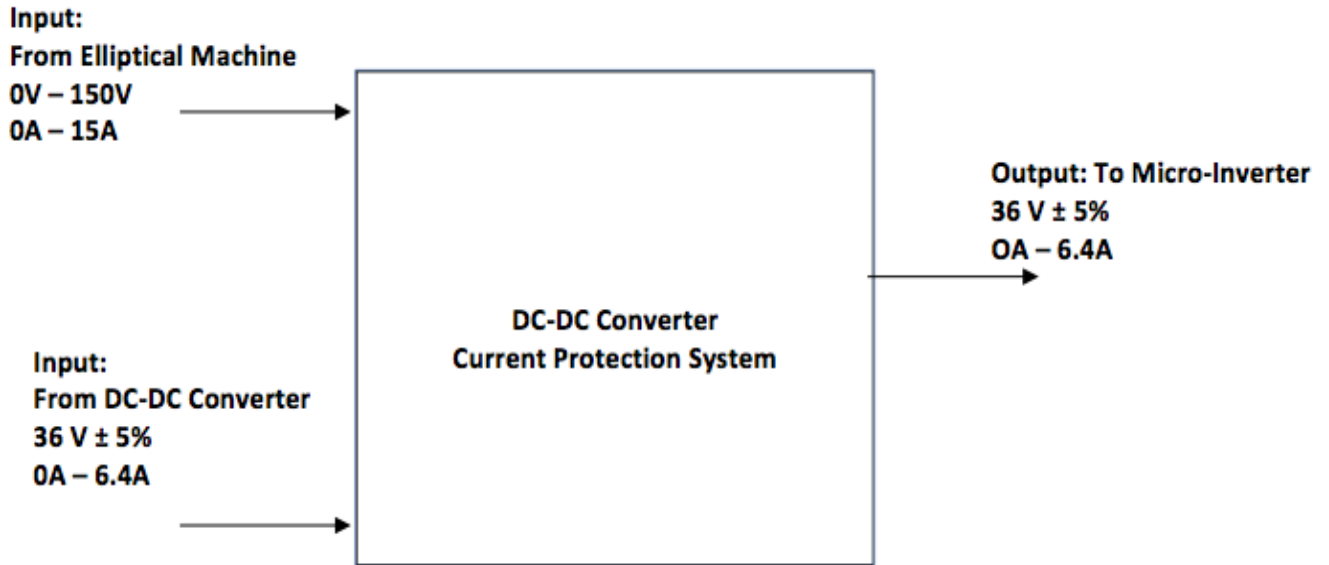
Figure 3-2: Current Protection System Level 0 Block Diagram

Table 3-1: DC-DC Converter Input Protection Circuit Inputs/Outputs/Functionality

Module	DC-DC Converter Input Protection Circuit
Inputs	Input signal generated from elliptical exercise machine: 0-150V, 0-15A Input signal from DC-DC converter: 36V ± 5%, 0-6.4A
Outputs	Output signal to Micro-inverter: 36V ± 5%, 0-6.4A.
Functionality	The current protection circuit must take in a current up to 15A and output no more than 6.4A to the DC-DC converter.

3.2   Level 1 Block Diagrams

Figure 3-3 shows the level 1 block diagram for the current protection. This level displays the current diverter, current limiter, current sense, and microcontroller elements. This system acts to mediate the signal from the DC-DC converter, ensuring that the current of the signal sent to the inverter does not exceed 6.4A. Tables 3-1 through 3-5 describe the individual elements' inputs, outputs, and functionality.
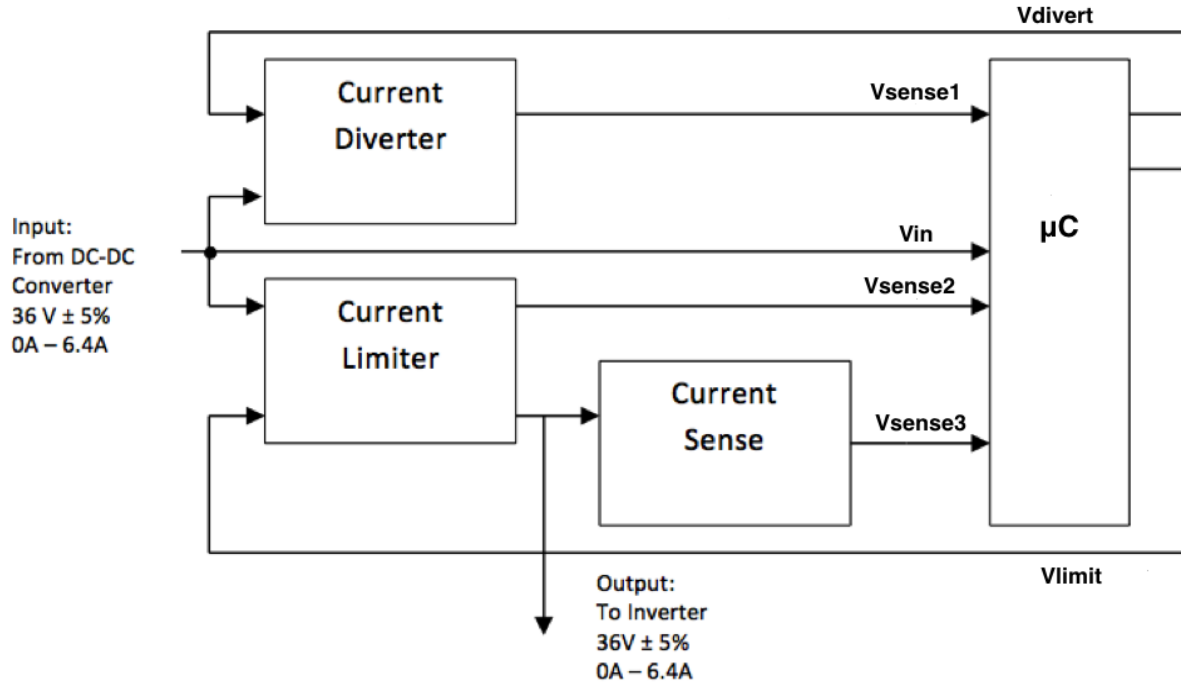
Figure 3-3: Current Protection System Level 1 Block Diagram

Table 3-2: Current Diverter Inputs/Outputs/Functionality

Module	Current Diverter
Inputs	Input signal from DC-DC converter: 36V ± 5%, 0-6.4A Microcontroller output signal
Outputs	ADC output signal to microcontroller
Functionality	This element must divert extra current to maintain an inverter input current of 6.4A.

Table 3-3: Current Limiter Inputs/Outputs/Functionality

Module	Current Limiter
Inputs	Input signal from DC-DC converter: 36V ± 5%, 0-6.4A Microcontroller output signal
Outputs	ADC output signal to microcontroller Output to inverter and current sense: 0-36V, 0-6.4A
Functionality	This element must limit the current to maintain an inverter input current of 6.4A.

Table 3-4: Current Sense Inputs/Outputs/Functionality

Module	Current Sense
Inputs	Input signal from current limiter
Outputs	ADC output signal to microcontroller
Functionality	This element must read the current at the input of the inverter and output a feedback signal to the microcontroller.

Table 3-5: Microcontroller Inputs/Outputs/Functionality

Module	Microcontroller
Inputs	• Input signal from DC-DC converter: 36V ± 5%, 0-6.4A • Input signal from current diverter output • Input signal current limiter output • Input signal from current sense output
Outputs	• Output signal to drive the current diverter • Output signal to drive the current limiter
Functionality	This element must drive both the current diverter and current limiter using given input signals.

4 Project Planning

4.1 Initial Project Planning

The Gantt chart, seen in figure 4-1 below, captures the initial project planning. Initial project planning entailed a minimal amount of time spent on researching topologies and included two design and build iterations. The initial plan did not emphasize isolating any modules from the previous input current protection systems nor does it emphasize the amount of time that integration and testing takes.

Task Name	Start Date	End Date	Days
Initial Design and Research	15-Sep	1-Dec	47
Project Plan	15-Sep	1-Dec	47
Input Protection Development	5-Jan	25-Apr	147
Research Topolgies	5-Jan	19-Jan	14
Collect Data from Elliptical Machine	19-Jan	25-Jan	7
Design and Simulate	26-Jan	25-Feb	21
Shop for and Order Parts	2-Feb	22-Feb	21
Integrate and Test	5-Feb	8-Mar	14
Adjustments and Test	5-Feb	22-Mar	14
Research Other Topolgies	23-Mar	29-Mar	7
Design and Simulate	23-Mar	29-Mar	21
Shop for and Order Parts	13-Apr	3-May	21
Integrate and Test	4-May	17-May	14
Adjustments and Test	18-May	Jun-14	14
Report and Presentation	12-Oct	5-Jun	145
Documentation	13-Oct	5-Jun	145
EE Department Wide Design Review	2-Feb	19-Feb	18
EE 461 Demo and Report	16-Feb	11-Mar	24
EE 462 Demo and Report	4-Apr	26-May	26
Sr. Project Expo Demo and Poster	21-May	4-Jun	15
ABET Sr. Project Analysis	1-Jun	5-Jun	5

Figure 4-1: Projected Project Plan Gantt Chart

4.2 Initial Cost Estimates

Initial cost estimates included costs for two prototypes due to the initial plan of two design and build iterations. Initial cost estimates also assumed the purchase of components for each prototype, without factoring in inherited components from past EHFEM groups.

Table 4-1: Initial Project Cost Estimates

Item	Number	Cost	Justification
Components	$55.00 per prototype	$110	Projecting two build phases
Labor	180 hours	$5400	Estimated labor cost of $30 per hour
Total		$5510	

4.3   Project Planning, Adjusted Time Estimates

As the current protection system project developed, time spent on understanding previous current input protection systems increased relative to time spent on researching various designs. Instead of a second design and build cycle, as shown in figure 4-1, development of a low voltage test took place for defective modules of previous current protection systems. Once the previously defective LT6105 became operable, integration into the overall system took longer than expected due to the time needed to become familiar with Atmel Studios 6 and the Atmel Software Framework built into Atmel Studios (ASF). Figure 4-2 below illustrates the changes between the expected timeline and the actual timeline.

Task Name	Start Date	End Date	Days	Q1 2014			Q2 2015			Q3 2015		
				Sep	Oct	Nov	Jan	Feb	Mar	Apr	May	Jun
Initial Design and Research	15-Sep	1-Dec	47									
Project Plan	15-Sep	1-Dec	47									
Input Protection Development	5-Jan	25-Apr	147									
Research Topologies	5-Jan	19-Jan	14									
Collect Data from Elliptical Machine	19-Jan	25-Jan	7									
Research and Understand Previous Design	26-Jan	25-Feb	30									
Identify Failure of Previous Design	2-Feb	22-Feb	21									
Shop for and Order Parts	5-Feb	8-Mar	14									
Isolate Defected Modules	5-Feb	22-Mar	14									
Design Module Specific Test	23-Mar	29-Mar	35									
Test and Verify Modularly	23-Mar	29-Mar	35									
Modify ASF Code	4-May	5-Jun	31									
Integrate and Test	4-May	5-Jun	31									
Adjustments and Test	18-May	14-Jun	27									
Report and Presentation	12-Oct	5-Jun	145									
Documentation	13-Oct	5-Jun	145									
EE Department Wide Design Review	2-Feb	19-Feb	18									
EE 461 Demo and Report	16-Feb	11-Mar	24									
EE 462 Demo and Report	4-Apr	26-May	26									
Sr. Project Expo Demo and Poster	21-May	4-Jun	15									
ABET Sr. Project Analysis	1-Jun	5-Jun	5									

Figure 4-2: Actual Project Gantt Chart

4.4   Adjusted Cost Estimates

Total costs for this project, as shown in table 4-2 below, differ by $69.72. The unexpected lack of cost for this project results from inheriting components used in previous EHFEM groups. Since the LT6105 represents the only defective module from Cameron and Eric's current input protection system, the author of this report managed to use many of their components, including the ATMEL SAM4SD32 microcontroller.

Table 4-2: Adjusted Cost Estimates

Type of Cost	Item	Quantity	Unit Price ($USD)	Total Price ($USD)	Justification
Fixed	LT6105CMS8#PBF	6	1.38	23.50	2 separate rounds of LT6105 chips purchased as soldering represented a significant challenge
	Proto Board Adapter for MSOP-8	4	2.60	16.78	Each LT6105 needs an adapter
Variable	Labor	-	-	5,400.00	Estimated labor cost of $30 per hour and 180 hours of labor
Total				$5,440.28	Sum of labor and component costs

5   Current Limiter/Diverter Circuit

5.1   Spatial Considerations

Measuring available space in the enclosure allows appropriate size limitations. Available space in the bottom left of the circular enclosure measures as 7" x 3.5" x 4." The Input Current Protection System seeks to meet a size specification of 6" by 3" by 3" to fit within the EFEM enclosure.

5.2   Surface Mount Soldering

This project seeks to get a working Current Input Protection System by first getting the LT6105 High Current Sense Amplifier functioning properly. This entails soldering the SMD component onto a breakout board without causing thermal damage and following ESD protocol. The datasheet [9] specifies a soldering lead temperature time of 10 seconds. With the available soldering equipment soldering any single pin of the LT6105 without causing solder bridges between multiple pins represents a challenge. The most effective soldering tactic found involved a generous amount of flux, a sweep of solder across all pins, followed by light de-soldering to remove solder bridges. Figure 4 below shows an LT6105 soldered onto a breakout board.

Figure 5-1: SMD LT6105 Soldered onto Breakout Board

5.3   High Current Sense Amplifier Test Circuit

The LT6105 worked under a preliminary test, but I sought thorough testing before moving onto attempting to incorporate the high current sense amplifier into the Input Current Protection System. Figure 5-2 shows the original test schematic created for this purpose. Rload, Rin, and Rout values match the output resistances used in the Current Protection System. Note that while current does not ideally flow through Rmatch, some amount of leakage current exists. Rmatch matches Rin to reduce disparity between the voltage potentials seen by pin 8 and pin 1.

Table 5-1: Pin Names and Functions of LT6105 [9]

Pin Names	Pin Functions
P1	Negative Input: V(+IN, -IN) to V⁻ is -9.5V to 44V
P2	Positive rail: 2.85V to 36V
P4	Output of high current sense amplifier: V^- to $(V^- + 36V)$
P5	Negative rail: ground
P8	Positive Input: Max V(+IN, -IN) to V⁻ is -9.5V to 44V

After developing this test schematic, seen below in figure 5-2, the author identified various errors. First, this test seeks to identify that the output voltage increases linearly with an increase in Vsense. This suggests a test setup that consists of directly varying Vsense in a manner that regulates the current flowing through the sense resistor. Secondly, figure 5-2 shows the load connected to Vs+ when the load should attach to Vs- and the input should connect to Vs+. Figure 5-3 shows this necessity due to the need for a higher voltage potential at Vs+ than at Vs- to ensure proper current sensing.
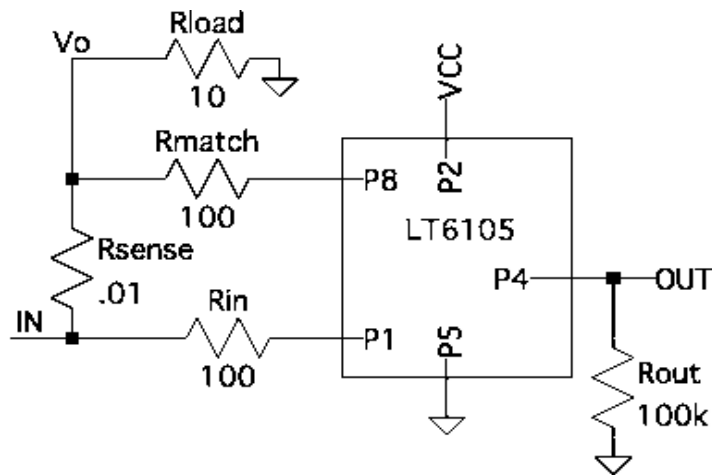
Figure 5-2: High Current Sense Amplifier Test Schematic
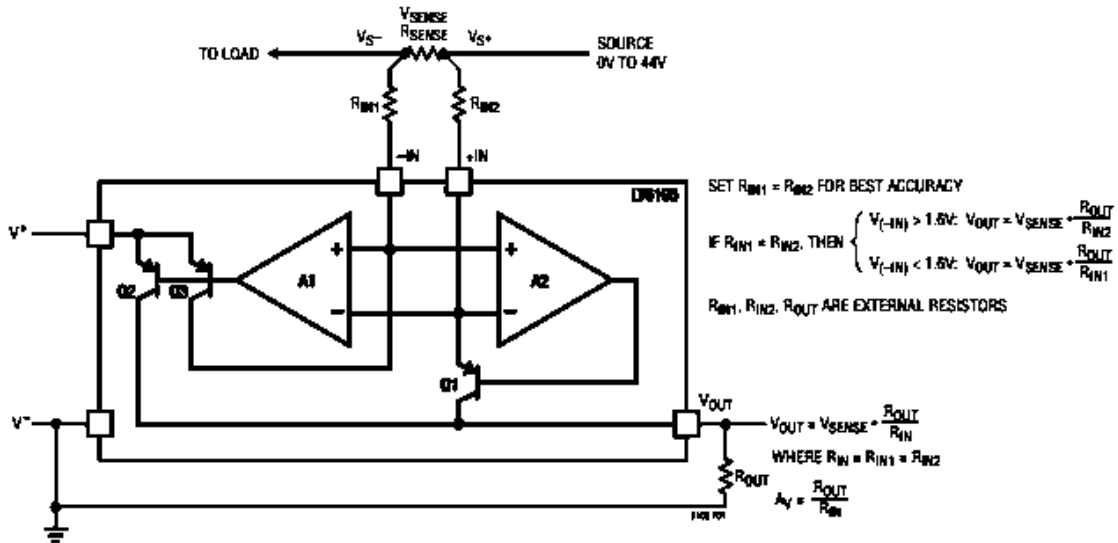
Figure 5-3: Simplified Block Diagram of LT6105

Figure 5-4 below shows the final LT6105 test schematic. By increasing the Rmatch value from 100Ω to 510Ω and by decreasing the Rout value from 100kΩ to 1kΩ, the gain of the sensed current decreased from approximately 100 to approximately 2. The Keithley functions to set Vsense to a known value and to limit the current running through Rsense, ensuring that none of the resistors exceed their ¼ W rating. The resistance values shown in figure 5-4 represent nominal values while table 5-3 reveals the actual resistance values.

Test Equipment

- Agilent E3631A Triple Output DC Power Supply
- Keithley 2401 SourceMeter
- Agilent 33401A Multimeter
- 10Ω, 300W Resistor
- 10 banana-grabber
- 2 alligator clips
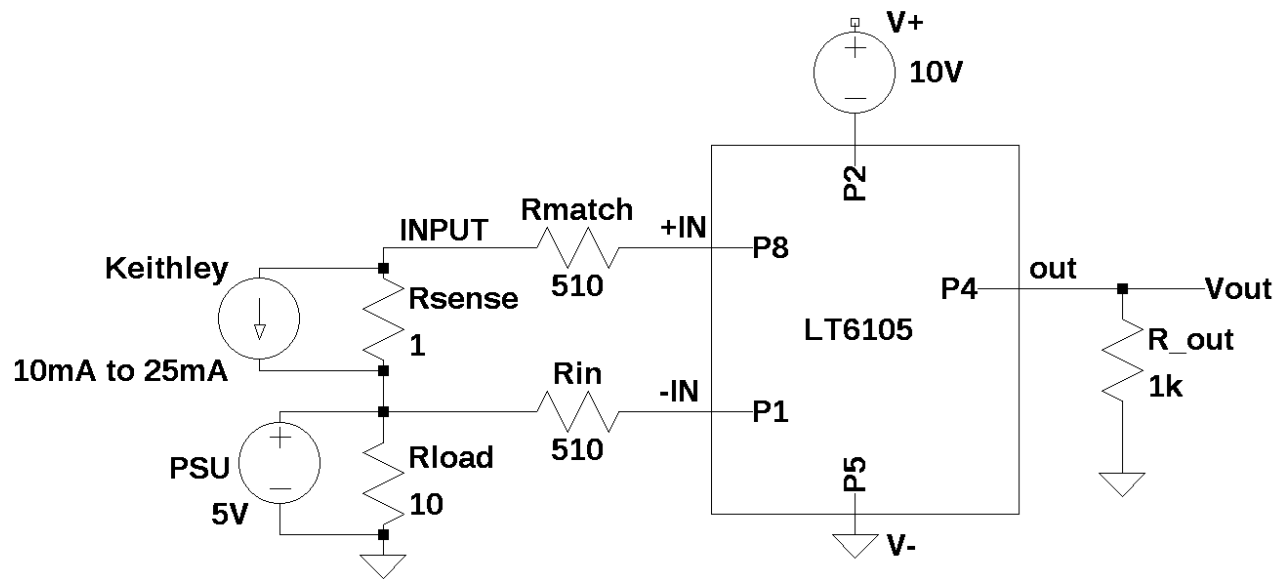
Figure 5-4: Revised High Current Sense Amplifier Test Schematic

$$Av = \frac{Rout}{Rin} = \frac{1000\Omega}{500} = 2 \ (5.1)$$

$$Vout(theoretical) = Vsense * Av \ (5.2)$$

Soldering three LT6105's onto breakout boards ($Vout_1$ through $Vout_3$), developed necessary soldering skill resulting in less thermal exposure in each successive attempt. $Vout_4$ represents the LT6105 that failed in the Eric Funsten and Cameron Kiddoo's senior project. As shown in table 5-4 $Vout_1$ and $Vout_4$ represent damaged modules while table 5-4 confirms $Vout_2$ and $Vout_3$'s functionality.

The minor disparity between $Vout_{theoretical}$ and the measured Vout values implies leakage current through Rin and Rmatch, emphasized by their difference in values. The disparity between V_{out2} and $Vout_3$ results from use of different resistor values for testing the two sensors. Table 5-3 lists the resistance values used in measuring $Vout_2$ as "Setup 2" while "Setup 1" shows the resistance values used in determining $Vout_3$. Two different setups exist because during initial soldering attempts, $Vout_2$ ended up on the breakout board backwards. All other testing used setup 1.

Table 5-2: Measured Vout of LT6105's

V_{sense} (mV)	$Vout_{theoretical}$ (mV)	$Vout_1$ (mV)	$Vout_2$ (mV)	$Vout_3$ (mV)	$Vout_4$ (mV)
20	39.2	7.2	37.12	38.463	0.003
25	49.02	7	46.68	48.04	0.002
30	58.8	10-20	56.19	57.619	0.002
35	68.6	35-40	65.68	67.202	0.003

Measured resistance values, shown below in table 5-3, display values for both setups. These values emphasize that the actual gain and performance of the test schematic should not vary significantly between each other nor do they significantly different from nominal expectations, expressed by equation 5.1 and 5.2.

Table 5-3: Measured Resistance Values

Resistor Name	Setup 1	Setup 2
R_{in} (Ω)	500.7	498
R_{match} (Ω)	500	501
R_{sense} (Ω)	1.07	1.06
R_{out} (Ω)	978	974

5.4 Thermal Considerations

The thermal calculations from previous reports [15] aided in determining whether or not one MS-302-55E heat sink, shown in figure 6-3, suffices as thermal protection for both the FGA180N33ATDTU IGBT [11] and the IXTH96P085T-ND PMOS [12]. The thermal considerations made follow:

$$P_{max} = \frac{Tjmax - TA}{R\theta - R\theta CS - R\theta HA} \text{ (5.3)}$$

Where: P_{MAX} = maximum component power dissipation [W]
T_{JMAX} = maximum junction operating temperature [°C]
T_A = Ambient air temperature [°C]
$R_{\theta JC}$ = junction to case thermal resistance [°C/W]
$R_{\theta HA}$ = Heat sink to ambient (air) thermal resistance [°C /W]

$$R_{\theta HA} = \frac{Tjmax - TA}{Pmax} - R\theta JC - R\theta CS \text{ (5.4)}$$

$$R_{\theta HA}(5.61W) = \frac{(100°C - 25°C)}{5.61\ W} - 0.32° \frac{C}{W} - 0.15° \frac{C}{W} = 12.9° \frac{C}{W} \text{ (5.5)}$$

$$R_{\theta HA}(8.8W) = \frac{100°C - 25°C}{8.8W} - 0.32° \frac{C}{W} - 0.15° \frac{C}{W} = 8.05° \frac{C}{W} \text{ (5.6)}$$

$$R_{\theta HA}(1.6W) = \frac{125°C - 25°C}{1.6W} - 0.42° \frac{C}{W} - 0.15° \frac{C}{W} = 61.93° \frac{C}{W} \text{ (5.7)}$$

From 5.6 and 5.7, the heat sink to ambient values for the IGBT and PMOS follow as $8.05 \frac{°C}{W}$ and $61.93 \frac{°C}{W}$. These values suggest that IGBT requires a heat sink with a thermal resistance less than $8.05 \frac{°C}{W}$. Since the MA-302-55E [13] has a thermal resistance of $3 \frac{°C}{W}$, and because the PMOS only needs a heat sink with a thermal resistance less than $61.93 \frac{°C}{W}$, one heat sink suffices as thermal protection for both the IGBT and the PMOS.

Figure 5-5: MA-302-55E Heatsink [6] [13]

6   Input Current Protection Integration

6.1   Atmel Software Framework

Cameron Kiddoo and Eric Funsten [6] developed the most recent current limiting software, building upon David Braun's work [5], using the SAM4s Xplained Pro Evaluation Kit [3] seen in figure 6.2. This microcontroller utilizes the Atmel Software Framework (ASF), a tool intended to save programmers time by allowing importation of modules, eliminating the need to write various drivers and initialization functions. Unfortunately the ASF modules used in previous reports lacks documentation. This necessitated module discovery using methodical identification of missing header files after compilation, and making educated guesses as to which modules contained the missing files. The author provides the used modules below to save future projects time.

I recommend that anyone using ASF uses Atmel Studios 6.2 (AS). Only AS supports the ASF wizard and attempting to manually import ASF files into alternative IDEs takes time and work. Fully update AS and create a project with the code in Appendix B; opening up the ASF wizard and beginning to import needed modules, automatically creates the "asf.h" header file.

Import all needed modules, then find "conf_uart_serial_.h" by opening the AS solution explorer, expanding the "src" and then "config" folders. Once found, edit "conf_uart_serial_.h" until it matches figure 6.1. Note that this configuration works with the code included in Appendix A, not with the code used by Cameron and Eric [6].

The SAM4S Xplained Pro Evaluation Kit comes with an onboard programmer/debugger. With an updated AS6.2 however, the author of this report found that AS recognized the device, but no programming tool. The following usb installer solved this issue: "distribute.atmel.no/tools/AS6/driver-atmel-bundle-7.0.666.exe". After installation and restarting AS6.2, AS6.2 immediately recognized the debugger.

Now that the code in appendix B can compile, verify communication between the board and Tera Term using commands listed in table 6.1.

Needed ASF Modules
- Generic board support (driver)
- Standard serial I/) (stdio) (driver)
- Analog-to-digital converter (ADC) (driver)
- Digital-to-Analog Converter (DACC) driver
- Real Time Timer (RTT) (driver)
- Watchdog Timer (WDT) (driver)
- General purpose I/O (GPIO) (service)

- General purpose (I/O) (IOPORT) (service)
- Serial interface (USART) (service)

```
/* A reference setting for USART */
/** USART Interface */
#define CONF_UART               USART1
/** Baudrate setting */
#define CONF_UART_BAUDRATE      115200
/** Character length setting */
#define CONF_UART_CHAR_LENGTH   US_MR_CHRL_8_BIT
/** Parity setting */
#define CONF_UART_PARITY        US_MR_PAR_NO
/** Stop bits setting */
#define CONF_UART_STOP_BITS     US_MR_NBSTOP_1_BIT

// Add the definitions below
#define CONF_UART_PIO PINS_UART1_PIO
#define CONF_PINS_UART PINS_UART1
#define CONF_PINS_UART_FLAGS PINS_UART1_FLAGS

#endif/* CONF_USART_SERIAL_H_INCLUDED */
```

Figure 6-1: Needed Defines in "conf_uart_serial.h" for Serial Communication

Figure 6-2: SAM4S Xplained Pro Evaluation Kit (ATSAM4SD32C Microcontroller) [3] [6]

Table 6-1: Available Commands in Current Limiting Test Program [6]

Keyboard Input	Performed Operation
'p'	Print out the 4 ADC values and 2 DAC values
'w'	Increase n_FET_gate DAC value by 1
'W'	Increase n_FET_gate DAC value by 10
's'	Decrease n_FET_gate DAC value by 1
'S'	Decrease n_FET_gate DAC value by 10
'e'	Increase p_FET_gate DAC value by 1
'E'	Increase p_FET_gate DAC value by 10
'd'	Decrease p_FET_gate DAC value by 1
'D'	Decrease p_FET_gate DAC value by 10
'1'	Test p_FET_gate
'2'	Test n_FET_gate
'r'	Run the current limiting test program
'R'	N_FET_gate set to 200 and p_FET_gate set to 1900

6.2 Current Limiter/Diverter Circuit

The current limiter/diverter circuit design comes from Dr. Braun's Sabbatical Report [4], seen in figure 6-3. While this project confirmed the operation of the LT6105, high current sensing module, integration of the LT6105 within the overall current limiter/diverter circuit necessitates understanding the system as a whole. Figure 6-3 shows nodes V_{in}, V_{dn}, V_{dp}, and $Vout_{6105}$, key voltages sent to ADC's that allow microcontroller processing. These four voltages determine the DAC channel outputs from the microcontroller. This allows the microcontroller to turn off the PMOS if it senses an overcurrent condition of greater than 6.4A. When the PFET turns off, the IGBT turns on, in order to divert the extra power safely. Note that a zener diode, with a reverse voltage breakdown of 20V, sits on the gate of the PMOS because the PMOS has a maximum V_{GS} of 20V. [12]
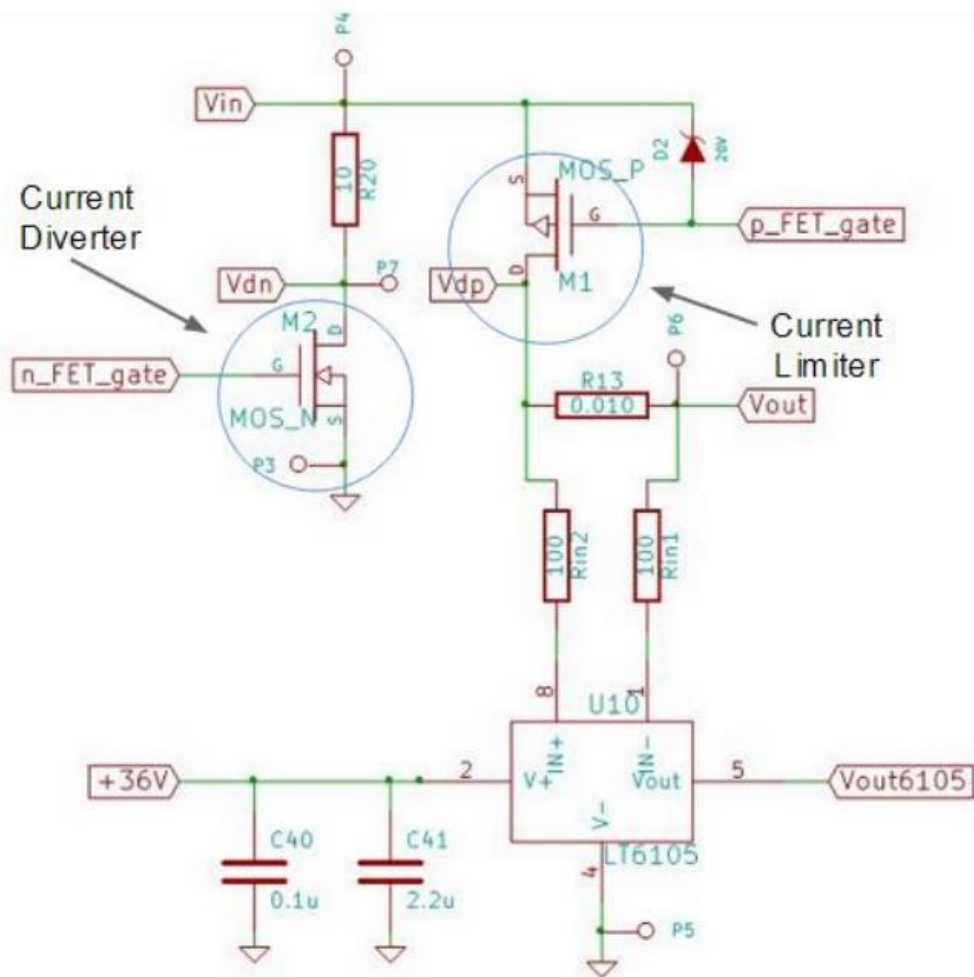
Figure 6-3: Current Limiter/Diverter Circuit [5] [6]

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Figure 6-4 displays a built current limiter/diverter from Cameron and Eric's project [6]. Two discrepancies found in this diagram follow: first, the connection shown at pin 6 of the $Vout_{6105}$ should connect to pin 5, (shown in figure 6-3) and secondly, switch pins 2 and pins 3 on the MAX9632 (shown by figure 6-5). These errors occur in figure 6-4. Figures 6-3 and 6-5 show correct pin. The previous corrections seek to correct figure 6-4, causing figure 6-4 to correctly represent figures 6-3 and 6-5.

Figure 6-4 includes the voltage followers and voltage dividers, seen in Figure 6-6, which condition the four key voltages before the microcontroller can read them.
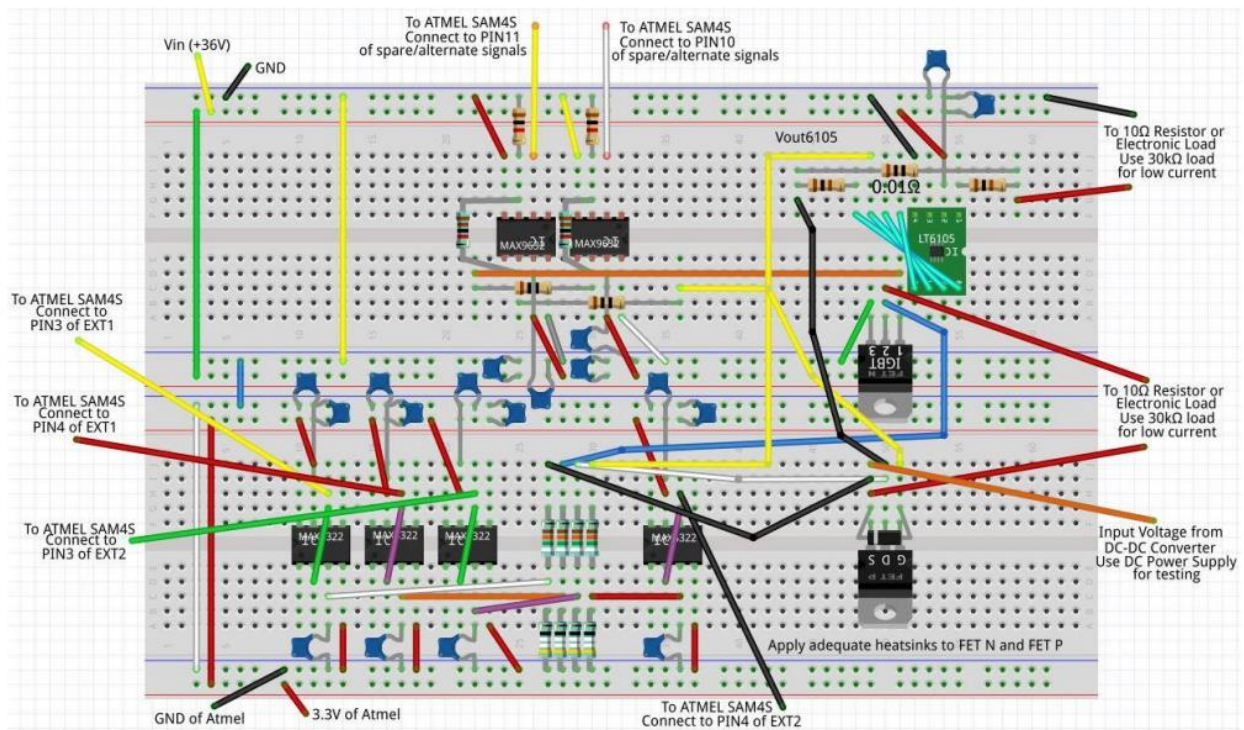
Figure 6-4: Breadboard Layout of Current Limiter Circuit (Not to Scale) [6]
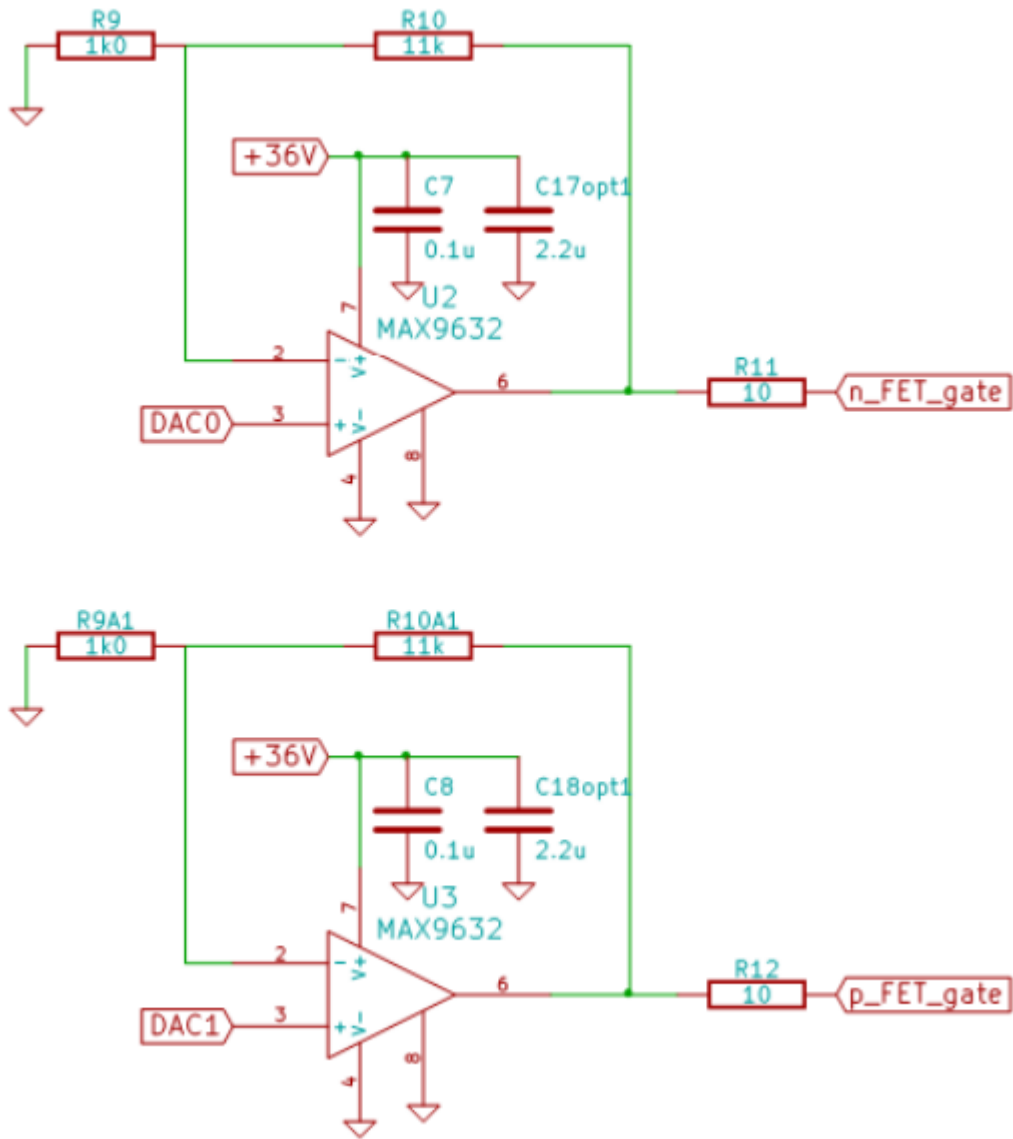
Figure 6-5: Non-Inverting Amplifiers for DAC Outputs (Gain = 12) [5] [6]
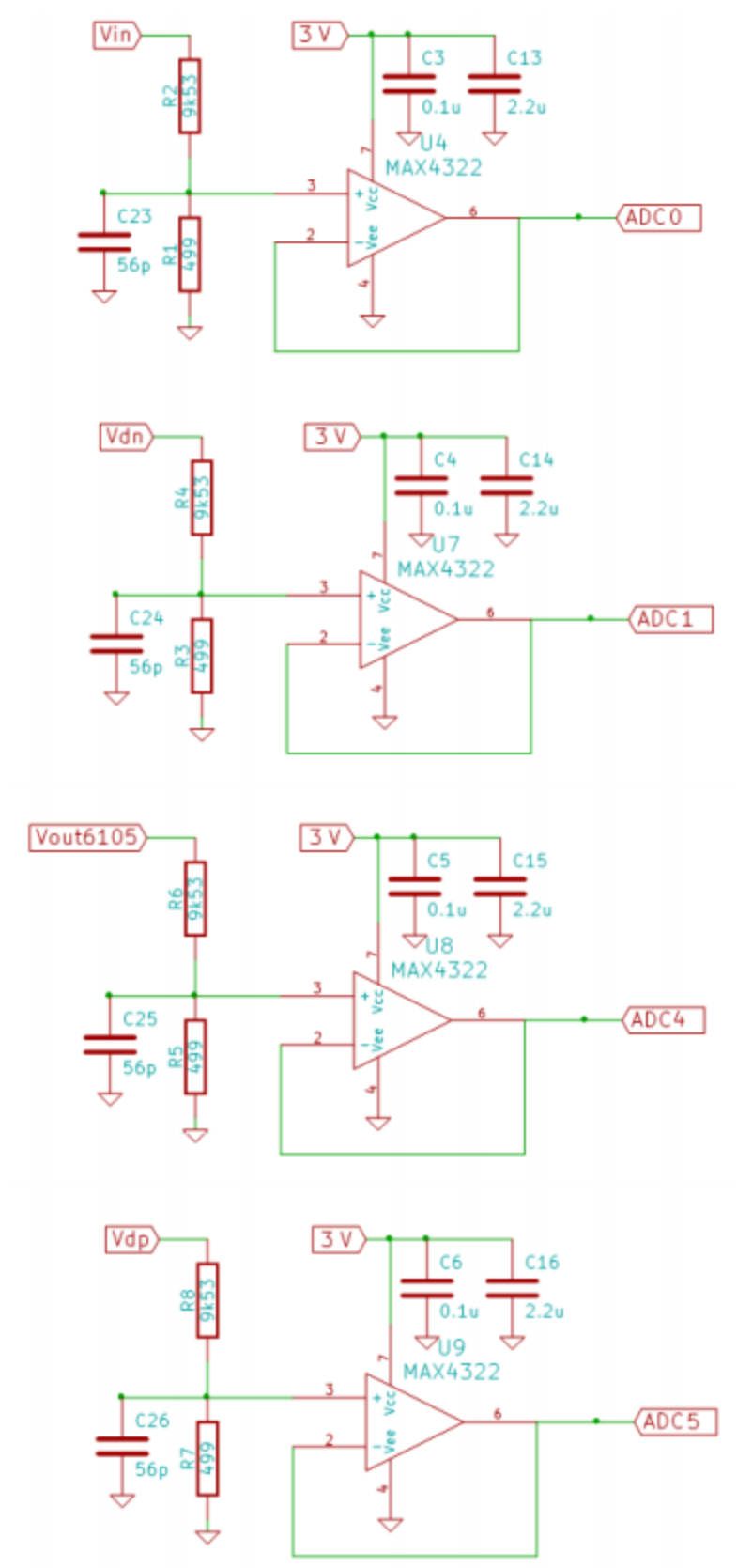
Figure 6-6: Voltage Followers and Voltage Dividers for ADC Inputs [5] [6]

6.3   Current Protection System Testing

Testing began by verifying that pins 10 and 11 on the Atmel SAM4S output voltages corresponding to the output seen on Tera Term, when the 'p' command runs. Using a multi-meter, measurements of pins 10 and 11 (the two "DAC Values") showed pin 10 and pin 11 at 0.55V, when Tera Term reported DAC Values of 0. Next, running command 'R' sets the DAC values to 200 and 1900, increasing pin 10 to 0.67V, while pin 11 increases to 1.58V. This shows that the code successfully controls the voltages output to the gates of the IGBT and the PMOS.

With the code, microcontroller, and LT6105 module verified as working, the wiring diagram consulted, and the previously mentioned errors discovered, the system integration can start. However, once the microcontroller outputs connect as DAC inputs, the author found that, regardless of whether the pin 11 output 0.55V or 1.58V, the output of the MAX9632 stayed at 11.4V. Observation, by touch, of the MAX9632 revealed that significant heat dissipation took place. Based on these observations, the MAX9632 incurred damage that prevents the microcontroller from regulating the IGBT and the PMOS.

Testing of the MAX9632's buffer amplifiers followed. Characterizing the MAX9632's in a non-inverting amplifier setup, show in figure 6-5, using 1k resistors for the voltage divider, resulted in the data displayed in table 6-3. Table 6-2 shows the pin names and function. The chosen resistors provide a gain of 2, shown by $OUT_{THEORETICAL}$. The data shows that the MAX9632 used to amplify and buffer the signal to the PMOS operates as expected, but the MAX9632 corresponding to the IGBT stopped functioning. This MAX9632 corresponds to the chip that showed significant heat dissipation, further suggesting that this amplifier incurred damage.

Further investigation of the MAX9632 revealed that a solder joint had become unconnected, likely from moving the MAX9632's between boards. After touching up the MAX9632 solder joints, both amplifiers began functioning as expected. Table 6-3 shows the MAX9632 test results before the soldering touchup as OUT_{IGBT} while $OUT2_{IGBT}$ shows test results after the soldering touchup. The MAX9632's underwent verification in the current protection system, and output voltages with a gain of 12 with respect to their inputs.

While testing the current protection system, the input must come from a power supply capable of supplying significant current. Using a suitable power supply, current limiting became operational, as shown in table 6-5. The IGBT and PMOS dissipated a maximum of 69W and a minimum of 41.2W in the last case. The performed tests included changing the hard coded values of "v_sense_goal" and "seek_v" in the code

found in appendix A, to the values shown in table 6-5. The current limiting program, initiated with command 'r', allowed current regulation based on the chosen value of "v_sense_goal." Table 6-5 represents these chosen values as V_{GOAL} and shows the input voltage and supply current sourced by a power supply. V_{OUT} limiting to a value similar to V_{GOAL} reveals successful testing. This shows successful current limiting to the DC-DC converter. Note the author learned that the code needs a printing statement for the current limiting program to function properly, Cameron and Eric's report [6] confirms this.

The primary addition this project seeks to accomplish, integration of a working LT6105 into Cameron and Eric's previous current limiting system, and verification of the LT6105 within the current limiting system took place, as shown in table 6-4. Table 6-4 reports a higher V_{OUT} for a V_{SENSE} of 17.3mV as opposed to 18mV. Difficulty in getting accurate measurements across the sense resistor results in this. Table 6-4 confirms a linear relationship between V_{SENSE} and V_{OUT} on a scale of volts. With a larger resistor as V_{SENSE}, confirmation of a linear relationship on the scale of volts could take place.

In considering timing, remove all printing statements from the code found in appendix B. Then using the RTT timer reveals the time it takes to read all four ADC's. At about 5µs, meeting the timing requirements for the current protection system.

Table 6-2: Pin Names and Functions of MAX9632 [17]

Pin	Name	Function
P1, P5	N.C.	Not Connected
P2	IN-	Negative Input ((V_{EE} – 0.3V) to (V_{CC} +0.3V))
P3	IN+	Positive Input ((V_{EE} – 0.3V) to (V_{CC} +0.3V))
P4	V_{EE}	Negative Supply Voltage (ground)
P6	OUT	Output ((V_{EE} – 0.3V) to (V_{CC} +0.3V))
P7	V_{CC}	Positive Supply Voltage (4.5 to 36V)
P8	SHDN	Active-High Shutdown (V_{EE} to V_{CC})

Table 6-3: Measured Outputs of MAX9632's

V_{IN} (V)	$OUT_{THEORETICAL}$ (V)	OUT_{PMOS} (V)	OUT_{IGBT} (V)	$OUT2_{IGBT}$ (V)
1	2	1.978	1.981	1.96
1.5	3	2.98	1.981	2.96
2	4	3.963	1.981	3.89
2.5	5	4.95	1.982	4.93
3	6	5.94	1.982	5.93
3.5	7	6.93	1.984	6.94

Table 6-4: Vsense and Vout of LT6105 (Gain of 100)

V_{SENSE} (mV)	V_{OUT} (V)
5	5.3
17.3	18.1
18	17.8

Table 6-5: Current Limiting Data with LT6105

V_{IN} (V)	I_{SUPPLY} (A)	$V_{(GOAL)}$ (ADC)	$V_{(GOAL)}$ (V)	V_{OUT} (V)	I_{OUTavg} (A)
20	3.7	600	9.73	9.8	1.749
20	3.71	700	11.35	11.3	1.72
20	3.69	800	12.97	13.11	1.49
20	3.6	900	14.59	14.62	1.55
20	3.59	1000	16.21	17.51	1.725

Test Equipment [6]

- BK Precision 9153 60V/9A 540W Programmable DC High Power Supply (20V)
- Two 10Ω resistors rated for 300W
- Agilent E3630A Triple Output DC Power Supply (24V)
- Agilent MSO-X 2012A mixed Signal Oscilloscope
- Agilent U3606A Multimeter
- Atmel SAM4S Xplained Pro Microprocessor
- Current limiting circuit
- 4 banana-grabber
- 2 spade-banana
- 4 banana-banana
- 2 scope probe
- MA-302-55E Heatsink
- 8 alligator clips
- Laptop running Tera Term and AS6.2
- Microcontroller code (Appendix B)

7 Conclusion and Future Projects

The input current protection system created by Cameron Kiddoo and Eric Funsten [6] demonstrated significantly improved efficiency over the previous design developed by Zack Weiler and Ryan Turner [7]. The current sense circuit also adheres to the specifications outlined by Byung Yoo and Sheldon Chu [16]. While Cameron and Eric verified their design in theory, a primary issue with their input protection circuit resided in the lack of a functioning high current sense amplifier. This project aimed to improve upon this previous project by identifying the cause of failure for their high-current sense amplifier and implementing an input current protection system with a functioning high-current sense amplifier.

Chapter 5 details the final test schematic developed to verify high-current sense amplifiers separate from the overall current input protection system. The final design of this test schematic allows for high-current sense amplifier verification without using high voltage. This allowed the definitive determination of the inoperability of Cameron Kiddoo's and Eric Funsten's high-current sense amplifier inoperable, eliminating the possibility that the issue they encountered merely involved integrating a working high-current sense amplifier into the overall input current protection system. This confirms the suspicion that their high-current sense amplifier became damaged from exposure to ESD or overheating.

Chapter 6 details this projects attempts at integrating working high current sense amplifiers into the input current protection system previously verified by Cameron and Eric. This report provides verification of the LT6105 verification within the current limiting protection system and the current protection system meets specifications. Future projects would do well to convert the working design to a printed circuit board and to look at improving the software used for current limiting. Incorporating the current limiting system with a voltage protection circuit implies the need for adjustments to the software. The author of this report recommends that any future projects seeking to improve upon the software relied upon by this input current protection system consist of someone familiar with Atmel Studio's ASF.

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A. **APPENDIX — ANALYSIS OF SENIOR PROJECT DESIGN**
Project Title: Current Protection for Energy Harvesting for Exercise Machines (EHFEM)
Student's Name: **Colton Crivelli**
Advisor's Name: **David Braun**

1. Summary of Functional Requirements

The current limiting system for the EHFEM prevents the DC-DC converter from drawing more than 6.4A and allows overcurrent conditions for no longer than 100μs [6]. The current limiting system design allows the overall machine to pay itself off after 35,000 hours of use, assuming PG&E rates and an operation intensity of 10 watts per hour. Lastly, the protection circuit should have an area no greater than 6" by 3" by 3 and an average current protection circuit should operate for 10 years without failure.

2. Primary Constraints

Implementing a circuit protection system for an EHFEM presented a challenge because the circuit must perform quickly, efficiently, at must not cost more than $25. This price budget implies that the component count needs to remain low, which limits the design complexity. Similarly, cost constrains microcontroller options for interfacing with the inverter, and the microcontroller directly affects the response time of the protection circuit. Time also constrains this project; the project seeks completion by June 1th, 2015.

3. Economic

Human Capital and Financial Capital
An affordable exercise machine that pays itself off would catch they eyes of all recreational centers, gyms, studios, and fitness or environmental enthusiasts around the world. Individuals concerned with saving money in the long run and/or environmental conscious individuals would have an incentive to update or replace all of their current exercise machines with EHFEM. However, individuals invested in the oil industry may oppose the EHFEM. Since the product supplies the grid with electrical energy, it could negatively affect companies in competition with PG&E; financial capital could shift from alternative energy sources to the grid.

Manufactured or Real Capital
Manufacturers of exercise machines would need to augment their current processes to accommodate the designs of an EHFEM. Similarly, manufacturing companies that design electrical boards, components, inverters, and microcontrollers gain business.

Natural Capital
The prospect recreational centers filled with hundreds of EHFEM systems, used by people up to 14 hours a day, has significant implications for natural capital. A new source of electrical energy for the grid could reduce the ways that companies

manipulate nature to produce energy (i.e. Hoover Dam). Providing another source of energy for the electric grid could cause electric energy use over other energy sources, such as oil. A decrease in oil takes a step towards conserving the Earth's natural resources. Bio capacity, in general, would increase since the prospect of a widely used EHFEM would provide a widespread renewable energy source.

Costs

Costs of the project's lifestyle include the design, assembly, and manufacturing of the product. Once a customer has a finished product, it ceases to tax any resources or cost the customer. The benefits of the project begin once a customer has the product. The customer gets the benefit of having an exercise machine and the perpetual benefit of increasing bio-capacity and making money as the customer uses the product. This analysis assumes that the customer considers the use of the product as a benefit.

Inputs of using the product consist of a person peddling the EHFEM. The inputs of this project consist of labor and components used to create an intelligent and effective design. The project costs all students and the project coordinator (David Braun) time. CPSLO pays for a portion of the components needed to produce the EHFEM. Manufacturing EHFEM's on a large scale after product development causes a cost transition to the individual attempting to sell the EHFEM's. Note that the project costs the environment very little (limited to the materials used in manufacturing an EHFEM).

Table A-1: Initial Project Cost Estimates

Item	Number	Cost	Justification
Components	$55.00 per prototype	$110	Projecting two build phases
Labor	180 hours	$5400	Estimated labor cost of $30 per hour
Total		$5510	

Table A-2: Total Project Costs

Type of Cost	Item	Quantity	Unit Price ($USD)	Total Price ($USD)	Justification
Fixed	LT6105CMS8#PBF	6	1.38	23.50	2 separate rounds of LT6105 chips purchased as soldering represented a significant challenge

	Proto Board Adapter for MSOP-8	4	2.60	16.78	Each LT6105 needs an adapter
Variable	Labor	-	-	5,400.00	Estimated labor cost of $30 per hour and 180 hours of labor
Total				$5,440.28	Sum of labor and component costs

Equipment needed to development the EHFEM consists of measuring and assembling equipment such as: an oscilloscope, power supply, multi-meter, ammeter, simulation software, and soldering stations, however CPSLO provides necessary equipment for this project.

The finish project provides energy back to the electric grid. PG&E purchases the energy generated from the EHFEMs; both PG&E and the seller of the energy generated by the exercise machines profit from this.

Product improvements take place year-to-year, by students and Dr. Braun, until we produce a cost-effective product that meets all marketing requirements. Products exist until a mechanical or electrical failure occurs, after at least ten years, or until an improved version incentivizes product replacement.

Fall 2014

Task Name	Start Date	End Date	Days	Sep	Oct	Nov	Jan	Feb	Mar	Apr	May	Jun
Initial Design and Research	15-Sep	1-Dec	47									
Project Plan	15-Sep	1-Dec	47									
Input Protection Development	5-Jan	25-Apr	147									
Research Topolgies	5-Jan	19-Jan	14									
Collect Data from Elliptical Machine	19-Jan	25-Jan	7									
Design and Simulate	26-Jan	25-Feb	21									
Shop for and Order Parts	2-Feb	22-Feb	21									
Integrate and Test	5-Feb	8-Mar	14									
Adjustments and Test	5-Feb	22-Mar	14									
Research Other Topolgies	23-Mar	29-Mar	7									
Design and Simulate	23-Mar	29-Mar	21									
Shop for and Order Parts	13-Apr	3-May	21									
Integrate and Test	4-May	17-May	14									
Adjustments and Test	18-May	Jun-14	14									
Report and Presentation	12-Oct	5-Jun	145									
Documentation	13-Oct	5-Jun	145									
EE Department Wide Design Review	2-Feb	19-Feb	18									
EE 461 Demo and Report	16-Feb	11-Mar	24									
EE 462 Demo and Report	4-Apr	26-May	26									
Sr. Project Expo Demo and Poster	21-May	4-Jun	15									
ABET Sr. Project Analysis	1-Jun	5-Jun	5									

Figure A-1: Original Estimated Development Time

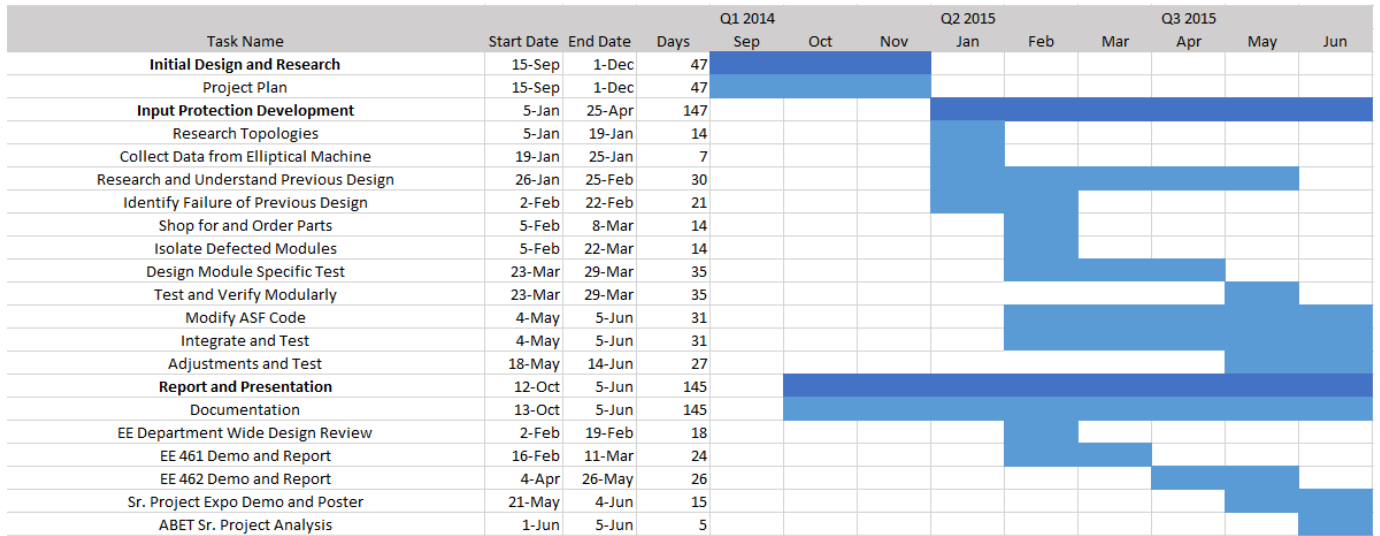| Task Name	Start Date	End Date	Days	Q1 2014			Q2 2015			Q3 2015		
				Sep	Oct	Nov	Jan	Feb	Mar	Apr	May	Jun
Initial Design and Research	15-Sep	1-Dec	47									
Project Plan	15-Sep	1-Dec	47									
Input Protection Development	5-Jan	25-Apr	147									
Research Topologies	5-Jan	19-Jan	14									
Collect Data from Elliptical Machine	19-Jan	25-Jan	7									
Research and Understand Previous Design	26-Jan	25-Feb	30									
Identify Failure of Previous Design	2-Feb	22-Feb	21									
Shop for and Order Parts	5-Feb	8-Mar	14									
Isolate Defected Modules	5-Feb	22-Mar	14									
Design Module Specific Test	23-Mar	29-Mar	35									
Test and Verify Modularly	23-Mar	29-Mar	35									
Modify ASF Code	4-May	5-Jun	31									
Integrate and Test	4-May	5-Jun	31									
Adjustments and Test	18-May	14-Jun	27									
Report and Presentation	12-Oct	5-Jun	145									
Documentation	13-Oct	5-Jun	145									
EE Department Wide Design Review	2-Feb	19-Feb	18									
EE 461 Demo and Report	16-Feb	11-Mar	24									
EE 462 Demo and Report	4-Apr	26-May	26									
Sr. Project Expo Demo and Poster	21-May	4-Jun	15									
ABET Sr. Project Analysis	1-Jun	5-Jun	5									

Figure A-2: Actual Project Plan Gantt Chart

After integration into the California Polytechnic recreational, EHFEM manufacturing could take place on a large scale, allowing public use.

4. Commercial Manufacturing

Table A-3: Profit per Year and Cost for user Over Time

≈ devices sold per year	≈ manufacturing cost per device ($)	≈ purchase price per device ($)	≈ profit per year ($)	≈ cost for user after 10 years ($)
1,000	50	75	25	0

Note the manufacturing cost per device and the purchasing price per device, as displayed in table A-2, only represent the cost of the input current protection circuit. Conversely, the cost to the user after ten years represents the system in its entirety. A user buys an EHFEM machine for approximately $500, after which constant use of the elliptical trainer at an average rate, for ten years, would result in the user earning $500 for the energy produced. Each year, the user of the machine makes 1/10 of the cost of the machine and after the tenth year of using the machine, the owner makes money. This continues until a mechanical or electrical failure causes the owner to fix or replace the machine (this shouldn't happen until after the ten year period).

5. Environmental

The EHFEM project seeks to create a product that affects the environment merely in use; the product improves bio-capacity by creating a renewable energy source for the electric grid. Environmental impacts associated with the manufacturing of the product consist of the materials needed to construct the mechanical and electrical components of the exercise machine.

Assuming a purely mechanical final iteration of the EHFEM, except for the electrical components that convert the operation of the machine into energy that goes into the grid, this project limits direct use of natural resources to materials used to create the machine. This includes resources such as metal, aluminum, rubber, or other material for the machines frame, and resources such as silicon, copper, and metals used for the electrical components.

By creating a renewable energy source for the electric grid, the EHFEM saves natural resources. Apart from the minimal amount of natural resources that the product's manufacturing requires, it does not harm any ecosystems or rely on the continuing use of any natural resources.

This project impacts all species by improving general bio-capacity. By providing the electric grid with an additional renewable source, this product has the potential to mitigate the use of energy sources that tax natural resources. If the use of energy sources that tax natural resources decreases significantly, life everywhere, for all ecosystems, could become more sustainable which would affect every species in every ecosystem; in other words, every species benefits, albeit in a minimal fashion.

6. Manufacturability

The EHFEM project seeks to develop a prototype that meets all marketing specifications, while spending the least amount. This has led to the use of donated components, such as the inverters. This leads to future challenges in manufacturing, because the components used to create a functioning prototype differ from ideal components for mass manufacturing, resulting in necessary tweaks and design adjustments before manufacturing can take place. Integrating the electrical components that allow energy conversion into a suitable design for an exercise machine represents another challenge.

7. Sustainability

The only issues that maintaining the completed system, over the maintenance of a standard exercise machine, relates to the energy conversion circuitry. With proper protection of electrical components and temperature regulation, product maintenance should not increase significantly.

This project directly impacts the sustainable use of resources, because it provides a new renewable supply of electrical energy. This means that the use of electrical energy becomes more sustainable.

Upgrades that would improve the design of the project would make the energy conversion more efficient and/or eliminate the number of necessary components, both of which would improve the overall cost-effectiveness of the system. This project seeks to find a simpler, cleverer design; a more efficient design that also uses less components.

8. Ethical

The environmental impacts due to the EHFEM cause numerous ethical implications. Looking through the framework of Kant's Categorical Imperative, if an individual does not actively seek to promote renewable sources of energy, he or she fails to improve bio-capacity. Without an improvement in bio-capacity the Earth becomes unsustainable and humans die. Deduction shows if an individual does not choose to promote an EHFEM, they choose not to improve the world's bio-capacity, implying that they choose to let human's dies. Kant's Categorical Imperative reasons it unethical to oppose the EHFEM product because it could prevent death.

Psychological egoism similarly supports the EHFEM project, because they make the customer money after ten years of use. Monetary self-interest and environmental self-interest both support the EHFEM project.

The IEEE Code of Ethics states that the members of IEEE aim "to improve the understanding of technology, its appropriate application, and potential consequences." The EHFEMs seeks to accomplish these same goals in the sense that it attempts to improve upon the already existing technology of exercise machines. Furthermore, it's attempting to apply energy-converting technology to an exercise machine in order to create a renewable source—an appropriate and positive application.

9. Health and Safety

The EHFEM project seeks to meet safety requirements [5]. Since this product consists of more electrical components than a standard exercise machine, the project seeks to ensure component isolation and temperature regulation.

10. Social and Political

Social and political issues stem from the EHFEM project seeking to create a renewable energy source for the electric grid; it should have significant social impact to anyone concerned with the environment. Social groups that aim to further the conscientious use of natural resources would want to promote EHFEM's.

Direct stakeholders of the EHFEM project consist of Cal Poly SLO, David Braun as the project advisor, and the numerous students working on creating an EHFEM system that meets all marketing requirements. Since the project has potential to significantly impact the environment, every living thing on Earth seen as an indirect stakeholder. Environmental decline affects everyone. On a smaller scale, exercise enthusiasts and gym owners represent stakeholders in EHFEM systems because they could decrease the cost of a large portion of their equipment (in the long run).

This project has the potential to harm industries, or individuals invested in these industries, which rely on the use of natural resources as a source of energy— exemplified by the oil industry. Assuming that EHFEMs made electrical energy considerably more sustainable it could push society into mitigating oil as a primary use of energy, which would harm those involved in oil industries.

This project benefits the masses by potentially improving bio-capacity. It also benefits everyone that uses exercise machines by creating an economically friendly version that has the potential to pay itself off.

All stakeholders that benefiting from improved environmental health have equal stake because bio-capacity improves for everyone. This assumes EHFEM manufacturing takes place worldwide and that energy companies in all countries cooperate with the idea of using the machine as a renewable energy source. If product manufacturing stayed in America, or if some energy companies reject it, than not all areas would benefit from the project. Stakeholder benefit inequality stems from differing economic power. An EHFEM costs hundreds of dollars more than a standard exercise machine, but pays itself off after ten years of use. This means that the product benefits those that have enough money to make the initial investment of buying the EHFEM over a standard exercise machine.

11. Development

A primary analysis technique that I have learned during the course of the project consists of Monte Carlo analysis to account for the variances in performance of a system due to component tolerances. Other techniques that I have learned include capacitive filtering to prepare the signal that enters the current input protection circuit, and using an Atmel SAM4s microcontroller requires learning how to implement the Atmel Software Framework [6]. The literature represents personal development because each article seeks to answer and support specific questions encountered during the EHFEM project.

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B. APPENDIX — Microcontroller Code

```
/**
 * Project: Current Limiter
 * Description: This program utilizes four ADC channels (EXT1:Pins 3 and 4, EXT2:Pins 3 and 4)
 * which are connected to voltage buffers, and two DAC channels (SPARE1:Pins 10 and 11) which
 * are connected to x12 gain non-inverting op-amps. The goal of this program is to drive two
 * transistors (IGBT and PMOS) in order to limit the current from the output of a DC-DC
 * converter to an inverter. It was tested on a ATSAM4SD32C microcontroller using the SAM4S
 * Xplained Pro Evaluation Kit.
 * Modifications made to Dr. Braun's source code included.
 * Last Updated: 6/7/14
 */
/*
 * Include header files for all drivers that have been imported from
 * Atmel Software Framework (ASF).
 */
#include <asf.h>
#define ADC CLOCK 22000000
#define n_FET_gate_max 200

int counter;
uint16_t n_FET_gate = 0;
uint16_t p_FET_gate = 0;
uint32_t v_in;
uint32_t v_dn;
uint32_t v_dp;
uint32_t v_sense;

static volatile uint16_t seek_v = 1000;           // Voltage goal for set point
static volatile uint16_t v_sense_goal = 1000;     // ADCA0 setting when I_SENSE equals the goal
// (i goal) "12" bit
static volatile uint16_t v_sense_i_min = 500;     // ADCA0 setting when I_SENSE equals the minimum
// current where the nFET turns off "12" bit
static volatile uint16_t v_sense_i_max = 1300;     // ADCA0 setting when I_SENSE equals the minimum current
// where the nFET turns on fully (4095) "12" bit
static volatile uint16_t v_in_dac1;               // DAC1 bits corresponding to maximum Vin
static volatile uint16_t v_in_20V_dac = 2060;     // DAC1 bits corresponding to 20V on Vin
static volatile uint16_t v_in_dac_delta;          // temporary variable
 * interrupt.
 */
static void configure_rtt(void)
{
        uint32_t ul_previous_time;

        // configure RTT for a 1 second tick interrupt
        rtt_init(RTT, 1);
```

```c
        ul_previous_time = rtt_read_timer_value(RTT);
        while (ul_previous_time == rtt_read_timer_value(RTT));
}


// configure UART console
static void configure_console(void)
{
        const usart_serial_options_t uart_serial_options = {.baudrate = CONF_UART_BAUDRATE, .paritytype = CONF_UART_PARITY};

        // configure console UART
        sysclk_enable_peripheral_clock(CONSOLE_UART_ID);
        pio_configure_pin_group(CONF_UART_PIO, CONF_PINS_UART, CONF_PINS_UART_FLAGS);
        stdio_serial_init(CONSOLE_UART, &uart_serial_options);
}


/**
* ADC Interrupt Handler
* Reads in from 4 ADC channels and outputs to two DAC channels
*/
void ADC_Handler(void)
{
        uint32_t status;
        uint8_t done = 0;
        uint32_t dac_val = 0;

        // Check the ADC conversion status
        if ((adc_get_status(ADC) & ADC_IER_EOC5) == ADC_IER_EOC5)
        {
                // Get latest digital data value from ADC and can be used by application
                v_in = adc_get_channel_value(ADC, ADC_CHANNEL_0);
                v_dn = adc_get_channel_value(ADC, ADC_CHANNEL_1);
                v_dp = adc_get_channel_value(ADC, ADC_CHANNEL_4);
                v_sense = adc_get_channel_value(ADC, ADC_CHANNEL_5);
                adc_start(ADC);

                // write DAC values to both DAC channels (Channel 0: n_FET_gate, Channel 1: p_FET_gate)
                done = 0;
                while(!done)
                {
                        status = dacc_get_interrupt_status(DACC);
                        // if ready for new data
                        if ((status & DACC_ISR_TXRDY) == DACC_ISR_TXRDY)
                        {
                                dac_val = (0xFFF & n_FET_gate) | 1 << 28 | (0xFFF & p_FET_gate) << 16;
                                dacc_write_conversion_data(DACC, dac_val);
                                done = 1;
                        }
                }
                //uncomment for RTT timing
                //printf("Output: %x\n\r", dac_val);
```

```c
            /*if(++counter == 10000)
            {
                    printf("Time: %u\n\r", (unsigned int)rtt_read_timer_value(RTT));
                    counter = 0;
                    configure_rtt();
            }*/
        }
}

// configure ADC
static void adc_setup(void)
{
        sysclk_enable_peripheral_clock(ID_ADC);

        adc_init(ADC, sysclk_get_cpu_hz(), ADC_CLOCK, 6);
        adc_configure_timing(ADC, 0, ADC_SETTLING_TIME_3, 1);
        adc_set_resolution(ADC, ADC_MR_LOWRES_BITS_12);

        adc_enable_channel(ADC, ADC_CHANNEL_0);
        adc_enable_channel(ADC, ADC_CHANNEL_1);
        adc_enable_channel(ADC, ADC_CHANNEL_4);
        adc_enable_channel(ADC, ADC_CHANNEL_5);
        NVIC_EnableIRQ(ADC_IRQn);
        adc_enable_interrupt(ADC, ADC_IER_EOC5);
        adc_configure_trigger(ADC, ADC_TRIG_SW, 0);
        //adc_configure_trigger(ADC, ADC_TRIG_SW, ADC_MR_FREERUN_ON);
}

// configure DAC
static void dacc_setup(void)
{
        sysclk_enable_peripheral_clock(ID_DACC);
        dacc_reset(DACC);
        dacc_set_transfer_mode(DACC, 1);
        dacc_set_power_save(DACC, 0, 0);
        dacc_set_timing(DACC, 0x08, 0, 0x10);
        dacc_enable_flexible_selection(DACC);
        dacc_enable_channel(DACC, 0);
        dacc_enable_channel(DACC, 1);
}

/************************************************************************
 * scale DMM to ADC -- given a DAC value, provides the 12 bit ADC
 * value that should measure the same
 *
 * Parameters
 * DMM val DMM reading
 * adc_gain gain on ADC input (likely < 1.0)
 *
 * Returns
 * adc val 12 bit adc reading corresponding to the dac value
```

```c
*********************************************************************/
int16_t scale_DMM_to_ADC(float DMM_val, float adc_gain)
{
        int16_t adc_val;
        float adc_val_float;

        adc_val_float = DMM_val * adc_gain / 3.3 * 4095;
        adc_val = (int16_t) adc_val_float;
        return adc_val;
}

int main (void)
{
        sysclk_init();
        board_init();

    // disable watchdog
     WDT->WDT_MR = WDT_MR_WDDIS;

    // insert application code here, after the board has been initialized
     configure_console();
     adc_setup();
     dacc_setup();

    // output example information
    puts("Hello World!\r");
    printf("Clock: %u", sysclk_get_cpu_hz());
    counter = 0;
    adc_start(ADC);
    char input;
    int delta_read;
    uint8_t done;

    while (1)
    {
            done = 0;
            input = getchar();
            switch(input)
            {
                    // test serial connection
                    case 'a':
                    printf("%c", input);
                    ioport_toggle_pin_level(LED_0_PIN);50 | Page
                    break;

                    //Print out the 4 ADC values and 2 DAC values
                    case 'p':
                    printf("ADC Values: %u %u %u %u DAC Values: %u %u\n\r", v_in, v_dn, v_dp, v_sense, n_FET_gate, p_FET_gate);
                    break;
```

```c
//Increase n_FET_gate by 1 (DAC value)
case 'w':
n_FET_gate = n_FET_gate < 4095 ? n_FET_gate+1 : 4095;
break;

//Increase n_FET_gate by 10 (DAC value)
case 'W':
n_FET_gate = n_FET_gate <= 4085 ? n_FET_gate+10 : 4095;
printf("%u\r\n", n_FET_gate);
break;

//Decrease n_FET_gate by 1 (DAC value)
case 's':
n_FET_gate = n_FET_gate > 0 ? n_FET_gate-1 : 0;
break;

//Decrease n_FET_gate by 10 (DAC value)
case 'S':
n_FET_gate = n_FET_gate >= 10 ? n_FET_gate-10 : 0;
break;

//Increase p_FET_gate by 1 (DAC value)
case 'e':
p_FET_gate = p_FET_gate < 4095 ? p_FET_gate+1 : 4095;
break;

//Increase p_FET_gate by 10 (DAC value)
case 'E':
p_FET_gate = p_FET_gate <= 4085 ? p_FET_gate+10 : 4095;
break;

//Decrease p_FET_gate by 1 (DAC value)
case 'd':
p_FET_gate = p_FET_gate > 0 ? p_FET_gate-1 : 0;
break;

//Decrease p_FET_gate by 10 (DAC value)
case 'D':
p_FET_gate = p_FET_gate >= 10 ? p_FET_gate-10 : 0;
break;

//p FET gate test
case '1':
n_FET_gate = 0;
p_FET_gate = 0;

while(!done)
{
        if (v_sense > p_FET_gate)
        {
```

```c
            delta_read = v_sense - p_FET_gate;

            if (delta_read > 2048)
                    p_FET_gate += 1024;

            else if (delta_read > 1024)
                    p_FET_gate += 512;

            else if (delta_read > 512)
                    p_FET_gate += 256;

            else if (delta_read > 256)
                    p_FET_gate += 128;
            else if (delta_read > 128)
                    p_FET_gate += 64;

            else if (delta_read > 64)
                    p_FET_gate += 32;

            else if (delta_read > 32)
                    p_FET_gate += 16;

            else if (delta_read > 16)
                    p_FET_gate += 8;

            else if (delta_read > 8)
                    p_FET_gate += 2;

            else
                    p_FET_gate++;

            if (p_FET_gate > 4095)
                    p_FET_gate = 4095;
    }

    else if (v_sense == p_FET_gate)
    {
            // We've reached the Vout_6105 voltage representing the goal
            // output current
            printf("Goal Reached\r\n");
             done = 1;
    }

    else if (v_sense < p_FET_gate)
    {
            delta_read = p_FET_gate - v_sense;
            if (delta_read > 2048)
                    p_FET_gate -= 1024;

            else if (delta_read > 1024)
                    p_FET_gate -= 512;
```

```c
                else if (delta_read > 512)
                        p_FET_gate -= 256;

                else if (delta_read > 128)
                        p_FET_gate -= 64;

                else if (delta_read > 64)
                        p_FET_gate -= 32;

                else if (delta_read > 32)
                        p_FET_gate -= 16;

                else if (delta_read > 16)
                        p_FET_gate -= 8;

                else if (delta_read > 8)
                        p_FET_gate -= 2;

                else
                        p_FET_gate--;

                if (p_FET_gate > 4095)
                        p_FET_gate = 0;

                v_in_dac_delta = (v_in_dac1 - v_in_20V_dac);

                if (v_in_dac_delta < 4095)
                {
                        // (v in dac delta > 4095) means negative delta and
                        // implies v in dac1 < v in 20V dac
                        if (p_FET_gate < v_in_dac_delta)
                                p_FET_gate = v_in_dac_delta;
                }
        }

        // Adjust p FET gate value
        ioport_toggle_pin_level(LED_0_PIN);
        ioport_toggle_pin_level(EXT1_PIN_5);

        // Adjust DAC0, if necessary to adjust n FET gate
        // If the floating point arithmetic proves too slow, use integer
        // arithmetic or a LUT (look up table)
        if (v_sense > v_sense_i_max)
                n_FET_gate = n_FET_gate_max;

        else if (v_sense > v_sense_goal)
        {
                //n FET gate = (uint16 t) ((float) n FET gate max.0 * ((float)
                (adc_pin_a0_reading - v_sense_goal))/((float) (v_sense_i_max - v_sense_goal)));
                n_FET_gate = (uint16_t) ((uint32_t) (n_FET_gate_max * ((uint32_t) ((v_sense -
v_sense_goal))))/(v_sense_i_max - v_sense_goal));
        }
```

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```c
                        else if (v_sense > (v_sense_i_min))
                                n_FET_gate = 0;

                        else
                        {
                                // ADCA0 reads between 0 V (200) and v_sense_i_min (+200), since we calculated
                                // v sense i min ignoring the 0V offset
                                //n FET gate = (uint16_t) ((float) n_FET_gate_max.0 * ((float) (v_sense_i_min + 200 -
adc_pin_a0_reading))/((float) v_sense_i_min));
                                n_FET_gate = (uint16_t) ((uint32_t) (n_FET_gate_max * ((uint32_t)((v_sense_i_min -
v_sense))))/(v_sense_i_min));

                                // The 200 offset accounts for the ADC reaching 200 (approximately), when its input = 0V.
                        }
                }
                break;

                //n FET gate test
                case '2':
                n_FET_gate = v_in;

                while(!done)
                {
                        if(v_in == seek_v)
                        {
                                done = 1;
                                printf("Done Seeking\r\n");
                        }

                        else
                        {
                                if(v_in < seek_v)
                                        n_FET_gate = n_FET_gate < 4095 ? n_FET_gate+1 : 4095;

                                else
                                        n_FET_gate = n_FET_gate > 0 ? n_FET_gate-1 : 0;
                        }
                }
                break;

                default:
                ioport_set_pin_level(LED_0_PIN, !LED_0_ACTIVE);
        }

    // is button pressed?
    /*if (ioport_get_pin_level(BUTTON_0_PIN) == BUTTON_0_ACTIVE)
    {
        // Yes, so turn LED on.
        ioport_set_pin_level(LED_0_PIN, LED_0_ACTIVE);
    }
```

```c
        else
        {
            // No, so turn LED off.
            ioport_set_pin_level(LED_0_PIN, !LED_0_ACTIVE);
        }*/
    }
}
```