Phase Locked Loop Integrated Circuit

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2015

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Abstract

This project focuses on the design and simulation of a phase locked loop (PLL) integrated

circuit. A PLL is an advanced topic and requires knowledge of control systems, analog and

digital design, as well as communication basics to fully understand. A PLL often consists of a

phase detector, low-pass filter, and a voltage-controlled oscillator (VCO). This project delves

into each individual block of the full circuit and gives careful consideration to each, exploring

the different design techniques used to complete a PLL design. Although this particular circuit

could be used for a number of different applications, this project focuses on the design of a PLL

for simple clock generation.

Acknowledgements

We would like to thank Professor Tina Smilkstein for signing on as our project advisor, as well as the entire California Polytechnic State University Electrical Engineering Department. Their support and insight were crucial in the development of this project.

Introduction

Phase locked loops (PLLs) can be found in many different types of circuits nowadays. Their applications range from a variety of uses. From synchronization of clock signals, demodulation, clock recovery, jitter and noise reduction, and de-skewing, the list of different fields to which PLL operation can be applied is extensive. A PLL operates by comparing a certain operating frequency with the circuit clock frequency and subsequently adjusting its output to match the input. It is analogous to a car's cruise control system [2]. As the car exceeds the speed specified by the user, the system slows it down. If the car's speed drops below the specified level, the car speeds up. To fully understand how this operation occurs, the basic structure of a PLL must be described and examined.
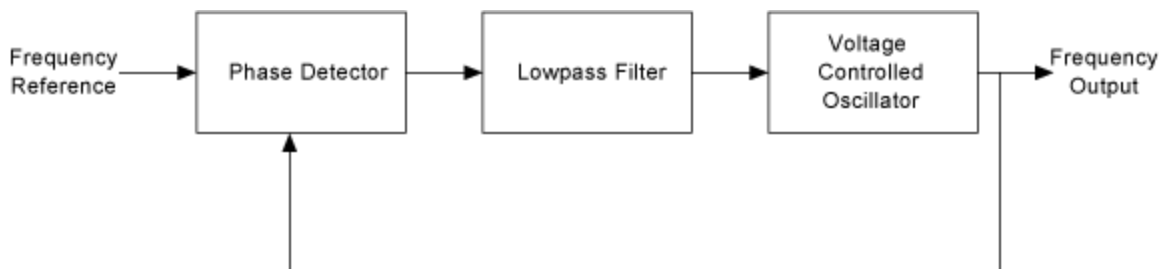
Figure 1: Basic PLL Circuit Structure

There are generally three components that can be found in any type of PLL regardless of its application. These parts include a phase detector, a low pass filter, and finally a voltage controlled oscillator (VCO) as depicted in *Figure 1*. Each of these components has a different and unique function required for the PLL to operate correctly. First and foremost, the phase detector plays a crucial role in the system operation and can be categorized into two areas: a

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phase only detector, or a frequency and phase detector (phase frequency detector or PFD). A

phase only detector is just that, it is only able to detect the phase difference between two

different signals of the same frequency. A frequency and phase detector however, is able to

compare the frequency of two different incoming signals (one from the input and one from the

feedback of the system) and detects the phase difference between the two [1]. This phase and

frequency difference is then translated into an "error" voltage which is passed on to the next

stage. Due to the specific application of the PLL being explored in this document, the latter of

these two types of detectors (phase frequency detector) will be focused on. As far as

implementation and design of the phase detector is concerned, there are many avenues of

approach. This will be discussed in the later design specifics portion of this document.

Because a PFD is being used, a charge pump (not shown in *Figure 1*) must be implemented as

well. A charge pump simply inputs the output from the PFD, and depending on that output,

"pumps" current in or out of the circuit block after it (in this case, the low pass filter). This will

be done by either completing the circuit connection to the rail or ground, sourcing current, or

dissipating it. This variation in current that the low pass filter sees changes the voltage at the

output of the filter and plays a crucial role in determining the control voltage for the VCO. Refer

to the charge pump design details in the design section of this report for a more detailed analysis

of how this operates.

After the charge pump is the loop low-pass filter. As the name suggests, it filters out undesirable

signals and noise coming from the phase detector. The loop filter is a very important block of

the PLL. This is due to a number of reasons, but most importantly, the loop filter is responsible in a large part for many of the characteristics of the PLL. More specifically, it is what determines the stability of the system, how quickly the PLL responds to frequency changes, and how effectively it removes signals with unwanted frequencies from entering the VCO. For example, if the PLL wants to change frequencies quickly, the cutoff frequency at which signals aren't able to pass through any more cannot be too low. This is because a low cut-off frequency corresponds to slower circuit operation. At higher cutoff frequencies, the circuit may operate faster, yet unwanted frequencies may pass through the pass-band. In addition, care must be taken to ensure the filter is stable, as the contrary could prove detrimental to the circuit operation. An unstable system will produce unwanted oscillations that will disrupt an efficient and accurate reading of the signal driving the VCO [1]. These are just a taste of the considerations which will need to be taken into account while designing an effective filter.

Lastly, the VCO is what produces the second signal which will be compared to the input signal. As the name suggests, it is controlled by the voltage signal stemming from the phase detector after it has been passed through the filter. The VCO design can vary greatly depending on the need for the circuit. Whether designing a low noise, low power, or just a basic oscillator, the specifications can vary greatly. For this project, a basic ring VCO with a slight emphasis on noise reduction will be developed.

With the fundamentals of PLLs covered and a solid understanding of what problems they are able to address, the goals and process of this specific project can be explained in detail. The

ultimate goal of this project is to design and simulate a PLL IC in order to gain a better understanding of how the circuit operates and what details need to be taken into consideration during design. This project focuses on a general design to illustrate PLL operation instead of focusing on a highly specific and specialized application. The details regarding the specifications of this PLL will be covered in the requirements sections of this document. Ideally, this project would be taken to the tape-out stage, and the PLL IC would actually be fabricated. Upon examining the tape-out scheduling with regards to the design process being used however, it was determined that this is not a realistic goal. Due to this limitation, the end goal will be to use the Cadence Virtuoso Layout Suite to design the circuit and test it through multiple simulations. What this will result in, is a layout which could be sent to fabrication companies for eventual tape-out.

Technical Aspects of PLLs

With a general background of PLLs given above, a more in depth description can be given, explaining the different technical factors to take into consideration while designing a PLL system. This section will delve into some specifics and characteristics of the different parts of a PLL which are crucial to fully understand the design process.

First and foremost, two common PLL characteristics are its type and order. A PLL's type is given in reference to how many integrators are present in the system, whereas a PLL's order refers to the number of poles that the system has. In a PLL, a VCO is considered an integrator as it provides a voltage to phase relationship. Because the VCO is an integral part of the PLL, all PLLs are at a minimum type 1. Type II PLLs have another integrator in the loop filter transfer function [3]. Type IIs are much more common in industry for a number of reasons.

Although Type 1 PLLs have a few advantage over Type II PLLs, such as lower settling times (the time it takes for the PLL system to stably change from one frequency to the new frequency) [4], Type II PLLs are generally preferred. Although lower settling time means faster system operation, Type II PLLs have an advantage in that the way the DC signal level shifts isn't directly dependant on the input to the gain block. By using an integrator in the loop filter, the output can be arbitrarily set to a DC level that isn't limited by the input to the filter [3]. Refer to *Figure 2* below for an illustration of this point.
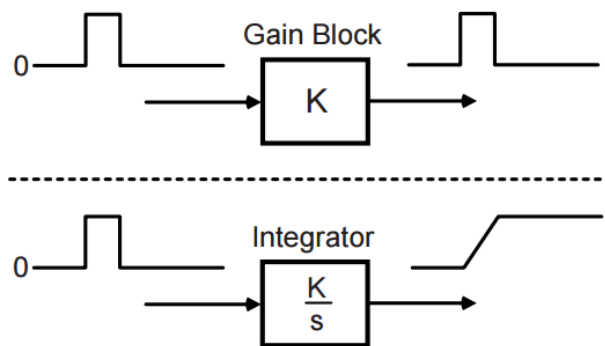
Figure 2: Gain Block vs. Integrator Block [3]

As can be seen above, the output of the Gain Block is constrained to a certain DC level that in many cases may not have enough range to encompass that of the VCO input. To fix this issue, other amplifying circuits might have to be implemented which would result in more transistors and a higher circuit cost. Essentially, a loop filter containing an integrator (A type II PLL) provides better control of the loop.

Another important concept to understand is the frequency range and bandwidth of the PLL loop. The frequency range is simply that: the range of frequencies over which the PLL can reliably lock and hold its state at. The loop bandwidth is related to the natural frequency of the loop and is the frequency at which the PLL will start to lose lock when the reference changes. This PLL characteristic is largely determined by the low pass filter specifications and values.

In order to better understand the effect that the low pass filter has on the PLL system as a whole, the transfer function characteristics of the PLL loop system will be explained. There are a number of acronyms and symbols used which are listed in *Table 1* below.

ζ	Damping Factor of System
ω_n	Natural Frequency
ω_z	Stabilizing Zero Frequency
K_{VCO}	VCO Gain in Hz/V
I_{CP}	Charge Pump Current
N	Feedback Divisor (1 for this circuit)
C_1	Large Low Pass Filter Capacitor
R_{LPF}	Large Low Pass Filter Resistor

To understand how the loop filter affects the entire system transfer function as a whole, the general closed loop transfer function for a system must be derived. This can is represented below in *Equation 1*.

$$H(S) = \frac{G(S)}{1 + G(S)} \qquad [1]$$

In *Equation 1,* G(S) is the open loop transfer function and is given by *Equation 2* [2].

$$G(S) = \frac{K_{VCO}}{S} * \frac{I_{CP} * F(S)}{N} \qquad [2]$$

In *Equation 2* It's clear to see that the open loop gain is affected by F(S) which in turn affects the entire transfer function of the complete system. F(S), the low pass filter transfer function depends on what type of filter is chosen, and the values chosen for its components.

$$\omega_n = \sqrt{K_{VCO} * \frac{I_{CP}}{N * C_1}} \qquad [3]$$

$$\omega_z = \frac{1}{R_{LPF} * C_1} \qquad [4]$$

$$\zeta = \left(\frac{RC_1}{2}\right) * \sqrt{\frac{K_{VCO} I_{CP}}{N C_1}} \qquad [5]$$

Equations 3, 4, and 5, illustrate how the values chosen by the low pass filter really affect certain PLL characteristics. The values of the Capacitor and Resistor of the low pass filter determine the natural frequency, stabilizing zero frequency, and consequently the bandwidth of the loop. In addition, the damping factor is dependant on these component values [2]. The calculations for these components will be performed in the Low Pass Filter design section once the topology of the filter has been explained.

Requirements/Specifications

With many of the following terms depicted in *Table 2* described in the previous section, this

PLL's specifications are as follows:

Table 2: PLL Requirements and Specifications

Specifications	Value
Input Signal Type	LVCMOS
Type	II
Order	2nd
Output Signal Type	LVCMOS
Loop Bandwidth	< 100MHz
Output Frequency Range	50-230 MHz
Reference Voltage	1.8V
Number of Inputs	1
Number of Outputs	1
Settling Time	< 500ns
Damping Factor	$0.9 < \zeta < 1.1$
Charge Pump Current Drive	< 25μA
Input Clock Duty Cycle	50%

This PLL was designed with these specifications in mind, and throughout the design section, it

will be verified that the specifications were met.

Phase Frequency Detector

Design

A phase detector circuit is one that detects the phase difference between two input signals.

Originally an XOR gate was used as the phase detector block because of its simple and easy to

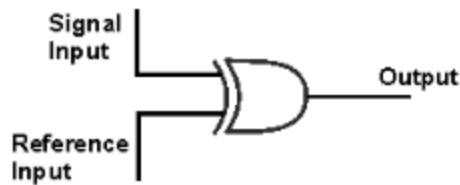implement design as shown below in *Figure 3*.

Figure 3: XOR gate [7]

It was able to produce a pulse on either the rising or falling edge of a signal which accurately

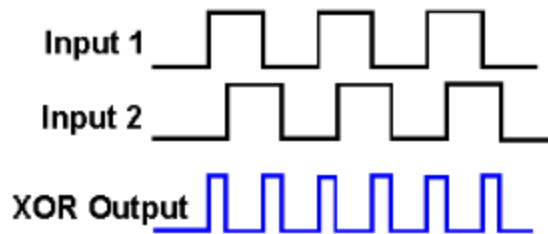depicts the difference in phase between the two signals as shown below in *Figure 4*.

Figure 4: XOR phase detector output [7]

However the main problem with the XOR gate was that it can only detect the phase difference

but not any difference in frequencies between the input signals. It was then decided that a

frequency phase detector would have to be used in this PLL design. A phase frequency detector

detects the difference in the phase and frequency between the two input signals.

Figure 5: PFD Highest Level Block Diagram

It outputs a signal from either the UP or DOWN output to the charge pump depending on which input signal is leading the other as shown above in *Figure 5*. The PFD is comprised of two D Flip Flops and an AND gate connected to the reset of each flip flop as shown in *Figure 6*.
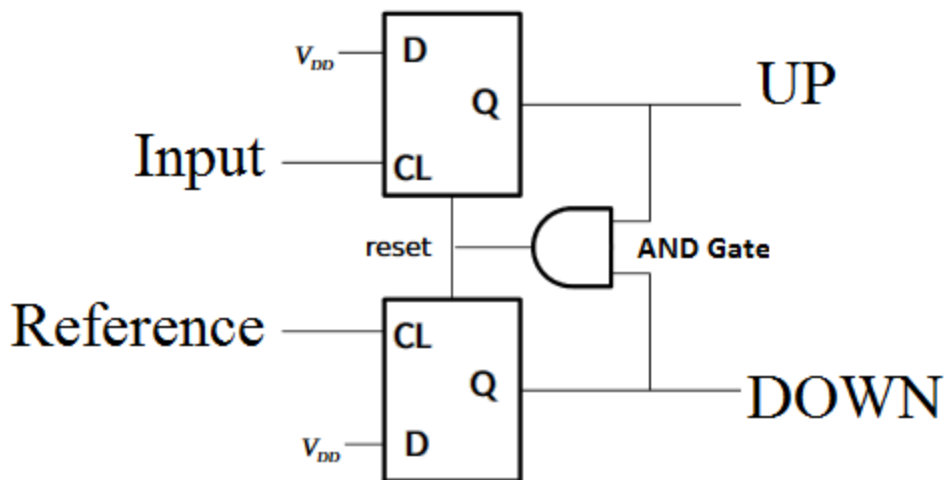

Figure 6: PFD Block Diagram [2]

For the D Flip Flops a design had to be chosen to make sure the PFD operated as predicted. With many different possible designs available for D Flip Flops a Master Slave topology was found to be the best for this implementation. It provided a circuit that wouldn't contain a possible floating node at which the value could be high or low.
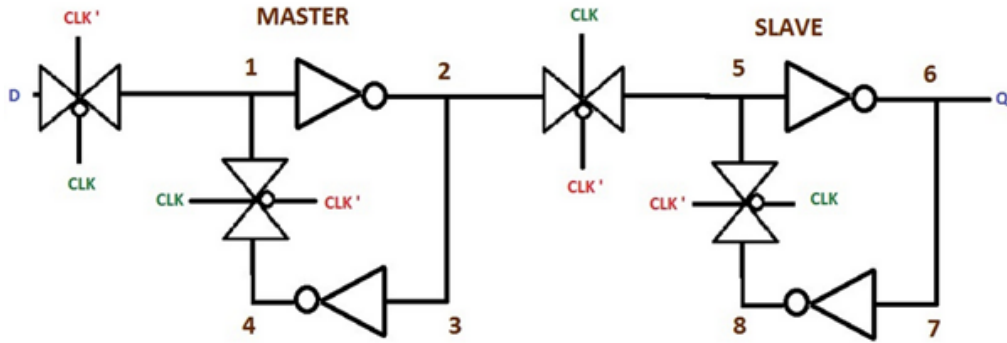
Figure 7: Master Slave D Flip Flop

The initial design of the flip flop shown in *Figure 7* didn't contain a reset function so one had to be added to achieve the desired response. The design shown in *Figure 8* was the finalized schematic that was chosen.
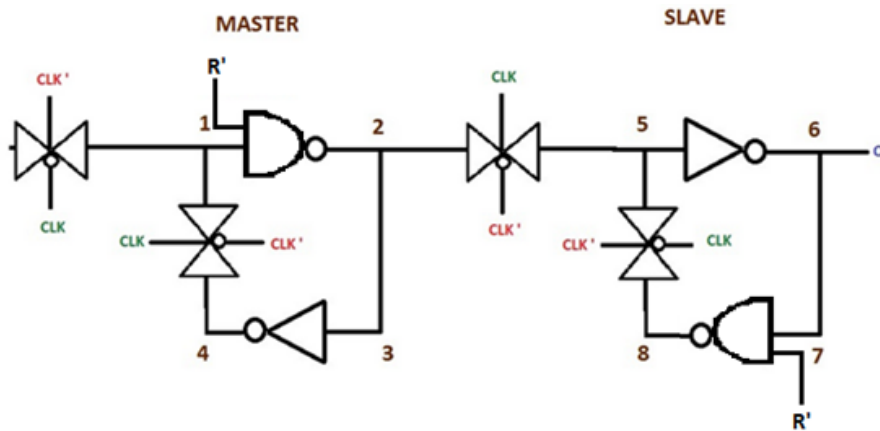

Figure 8: Final D Flip Flop Schematic

With the asynchronous reset implemented in *Figure 8* the expected response is that when the reset goes high the output goes low until the next clock rising edge at any time. Depending on whether the clock is high or low when the reset is triggered, the Master or Slave loop will output the expected value. If reset is triggered when clock is high the transmission gate between the Master and Slave will be on and the NAND gate in the Master loop determines the output. If the

reset is triggered when the clock is low the transmission gate between the Master and Slave will be off and the NAND gate in the Slave loop determines the output. If reset stays high for long enough for the clock signal to go from low to high or high to low the flip flop will still operate as intended because the Master and Slave loops can hold the last value used.
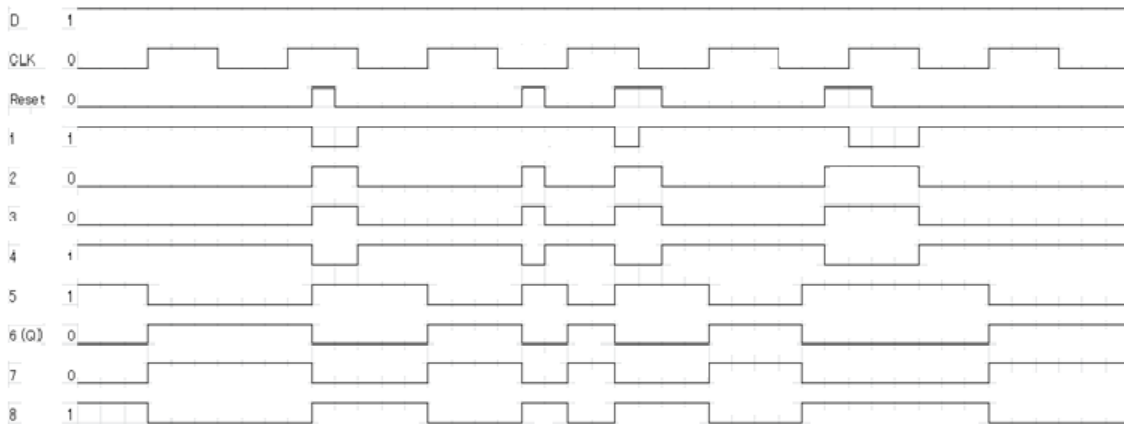

Figure 9: Sample input clock with sample reset trigger

After the D Flip Flops were designed the functionality of the PFD was tested. Looking at *Figure 9* UP and DOWN are triggered on the rising edge of each input signal and when both are logic high then the reset is triggered and both go low until the next rising edge. This will ideally cause UP and DOWN to never be both high at the same time. The UP and DOWN signals will then feed into the input of the charge pump.

Looking at the possible test cases for the PFD there are two main ones that can be analyzed. The first is where the Input is leading the Reference and the second being the Reference leading the Input.
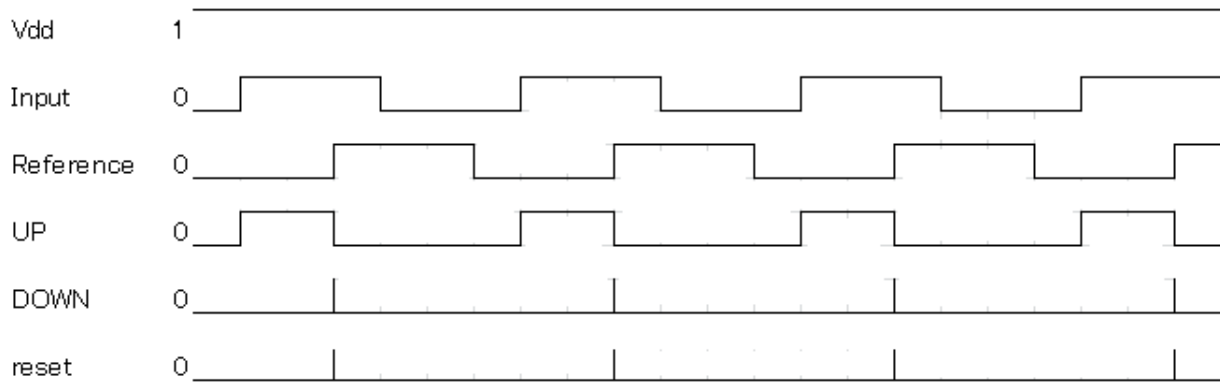
Figure 10: Input leading Reference

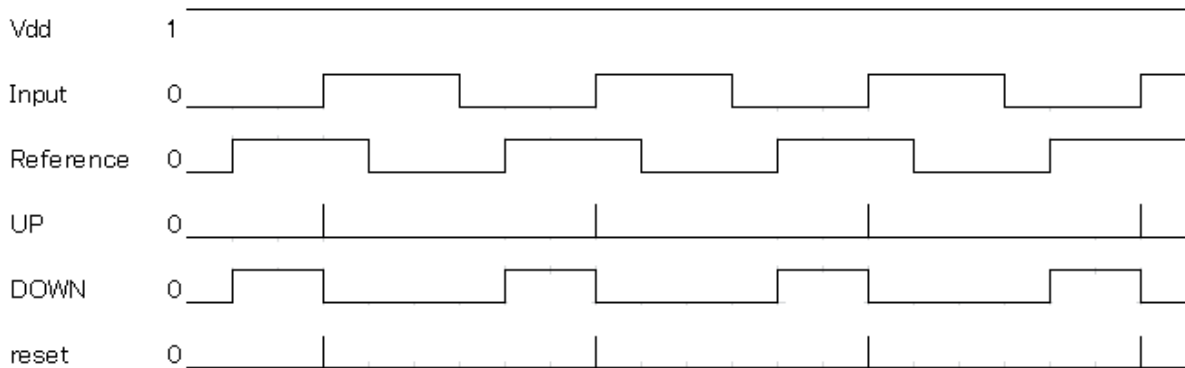*Figure 11: Reference Leading Input*

The difference in phase can be observed in the UP and DOWN outputs. In *Figure 10* where the Input is leading the Reference the UP output will cause for the system to speed up so that the Reference signal can catch up. In *Figure 11* where the Reference is leading the Input the DOWN output will cause for the system to slow down so that the Reference can match the Input.
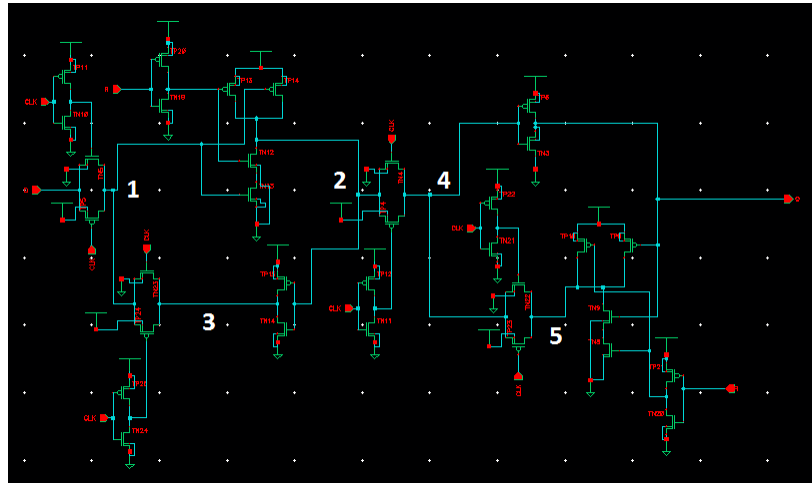
Figure 12: D Flip Flop at transistor level

When designing the D Flip Flop the W/L ratio of certain transistors had to be changed to make sure that it operated correctly. At node 4 in *Figure 12* above the inverter required a larger W/L, 1μm/180 nm, ratio because the transmission gate was pulling to much current to the ground causing for less voltage to be outputted. For the other transistors the minimum W/L, 220 nm/180 nm, was used to make it the flip flop operated as fast as possible.

Figure 13: D Flip Flop Simulation

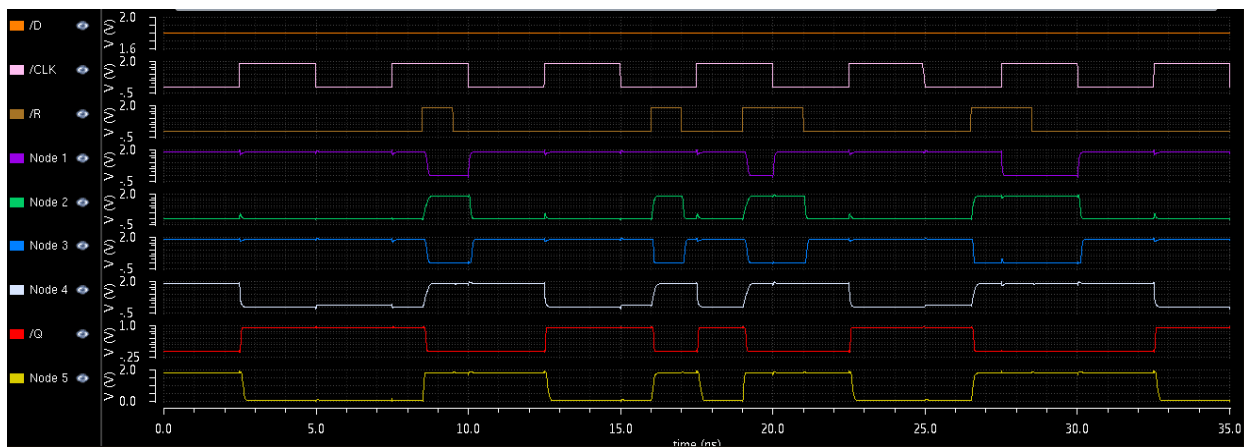The flip flop was tested by triggering the reset at four points, when the clock is high, when the clock is low, at the rising edge of the clock, and at the falling edge of the clock shown in *Figure 13*. With the reset triggered the output, Q, was looked at to make sure it was high at the rising edge of the clock and went low at any point when the reset is high and stayed low until the next rising edge. From the simulation it was observed that the D Flip Flop was operating correctly so it was then implemented into the PFD.
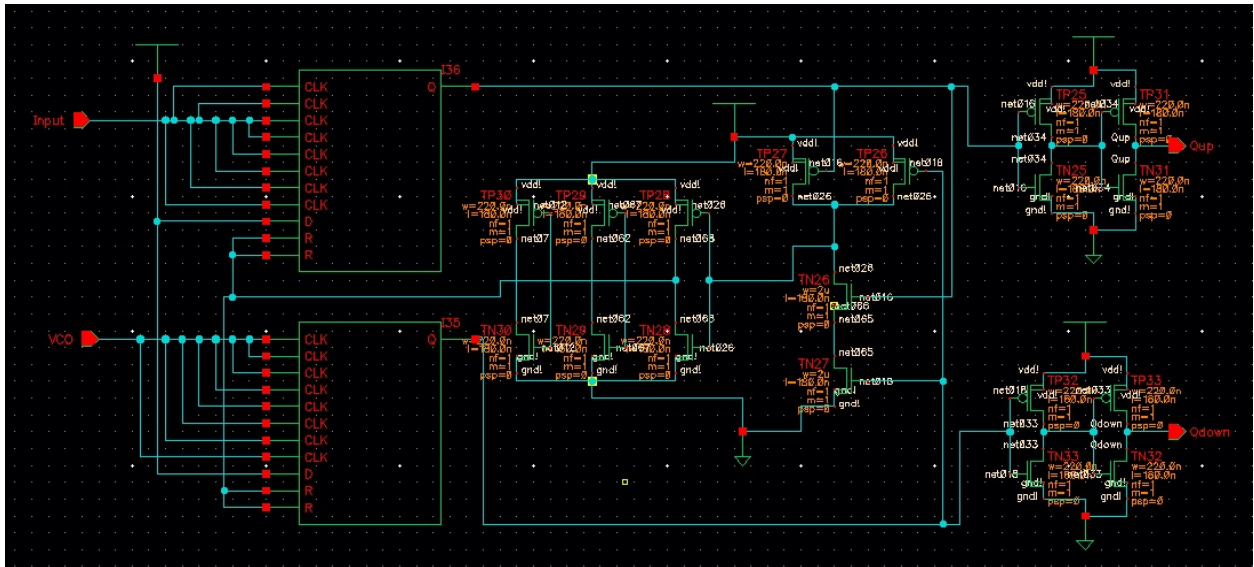
Figure 14: PFD Schematic

When designing the AND gate in *Figure 14* the W/L ratio of the NMOS transistors in the NAND gate had to be increased. The reset originally stayed logic high after it was triggered because the value of reset wasn't going low enough after the PFD was reset. So the widths of the NMOS transistors in the NAND gate were increased so that the reset would go all the way down to logic low. Also after testing the PFD it was observed that at the UP and DOWN output didn't give a

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clean signal so two inverters were added to make sure the signal goes all the way from rail to

rail.

Figure 15: PFD Simulation

In *Figure 15* the Input signal is leading the Reference, or VCO, signal so as expected the UP

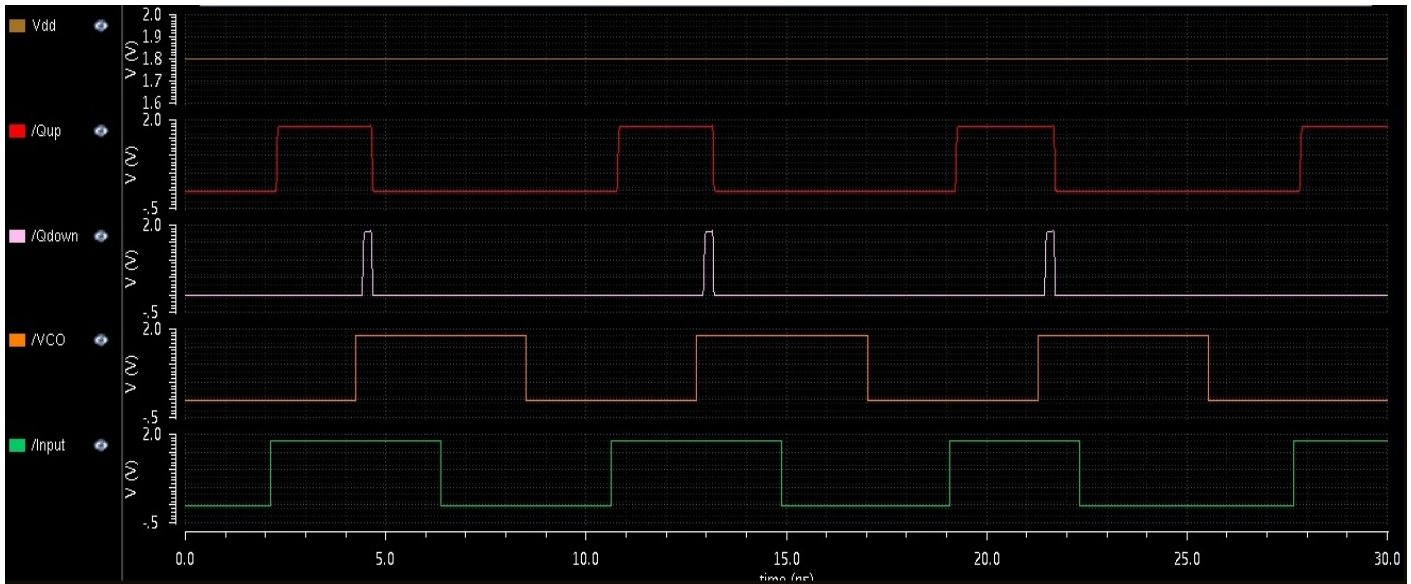output is triggered high until the rising edge of the Reference. When both the UP and DOWN

signals go high there is a delay of approximately 300ps until they both go back down to ground.

This 300ps delay is used to detect small changes in phase between the Input and Reference [2].

Charge Pump and Low Pass Filter

Design

A charge pump circuit takes in the UP and DOWN output pulses from the PFD and changes it to a single DC voltage. At the start of the design process a simple schematic was used for the Charge Pump to see if the basic operation of the block could be verified shown below in *Figure 16*.
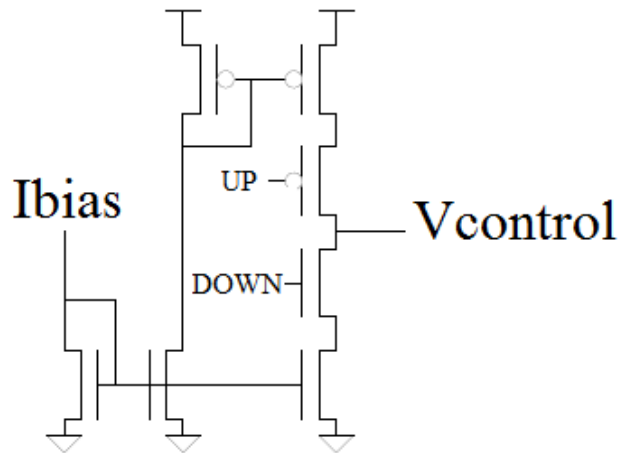
Figure 16: Original Charge Pump Schematic

In this design the two current controlled switches were created using current mirrors connected to a biasing current, the current through both the UP and DOWN signals have to be the same to prevent mismatching. Depending on the UP or DOWN input the Charge Pump would either pump current into the low pass filter or drain current out. When the Input is leading the Reference the UP signal will be triggered and current will flow into the low pass filter increasing Vcontrol. When the Reference is leading the Input the DOWN signal will be triggered and current will sink out of the low pass filter decreasing Vcontrol. This design however caused for

a very inconsistent control voltage to be outputted and in many cases didn't operate as intended.

A new design for the charge pump shown below in *Figure 17* was implemented to ideally get rid

of the inconsistencies at the output.
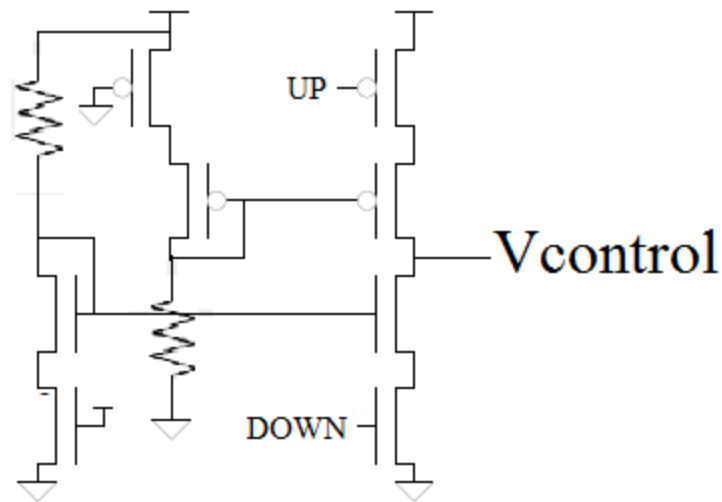
Figure 17: Finalized Charge Pump Schematic

This design accomplished that goal. With the UP and DOWN inputs being fed into transistors

located at the rails the output was much less susceptible to noise [2]. The values of the resistors

were also set to values that would cause the currents through UP and DOWN to be matched.

Also the W/L ratio for many of the transistors had to be greatly increased to lower the sensitivity

of the system.

Low Pass Filter

The low pass filter was implemented with the topology seen in *Figure* 18. It was determined that

a Type II 2nd order passive filter should be utilized due to its simple nature.
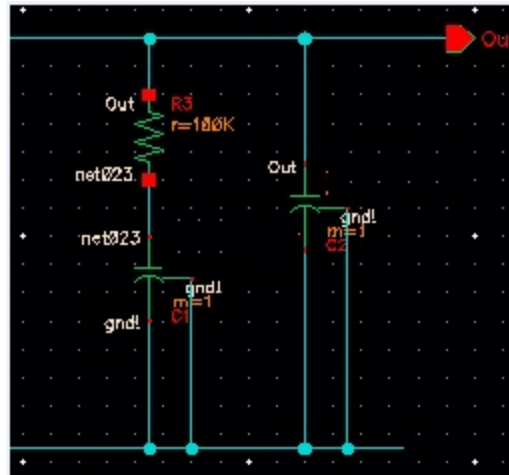
Figure 18: Low Pass Filter Schematic

The transfer function of this particular loop filter is given by *Equation 6* and further simplified

by *Equation 7*. For stability reasons, and to prevent introducing a new pole into the system, C2 is

chosen to be 10 times smaller than C1. Because it is significantly smaller than C1, the stability of

the loop isn't affected, and it can be ignored for calculation purposes.

$$F(S) = \frac{1}{s(C_1 + C_2)} * \frac{1 + sR_{LPF}C_2}{1 + sR_{LPF}C_{||}} \qquad [6]$$

$$F(S) = R_{LPF} + \frac{1}{C_1 s} \qquad [7]$$

By plugging in the loop filter transfer function into *Equations 1 and 2*, we obtain:

$$H(S) = \frac{\omega_n^2 * \left(1 + \frac{s}{\omega_z}\right)}{s^2 + 2s\zeta\omega_n + \omega_n^2} \qquad [8]$$

Equation 8 depicts the final general transfer function of this system. Utilizing the formulas introduced in *Equations 3 and 5*, sufficient values for the low pass filter were calculated. By selecting a 100 kilo-ohm resistor for R1, and a C1 value of 128fF, we were able to obtain a natural frequency of 177 Mrad/sec and a damping factor of 1.13, which is within the desired specified range. The loop bandwidth was calculated from the natural frequency to be 75.8 MHz, which falls under the specified loop bandwidth of 100 MHz.
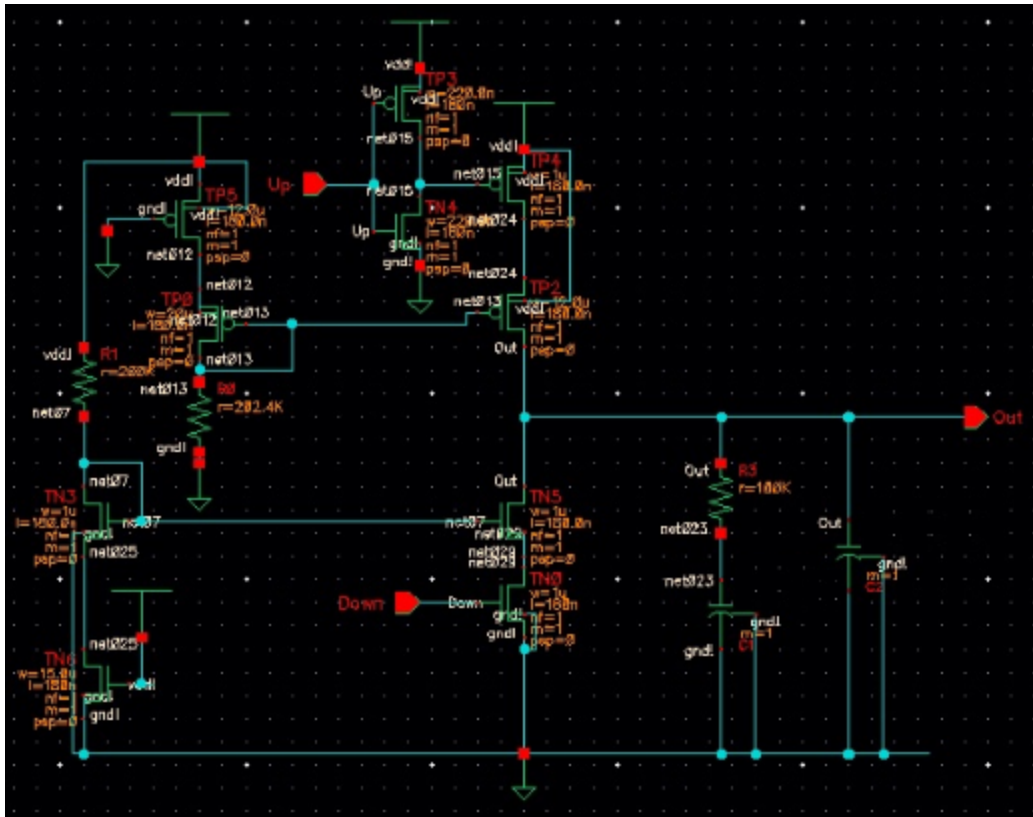
Figure 19: Charge Pump with Low Pass Filter Schematic

The sizing of transistors in the Charge Pump was much more difficult than in the other blocks.

The W/L ratio of the diode connected transistors in *Figure 19* had to be much larger than the

transistors connected to their bases to prevent channel width modulation as well as making sure

the current mirror was able to pass enough current to keep the transistors in their required area of

operation. The transistors at the rails also had a larger W/L ratio to help with the system's

sensitivity to noise [2].

Figure 20: Charge Pump and Low Pass Filter Simulation

As shown in *Figure 20* above the DOWN signal has a much high duty cycle than the UP signal

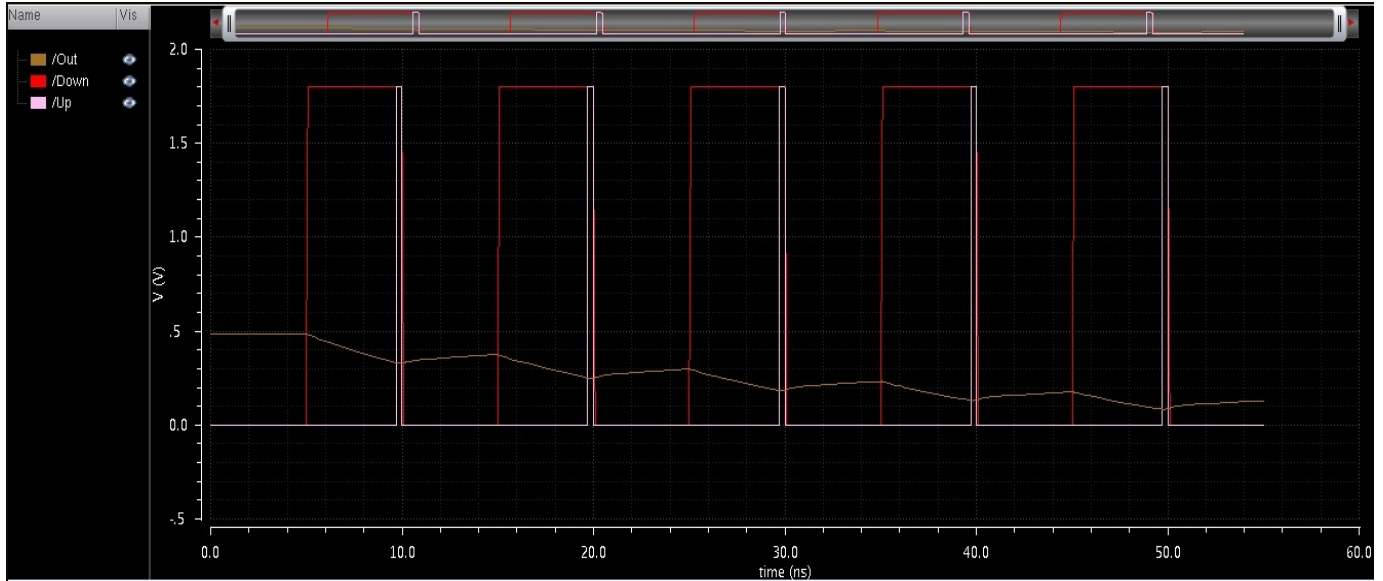so the Charge Pump is sinking current out of the low pass filter and Vcontrol is decreasing over

time. The current through the UP and DOWN inputs was set to 23µA and the capacitors in the

low pass filter were set to 128 fF so the change in voltage was .01797 V/nsec, $\frac{I}{C} = \frac{dV}{dt}$.

Once the Charge Pump's functionally was shown to be operating correctly sample Input signals

were then sent through the PFD to verify that the output of the Charge Pump, the control voltage,

would be able to lock to a DC voltage. Refer to *Figures 21, 22, 23, and 24,* for simulations of the

output of the low pass filter. In each case the settling nature of each signal is clearly visible. The

"blips" seen on the signals are caused by the UP and DOWN switching action of the PFD. This

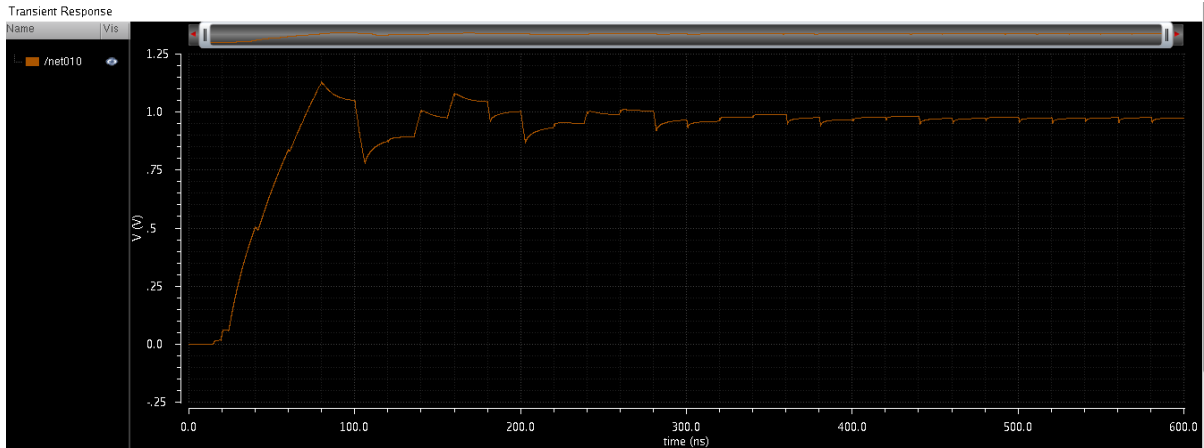occurs when they are both on at the same time.

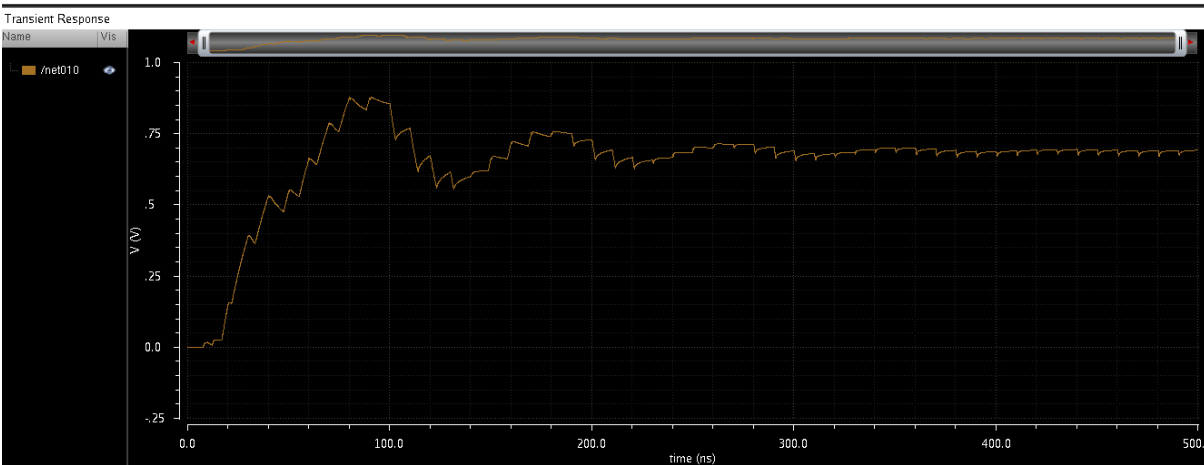*Figure 21: Input Signal of 50 MHz*

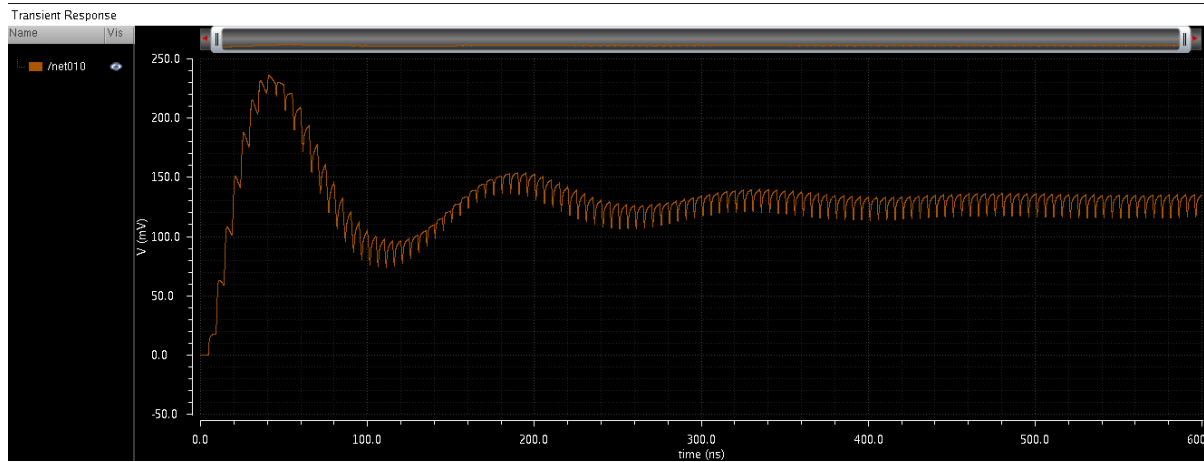*Figure 22: Input Signal of 100 MHz*
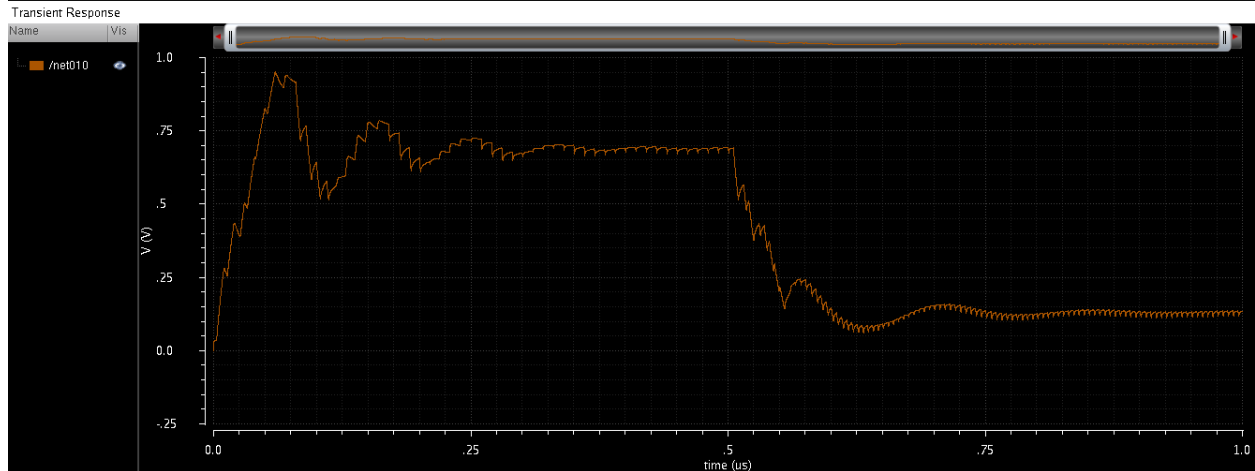

Figure 23: Input Signal of 200 MHz

Figure 24: Input Signal of 100 MHz changed to 200 MHz after 500 nsec

Using the Input signal shown above in *Figure 24*, the settling time was found to be

approximately 450 nsec which meets our specification of less than 500 nsec.

Voltage Controlled Oscillator

Design

As discussed before, the VCO is responsible for providing the frequency at which the Phase

Locked Loop operates at. The frequency is variable, depending on the level of the voltage being

sent to its control terminal. Depending on the design, the frequency will either increase or

decrease as the control voltage is raised. For the purposes of this VCO design and test stage, the

control voltage was simulated to determine the oscillator gain and KVCO characteristics, as well

as its operable linear range. This will be explained in more detail in later sections.

There were a number of different options for the design of the VCO, but ultimately a ring

oscillator was chosen. This type of VCO employs an odd number of inverters connected to each

other in a loop (See *Figure 25)*.
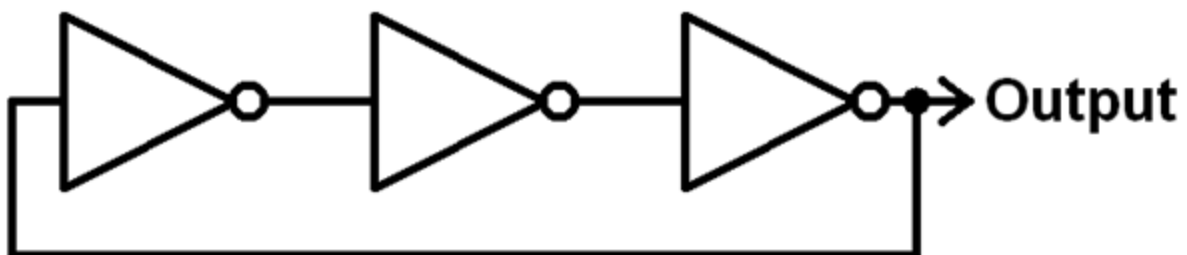
Figure 25: Simple Ring Oscillator Circuit Block Diagram

At every run through the system, each node oscillates between a 1 and 0 due to the inverting

action. This produces a waveform at a certain frequency at the output of the circuit. This

frequency is determined by $f = 1/2Nt_d$, where f is the frequency, N is the number of inverter stages, and t_d is the time delay characteristic of the inverter being used.

To implement a variable frequency "system" controlled by an external voltage, a current-starving NMOS was placed at the bottom node of each inverter as depicted in *Figure 26* below.
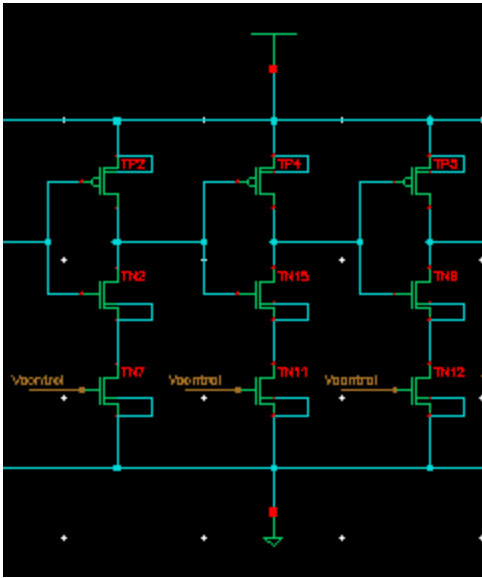
Figure 26: Current-Starving Topology Utilizing an NMOS

Figure 26 shows an inverter chain with the PMOS source tied to the rail and the NMOS source tied to ground, with their gates and drains connected to each other. The NMOS at the bottom of each inverter serves as the "current-starver". The control voltage is sent to the gate of this NMOS and can control the amount of current flowing through the chain. This, in turn, affects the frequency of the loop.

For the purposes of this PLL design, a low frequency specification was chosen. In this case, about 50 MHz to about 250 MHz with the least steep KVCO curve was desired. With this in mind, the first step in achieving these design goals was to do some transistor characterization to determine an optimal sizing ratio for the length and widths of the field effect transistor (FET) channels.

Within Cadence, a simple NMOS was laid out and the drain source current (I_{ds}) vs drain source voltage (V_{ds}) plots were obtained for a gate source voltage (V_{gs}) of about 0.7 volts. The channel length and widths were then varied to observe the effects that it might have on the I_{ds} vs V_{ds} plot. Refer to *Figures 27, 28, and 29* for an example.
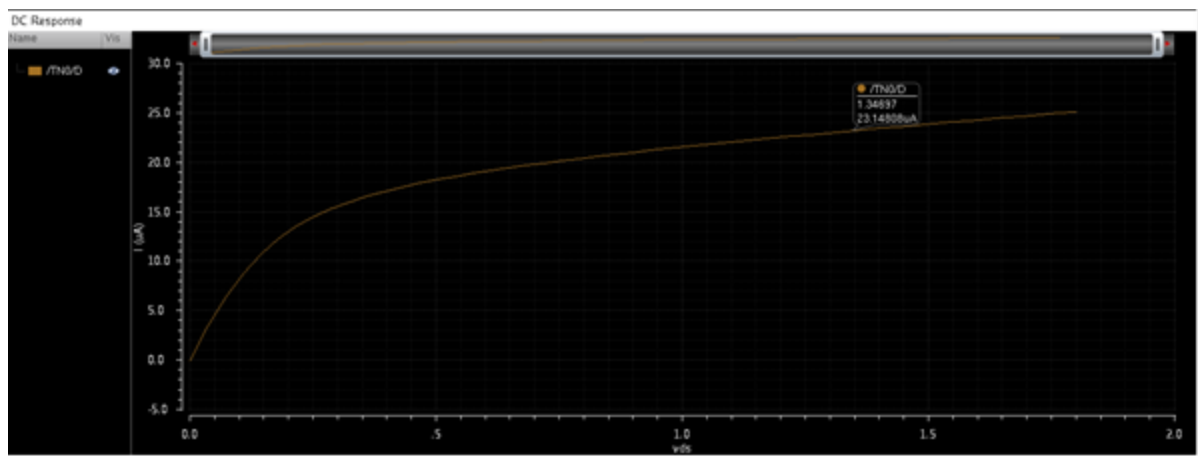
Figure 27: Transistor I_{ds} vs V_{ds} plot 220/180nm W/L ratio
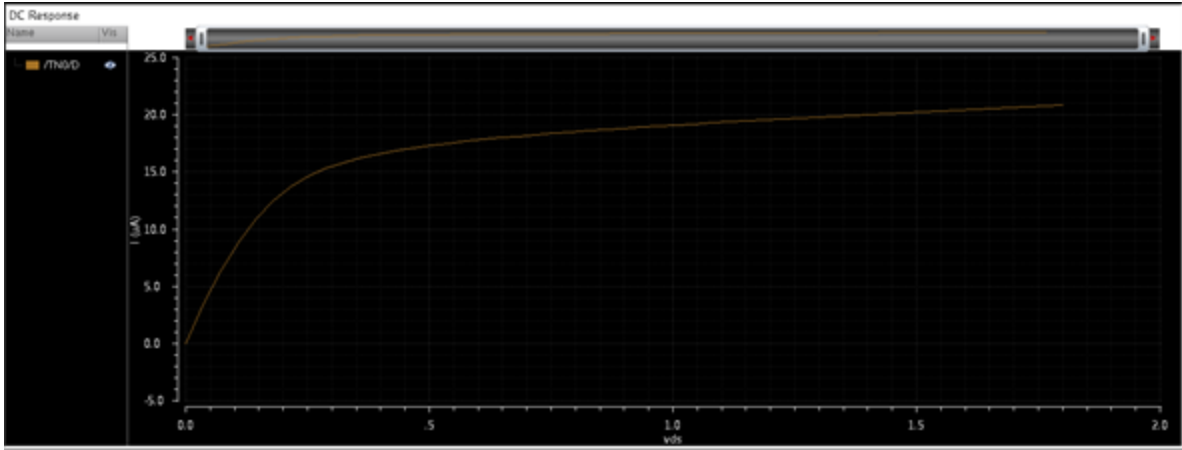
Figure 28: Transistor I_{ds} vs V_{ds} plot 330/270nm W/L ratio
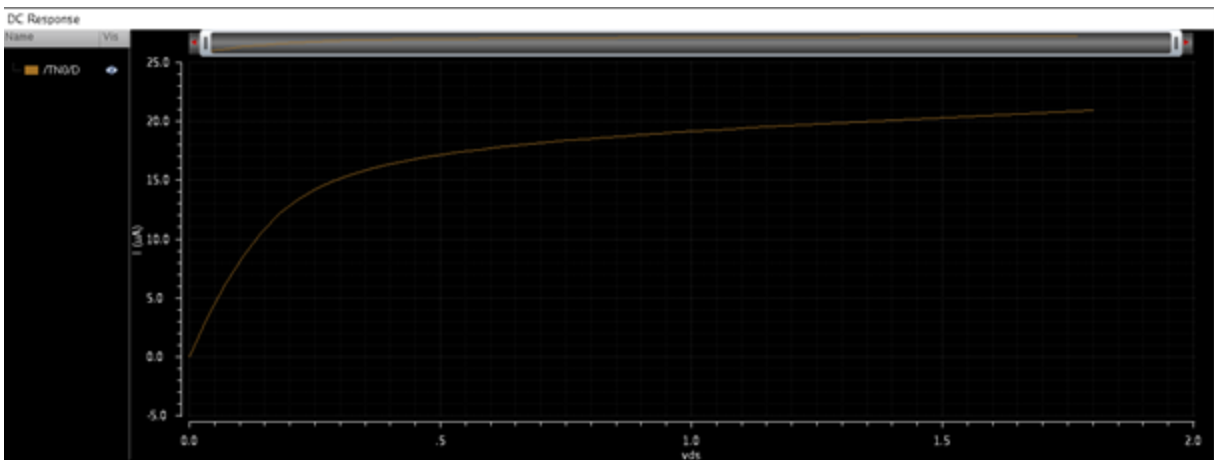
Figure 29: Transistor I_{ds} vs V_{ds} plot 440/360nm W/L ratio

As can be observed from the above figures, as the channel widths and lengths are increased, the more the curve flattens out towards the higher end of V_{ds}. The goal of this exercise was to obtain the transistor channel width and length values that would maximize our KVCO linear range. That being said, there is a stark difference between the curvature depicted in *Figures 27 and 29,* but it was found that at higher width and length sizes, the curvature difference is negligible. At

this point the determining factor for the transistor channel sizes would be the affect it has on the frequency of the system as a whole. Recall from earlier that the two main methods for changing the frequency of a ring oscillator involve changing the number of inverters in the loop, and/or changing the channel and width lengths of the transistors, modifying their capacitance, and thus affecting the time that it takes for the nodes to oscillate between 1 and 0. In this particular case, a W/L value of 660/540nm, in addition to a 9 inverter string, was used to obtain our desired frequency.

Simulation

With this design, the frequency increased as the control voltage was increased. In order to obtain the VCO gain, an excel graph was generated by plotting the frequency versus control voltage. The resulting plot can be seen in *Figure 30.*
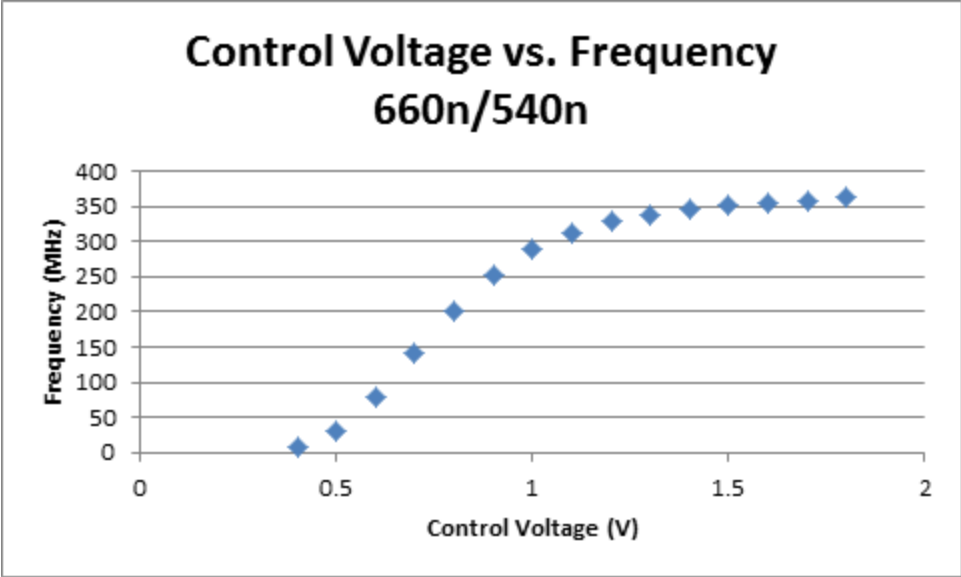
Figure 30: Control Voltage versus Frequency for the 660n/540n W/L Ratio

In *Figure 30,* the linear portion of the graph contains the usable frequencies at which the VCO will operate properly. It is the tuning range within which the VCO must operate. The KVCO could be determined by finding the slope of this linear portion. In this case, the tuning range was roughly between 25MHz to 285MHz, encompassing a control voltage range of about 0.5V to 1V (0.5V range). This is about a third of our full voltage range of 0-1.8V. We didn't want to limit our input voltage range to a fraction of our rail and so set about to modify the design in order to make the KVCO slope as shallow as possible.

The first modification came in the form of a current mirror control "system" that would be mirrored with all the current starving NMOS transistors below the inverter ring. The control voltage would be sent solely to the gate of an N channel device connected to the drain of the current mirror. Once the same analysis was performed on this circuit, the following excel plot was obtained.
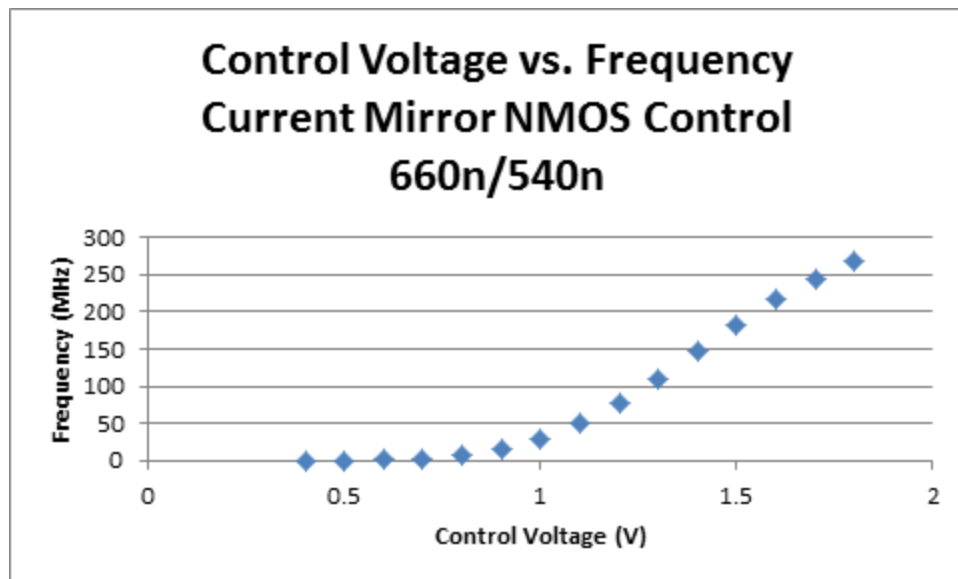
In *Figure 31,* it can be noticed that the KVCO of the circuit has become slightly shallower. The linear portion of this graph extends from about 1.1V to 1.7V. This is a very slight different from the previous 0.5V difference.

One more change was made to the design in order to decrease the steepness of the KVCO Characteristic. Simply put, the NMOS connected to the rail was replaced with a P Channel device (see *Figure 32*). With some modifications to the channel length and width ratio, this allows the control voltage to pull all the way down to 0 V and provided a much more linear KVCO characteristic (see *Figure 34)*. *Figure 33* depicts the difference that just changing the NMOS to a PMOS made, whereas *Figure 34* depicts the final plot once the W/L values had been changed to the desired specifications.
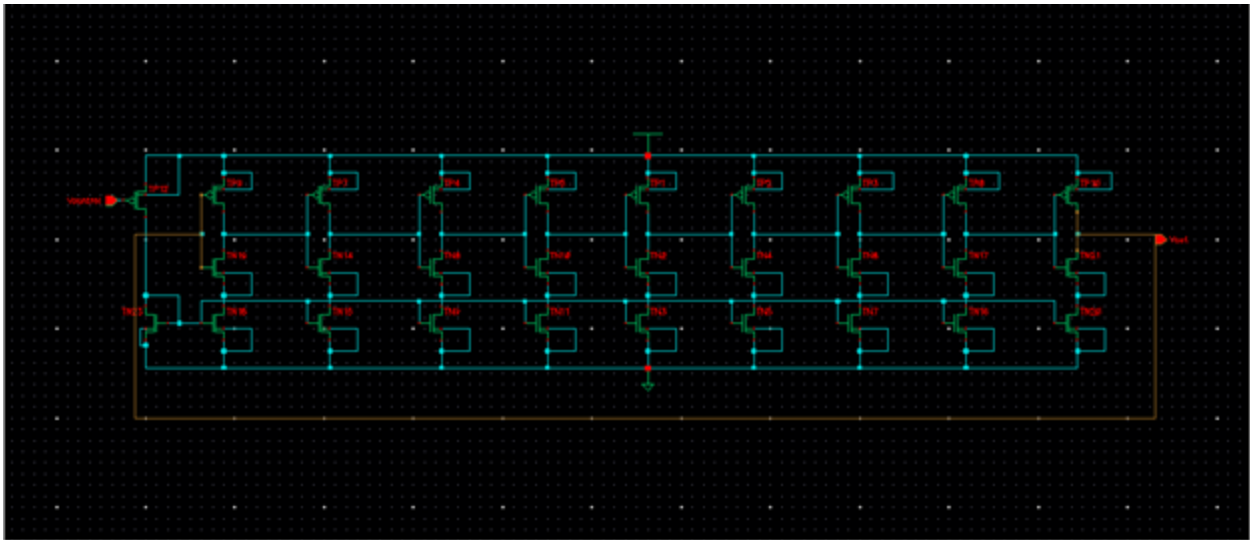
Figure 32: Nine Inverters in Series with PMOS Control for Current Mirror
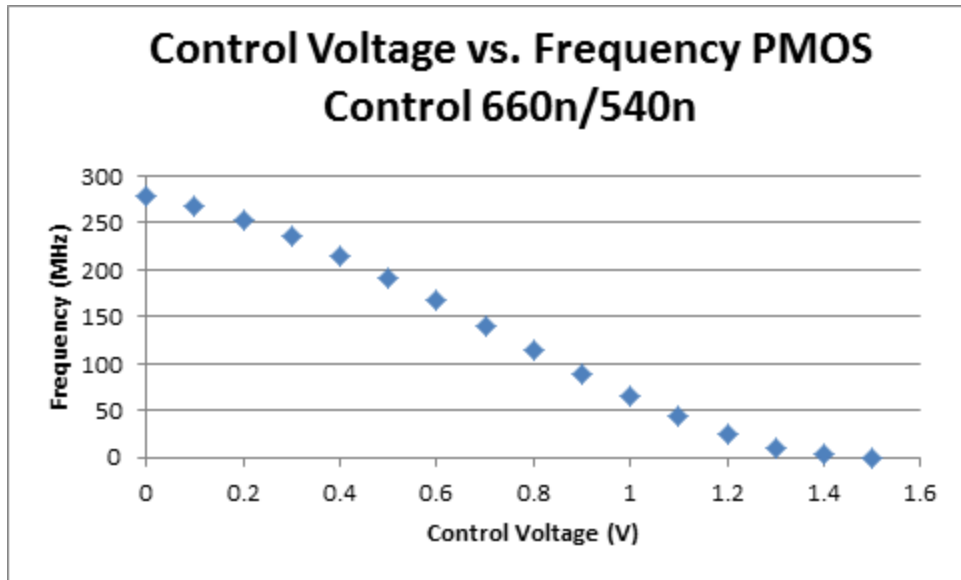
Figure 33: Control Voltage vs. Frequency when replacing NMOS control with PMOS 660n/540n
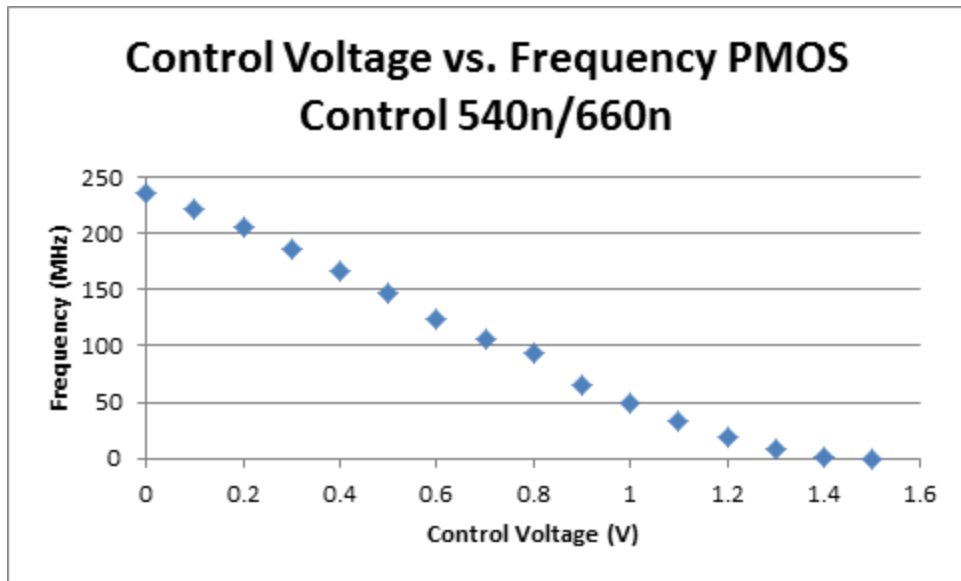
Figure 34: Control Voltage vs. Frequency when replacing NMOS control with PMOS 540n/660n

In *Figure 34* it can be noticed that almost the entire range of control voltage values is usable in this linear range. The voltage can be varied from 0V to 1.4V while still maintaining linearity. This results in a change of frequency from about 235MHz to 2MHz, well within the desired frequency range.

The only difference between this design and the one incorporating the NMOS is that the frequency now decreases instead of increasing as the control voltage is raised. This change in direction shouldn't matter and can be resolved easily by switching the input terminals to the phase frequency detector. The final product of this design is a VCO that changes frequency linearly from 2MHz to 235MHz over the range of 0 to 1.4 volts. Refer to *Figure 35* for an illustration of this.
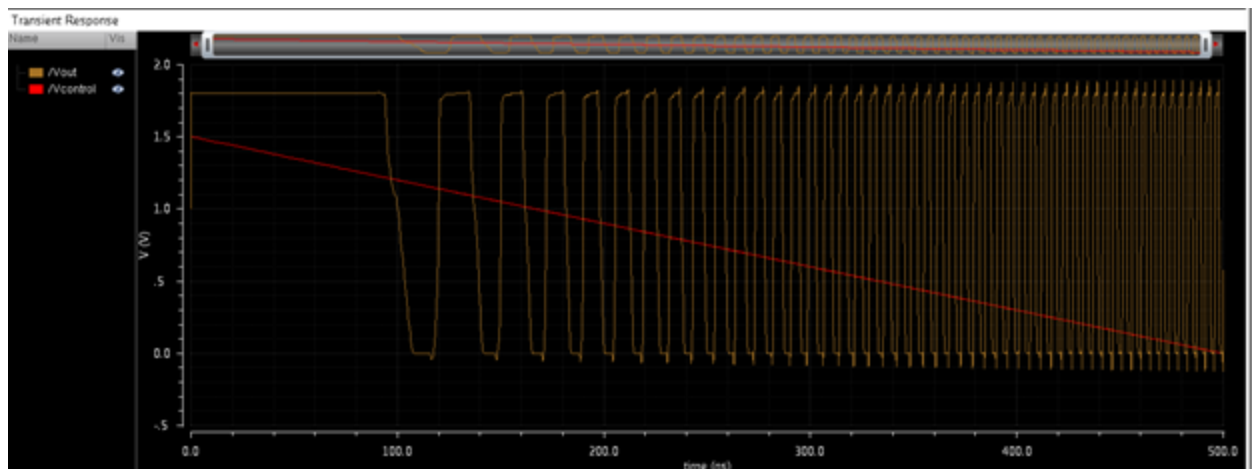
Figure 35: Frequency Changing as Control Voltage Changes

The 1V spike seen at the rails at high frequencies is due to the capacitances charging up to above and below rails. A small capacitor could be placed between the power and ground rails to negate this effect, but it was determined unnecessary for the purposes of this design as capacitors take a large amount of space on the chip layout.

The final step for the VCO implementation is to calculate the KVCO value which is as simple as obtaining the slope from the control voltage versus frequency plot depicted in *Figure 34*. The linear range extends from 0V to about 1.3V. With that in mind, the negative slope is calculated to be 174.7 MHz/V.

$$KVCO = \frac{235.5MHz - 8.33MHz}{1.3V - 0V} = 174.7MHz/V$$

Final Implementation

After each the design and verification of each block was completed the whole PLL was connected together so the functionality could be tested.
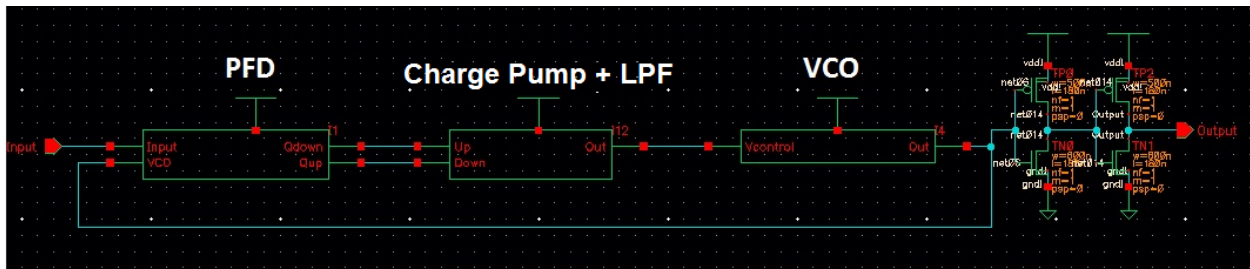
Figure 36: PLL Block Diagram

When connecting all of the blocks together, shown above in *Figure 36*, the PFD's UP and DOWN outputs were tied to the Charge Pump's DOWN and UP inputs respectively. This was because of the choice to use a PMOS driven VCO. Since the VCO is driven using a PMOS instead of a NMOS as the control voltage decreases the frequency increases. Becauses of this for the Reference signal outputted from the VCO to speed up, the control voltage would have to be lowered. For this to happen the DOWN signal at the input of the Charge Pump would have to have a larger duty cycle than the UP input. So assuming that the Input signal is at a higher frequency than the Reference signal the PFD will output a higher duty cycle signal from the UP output which is then fed into the DOWN input of the Charge Pump increasing the frequency of the Reference signal. The two inverters connected to the output of the PLL were added to make the rising and falling edges more precise. In the figures below the blue VCO signal represents the output of the VCO and the green Output signal represents the same signal after having passed through both inverters.

For testing the PLL the frequency range chosen to test was bound by the VCO's region of operation. It was found that the VCO could operate from 50-235 MHz so those frequencies were used at the boundaries of the operation of the PLL.
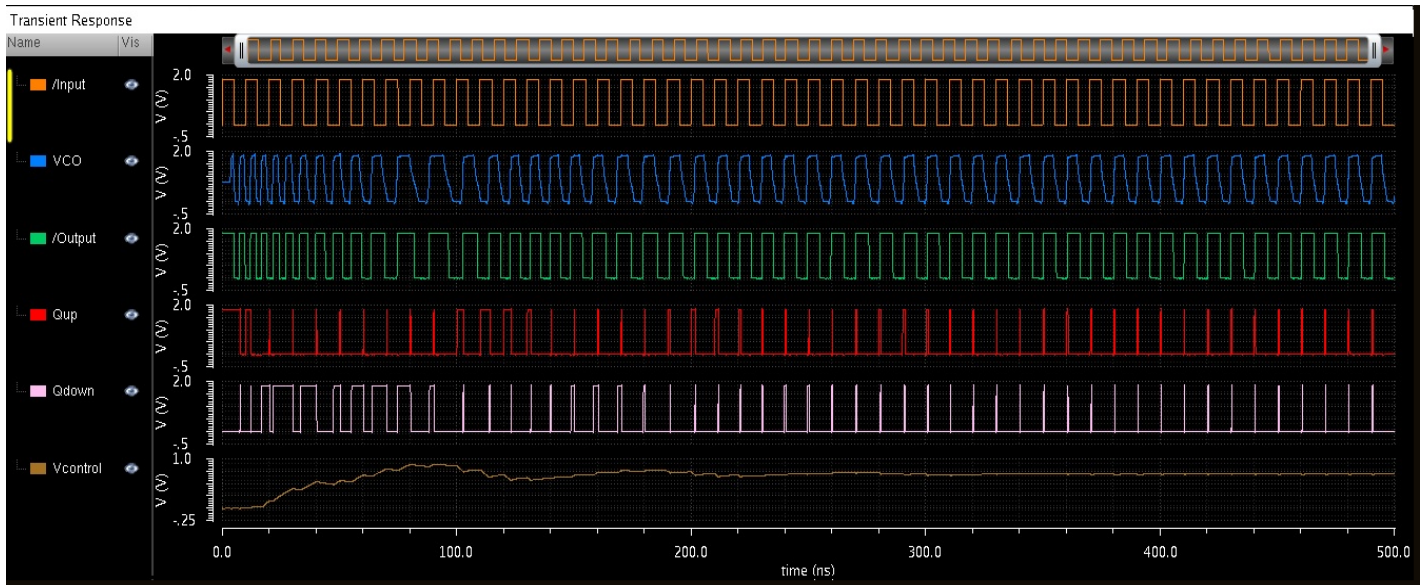
Figure 37: Input Signal of 100 MHz

The first test was a 100 MHz signal that was used as a sort of midpoint to make sure the PLL was operating correctly before we tried frequencies closer to the boundaries. From *Figure 37* it can be observed that after approximately 200 nsec the PLL output is able to latch onto the input signal.
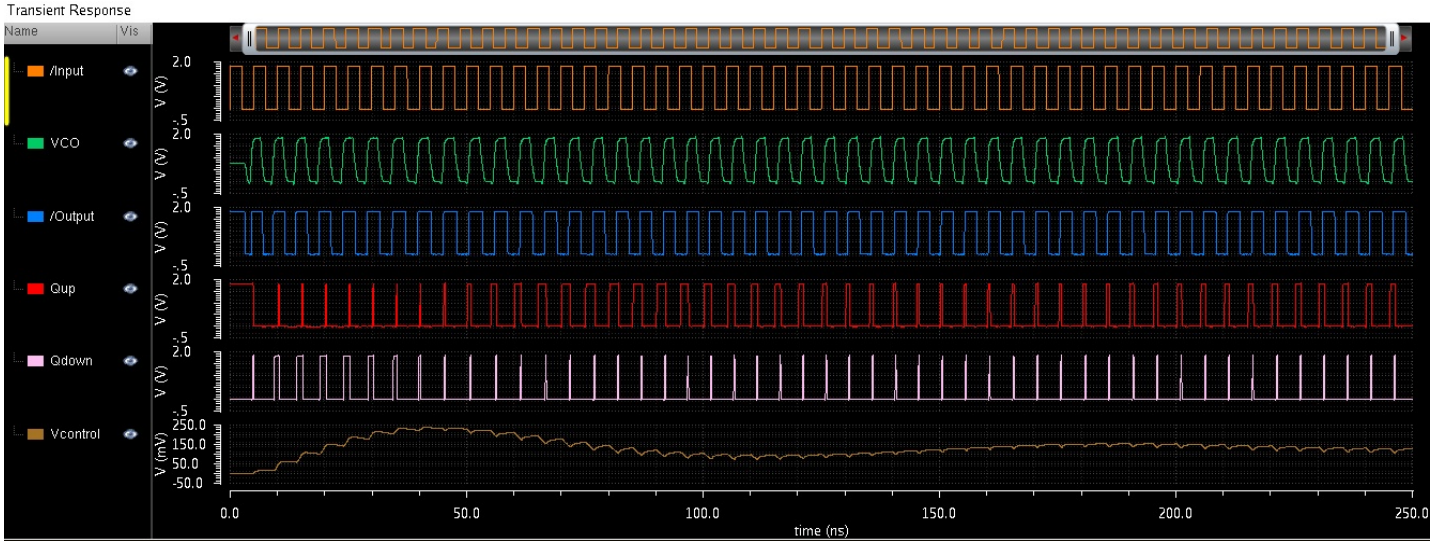
Figure 38: Input Signal of 200 MHz

Similar to the 100 MHz case the settling time is also about 200 nsec but at 200 MHz the output

signal doesn't go to a fully stable state as there is still some ripple observed shown above in

Figure 38.
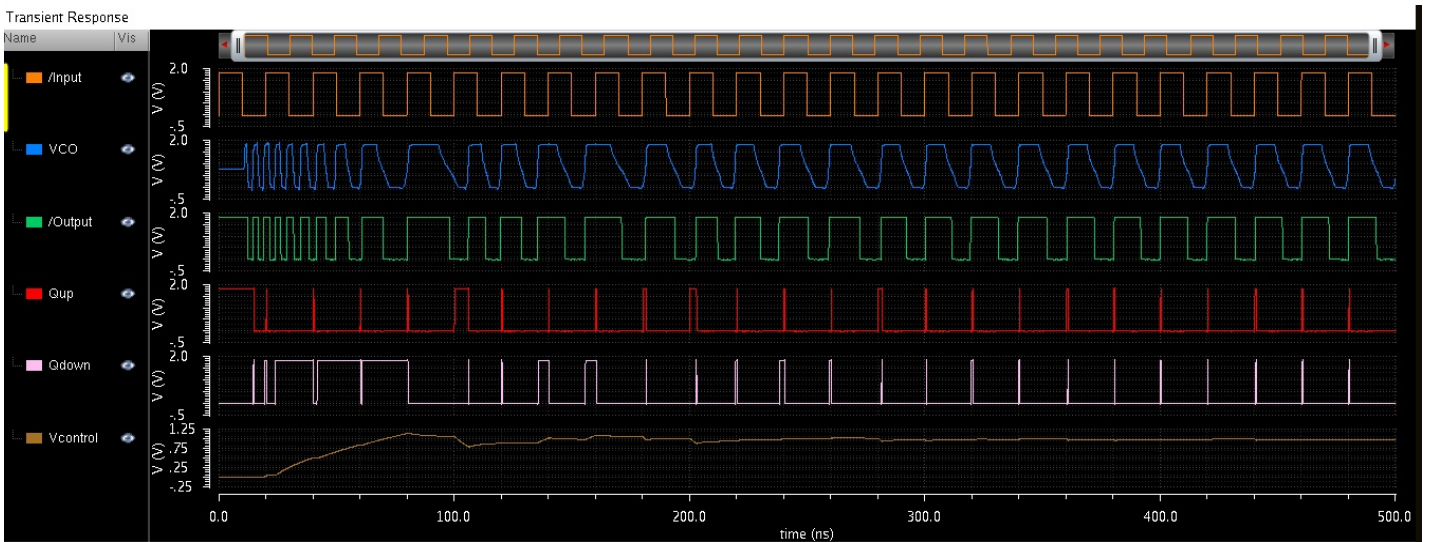
Figure 39: Input Signal of 50 MHz

The settling time for the 50 MHz in *Figure 39* was also close to 200 nsec but the output was

much more stable than the 200 MHz signal.
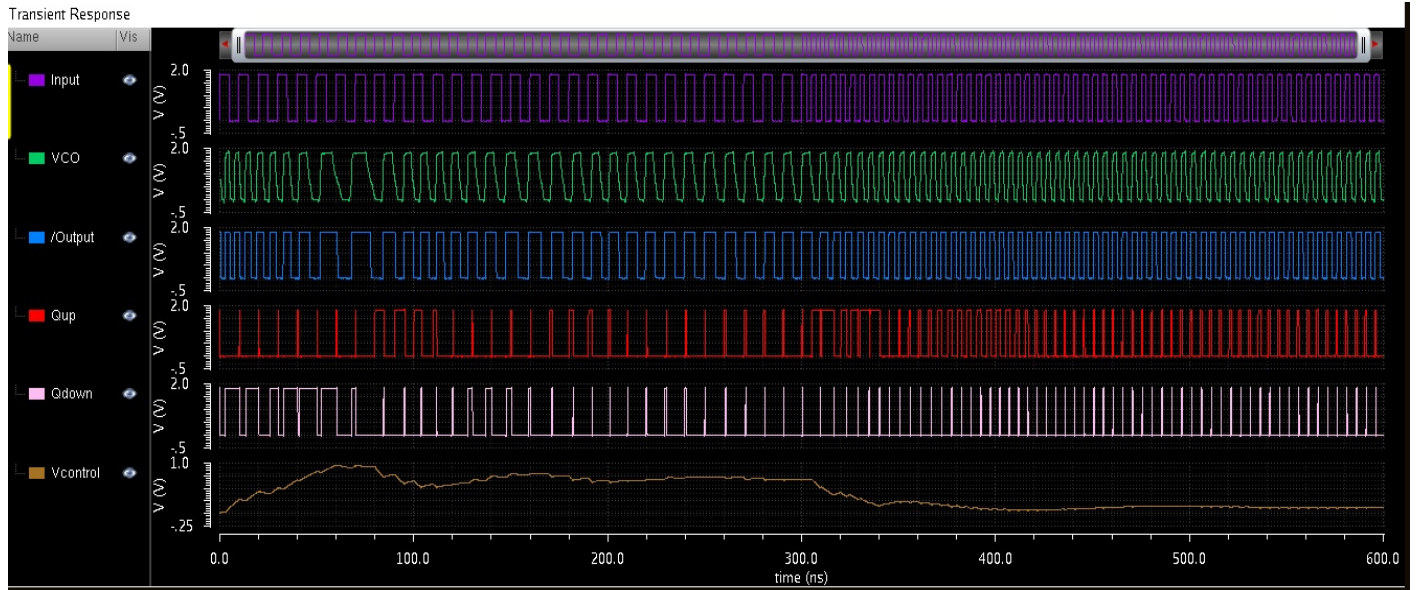
Figure 40: Input Signal of 100-200 MHz

The final test case was one where the frequency was changed from 100 MHz to 150 MHz after

300 nsec, which was hopefully enough time for the system to lock at both frequency inputs. It

was observed that the PLL was able to lock at both frequencies shown in *Figure 40*.
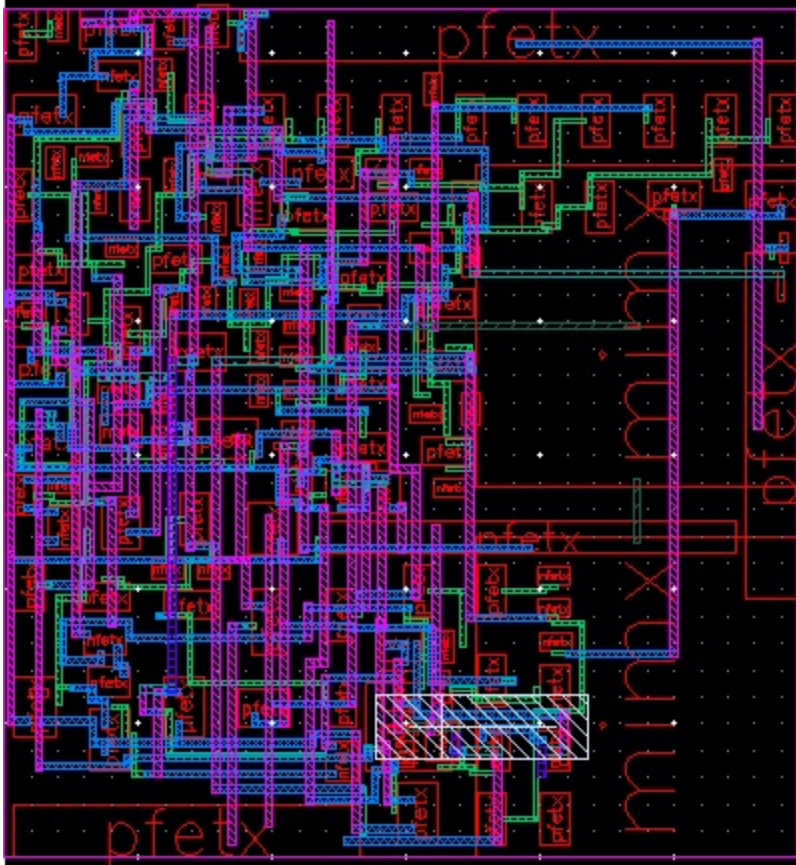
Figure 41: Layout of the PLL

The layout of the PLL, shown above in *Figure 41*, was originally a goal to be completed but because of many different problems using the Layout tools in Cadence we weren't able to. The Auto Routing tool was only able to make approximately 70% of the connections and there were hundreds of DRC errors associated with it. This gave us limited options on how to complete this objective. Each DRC error could have been dealt with one by one or the whole PLL could have been manually routed but due to time constraints neither of these options seemed realistic.

Conclusion

Overall, designing a PLL gave us a great opportunity to go through the entire design process of an IC. By researching, designing, and testing the PLL we were able to review and expand on many different topics that have been learned throughout our college career. Since PLL design requires knowledge of control systems, analog, digital circuitry and communications, this project served as a perfect means to exercise this knowledge in a "real-world" application. Also by using Cadence's Virtuoso software we were able to gain experience using a design tool that is used in industry. It was unfortunate that we were not able to take this project to the tapeout stage, but the design process took longer than anticipated and the layout was proving to be more challenging due to program restraints. In any case, the design and schematic work proved challenging in its own right and provided us with an opportunity to approach a design oriented project with many different options.

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Project Title: Phase Locked Loop Integrated Circuit

Students: Jonathan Bonello and Scott Buchanan

Advisor: Professor Tina Smilkstein

1. Summary of Functional Requirements

This project focuses on the design and application of a Phase Locked Loop (PLL). The PLL will consist of a number of components, most notably a voltage controlled oscillator, phase frequency detector, charge pump, and loop filter. The design of this project will focus around these four components, and the process behind them.

2. Primary Constraints

The largest challenges associated with this project will come from a lack of knowledge about PLL layout and design. A large amount of personal research will need to be done to understand PLL operation and design techniques inside and out, especially since PLLs have not been covered in the Electrical Engineering coursework taken up to this date. On top of this, the Cadence Virtuoso Layout Suite will need to be learned. It will take a number of weeks to become proficient at this software, and it is only until then that significant progress will be able to be made on this project.

3. Economic

As far as our own economic details are concerned, the monetary cost of this project will be little to none. Online sources as well as books and journals on PLL design can all be referenced for no charge. In addition to this, there will be no bill of physical materials as the Cadence software will be used to design and simulate the integrated circuit. This process will most likely not carry over into tape-out and so there will be no material costs associated with that. However, if this were a circuit design company creating this chip, the costs would be significantly larger. The Cadence software in and of itself costs upwards of $250,000. A company wanting to use this software commercially would be subject to these costs. In addition, the fabrication and testing process could cost an extensive amount.

As far as time is concerned, the development time was split up as follows: the fall term included preliminary VCO, and Phase Frequency Detector design as well as taking the time to learn more about the Cadence software and PLL design techniques. The winter term was focused around polishing our existing designs and designing a loop filter to help the PLL meet the specifications listed. Spring term involved final system implementation and final compiling of all the documentation regarding the project.

4. If Manufactured on a Commercial Basis

Since this IC is being designed to be added to multiple type of systems it will be available for purchase separately. If it were manufactured in mass the price per unit would drop considerably and we might see the PLL price drop to around three or four dollars per

chip. In this case, a profit of five dollars could be made per chip. If the need for such a PLL begins to increase, since technology is always trending toward faster and more accurate operating speeds, then more of this product can be sold. Understandably, the manufacturing of this product would take a number of years to pay off the costs of the Cadence software and testing procedures.

5. Environmental

The only environmental concerns would be those associated with powering the computers that will be running the simulations as well as the fabrication process. The fabrication process involved uses many rare metals and silicon. It involves many chemicals which can also be harmful to the environment if disposed of improperly. On top of this there is, of course, the cost of electricity to run the fabrication machines. This has an impact on the environment. As far as our project is concerned, if the tape-out stage is not reached, none of these will be of any immediate concern.

6. Manufacturability

As far as manufacturing is concerned, a partnership with a manufacturing company would definitely need to be formed. Trying to fabricate this chip without the aid of a large facility dedicated towards that purpose would be unreasonable. It would simply be too expensive. On top of this, our chip is being developed in the IBM 180nm cmrf7sF process. The fabrication company we pick would need to support this process. Given that there are many of these companies, this shouldn't be an issue. Complications may arise

if facilities need to be shut down for any number of reasons, but in general there is a wide range of available options for manufacturing.

7. Sustainability

There are not many sustainability concerns tied to this project. Once the chip has been fabricated and is installed on the board level, very little to no upkeep is required to ensure proper operation. The only impact this product will have on sustainable use of resources is that of electricity use. With this in mind, upgrades to improve its sustainability feature would be along the lines of minimal power use/low power operation. This would minimize the electricity being used while running this product. Attempting to upgrade the chip to implement this feature would be an extensive process and would require re-design of the circuits involved, and more testing to ensure it operates as intended.

8. Ethical

To examine the ethical issues related to this project, the pertinent IEEE code of ethics will be cited. The code states that it is imperative that the engineer is able "to seek, accept, and offer honest criticism of technical work, to acknowledge and correct errors, and to credit properly the contributions of others" [6]. This is an issue commonly encountered among students and is one that will be adhered to throughout the duration of this project. If a project member fails to accept honest criticism of his/her technical work, serious problems regarding the circuit's functionality could arise, resulting in product defect, and subsequently, loss of revenue for the company producing it. Depending on the application of the product being used, lives could be put at risk as well.

Although the risk of loss of life should not be a concern for this project, this ethical code will still need to be followed.

One other pillar of the code of ethics that especially applies to this project is the agreement "to assist colleagues and co-workers in their professional development and to support them in following this code of ethics" [6]. Throughout this project, Scott and Jonathan will be helping each other grow professionally. Whether it's keeping each other accountable for the technical work we do, or being honest in stating claims about estimates we will ensure our actions are consistent with the other pillars in the IEEE code of ethics.

9. **Health and Safety**

This chip will have almost no risk associated with it once it has been manufactured and installed on the board level. There is no worry of electrical shock as the power that runs the chip is not enough to cause damage to the human body. During manufacturing however there may be the usual safety concerns surrounding operation and use of the equipment used to fabricate.

10. **Social and Political**

As far as social issues are concerned, again, the fabrication and manufacturing processes will make the most impact. Depending on where the chip will be fabricated, the company that acquires the job will have more work, stimulating the local economy.

Whether this is in the United States or abroad, this will be an effect to consider. Stakeholders include the above mentioned fabrication company and the companies that utilize such PLLs. Regarding the actual product itself, its implementation into many different applications might cause an impact on society as PLLs are used in all manners of applications. However, this effect will be extremely difficult to recognize immediately, and is not exclusively tied to the production of our chip.

11. Development

During this development process, Scott and I were required to learn and become proficient at the Cadence Virtuoso Layout Suite. This necessitated us to take a course and complete a number of tutorials. Being an industry-grade software program, this was not a trivial task. On top of this, a review of circuit design techniques as well a broad understanding of PLLs was required. Only until these two aspects were combined were we able to begin the actual design cycle. During this time, care was taken to ensure proper circuit operation through extensive simulation and testing. In addition, the design was being constantly checked against the system requirements specified in the project document.