Energy Harvesting From Exercise Machines:

LT8705 DC-DC Conversion for Elliptical Trainers

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1 Abstract

Cal Poly's Energy Harvesting from Exercise Machines (EHFEM) program aims to power the grid using human energy harvested from exercise machines in its gym. Doing so could save the school money and increase the total supply of power available on the grid. This document belongs to one of many groups attempting to design a suitable DC-DC conversion system for an elliptical trainer using an LT8705 Four-Switch Buck-Boost converter. Past teams have built other converters and developed system compatibility characteristics such as filtering, safety, and stability for interfacing components. These teams fall into one of two departments in EHFEM: DC-DC Conversion or Input Protection Circuitry.

2 Introduction

Cal Poly's Energy Harvesting from Exercise Machines (EHFEM) program aims to power the grid[1] using human energy[2] harvested from exercise machines[3] in its gym. Doing so could save the school money and increase the total supply of power available on the grid. This document belongs to one of many groups attempting to design a suitable DC-DC conversion system for an elliptical trainer using an LT8705 Four-Switch Buck-Boost (a.k.a. 'the LT8705') converter. Past teams have built other converters and developed system compatibility characteristics such as filtering, safety, and stability for interfacing components. These teams fall into one of two departments in EHFEM: DC-DC Conversion or Input Protection Circuitry. If necessary, EFHEM may require a Current Limiting team as well.

Professor Braun of California Polytechnic State University, San Luis Obispo, began the EHFEM program in 2007, aiming to utilize lost kinetic energy generated by humans [1]. Its first team charged a car battery using an elliptical trainer. The success of this project progressed EHFEM's goals toward storing this power on the grid rather than in a battery, requiring the use of an inverter as determined by [3]. Its primary aims support the "Go Green" movement to save the environment.

EHEM obtained inverter models M175 and M215 from Enphase Energy; however, measurements taken by Turner and Weiler in [8] indicate the volatile, un-filtered elliptical energy will fry the inverters, so the elliptical energy needs to be conditioned before coming in contact with the inverters. They, and Kiddoo

[1] The source from which all of our homes, businesses, and entertainment centers attain their power
[2] Kinetic energy produced by human movement
[3] Exercise machines: in this document, machines such as exercise bikes, elliptical runners/trainers, etc. This document pertains to an elliptical trainer.

and Funsten in [11], have since added Input Protection Circuitry[4], and performed research in adding Current Limiting[5] as an additional safety precaution.

Previous elliptical trainer DC-DC conversion groups include: *Energy Harvesting From Elliptical Machines Using Four-Switch Buck-Boost Topology* by Alvin Hilario [4], *Elliptical Machine DC-DC Converter for the Energy Harvesting from Exercise Machines Project* by Greg Hollister [5], *Energy Harvesting From Exercise Machines: Forward Converters With A Central Inverter* by Nick Lovgren [6], and *DC-DC Converter Design Using SEPIC Topology* by M. Kou [7]. These groups all developed DC-DC conversion systems prior to the measurements taken in [8] and therefore did not properly consider system transient impacts on their designs. Their reports contain valuable elliptical trainer power data.

This project works alongside *Buck-Boost DC-DC Converter with Input Protection System,* by David Yoo and Sheldon Chu [9], and *Energy Harvesting From Exercise Machines - DC-DC Buck Boost Converter (LT3791)*, by Matt Wong [10], and are the only three groups to have designed DC-DC since adding protection circuitry to the elliptical. We hope to build sustainable, system compatible circuits by considering input extremities, component stress levels, and thermal constraints to implement an economical DC-DC converter with more than 90% efficiency. The project aims to build a product durable for 10 years, at minimal cost. Existing energy harvesting equipment for exercise machines can cost thousands of dollars, and the energy saved is not guaranteed to pay for the price of the machine throughout its lifetime [24]. Design simplicity and student labor minimize development costs, giving EHFEM an edge over existing technology.

3 Marketing Requirements and Specifications

EHFEM determines the converter marketing requirements, and [11] and [16] determine the input and output operating requirements.

Table 3.1 and Table 3.2 show the requirements and specifications of the LT8705 4-switch Buck Boost controller used in our design, and justify each specification with the appropriate marketing requirements.

To make a product marketable, it must generate a profit. It needs to be affordable, and cheap to produce. The materials used in production should comply with the Resistance of Hazardous Substances (RoHS) directive for environment friendly disposal. The product must meet National Electrical Code (NEC) and National Electrical Manufacturer's Association's (NEMA's) safety standards. The input constraints were calculated using Weiler and Turner's Input Protection Circuitry initially, Funsten and Kiddoo's later designs did not cause any need for us to alter ours. Our converter drives the M215 inverter for increased power. Specifications account for all known design hazards.

[4] Circuitry that eliminates and protects a circuit from dangerous transients

[5] Circuitry that re-routes undesired, excess current. Necessary if the elliptical produces more power than the inverter can handle.

Table 3.1 ENERGY HARVESTING FROM EXERCISE EQUIPMENT MARKETING REQUIREMENTS AND SPECIFICATIONS

Justification	Engineering Specifications	Marketing Requirements
The safety protection circuitry outputs 40V average. Safety protection circuitry attempts to limit output voltage to <65V [2]. LT8705 datasheet indicates 80V max [12]. Elliptical won't produce less than 5V [8].	5V-80V input range.	1,5
Peak output voltage of safety protection circuitry is 65V and 10Ω resistance [8].	6.5A input current maximum.	1,5
Peak efficiency inverter voltage [2].	The converter outputs 36V	1,5
Peak power into inverter <225W [8].	Peak average output current = 6A	1,5
[12] indicates peak η=98%. Higher efficiency produces greater revenue.	Efficiency (η) > 94%	2,5
Must fulfill national standards for safe electrical and mechanical operation. NEC applies to electrical wiring and installation safety requirements. IEEE 1547 applies to interconnections between generators and the power grid. NEMA applies to testing and operational safety standards. [3]	System must fulfill NEC, IEEE 1547, and NEMA electrical safety standards.	1,4,6
Amount of money requested by the EE department to keep project costs affordable [1].	Gross Hardware cost < $250.	2
Fits within exercise machine [4].	The component system dimensions are less than 6"x6"x2".	2,3,6,7
Complying with RoHS considers long-term environmental impacts.	Components maintain RoHS compliance for safe disposal once expired.	1

NEC standard when connecting to grid [3].	**Power Factor > 0.95**	**4**
The EHFEM system should not cause the elliptical machine to respond in unexpected ways. Elliptical machine responds based on selected resistance setting [2][4][5][6][7].	**Elliptical trainer's user receives just as satisfying an exercise experience with the EHFEM system installed as without.**	**6,7**
Lead's radiation harms both people and the environment [3].	**Product uses lead-free solder.**	**4**

Table 3.2 EHFEM Marketing Requirements

Marketing Requirements
1. Sustainable and Reliable
2. Cost Effective
3. Components: small and discrete
4. NEC/UL/RoHS Compliant
5. The converter operates at maximum efficiency
6. Additional components don't impact user's safety
7. Does not alter machine exterior

EHFEM aims to provide environmental friendly energy conserving solutions. It realizes even the smallest parts, i.e. resistors, capacitors, inductors, PCB materials, etc., can significantly impact the environment. The LT8705C project integrates a low-cost, eco-friendly energy solution which considers the user's safety, making the project reliable and sustainable. The project maximizes efficiency of all involved systems, maximizing the energy conserved [13].

4 FUNCTIONAL DECOMPOSITION (LEVEL 0 and LEVEL 1)

4.1 *Level 0 Block Diagram Function Description:*

Figure 4.1.1 shows the Level 0 Block diagram of the elliptical trainer system. The elliptical trainer funnels through input protection circuitry and DC-DC conversion before reaching a microinverter that places the power on the grid. This project focuses on the design and development of the DC-DC converter highlighted in red. Tables 4.1.1-4.1.4 describe the characteristics of each component in Figure 4.1.1.

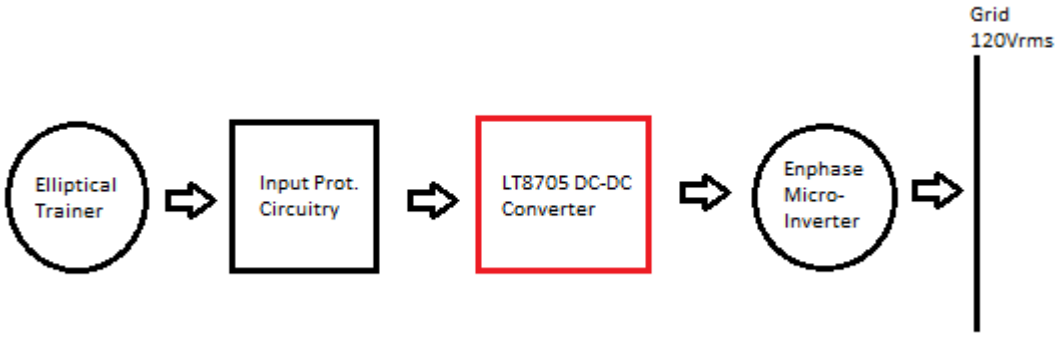

Figure 4.1.1 Level 0 Block Diagram: EHFEM System

Table 4.1.1 Elliptical Trainer

Module	Elliptical Trainer
Inputs	Human energy
Outputs	Electrical Energy: $V_{IN,MAX}$=65V, $I_{MAX,DC}$=15A [8]
Functionality	Source. Provides circuit with power.

Table 4.1.2 Input Protection Circuitry

Module	Input Protection Circuitry
Inputs	Elliptical Trainer. Values are seen in Table 3.1 Outputs.
Outputs	$V_{MAX,DC}$=65V, $I_{MAX,DC}$=6.5A [8]
Functionality	Filters and stabilizes power delivered by the elliptical.

Table 4.1.3 LT8705 DC/DC Converter

Module	LT8705 4-Switch Buck Boost Controller
Inputs	-Input from protection circuits: 0-65 V DC, 0-6.5 A [8] -300W DC power limit for LT8705 chip [12]
Outputs	-Micro Inverter: $V_{IN,MAX,DC}$=48V, $I_{MAX,DC}$=15A [16]
Functionality	Channels conditioned energy from protection circuitry to micro inverter.

Table 4.1.4 Enphase Energy M215 Microinverter

Module	MicroInverter
Inputs	36V, 6A [8]
Outputs	215W AC, single or 3-ø [16]
Functionality	Delivers elliptical power to grid.

4.2 Level 1 Block Diagram Function Description:

Figure 4.2.1 describes what the LT8705 does internally. Safety circuitry supplies current in through a "Power Path" and out to the inverter. The rest of the blocks sense and regulate the power going through the Power Path and condition it. Each of the blocks and external connections are described in Table 4.2.1 through

Table 4.2.9. The functions were either derived or deduced, or came from [12]. Section 6 discusses any derivations and deductions.

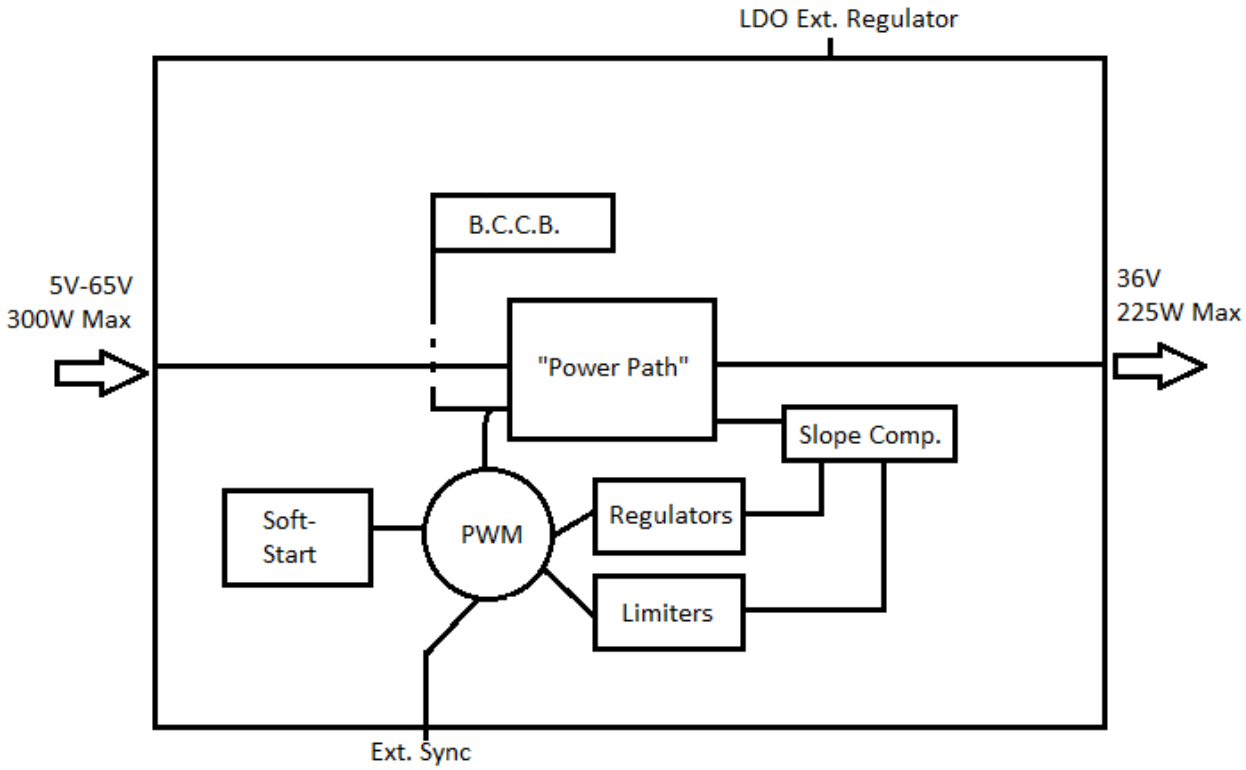

Figure 4.2.1 4-Switch Buck-Boost Internal Flow

Table 4.2.1 LT8705 Soft Start

Module	Soft Start (SS)
Inputs	Internally driven.
Outputs	LT8705 pulse-width modulator (PWM)
Functionality	Slows switching to regulate current pull during start-up. Start-up time is determined by the time constant of the SS pin capacitor and an internal 100kΩ resistor. 100nF to 1µf recommended by the datasheet. Increasing C_{SS} increases start up time, and reduces peak current pull during start-up.

Table 4.2.2 Boost Capacitor Control Block (B.C.C.B)

Module	B.C.C.B.
Inputs	Internally driven.
Outputs	Gates of switches Q1 and Q4.

Functionality	Boosts Q1 and Q4's ability to switch after remaining closed for extended periods of time. Need to be large enough to store 10x the gate charge of Q1.

Table 4.2.3 The "Power Path"

Module	LT8705 4-Switch Buck Boost Controller
Inputs	-Input from protection circuits: 0-65 V DC, 0-6.5 A [8] -300W DC power limit for LT8705 chip
Outputs	-Micro Inverter: $V_{IN,MAX,DC}$=48V, $I_{MAX,DC}$=15A [16]
Functionality	Core of the circuit. Consists of the four switches, diodes, inductor, sense resistors, and filter capacitors. Channels the energy from the elliptical trainer into a useable form for the inverter.

Table 4.2.4 Pulse-Width Modulator (PWM)

Module	LT8705 4-Switch Buck Boost Controller
Inputs	Sense circuitry and soft-start.
Outputs	Q1, Q2, Q3, Q4 gates, Sync pin
Functionality	Regulates all switching activity within the circuit.

Table 4.2.5 Slope Compensation

Module	Slope Compensator
Inputs	Power Path.
Outputs	Regulators and current limiters.
Functionality	Combines with the sensed voltages that feed the regulators and current limiters for improved switching performance.

Table 4.2.6 Regulators

Module	Input/Output Voltage Regulators
Inputs	-Input from protection circuits: 0-65 V DC, 0-6.5 A [8] -300W DC power limit for LT8705 chip

Outputs	PWM
Functionality	FBIN stops switching activity when the source voltage drops below a specified level. FBOUT regulates the output voltage at the desired level. The SHDN pin tells the circuit when to turn off when power is no longer present.

Table 4.2.7 Limiters

Module	Input/Output Current Limiting
Inputs	Slope compensator
Outputs	PWM
Functionality	Pins CSP/CSN, CSPIN/CSNIN, and CSPOUT/CSNOUT limit the current draw from the source and into the load. The elliptical trainer can potentially produce 422.5W but the maximum power the LT8705 can withstand is 300W. Similarly, the inverter only handles 225W. At 65V the current is limited to 6.0A

Table 4.2.8 LDO External Regulator

Module	LDO33 Pin
Inputs	Internally driven.
Outputs	3.3V, 17.25mA
Functionality	Bonus voltage regulator built into the chip. Able to drive small loads like microprocessors. Almost used to drive a fan for cooling the board, but did not provide enough power for a fan on the board.

Table 4.2.9 External Sync

Module	Sync/Clockout Pins
Inputs	PWM

Outputs	Other Converters
Functionality	The SYNC pin allows interleaving multiple SMPSs for higher efficiency. CLKOUT drives another SMPS, and its duty cycle can be used to estimate the internal temperature of the die.

5 Financial Analysis

5.1 Pre-Analysis

This section of the report analyzes the financial prospects of the project.

Table 5.1.1, Table 5.1.2,

Table 5.1.3, and Table 5.1.4 estimate the cost of components needed to build the figure shown in Figure 5.1.1 **Design of LT8705 4-Switch DC-DC Converter**.

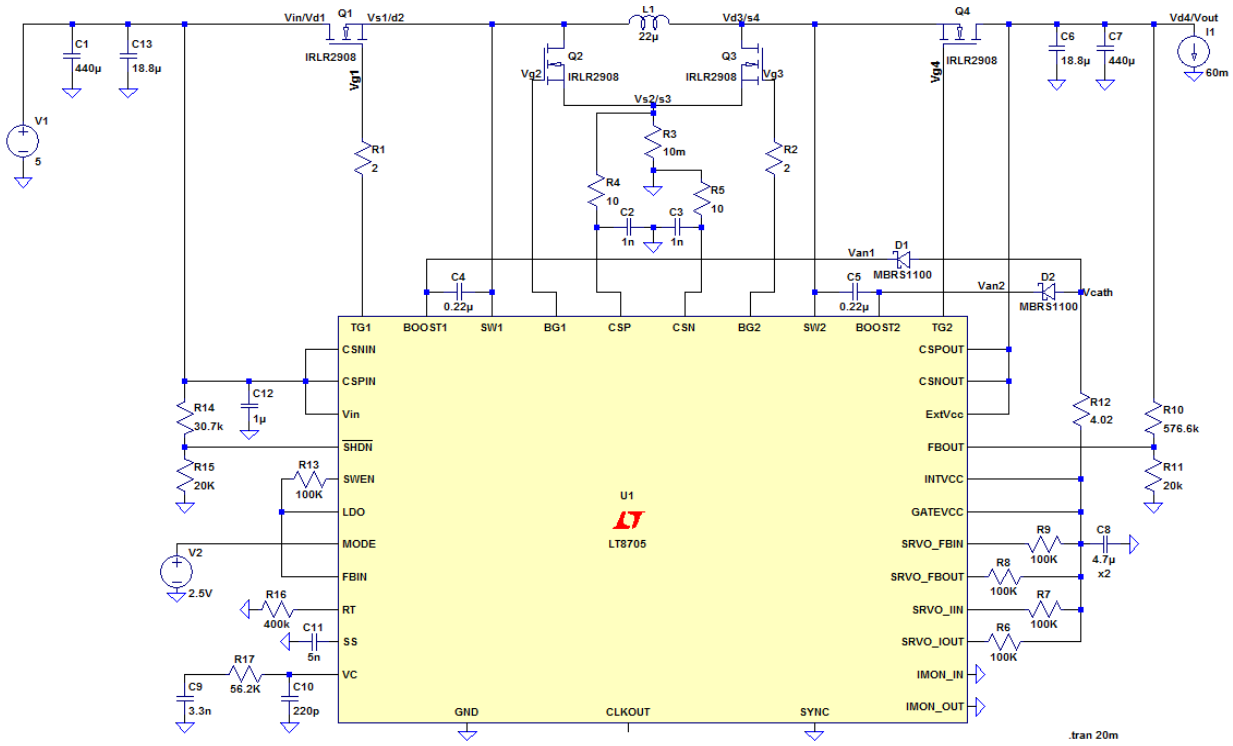

Figure 5.1.1 Design of LT8705 4-Switch DC-DC Converter

Table 5.1.1 Capacitor Value, Quantity, and Cost

Cost ($)	Quantity	Capacitors (F)
$10x2 = 20	2	440u
$7x2 = 14	2	18.8u
$0.15x3 = 0.45	3	1u
0.03	1	5n
0.01	1	220p
0.01	1	3.3n
$0.06x2 = 0.12	2	0.22u
$0.26x2 = 0.52	2	4.7u
35.14	14	Total

Table 5.1.2 Resistor Value, Quantity, and Cost

Cost ($)	Quantity	Resistors (Ω) [1% Tolerance]
0.05	1	30.7k
$0.05x2 = 0.10	2	20k
$0.05x5 = 0.25	5	100k
0.05	1	400k
0.05	1	56.2k
$0.05x2 = 0.10	2	2
0.01	1	10m
$0.05x2 = 0.10	2	10
0.05	1	4.02
0.05	1	576.6k
0.81	17	Total

Table 5.1.3 Miscellaneous Value, Quantity, and Cost

Cost ($)	Quantity	
1.00	1	Inductor - 22uH
$0.15x2 = 0.30	2	Diode
$3.00x4 = 12.00	4	Power Mosfet
7.00	1	LT8705
20.30	8	Total

Table 5.1.4 Total Cost of all Components

Cost ($)	Component
35.14	Capacitors
0.81	Resistors
20.30	Miscellaneous
56.25	Total

PG&E charges 15.9 cents per kilowatt hour (kWh) during peak hours winter [18], the time of year the Rec Center is most used. Calculation 5.1 estimates how much saved energy pays for the price of the components.

$$\$56.52/\$.159/kwh = 354\ kWh \tag{5.1}$$

The EFHEM project needs to save 354kWh to pay for the estimated components. Enphase rates their M215 Inverter at 215W maximum, or .215kW. The ratio of calculation 5.1 and the inverter's power predicts the minimum number of hours the elliptical trainer needs to operate to pay for the components.

$$\frac{354kWh}{.215kW} = 1{,}650\ hours \tag{5.2}$$

Equation 5.2 predicts the elliptical trainer needs to operate 1,650 hours to pay for the cost of components. Assuming an elliptical trainer at the gym operates 6 hours a day, this means the converter is estimated to take 275 days to pay for components; less than one year.

The previous calculations don't account for the costs of labor necessary complete the design. The average rate of pay of an intern could be $25.00 hourly. For three students who each put 150 hours into the project, this accumulates to

$$3\ students * \$25.00/(hr * student) * 150\ hours\ = \$11{,}250 \quad (5.3)$$

The project could never repay such a cost in its lifetime.

5.2 Post-analysis

This portion of the report analyzes the differences between the predicted and actual costs of constructing the circuit.

Table 5.2.1 Complete Cost Analysis

Component Value	Part Number	Ordered for Project	ppu (price per unit) ($)	Total Cost ($)
-	LT8705EFE	2	-	
-	CSD19506KCS	4 (3 samples)	5.18	5.18
-	MBRS1100	12	-	
33uH	XAL1510-333	3	-	
470uF	EEV-FK1K471M	4	2.41	9.64
150uF	EEVFK1K151Q	10	1.70	17.00
1uF	C3216X7R2A105M160AA	10	.26	2.59
10uF	CL21B106KPQNNNE	5	.29	1.45
1.8uF	C0805C185K4RACTU	4	.84	2.52
3.3nF	0805YA332FAT2A	3	.60	1.80
1nF	CL21B122KBANNNC	4	.10	.40
270pF	C0603C271K5RACTU	3	.36	1.08
1mΩ	CSNL1206FT1L00	4	1.05	4.20
4.02Ω	CRCW12064R02FKEA	3	.10	.30
10mΩ	ERJ-8BWFR010V	3	1.17	3.51
10Ω	RK73H2BTTD10R0F	4	.10	.40
20kΩ	WK73R2HTTE2002F	4	.27	1.08
27.4kΩ	ERJ-3EKF2742V	3	.10	.30
56.2kΩ	CRCW251256K2FKEG	3	.39	1.17
62kΩ	ERJ-6ENF6202V	3	.10	.30
576kΩ	P576KDACT-ND	3	.63	1.89
261kΩ	ERJ-3EKF2613V	3	.10	.30
200kΩ	P200KHCT-ND	6	.10	.60
Heatsink	577202B00000G	4	.35	1.40
Red Posts	J10125-ND	2	4.05	8.10
Black Posts	111-0703-001	2	4.05	8.10
4-Layer Board	EZQ # 1017678	2	205.00	410.00
Stencil		1	100.00	100.00
Total				**583.31**

PG&E charges 15.9 cents per kilowatt hour (kWh) during peak hours winter [18], the time of year the Rec Center is most used. Calculation 5.4 estimates how much saved energy pays for the price of the project.

$$\frac{\$583.31}{\frac{\$.159}{kwh}} = 3{,}670\ kWh \quad (5.4)$$

The EFHEM project needs to save 354kWh to pay for the estimated components. Enphase rates their M215 Inverter at 215W maximum, or .215kW. The ratio of calculation 5.4 and the inverter's power predicts the minimum number of hours the elliptical trainer needs to operate to pay for the components.

$$\frac{3{,}670kWh}{.215kW} = 17{,}100\ hours \tag{5.5}$$

Equation 5.5 predicts the elliptical trainer needs to operate 17,100 hours to pay for the complete project. Assuming an elliptical trainer at the gym operates 6 hours a day, this means the converter is estimated to take 2,850 days to pay for itself; 7.8 years. Precor fitness provides a 10 year warranty for parts and wear items, and provides servicing for its products [7].

More than 700 hours of work were done to complete this project. Supposing the same circumstances as calculation 5.3,

$$\frac{\$25.00}{hr} * 700\ hours = \$17{,}500$$

The project cost more than $17,500 in labor.

5.3 Before and After

The initial cost analysis omitted layout expenses due to poor planning. The project took more than 150% of the predicted time to complete. Our team saved a lot of money by requesting free samples for several of the components: the LT8075 chips, MOSFETS, inductor, and diodes.

Cumulatively the project has the potential to be fiscally stable if the average lifespan of a Precor Elliptical Trainer could be verified to be longer than 10 years, and all of the considered values were as predicted. Unfortunately, the values used for calculations 5.1-5.6 represent conservative minimums, so current implementation is not profitable. However, the elliptical runner can produce stable power levels up to 420W, almost 200% of what the inverter can put out; in other words, currently EHFEM only harvests at 50% of its full potential. Future EHFEM teams should research optimizing the existing circuitry and maximize the potential power harvested from the elliptical trainers. Recommended points of improvement from start to finish of the EHFEM redesign include: increasing the maximum output power of the inverter; adjusting the input protection circuitry to allow the output of the elliptical to remain stable at higher levels; re-designing, for the purpose of optimizing, and interleaving two LT8705 converters (the ones in this project), although interleaving two of our converters would be sufficient. Redesigning the DC-DC converter should be placed last when optimizing the system since its constraints are determined from the other blocks of the project.

6 Design Considerations

The following section discusses the calculations and considerations made when building the LT8705 circuit. The equations used can be found in the LT8705 datasheet [12] unless otherwise specified.

6.1 Design One:

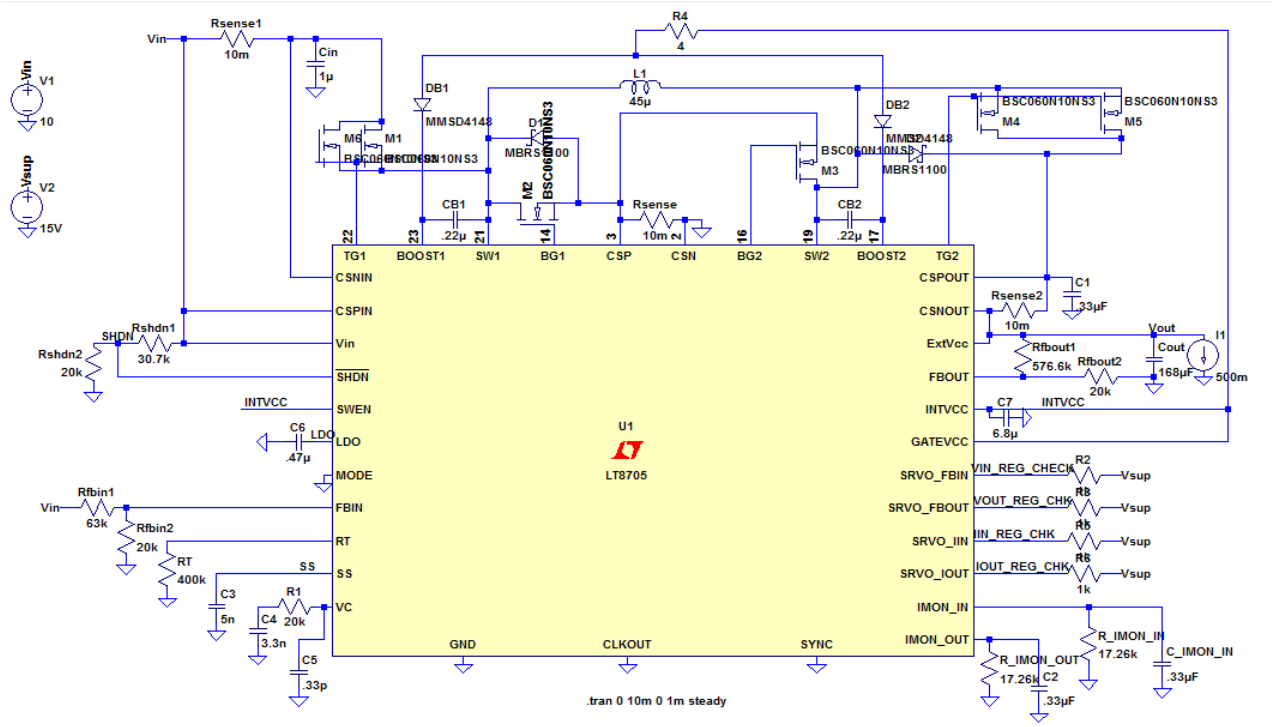

Figure 6.1.1 First Design, May 2014

6.1.1 Frequency Selection:

The datasheet recommends selecting the switching frequency of the buck-boost before anything else. Frequency selection trades off between efficiency and component sizes. Lower frequency increases efficiency by reducing switching losses, but increases the size of components. EHFEM wants the highest achievable efficiency, so our team picked a combination of the lowest operating frequency available in the LT8705 datasheet with the closest, simplest standard resistance value available for R_T.

$$f_{sw} = \left(\frac{43{,}750}{R_T + 1}\right) kHz$$

$$\boldsymbol{R_T = 400k\Omega,\ f_{sw} = 109.1kHz} \quad (6.1)$$

Calculation 6.1 shows the resistance needed to achieve the desired operating frequency, and the exact corresponding switching frequency.

6.1.2 Sense Resistor Selection

The datasheet recommends calculating R_{SENSE} next, which senses for and regulates slope compensation at peak and trough inductor current values. Several considerations are made whilst sizing R_{SENSE}, and these can be found in the datasheet. The calculations below only include the dominant decision factors. R_{SENSE} can't prevent current pull in boost mode, so Boost mode limits its size.

$$Max\ Duty\ Cycle\ (DC)M3\ Boost = \left(1 - \frac{V_{IN,MIN}}{V_{OUT,MAX}}\right) * 100 = \left(1 - \frac{5}{36.2}\right) * 100 = 86.1\%$$

Use this value with the table from Figure 6.1.2 to find the maximum sense voltage.

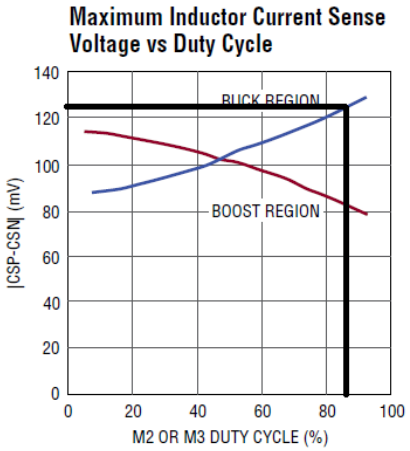

Figure 6.1.2 R_{SENSE} Voltage at Maximum Boost Duty Cycle

$$V_{RSENSE1,MAX} = 125mV$$

Inductor current ripple influences R_{SENSE}. The inductor value is not yet known so the estimation equations are used.

$$\Delta I_{L,MAX,BOOST} = \frac{V_{OUT,MAX} * I_{OUT,MAX,Boost}}{V_{IN,MIN} * \left(\frac{100}{\%ripple} - .5\right)} = \frac{36V * .5A}{5 * \left(\frac{100}{10} - .5\right)} = .66A \quad (6.2)$$

$$R_{SENSE,Max} = \frac{2 * V_{RSENSE,MAX} * V_{IN,MIN}}{2 * I_{OUT,MAX,Boost} * V_{OUT,MIN} + \Delta I_{L,MAX,BOOST} * V_{IN,MIN}} = \frac{2 * 125mV * 5V}{2 * 3.2 * 36 + .66 * 5} = 14.2m\Omega \quad (6.3)$$

$I_{OUT,MAX,Boost}$ was determined using the datasheet. It's the maximum output current in boost mode. The datasheet recommends using a value at least 30% less than the maximum.

$$Maximum\ Rated\ R_{SENSE} = \frac{14.2m\Omega}{1.3} = 10.6m\Omega$$

To simplify component sizing and selection,

$$\boldsymbol{R_{SENSE} = 10m\Omega}$$

Both R_{SENSE} values equal 10mΩ.

6.1.3 Inductor Selection

For high efficiency, choose an inductor with low core loss, i.e. ferrite, low DC resistance (DCR), high peak current limit to prevent saturation. Minimize radiated noise using toroid, pot core, or shielded inductors.

$$\boldsymbol{L_{MIN}} = \frac{(V_{OUT,MAX} - \frac{V_{IN,MIN} * V_{OUT,MAX}}{V_{OUT,MAX} - V_{IN,MIN}}) * R_{SENSE}}{.08 * f} = \frac{\left(36.2 - \left(\frac{5 * 36.2}{36.2 - 5}\right)\right) * .001}{.08 * 109{,}100} = \boldsymbol{3.5\mu H}$$

The LT8705 datasheet only gives a minimum inductance; example circuits use 22µH, so we chose 45µH because it was the largest inductor with 14A current rating in LTSpice library [12]. This halves the current ripple relative to 22µH.

6.1.4 Regulators and Limiters

The LT8705 has regulation and limiting features that simply the Level 0 Block Diagram design. The introduction indicated previous projects required current limiting external to the DC-DC converter the students had built. Using the internal limiting of the LT8705 allows us to eliminate this component of the system. This decreases size, and increases efficiency of the system.

6.1.5 Output Voltage Regulator

Regulates the output to a specified voltage using a resistive divider network. Large resistors consume less power when constant voltage is applied across them according to Ohm's Law.

$$V_{out} = 1.207V * \left(1 + \frac{R_{FBOUT1}}{R_{FBOUT2}}\right)$$

$$\boldsymbol{R_{FBOUT2} = 20k\Omega \rightarrow \ R_{FBOUT1} = 576.6k\Omega}$$

6.1.6 Input Voltage Regulator

If the source has high output impedance and large current pull causes it to drop below a specified setpoint, the input voltage regulator will stop switching activity to limit the voltage drop. **This is not accompanied by a soft-start.

$$V_{in,min} = 1.205V * \left(1 + \frac{R_{FBIN1}}{R_{FBIN2}}\right)$$

$$\boldsymbol{R_{FBIN2} = 20k\Omega \rightarrow \ R_{FBIN1} = 63k\Omega}$$

6.1.7 Input/Output Current Monitoring

These resistor-capacitor networks limit the input and output currents. The maximum in and out has to be 6.5A according to [2].

R_{IMON_IN} and R_{IMON_OUT} use the same equation for calculating their sizes, they differ in their limits. Calculate them as follows:

$$\boldsymbol{R_{IMON\_IN}} = \left(\frac{1.208}{I_{in,limit} * 1m\left(\frac{A}{V}\right) * R_{SENSE}}\right)\Omega = \frac{1.208}{6.5 * .001 * 10m\Omega} = \boldsymbol{17.26k\Omega}$$

$$\boldsymbol{R_{IMON\_OUT}} = \left(\frac{1.208}{I_{out,max,average} * 1m\left(\frac{A}{V}\right) * R_{SENSE}}\right)\Omega = \frac{1.208}{6.5 * .001 * 10m\Omega} = \boldsymbol{17.26k\Omega}$$

$C_{IMON\_IN,\ IMON\_OUT}$ can be any value between 0.1µF to 1µF. We chose 0.33µF.

The rest of the components were default FETs and diodes, and random values chosen from the datasheet. The simulation did not work, the simulation froze, seen in Figure 6.1.3.

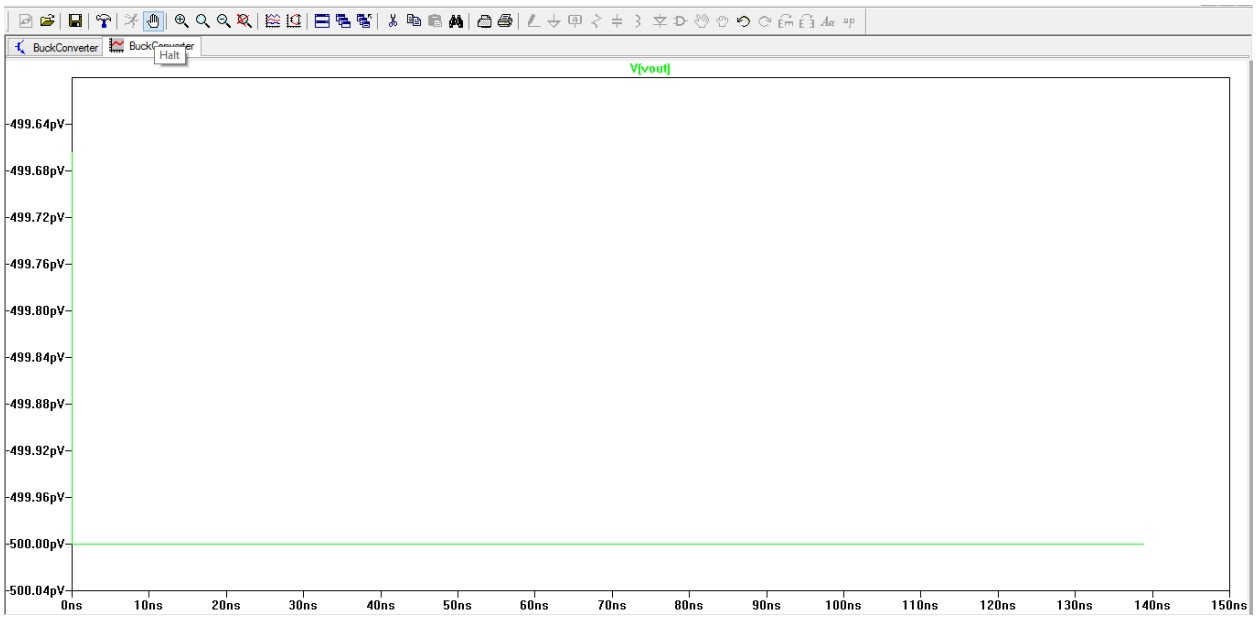

Figure 6.1.3 Frozen Simulation

6.2 Design Two:

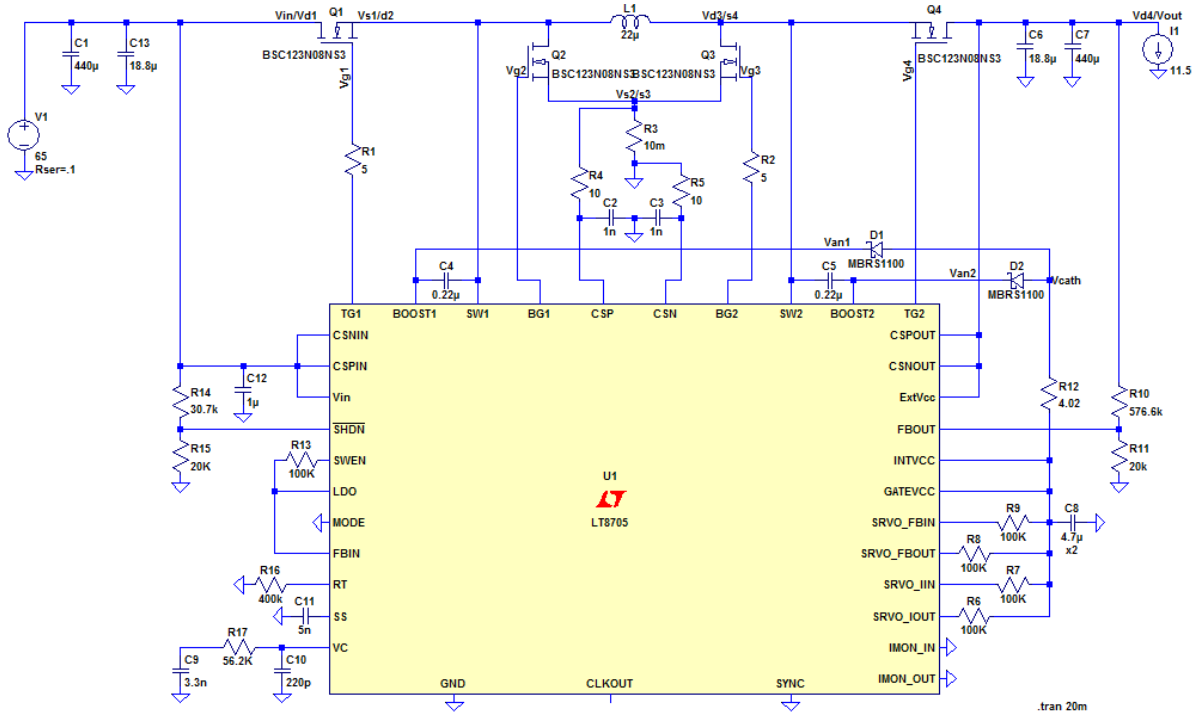

Figure 6.2.1 Second Design, June 2014

Design two, Figure 6.2.1, was practically a copied version of a simpler example LT8705 circuit given in LTSpice. It was used as a starting point since the first design didn't work and our group didn't know how to begin troubleshooting. It eliminated the SRVO pins, the regulator pins, and the sense resistors. The simulations following demonstrated a functional circuit but with many defects.

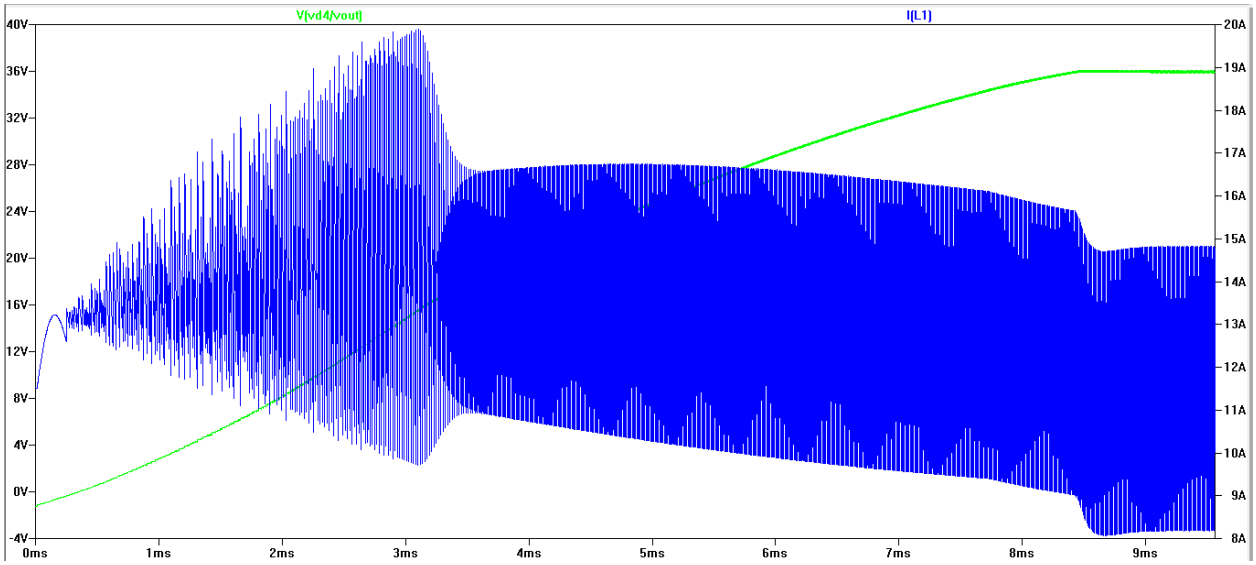

Figure 6.2.2 Inductor Current

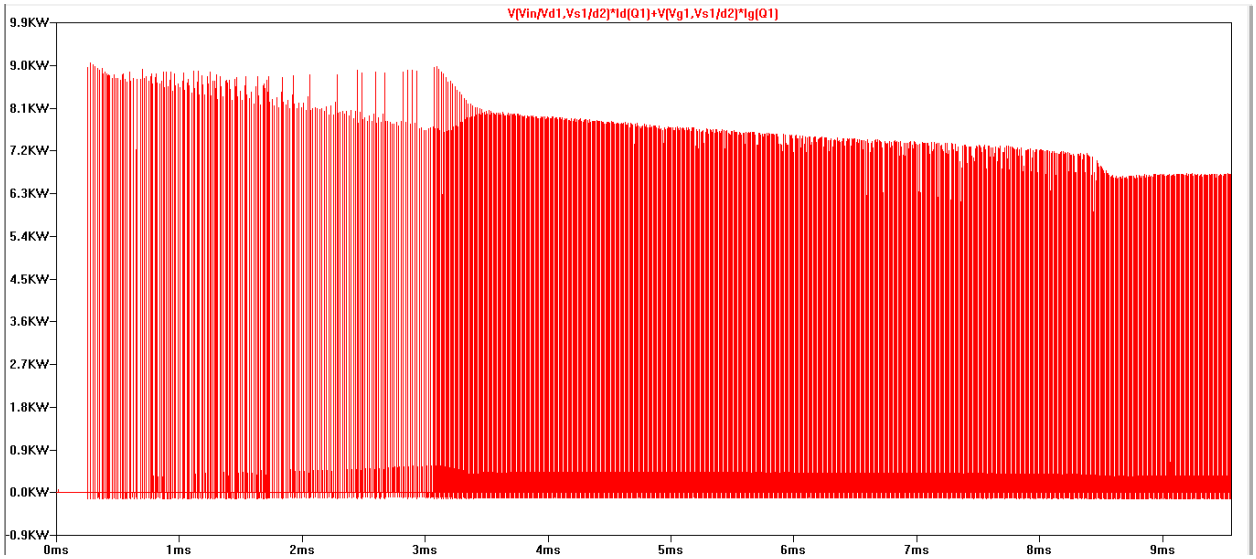

Figure 6.2.3 Q1 Power Dissipation

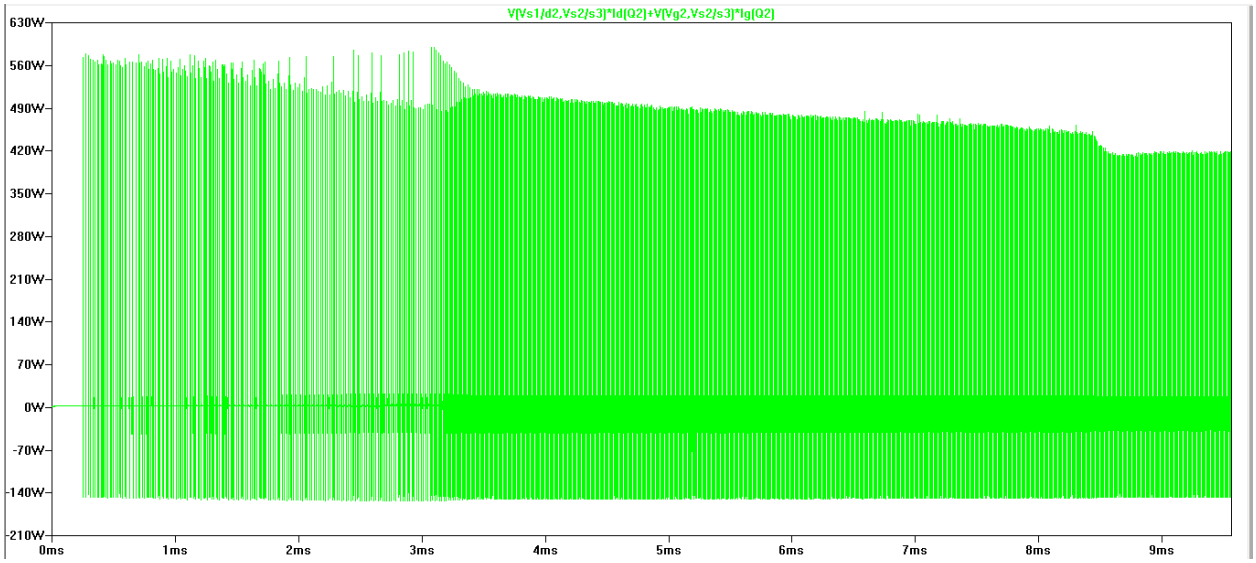

Figure 6.2.4 Q2 Power Dissipation

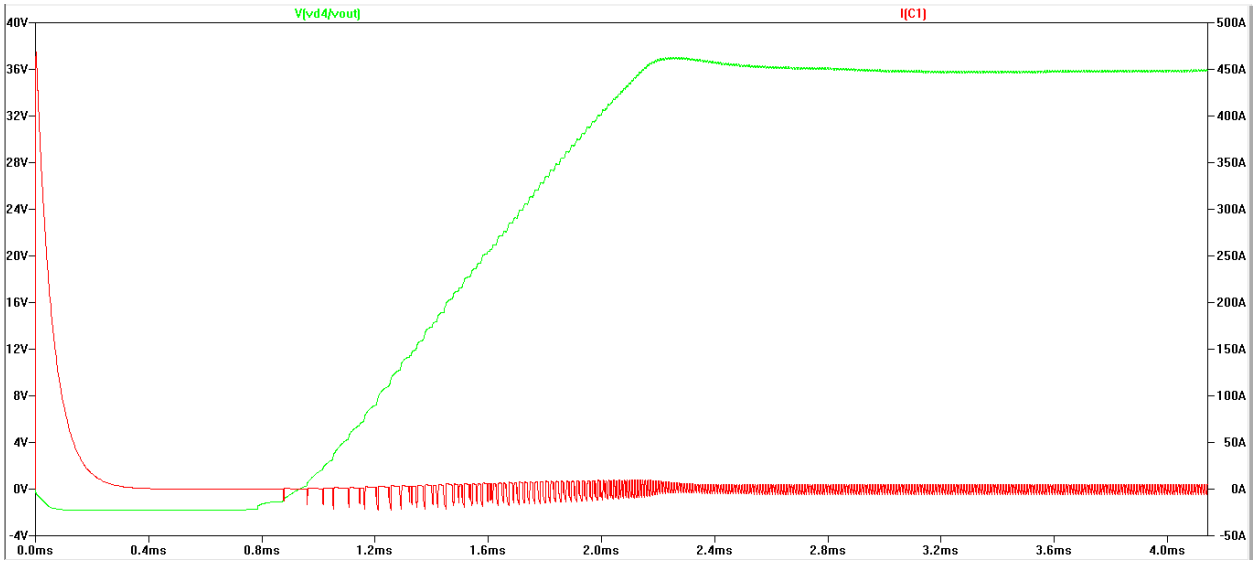

Figure 6.2.5 Input Capacitor Surge Current

Figures 6.2.2 through 6.2.5 show that our original design had way too high inductor current, huge power spikes in Q1 and Q2, and 500A of current at time t=0.

6.3 Design Three:

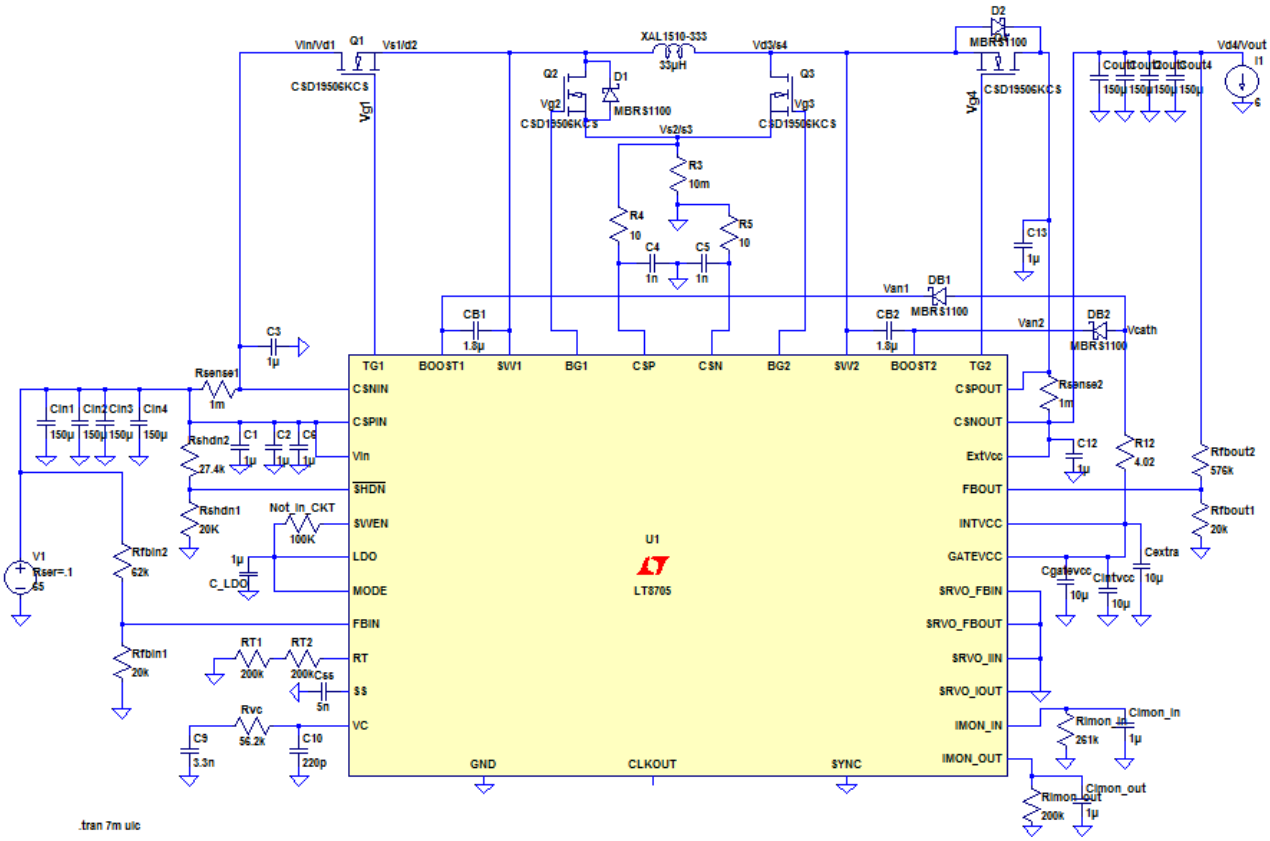

Figure 6.3.1 LT8705 Design 3 DC-DC Converter for EHFEM, October 2014

Many reconsiderations regarding the input and output current, voltage, and power relationships were made, and produced the following input/output constraints in addition to others that may appear later. The new values in this design passed simulation verifications.

6.3.1 Preliminary Considerations

The input protection circuitry provides 65V peak at 10Ω input resistance.

$$P_{in,max} = \frac{V^2}{R} = \frac{65^2}{10} = 422.5W \tag{6.4}$$

$$P_{out,max} = 215W, \;\; V_{out} = 36V \tag{6.5}$$

$$I_{out,max,average} = \frac{P_{out,max}}{V_{out}} = \frac{215}{36} = 5.97A \approx 6A \tag{6.6}$$

$$V_{IN,MAX,Boost} = \left(1 - DC(duty\ cycle)_{MIN,Boost}\right) * V_{out} = .97 * 36 = 34.9V \tag{6.7}$$

$$I_{IN,MAX,Boost} = \frac{P_{IN,MAX,Boost}}{V_{IN,MAX,Boost}} = \frac{V_{IN,MAX,Boost}}{10\Omega} = 3.214A \tag{6.8}$$

The LT8705 can only handle 300W max, so equation (6.4) indicates the input power needs limiting. The current in (6.6) represents the peak *average* current entering the inverter while the output voltage is 36V and maximum power out is limited to 215W, seen in (6.5). Equations 6.5 and 6.6 determine the upper limit conditions of Boost Mode, important in determining component values, discussed later in this document.

6.3.2 "Power Path" Design

Start-up Time

The SS pin determines how long the LT8705 starts up. It's determined by the time constant of an internal 100kΩ resistor and the size of C_{SS} chosen by the user. The datasheet recommends at least 100nF. We chose C_{SS}=1µF.

6.3.3 Switching Frequency

The switching frequency drives the entire circuit, so accurate resistor values make a difference. No 400kΩ, SMD, 1% tolerance, affordable resistors were readily available for this component, however, 200kΩ resistors meeting these requirements were. Place two of these resistors in series to obtain the same results, as in Figure 6.3.2.

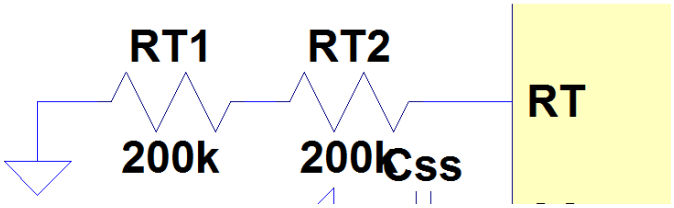

Figure 6.3.2 Close-Up of R_T Pin from Figure 6.3.1

Not a lot of current flows through these resistors, reducing their need for large power ratings. 0.1W works fine.

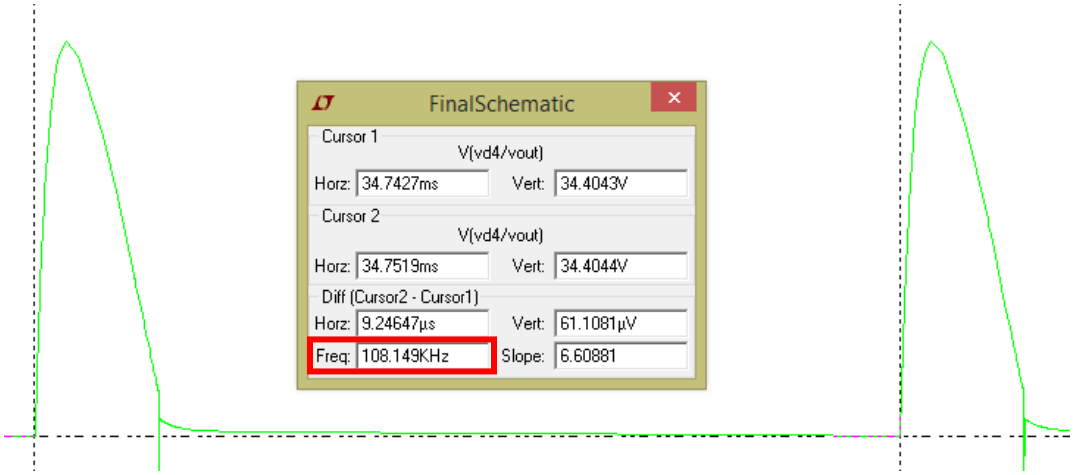

Figure 6.3.3 Simulation Capture Verifying Estimated Duty Cycle

The measured frequency in Figure 6.3.3 approximately equals our estimated frequency from Equation 6.1, verifying appropriate behavior in the circuit.

6.3.4 Sense Resistor Selection

In Design One, several errors were made when calculating the sense resistors. Those mistakes were corrected in the third design. In Figure 6.3.1, it can be seen that we measured the voltage using Buck mode, but the duty cycle used was for Boost mode. Figure 6.3.4 corrects that mistake.

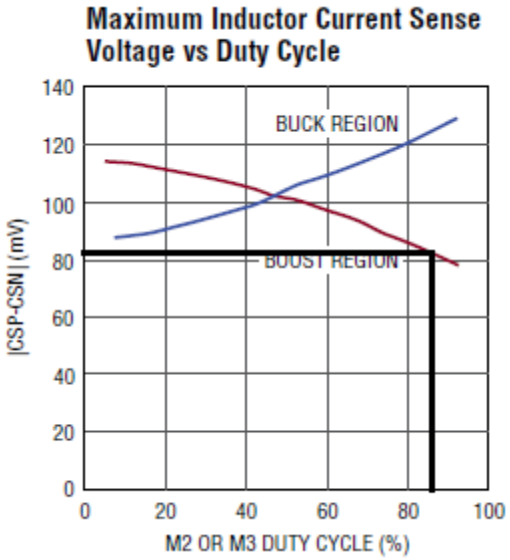

Figure 6.3.4 R_{SENSE} Voltage at Maximum Boost Duty Cycle

$$V_{RSENSE1,MAX} = 82mV$$

We used an incorrect value of 0.5A for $I_{OUT,MAX,BOOST}$ in Design One because we thought the datasheet said that's what it was supposed to be. However, the maximum output current depends on the input voltage, and occurs when V_{IN}<V_{OUT} by a small amount. This value was recalculated to be 3.2A as seen in Equation 6.8. The adjusted values recalculate R_{SENSE} as follows.

$$\Delta I_{L,MAX,BOOST} = \frac{V_{OUT,MAX} * I_{OUT,MAX,Boost}}{V_{IN,MIN} * \left(\frac{100}{\%ripple} - .5\right)} = \frac{36 * 3.214}{5 * \left(\frac{100}{30} - .5\right)} = 8.13A$$

$$R_{SENSE,Max} = \frac{2 * V_{RSENSE,MAX} * V_{IN,MIN}}{2 * I_{OUT,MAX,Boost} * V_{OUT,MIN} + \Delta I_{L,MAX,BOOST} * V_{IN,MIN}} = \frac{2 * 82mV * 5V}{2 * 3.2 * 36 + 8.13 * 5} = 3.02m\Omega$$

The datasheet recommends using a value at least 30% less than the maximum.

$$Maximum\ Rated\ R_{SENSE} = \frac{3.02m\Omega}{1.3} = 2.46m\Omega$$

To simplify component sizing and selection,

$$\boldsymbol{R_{SENSE} = 1m\Omega}$$

**There are two R_{SENSE} in the circuit, therefore this value meets the requirement R_{SENSE1}+R_{SENSE2} < R_{SENSE}. This is important because having too much resistance on the power path can cause the device to stop functioning in deep boost mode.

6.3.5 Inductor Selection

For high efficiency, choose an inductor with low core loss, i.e. ferrite, low DC resistance (DCR), high peak current limit to prevent saturation. Minimize radiated noise using toroid, pot core, or shielded inductors.

$$\boldsymbol{L_{MIN}} = \frac{(V_{OUT,MAX} - \frac{V_{IN,MIN} * V_{OUT,MAX}}{V_{OUT,MAX} - V_{IN,MIN}}) * R_{SENSE}}{.08 * f} = \frac{\left(36.2 - \left(\frac{5 * 36.2}{36.2 - 5}\right)\right) * .001}{.08 * 109{,}100} = \boldsymbol{3.5\mu H}$$

$$I_{pk,sat} = I_{out,max,average} + \frac{V_{OUT,MIN} * DC_{Max,M2,BUCK}}{2 * L * f}, where$$

$$DC_{Max,M2,BUCK} = \left(1 - \frac{V_{OUT,MIN}}{V_{IN,MAX}}\right) = .446$$

Letting L=33µH,

$$\boldsymbol{I_{pk,sat}} = 6 + \frac{36 * .446}{2 * 33e - 6 * 109100} = \boldsymbol{8.23A}$$

Now, given an inductor value, recalculate the inductor current ripple using page 22 of the datasheet [12]:

$$\Delta I_{L,MAX,BOOST} = \frac{DC_{Max,M3,Boost} * V_{IN,MIN}}{f * L} = \frac{.861 * 5V}{109.1kHz * 33\mu H} = 1.196A$$

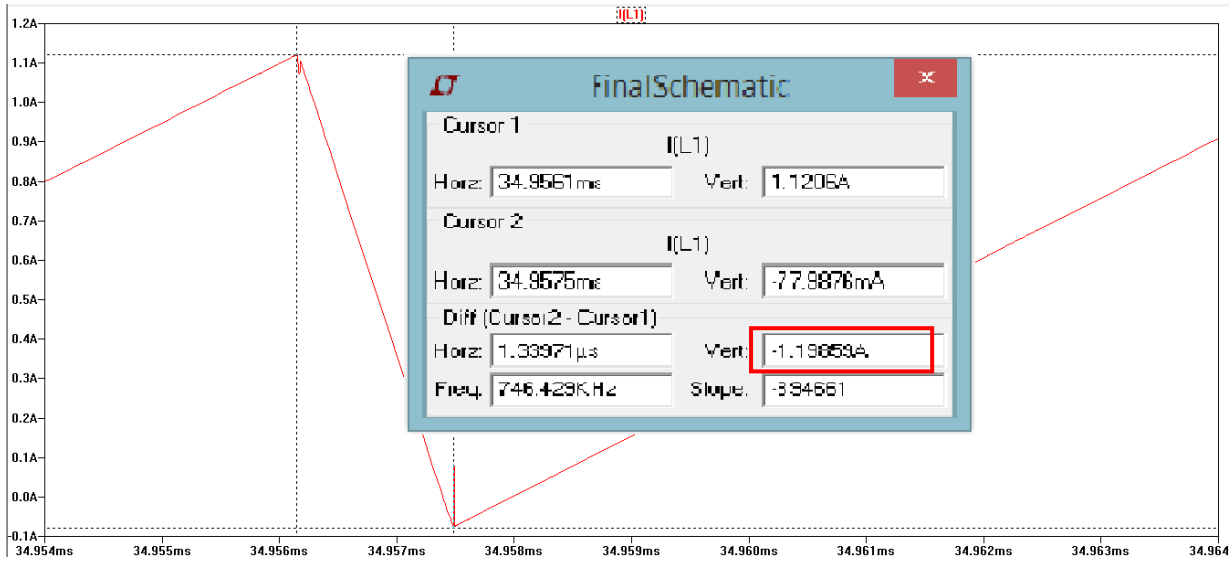

Figure 6.3.5 Simulated Inductor Current, Boost Mode, V_{IN}=5V

Figure 6.3.5 shows the inductor current ripple is 1.199A. This value is high though because the limits are longer than T=1/f_{sw}, indicating appropriate operation in boost mode.

Inductor saturation current decreases as its inductance increases. The XAL1510-333 was the highest inductor value available on the market that maintained its saturation current rating even as its nominal inductance decreases. The datasheet indicates in circuit operation its inductance could fall as low as 22µH.

$$\Delta I_{L,MAX,BOOST} = \frac{DC_{Max,M3,Boost} * V_{IN,MIN}}{f * L} = \frac{.861 * 5V}{109.1kHz * 22\mu H} = 1.794A$$
$$\Delta I_{L,MAX,BUCK} = \frac{DC_{MAX,M2,BUCK} * V_{OUT,MIN}}{f * L} = \frac{.4523 * 35.6V}{109.1kHz * 22\mu H} = 6.71A \quad (6.9)$$

At 22µH, the inductor's saturation current needs to remain higher than:

$$I_{PK,Saturation} = I_{out,average} + \frac{\Delta I_{L,MAX,BUCK}}{2} = 6 + 3.355 = 9.355A$$

The datasheet indicates its saturation current at 22µH is 17A [27]. The XAL1510-333 suffices for this circuit.

6.3.6 MOSFET Selection

Important considerations include heat dissipation, switching speed, reverse breakdown voltage, threshold voltage, on-resistance, gate-drain capacitance, and maximum current. V_{GS} = 6.35V. Table 6.3.1 compares the different kinds of power MOSFETs considered for the design, and their rated specifications.

Table 6.3.1 MOSFET Rating Chart

	CSD1905KCS	IXTH	FDS3590	CSD19506KCS	irf7493pbf-1
Pmax	300	480		375	
Vds	80	100	80	80	80
Vgs	20	30	20	20	20
Rds	2.6m	5.4m	32m	2.0m	15m
Qg	76n	151n	25n	120n	35n
Qgd	11n	45n	5.8n	20n	12n
Qgs	25n	39n	4.5n	37n	5.7n
Vth	2.6	3	3	2.5	3
t(on)delay	31n	33n	11n	19n	8.3n
tr	16n	54n	8n	11n	7.5n
t(off)delay	62n	42n	26n	30n	30n
tf	6n	31n	12n	10n	12n
Cin	6.09n	6.9n	1.18n	9.38n	1.51n
Cout	1.6n	.923n	.171n	2.26n	.32n
Rjc	.5C/W	.31C/W	25C/W	.4C/W	
Rja	62C/W		50C/W	62C/W	
Diode					
Vsd	0.9		0.74	0.9	1
Qrr	400n			525n	52n
trr	88n			107n	37n
Ids	100		2.1	100	9.3

The FET highlighted in yellow possesses the most desirable operating characteristics. The actual gate charge for our project is 84nC because the rated spec is measured at 10V. Our system uses 6.35V.

The switches consume the most power in the circuit due to their switching losses. This increases their temperatures, potentially harming the circuit. Temperature rise depends on the case-ambient resistance of the FET, and the number of watts dissipated in the switch.

$$thermal\ resistance\ CSD19506KCS\ \theta_{JA} = 62℃/W$$

The Table 6.3.2 attempts to predict the temperatures each of the switches reaches during operation, first through calculation in the datasheet, and second by simulation.

Table 6.3.2 Predicted Switching Losses and Temperatures during Actual Operation

Switch	Estimated Power Loss (W)	Estimated Operating Temperature (ºC)	Simulated Power Loss (W)	Simulated Temperature Rise (ºC)
Q1	1.06	90.41	636m	64.43
Q2	230m	39.26	63.63m	28.95
Q3	21.3m	26.32	94µ	25.01
Q4	93µW	25.01	143m	33.87

The calculations for the estimated power loss can be found in the datasheet, the temperatures were estimated using the following equation:

$$T(℃) = 25℃ + P_{loss} * \theta_{JA} \tag{6.10}$$

The datasheet indicates θ_{JA} includes the case-ambient resistance.

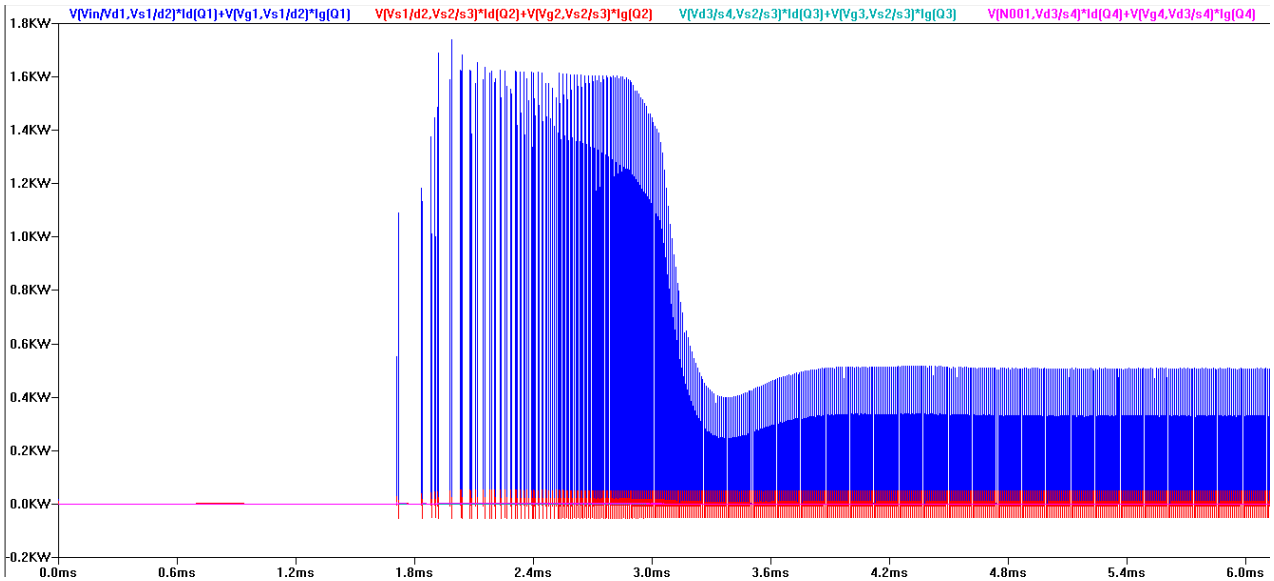

Figure 6.3.6 65V Startup Simulation

Figure 6.3.6 represents the unrealistic scenario in which the output voltage of the elliptical trainer reaches 65V during start up. It indicates the spikes could reach up to 1.8kW instantaneously. While the Safe Operating Region (SOA) of the CSD19506KCS shown in the Figure 6.3.7 could handle up to 6.825kW,

1.8kW is still a large amount of power. The next section of the design considers heat sinks to relieve this problem.

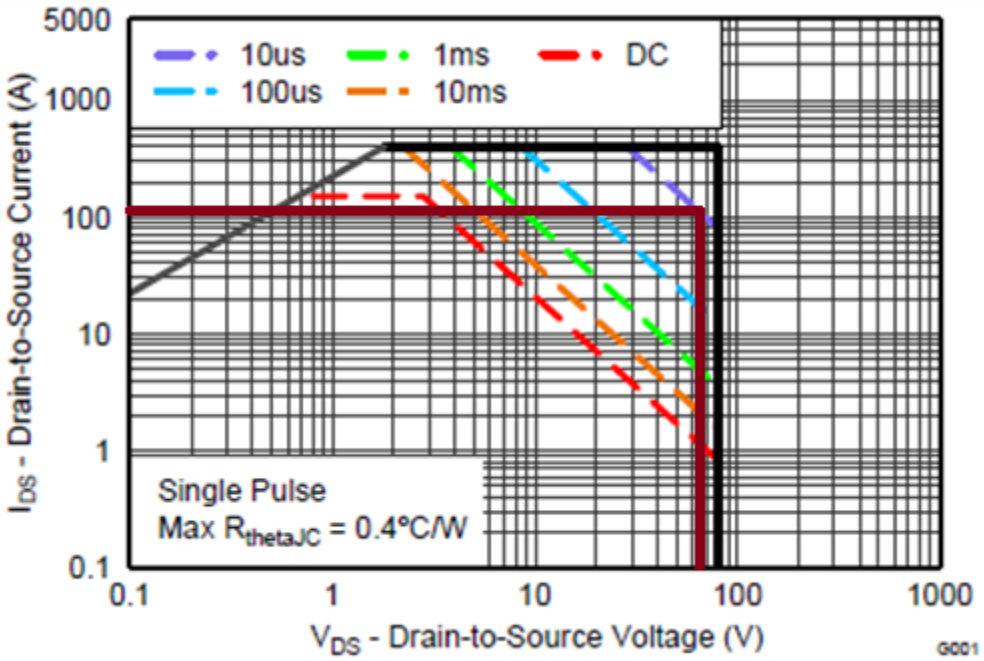

Figure 6.3.7 SOA of CSD19506KCS

$$P_{max,10\mu s} = V_{DS,MAX} * I_{DS,MAX} = 65V * 105A = 6.825kW$$

6.3.7 Heatsinks

We needed to conserve board space the heatsink package isn't much larger than the actual FETs.

$$thermal\ resistance\ heatsink\ \theta_{JA} = 24.4℃/W$$

The degree to which temperature the FETs would affect the circuit isn't an exact science due to the inaccuracy of FET simulation files. They were custom built with only limited information from the datasheet. Table 6.3.3 illustrates the degree to which the heatsinks are estimated to impact the circuit's operation.

Table 6.3.3 Modified Switch Temperatures after using Heatsinks

Switch	Estimated Power Loss (W)	Estimated Operating Temperature (ºC)	Simulated Power Loss (W)	Simulated Temperature Rise (ºC)
Q1	1.06	50.74	636m	40.52
Q2	230m	30.61	63.63m	26.55
Q3	21.3m	25.52	94µ	25.00
Q4	93µW	25.00	143m	28.49

A fan can further increase the air flow across the top of the board, and reduce the temperature impacts on the circuit.

6.3.8 C_{IN} and C_{OUT} Selection

Use parallel combination of capacitors to achieve minimal ESR. Need appropriate current ripple.

$$\boldsymbol{I_{rms}} = I_{out,max,average} * \frac{V_{out}}{V_{in,max}} * \sqrt{\frac{V_{in,max}}{V_{out}} - 1} = 6 * \frac{36}{65} * \sqrt{\frac{65}{36} - 1} = \boldsymbol{3A} \qquad (6.11)$$

The input/output capacitance needs to be nominally large, but physically small, handle a large amount of current ripple, and have low ESR.

The schematic has four 150µF capacitors on the input and output. Each has 320mΩ ESR, reducing the combined ESR to 80mΩ. Each can handle 0.5A, and the additional 1µF capacitors further reduce the ESR and absorb some of the extra current.

6.3.9 Schottky Diodes D1 and D2

Prevent body diodes of M2 and M4 from turning off, and reduce reverse recovery times. Place adjacently to respective switches. High reverse voltage, low reverse leakage current. Figure 6.3.8 shows the characteristics of the diode chosen for the design. The appropriate function of the diode is verified later.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage MBRS190T3 MBRS1100T3	V_{RRM} V_{RWM} V_R	 90 100	V
Average Rectified Forward Current T_L = 163°C T_L = 148°C	$I_{F(AV)}$	 1.0 2.0	A
Non−Repetitive Peak Surge Current (Surge Applied at Rated Load Conditions Halfwave, Single Phase, 60 Hz)	I_{FSM}	 50	A
Operating Junction Temperature (Note 1)	T_J	−65 to +175	°C
Voltage Rate of Change	dv/dt	10	V/ns

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The heat generated must be less than the thermal conductivity from Junction−to−Ambient: $dP_D/dT_J < 1/R_{\theta JA}$.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance − Junction−to−Lead (T_L = 25°C)	$R_{\theta JL}$	22	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Maximum Instantaneous Forward Voltage (Note 2) (i_F = 1.0 A, T_J = 25°C)	V_F	0.75	V
Maximum Instantaneous Reverse Current (Note 2) (Rated dc Voltage, TJ = 25°C) (Rated dc Voltage, T_J = 100°C)	I_R	 0.5 5.0	mA

2. Pulse Test: Pulse Width = 300 µs, Duty Cycle ≤ 2.0%.

Figure 6.3.8 Screen Capture of Important Diode Characteristics

The diode leaks less than 1mA while reverse biased. At 65V this is less than 6mW loss through the diode, given by:

$$P_{reverse,loss} = V_{in,max} * I_R = 65V * .5mA = 37.5mW \quad (6.12)$$

The forward biased the maximum predicted loss

$$P_{forward,loss} = V_F * I_F = .75V * 1A = 750mW \quad (6.13)$$

Equations 6.12 and 6.13 represent the maximum losses of the diode. The power through the system under maximum conditions is 215W. This means η_{loss}= 0.75W/215W= 0.35% maximum. This is insignificant.

6.3.10 Boost Capacitors C_{B1} and C_{B2}

Charge to ~6.3V. Need to store ~100x the gate charge capacities of M1 and M4. Datasheet specifies 0.1µF to 0.47µF X5R or X7R dielectric. The circuit could not simulate using 0.22µF capacitors in deep boost (V_{IN}=5V) mode. The hypothesis was made that this could be due to the boost capacitors being inappropriately sized. The following calculations were performed.

$$\begin{gathered} Q_{g,FET} = 84nC \\ Q_{CB1,CB2} = 100 * Q_{g,FET} = 8.4\mu C \\ Q = CV \rightarrow 8.4\mu C = 6.35V * C_{CB1,CB2} \\ \boldsymbol{C_{CB1,CB2} \geq 1.323\mu F} \end{gathered} \quad (6.14)$$

Inability of the circuit to operate in boost mode because of these capacitors indicates these capacitors are important for correct operation of the circuit. In this circumstance manufacturing tolerances are especially important. The C0805C185K4RACTU capacitor's nominal value equals 1.8µF. Its 10% tolerance gives it a minimum factory capacitance value of:

$$C_{min,factory} = 1.8\mu F - 10\% = .9 * 1.8 = 1.62\mu F$$

The datasheet indicates increasing voltage across the capacitor could lead to up to a further 15% decrease in its factory capacitance.

$$C_{min,actual} = 1.62\mu F - 15\% = .85 * 1.62\mu F = 1.377\mu F \quad (6.15)$$

$$C_{max,actual} = 1.8\mu F + 10\% = 1.1 * 1.8\mu F = 1.98\mu F \quad (6.16)$$

Equation 6.15 shows that the C0805C185K4RACTU is guaranteed to meet absolute minimum requirements for the circuit to operate correctly. Equation 6.16 applies to the capacitance placed on the GateVCC pin.

6.3.11 IntVCC/GateVCC

The IntVCC pin requires at least 4.7µF of capacitance. Use ceramic X7R dielectric capacitors. The GateVCC pin requires at least 10x the capacitances placed at C_{B1} and C_{B2}. Using the capacitance calculated from (6.16):

$$C_{GateVCC} = 10 * C_{B1,max,actual} = 10 * 1.98\mu F = 19.8\mu F$$

The cheapest way to achieve this minimum requirement was to parallel three 10µF capacitors.

$$C_{min,3x10\mu F} = 3 * 10 * .9 * .85 = 22.95\mu F$$

6.3.12 Remaining Components

The remaining components in the circuit are filter and control circuitry components whose values are given in the datasheet. No calculations were performed for these components.

6.4 Regulators and Limiters

The LT8705 has regulation and limiting features that simply the Level 0 Block Diagram design. The introduction indicated previous projects required current limiting external to the DC-DC converter the students had built. Using the internal limiting of the LT8705 allows us to eliminate this component of the system. This decreases size, and increases efficiency of the system.

6.4.1 Output Voltage Regulator

Regulates the output to a specified voltage using a resistive divider network. Large resistors consume less power when constant voltage is applied across them according to Ohm's Law.

$$V_{out} = 1.207V * \left(1 + \frac{R_{FBOUT1}}{R_{FBOUT2}}\right)$$

$$\boldsymbol{R_{FBOUT2} = 20k\Omega \rightarrow \ R_{FBOUT1} = 576.6k\Omega}$$

6.4.2 Input Voltage Regulator

If the source has high output impedance and large current pull causes it to drop below a specified setpoint, the input voltage regulator will stop switching activity to limit the voltage drop. **This is not accompanied by a soft-start.

$$V_{in,min} = 1.205V * \left(1 + \frac{R_{FBIN1}}{R_{FBIN2}}\right)$$

$$\boldsymbol{R_{FBIN2} = 20k\Omega \rightarrow \ R_{FBIN1} = 62k\Omega}$$

6.4.3 Input/Output Current Monitoring

These sensors prevent the LT8705 from drawing too much power. They limit the current pull beyond a set point. The maximum output current was calculated in (6.6) earlier, the same process is applied to the input current.

$$P_{IN,MAX,LT8705} = 300W = V_{IN,MAX} * I_{in,limit}$$

$$\boldsymbol{I_{in,limit}} = \frac{300}{65} = 4.615A \rightarrow \boldsymbol{4.61A}$$

$$\boldsymbol{I_{out,max,average}} = \frac{P_{out,max}}{V_{out}} = \frac{215}{36} = 5.97A \approx \boldsymbol{6A}$$

R_{IMON_IN} and R_{IMON_OUT} use the same equation for calculating their sizes, they differ in their limits. Calculate them as follows:

$$\boldsymbol{R_{IMON\_IN}} = \left(\frac{1.208}{I_{in,limit} * 1m\left(\frac{A}{V}\right) * R_{SENSE}}\right)\Omega = \frac{1.208}{4.61 * .001 * .001} = \boldsymbol{262.6k\Omega}$$

$$\boldsymbol{R_{IMON\_OUT}} = \left(\frac{1.208}{I_{out,max,average} * 1m\left(\frac{A}{V}\right) * R_{SENSE}}\right)\Omega = \frac{1.208}{6 * .001 * .001} = \boldsymbol{201.3k\Omega}$$

$C_{IMON\_IN,\ IMON\_OUT}$ can be any value between 0.1µF to 1µF. 1µF was chosen in our design.

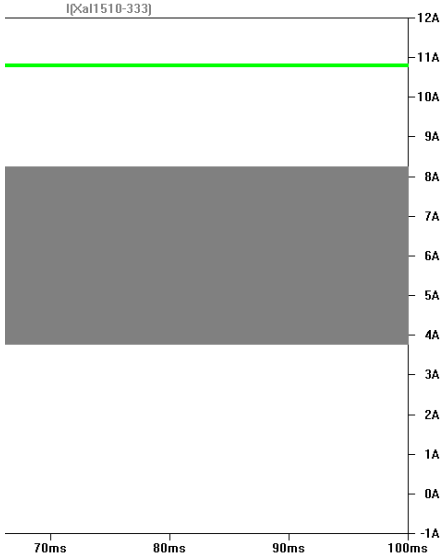

Figure 6.4.1 Limited Inductor Current (Gray)

Figure 6.4.1 shows successful current limiting of the device because at 65V in the output current naturally wants to be 11.8A according to I_{out} = 422.5W/36V. Figure 6.4.1 shows that the current ripples between 8.3 and 3.8A, producing ΔI_L=8.3-3.8=4.5A; less than calculated in Equation 6.9.

6.4.4 Estimated Efficiency

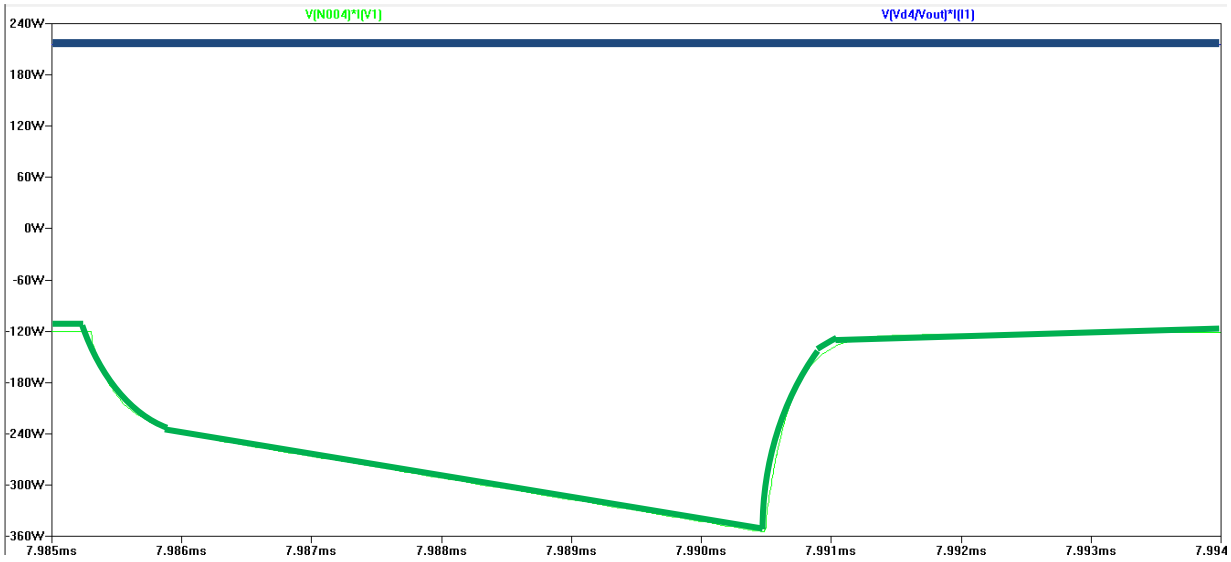

Figure 6.4.2 Power In (Green) and Out (Blue)

$$P_{in,Fig.6.4.2} = 221.5W$$
$$P_{out,Fig.6.4.2} = 215.84W$$
$$\boldsymbol{\eta = \frac{P_{out}}{P_{in}} = \frac{215.84}{221.5} = 97.4\%}$$

Simulations of Figure 6.4.2 estimate 97.4% efficiency. This means our circuit rides the border of peak efficiency of the LT8705, 98%, guaranteed by Linear Technology, its manufacturer [12]. Implementation of the actual circuit may still have better or worse efficiency than this. The component parasitics used in the simulation lean toward the higher ends of the parasitic ratings in the components' respective datasheets, however, simulations can't account for all of the parastics that occur in implementation, and don't account for thermal events.

6.4.5 Unresolved Issues

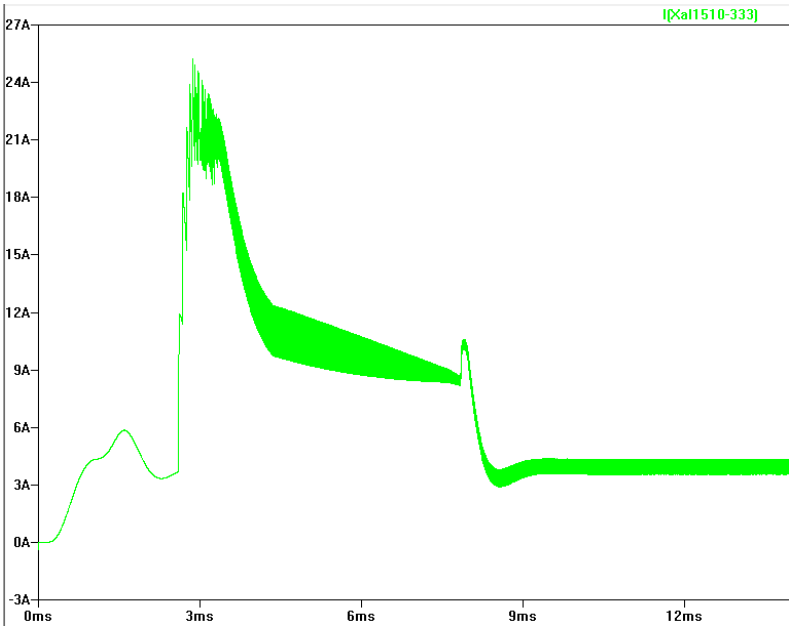

Figure 6.4.3 26A Peak Inductor Current

Despite the successful current limiting seen in Figures 6.3.6, 6.4.1, and 6.4.3, these Figures illustrate potential problems with the current draw through the inductor, and power dissipated through the FETs during start-up. Also, the RMS current through the input/output caps pushes each of their maximum ratings. These are most likely simulation errors and we will attempt to account for them. We also need to simulate the circuit using an approximate elliptical trainer source.

6.5 Design Four:

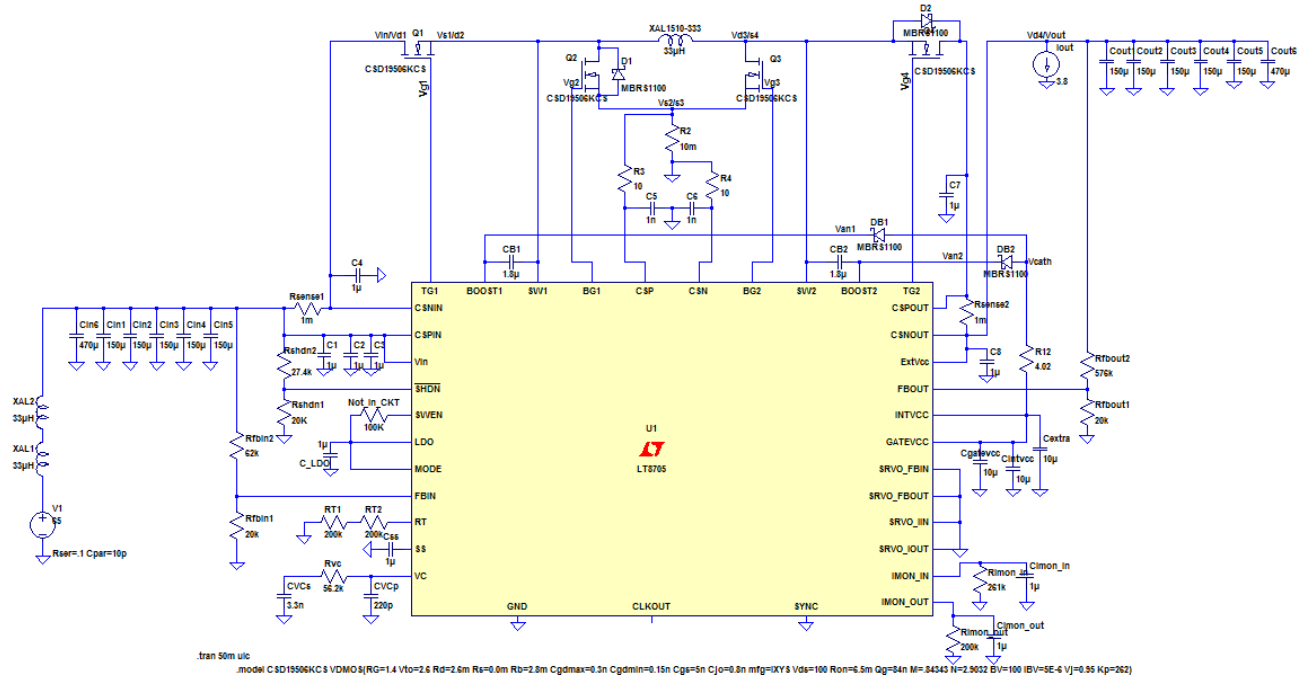

Figure 6.5.1 Final Schematic, November 2014

The final design, Figure 6.5.1, resolved all previously unresolved issues, except for the input spikes into the input capacitors on their initial charge. The 26A peaks during start-up were reduced to <12A, verified in Figure 6.5.2, by increasing C_{SS} to 1µF for the simulation. This made the simulation take a VERY long time. The .raw file contains 12GB of data.

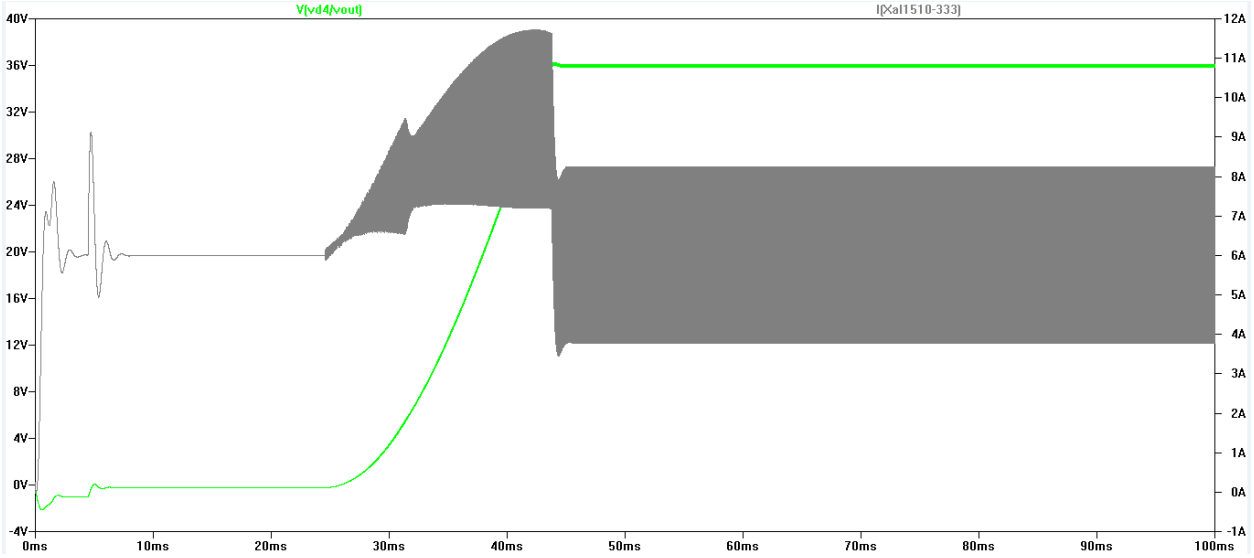

Figure 6.5.2 Simulation using appropriate C_{SS} Value. Peak current greatly reduced.

Extra room was available on the board during layout so an additional 470µF was placed on the input and output sides, increasing the RMS capacity of the input and output caps to 3.9A each, giving them 0.9A buffering from their maximum ratings, found using Equation 6.11.

In addition to increasing the current carrying capabilities of the input/output capacitors and obtaining an exact peak current during start-up a simulation was performed using elliptical data as the source.

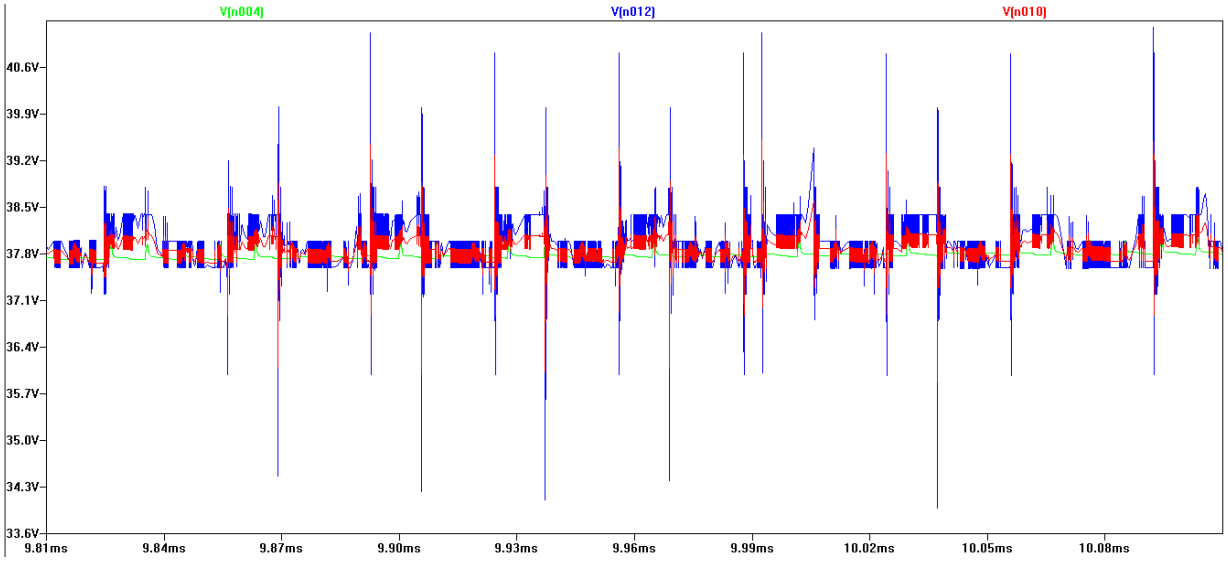

Figure 6.5.3 Elliptical Input (blue), Partially Filtered Input (red), Input Cap Voltage (green)

Figure 6.5.3 shows the elliptical trainer data given to us by Professor Braun from [2]. The high dV/dt spikes would blow our input capacitors according to the equation i_c=C*dV/dt. dV/dt measured to 9GV/s at some points, producing hundreds of amps of current. Adding the two inductors between the source and our circuit easily solved this problem. Figure 6.5.4 shows the beautiful 470µF current waveform; the one with the greatest potential current pull.

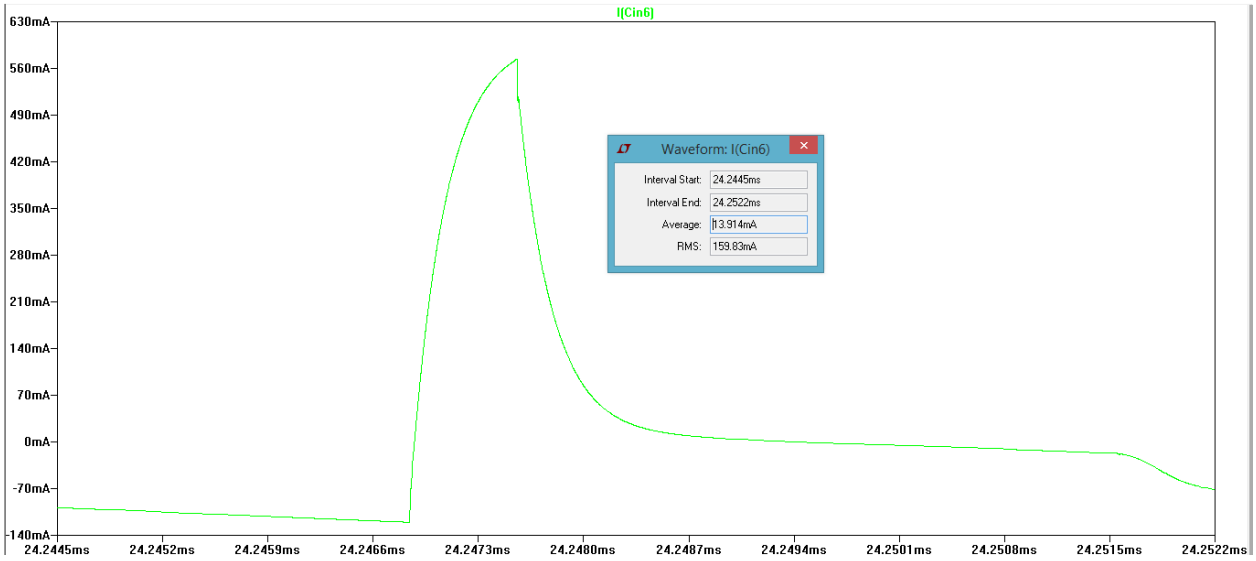

Figure 6.5.4 Input Capacitor Current Waveform with Filtered Elliptical Input

The datasheet of the capacitor rates the RMS current at 917mA [29]. Its simulated value is 159mA, not even close.

6.5.1 Remaining Challenges

We could not get a simulation to run when ramping the voltage source slowly while attempting to eliminate the large surge currents during turn-on for the input capacitors. In actual implementation the runner's speed should be decreased very slowly. Our heatsinks may be too small, and an overlooked potential problem may even be present during start-up. The circuit indicates it needs ~12A during start-up, but according to [2] we will only be able to pull out 6.5A max. We predict this won't be a problem because the input voltage regulator will stop switching activity if the source is pulled too hard [12].

7 PCB Layout

The PCB design process involves the design of the LT8705, packages, traces, vias, copper, and ground layers. The Eagle (EASILY APPLICABLE GRAPHICAL LAYOUT EDITOR) PCB design software was chosen to carry out the layout [19]. Creating a sufficient board first involved designing a schematic with the correct packages in place for our components. The packages for each component were carefully chosen using their corresponding datasheets. The schematics were designed using Figure 6.5.1. Table 7.1 lists the components and packages used in the PCB design.

Table 7.1 List of components, schematic number, part number, and packages used in PCB design

Component	Schematic Number	Part Number	Package
LT8705EFE	U1	LT8705EFE#PBF	CUSTOM
LT8705EUHF	U1	LT8705EUHF#PBF	CUSTOM
CSD19506KCS	Q1	CSD19506KCS	TO220
	Q2		TO220
	Q3		TO220
	Q4		TO220
CSD19505KCS	Q1,Q2,Q3,Q4	CSD19505KCS	TO220
MBRS1100	DB1	MBRS1100	SMB
	DB2	MBRS1101	SMB
	D1 (optional)	MBRS1102	SMB
	D2 (optional)	MBRS1103	SMB
33uH	L1	XAL1510-333	CUSTOM
150uF	Cin1,Cin2,Cin3,Cin4	EEVFK1K151Q	CUSTOM
	Cout1,Cout2,Cout3,Cout4		CUSTOM
1uF	Css	C3216X7R2A105M160AA	1206
	C1, C2, C3, C4	C3216X7R2A105M160AA	1206
	C7, C8	C3216X7R2A105M160AA	1206
	Cimon_in, Cimon_out	C3216X7R2A105M160AA	1206
	C_LDO	C3216X7R2A105M160AA	1206
10uF	Cintvcc	CL21B106KPQNNNE	0805
	Cgatevcc	CL21B106KPQNNNE	0805
	Cextra	CL21B106KPQNNNE	0805
1.8uF	CB1, CB2	C0805C185K4RACTU	0805

3.3nF	Cvc_s	0805YA332FAT2A	0805
1nF	C5	CL21B122KBANNNC	0805
	C6		0805
220pF	Cvc_p	C0603C271K5RACTU	0805
1mΩ	Rsense1,Rsense2	CSNL1206FT1L00	1206
4.02Ω	R1	CRCW12064R02FKEA	1206
10mΩ	R2	ERJ-8BWFR010V	1206
10Ω	R3,R4	RK73H2BTTD10R0F	1206
20kΩ	Rshdn2	WK73R2HTTE2002F	1020
	Rfbin2		1020
	Rfbout2		1020
27.4kΩ	Rshdn1	ERJ-3EKF2742V	0603
56.2kΩ	Rvc	CRCW251256K2FKEG	2512
62kΩ	Rfbin1	ERJ-6ENF6202V	0805
576kΩ	Rfbout1	P576KDACT-ND	0805
261kΩ	Rimon_in	ERJ-3EKF2613V	0603
200kΩ	Rimon_out	P200KHCT-ND	0603
	RT1, RT2		0603

Component ratings are important when designing a PCB board layout. Ratings help with component placement and trace widths. Table 7.2 lists each component and its max ratings.

Table 7.2 List of component ratings measured through Ltspice simulations in buck mode (max ratings)

Schematic Number	**Vp (V)**	**Vrms (V)**	**Vave (V)**	**Ip (A)**	**Irms (A)**	**Iave (A)**	**Power (W)**
Q1	65			30	4.58	3.2	0.7
Q2	65			30	4.24	2.74	0.295
Q3	36			30	0	0	0
Q4	36			30	6.25	5.96	0.145
DB1	-65	51.5	-40	2.0	45m	4.8m	3.35E-03
DB2	-40	-35.5	-35.5	1.8	2.7m	0.2m	6.91E-06
L1	65	31.9	4.8	32, 8.25 repetitive	6.02	6	1.25E+01
Cin1,Cin2,Cin3,Cin4	65	0	65	100	498.5m	43.1m	3.20E-03
Cout1,Cout2,Cout3,Cout4	38	0.2	35.6	31	412.6m	19.9m	3.20E-03
Css							
C1, C2, C3, C4	65, 65	65, 65	65, 65	1.2, 1.2	307.8m, 316.3m	3.47m, 3.53m	2.54E-03
C7, C8	36, 36	36, 36	36, 36	.9, .9	97.5m, 98.5m	7.09m, 7.15m	8.20E-02

Cimon_in, Cimon_out	3	3	17.5m, 48.7m	10u, 10u	0, 0	0,0	0
C_LDO	3.3	3.3	3.3	0	0	0	0
Cintvcc	2.5, 6.3	0, 0	2.5, 6.3	0, 1.2	0, 77m	0, 0	0.001
Cgatevcc							
Cextra							
CB1, CB2	-7, 6.7	-7, 6	-7, 6	2.5 repetitive	85m, 2.67m	0, 0	6.00E-04
Cvc_s	1.3	1.3	1.3	88n	73.906n	0	0
C5	0	0	0	0	0	0	0
C6	270m	47.331m	-30.74m	7.5m	254.86µ	-1.1488µ	0
Cvc_p	1.31	1.3048	1.3048	0	0	0	0
Rsense1,Rsense2	65,1	1,1	1,1	25, 25	4.61, 6.27	3.21, 5.96	0.0605
R1	4	0.2	0.02	1	50m	5m	1.00E-02
R2	1	1	1	9	4.3	2.74	1.80E-01
R3,R4	1	1	1	25m	5m	5m	0.016
Rshdn2	27.5	27.5	27.5	1.3m	1.3m	1.3m	0.033
Rfbin2	15.7	15.7	15.7	1m	1m	1m	0.0123
Rfbout2	1.207	1.207	1.207	0.1m	0.1m	0.1m	7.20E-05
Rshdn1	37.5	37.5	37.5	1m	1m	1m	0.044
Rvc	3	1.4	1.4	5u	5u	5u	1.00E-05
Rfbin1	49.3	49.3	49.3	0.7m	0.7m	0.7m	0.033
Rfbout1	40	35	35	60u	60u	60u	2.08E-03
Rimon_in	3	1.208	1.208	60u	60u	60u	0
Rimon_out	3	1.208	1.208	60u	60u	60u	0

7.1 First Revision

The first draft of the schematic and board layout involved familiarizing ourselves with the software and its capabilities. The initial 2-layer design included several shortcomings (see Figure 7.1.1, 7.1.2). First, the feedback in and out resistors were designed to be potentiometers so that the exact output voltage could be achieved by manually varying the resistances. Although this design does work, these potentiometers take up much more space than regular packaged resistors. In addition, having an approximate resistance near the one calculated would only cause slight voltage changes in the millivolt range. Second, the components in the PCB board design were placed too far from the LT8705 controller causing long trace paths which accumulate inductance. This includes the sense resistor and power MOSFETs. The LT8705 datasheet suggests the power MOSFETs be as close to the microcontroller as possible, including the sense resistors [12]. For these reasons, a second design required the datasheet suggestion be met.

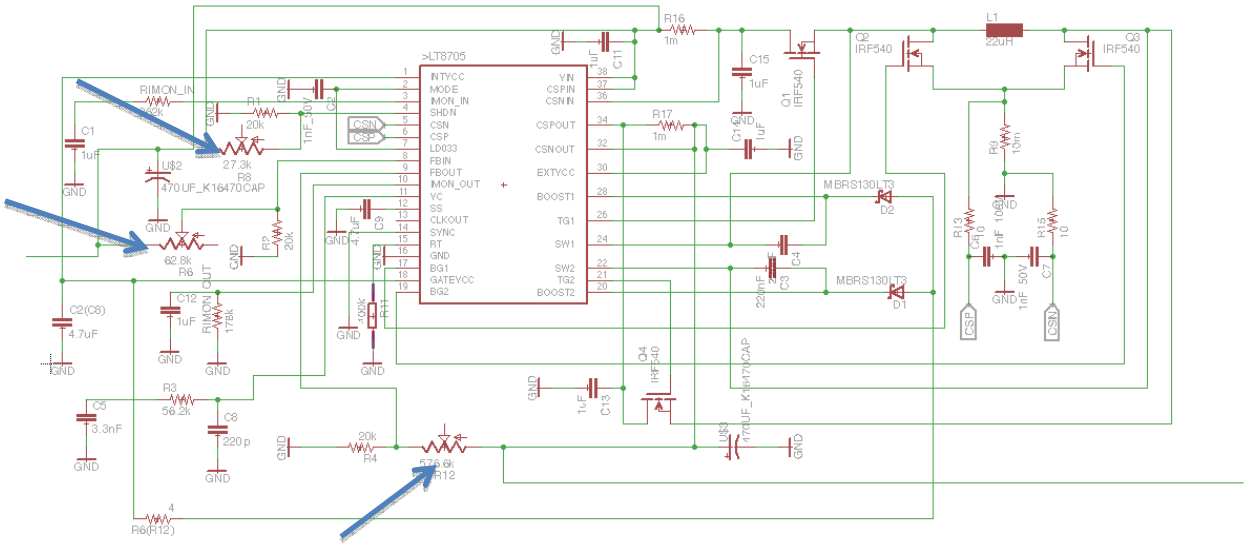

Figure 7.1.1: First revision EAGLE schematic

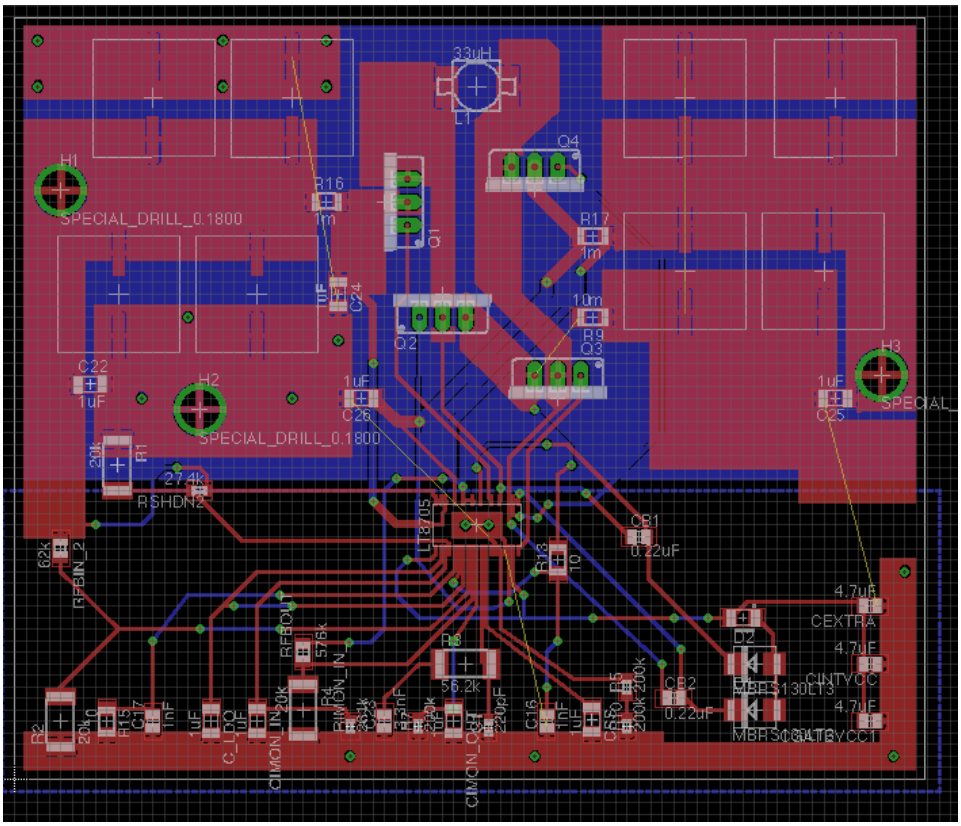

Figure 7.1.2 First revision PCB board layout

7.2 Second Revision

The second iteration of the 2-layer PCB and EAGLE schematic design involved adding more input and output capacitors, a bigger inductor, and moving the power MOSFETs closer to the DC-DC converter (see Figure 7.2.1, 7.2.2). In addition, 4.7uF capacitors were added to the gate pins of the controller. Adding more input and output capacitors helps reduce ripple voltage, and in turn reduces rms ripple current. The more capacitance at the input and output of this PCB design, the better. A bigger inductor helps reduce current change with respect to time. A 33uH inductor improved the current ripple, and limited the current to a value where adjacent components in the power path were in safe operating regions. Moreover, placing power MOSFETs Q2 and Q3 closer to the controller helps with the efficiency and switching [12]. The LT8705 datasheet suggests Q2 and Q3 be as close to the controller as possible. Moving these MOSFETs closer to the controller means changing trace and component placement. Adding capacitors to the gate pins helps reduce voltage at these pins and increases efficiency of the overall design.

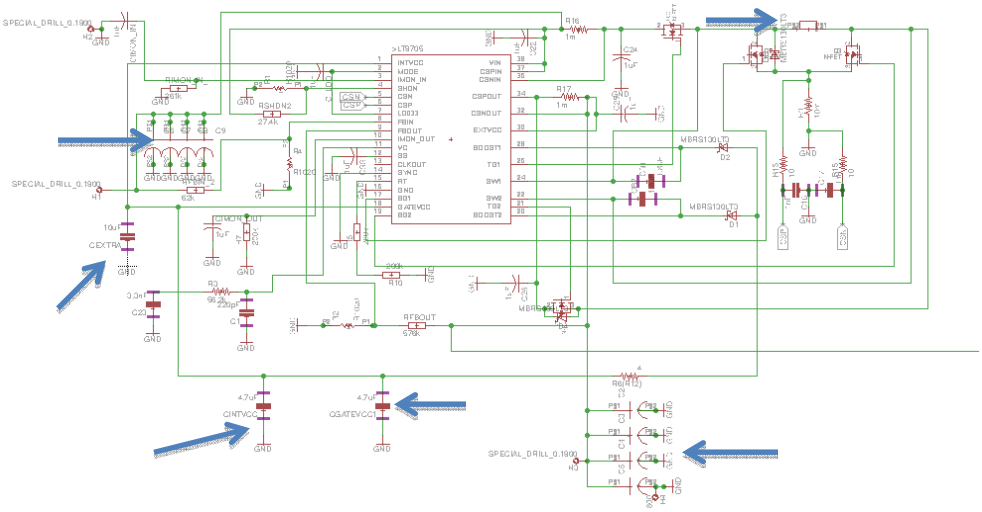

Figure 7.2.1 Second revision EAGLE schematic

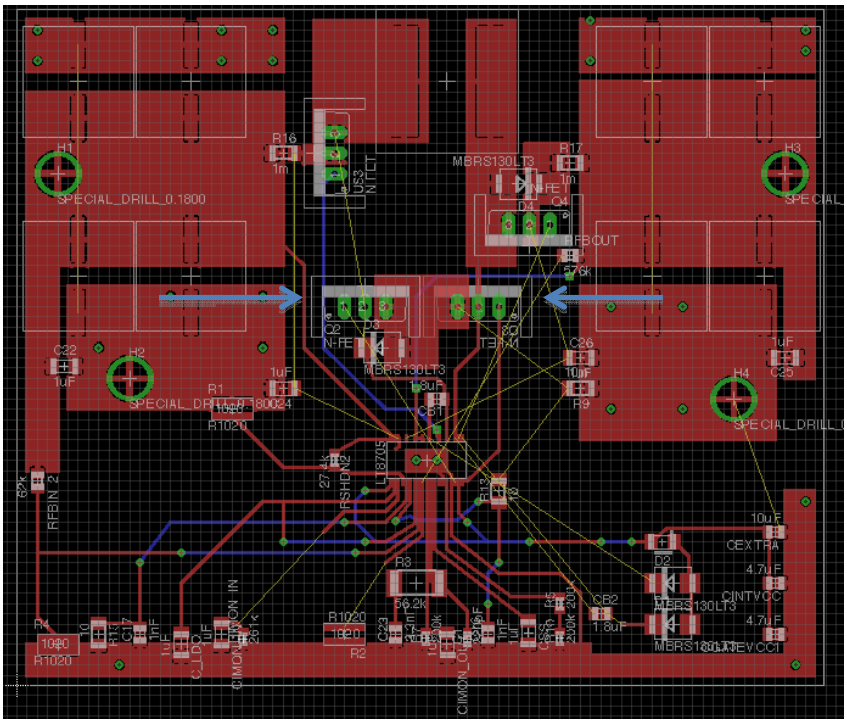

Figure 7.2.2 Second revision PCB board layout

7.3 Third Revision

The third iteration of the PCB design had drastic changes. The previous designs had a 2-layer board consisting of a top layer and bottom ground layer. However, the LT8705 datasheet states to not have any traces in the ground layer [12]. Therefore, a new 4-layer design creates a bottom ground layer and three other layers for trace design (see Figure 7.3.1, 7.3.2). A multilayer board provides heat sinking for power components [12]. This also gave us the opportunity to start over and place components closer to the controller allowing for shorter traces and a symmetrical design. The main purpose of the new design was not only bringing components closer, but to shorten the power path as well. This design also includes the same component names that the final schematic Ltspice design contains. Having the same component names makes it easy to find components and test them. The 4-layer design was not finished because traces were placed on the second layer. The LT8705 datasheet suggests the layer with the power MOSFETs (layer 1) be closest to the ground layer. Therefore, components had to be moved so that traces could be only placed on layers 1 and 3.

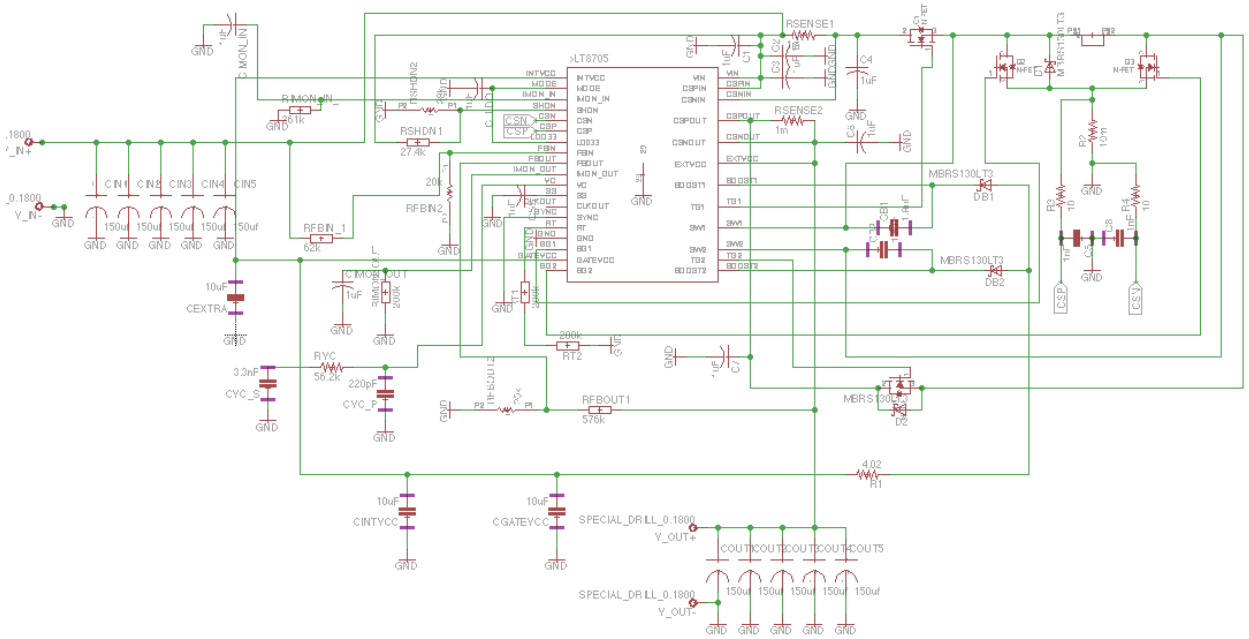

Figure 7.3.1 Third revision EAGLE schematic

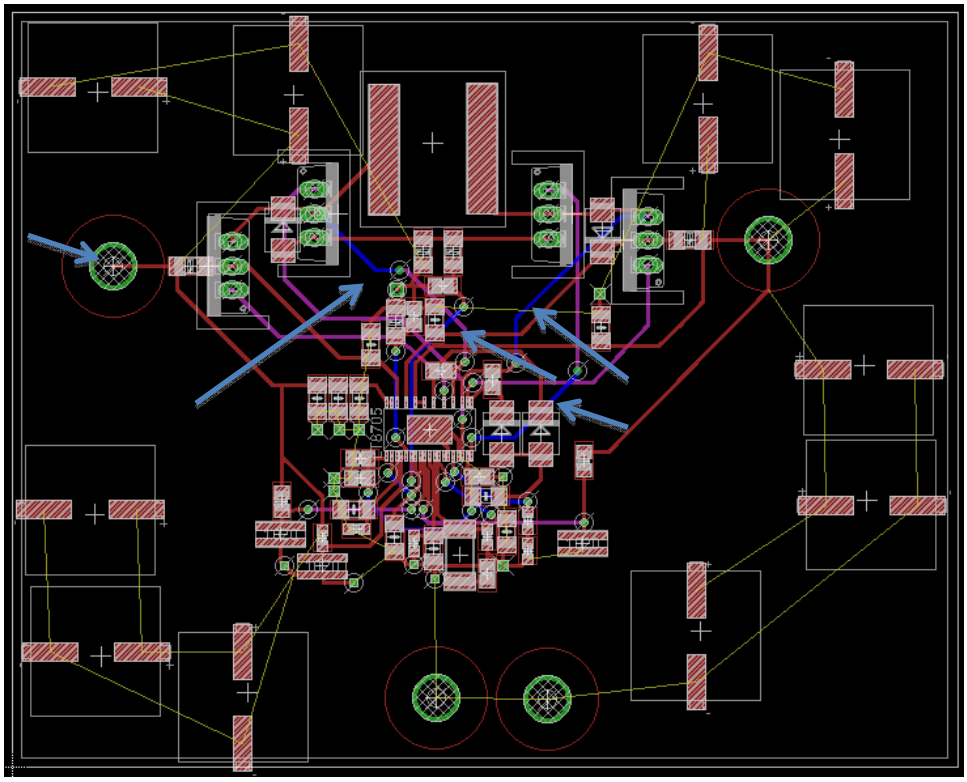

Figure 7.3.2 Third revision PCB board layout

7.4 Fourth Revision

The fourth iteration of the 4-layer PCB design involved adding more input and output capacitors, a total of two ground layers, and shorter power path (see Figure 7.4.1, 7.4.2). Since components were placed close together and near the IC, this gave more room for the addition of more input and output capacitors. The capacitors were not wired in this design so that placement could be flexible. The power path was not filled with copper at this point because trace width and length were still being discussed. All trace widths not in the power path had a width of 12 mils. All vias were set to have a diameter of 14 mils. Two different vias (square for ground and octagonal for trace layers) helped send traces to the ground layers (layers 2 and 4) or to the other trace layers (layers 1 and 3). The addition of a second inductor was discussed, but the proposition was excluded to save cost and soldering space.

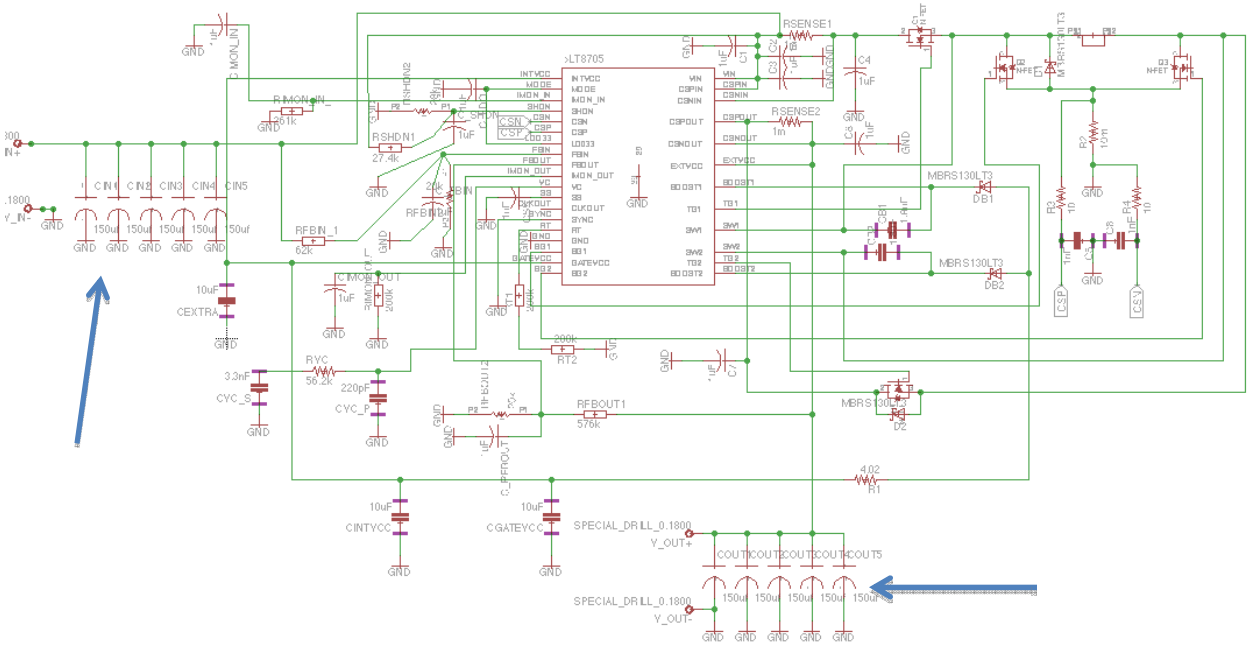

Figure 7.4.1 Fourth revision EAGLE schematic

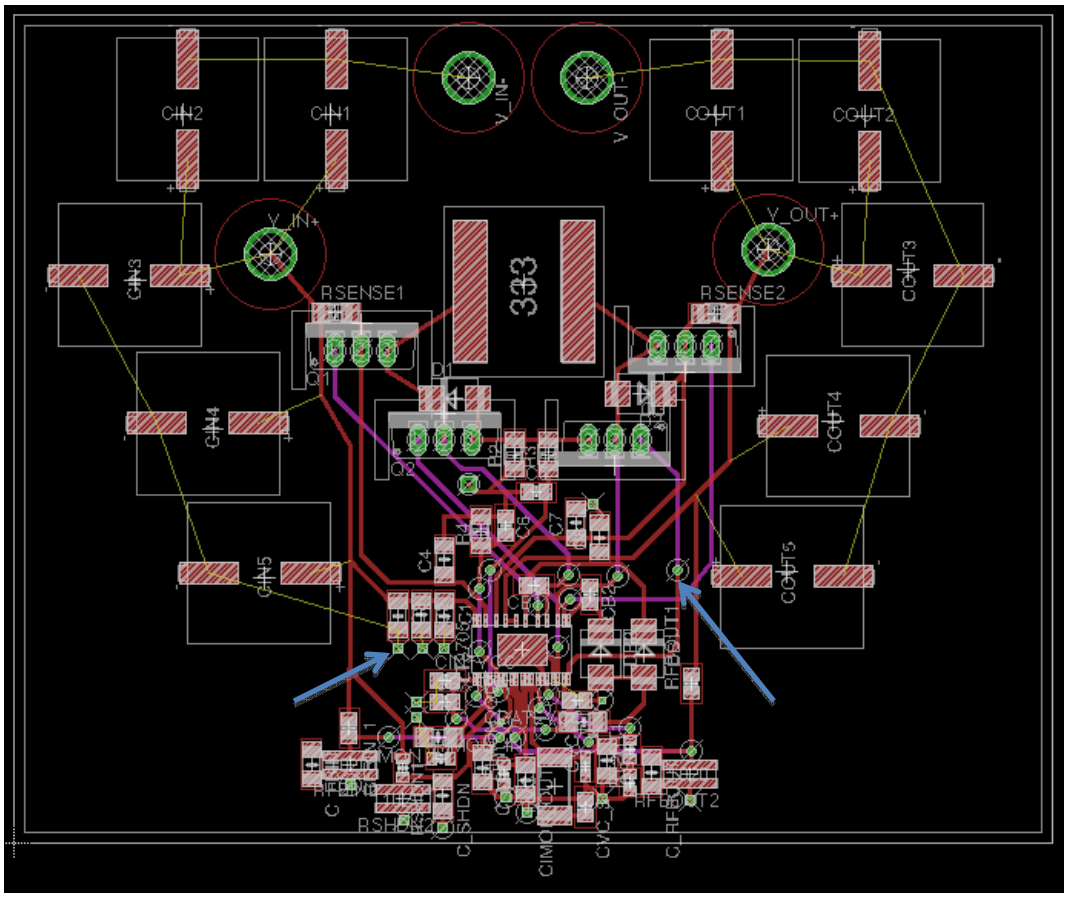

Figure 7.4.2 Fourth revision PCB board layout

7.5 Fifth Revision

The fifth iteration of the 4-layer PCB board design contains properly spaced input and output capacitors, copper filled power path, and wider traces for high current change paths (see Figure 7.5.1, 7.5.2). All square vias send traces to ground, while octagonal vias send traces to another trace layer. Multiple vias were placed on power components per LT8705 datasheet [12]. The red color on the PCB board is the copper filled top layer. The third layer consists of the purple traces. Ground layers were turned off in screenshots so the components and traces could be visible. The capacitors were spaced outwards to allow for test points and soldering small packages. The power path in this design is short and wide. The small signal ground covers the bottom half of the PCB board while the power ground covers the top half.

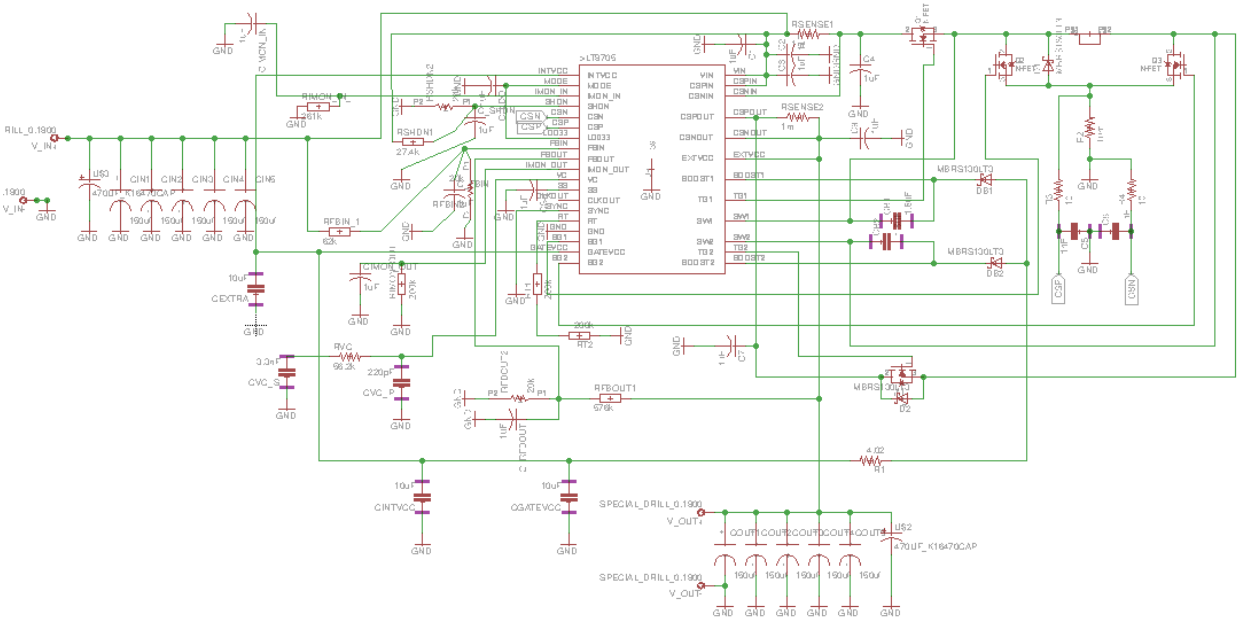

Figure 7.5.1 Fifth revision EAGLE schematic

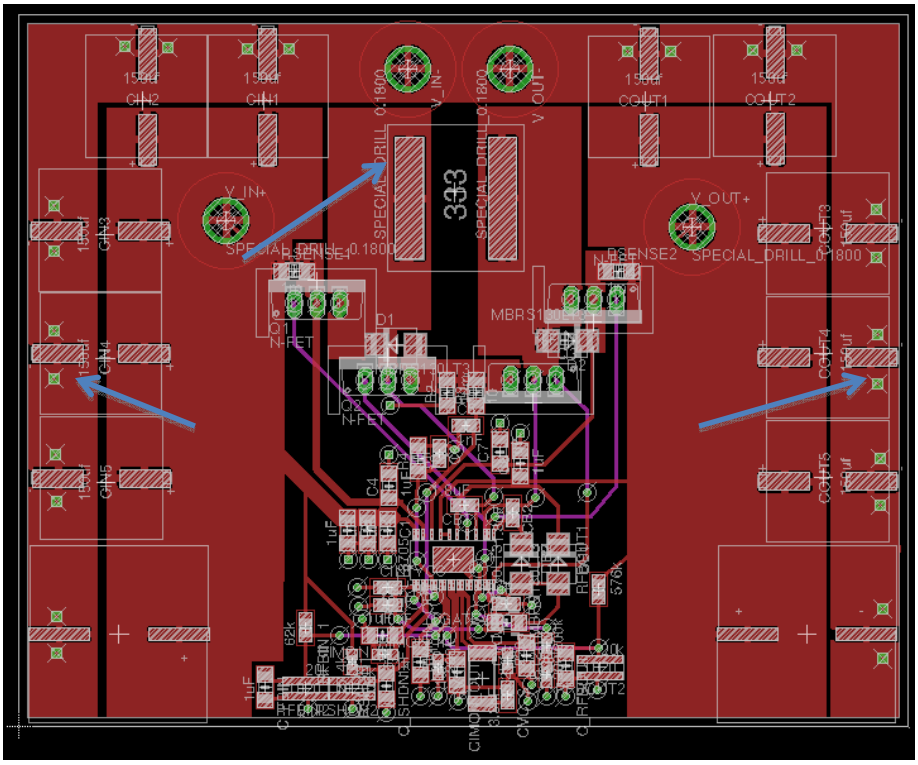

Figure 7.5.2 Fifth revision PCB board layout

7.6 Sixth Revision

The sixth and final iteration of the 4-layer PCB board design includes the partitions ground planes, widened power MOSFET traces, and cleaned silkscreen (see Figure 7.6.1, 7.6.2). Much like the fifth iteration, the small signal (digital) ground covers the bottom half of the board, and the power ground covers the top half. Both ground planes cross at one single point. The MOSFET traces were widened to accommodate the higher current peaks and protection of components. The largest possible trace width without moving components was used. One of the main changes in this design involved the silkscreen. Removing the values of each component from the PCB board helps us easily locate component names when soldering (see Figure 7.6.2). The component names were placed and sized so soldering could be efficient. Although the datasheet states not to have traces in parallel, board size limitations caused some parallel traces which may bring down the measured simulation efficiency.

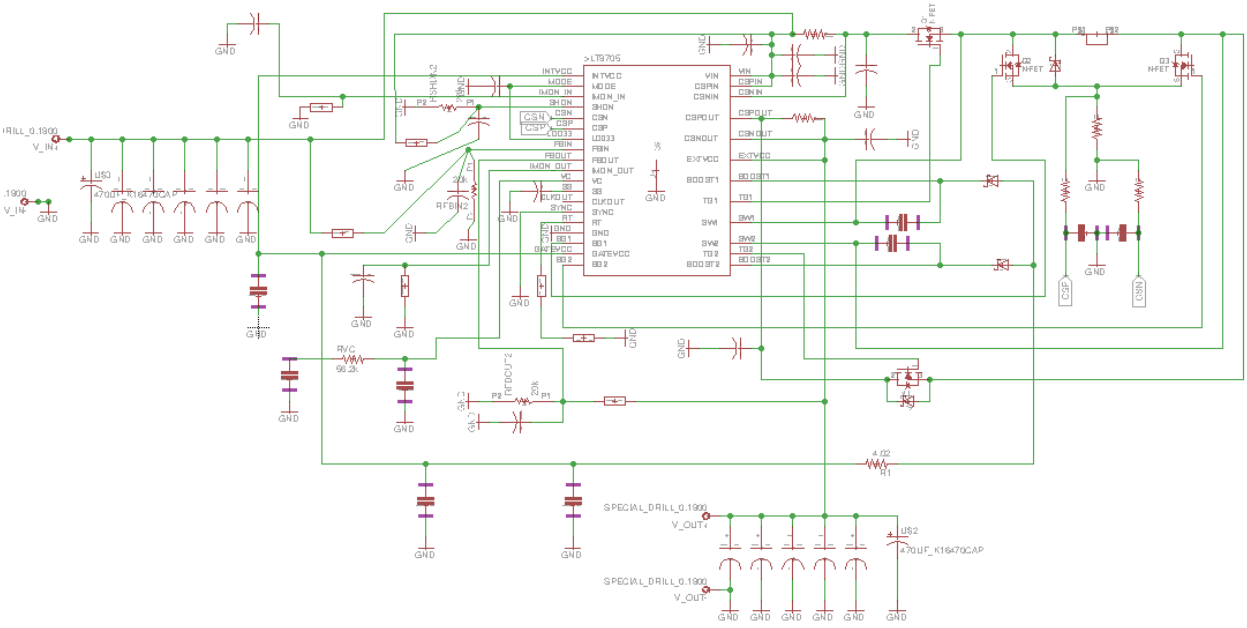

Figure 7.6.1 Sixth revision EAGLE schematic

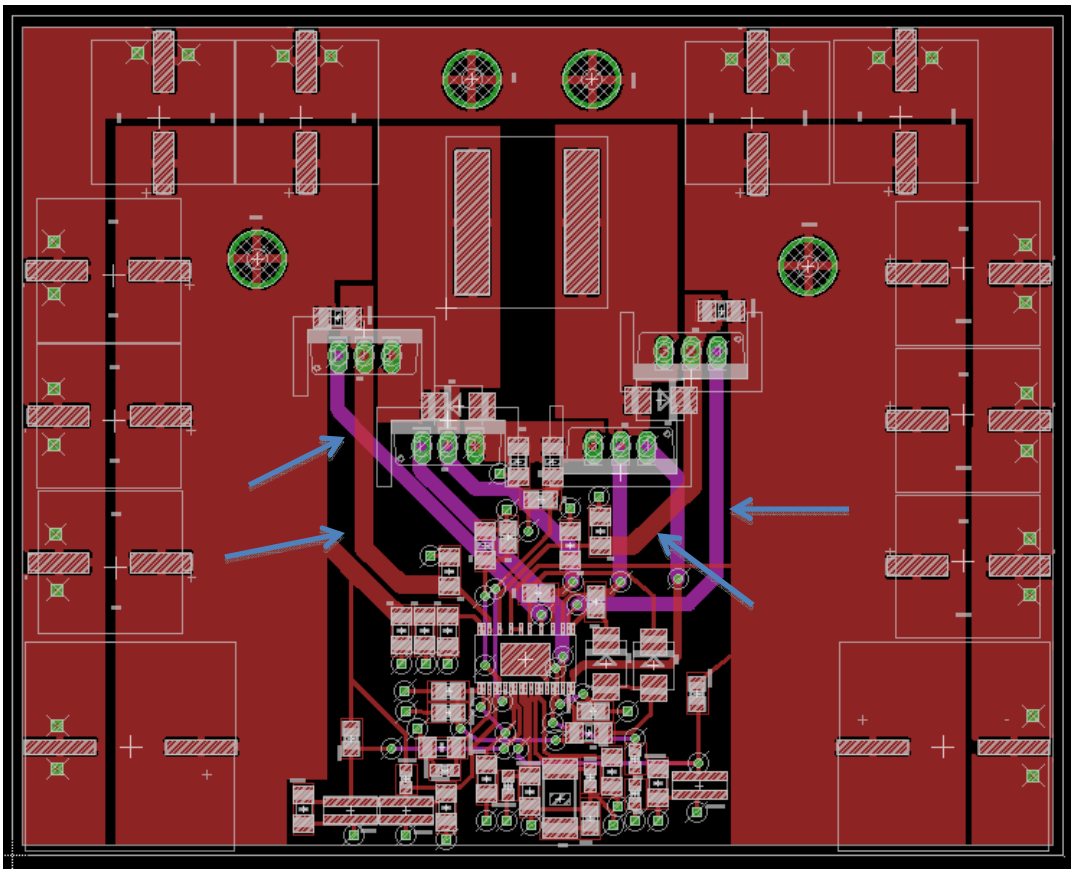

Figure 7.6.2 Sixth revision PCB board layout

7.7 Final Revision

The seventh iteration of the PCB board layout consists of changes to the PCB board layout only. We used the schematic from the sixth iteration. The major changes include adding bigger heat sinks to Q1 and Q5 (switch 4). These power MOSFETs have large amounts of power and therefore higher temperatures. The larger heat sinks help vent the MOSFETs at a better rate than the smaller heat sinks used on Q2 and Q3. This included moving Q1 and Q5 in a vertical orientation so that the larger heat sinks did not interfere with other components (see Figure 7.7.1). Once we added the heat sinks, the LT8705 datasheet [12] says to fill empty area with as much copper as possible. We added copper ground to the digital component's ground (bottom half of board) and a larger power path to accommodate the datasheet suggestion. The final PCB board layout can be seen on Figure 7.7.2.

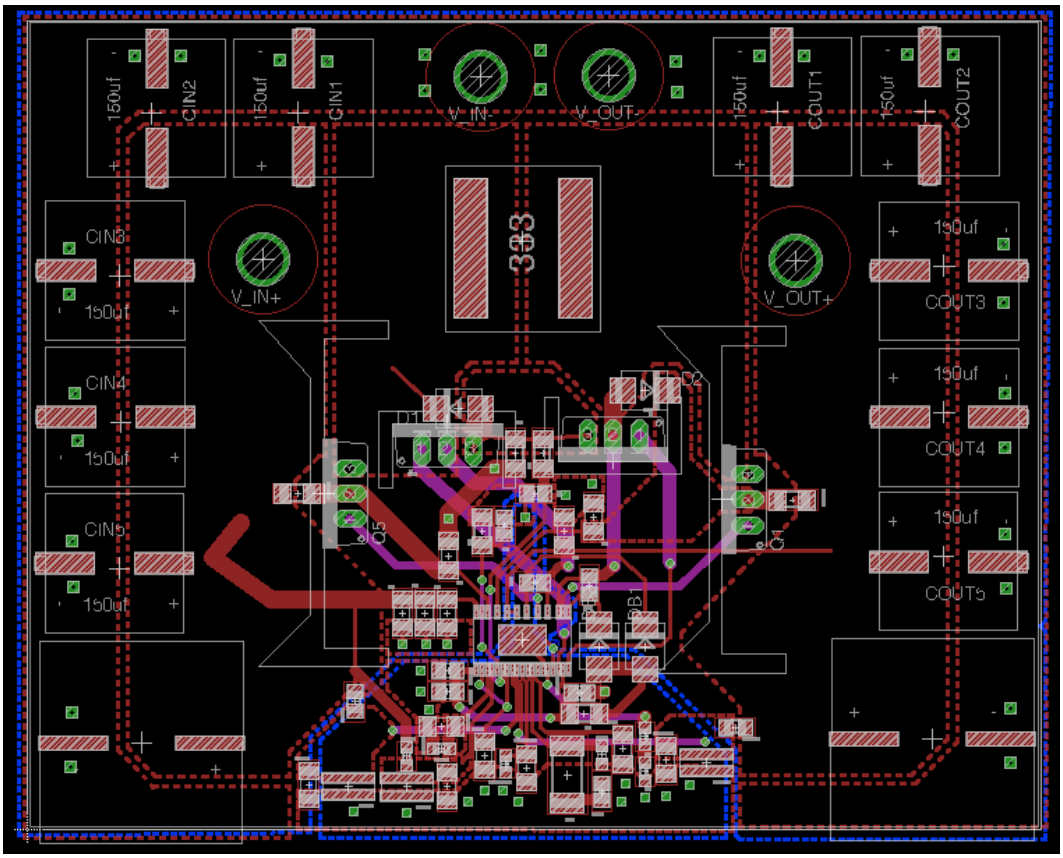

Figure 7.7.1 Final revision PCB board layout

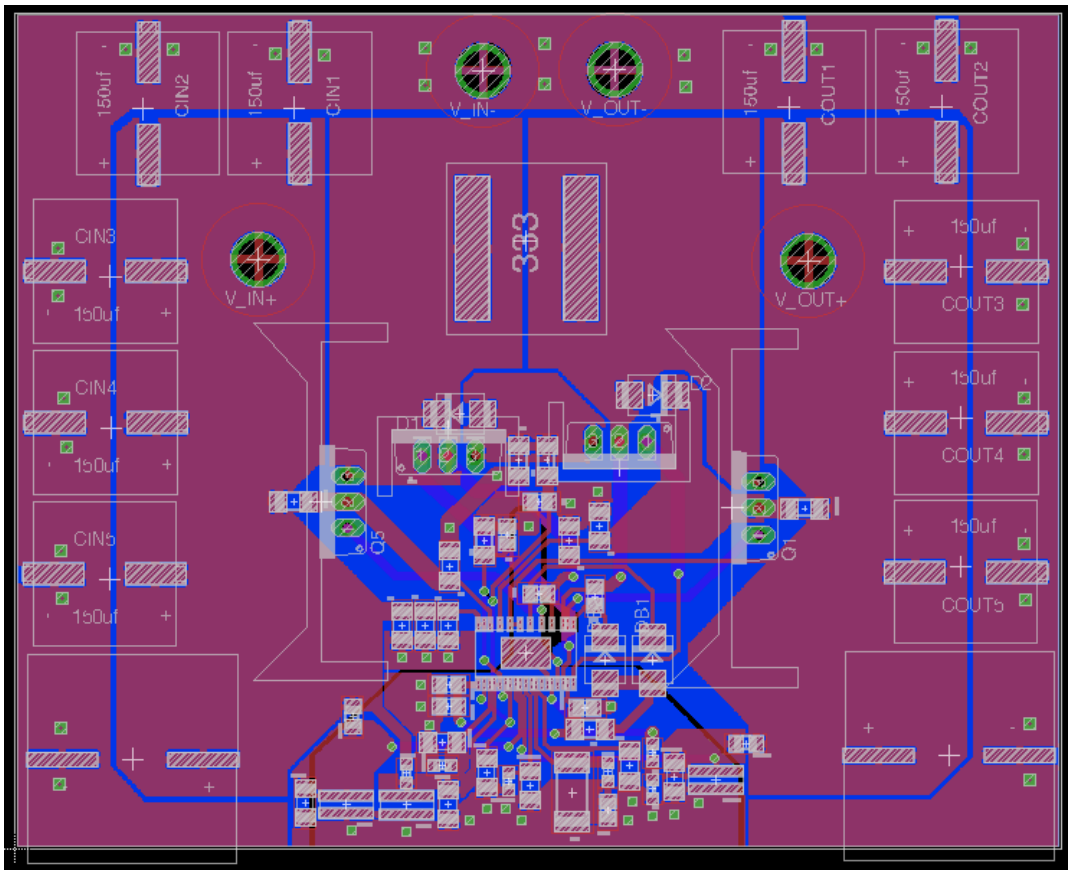

Figure 7.7.2 Final PCB board layout used for fabrication

LT8705 suggested PCB design Checklist [12]

- The ground plane layer should not have any traces and be as close as possible to the layer with the power MOSFETs
- The high current change path formed by switch Q1, Q2, D1, Rsense, Cin capacitors, Q3, Q4, D2, and Cout capacitors should be compact with short leads and PC trace lengths.
- Avoid running signal traces parallel to the traces that carry high current change because they can receive inductively coupled voltage noise (SW1, SW2, TG1, and TG2).
- Use immediate vias to connect components to the ground plane. Use several vias for each power component.
- Flood all unused areas in all layers with copper. Flooding with copper will reduce temperature rise of power components.
- Partition the power ground from the signal ground. The small-signal component grounds should not return to the IC GND through the power ground path.
- Place switch Q2 and Q3 as close to the controller as possible, keeping GND, BG, and SW traces short.
- Minimize inductance from the sources Q2 and Q3 to Rsense by making the traces short and wide.
- The output capacitor (-) terminals should be connected as closely as possible to the (-) terminals of the input capacitor.

- Connect the input capacitors, Cin, and output capacitors, Cout, closely to the power MOSFETs. These capacitors carry the MOSFET AC current in the boost and buck regions.
- Connect the FBout and FBin pin resistor dividers to the (+) terminals of Cout and Cin, respectively.
- Route current sense traces (CSP/CSN, CSPIN/CSNIN, CSPOUT/CSNOUT) together with minimum PC trace spacing.
- Connect the Vc pin compensation network closely to the IC, between Vc and the signal ground pins. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.
- Connect the INTVcc and GATEVcc bypass capacitors close to the IC. The capacitors carry the MOSFET drivers' current peaks.

8 PCB Manufacturer and Assembly

8.1 Manufacturer

CadSoft EAGLE does not have in-house manufacturing available; an external board house must be employed to manufacture the PCB. The time constraints of this project rule out the less expensive option of overseas manufacturing. Extensive research uncovered Pentalogix, a trusted board house in Portland, Oregon that guarantees shipping date. Pentalogix meets all minimum specs of the LT8705 buck-boost converter board; 4 layers, 12mil traces, 6mil trace spacing, 1 oz. copper, solder mask and stencil.

Some of the Pentalogix requirements/features for fabrication [21]:

- 0.062" Thick
- Minimum line and space = 0.005"
- Minimum finished drill size = 0.008"
- Maximum finished drill size = 0.350"
- Green SolderMask both sides.
- White SilkScreen Top, Bottom or Both
- Tin/Lead HASL or Immersion Silver (ROHS) finish plating
- Electrical test included
- Irregular board shape
- Internal cutouts
- Electrical test comes included with all multi-layer (4-8 layers) boards.

8.2 Solder Paste

EHFEM's products should comply with RoHS. Use lead-free solder. The solder paste used for board assembly came from Cal Poly and whether the solder used in the construction of our board contains lead is unknown. Solder paste reflow temperatures should be less than the maximum temperature tolerances of circuit components; i.e. dielectric capacitors.

8.3 Assembly

A reflow oven most effectively solders the small pins of the LT8705. It's used for the most of the components on the PCB, aside from the MOSFETs, and banana plugs.

The stencil was laid down flat across the board and solder paste was applied to fill all component footprints, making sure that all pads are fully covered in paste. The stencil was removed and then the parts were individually placed on the board with fine, non-magnetic tweezers.

Place the IC first, then place the surrounding small components (0603,0805, etc.) second. Place the bigger capacitors last and it's ready for the reflow oven.

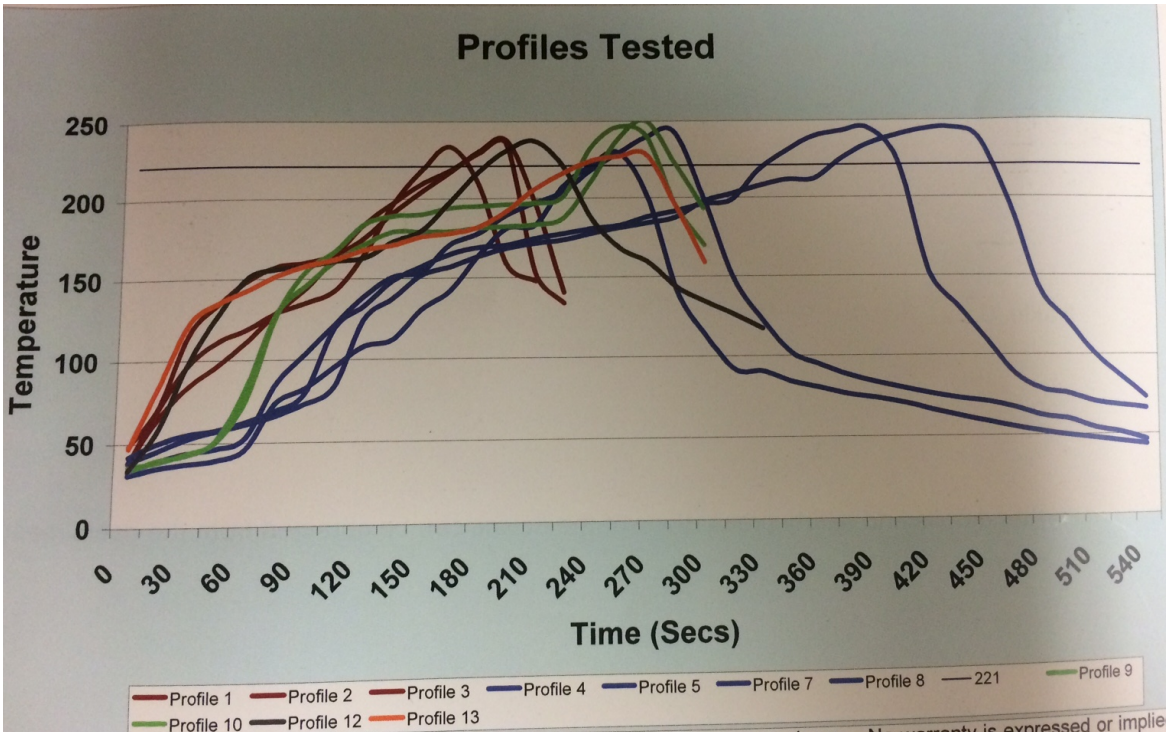

Figure 8.3.1 Pre-made Reflow Profiles from Cal Poly's Reflow Oven Located in the CPE Club Office

Normally solder profiles are built using information from the solder paste's manufacturer. We did not know this at the time and picked one of the profiles from the above list.

The first attempt to solder the board used the small board option. The solder for the large components did not properly fuse. Increasing the settings to medium resolved this issue. Attach the heat sinks to the MOSFETs and hand-solder them to the board. Figure 8.3.2 shows the completed board on the next page.

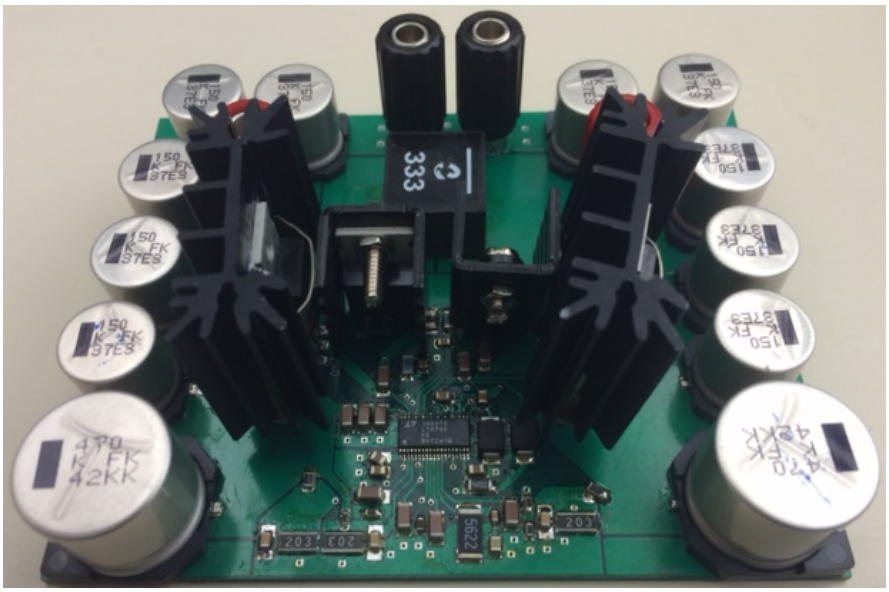

Figure 8.3.2 Final assembled PCB board

9 Testing

9.1 Equipment

- Digital Multimeter (DMM)
- Oscilliscope
- Electronic Load
- Power Source

9.2 Setup

Preliminary continuity checks verified Figure 8.1's connections. Do this using a DMM. This process helps prevent shorts. The test plan in Figure 9.1 shows which nodes were tested.

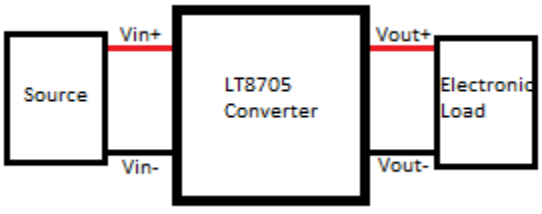

Figure 9.1 Test Setup Schematic

An electronic load[6] connects V_{OUT}^{+} and V_{OUT}^{-}. The tests for this circuit use the BK8540-ND[7] electronic loads available in the power lab, Room 104. Figure 9.3 shows a picture.

[6] An electronic load pulls a pre-determined amount of current from a circuit and conveniently displays the voltage across itself (and/or the power). Useful for simulating real loads.

Figure 9.2 Electronic Load Used for Testing

The manufacturer rates this device for 150W, so do NOT use it when testing powers greater than this value. The same constraints apply to the voltage source.

Connect V_{IN}^{+} and V_{IN}^{-} using the voltage source available at the desk. The voltage source's power ratings limit voltage limits of the test bench. Once again, DO NOT TEST POWERS GREATER THAN THE RATINGS OF EITHER THE SOURCE OR THE LOAD.

Some safety considerations help detour any unexpected injury. A plastic cover over the PCB board while increasing voltage helps against any capacitor explosions or fire. Figure 9.2 shows the plastic cover used to protect us from any issues.

[7] 150W Rating

Figure 9.3 Plastic Covering over Enclosed Circuit

9.3 Procedure

Determine the load current using the mathematical relations in 9.1 and 9.2. Table 9.1 summarizes input and output power relationships assuming 95% efficiency, 10Ω input resistance, and V_{OUT}=36V.

(9.1)

(9.2)

Table 9.1 Estimated V_{IN}:I_{OUT} Relations

V_{IN}	P_{IN}	P_{OUT}	I_{OUT}
5.000	2.500	2.375	0.066
6.000	3.600	3.420	0.095
7.000	4.900	4.655	0.129
8.000	6.400	6.080	0.169
9.000	8.100	7.695	0.214
10.000	10.000	9.500	0.264
11.000	12.100	11.495	0.319
12.000	14.400	13.680	0.380
13.000	16.900	16.055	0.446
14.000	19.600	18.620	0.517
15.000	22.500	21.375	0.594
16.000	25.600	24.320	0.676
17.000	28.900	27.455	0.763
18.000	32.400	30.780	0.855
19.000	36.100	34.295	0.953
20.000	40.000	38.000	1.056
21.000	44.100	41.895	1.164
22.000	48.400	45.980	1.277

23.000	52.900	50.255	1.396
24.000	57.600	54.720	1.520
25.000	62.500	59.375	1.649
26.000	67.600	64.220	1.784
27.000	72.900	69.255	1.924
28.000	78.400	74.480	2.069
29.000	84.100	79.895	2.219
30.000	90.000	85.500	2.375
31.000	96.100	91.295	2.536
32.000	102.400	97.280	2.702
33.000	108.900	103.455	2.874
34.000	115.600	109.820	3.051
35.000	122.500	116.375	3.233
36.000	129.600	123.120	3.420
37.000	136.900	130.055	3.613
38.000	144.400	137.180	3.811
39.000	152.100	144.495	4.014
40.000	160.000	152.000	4.222
41.000	168.100	159.695	4.436
42.000	176.400	167.580	4.655
43.000	184.900	175.655	4.879
44.000	193.600	183.920	5.109
45.000	202.500	192.375	5.344
46.000	211.600	201.020	5.584
47.000	220.900	209.855	5.829
48.000	230.400	218.880	6.080
49.000	240.100	228.095	6.336
50.000	250.000	237.500	6.597
51.000	260.100	247.095	6.864
52.000	270.400	256.880	7.136
53.000	280.900	266.855	7.413
54.000	291.600	277.020	7.695
55.000	302.500	287.375	7.983
56.000	313.600	297.920	8.276
57.000	324.900	308.655	8.574
58.000	336.400	319.580	8.877
59.000	348.100	330.695	9.186
60.000	360.000	342.000	9.500
61.000	372.100	353.495	9.819
62.000	384.400	365.180	10.144
63.000	396.900	377.055	10.474

64.000	409.600	389.120	10.809
65.000	422.500	401.375	11.149

Turn both devices on, setting both V_{IN}=0V and I_{OUT}=0A[8]. Read the source and load manuals for instructions on setting up the limits of each device.

Increase the current limit to the value of I_{OUT} before incrementing the voltage. When V_{IN} gets too high relative its I_{OUT}, V_{OUT} may rise unpredictably and is not allowed to exceed 80V because of the capacitors. Measure the voltage, current, and powers in and out of the system and compare with Table 9.1. Table 9.2 contains the results.

Table 9.2 Measured output voltages at varying input voltages

V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	η (%)
6	.68	4.08	33	0.06	1.98	49
10	.69	6.9	35	0.12	4.2	61
15	.71	10.65	28	0.12	3.36	32
20	.72	14.4	14	0.12	1.68	12

The results from Table 9.2 indicate the circuit operates incorrectly. A spark occurred while attempting to probe the gate of Q1. Figure 9.3.1 and a continuity test verify it shorted.

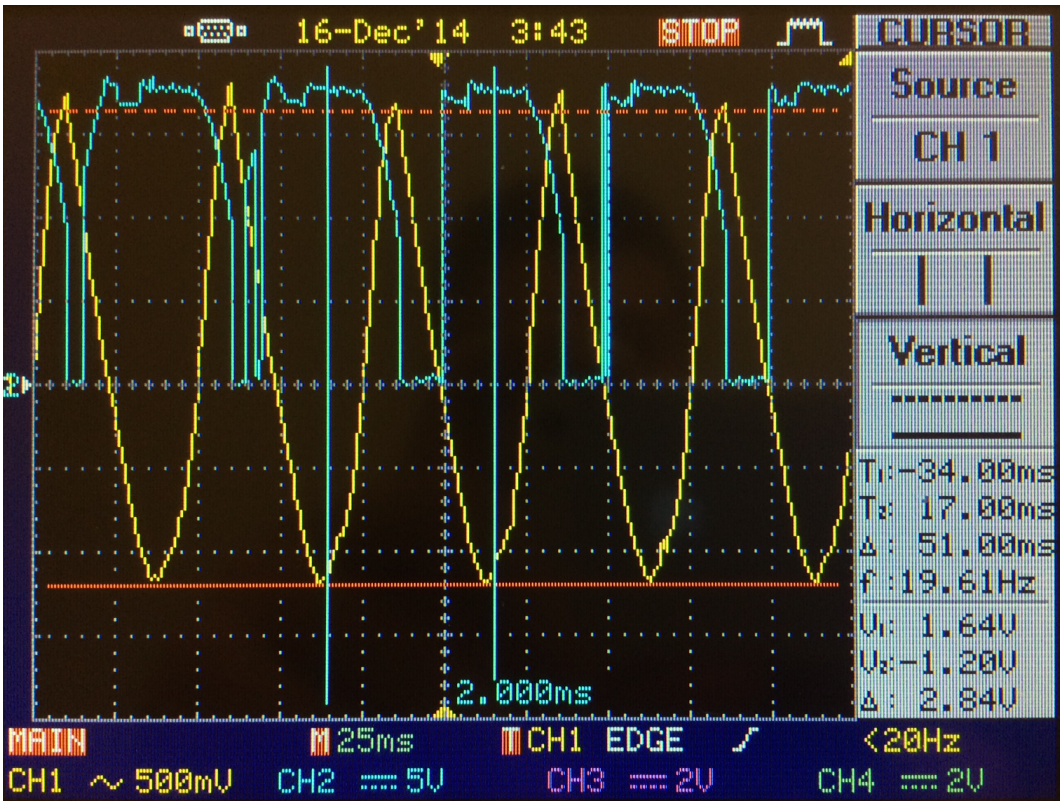

Figure 9.3.1 V_{OUT} Ripple, V_{IN}=10V, $V_{GS,Q1}$ blue, V_{OUT} yellow

[8] The BK8540-ND can be disconnected from the circuit using the 'Short' button while remaining powered on.

The gate-source voltage oscillates between 0V and 23V, the same values as V_{DS}. This verifies V_G has been shorted to V_D and the circuit cannot operate correctly. Figure 9.3.1 illustrates the circuit oscillating 20Hz (cycles per second). The design should oscillate 100 kHz (thousand cycles per second). Finally, the peak-peak ripple, V_{pp}, measures to be 2.84V, the calculations squelch it to .2V_{pp}. Q1 needs to be de-soldered and replaced for accurate circuit behavior (assuming nothing else has fried on the board related to Q1's failure).

10 Conclusions

EHFEM provides innovative solutions toward solving the world energy crisis and reducing human-produced greenhouse gases. It uses environment friendly materials and complies with international electrical standards.

Referring to Figure 12.1 Project Plan Gantt Chart, the project did not meet its original goals. Future teams who desire to successfully complete the project should make a plan, and then extend the times allotted to each phase of their plan threefold (or more). Major sources of lost time during this project include inadequate switch models, inadequate source models, learning new information about the project each time the team met, collaborating with other teams, improperly utilizing past sources, improperly comprehending results, finding appropriately sized components, and choosing the correct CAD program. Capitalize on times when everyone in the group can meet, and leave an abundance of time available for other classes. Figure 10.1 Post-Project Gantt Chart, more accurately describes the progress our team made designing the LT8705 circuit.

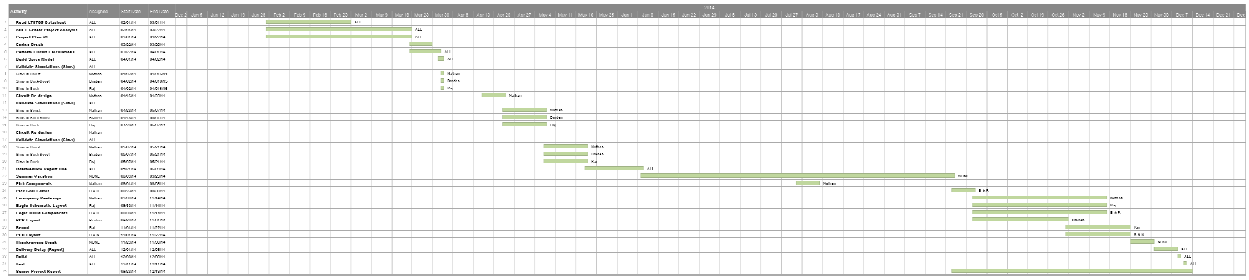

Figure 10.1 Post-Project Gantt Chart

Table 10.1 **Gantt Chart Time Allotments** clarifies Figure 10.1 **Post-Project Gantt Chart**'s poor resolution.

Table 10.1 Gantt Chart Time Allotments

Activity	Assigned	Start Date	End Date
Read LT8705 Datasheet	ALL	02/01/14	03/01/14
ABET Senior Project Analysis	ALL	02/01/14	03/22/14
Project Plan V1	ALL	02/01/14	03/22/14
Spring Break		03/22/14	03/29/14
Perform Circuit Calculations	ALL	03/22/14	04/01/14
Build Spice Model	ALL	04/01/14	04/02/14
Validate Simulations (Sims)	ALL		
Sims in Boost	Nathan	04/02/14	04/016/14
Sims in Buck-Boost	Braden	04/02/14	04/016/15

Sims in Buck	Raj	04/02/14	04/016/16
Circuit Re-design	Nathan	04/16/14	04/23/14
Validate Simulations (Sims)	ALL		
Sims in Boost	Nathan	04/23/14	05/07/14
Sims in Buck-Boost	Braden	04/23/14	05/07/14
Sims in Buck	Raj	04/23/14	05/07/14
Circuit Re-design	Nathan		
Validate Simulations (Sims)	ALL		
Sims in Boost	Nathan	05/07/14	05/21/14
Sims in Buck-Boost	Braden	05/07/14	05/21/14
Sims in Buck	Raj	05/07/14	05/21/14
Intermediate Report Due	ALL	05/21/14	06/09/14
Summer Vacation	NONE	06/09/14	09/23/14
Pick Components	Nathan	08/01/14	08/08/14
Pick CAD Editor	B & R	09/23/14	09/30/14
Emergency Re-design	Nathan	09/30/14	11/14/14
Eagle Schematic Layout	Raj	09/30/14	11/14/14
Eagle Build Components	B & R	09/30/14	11/14/14
PCB Layout	Braden	09/30/14	11/01/14
Report	Raj	11/01/14	11/22/14
PCB Layout	B & N	11/01/14	11/22/14
Thanksgiving Break	NONE	11/23/14	11/30/14
Delivery Delay (Work on Report)	ALL	12/01/14	12/08/14
Build	ALL	12/09/14	12/09/14
Test	ALL	12/11/14	12/11/14
Senior Project Report	ALL	09/23/14	12/13/14

The figure and table above indicate insufficient time for building and testing, and this can be attributed to the delivery delay that occurred during dead week. Receipts revealed Pentalogix forgot to include solder paste when placing the original orders out, so although all of the parts, the board, and stencil were in hand, nothing could be put together.

The emergency re-design in September came from knowledge gained working an internship over summer. Before summer vacation, the team was still rather mystified about how to KNOW the circuit was behaving appropriately. Post-summer vacation, system interfacing and many fundamental power concepts directed the circuit's re-design.

Although the circuit failed its testing, this data is inconclusive. LtSpice simulations predict more than adequate circuit behavior, failure to realize the predictions probably occurred during the Layout and Assembly in Sections 7 and 8. Future groups elaborating on the LT8705 design should focus primarily on the following areas. Key points of improvement in these areas include:

- Larger Board Dimensions: a must. Going into full Buck mode dissipates a LOT of heat, so the FETs need the largest heat sinks possible. This space needs to be accommodated through using a larger board.

- Easily Accessible Test Points: if you think you can *probably* access a connection, you probably can't. Referring to [9], David and Sheldon soldered test pegs that oscilloscope probes could easily connect to.

Time, money, and resources constrained the project the most. Braden and Raj chose Eagle as their CAD Editor for its compatibility with Apple products, which later inhibited the amount of space on the board for financial reasons, which left inadequate space for large heat sinks and accessible test points. Inaccessible test points, delivery delays, and finals left the group with poor ability to properly test its finished product. As mentioned before, future groups are advised to re-use the design but properly lay the components out in a CAD program that offers larger board dimensions.

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12 APPENDIX A: Senior Project Analysis

12.1 Summary of Functional Requirements

The EHFEM project harvests wasted energy from elliptical trainers. EHFEM has a number of sub-groups working together to create a stable and reliable DC-DC conversion system that harvests energy with 85% efficiency [1]. Input protection circuitry handles the unpredictable waveform from the elliptical, which stabilizes it for the LT8705C buck-boost converter [8]. The buck-boost converts this waveform into an approximate DC voltage, but may contain large ripple [13]. The ripple is filtered through an output capacitance, and a constant DC voltage with varying current is produce. A current limiter handles current overflow to comply with the inverter's current rating. The current inverter supplies this power back to the grid [8].

12.2 Primary Constraints

Time and money cripple this project. The elliptical energy creates a lot of stress on components, requiring high ratings, and low tolerances. The project has an abundance of background material that must be read before beginning the design stages, and other classes still need time allotted to them. The LT8705 IC has 38 pins, most likely requiring a more complex board, meaning more money. This makes the project less cost-effective.

12.2.1 Economic

Human Capital

- Engineers design and manufacture the board.
- Skilled workers assemble and install the system to the exercise machine.
- The general public uses the EHFEM elliptical.
- Cal Poly's Recreational Center will dispose of it appropriately and students will use nontoxic components for human health [16].

Financial Capital

- Assembling the board requires components/IC's purchased from supply companies.
- Manufacturing technologies develop the PCB boards.

Manufactured or Real Capital

- Manufacturing facilities develop the tools used in other facilities where circuit components are developed.

Natural Capital

- The converter consists of plastics, copper, silicon, and various other elements used in processing the boards [3].
- EHFEM capitalizes on waste and produces clean energy.

When and where do costs and benefits accrue throughout the projects lifecycle?

- Costs accumulate as time progresses through the project. Hours get devoted to development, and expenses increase with unexpected component failures and burnouts.

- The converter's benefits accrue at the project completion. The completed project harvests wasted energy.

What inputs does the experiment require? How much does the project cost? Who pays?

- The project requires component inputs and labor input.
- The estimated project cost is $9,980, labor and parts included.
- Recreation centers purchase the product as a method of saving energy.
- Cal Poly's Electrical Engineering department pays for the EHFEM components.

How much does the project earn?

- The project earns at a rate expected to pay itself off in 10 years.

12.2.2 Timing

- The final product emerges as the final design is completed and tested.
- The product is expected to last 10 years.
- Regular scheduled maintenance is not expected within the first 10 years [15].
- Figure A-1 and Table A-1 show the Project Plan Gantt Chart and Task Distribution starting from January 2014 to December 2014.

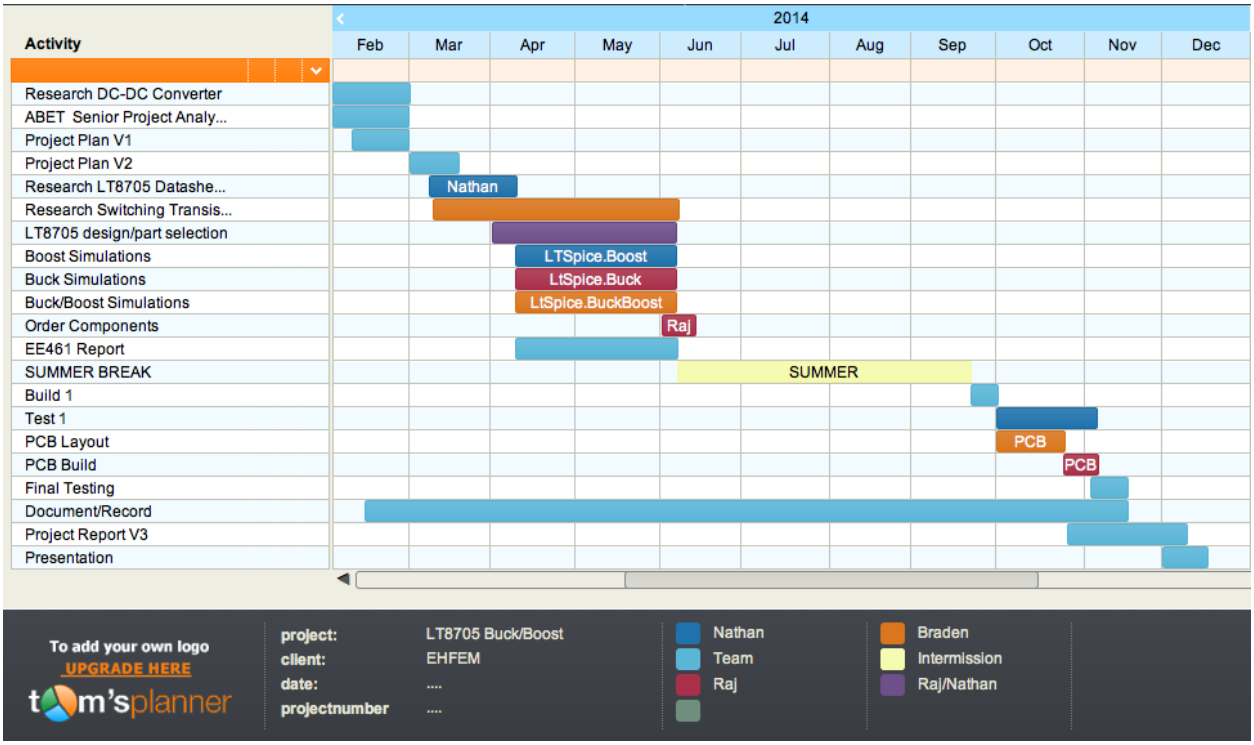

Figure 12.1 Project Plan Gantt Chart

Table 12.1 Project Plan Task Distribution

Assigned To	Finish	Start	Duration (Days)	Task Name
Team	02/22/14	01/22/14	32	Research DC-DC Converter
Team	02/27/14	02/07/14	20	ABET Senior Project Analysis
Team	02/28/14	02/12/14	13	Project Plan V1
Team	03/14/14	03/02/14	11	Project Plan V2
Nathan	04/14/14	03/14/14	30	Research Converter Data Sheet
Braden	06/06/14	03/21/14	75	Research Transistors
Raj/Nathan	06/11/14	04/05/14	67	LT8705Design/Part Selection
Raj	06/19/14	06/12/14	8	Order Component
Braden/Raj	10/02/14	09/19/14	80	Build 1
Nathan - team	11/04/14	10/01/14	39	Test 1
Braden/Nathan	10/28/14	10/09/14	19	Design 2 - PCB layout etc
Team	11/04/14	10/28/14	17	Build 2 - PCB construct
Team	11/20/14	11/5/14	16	Final Testing
Raj - team	12/04/14	01/22/14	227	Documentation
Team	12/03/14	11/18/14	12	Project Report V3
Team	12/05/14	12/05/14	1	Senior Project Presentation

If Manufactured on a Commercial Basis

- Estimated parts cost of devices sold per year: 25 units at $40 = $1000
- Estimated purchase price: $200 X 25 units = $5000 revenue
- Expected labor cost: $150 per unit. Labor cost per year: $150x25 = $3750
- Estimated profit per year: $250
- No expected maintenance fees for first 10 years of use; replacement parts available for $20 after first 10 years.

12.2.3 Environmental

Positive Impacts

- EHFEM produces clean, renewable energy [1]. This energy can be used by the general public once made available by the power company.
- Recreation centers become less dependent on the power grid. Saving energy will benefit the general public in the long term.
- Sends clean energy back to grid. The power company will have more energy available for the public with the addition of the EHFEM project to the Recreation Center.

Negative Impacts

- Production requires Earth's natural resources: oil, copper, silicon etc. These resources are limited and may not be available forever.
- Production requires energy from manufacturing and transportation of parts. Burning of fossil fuels may be detrimental to the environment.

12.2.4 Manufacturability

- Issues associated with manufacturing include damage to materials used in production due to miscalculation, and heat sensitive components such as wires and transistors. EHFEM system design intends assembly to be the most difficult part of manufacturing. Labor costs exceed project budget [1].

12.2.5 Sustainability

- System should maintain proper working order for 10 years (project goal) without any replacement parts.
- Possible system error due to human production error. Some components may not have the correct calculations which may compromise the product.
- Exercise machines function everyday resulting in wear and tear. System requires testing after first 10 years to ensure maximum efficiency [15].

12.2.6 Ethical

- The project follows a Utilitarian approach
  - The utilitarian approach implies the greatest good for the greatest number. The EHFEM project provides clean and renewable energy back to the grid, and at the same time, promotes a healthy and fit lifestyle.
- The EHFEM design is developed with customer safety in mind. The components must show discreetness and not alter the operation of the exercise machine in any way.
- IEEE code of ethics #1: "to accept responsibility in making decisions consistent with the safety, health, and welfare of the public, and to disclose promptly factors that might endanger the public or the environment" [17].
  - The system requires human contact, therefore users needs to be notified of the harvesting application. User must consent energy harvesting to avoid legal issues. Warnings should appear on consent form
- IEEE code of ethics #5: "to improve the understanding of technology; its appropriate application, and potential consequences" [17].
  - The EHFEM system improves our understanding of energy harvesting machines by capturing clean energy from human physical activity. The system applies to elliptical machines found in most Recreation Centers, and results in clean energy delivered back to the energy grid.
- Cheap components lead to a low production cost; however components must fall under the RoHS compliance. This provides that each component consists of non-toxic elements (ie. Lead-free) for user and overall safety [3].

12.2.7 Health and Safety

- The project aims to create clean renewable energy by promoting exercise to the general public.
- The system requires soldering components on to the PCB board. The soldering process poses potential health risks from high temperatures and fumes [14].
- User must comply with the elliptical machine instructions in order to guarantee safety. The EHFEM project does not impose any added health risks from normal exercise use. Therefore, customer may exercise without potential safety concerns.
- Precautions must be taken with electrical equipment from potential perspiration and water damage. Spilled drinks could affect the elliptical machine components, thus limit drinks near exercise machine for safe machine use.

12.2.8 Social and Political

- The project makes a social impact on the community and other universities by showing energy conservation at the Cal Poly Recreation Center. This includes potential Recreation Center cost cuts on energy.

Direct Stakeholders

- Cal Poly and relevant public relations benefit from the project by cutting energy spending, and sending energy back to the power company grid.
- Project members benefit from the success of the project. A successful project means all students involved may get recognition and possible financial gain if sold commercially.
- Advisor, Professor Braun, benefits by leading a successful project team [1].

Indirect Stakeholders

- Cal Poly Students – EHFEM uses department funding and other resources.
- Parts manufacturers have their names on the components used in production. The manufacturers show that each component complies with the correct electronic compliances.
- Inequities arise only if the project fails and the department's funds go to waste.
- If project succeeds, San Luis Obispo Power Company will receive clean renewable energy.
- Patents and delivery services make sure components arrive on time with legal agreement from specific patents. Configuring the product with correct DC/AC conversion requires patent identification for basic design [17].

12.2.9 Development

New techniques and understandings gathered through the project

- Using IGBTs (insulated-gate bipolar transistor) to bias the DC-DC converter for maximum efficiency.
  - Knowledge of different transistor applications help project members develop a product within the intended ethical frameworks.
- Ethical Frameworks
  - Understanding of ethical frameworks is fundamental to engineering design. The guidelines make sure all people involved are safe, and the product executes its intended purpose. For EHFEM, the utilitarian approach becomes paramount.
- Organized project planning skills

- Planning the project in advance requires extensive literature search and organized scheduling. This process helps each team member become familiar with product and each other.

- Literary Search
  - Gaining sufficient knowledge of the product and each component helps in designing the most efficient system possible. Innovative design could possibly arise from widespread research.
  - See pages 60-61 for literature search list.