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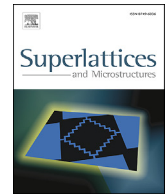

Rapid thermal annealing: An efficient method to improve the electrical properties of tellurium compensated Interfacial Misfit GaSb/GaAs heterostructures

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ABSTRACT

The effect of thermal annealing on Te compensated Interfacial Misfit GaSb/GaAs heterostructures is investigated by using two different thermal annealing procedures, namely rapid thermal annealing and furnace annealing. The electrical properties of the devices are studied by using Current–Voltage, Capacitance–Voltage and Deep Level Transient Spectroscopy techniques. It is observed that rapid thermal annealing treatment is superior in terms of improvement of the electrical characteristics compared to furnace annealing treatment. The lowest leakage current and defect concentration are obtained when rapid thermal annealing is employed.

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1. Introduction

III-Sb based devices attract considerable attention in high speed and low power consumption electronic devices compared to other III–V based devices such as InP and GaAs [1,2]. This is due to the band gap offset, electronic barrier and extremely high mobilities of such Sb based devices. The use of high quality semi-insulating GaAs and Si substrates instead of GaSb for the epitaxial growth of III-Sb heterostructures has several advantages including lower costs and larger sizes of substrates. In addition, such substrates allow the integration of optoelectronic devices such as laser diodes [3], detectors [4], and transistors [5]. Therefore tremendous efforts have been devoted to grow high quality III-Sb layers on GaAs and Si substrates despite the large lattice mismatch between these materials that result in the creation of defects and dislocations. One of the promising techniques to get high quality buffer free GaSb layer is by using the Interfacial Misfit (IMF) method. By using this technique the IMF array is comprised of Ga-dangling bonds with a sheet density of 3×10^{12} cm^{-2}, which create interfacial states [6]. These interfacial states, which are introduced between GaSb and GaAs have serious effect on the performance of the devices [7,8]. A. Jallipalli et al.[6] introduced the concept of delta doping at the interface between GaSb and GaAs to compensate the Ga

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dangling bonds. However, in previous studies by our group on similar Te-doped (delta doped) GaSb/GaAs devices [7] we observed that their electrical behaviour worsens. In another studies [9] on Interfacial Misfit (IMF) GaSb/GaAs, the effect of rapid thermal annealing was studied. The devices show better electrical properties after thermal annealing treatment. In this study we have investigated the effect of two different thermal annealing treatments on the electronic properties of the Te-delta doped devices using Current–Voltage (I–V), Capacitance–Voltage (C–V) and Deep Level Transient Spectroscopy (DLTS). The experimental results show that the rapid thermal annealed (RTA) samples have better electrical properties than as-grown and furnace annealed (FA) samples.

2. Experiment details

The growth conditions of the devices investigated here are similar to those reported in Refs. [7,9]. In brief, the IMF is created between the 10 nm GaAs and 10 nm GaSb layers. In order to compensate the dangling bonds created between Ga and Sb atoms (shown by the circles in Fig. 1b), a sheet of 10^{12} cm^{-2} of Te atoms are deposited. The intension was to reduce the dangling bonds created at the misfit as reported in Ref. [7]. The layer structure of Te compensated Interfacial Misfit GaSb/GaAs and the schematic representation of misfit are shown in Fig. 1a and b, respectively. The rapid thermal annealing and furnace annealing were performed on Te-compensated IMF GaSb/GaAs samples. The RTA is performed in rapid thermal annealer (RTA) in a N_2 ambient. The samples annealing time for RTA was 2 min at 400 °C. While in the furnace annealing, N_2 was purged into a glass furnace for 2 min, and then the samples were introduced into the furnace where they reached a temperature of 400 °C over a period of 2 min and left for an additional 2 min at 400 °C.

After post growth RTA and furnace annealing, the ohmic contacts were formed on the top of the p^+ GaSb layer and the bottom of the n^+ GaAs substrates. Mesas with 200 μm diameter were formed and isolated from each other by using wet chemical etching.

The Te compensated samples have been studied carefully by I–V and C–V measurements using a current source unit (Keithley 236) and Boonton capacitance meter (B7200), respectively which are controlled by software. The emission from the traps depends upon the temperature. In order to get accurate information about defects, a very temperature stable cryostat (model Janis CCS-450) controlled by Lake Shore 331 is in the temperature range of 10 K–450 K with stability of $\pm$ 1 K. The capacitance meter (Boonton 7200) and pulse generator (Agilent 33220A) are used to get information about defects.

3. Results and discussion

3.1. Current–Voltage (I–V) measurements

The Current–Voltage (I–V) measurements were performed on as-grown and annealed Te compensated samples as shown in Fig. 2. The reverse current of RTA samples is one and two orders of magnitude lower than as-grown and furnace annealed samples, respectively It is worth mentioning that several devices having different diameters were tested and similar results were obtained. Additionally, the rectification ratio for the RTA samples (1×10^6 at $\pm$ 0.55 V) is one order of magnitude higher than as-grown and FA samples. However, the 400 °C FA samples exhibited the highest reverse current which is an indication of adverse electrical activity after furnace annealing. This effect will be further explored by Capacitance-Voltage and DLTS measurements in the following sections.

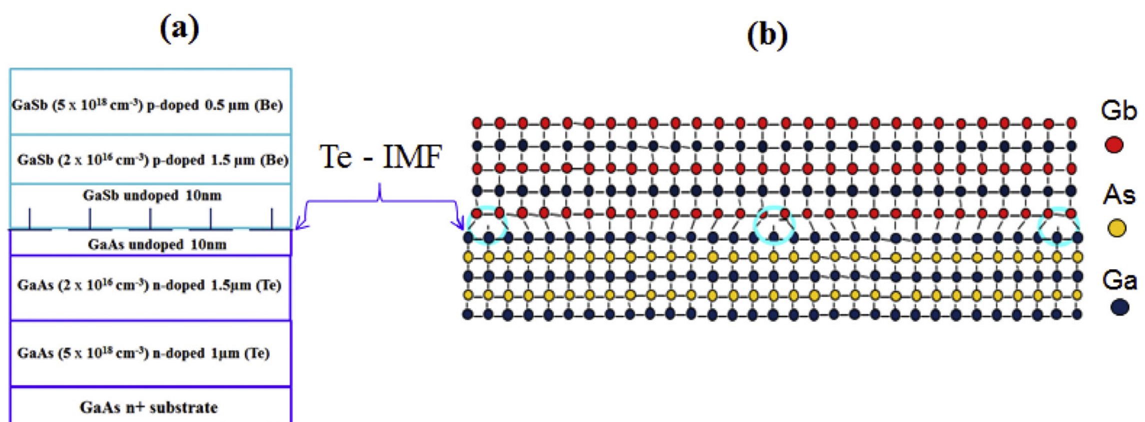

Fig. 1. (a) Layer structure of GaSb/GaAs Interfacial Misfit heterostructures and (b) schematic representation of Interfacial Misfit formation.

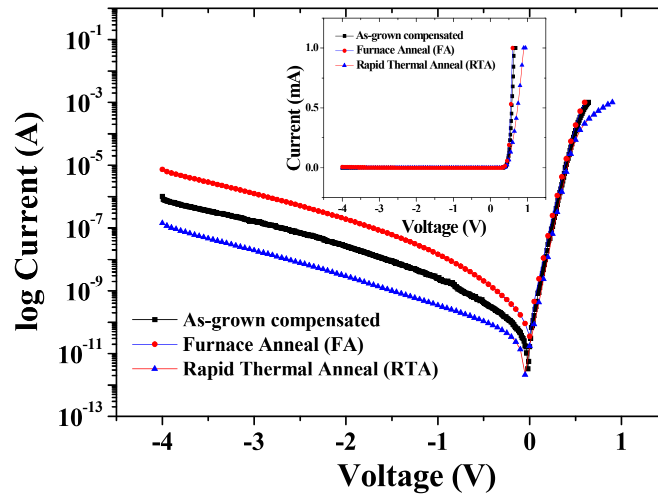

Fig. 2. I–V characteristics of as-grown and annealed (400 °C Rapid thermal annealing (RTA) and furnace annealing (FA)) Te compensated GaSb/GaAs samples. The insert shows the turn on (V_{on}) of as-grown and annealed (400 °C RTA and FA) devices.

3.2. Capacitance–Voltage (C–V) measurements

The Capacitance–Voltage (C–V) measurements are performed at a fixed frequency of 1 MHz over a range of temperatures (100 K–450 K). The room temperature C–V data is plotted as $1/C^2$ versus ($V_{on} + V_R$) as shown in Fig. 3 for as-grown and annealed samples (RTA and FA) which reveal a non-linear behaviour. It is worth noting that the C–V data plotted for different temperatures shows similar behaviour. The interface state capacitance is extracted from the plot of C versus $(V_{on} + V_R)^{-1/2}$ as shown in Fig. 4.

It is worth pointing out that the value of interface states capacitance is lowest in RTA samples. Both I–V and C–V characteristics shown in Figs. 2 and 4, respectively, confirm the effect of annealing on the interface in terms of low reverse leakage current and small interface capacitance of the devices. The RTA samples have the smallest reverse current and interface state capacitance. These higher capacitance values are indications of higher density of interface trap states for as-grown and FA samples, as will be shown in the DLTS section.

3.3. Deep Level Transient Spectroscopy (DLTS) measurements

The existence of and the effect of annealing (rapid thermal and furnace annealing) on electrically active defects near and away from the interface of Te-compensated GaSb/GaAs samples are investigated by applying small to large reverse biases using DLTS. Fig. 5a shows the DLTS spectra of as-grown and 400 °C rapid thermal and furnace annealed samples for a reverse

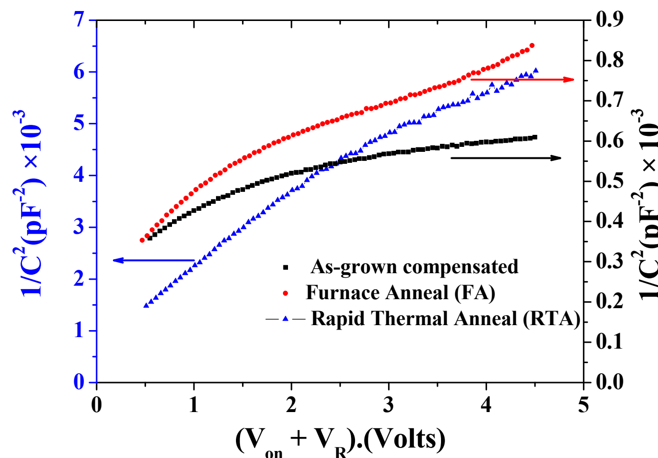

Fig. 3. Room temperature plots of $1/C^2$ as function of ($V_{on} + V_R$) for as-grown and annealed (400 °C RTA and FA) Te-compensated samples.

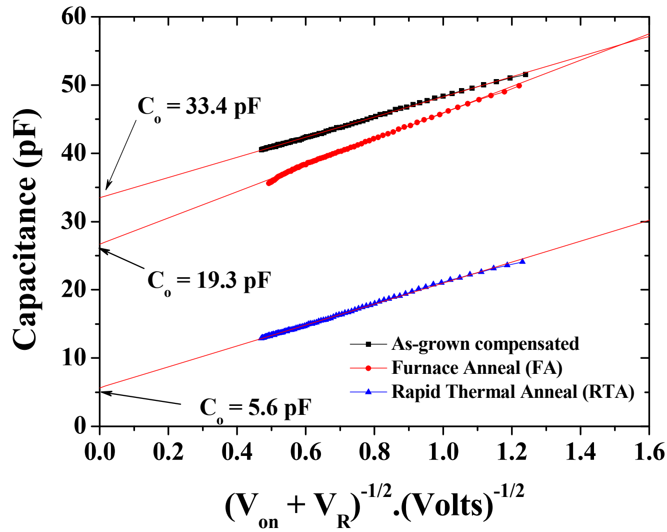

Fig. 4. Plots of capacitance (C) as function of $(V_{on} + V_R)^{-1/2}$ for as-grown and annealed (400 °C RTA and FA) Te-compensated samples. The RTA samples exhibit the lowest interface state capacitance compared to as-grown and furnace annealed samples.

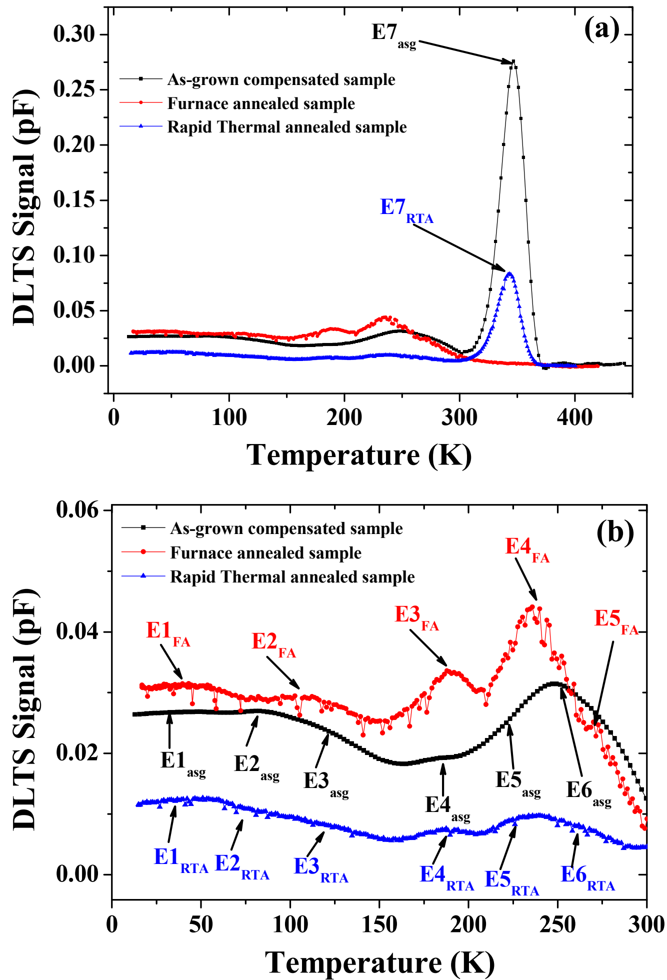

Fig. 5. DLTS spectra of as-grown and annealed (400 °C rapid thermal and furnace anneal) Te compensated samples. The DLTS measurements were taken with a small reverse bias, $V_R = -0.25$ V, in order to probe the region near to the interface (depletion width extend from 0.20 μm to 0.315 μm). The filling pulse characteristics were: $V_p = 0$ V, $t_p = 1$ m sec, and rate window = 200 s^{-1} and (b) DLTS peaks detected in the temperature range 10–300 K are shown for clarity.

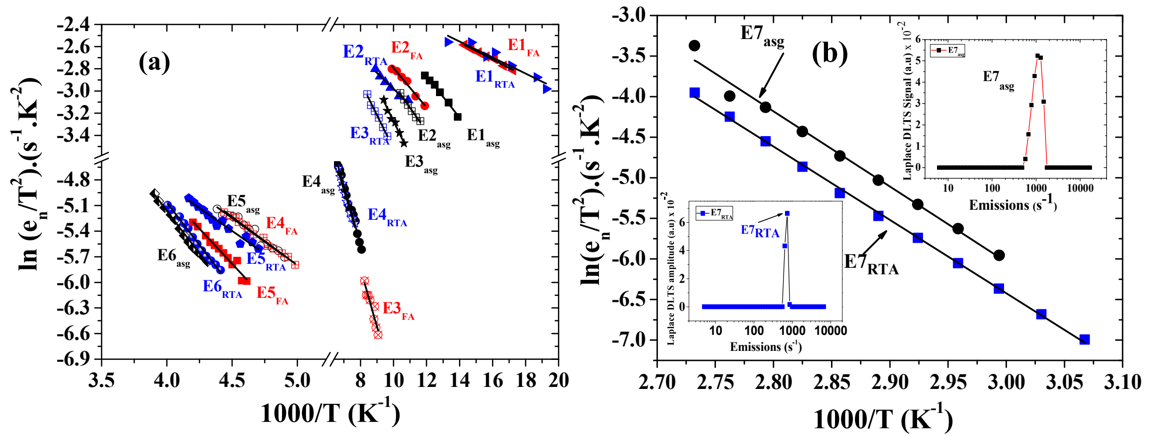

Fig. 6. Arrhenius plots obtained from Laplace DLTS of (a) as-grown and annealed (400 °C RTA and FA) Te-compensated GaSb/GaAs samples using a small reverse bias of $V_R = -0.25$ V and (b) peaks $E7_{asg}$ and $E7_{RTA}$ for as-grown and RTA compensated samples, respectively.

bias of $V_R = -0.25$ V, $V_P = 0$ V and $t_p = 1$ m sec. The depletion width extend from 0.20 µm from equilibrium condition (0 V) to 0.315 µm at a reverse bias of $V_R = -0.25$ V. For clarity Fig. 5b displays the peaks detected in the temperature range 10–300 K.

Seven electron trap peaks, labelled $E1_{asg}$, $E2_{asg}$, $E3_{asg}$, $E4_{asg}$, $E5_{asg}$, $E6_{asg}$ and $E7_{asg}$, are observed in as-grown samples. A similar number of defects is also detected in rapid thermal annealed samples, labelled here as $E1_{RTA}$, $E2_{RTA}$, $E3_{RTA}$, $E4_{RTA}$, $E5_{RTA}$, $E6_{RTA}$ and $E7_{RTA}$. However, in FA samples five electron trap peaks, $E1_{FA}$, $E2_{FA}$, $E3_{FA}$, $E4_{FA}$ and $E5_{FA}$ are detected. The amplitude of the main DLTS signal in RTA samples ($E7_{RTA}$) is lower than that of the as-grown samples ($E7_{asg}$). The peaks $E7_{asg}$ and $E7_{RTA}$ are identified as EL2 trap, which is well-known in GaAs. Its concentration is much lower in rapid thermal annealed samples than in the as-grown samples. However, this defect is absent in furnace annealed samples. Fig. 6a and b show the Arrhenius plots of as-grown, RTA and FA samples for a small reverse bias of $V_R = -0.25$, $V_P = 0$ V and tp = 1 m sec. The traps emission rates are extracted from Laplace DLTS. The activation energies, capture cross-sections and concentrations of the traps are summarized in Table 1.

DLTS spectra obtained for a larger reverse bias of $V_R = -4$ V, $V_P = 0$ V and $t_p = 1$msec for as-grown, RTA and FA samples are shown in Fig. 7. The depletion width extends from 0.20 µm to 0.81 µm from thermal equilibrium (0 V) to $V_R = -4$ V. As can be seen from Fig. 7a the amplitude of all the DLTS peaks increases. This indicates an increase of the concentration of all traps. In particular, the concentration of trap $E7_{asg}$ (EL2 defect) is increased from 2.51×10^{14} cm^{-3} close to the GaSb/GaAs interface region [$V_R = -0.25$ V (0.315 µm)] to 3.36×10^{15} cm^{-3} away from interface region [$V_R = -4$ V (0.81 µm)].

However, for RTA devices the concentration of $E7_{RTA}$ (EL2) has increased only by a smaller amount from 5.62×10^{12} cm^{-3} to 7.91×10^{12} cm^{-3}. The concentration increase of EL2 in RTA samples is much lower as compared to as-grown samples. This trap (EL2) which was absent near the GaSb/GaAs interface in FA samples at smaller reverse bias, but is detected away from the

Table 1
Activation energies, capture cross-sections and concentrations of traps detected in Te-compensated as-grown, FA and RTA samples at $V_R = -0.25$ V, $V_P = 0$ V, and $t_p = 1$ m sec.

Sample ID	Traps	Activation energy (eV)	Apparent capture cross-section (cm^{-2})	Trap concentration (cm^{-3})
Compensated as-grown (asg)	$E1_{asg}$	0.007 ± 0.001	2.05×10^{-21}	2.49×10^{13}
	$E2_{asg}$	0.016 ± 0.001	4.89×10^{-21}	2.52×10^{13}
	$E3_{asg}$	0.026 ± 0.002	9.89×10^{-21}	2.50×10^{13}
	$E4_{asg}$	0.058 ± 0.004	7.61×10^{-21}	2.28×10^{13}
	$E5_{asg}$	0.096 ± 0.004	7.15×10^{-21}	2.53×10^{13}
	$E6_{asg}$	0.173 ± 0.002	1.58×10^{-19}	2.93×10^{13}
	$E7_{asg}$	0.750 ± 0.004	4.81×10^{-12}	2.51×10^{14}
Furnace Annealed (FA)	$E1_{FA}$	0.006 ± 0.004	3.17×10^{-21}	1.09×10^{13}
	$E2_{FA}$	0.012 ± 0.002	3.15×10^{-21}	9.87×10^{12}
	$E3_{FA}$	0.052 ± 0.002	2.89×10^{-21}	1.13×10^{13}
	$E4_{FA}$	0.098 ± 0.002	1.34×10^{-20}	1.50×10^{13}
	$E5_{FA}$	0.142 ± 0.004	7.42×10^{-20}	8.56×10^{12}
Rapid Thermal Annealed (RTA)	$E1_{RTA}$	0.007 ± 0.002	3.35×10^{-21}	8.45×10^{11}
	$E2_{RTA}$	0.015 ± 0.002	5.32×10^{-21}	6.38×10^{11}
	$E3_{RTA}$	0.026 ± 0.002	1.19×10^{-19}	5.08×10^{11}
	$E4_{RTA}$	0.055 ± 0.003	9.72×10^{-21}	5.60×10^{11}
	$E5_{RTA}$	0.092 ± 0.004	8.22×10^{-21}	6.54×10^{11}
	$E6_{RTA}$	0.171 ± 0.002	2.57×10^{-19}	5.10×10^{11}
	$E7_{RTA}$	0.78 ± 0.01	1.37×10^{-11}	5.62×10^{12}

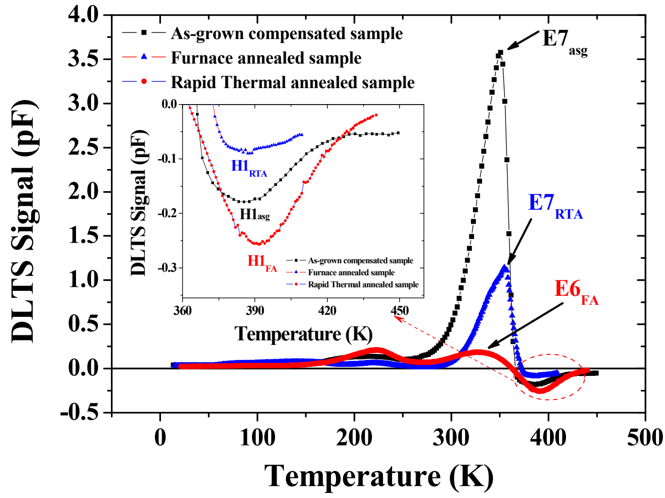

Fig. 7. DLTS spectra of as-grown and annealed (400 °C rapid thermal and furnace anneal) Te-compensated samples. The DLTS spectra shown are taken with a large reverse bias, $V_R = -4$ V, in order to probe an extended region from the interface. The filling pulse characteristics were: $V_p = 0$ V, $t_p = 1$ m sec, and rate window = 200 s^{-1} and in the inset hole peaks for as-grown, RTA and FA samples are shown for clarity.

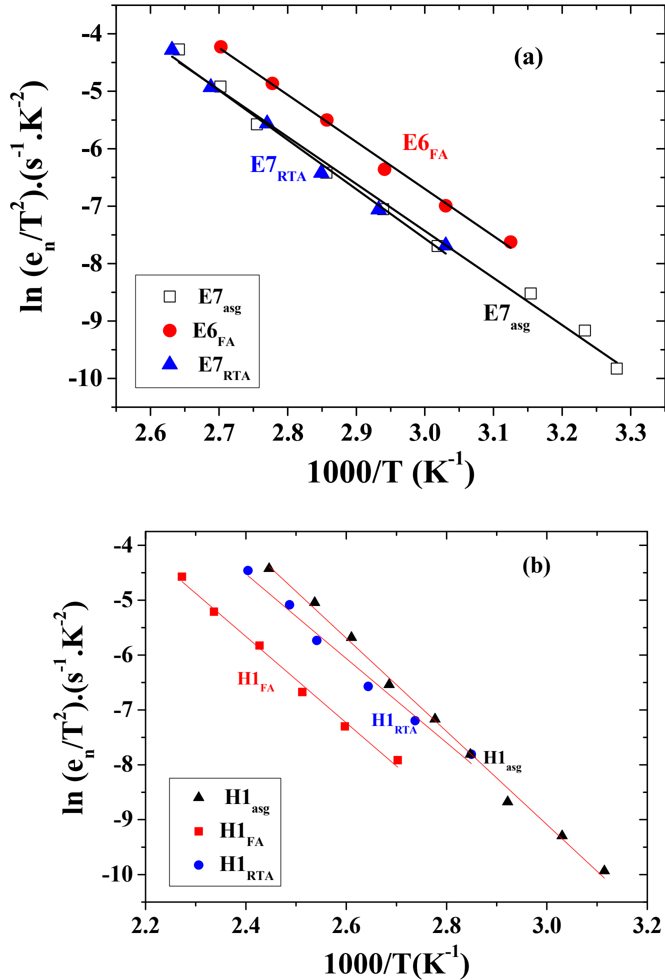

Fig. 8. (a) Arrhenius plots obtained from Laplace DLTS data for as-grown and annealed (400 °C RTA and FA) Te-compensated samples at a larger reverse bias of $V_R = -4$ V which allows probing the region away from the interface of GaAs/GaSb heterojunction devices and (b) A new hole trap is detected in all Te-compensated as-grown and annealed devices.

Table 2
Activation energies, capture cross-sections and concentrations of traps detected in Te-compensated as-grown, FA and RTA samples at $V_R = -4$ V, $V_P = 0$ V, and $t_p = 1$ m sec.

Sample ID	Traps	Activation energy (eV)	Apparent capture cross-section (cm^{-2})	Trap concentration (cm^{-3})
Compensated as-grown (asg)	$H1_{asg}$	0.73 ± 0.01	1.86×10^{-13}	1.58×10^{14}
	$E7_{asg}$	0.71 ± 0.01	7.76×10^{-15}	3.36×10^{15}
Compensated Furnace Anneal (FA)	$H1_{FA}$	0.68 ± 0.01	7.76×10^{-15}	1.21×10^{14}
	$E6_{FA}$	0.71 ± 0.01	8.10×10^{-13}	1.96×10^{14}
Compensated Rapid Thermal Anneal (RTA)	$H1_{RTA}$	0.66 ± 0.01	1.55×10^{-14}	1.65×10^{14}
	$E7_{RTA}$	0.74 ± 0.01	1.18×10^{-12}	7.91×10^{12}

interface for V_R = -4 V with a concentration of 1.96×10^{14} cm^{-3}. This behaviour has strong effect on the obvious decrease of the leakage current after RTA (Fig. 2), since the EL2 trap play an important role in the electrical and optical properties of GaAs layers. It is worth pointing out that a new hole trap is detected in as-grown and annealed samples when a larger reverse bias of $V_R = -4$ V is applied, as shown in Fig. 7b. The activation energy of this hole trap in as-grown, RTA and FA samples is $H1_{asg} = 0.72$ eV, $H1_{RTA} = 0.66$ eV and $H1_{FA} = 0.68$ eV, respectively. The concentration of this defect is similar in all samples. The origin of this hole trap can be related to Te inter-diffusion as observed by E. Kuramochi et al. in GaSb samples [10].

Fig. 8a and b show the Arrhenius plot of as-grown, and RTA and FA samples at $V_R = -4$ V. In the following, only the activation energies of the main electron trap (EL2) (Fig. 8a) and the new hole trap are extracted and discussed (Fig. 8b). Their properties are summarised in Table 2. The other DLTS peaks shown in Fig. 5b, and summarized in Table 1, in Te-compensated samples in the temperature range of ~50 K–300 K are similar to those observed near the interface ($V_R = -0.25$ V).

In order to study further the existence of defects at/or close to the interface between GaAs and GaSb, a forward pulse is applied. The DLTS experimental conditions used for this study are $V_R = 0$ V, $V_P = 0.5$ V and tp = 1 m sec. The filling pulse $V_P = 0.5$ V is equivalent to the turn-on voltage observed from the I–V characteristics. The DLTS spectra are shown in Fig. 9 for as-grown, RTA and FA samples.

As shown in Fig. 9, the shape of the signal due to the hole trap is asymmetric in all samples. The DLTS hole peak amplitude is however lowest in RTA samples. The FA samples exhibit the highest DLTS hole peak. In addition, a broader electron peak is also detected in the temperature range of 10 K–200 K, as shown in the inset of Fig. 9. In order to resolve the asymmetric hole peaks, Laplace DLTS measurements are performed as shown in Fig. 10 (b, c and d), where four hole peaks are revealed in as-grown, FA and RTA samples. Arrhenius plots of the emission rate versus temperature for all samples are plotted and shown in Fig. 10a.

Four very well resolved peaks are detected in as-grown ($H1_{asg}$, $H1_{asg}$, $H1_{asg}$, $H1_{asg}$), rapid ($H1_{RTA}$, $H1_{RTA}$, $H1_{RTA}$, $H1_{RTA}$) and furnace ($H1_{FA}$, $H1_{FA}$, $H1_{FA}$, $H1_{FA}$) annealed samples by using Laplace DLTS as shown in Fig. 10(b), (c) and (d), respectively. It is worth mentioning here that these peaks are only present in as-grown and annealed Te compensated samples. These are absent in uncompensated samples (i.e. without Te delta-doping) as reported before [9]. One can therefore infer that these hole traps are due to the incorporation of Te. The summary of the traps detected at $V_R = 0$ V, $V_P = 0.5$ V and t_p = 1msec are given in Table 3.

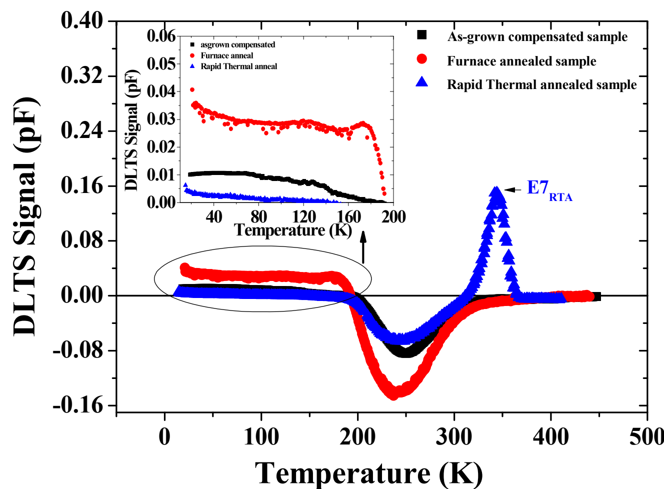

Fig. 9. DLTS spectra of as-grown and annealed (400 °C RTA and FA) Te-compensated GaSb/GaAs samples. The DLTS spectra shown are taken at a forward voltage with an amplitude equivalent to the turn-on voltage of the devices in order to probe the interface between GaSb and GaAs. The reverse bias is $V_R = 0$ V and the filling pulse characteristics were: $V_p = 0.5$ V, $t_p = 1$ m sec, and rate window = 200 s^{-1}. For clarity the inset displays the peaks detected in the temperature range 10–200 K.

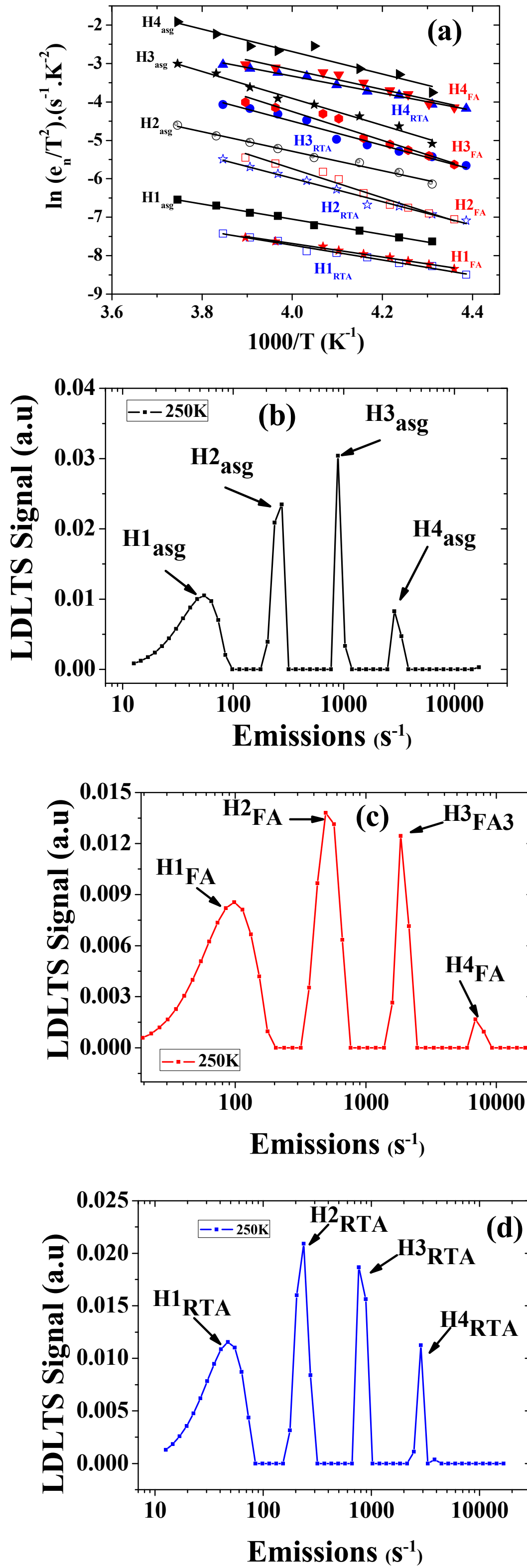

Fig. 10. (a) Arrhenius plots obtained from Laplace DLTS for as-grown and annealed (400 °C rapid thermal and furnace anneal) Te-compensated samples for a forward bias voltage of $V_p = 0.5$ V which allows probing the interface region of GaAs/GaSb heterojunction devices. Laplace DLTS revealed four hole traps in all compensated samples (b) as-grown, (c) furnace annealed (d) rapid thermal annealed.

Table 3
Activation energies, capture cross-sections and concentrations of traps observed in as-grown, rapid thermal and furnace annealed Te-compensated samples at $V_R = 0$ V, $V_P = 0.5$ V, $t_p = 1$ m sec.

Sample ID	Traps	Activation energy (eV)	Apparent capture cross-section (cm^{-2})	Trap concentration (cm^{-3})
Compensated as-grown (asg)	$H1_{asg}$	0.163 ± 0.003	2.57×10^{-21}	2.49×10^{13}
	$H2_{asg}$	0.219 ± 0.005	1.89×10^{-19}	2.52×10^{13}
	$H3_{asg}$	0.252 ± 0.013	1.56×10^{-17}	2.50×10^{13}
	$H4_{asg}$	0.302 ± 0.007	3.46×10^{-17}	2.28×10^{13}
Furnace Annealed (FA)	$H1_{FA}$	0.153 ± 0.004	8.10×10^{-22}	1.09×10^{13}
	$H2_{FA}$	0.221 ± 0.009	1.72×10^{-18}	9.87×10^{12}
	$H3_{FA}$	0.302 ± 0.010	6.52×10^{-17}	1.13×10^{13}
	$H4_{FA}$	0.325 ± 0.009	1.67×10^{-17}	1.50×10^{13}
Rapid Thermal Annealed (RTA)	$H1_{RTA}$	0.167 ± 0.004	1.45×10^{-21}	8.45×10^{11}
	$H2_{RTA}$	0.191 ± 0.003	3.76×10^{-19}	6.38×10^{11}
	$H3_{RTA}$	0.263 ± 0.007	7.43×10^{-19}	5.08×10^{11}
	$H4_{RTA}$	0.290 ± 0.008	4.51×10^{-18}	5.60×10^{11}

Some of these defects (i.e. $H3_{asg}$, $H3_{RTA}$ and $H2_{FA}$, $H4_{asg}$, $H4_{RTA}$ and $H3_{FA}$) have energies close to the ones predicted theoretically as native defects in GaSb [11–13]. All the other traps observed in the samples investigated in this work are reported here for the first time and a theoretical model is required to explore their origins. In recent study we showed that the incorporation of Te at the interface between GaSb and GaAs creates additional states [7]. In this work we showed the concentration of these additional states could be decreased by choosing appropriate annealing conditions. We also showed here and in the previous studies [9] that rapid thermal annealing is an effective way of improving electrical properties of the devices. For both annealing procedures, the peak annealing temperature (400 °C) is the same; however the duration of the ramping of the temperature to reach 400 °C is different. For the RTA system it takes only a few seconds, while for the furnace apparatus several minutes are needed. Therefore, it is most probable that the difference in the time period to attain the intended annealing temperature could account for the difference in the concentration of the traps observed in both annealing methods.

4. Conclusion

In summary, the effect of different thermal annealing protocols, namely rapid thermal and furnace annealing, on the electrical properties of Te compensated Interfacial Misfit GaAs/GaSb heterostructures is studied. Both types of annealing are performed at 400 °C for 2 min. I–V and C–V characteristics show that the smallest reverse current and the lowest interface states capacitance are obtained when the Te compensated samples are thermally treated by using the rapid thermal annealing process. The furnace annealing procedure resulted in the highest value of reverse current. Furthermore, DLTS measurements are performed with small to large reverse biases and also with forward filling pulse voltages. The concentrations of all traps detected in rapid thermal annealed samples are lower than those of as-grown and furnace annealed samples. Forward bias DLTS measurements detected four hole traps in all samples, and the concentration of the traps is lowest in rapid thermal annealed samples. One can therefore conclude that rapid thermal annealing is far more effective annealing treatment compared to the furnace annealing process in terms of better electrical properties of the devices.

Acknowledgements

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