ELECTRICAL ENGINEERING DEPARTMENT
CALIFORNIA POLYTECHNIC STATE UNIVERSITY:

SAN LUIS OBISPO

BUCK-BOOST DC-DC CONVERTER with INPUT PROTECTION SYSTEM

FOR THE

ENERGY HARVESTING from EXERCISE MACHINES PROJECT

By

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Chapter 1: Project Abstract

Cal Poly's Energy Harvesting from Exercise Machines (EHFEM) project comprises of multiple subprojects seeking to effectively create a sustainable energy source through harvesting electrical energy generated from physical exercise machines. This project designs and implements a Buck-Boost DC-DC converter using a LT3791-1 4-Switch Buck-Boost Controller, replacing the previous SEPIC design. The DC-DC converter must operate within limits set by the maximum input range of the LT3791-1 controller. An input protection system prevents inputs higher than rated values, which may adversely damage the Buck-Boost DC-DC converter. These inputs include overvoltage transients, average voltage, and current output by the Precor EFX 561i elliptical generator. Therefore, integrating a modified version of Ryan Turner and Zack Weiler's DC-DC Converter Input Protection System prevents system damage if generator outputs stray beyond safe operational range. This system also provides charge accumulation protection generated during an open-load phase during start-up of the Enphase M175 Micro-Inverter. Additionally, the DC-DC converter's output must provide a voltage within the micro-inverter's input voltage range to apply $240V_{RMS}$ power back to the electrical grid.

Chapter 2: Introduction

California Poly San Luis Obispo's ongoing EHFEM project seeks to effectively harvest renewable energy from power generated by physical exercise machines at a low implementation cost. The EHFEM project seeks to convert exercise machines into energy generating units that attain a zero lifecycle cost after ten years. A team of mechanical and electrical engineering students first established the EHFEM project in 2007 while seeking to convert an exercise bike into a standalone DC and AC generating system [1]. Since then, the EHFEM project has progressed on to harvesting electrical energy from elliptical trainers. Overall, the EHFEM project consists of multiple subprojects focusing on converting different exercise machine types into power generators.

The EHFEM project currently focuses on converting a Precor EFX 561i elliptical machine into an effective power generating unit. Previous project teams developed a generator unit attached to the elliptical machine. This project scales the output voltage and current of the on-board generator using a DC-DC converter and feeds into an Enphase M175 Micro-Inverter to send AC power back to the electrical grid with minimum power conversion loss. An input protection system connects between the generator and DC-DC converter preventing transient voltage and current spikes from adversely damaging the DC-DC converter. This project seeks to implement an input protection scheme with a buck-boost DC-DC converter based on a LT3791-1 topology to improve upon the previously designed SEPIC topology and input protection system [2, 3].

The LT3791-1 accepts a maximum input voltage of 60V [4]. Any input exceeding this maximum threshold may adversely damage the controller. Therefore, an input protection system helps to prevent DC-DC converter damage during overvoltage transients exceeding 60V. A

modified version of the previous input protection system should apply a maximum of 60V to the DC-DC converter [2].

A previous SEPIC input protection system failure resulted in a catastrophic failure that damaged both the input protection circuit and SEPIC converter designed by Martin Kou [3]. The new input protection circuit must operate within 4.7V to 60V and protect against transient and sustained overvoltage events while allowing the DC-DC converter to remain operational.

Customer Needs Assessment

Overall, the EHFEM project targets users of Cal Poly's Recreational Center and aims to modify existing or newly installed elliptical machines with energy generating units. EHFEM altered elliptical machines effectively convert mechanical energy into electrical energy applied back to the electrical grid. The implementation of this project's Buck-Boost DC-DC converter and its input protection system must not alter the user's exercise experience or negatively impact their safety. It must also fit within the enclosure of the Precor EFX 561i elliptical machine in a way that resists damage resulting from vibration or water spilled on the enclosure. Additionally, the implemented system must properly function and connect, both physically and electrically, with the existing generator and Enphase M175 Micro-Inverter. The unit should also maintain a nominal life expectancy of at least 10 years with an average use of 18 hours per day and reach zero system lifecycle cost.

Chapter 3: Project Objectives

3.1. Requirements and Specifications

Subcomponent characteristics primarily influenced this project's overall requirements and specifications. Prior EHFEM subprojects and manufacturer-provided components defined design parameters. Previous converter design cost estimates aided in projecting this system's final cost. Required system inputs and outputs derive from output characteristics of the elliptical machine's generator and micro-inverter's input characteristics. Electrical specifications derive from Martin Kou's thesis, Ryan Turner's and Zack Weiler's senior projects, and component datasheets. Integrating banana-to-banana leads rather than soldered leads prevent potential broken contact points between the generator, converter, and micro-inverter. Marketing requirements derive from a customer needs assessment. Overall, the system must maintain a low cost, operate reliably and safely, and must couple with existing components while not altering the user's exercise experience when operating the elliptical machine. Table 3-1 summarizes project requirements and specifications.

Table 3-1: EHFEM DC/DC Converter with IPSC Requirements and Specifications

Marketing Requirements	Engineering Specifications	Justification
1	System and component costs must not exceed $300 per unit.	The previous input protection system's cost approximated $46.00. Furthermore, the previous SEPIC DC-DC converter design cost approximately $365.00. A proposed 18% cost reduction decreases total project expenses while maintaining or increasing functionality. [6] [7]

2, 3, 7	System must fulfill NEC, IEEE 1547, and NEMA electrical safety standards.	Must fulfill national standards for safe electrical and mechanical operation. National Electrical Code applies to electrical wiring and installation safety requirements. IEEE 1547 applies to inter-connections between generators and the power grid. NEMA applies to testing and operational safety standards. [5] [6] [7]
2, 3, 6	Must have an operational life of 65,700 hours without need of repair or replacement.	The system must operate a minimum of 10 years under normal use (18 hour per day), totaling approximately 33000 hours.
4	Input protection system must provide an overvoltage protection up to 150V.	Prior tests demonstrate the Precor elliptical trainer capable of generating voltage spikes over 100V, far above the maximum LT3791-1 input voltage [2]. Therefore implementing a protection system prevents component damage.
4	DC-DC converter must receive a maximum input voltage of 60V.	LT3791-1 accepts nominal input voltages ranging from 4.7V to 60V. Voltages excess of 60V may cause significant damage to the DC-DC converter [4].
4	DC-DC converter must supply less than 8A to the Enphase M175 Micro-Inverter.	The Enphase M175 Micro-Inverter's accepts a maximum input current of 8A [8]. Higher values may adversely damage the micro-inverter.
4	DC-DC converter must maintain 36V ± 5% output to the Enphase M175 Micro-Inverter.	The Enphase M175 Micro-Inverter must receive a 36V input to maintain peak power conversion efficiency [9].
4	System input and output connections must feature banana plugs.	All components must physically and electrically connect with each other. Readily removable or connectable banana-to-banana leads are more durable than soldered wire connection leads.
4, 5	System must fit within elliptical trainer's enclosure.	All components should fit within the elliptical trainer's enclosure to prevent user tampering.
5	System must have an operational input impedance of approximately 10 Ω.	The input impedance must remain 10Ω to preserve the user's exercise experience. Altering the input impedance alters the braking system's nominal resistance [2].
6	Circuit components must maintain ROHS compliance.	Promotes safe component disposal, thereby decreasing long-term harmful environmental impacts.

Marketing Requirements

1. Low cost
2. Reliable
3. Structurally durable
4. Compatible and easy to implement with existing components
5. Does not change the user's exercise experience
6. Environmentally sustainable
7. Conform to safety standards

The requirements and specifications table format derives from [10], Chapter 3.

Table 3-2: EHFEM DC/DC Converter with IPSC Deliverables

Delivery Date	Deliverable Description
Feb. 20, 2014	Cal Poly EE Department Design Review
Mar. 14, 2014	EE463 Report
Mar. 14, 2014	EE463 Demo Device(s)
May 23, 2014	EE464 Report
May 23, 2014	EE464 Demo Device(s)
May 30, 2014	ABET Sr. Project Analysis
May 30, 2014	Sr. Project Expo Poster

Chapter 4: Functional Decomposition

4.1. Level Zero Block Diagram

The level zero functional decomposition block diagram, shown in Figure 4-1, depicts a one input and one output system. This block receives an input DC power from the elliptical trainer's generator and scales its voltage up or down to output power rated at 36V to the Enphase Micro-Inverter.

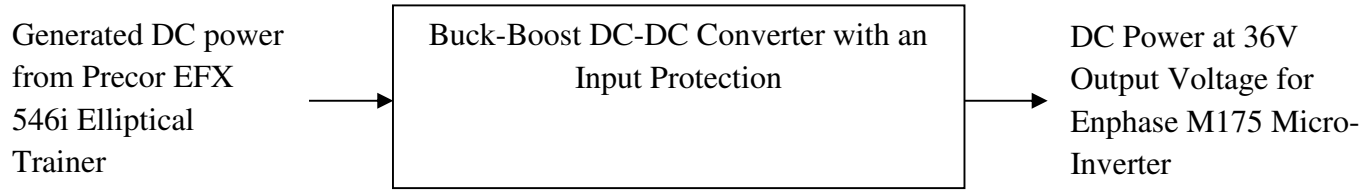

Figure 4-1: Level Zero Block Diagram

Table 4-1 Level Zero Block Diagram Functional Analysis

Input	• Generated DC power from EFX 546i Elliptical Trainer • 0V - 60V average depending on user's fitness and machine's resistance • 6A max input current at 10Ω input impedance
Output	• 36V ±5% Output Voltage for Enphase Micro-Inverter • 7.5A max output current
Functionality	Converts generated DC power from EFX 546i Elliptical Trainer to rated 36V applied to Enphase Micro-Inverter

4.2. Level One Block Diagram

The level one block diagram depicts three main system blocks with primary functionalities displayed in Figure 4-2. The DC-DC converter may require two controllers in parallel instead of one controller. Figure 4-2 also includes an input protection circuit, its feedback loop, and its system functionality.

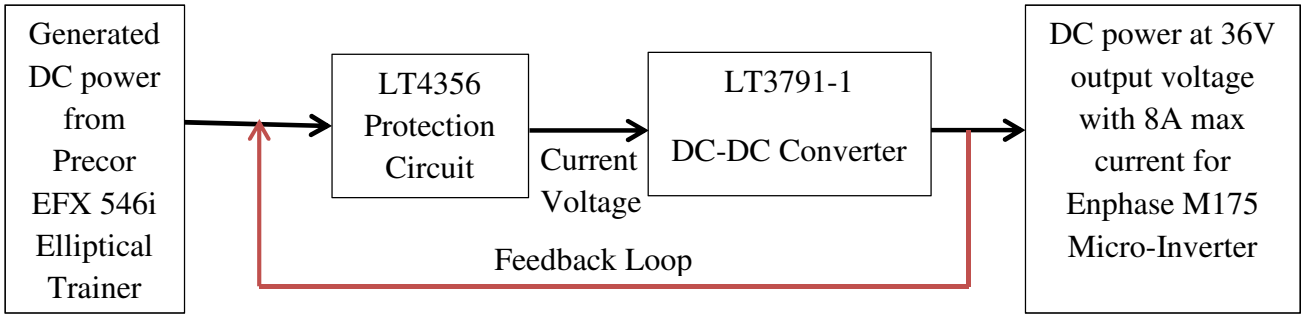

Figure 4-2: Level One Block Diagram

Table 4-2: Level One Block Diagram Protection Circuit Functional Analysis

Module	LT4356 Protection Circuit
Inputs	• Generated DC power from EFX 546i Elliptical Trainer • 0V - 60V average depending on user's fitness and machine's resistance
Outputs	• Regulated 60V and 6A max current at 10 Ω input impedance
Functionality	Surge stopper regulates system input voltage and current to 60V and 6.5A. Contains current sensing feedback loop from an input of Enphase Micro-Inverter to protection circuit to detect transient over-voltage events occurring at converter input. Also detects five minute start-up period of Enphase Micro-Inverter. When transient or five minute start-up period occurs, voltage builds up over the limit of the system and the protection circuit provides an alternate path for voltage and current to dissipate.

Table 4-3: Level One Block Diagram DC-DC Converter Circuit Functional Analysis

Module	LT3791-1 DC-DC Converter
Inputs	• Regulated 60V and 6A max current at 10 Ω input impedance
Outputs	• 36V ±5% output voltage for Enphase Micro-Inverter • 7.5A max output current
Functionality	Converts DC power provided from protection circuit to power rated at 36V that the Enphase Micro-Inverter can invert to 240V RMS AC power. Controller regulates the output voltage and current output.

Chapter 5: Project Planning

5.1. Initial Gantt Chart

Figure 5-1: Estimated Project Gantt Chart

Figure 5-1**Error! Reference source not found.** depicts this project's estimated Gantt Chart during EE460, EE463, and EE464. Fall 2013 covers EE460 and lists course deliverables. Winter 2014 depicts an initial system design phase, not including an academic winter break. Initial system design occurs over five weeks with time allocated for revisions and faculty advisor design confirmation. Two further design and confirmation phases ensure proper circuit design before ordering, building, and testing a prototype. Parts selection occurs throughout the first two design processes with a two week buffer accommodating purchasing and shipping a finalized parts list. Three additional weeks provide adequate time for prototype construction. Prototype testing occurs during a period two weeks prior and two weeks after an academic spring break. Implementing further design revision and part purchasing stages over the course of five weeks prepare for the final circuit design. An initial Project Report V1 is due the last day of EE463 at the end of Winter Quarter. The final design and Project Report V2 are due on May 23rd, the end of Spring Quarter's 8th week of instruction. Documentation occurs throughout design, prototype, and test phases.

5.2. Predicted Cost Estimate

Approximately 2 LT3791-1 ICs maintain the previous SEPIC DC-DC power output capacity of 288W. Each IC costs approximately $7.50, totaling a minimum of $22.50. A modified version of Ryan Turner and Zach Weiler's DC-DC Converter Input Protection System project serves as the input protection system [2]. Their system cost $46.43 including various components. Further appropriation of funds considers the cost of the converter and input protection circuit PCBs in addition to component costs for the DC-DC converter schema itself.

Optimistically, the full design, implementation, and testing of this project requires 150 hours in addition to best-case component costs.

Nominally, aside from the previously estimated costs of the LT3791-1 ICs and input protection system, the DC-DC converter and PCB manufacturing may cost higher than expected. An additional $85.00 considers shipping and handling, not including component costs. Nominally, the full design, implementation, and testing of this project requires 200 man hours.

Pessimistically, the full design, implementation, and testing of this project requires 400 hours in addition to the cost for additional misplaced or damaged parts. Our pessimistic estimation also considers multiple iterations of the project.

<table>
<tr><th>Costs</th><th>Optimistic</th><th>Most Likely</th><th>Pessimistic</th><th>Estimated</th></tr>
<tr><td>Total Component (Fixed)
<table>
<tr><th>Component</th><th>Cost</th></tr>
<tr><td>LT 3791</td><td>$ 22.50</td></tr>
<tr><td>LT 4356</td><td>$ 8.49</td></tr>
<tr><td>IPSC and
DC-DC converter hardware</td><td>$ 70-90</td></tr>
<tr><td>Converter PCB</td><td>$ 100-300</td></tr>
<tr><td>Protection Circuit PCB</td><td>$ 5-80</td></tr>
<tr><td>LT3791-1 Controller</td><td>$ 10-20</td></tr>
<tr><td>Total Component Cost</td><td>Min = $ 215.99
Max = $ 520.56</td></tr>
</table></td><td>$215.00</td><td>$300</td><td>$520.00</td><td>$272.50</td></tr>
<tr><td>Total Labor (Variable)
$16 per hour</td><td>$2,400.00
150 Hrs</td><td>$3,200.00
200 Hrs</td><td>$6,400.00
400 Hrs</td><td>$3600.00</td></tr>
<tr><td>Total Cost</td><td></td><td></td><td></td><td>$3,872.50</td></tr>
</table>

Figure 5-2: Project Cost Estimates

Chapter 6: Previous Buck-Boost Converter Design Discussions

6.1. Alvin Hilario Four Switch Topology

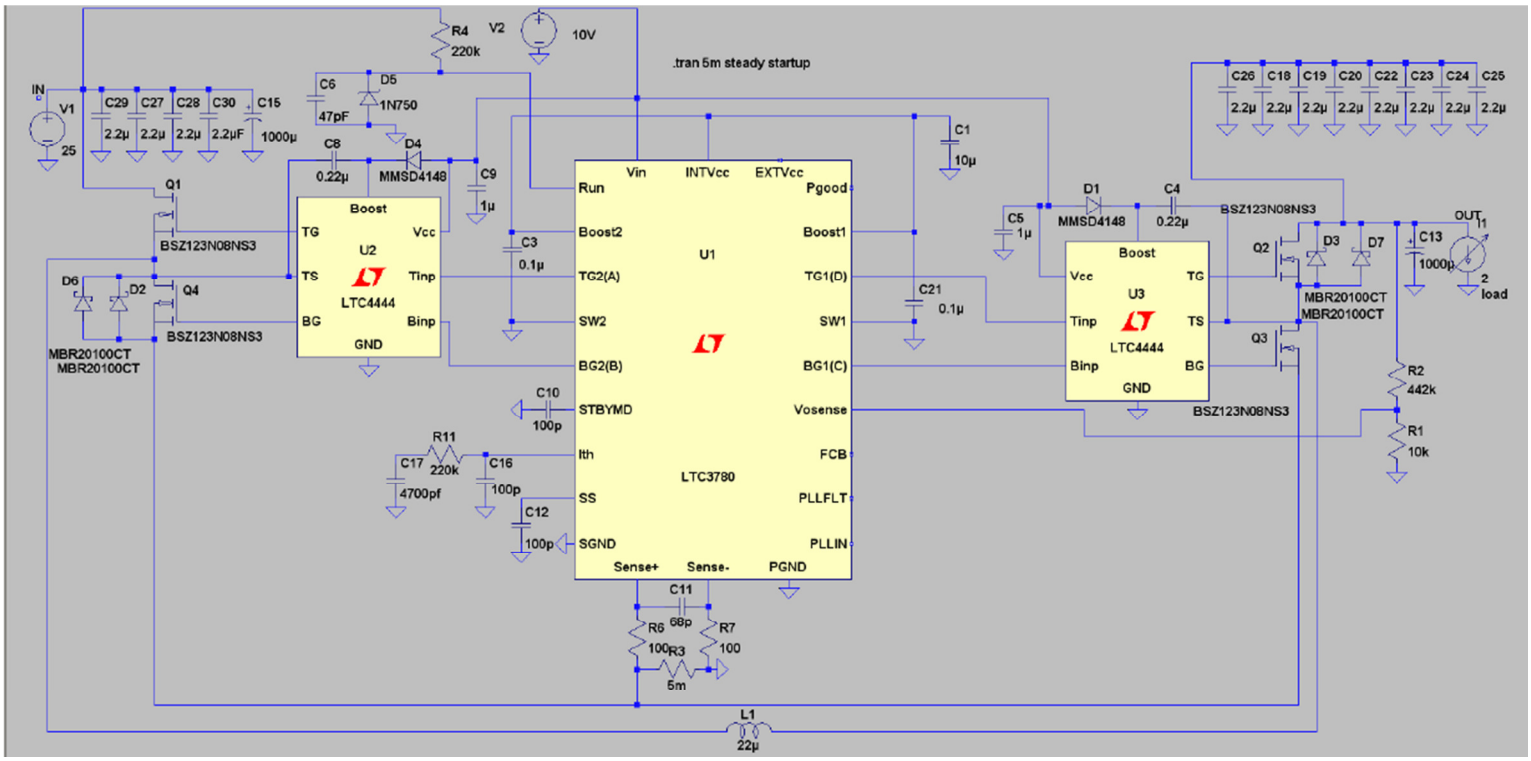

Figure 6-1: Alvin Hilario's Four-Switch Buck-Boost DC-DC Converter Design [9]

Alvin Hilario's Four-Switch Buck-Boost DC-DC converter design, Figure 6-1, utilizes two LT3780 High-Efficiency, Synchronous, 4-Switch Buck-Boost Controllers and an LTC4444 High Voltage Synchronous N-Channel MOSFET Driver. LT3780 PWM controls two LTC4444s, each of which control four NMOS switches connected to the power inductor. Hilario's design operates within a 5V to 52V input voltage range with 94.07% average power efficiency. Worst-case 68.84% power efficiency occurred at a 5V converter input. The inverter's worst output voltage ripple reaches 380mV, or 1.05%. His converter design cost roughly $80 including a custom-made PCB board. Hilario noted that the microinverter's inability to mimic a constant resistance and tends to draw too much current from the converter, thereby deregulating its intended 36V output.

6.2. Martin Kou SEPIC Topology

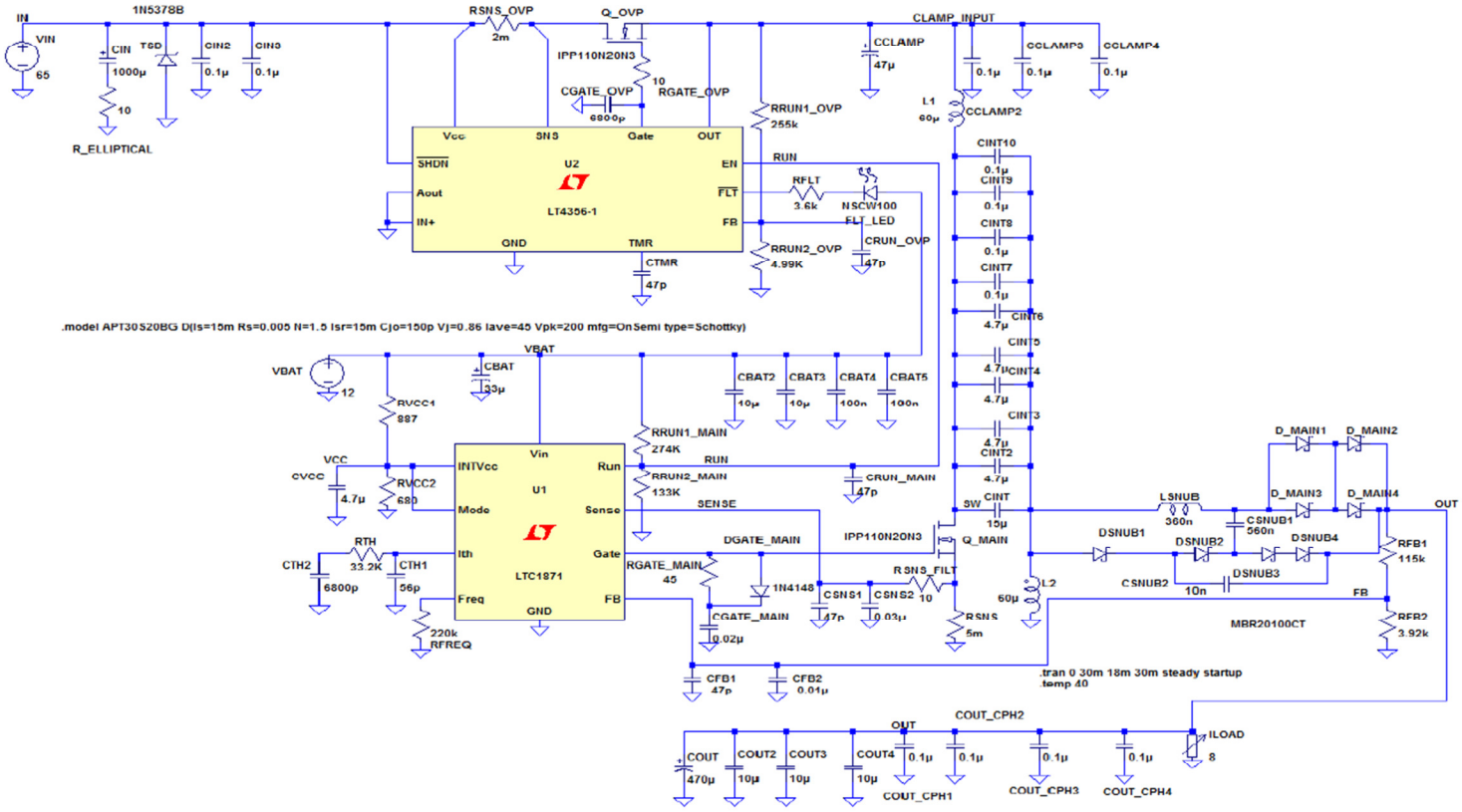

Figure 6-2: Martin Kou's SEPIC DC-DC Converter Design [3]

Martin Kou designed the Single Ended Primary Inductor Converter topology depicted in Figure 6-2. A SEPIC design controls energy exchange between coupling capacitors and switching inductors using a NMOS switch. Kou's SEPIC design attained 78.3% converter power efficiency at a 60V input and accepts an input range of 8V to 60V. Kou's project obtained a maximum of 78.7% power efficiency at a 50V input. Kou's SEPIC design does not feature a current limiter and uses fuses between the converter's output and inverter's input. Kou's SEPIC design cost $404.99.

6.3. LT3791-1 Design Parameterization

Operational Enphase M175-24-240 Micro-Inverter's and elliptical machine's generator characteristics limit input and output characteristics of the proposed DC-DC converter. Alvin Hilario previously characterized the Enphase Micro-Inverter's maximum 87.10% operating power efficiency at a 36V input voltage. Therefore, the converter's output voltage must regulate 36V for maximum micro-inverter efficiency. Furthermore, the micro-inverter accepts an 8A maximum input current [8]. However, the DC-DC converter should limit the microinverter input current to 7.5A or lower to prevent microinverter damage. The microinverter accepts 270W maximum at a regulated 36V and 7.5A input current. Sections 7.3 and 7.4 describe output current and voltage programming.

The elliptical machine's generator supplies power across a 10Ω resistor and provides a maximum 360W power output at 60V. Assuming maximum efficiency, where $P_{IN} = P_{OUT}$, the DC-DC Converter design handles up to 270W with a 52V input. Therefore, knowing $P = \frac{V^2}{R}$, the maximum input voltage to the system approximates 52V. Setting an overvoltage limit using a resistive voltage divider at the OVLO pin as described in Section 7.7 ceases device operation above a 51V input. Triggering an overvoltage event shuts off and resets the converter and ceases power MOSFET switching. An input protection system should divert converter input power when the converter is non-operational.

Chapter 7: LT3791-1 Topology Component Selection Overview

7.1. Block Diagram

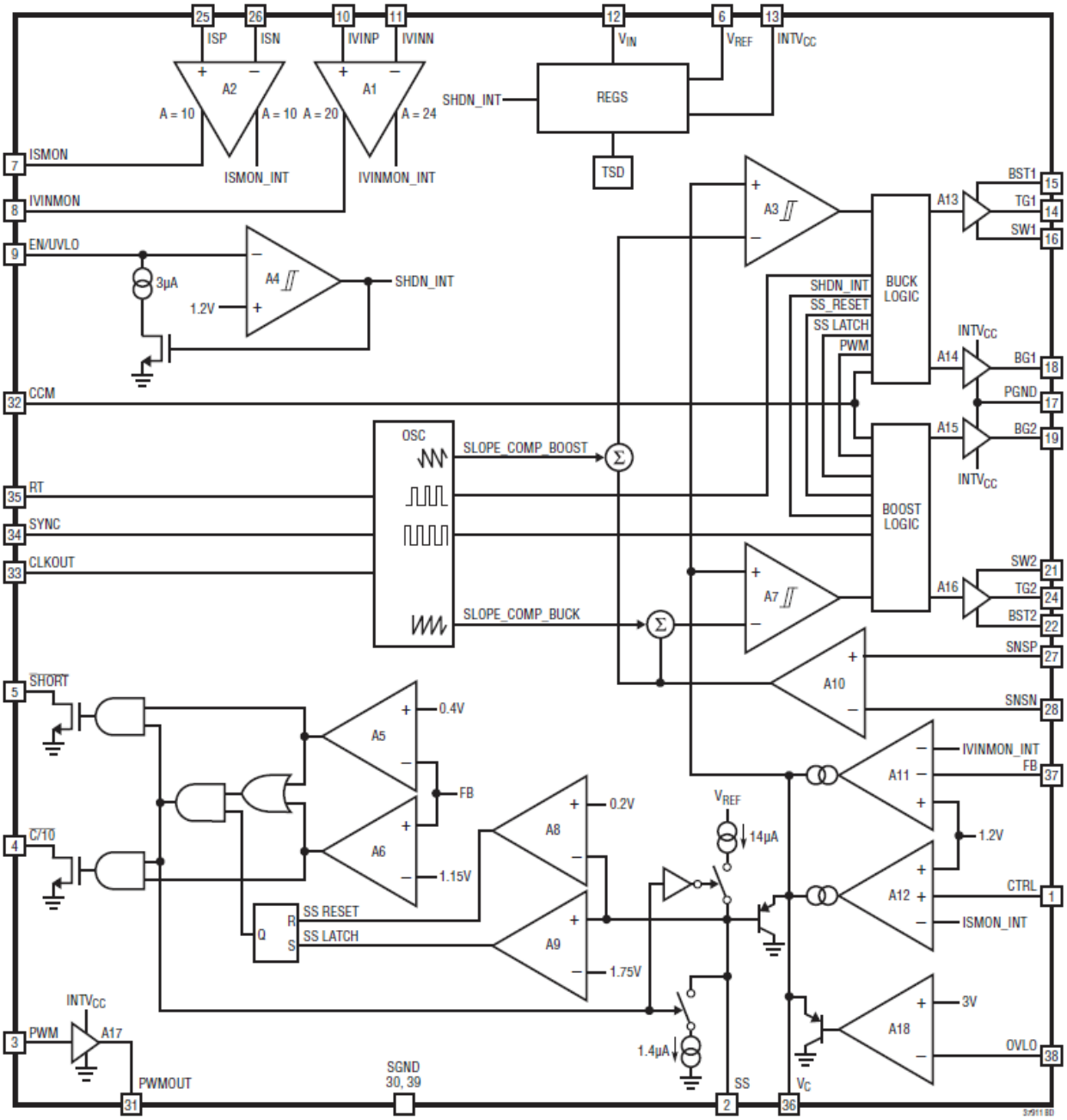

Figure 7-1: LT3791-1 Buck Boost 4-Switch Buck-Boost Controller Block Diagram [4]

This controller provides an output voltage above,

IVINP and IVINN pins detect current through the

7.2. Programing Switching Frequency using RT Pin

The LT3791-1 controller features a programmable

A resistor, R_T, connecting RT to ground

Figure 7-2 and

Figure 7-3 display the relationship between R_T and switching frequency values. Selecting a 400 kHz switching frequency and 59kΩ R_T value provides an arbitrary median between power efficiency and component sizes offered by the LT3791-1 controller.

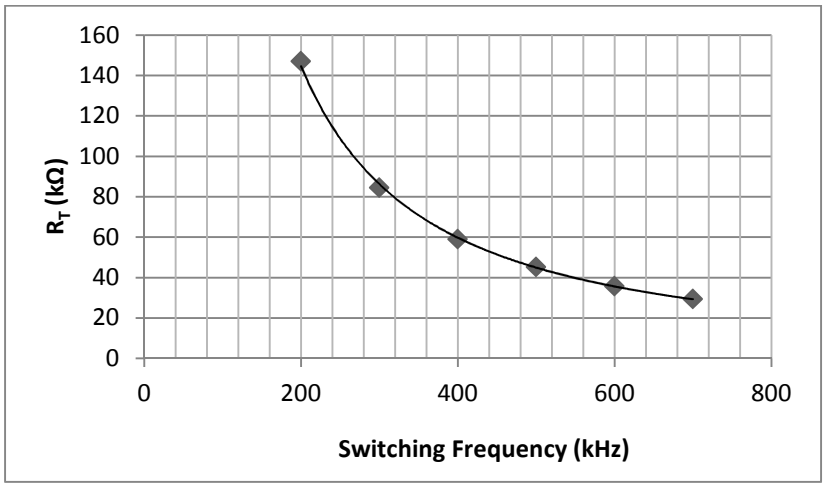

Figure 7-2: Programmable LT3791-1 R_T resistor values and switching frequency plot

Table 1. Switching Frequency vs R_T Value

f_{OSC} (kHz)	R_T (kΩ)
200	147
300	84.5
400	59.0
500	45.3
600	35.7
700	29.4

Figure 7-3: R_T vs. f_{OSC}, programmable switching frequency [4]

7.3. Programming Output Current using R_{OUT}

Placing R_{OUT} in series with the output load programs the converter's maximum output current. ISP and ISN pins sense the voltage drop across R_{OUT} while V_{CTRL} sets a $V_{(ISP-ISN)}$ threshold. Figure 7-4 lists typical $V_{(ISP-ISN)}$ thresholds versus V_{CTRL}. When V_{CTRL} > 1.3V, the $IOUT=100mVROUT$ (7.3-2). V_{CTRL} tied to $INTV_{CC}$ sets $V_{(ISP-ISN)}$ to 100mV.

Two LT3791-1 controllers evenly split supplied output current. Therefore, each controller requires one R_{OUT}. Initially, a 7.5A output load current resulted in a 0.0267Ω R_{OUT} value, thereby

outputting 3.75A per controller. However, an equivalent current sense resistor was not available, so R_{OUT} was selected as the next-nearest value of 0.027 Ω. Selecting R_{OUT} as 0.027Ω sets the $IOUT=100mVROUT$ (7.3-2). Each controller provides the load with 3.7A or a maximum 7.4A output current. Therefore, the load may receive a maximum power of 266.4W provided a 7.4A I_{OUT} and 36V V_{OUT} as programmed by R_{OUT} and FB pin feedback voltage.

V_{CTRL} (V)	$V_{(ISP-ISN)}$ (mV)
1.1	90
1.15	94.5
1.2	98
1.25	99.5
1.3	100

Figure 7-4: Output current selection, V_{CTRL} vs $V_{(ISP-ISN)}$ [4]

$$I_{OUT} = \frac{V_{CTRL}-200mV}{R_{OUT}*10} \quad (7.3\text{-}1)$$

$$I_{OUT} = \frac{100mV}{R_{OUT}} \quad (7.3\text{-}2)$$

Equation $IOUT=\frac{V_{CTRL}-200mV}{R_{OUT}*10}$ (7.3-1) determines maximum output current of a single device when the CTRL pin voltage pulls less than 1V. Equation $IOUT=\frac{100mV}{R_{OUT}}$ (7.3-2) determines maximum output current when the CTRL pin voltage pulls above 1.3V.

Intermediate V_{CTRL} values noted in Figure 7-4 replace the 100mV in Equation $IOUT=\frac{100mV}{R_{OUT}}$ (7.3-2) with corresponding $V_{(ISP-ISN)}$ values.

7.4. Programming Output Voltage using FB Pin

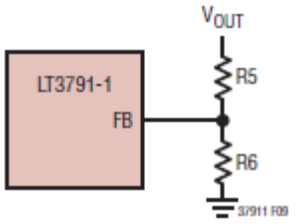

Figure 7-5: FB Pin output voltage divider [4]

A resistive voltage divider provides a 1.2V feedback to the FB pin when the output reaches the desired output voltage. Initially, R5 and R6 were selected as 200kΩ and 6.9kΩ, thereby programming an 35.98V output voltage. However, equivalent valued resistors lacked stock in Digikey and Mouser's databases, so R5 and R6 were selected as the next-nearest values of 196kΩ and 6.81kΩ. These values program the output voltage to 35.73V, well within the 5% tolerance of the 36V design requirement, Equation $VOUT = 1.2V * \frac{196k\Omega + 6.81k\Omega}{6.81k\Omega} = 35.737V$ (7.4-2).

$$V_{OUT} = 1.2 * \frac{R_5 + R_6}{R_6} \quad (7.4\text{-}1)$$

$$V_{OUT} = 1.2V * \frac{196k\Omega + 6.81k\Omega}{6.81k\Omega} = 35.737V \quad (7.4\text{-}2)$$

7.5. Inductor Selection

Equations $LBUCK > \frac{V_{OUT} * (V_{IN(MAX)} - V_{OUT}) * 100}{f * I_{OUT(MAX)} * \%Ripple * V_{IN(MAX)}}$ (7.5-1) and $LBOOST > \frac{V_{IN(MIN)}^2 (V_{OUT} - V_{IN(MIN)}) * 100}{f * I_{OUT(MAX)} * \%Ripple * V_{OUT}^2}$ (7.5-2) specify inductor sizing.

$$L_{BUCK} > \frac{V_{OUT} * (V_{IN(MAX)} - V_{OUT}) * 100}{f * I_{OUT(MAX)} * \%Ripple * V_{IN(MAX)}} \quad (7.5\text{-}1)$$

$$L_{BOOST} > \frac{V_{IN(MIN)}^2 (V_{OUT} - V_{IN(MIN)}) * 100}{f * I_{OUT(MAX)} * \%Ripple * V_{OUT}^2} \quad (7.5\text{-}2)$$

Inductor sizing depends upon variables including: output voltage V_{OUT}, switching frequency f, allowable inductor current ripple %Ripple, minimum input voltage $V_{IN(MIN)}$, maximum input voltage $V_{IN(MAX)}$, and maximum output load current $I_{OUT(MAX)}$. %Ripple was estimated as 20% to 40% of the output current values as noted by Design Calculations for Buck-Boost Converters by Michael Green of Texas Instruments [11].

Table 7-1 Inductor selection base parameters

$V_{IN(MIN)}$ [V]	$V_{IN(MAX)}$ [V]	V_{OUT} [V]	f [kHz]	$I_{OUT(MAX)}$ [A]	% Ripple [%]
5 V	51 V	36 V	400 kHz	3.7 A	30 %

Programmable undervoltage and overvoltage limits set in Section 7.7 determine $V_{IN(MIN)}$ and $V_{IN(MAX)}$. A 36V V_{OUT} is the optimal Enphase M175-24-240 Micro-Inverter input voltage as measured by previous project groups. Sections 7.2 and 7.3 indicate programming output current as 3.7A and switching frequency to 400 kHz. % Ripple was arbitrarily selected as a 30% inductor ripple current in respect to $I_{OUT(MAX)}$. Table 7-2 calculates a minimum inductor value based on the values in Table 7-1 variables.

Table 7-2: Minimum inductance value calculations

Calculation of minimum L_{BUCK}	**Calculation of minimum L_{BOOST}**
$> \frac{V_{OUT} * (V_{IN(MAX)} - V_{OUT}) * 100}{f * I_{OUT(MAX)} * \%Ripple * V_{IN(MAX)}}$ $> \frac{(36V) * (51V - 36V) * 100}{400{,}000\,Hz * 3.7A * 30\% * 51V}$ $L_{BUCK} > 23.847\ \mu H$	$> \frac{V_{IN(MIN)}^2 (V_{OUT} - V_{IN(MIN)}) * 100}{f * I_{OUT(MAX)} * \%Ripple * V_{OUT}^2}$ $> \frac{(5V)^2 (36V - 5V) * 100}{400{,}000Hz * 3.7A * 30\% * (36V)^2}$ $L_{BOOST} > 1.35\ \mu H$

Table 7-2: Minimum inductance value provides calculations showing that inductor size must exceed $23.847\ \mu H$. Selecting an Abracon AIRD-03-270K inductor rated at $27\mu H$ with a $\pm 10\%$ tolerance, 3.5A current rating, 23A saturation current, and a maximum $12m\Omega$ DCR meets this requirement. The Abracon AIRD-03-270K was the only inductor available and in-stock at Digikey or Mouser with specifications closest to the minimum inductor value of $23.847\mu H$ and a high current saturation rating.

7.6. R_{SENSE} and Maximum Output Current Selection

The required output current of the device determines inductor current sense resistor, R_{SENSE}, selection. Selecting an R_{SENSE} value determines maximum peak or valley current in boost or buck operation. LT3791-1's datasheet provides Equations

REF _Ref383771969 \h * MERGEFORMAT $L_{BOOST} > \frac{V_{IN(MIN)}^2 (V_{OUT} - V_{IN(MIN)}) * 100}{f * I_{OUT(MAX)} * \%Ripple * V_{OUT}^2}$ (

$IOUT\,MAXBOOST = 51mV RSENSE - \Delta IL2 * VINMIN VOUT$ (7.6-1) and

$IOUT\,MAXBUCK = (47.5mV RSENSE + \Delta IL2)$ (7.6-2).

$$I_{OUT(MAX_{BOOST})} = \left(\frac{51mV}{R_{SENSE}} - \frac{\Delta I_L}{2}\right) * \left(\frac{V_{IN(MIN)}}{V_{OUT}}\right) \quad (7.6\text{-}1)$$

$$I_{OUT(MAX_{BUCK})} = \left(\frac{47.5mV}{R_{SENSE}} + \frac{\Delta I_L}{2}\right) \quad (7.6\text{-}2)$$

$IOUT\,MAXBOOST = 51mV RSENSE - \Delta IL2 * VINMIN VOUT$ (7.6-1) and

$IOUT\,MAXBUCK = (47.5mV RSENSE + \Delta IL2)$ (7.6-2) equates to Equations

$RSENSE\,MAXBOOST = 2 * 51mV * VINMIN2 * IOUT * VOUT + \Delta ILBOOST * VINMIN$

$RSENSE\,MAXBUCK = 2 * 47.5mV2 * IOUT - \Delta IL(BUCK)$ (7.6-4) to solve for maximum R_{SENSE} values. R_{SENSE} ranges from 20% to 30% lower than the maximum calculated value as denoted by LT3791-1's datasheet.

$$R_{SENSE(MAX)_{BOOST}} = \frac{2*51mV*V_{IN(MIN)}}{2*I_{OUT}*V_{OUT}+\Delta I_{L(BOOST)}*V_{IN(MIN)}} \quad (7.6\text{-}3)$$

$$R_{SENSE(MAX)_{BUCK}} = \frac{2*47.5mV}{2*I_{OUT}-\Delta I_{L(BUCK)}} \quad (7.6\text{-}4)$$

Table 7-3: R_{SENSE} selection base parameters

$V_{IN(MIN)}$ [V]	$V_{IN(MAX)}$ [V]	V_{OUT} [V]	f [kHz]	I_{OUT} [A]	% Ripple [%]	ΔI_L [A]
5 V	51 V	36 V	400 kHz	3.7 A	30 %	1.05 A

Table 7-4: Maximum R_{SENSE} value calculations

Calculation of $R_{SENSE(MAX)_{BOOST}}$	**Calculation of $R_{SENSE(MAX)_{BUCK}}$**
$< \frac{2 * 51mV * V_{IN(MIN)}}{2 * I_{OUT} * V_{OUT} + \Delta I_{L(BOOST)} * V_{IN(MIN)}}$ $< \frac{2 * 51mV * 5V}{2 * 3.7A * 36V * 1.05\text{A} * 5V}$ $R_{SENSE} < 0.001863\ \Omega$	$< \frac{2 * 47.5mV}{2 * I_{OUT} - \Delta I_{L(BUCK)}}$ $< \frac{2 * 47.5mV}{2 * 3.7A - 1.05\text{A}}$ $R_{SENSE} < 0.016\ \Omega$

R_{SENSE} must equal less than 1.6mΩ as calculated in Table 7-4: Maximum RSENSE value. Selecting a 1.5mΩ R_{SENSE} satisfies these requirements. LT3791-1's datasheet recommends R_{SENSE} 20% to 30% lower than its maximum calculated R_{SENSE} value in either buck or boost mode, however 1mΩ is the next available lowest current sense resistor value.

7.7. Programming V_{IN} Undervoltage and Overvoltage Limits

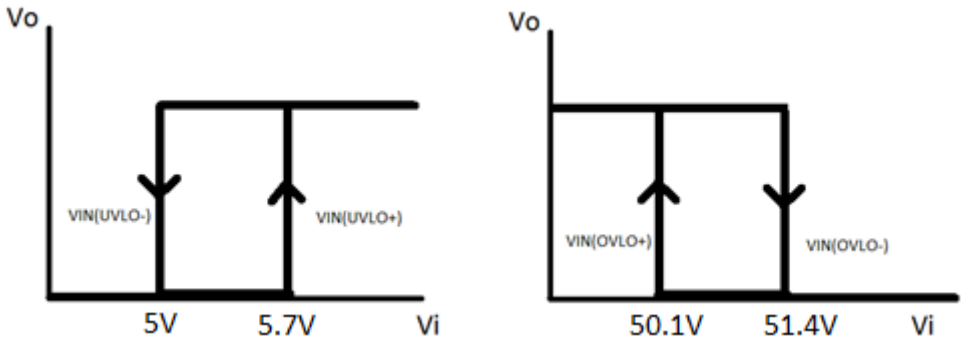

Figure 7-6: Undervoltage and overvoltage condition hysteresis windows

LT3791-1's EN/UVLO pin doubles as an enable control pin and undervoltage condition sensor. A resistor voltage divider sets a typical 1.2V at the EN/UVLO pin. Input bias current to EN/UVLO remains sub-μA while above 1.2V. Feedback below 1.2V enables a 3μA pull-down current so the user can define a rising hysteresis. Triggering an undervoltage condition resets the system's soft-start. A resistive divider on the OVLO pin sets an overvoltage condition. Triggering an overvoltage condition causes the controller to cease switching and resets the system's soft-start.

$VIN\,UVLO{-}{=}1.2{*}R1{+}R2R2$ (7.7-1) and

$VIN\,UVLO{+}{=}3\mu A{*}R1{+}1.215{*}R1{+}R2R2$ (7.7-2) set undervoltage falling and rising edge

$VIN(OVLO{-}){=}3{*}R3{+}R4R4$ (7.7-3) and $VIN\,OVLO{+}{=}2.925{*}R3{+}R4R4$ (7.7-4) set overvoltage falling and rising edge conditions. Figure 7-6: Undervoltage and overvoltage condition depicts undervoltage and overvoltage hysteresis windows.

$$V_{IN(UVLO^-)} = 1.2 * \frac{R_1+R_2}{R_2} \quad (7.7\text{-}1)$$

$$V_{IN(UVLO^+)} = 3\mu A * R_1 + 1.215 * \frac{R_1+R_2}{R_2} \quad (7.7\text{-}2)$$

$$V_{IN(OVLO^-)} = 3 * \frac{(R_3+R_4)}{R_4} \quad (7.7\text{-}3)$$

$$V_{IN(OVLO^+)} = 2.925 * \frac{R_3+R_4}{R_4} \quad (7.7\text{-}4)$$

Table 7-5: Undervoltage and overvoltage rising/falling hysteresis equations

$V_{IN(UVLO^-)}[V]$	5.071 V
$V_{IN(UVLO^+)}[V]$	5.734 V
$V_{IN(OVLO^-)}[V]$	51.387 V

$V_{IN(OVLO^+)}[V]$	50.102 V

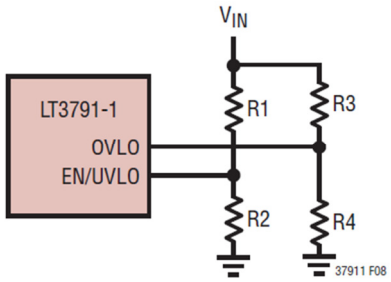

Figure 7-7: Overvoltage and undervoltage resistive voltage dividers [4]

Selecting R_1 and R_3 as 200k, and R2 and R4 as 62k and 12.4k, sets the falling and rising hysteresis conditions shown Table 7-5. Undervoltage and overvoltage limits set the maximum operating range to approximately 5.7V to 51V, well within the maximum 4.7V to 60V operating range of the LT3791-1 controller. A 51.4V maximum voltage limit allows a 275.625W maximum input power since the converter can output a maximum of 270W to the inverter given 36V and 7.5A output specifications as described in Section 6.3.

7.8. Programming Input Current Limit

Placing an input current sense resistor, R_{IN}, between pins IVINN and IVINP programs an input current limit. Using Equation (7.8-1), a 10mΩ resistor programs the input current limit to 4.2A. Each device should accept less than 2.5A knowing that a 50V input supplies up to 5A across a 10Ω resistance. The device switches from constant-voltage mode to constant-current mode when voltage across R_{IN} reaches 50mV. If the voltage across R_{IN} exceeds 50mV, then the

device decreases the amount of current delivered to the output, thereby regulating the current sense voltage to 50mV.

$$I_{IN} = \frac{50mV}{R_{IN}} \quad (7.8\text{-}1)$$

R_{IN} (mΩ)	I_{LIMIT} (A)
20	2.5
15	3.3
12	4.2
10	5.0
6	8.3
5	10.0
4	12.5
3	16.7
2	25

Figure 7-8: Input Current Limit vs R_{IN} [4]

7.9. Programming Soft-Start

Programmable soft-start reduces input power current surges by gradually increasing the controller's input current limit. Defining a soft-start capacitor, C_{SS}, in Equation $tss = \frac{1.2V}{14\ \mu A} * C_{ss}$ (7.9-1) sets soft-start time. A 33nF soft-start capacitor provides a soft-start interval of 2.8ms. A 100kΩ resistor placed in series between the soft-start capacitor and V_{REF} contributes extra soft-start charging current. LT3791-1's datasheet recommends a minimum soft-start value of 22nF.

$$t_{ss} = \frac{1.2V}{14\ \mu A} * C_{ss} \quad (7.9\text{-}1)$$

7.10. Power MOSFET Consideration

Each LT3791-1 requires four external power NMOS devices to control the charging and discharging phases of the power inductor during converter operation. $INTV_{CC}$ limits gate drive voltage to 5V, thus suggesting use of logic-level threshold MOSFET. Linear Technology's sample circuits in LT3791-1's datasheet specified Renesas RJK0651DPB NMOS devices as starting power MOSFETS. Initially MOSFET selection included the RJK0651DPB. However, distributors ran out of stock during the late-design phase, and Infineon's IPP230N06L3G NMOS was selected as an alternate [12].

Infineon's IPP230N06L3G features a 60V drain-source breakdown voltage, a typical 1.7V gate-threshold voltage, a low 16pF reverse transfer capacitance, and a low 23mΩ on-resistance. Specifically, low reverse capacitance, C_{RSS}, low on-resistance, $R_{DS(ON)}$, minimize switching losses.

The converter's design specifies a 400 kHz switching frequency or 2.5µs switching period. IPP230N06L3G's datasheet specifies 9ns turn-on and 19ns turn-off delays. Therefore the RJK0651DPB switches fast enough and accommodates a 400 kHz switching frequency.

$$P_{M1(BOOST)} = \left(\frac{I_{OUT}*V_{OUT}}{V_{IN}}\right)^2 * \rho_T * R_{DS(ON)} \quad (7.10\text{-}1)$$

$$P_{M2(BUCK)} = \frac{V_{IN}-V_{OUT}}{V_{IN}} * I_{OUT}^2 * \rho_T * R_{DS(ON)} \quad (7.10\text{-}2)$$

$$P_{M3(BOOST)} = \frac{(V_{OUT}-V_{IN})*V_{OUT}}{V_{IN}^2} * I_{OUT}^2 * \rho_T * R_{DS(ON)} + \frac{k*V_{OUT}^3*I_{OUT}*C_{RSS}*f}{V_{IN}} \quad (7.10\text{-}3)$$

$$P_{M4(BOOST)} = \frac{V_{IN}}{V_{OUT}} * \left(\frac{I_{OUT}*V_{OUT}}{V_{IN}}\right)^2 * \rho_T * R_{DS(ON)} \quad (7.10\text{-}4)$$

LT3791-1's datasheet specifies Equations $PM1BOOST=\left(\frac{I_{OUT}*V_{OUT}}{V_{IN}}\right)^2 * \rho_T * R_{DS(ON)}$

$PM4(BOOST)=VINVOUT*IOUT*VOUTVIN2*\rho T*RDSON$ (7.10-4) to determine maximum power dissipation at maximum output current. Normalization factor, ρ_T, accounts for varying $R_{DS(ON)}$ with temperature changes, as shown in Figure 7-9, at a rate of 0.4%/°C. A maximum

junction temperature of 125°C uses a ρ_T of 1.5. The constant k accounts for losses caused by reverse-recovery current and has an empirical value of 1.7. Low $R_{DS(ON)}$ and C_{RSS} devices minimize maximum power dissipation per MOSFET.

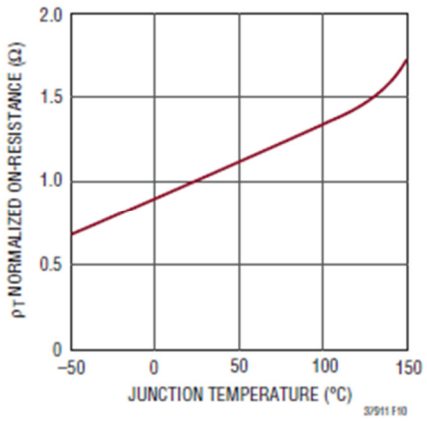

Figure 7-9: Normalized $R_{DS(ON)}$ vs. Temperature, [4]

Table 7-6: Power MOSFET selection base specifications

V_{IN} [V]	V_{OUT} [V]	f [kHz]	I_{OUT} [A]	$R_{DS(ON)}$ [Ω]	C_{RSS} [pF]	$\rho_{T(MAX)}$	k
5V-	36 V	400	3.7 A	23	16 pF	1.5	1.7

REF _Ref384161742 \h * MERGEFORMAT $PM1BOOST = \left(\frac{I_{OUT} * V_{OUT}}{V_{IN}}\right)^2 * \rho_T * R_{DS(ON)}$

PM4(BOOST)=VINVOUT∗IOUT∗VOUTVIN2∗ρT∗RDSON (7.10-4, using

V IN [V]	VOUT [V]	f [kHz]	IOUT [A]	$RDS_{(ON)}$ [Ω]	CRSS [pF]	$\rho_{T(MAX)}$	k
5V-51.4	36 V	400	3.7 A	23 mΩ	16 pF	1.5	1.7

Table 7-6's variables, calculates each switch's maximum power during buck and boost mode. Table 7-7: Maximum MOSFET power dissipation calculation displays calculated power dissipation results.

Table 7-7: Maximum MOSFET power dissipation calculation

$P_{M1(BOOST)} = \left(\frac{I_{OUT}*V_{OUT}}{V_{IN}}\right)^2 * \rho_T * R_{DS(ON)}$ $P_{M1(BOOST)} = \left(\frac{3.7A*36V}{5V}\right)^2 * 1.5 * 23m\Omega$ $\boldsymbol{P_{M1(BOOST)} = 26.5W}$
$P_{M2(BUCK)} = \frac{V_{IN}-V_{OUT}}{V_{IN}} * I_{OUT}^2 * \rho_T * R_{DS(ON)}$ $P_{M2(BUCK)} = \frac{51.4V-36V}{51.4V} * (3.7A)^2 * 1.5 * 23m\Omega$ $\boldsymbol{P_{M2(BUCK)} = 0.164W}$
$P_{M3(BOOST)} = \frac{(V_{OUT}-V_{IN})*V_{OUT}}{V_{IN}^2} * I_{OUT}^2 * \rho_T * R_{DS(ON)} + \frac{k*V_{OUT}^3*I_{OUT}*C_{RSS}*f}{V_{IN}}$ $P_{M3(BOOST)} = \frac{(36V-5V)*36V}{(5V)^2} * (3.7A)^2 * 1.5 * 23m\Omega + \frac{1.7*(36V)^3*3.7A*16pf*400kHz}{5V}$ $\boldsymbol{P_{M3(BOOST)} = 23.219W}$
$P_{M4(BOOST)} = \frac{V_{IN}}{V_{OUT}} * \left(\frac{I_{OUT}*V_{OUT}}{V_{IN}}\right)^2 * \rho_T * R_{DS(ON)}$ $P_{M4(BOOST)} = \frac{5V}{36V} * \left(\frac{3.7A*36V}{5V}\right)^2 * 1.5 * 23m\Omega$ $\boldsymbol{P_{M4(BOOST)} = 3.682W}$

7.11. Controller Syncing

LT3791-1 features clock syncing operates two parallel devices using CLKOUT and SYNC pins. The CLKOUT pin provides a 180^o out-of-phase square waveform at the switching frequency set by R_T in Section 7.2. The primary controller's CLKOUT connects to the secondary controller's SYNC pin with the primary controller's SYNC pin grounded. Connecting CLKOUT and SYNC generates a parallel two-phase converter, allowing each converter to split the total output load current while decreasing output ripple voltage. Two synchronized converters regulate 36V at 3.7A per device rather than one converter supplying 36V and 7.4A.

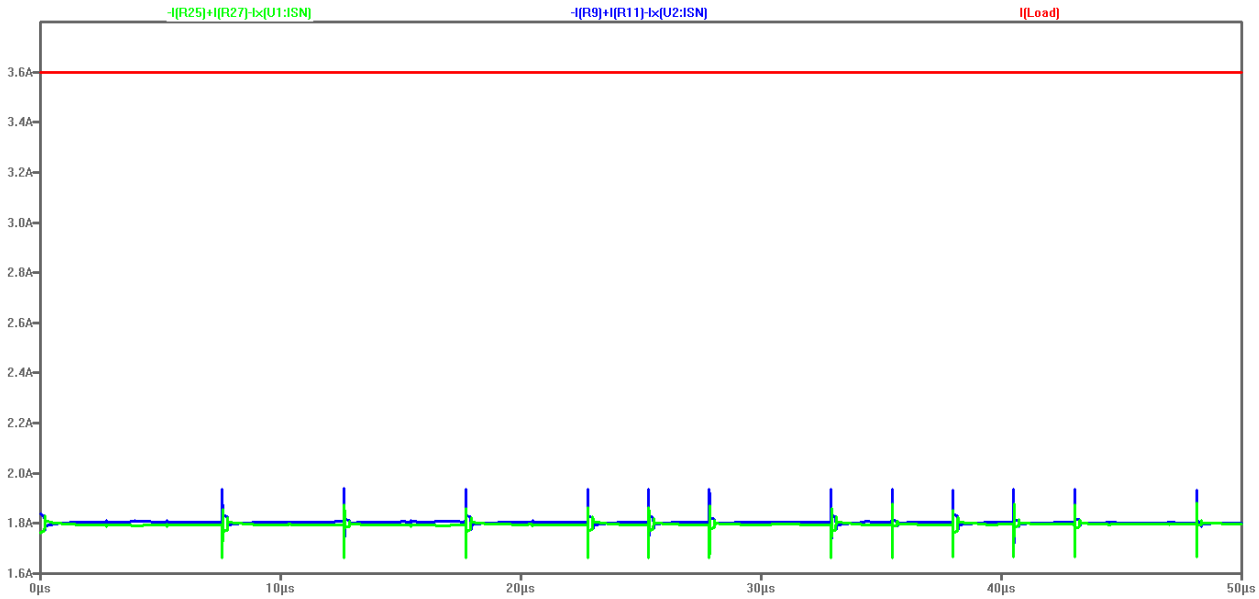

Figure 7-10: Parallel LT3791-1 DC-DC converter output currents
Board 1 Current (Green), Board 2 Current (Blue), Output current (Red)

Figure 7-10 displays the output load current (red trace) and output currents of two synchronized LT3791-1 controllers (green and blue traces). Each LT3791-1 controller outputs an average of 1.8A to supply a 3.6A load current at a 36V input and 36V output in buck-boost mode.

Chapter 8: LT3791-1 Operation Discussion

8.1. Power Switch Operation

Each LT3791-1 chip controls four external switches, M1-M4, connected to the power inductor, V_{IN}, V_{OUT}, and ground through a current sense resistor as shown in Figure 8-1: Four output switches across power inductor. The device operates in buck, buck-boost, or boost operation. The following discussion presents the operation of the four switches described in LT3791-1's datasheet.

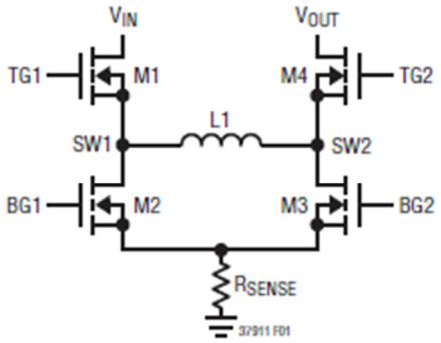

Figure 8-1: Four output switches across power inductor [4]

Buck Operation

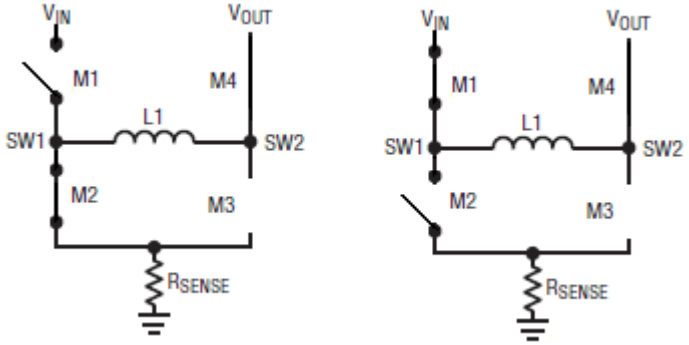

Figure 8-2: Power MOSFET buck operation, modified switching pattern [4]

Buck operation occurs when $V_{IN} > V_{OUT}$, during which switch M4 is always on and switch M3 is always off. Switch M2 turns on at the start of every cycle and R_{SENSE} sense inductor current whenever switch M2 is on. When the sensed inductor voltage falls below the

reference voltage, V_C, switch M2 turns off and switch M1 turns on. Switches M1 and M2 continue to synchronously operate as a typical synchronous buck regulator. Switch M1's duty cycle increases until the maximum duty cycle of the converter reaches 92%, or until the buck-boost region is reached, where V_{IN} approaches V_{OUT}. Figure 8-2displays buck mode switch operation and Figure 8-3: Buck operation waveform displays buck operation switching waveform.

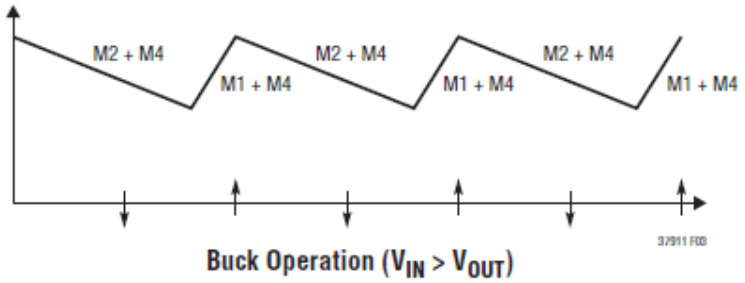

Figure 8-3: Buck operation waveform [4]

Buck-Boost Operation

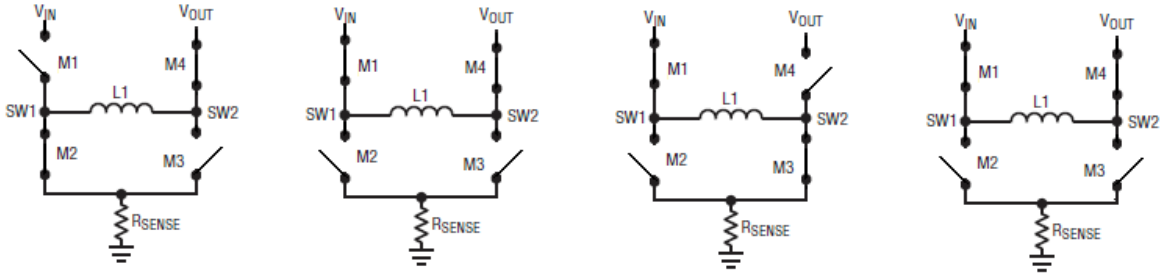

Figure 8-4: Power MOSFET buck-boost operation, modified switching pattern [4]

Buck-Boost operation occurs when $V_{IN} \approx V_{OUT}$ during which switches M2 and M4 turn on and M1 and M3 turn off at the start of every cycle. Then, switches M1 and M4 remain on until M1 and M3 turn on. Switches M1 and M4 then turn on for the rest of the cycle. Buck-Boost mode operates at a 8% switching duty cycle. Figure 8-4 displays switching operation and Figure 8-5 displays buck-boost operating switching waveform.

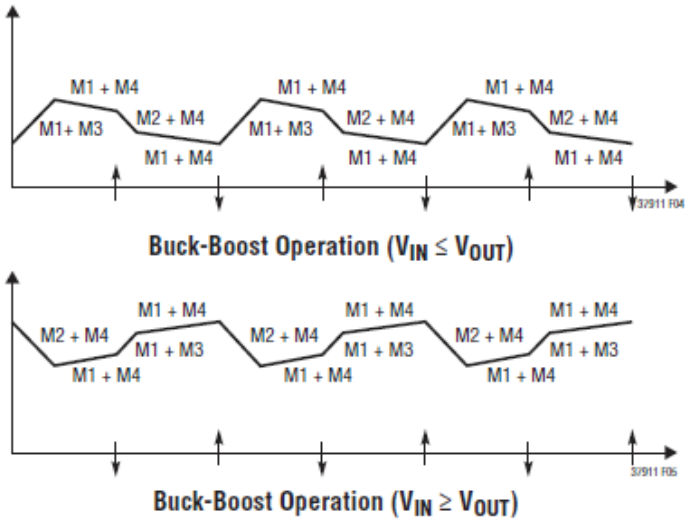

Figure 8-5: Buck-Boost operation waveform [4]

Boost Operation

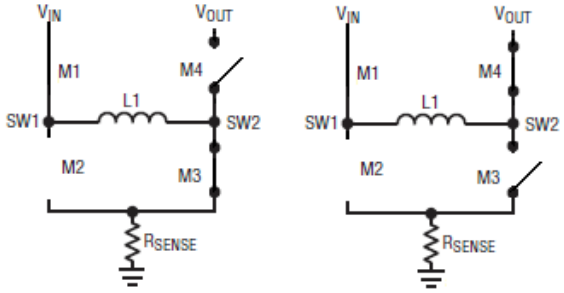

Figure 8-6: Power MOSFET boost operation, modified switching pattern [4]

Boost operation occurs when $V_{IN} < V_{OUT}$ during which switches M1 is always on and M2 is always off. Switch M3 turns on at the start of every cycle and R_{SENSE} sense inductor current whenever M3 switches. Switches M3 turns off and M4 turns on when the sensed inductor current exceeds V_C. Switches M3 and M4 continuously alternate in operation, thereby operating as a typical synchronous boost regulator. The switching duty cycle of M3 continues to decrease until reaching a minimum duty cycle of 8%. Figure 8-6 displays boost switching operation and Figure 8-7 displays boost operation switching waveform.

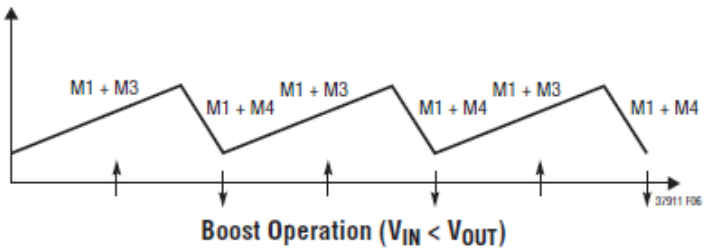

Figure 8-7: Boost operation waveform [4]

8.2. CCM and DCM Operation

The LT3791-1 controller operates in Continuous Conduction Mode (CCM) or Discontinuous Condition Mode (DCM). LT3791-1's datasheet recommends CCM for heavy loads and CCM activates when the CCM pin pulls higher than 1.5V, allowing inductor current to flow negative. DCM is recommended for light loads and activates when the CCM pin pulls less than 0.3V disallowing negative inductor current and allowing inductor current to remain at 0A during switching periods.

Connecting pins CCM to $\overline{C/10}$ with a 100kΩ pull-up resistor to $INTV_{CC}$ programs DCM operation at light loads and CCM operation at heavy loads. A light-load detection pulls down $\overline{C/10}$, which pulls up when FB exceeds 1.15V and the voltage across the output current sense resistor, $V_{(ISP-ISN)}$, senses less than 10mV. Pulling down $\overline{C/10}$ thus pulls down pin CCM and initiates DCM. Switch operations function as described in Section 8.1 for buck and boost operations in CCM mode. Switch operations in DCM function the same as in CCM but switch M4 turns off when inductor current flows negative.

Chapter 9: First Design Iteration

9.1. Initial Design

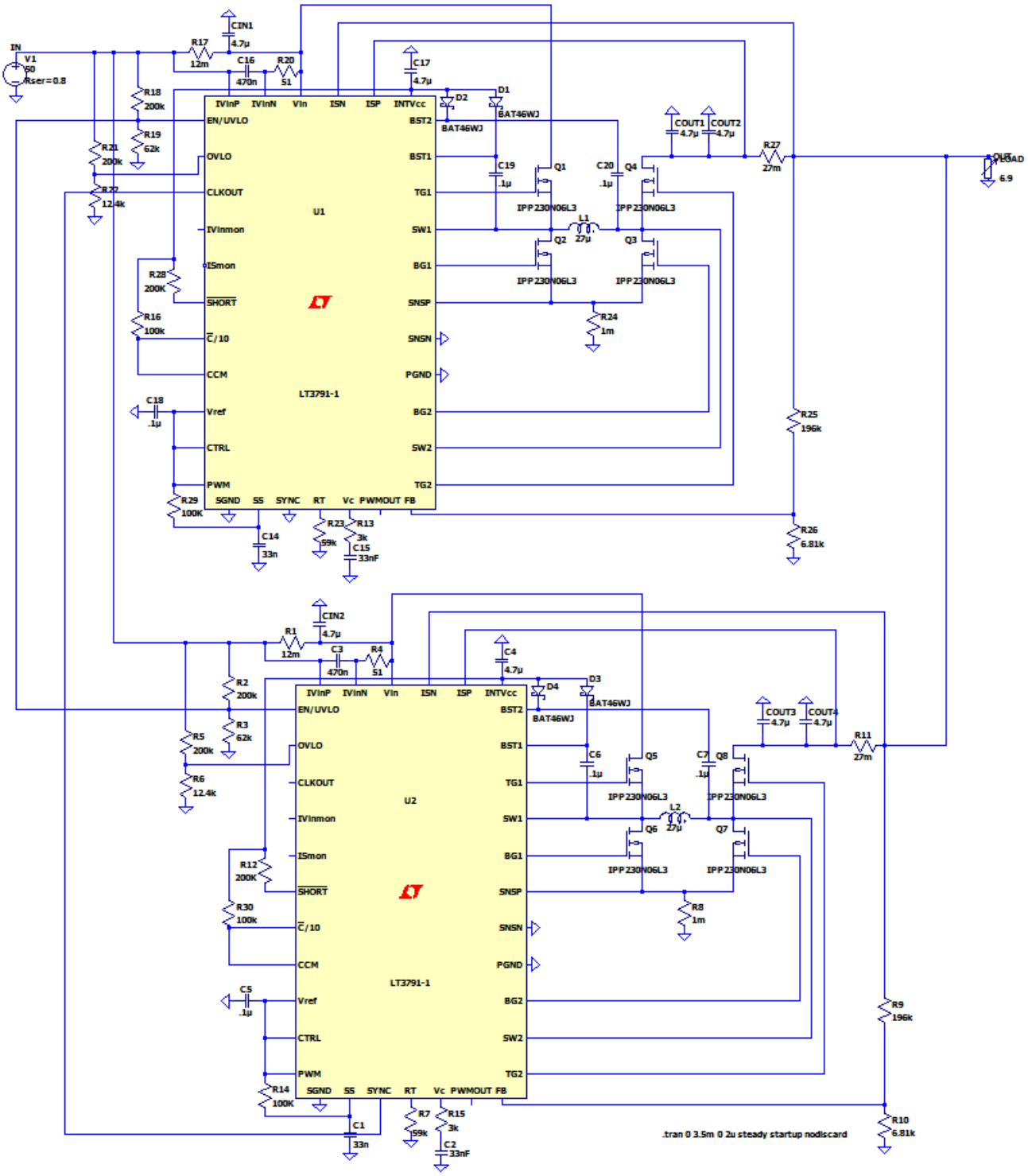

Figure 9-1: Parallel LT3791-1 Buck-Boost Converter Topology LTspice Schematic

Table 9-1: Initial LT3791-1 Buck-Boost Converter Component list

Type	Component	Value	Component	$/unit	QTY	Sum	P/N	Description	Company
Inductor	Power Inductor	39u	Inductor	$6.08	2	$12.16	AIRD-03-270K	INDUCTOR PWR DRUM CORE 27UH	Abracon
Resistors	In-Curr Sense Res	12m	R1	$1.17	2	$2.34	ERJ-8BWFR012V	RES 0.012 OHM 1W 1% 1206 SMD	Panasonic
	EN/UVLO	200k	R2	$0.10	2	$0.20	RC2012F204CS	RES 200K OHM 1/8W 1% 0805	Samsung
	EN/UVLE	62k	R3	$0.10	2	$0.20	ERJ-6ENF6202V	RES 62K OHM 1/8W 1% 0805 SMD	Panasonic
	Compensation	51	R4	$0.89	2	$1.78	CRCW080551R0FKEA	RES 51.0 OHM 1/8W 1% 0805 SMD	Vishay Dale
	OVLO	200k	R5	$0.10	2	$0.20	ERJ-6ENF2003V	RES 200K OHM 1/8W 1% 0805 SMD	Panasonic
	OVLO	12.4k	R6	$0.10	2	$0.20	ERJ-6ENF1242V	RES 12.4K OHM 1/8W 1% 0805 SMD	Panasonic
	RT	59k	R7	$0.10	2	$0.20	ERJ-6ENF5902V	RES 59K OHM 1/8W 1% 0805 SMD	Panasonic
	Rsense	1m	R8	$0.67	2	$1.34	CSR2512C0R001F	RES 0.001 OHM 3W 1% 2512	Riedon
	FB1	196k	R9	$0.10	2	$0.20	ERJ-6ENF1963V	RES 196K OHM 1/8W 1% 0805 SMD	Panasonic
	FB2	6.98k	R10	$0.10	2	$0.20	ERJ-6ENF1202V	RES 12K OHM 1/8W 1% 0805 SMD	Panasonic
	ROUT	27m	R11	$1.25	2	$2.50	WSL2512R0270FEA18	RES .027 OHM 2W 1% 2512 SMD	Vishay Dale
	RSHORT	200k	R12	$0.10	2	$0.20	ERJ-6ENF2003V	RES 200K OHM 1/8W 1% 0805 SMD	Panasonic
	C/10	100k	R13	$0.10	2	$0.20	ERJ-6ENF1003V	RES 100K OHM 1/8W 1% 0805 SMD	Panasonic
	RSS	100k	R14	$0.10	2	$0.20	ERJ-6ENF1003V	RES 100K OHM 1/8W 1% 0805 SMD	Panasonic
	RVC	3k	R15	$0.10	2	$0.20	ERJ-6ENF3001V	RES 3K OHM 1/8W 1% 0805 SMD	Panasonic
Switches			Q1-Q8	$1.06	8	$8.48	IPP230N06L3 G	MOSFET N-CH 60V 30A TO220-3	Infineon
Capacitors	CSS	33nF	C1	$0.24	2	$0.48	C0603C333K8RACTU	CAP CER 0.033UF 10V 10% X7R 0603	Kemet
	VC	33nF	C2	$0.24	2	$0.48	C0603C333K8RACTU	CAP CER 0.033UF 10V 10% X7R 0603	Kemet
	IN	470n	C3	$0.12	2	$0.24	C1005X5R1A474K050BB	CAP CER 0.47UF 10V 10% X5R 0402	TDK
	INTVCC	4.7u	C4	$1.40	2	$2.80	C3225X7S2A475M200AB	CAP CER 4.7UF 100V 20% X7S 1210	TDK
	VREF	0.1uF	C5	$0.10	2	$0.20	C1608X7R1E104K080AA	CAP CER 0.1UF 25V 10% X7R 0603	TDK
	BST	0.1uF	C6 and C7	$0.10	4	$0.40	C1608X7R1E104K080AA	CAP CER 0.1UF 25V 10% X7R 0603	TDK
	COUT	4.7u	C8	$0.48	4	$1.92	CL32B475KBUYNNE	CAP CER 4.7UF 50V 10% X7R 1210	Samsung
	Cap_IN	4.7u	C11	$0.45	2	$0.90	CGA6M3X7S2A475K200AB	CAP CER 4.7UF 100V 10% X7S 1210	TDK
Schottky			D1-D4	$0.44	4	$1.76	BAT46WJ,115	DIODE SCHOTKY 100V 0.25A SOD323F	NXP Semicond.
Controller	LT3791-1		Controller	$11.21	2	$22.42	LT3791IFE-1#PBF	IC REG CTRLR BUCK BST 38TSSOP	Linear Tech
					TOTAL	$62.40			
					W/ Tax	$67.39			

Figure 9-1 displays the initial implementation of this project's Buck-Boost DC-DC Converter based on an LT3791-1 4-Switch Buck-Boost Controller topology. Chapter 7 describes component selection. Table 9-1 outlines component cost and quantity before tax and shipping. Digikey.com's database provided a listing of all components. Section 17.D includes the initial design's SPICE Netlist.

9.2. Initial Design Simulations

Programmed overvoltage and undervoltage limits from Section 7.7 limit simulation voltage inputs between 5V and 51V. Simulated input power results from $P_{IN} = \frac{V_{IN}^2}{R_{IN}}$ where R_{IN} represents the nominal 10Ω elliptical machine resistance. $P_{IN} = P_{OUT}$ estimates output current knowing a regulated 36V V_{OUT}. Therefore, $P_{IN} = V_{IN}^2 * 10\Omega = P_{OUT} = V_{OUT} * I_{OUT}$. Calculations using a specific input power result in a specific current load. For example, a 50V input yields a 6.94A load current.

Section 17.E displays measured power efficiency measurements across a 6V to 51V input range while

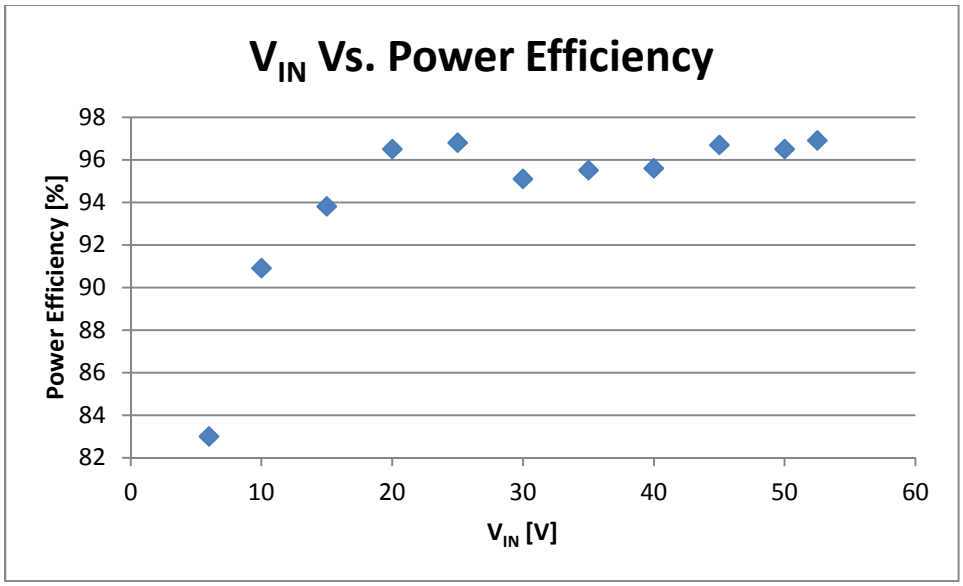

Figure 9-2 summarizes measured efficiency data. The synchronized parallel LT3791-1 Buck-Boost converter design performs at 94.3% average power efficiency across the simulated 6V to 51V input range. Simulated average power efficiency performs higher than Alvin Hilario's 94.07% power efficiency and Martin Kou's 78.3% power efficiency.

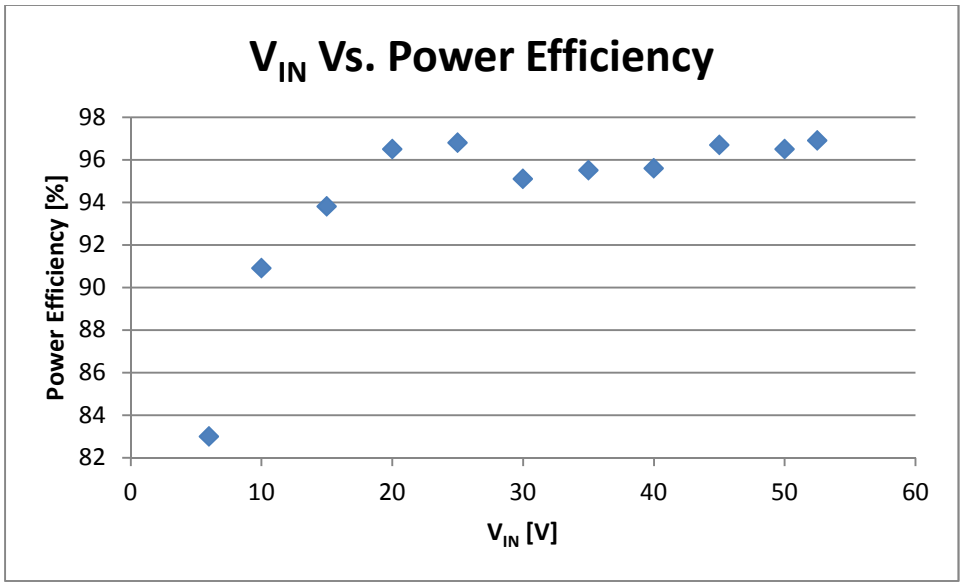

Figure 9-2: Parallel LT3791-1 Buck-Boost Converter Power Efficiency vs. V_{IN}

Tests also observed overvoltage and undervoltage conditions. System input voltage increased to 50V over 1ms to allow the converter enough time to regulate the output to 36V. Then, the output slowly increased to 54V to determine the voltage input at which the converter shuts off due to an overvoltage fault. Section 7.7 set the programmable overvoltage condition to 51.387 V. Figure 9-3 displays an overvoltage event triggering at 51.389V whereupon circuit operation ceases. Figure 9-4 displays an overvoltage event entering a safe operating range triggering at 50.54V, resuming switch operation. Figure 9-5 displays an undervoltage safety condition at approximately 6V at which the converter initiates operation. Figure 9-6 displays an undervoltage fault which ceases converter switching at approximately 5.056V.

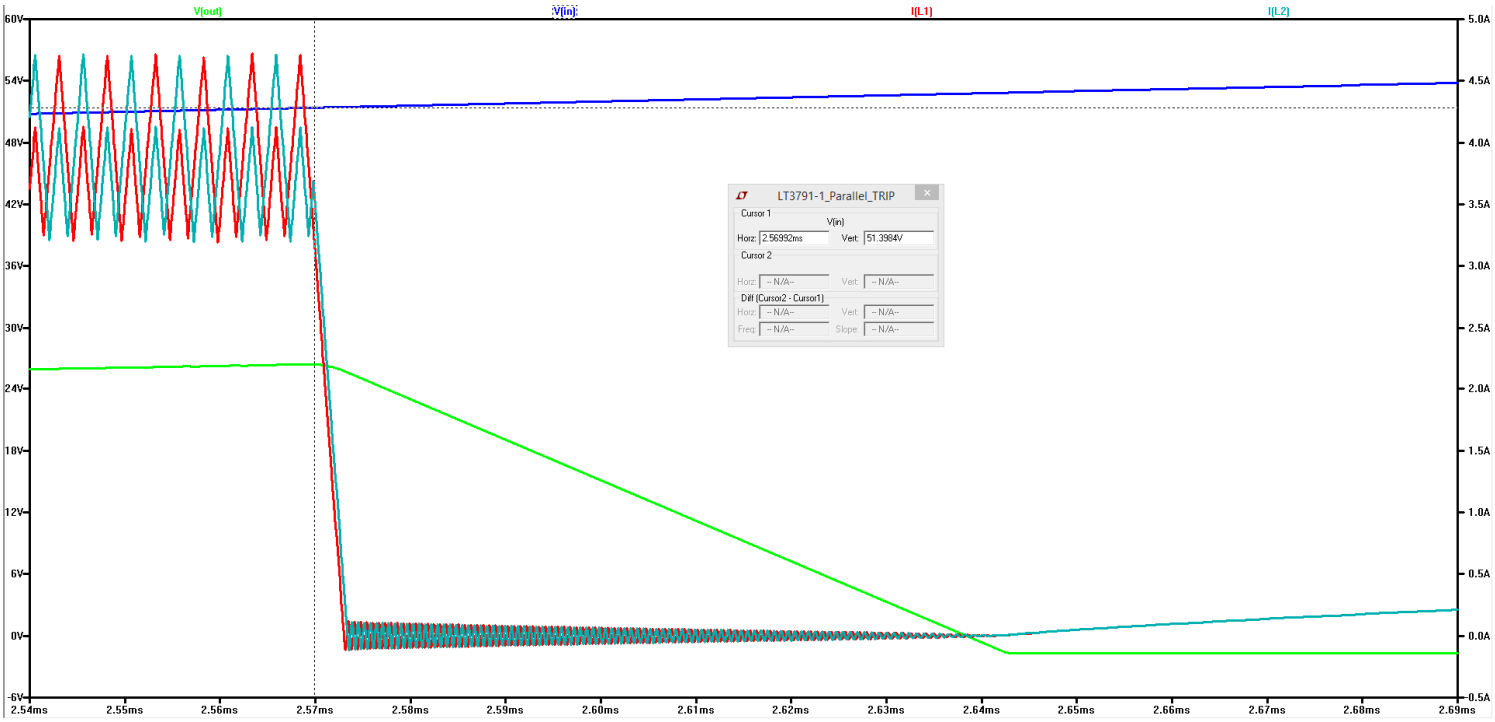

Figure 9-3: Input Overvoltage Fault Condition
V_{IN} (Blue), V_{OUT} (Green), Inductor 1 Current (Red), Inductor 2 Current (Cyan)

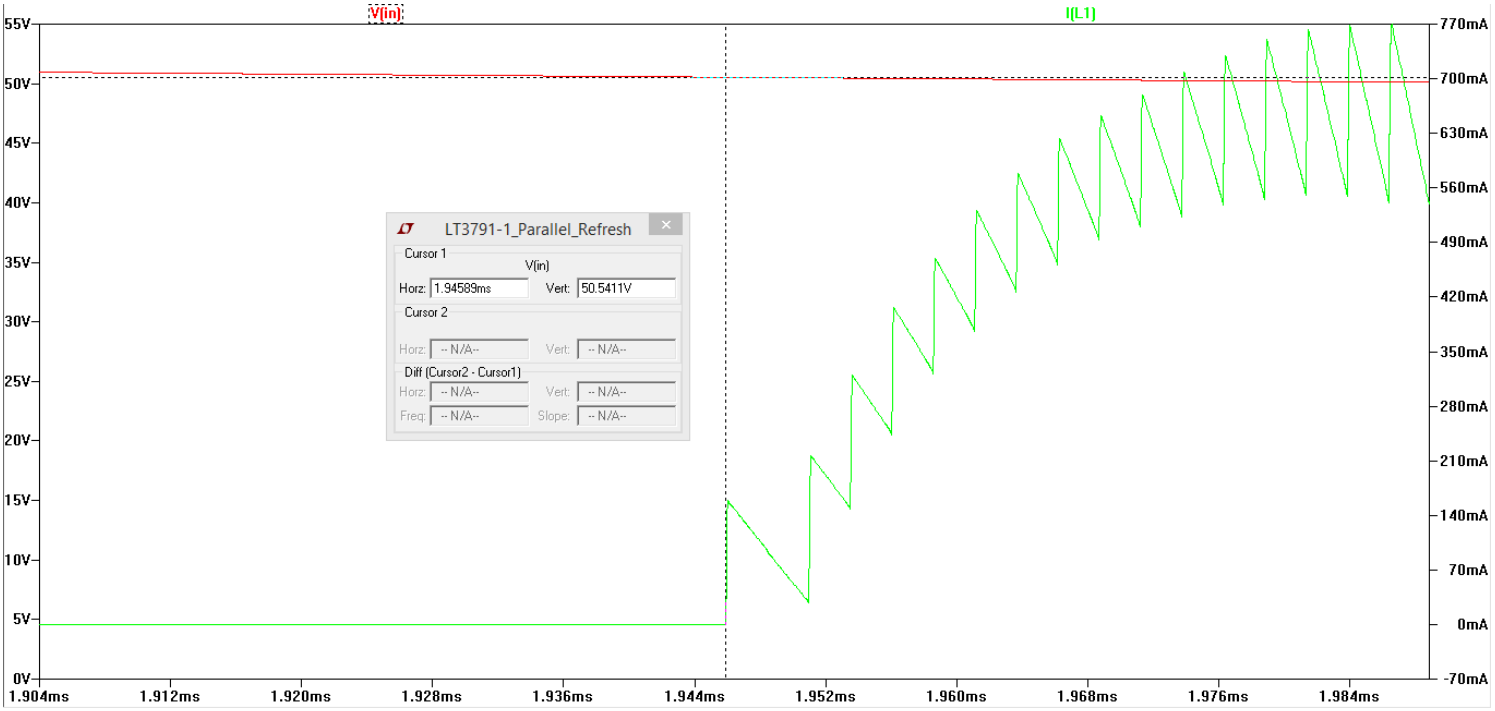

Figure 9-4: Input Overvoltage Safe Condition
V_{IN} (Red), Inductor 1 Current (Green)

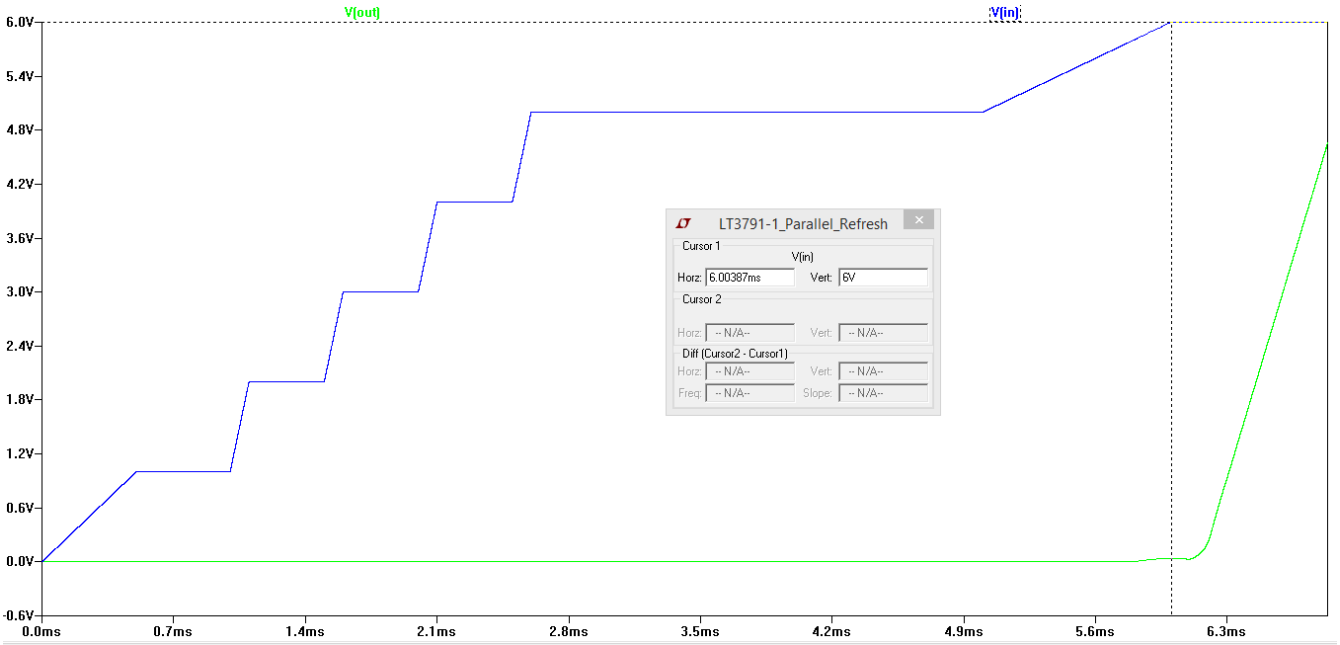

Figure 9-5: Input Undervoltage Safe Condition
V_{IN} (Blue), V_{OUT} (Green), G_{Q1} (Red)

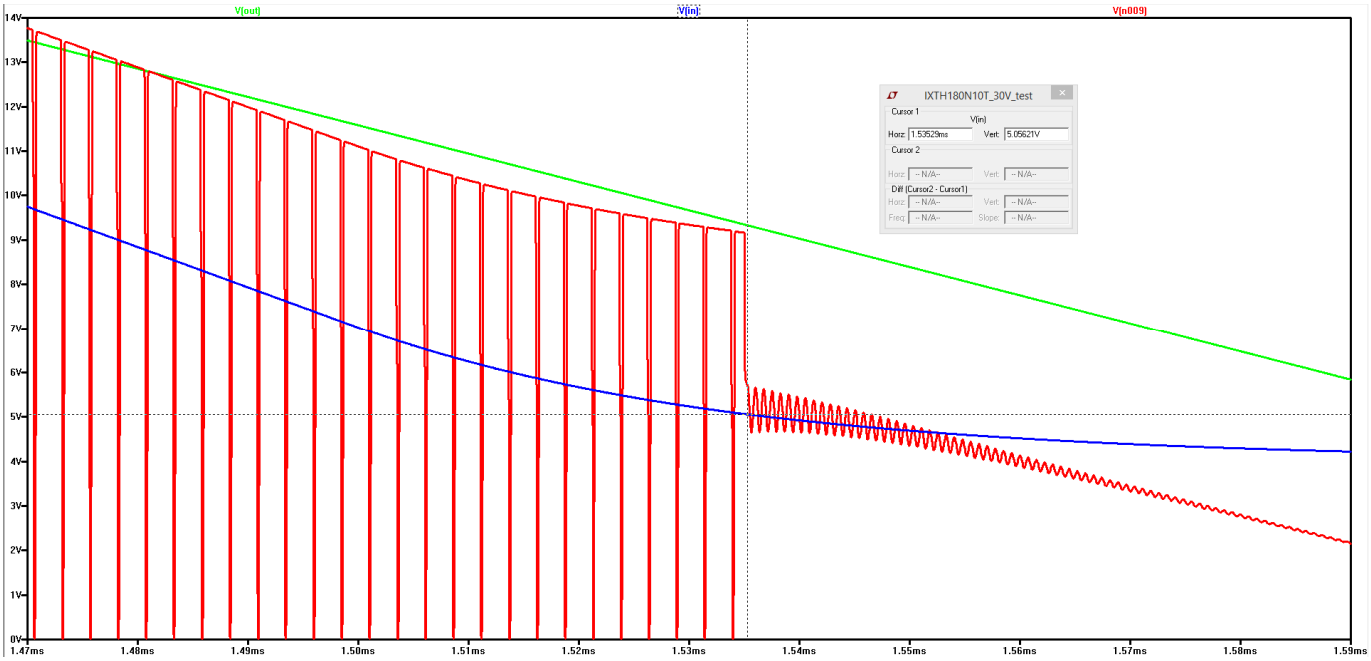

Figure 9-6: Input Undervoltage Fault Condition
V_{IN} (Blue), V_{OUT} (Green), G_{Q1} (Red)

9.3. Initial Design Errors

Further inspection of the first design iteration noted numerous critical errors. High current and power transients generated unreasonable simulations throughout all voltage and power inputs. The following discussion considers a 50V/250W input to the DC-DC converter using Figure 9-1 simulations. LTspice's ideal voltage source models supply as much current desired by the circuit to properly operate and maintain a specified source output voltage. Figure 9-7 displays initial design results with 800 kHz input power spikes reaching 3.6kW at a 50V input. The measured 800 kHz power spikes correlate with the two LT3791-1 controllers synchronously operating at 400 kHz 180^{o} degrees out of phase. The on-board EFX 546i Elliptical Trainer's generator does not supply 3.6kW at 50V; the generator may supply a maximum 250W across a 10Ω load. Therefore, further simulation design alterations must constrain and reduce input power transients.

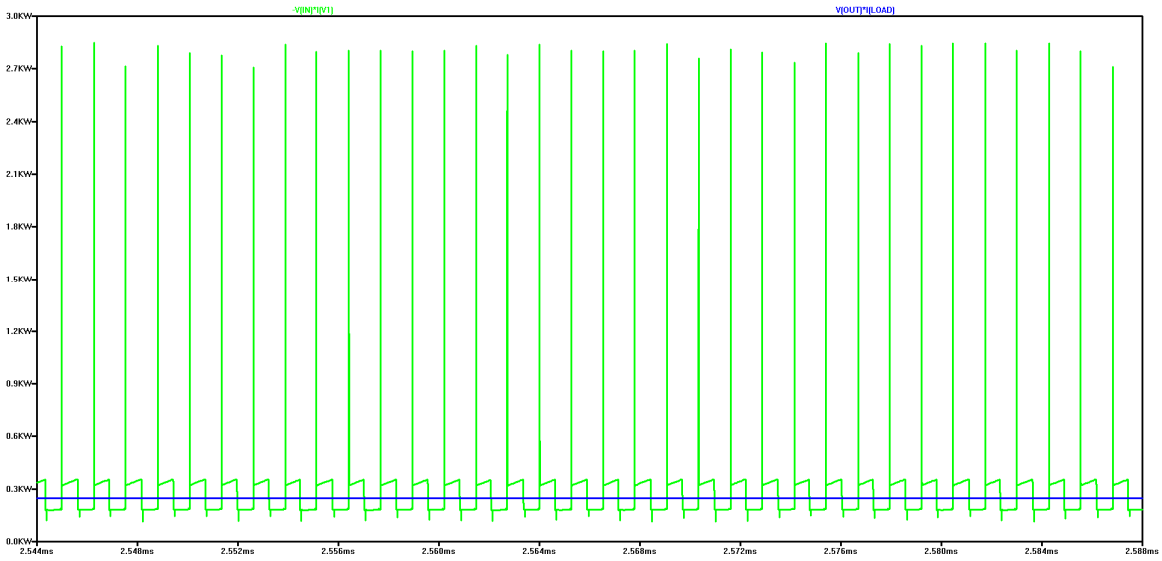

Figure 9-7: Switching Power Transients, 50V Input
Input Power (Green), Output Power (Blue)

Furthermore, power MOSFETs experienced large switching currents; far higher than their 30A current rating. During buck mode operation at a 50V input, switches Q1 and Q2 experience 67A switching current spikes. 67A exceeds IPP230N06L3's 30A rated current. Selecting higher

current and power rated MOSFETs may resolve the switching current spike issue displayed in Figure 9-8 and Figure 9-9. Figure 9-8 plots Q1 and Q2 switching currents while Figure 9-9 plots Q3 and Q4 switching currents. Figure 9-10 display power spikes correlating with switching current spikes. Switches Q1 and Q2 operate synchronously while in buck mode ($V_{IN} > V_{OUT}$) while Q3 remains off and Q4 remains on. Figure 9-11 closely inspects I_D, V_{DS}, and the power dissipation of Q1. V_{DS} does not decrease to 0V from 50V before I_D reaches 67A and thus a power spike of up to 3.3kW occurs.

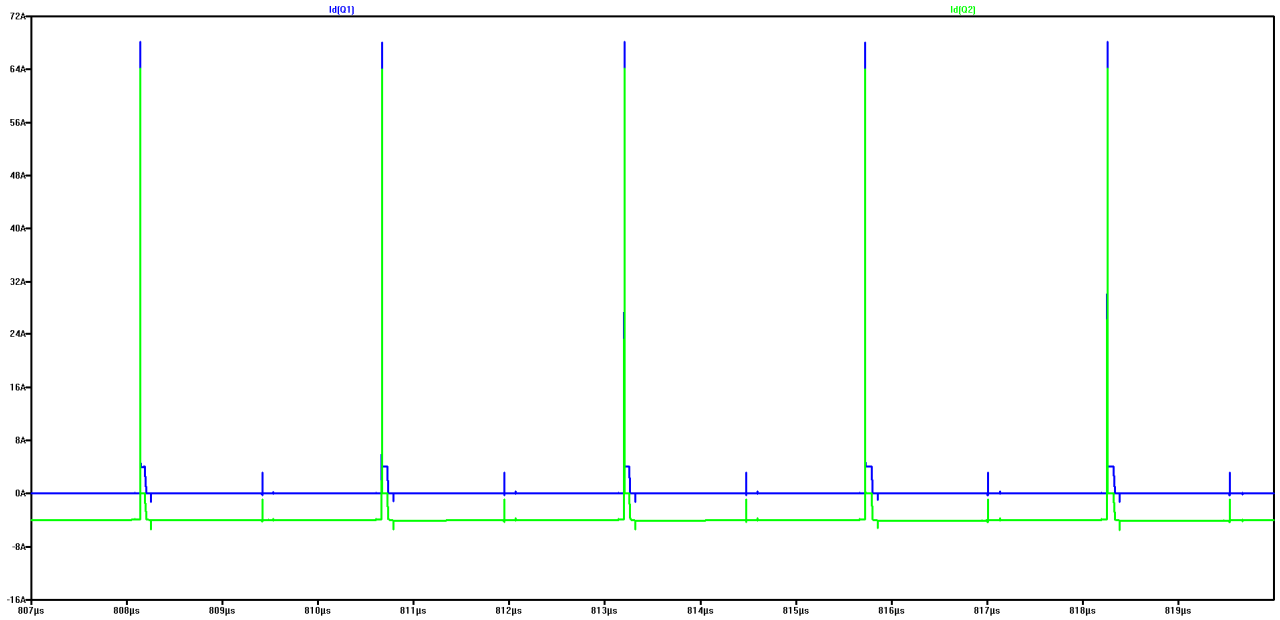

Figure 9-8: MOSFET switching current, 50V input, buck mode
Q1 (Blue), Q2 (Green)

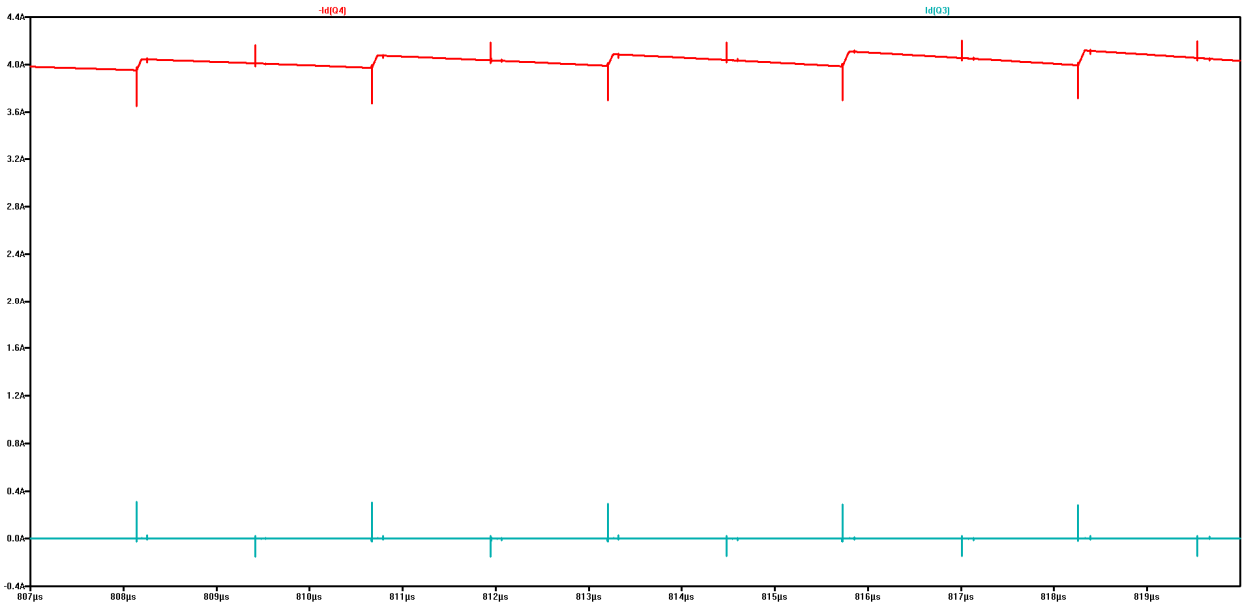

Figure 9-9: MOSFET switching currents, 50V input, buck mode
Q3 (Cyan), Q4 (Red)

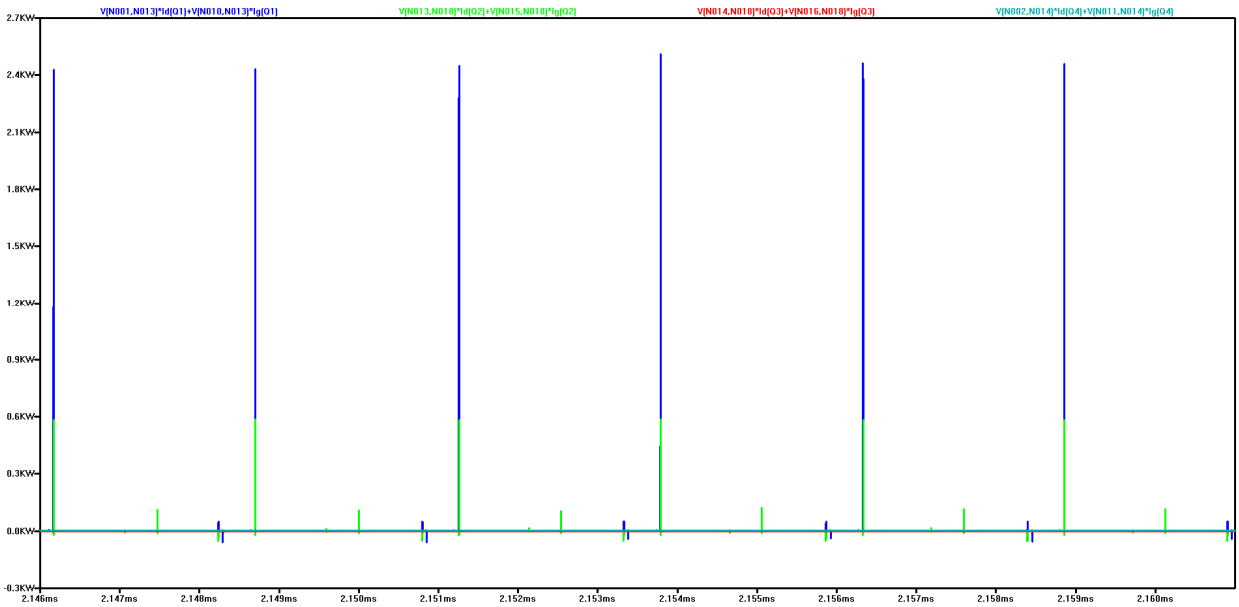

Figure 9-10: MOSFETS instantaneous power spikes, 50V input, buck
Q1 (Blue), Q2 (Green), Q3 (Red), Q4 (Cyan)

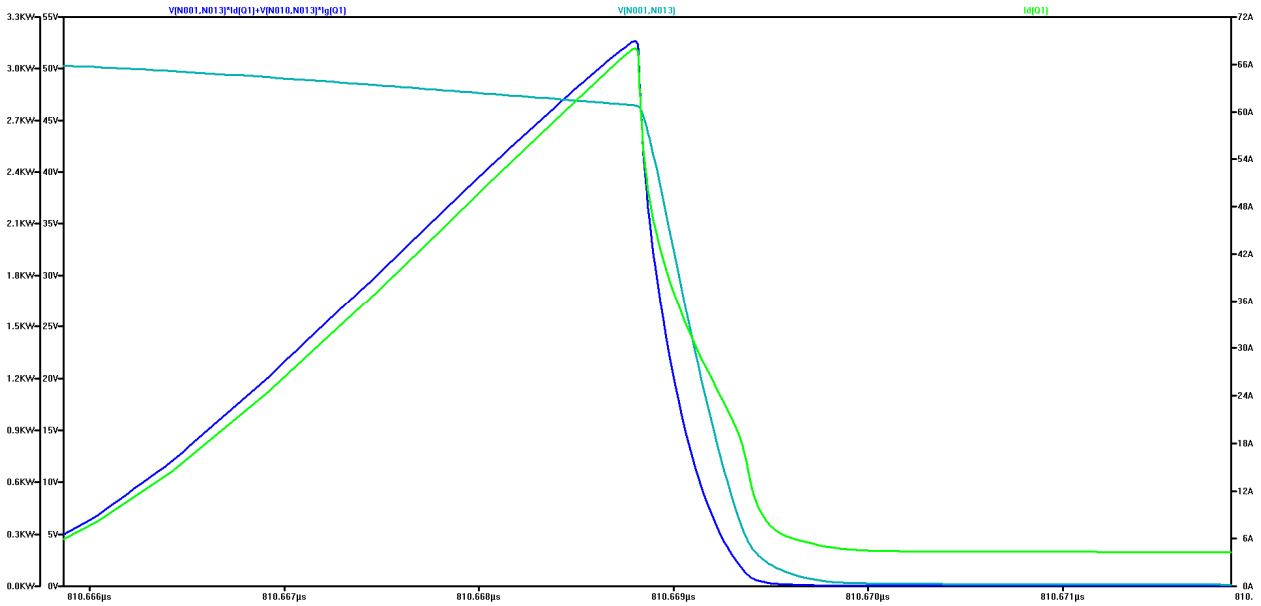

Figure 9-11: Closer inspection of Q1 turn-on V_{DS} versus I_D and resultant power spike P_{DQ1} (Blue), V_{DSQ1}(Cyan), I_{DQ1}(Green)

During a 10V input boost mode operation, switches Q3 and Q4 experience 13A switching current spikes, shown in Figure 9-12 and Figure 9-13. Figure 9-12 plots Q1 and Q2's switching currents while Figure 9-13 plots Q3 and Q4's switching currents. These current spikes correlate with MOSFET power spikes shown in Figure 9-14. Switches Q3 and Q4 operate synchronously in boost mode ($V_{IN} < V_{OUT}$) while Q2 remains off and Q1 remains on. Figure 9-15 closely inspects I_D, V_{DS}, and power dissipation of Q4. V_{DS} does not decrease to 0V from 36V before I_D reaches 67A and thus a power spike of up to 3.3kW occurs.

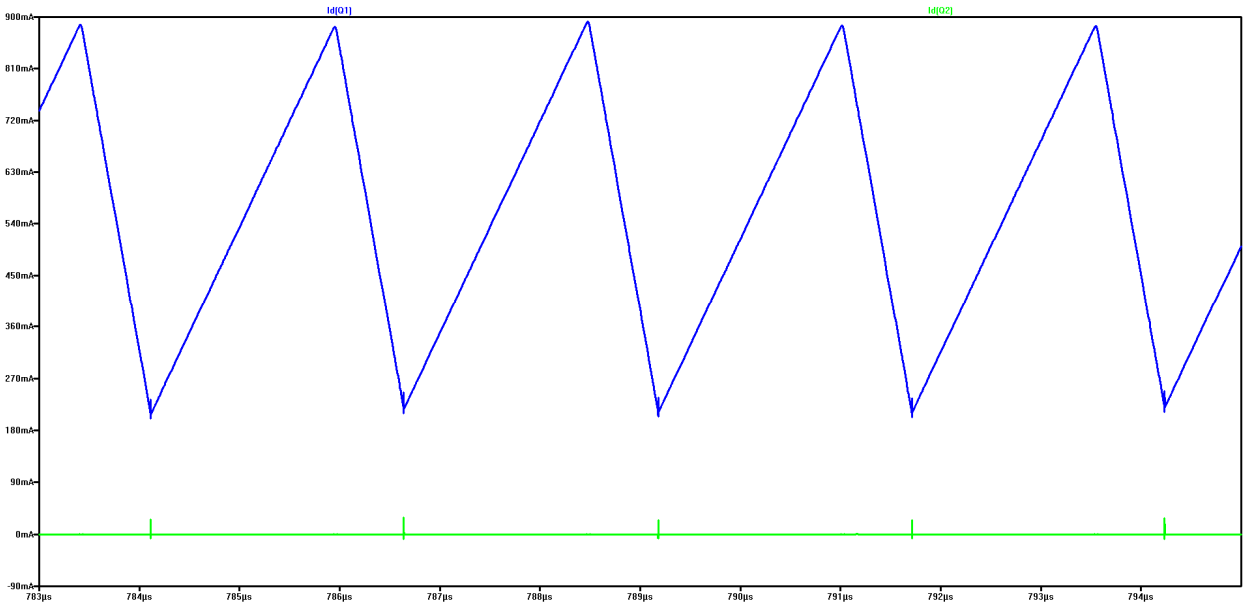

Figure 9-12: MOSFET switching current, 10V input, boost
Q1 (Blue), Q2 (Green)

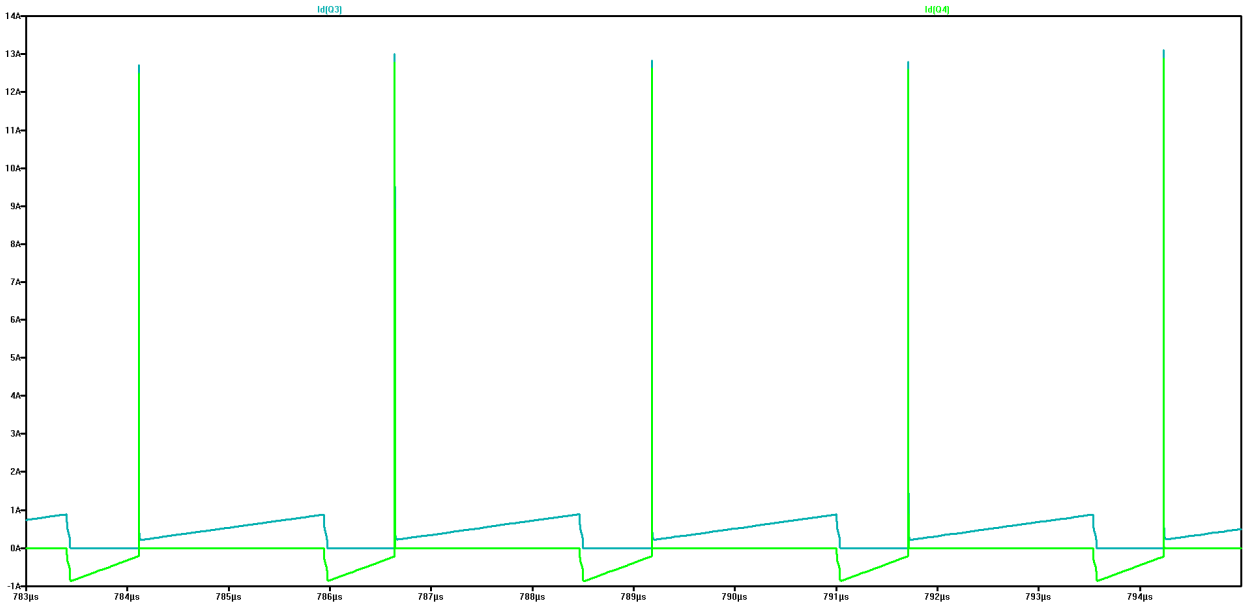

Figure 9-13: 10V input, boost, MOSFET switching current
Q3 (Cyan), Q4 (Green)

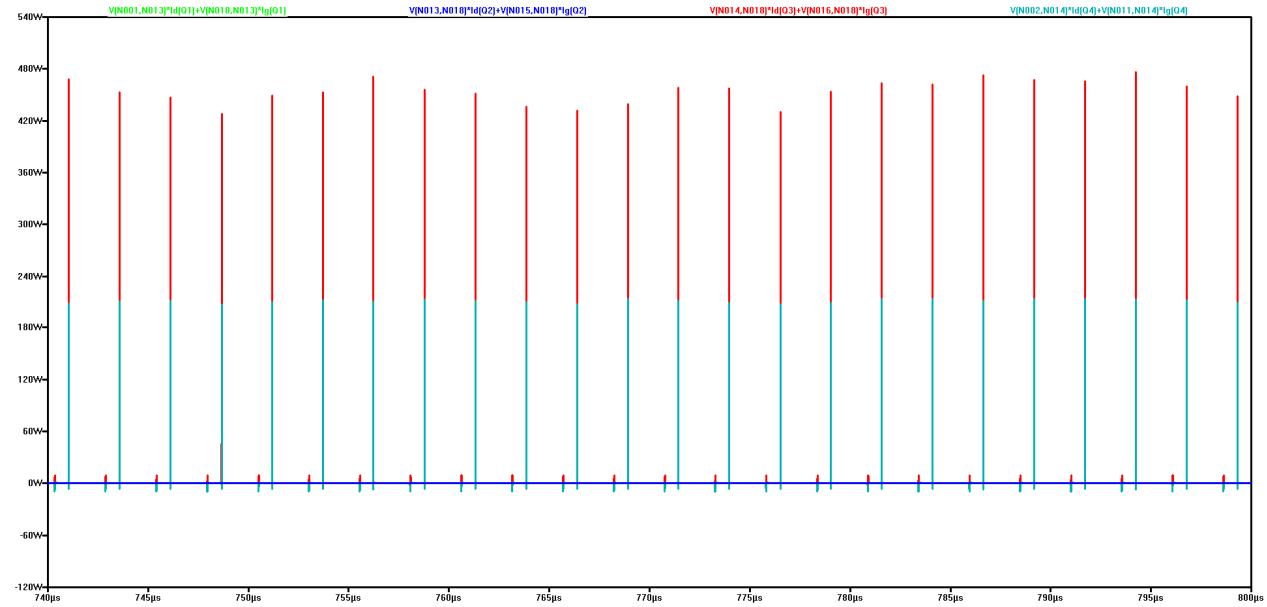

Figure 9-14: MOSFET instantaneous power spikes, 10V input, boost Q1 (Green), Q2 (Blue), Q3 (Red), Q4 (Cyan)

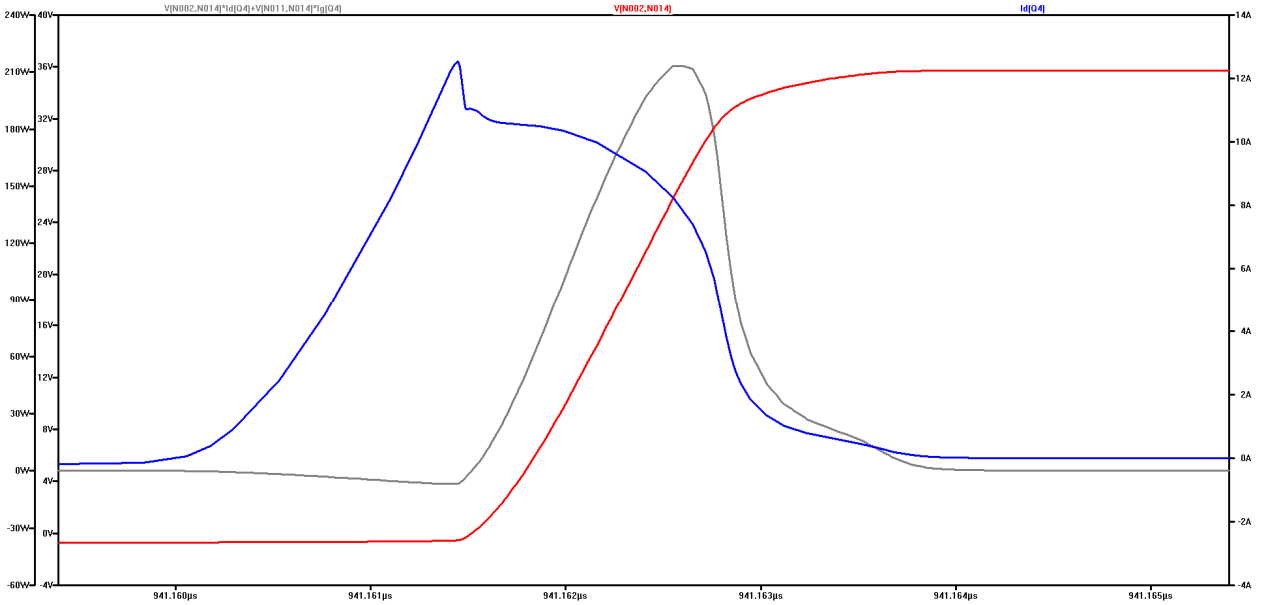

Figure 9-15: Closer inspection of Q4 turn-off V_{DS} versus I_D and resultant power spike P_{DQ1} (Blue), V_{DSQ1}(Cyan), I_{DQ1}(Green)

Output and input capacitors also experienced large power transients due to MOSFET switching. Adequately sized output capacitors must handle output voltage ripple during boost operation due to discontinuous conduction mode. Furthermore, adequately sized input capacitors must filter the input square wave current resultant of buck operation. Multiple parallel input and

output capacitors increase effective capacitance, reduce effective capacitor ESR, and allow higher RMS current handling. The initial design incorporated one input and two output 4.7μH capacitors, which was simulated and unable to handle the RMS current flowing through each capacitor. Figure 9-17 displays 35A switching currents flowing through an input capacitor.

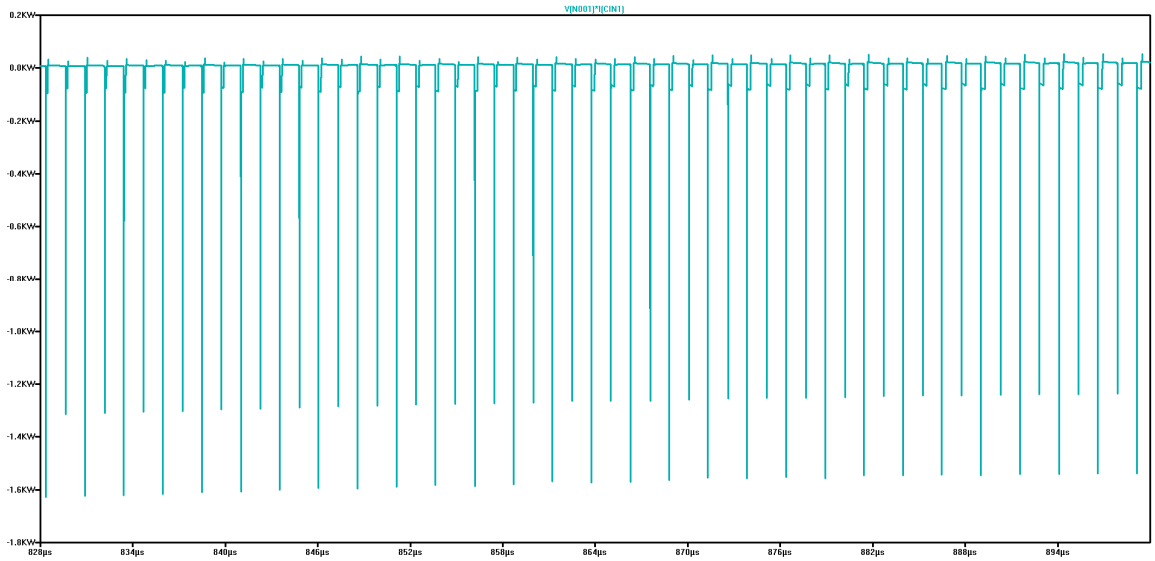

Figure 9-16: Simulated input capacitor power transients, 50V input

Figure 9-17: Simulated Input capacitor current transients, 50V input

Dr. Braun suggested three possible solutions to mitigate input power spikes aside from selecting a better power MOSFET. The first option introduced a parasitic series resistance to

LTspice's ideal voltage source to limit input current and power. The second option investigated the use of a snubber cell to reduce MOSFET current and voltage rises. The last option consisted of adding a parasitic input resistance at the input that decreased over time.

Chapter 10: Second Design Iteration

10.1. New Power MOSFET Consideration

The initial Infineon IPP230N06L3 MOSFET was ill-suited for the design because simulated switching drain current exceeded 30A and power dissipation exceeded 2.9kW. An Infineon IPI045N10N3 MOSFET rated at 100V drain-to-source voltage, 100A drain current, and a maximum $4.5m\Omega$ drain-to-source on-resistance replaced the initial MOSFET.

However, fellow EHFEM project member, Matthew Wong, discovered a more suitable power MOSFET. He discovered IXYS's IXTH180N10T N-Channel MOSFET parameterized by a 100V drain-to-source voltage, 180A drain current, and a maximum $6.4m\Omega$ drain-to-source on-resistance.

Table 10-1 compares Infineon's IPP230N06L3, IPI045N10N3, and IXYS' IXTH180N10T. IPP230N06L3 and IPI045N10N3 exhibit logic-level characteristics and are characterized by a low typical threshold voltage at 1.7V and 2.7V. While not considered a logic-level device, IXTH180N10T's exhibits a typical 3.5V typical threshold voltage. LT3791-1's datasheet suggested the use of logic-level power MOSFETs; therefore, the LT3791-1 controller may experience difficulty driving four IXTH180N10T MOSFETs. Of the three MOSFETs, the IXTH180N10T features the highest drain current, drain pulse current, and maximum power dissipation. IXTH180N10T also exhibits the lowest junction-to-case thermal resistance at $0.31°C/W$.

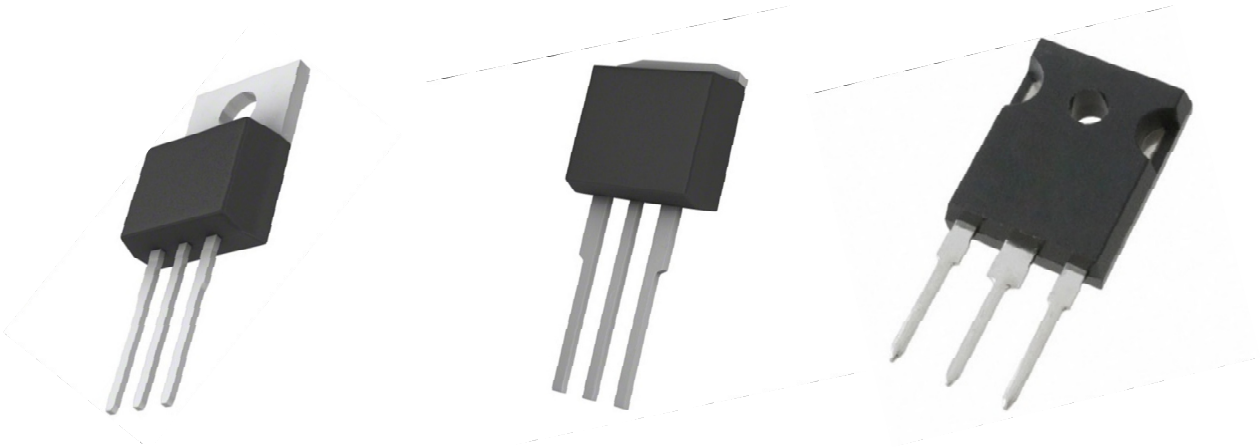

Figure 10-1: TO-220, TO-262, and TO-247 Packages
[Left, Center, Right]

Table 10-1: MOSFET Comparison Chart, 25°C, [13] [14] [15]

	IPP230N06L3 G	**IPI045N10N3 G**	**IXTH180N10T**
Package	TO-220	TO-263	TO-247
Operating Temp [$°C$]	-55 – 175 $°C$	-55 – 175 $°C$	-55 – 175 $°C$
R_{THJC} [$°C/W$]	4.2 $°C/W$	0.7$°C/W$	0.31 $°C/W$
R_{THJA} [$°C/W$]	62$°C/W$	62$°C/W$	N.A.
V_{DS} [V]	60 V	100 V	100 V
$V_{GS(TH)}$ [V], Typical	1.7 V	2.7 V	3.5 V
I_D [A]	30 A	100 A	180 A
I_{DPULSE} [A]	120 A	400 A	450 A
$R_{DSON(MAX)}$ [$m\Omega$]	23 $m\Omega$ @ 30A, 10V	4.5 $m\Omega$ @ 100A, 10V	6.4 $m\Omega$ @ 25A, 10V
Gate Charge (Q_G) [nC]	10 nC @ 4.5V	117 nC @ 10V	151 nC @ 10V
Input Capacitance [pF]	1600 pF	8410 pF	6900 pF
Maximum Power [W]	36W	214 W	480W

IXTH180N10T lacked a publically available VDMOS LTspice model for simulation use. Therefore, requiring LTspice parameter extraction from IXYS IXTH180N10T's datasheet. However, IXYS only provides IXTH180N10T's preliminary technical information [14]. As a result, key characteristics including a power deration chart and typical junction-to-ambient thermal resistance remain unavailable. Table 10-2 displays the derived LTspice model.

Table 10-2: IXTH180N10T LTspice Model

```
.model IXTH180N10T_2 VDMOS(RG=3.3 Vto=4.5 Rd=6.4m Rs=0.0m Rb=2.8m
        Cgdmax=0.3n Cgdmin=0.15n Cgs=6n Cjo=0.8n mfg=IXYS Vds=100 Ron=6.5m
        Qg=151n BV=100 IBV=250E-6 Vj=0.95 Kp=100.18)
```

R_G, or gate resistance, remained unspecified within listed characteristic values of the first three pages of IXYS's IXTH180N10T datasheet. However, a 3.3$m\Omega$ value gate resistance value

appears within Resistive Turn-On Time and Turn-Off/Turn-On Switching Time charts; therefore parameter RG = 3.3. VTO represents the threshold voltage of the MOSFET. VTO equates to IXTH180N10T's specified $V_{GS(TH)}$, typically 3.5V. The sum of parameters Rd and Rs should equal to $R_{DS(ON)}$, or 6.4mΩ. Maximum and minimum C_{RSS} values, or 300pF and 150pF, characterize Cgdmax and Cgdmin. Cgs equates to (C_{ISS} - $C_{OSS)}$, or (6900pF – 900pF) = 6000pF. Breakdown voltage, BV, occurs at 100V. The datasheet specifies a 250uA reverse breakdown current. Junction potential, VJ, equals V_{SD} or 0.95V. Equation (10.1-1) calculates transconductance, Kp, using datasheet parameters. g represents forward transcondunctance, $g_{fs,}$ defined on page 2 of IXTH180N10T's datasheet and I_D is 60A at 25°C and 6V V_{GS}.

$$Kp = \frac{g^2}{2I_D} = \frac{\left(110\frac{A}{V}\right)^2}{2(60A)} = 100.83\frac{A}{V^2} \qquad (10.1\text{-}1)$$

10.2. Further Design Alterations

The initial 27uH Abracon AIRD-03-270K unshielded inductor featured a 13.5A current rating, 23A saturation current, and 12mΩ max DC resistance. However, using an unshielded inductor near analog signal carrying traces may negatively affect critical signals. The unshielded inductor may form an inductive couple with nearby traces over an air-gap because the inductor's magnetic field escapes its package. A shielded inductor maintains most of its magnetic field within its package and thus mitigates inductive coupling to other components or traces [16]. Shielded inductors also maintain less wire turns than an unshielded equivalent and thus have a lower DCR and smaller physical profile.

No in stock approximate 27 uH shielded inductors were available within Digikey's catalog based on Section 7.5's inductor selection criteria. A 22uH inductor fulfills requirements if the allowable ripple current increases to 40% from 30% in Section 7.5. Therefore, selecting Wurth Electronic Inc's 74435582200, WE-HCI series, 22uH inductor fulfills requirements. The 74435582200 features a 15A current rating, 18A saturation current, and 7mΩ DCR. Wurth Electronic's 74435582200 benefits from shielding, a lower DCR, and higher current rating compared to the AIRD-03-270K. Using a shielded inductor minimizes the inductor's magnetic fields adverse electromagnetic effects on nearby components and traces.

Further additions include Schottky diodes connected across the Q2 and Q4's drain and source. Figure 10-3 displays the addition of Schottky diodes across Q2 and Q4. LT3791-1's datasheet suggests implementing Schottky diodes to conduct current during the dead time between power MOSFET switching [4]. The additional Schottky diodes intend to prevent the body diode of switches Q2 and Q4 from turning on and storing charge during dead time. They also reduce reverse-recovery current between switch M4's turn-off and switch M3's turn-on cycle. Selecting

Fairchild Semiconductor's MBR20100CT 100V 10A Schottky diode fulfills this application. The Schottky diode must handle current flowing through Q2 and Q4, equivalent to the inductor current. Figure 10-2 displays 3.6A inductor and Schottky diode currents for a 50V input at maximum current output. Therefore, the MBR20100CT's 10A forward current rating suffices.

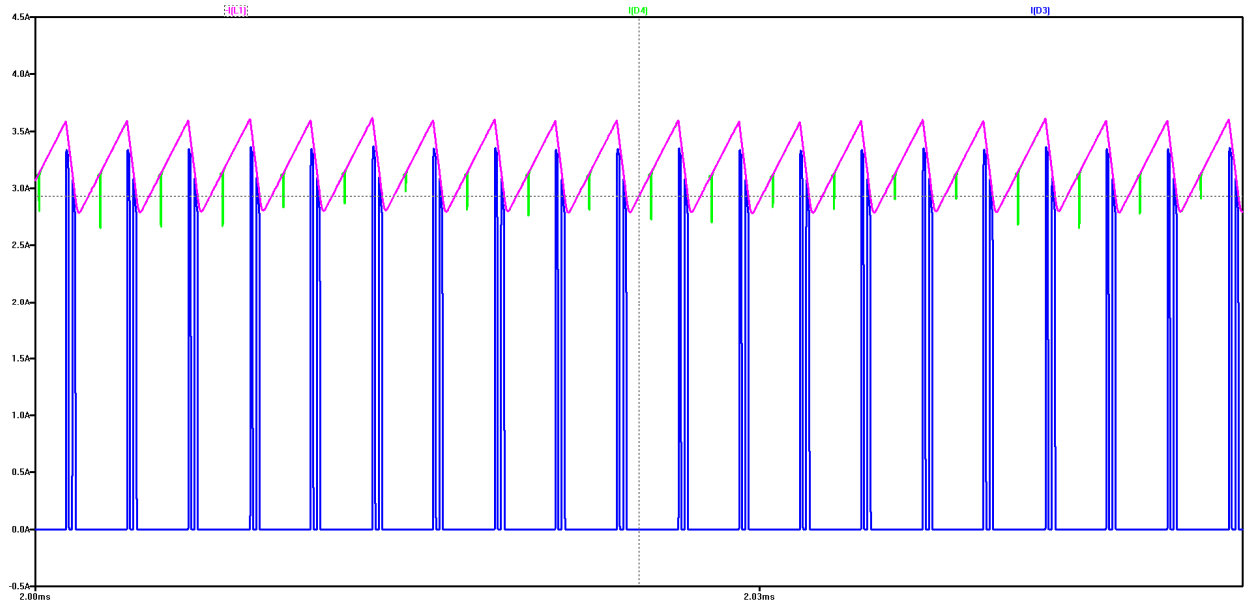

Figure 10-2: Parallel LT3791-1 Buck-Boost Converter Topology with IXTH180N10T MOSFETS 50V, Inductor Current vs. Schottky Diode Current
Inductor Current (Purple), I_{D5} (Green), ID1

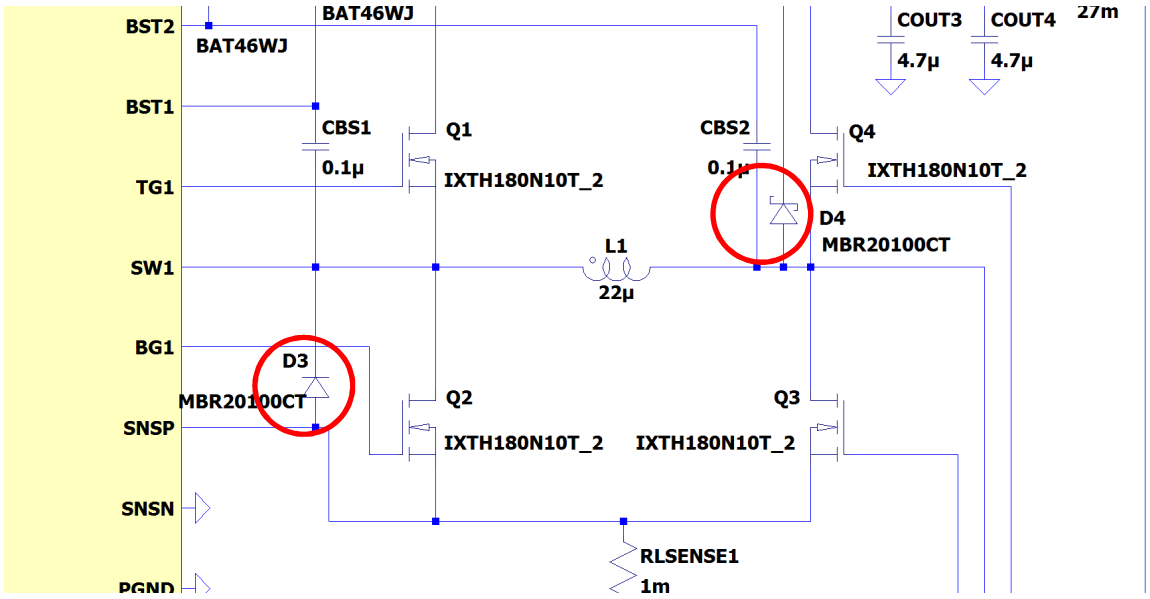

Figure 10-3: Additional Schottky Diodes D3 and D4 across Drain-Source of Q2 and Q4

Additional 100V 4.7uF output and input capacitors aid in filtering RMS output and input current. Initially, each controller had one input capacitor and two output capacitors. Input capacitors must filter square-wave current in buck mode due to Q1 switching periodically allowing then stopping system current flow. Similarly, output capacitors must filter RMS current due to Q4 switching at a 36V output.

10.3. Input Parasitic Resistance

Adding an input voltage source parasitic resistance reduced input power spikes. Dr. Braun suggested using parasitic resistance values under 1Ω. Although a series parasitic resistance decreased input power spikes, it also decreased system input voltage. Adding a series parasitic resistance did not completely limit input power, but it did significantly decrease power transients. Input power larger than nominal values were still apparent as the design charged up to a 36V output. However, the additional parasitic resistance did limit input current power at steady state. Figure 10-4 and Figure 10-5 compare simulations with and without a parasitic input source resistance. The additional parasitic resistance noticeably reduced input power transients.

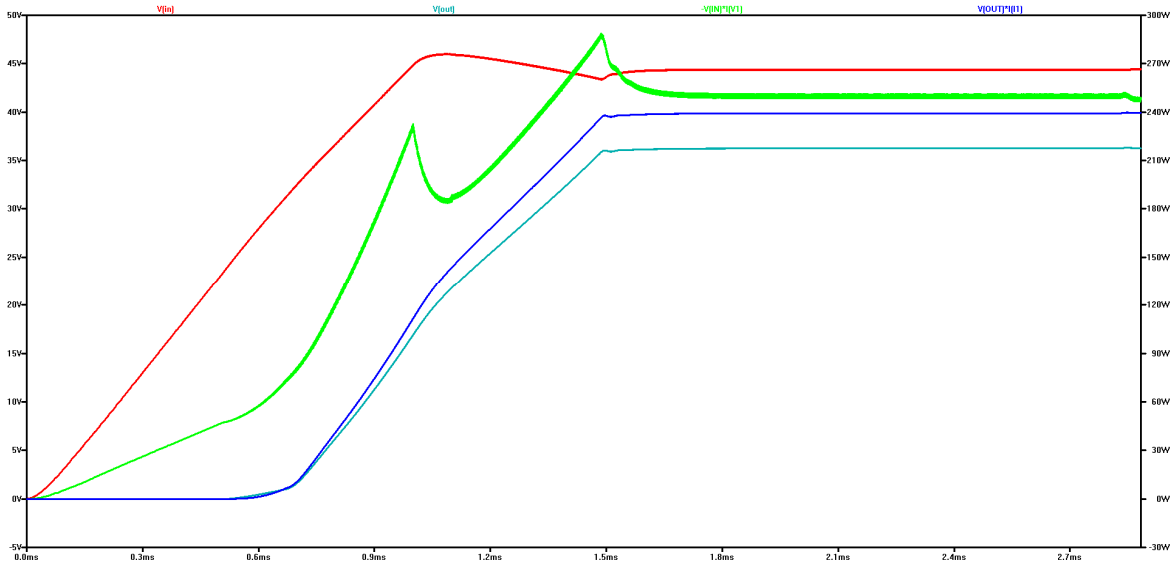

Figure 10-4: Parallel LT3791-1 Buck-Boost Converter Topology with IXTH180N10T MOSFETS 50V, 250W nominal input with 1Ω parasitic source resistance
Input Voltage (Red), Output Voltage (Cyan), Input Power (Green), Output Power (Blue)

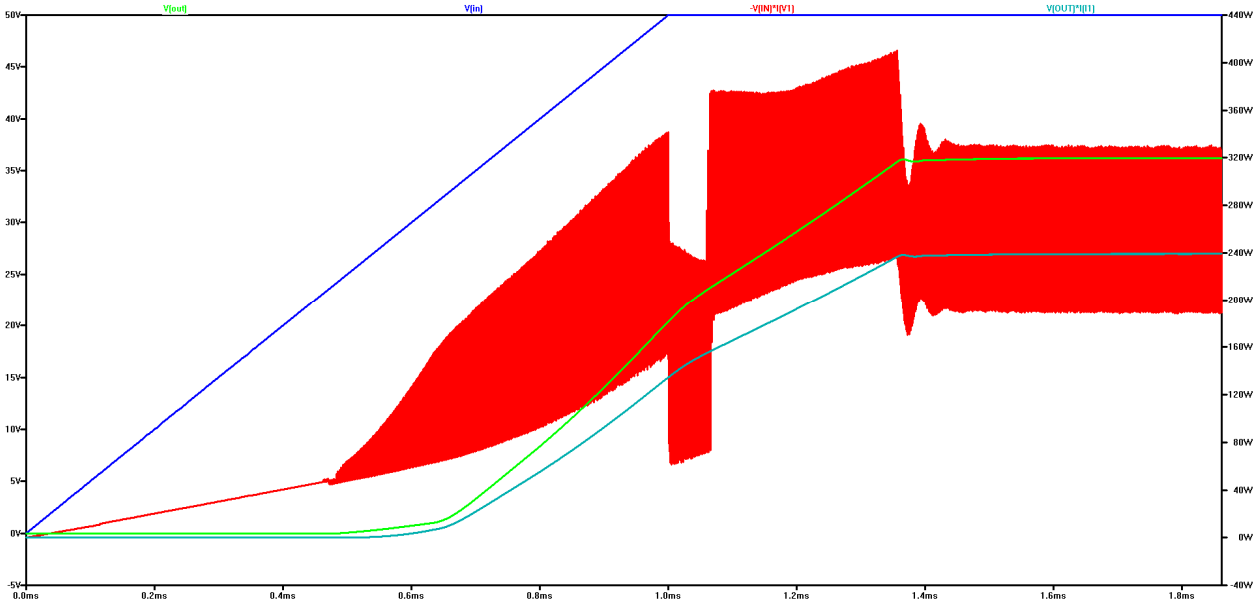

Figure 10-5: Simulated Parallel LT3791-1 Buck-Boost Converter Topology with IXTH180N10T MOSFETS 50V, 250W nominal input without parasitic source resistance
Input Voltage (Blue), Output Voltage (Cyan), Input Power (Red), Output Power (Green)

Although adding a parasitic input source resistance significantly decreased input power transients, it also generated further problems testing the design. The additional parasitic input resistance causes an internal voltage source droop and thus input voltages fall below nominal values. For example, the 50V input voltage case described in Figure 10-4 droops to 44.3V at

steady state. Parasitic source resistances cause problems at lower voltage inputs. At a 6V input, a large parasitic source resistance decreases actual applied input voltage to less than 5V. The converter then ceases operation due to an undervoltage detection fault. Therefore, parasitic input source resistance must decrease as input voltage decreases to prevent the device from ceasing operation.

10.4. Snubber Circuit Design

High MOSFET switching current and instantaneous power spikes throughout simulation scenarios indicate potential MOSFET damage during circuit operation. Therefore, implementing a snubber cell to reduce MOSFET switching current may mitigate potential damage.

MOSFET simulations indicated current spikes occurred during the turn-on phase of Q1 and Q2 when the system operated in buck mode at input voltages larger than 36V. Theoretically, adding a snubber cell onto MOSFETs delays current rise and reduces current peaks. Therefore, adding a snubber cell may achieve desired low switching current and reduce instantaneous power spikes.

Initial snubber circuit selected to obtain this goal was mentioned in Markin Kou's thesis which shows turn-on and turn-off snubber circuit design. This design is shown in Figure 10-6 and was added onto Q1 to reduce current spikes at the maximum input and load.

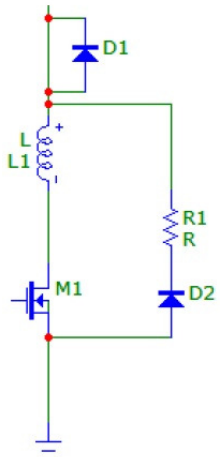

Figure 10-6: Martin Kou's Basic Turn-On Snubber Circuit Design [3]

Another consideration was implementing a simple RC snubber circuit that contained an RC circuit connected to ground. Figure 10-7 displays a sample RC snubber. This design tip was stated in a Texas Instrument's article [17].

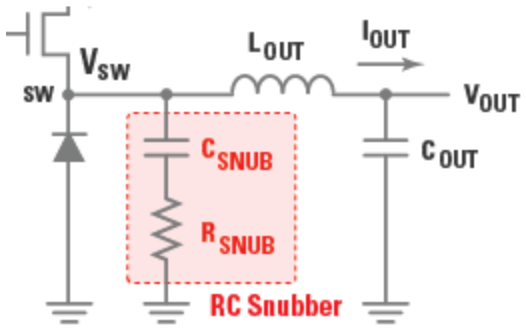

Figure 10-7: Simple RC Snubber Circuit [17]

Figure 10-7 was modified to be a turn-off RC snubber circuit for Q4 current flow and power spikes. Figure 10-8 displays the converter an RDC and RC snubber design on Q1 and Q4.

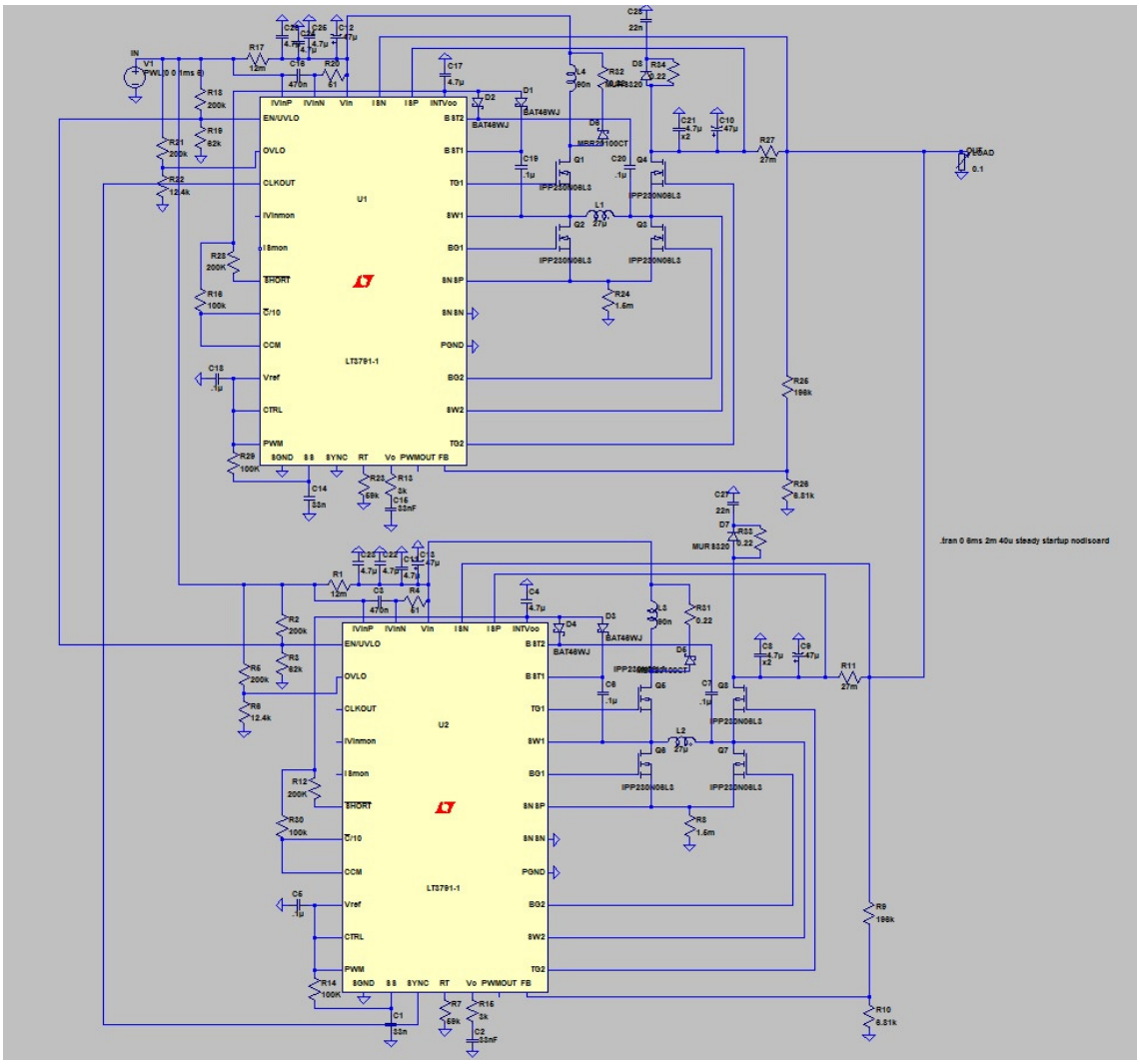

Figure 10-8: Parallel LT3791-1 Buck-Boost Converter Topology with additional turn-on and turn-off snubber cells

Adding snubber circuits dramatically decreased current spikes, leading to a direct decrease in power spikes. As shown in Figure 10-9, the current spike of Q4 decreased by ¼, which reduced the MOSFET power spike from 2kW to 300W. This reduction was effective in terms of overall power dissipation but it still required significant improvement. None of the considered MOSFETs aside from IXTH180N10T could handle instantaneous 300W power dissipation.

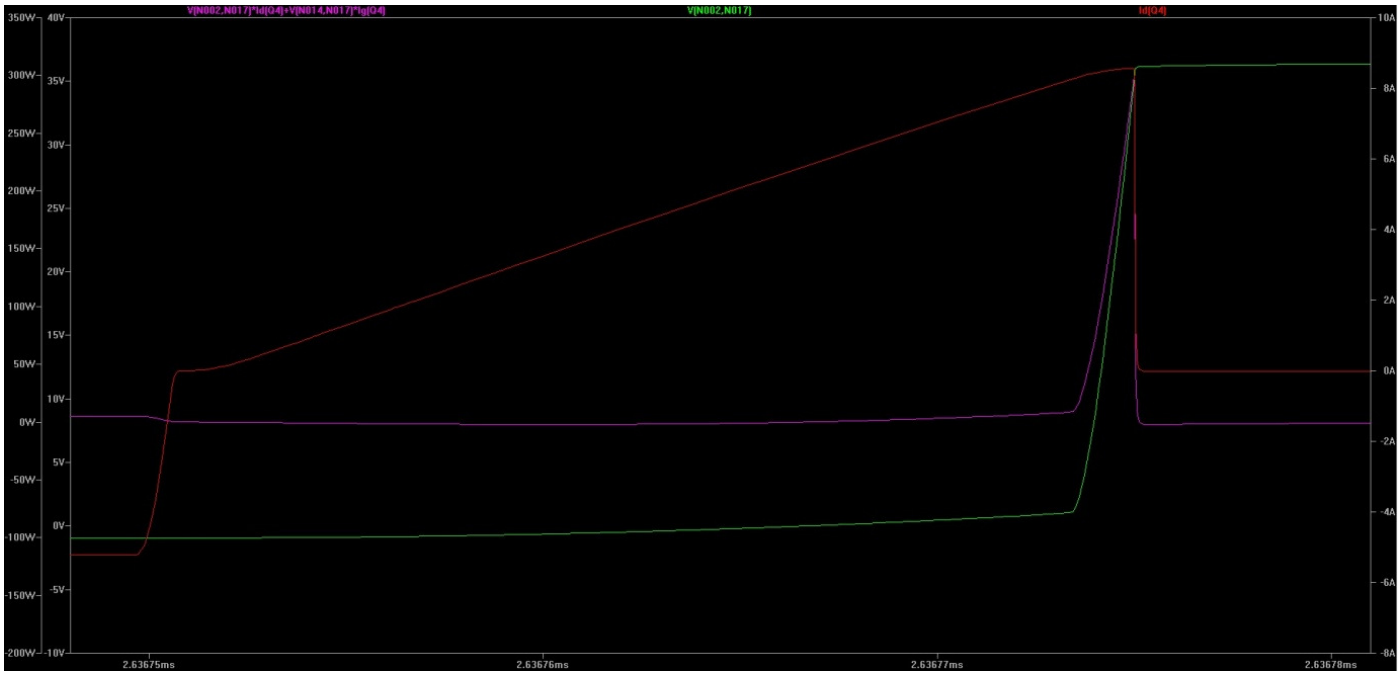

Figure 10-9: Parallel LT3791-1 Buck-Boost Converter Topology simulations, Q4 Drain Current (Red), V_{DS} (Green, Dissipated Power (Purple)

Various other snubber circuit designs were considered and tested including RCL, RCD, and RLD snubber. However, none of these circuits were able to completely reduce the power dissipation to operating level.

Equation (10.4-1) was used to find the value of the snubber capacitor.

$$C_{SNUB} = \frac{I_L * t_f}{2 * Vs} \qquad (10.44\text{-}1)$$

Vs equates to 36V, the output voltage or drain voltage of Q4. The simulated period of switching estimates 2.6us as t_f's value. A 0.96pF snubber capacitance results from these parameters. The capacitor must discharge before the transistor turns on again. Equation (10.4-2) estimates the snubber resistance. Since $t_{on} = t_f$, the value of R_{SNUB} estimates 5420Ω.

$$R_{SNUB} < \frac{t_{on}}{5 * C} \qquad (10.44\text{-}2)$$

The snubber circuit with these values, however, did not reduce the current spike nor delay the rise of current. Therefore, snubber capacitance and resistance were manipulated until suitable

switching current and instantaneous power dissipation simulations were obtained. Snubber circuits add two additional components per MOSFET to this design. In total, turn-on and turn off snubbers potentially add sixteen passive components to the system. Adding snubber cells was eliminated due to its complexity and its numerous component additions to the final PCB.

10.5. Decreasing Input Resistance

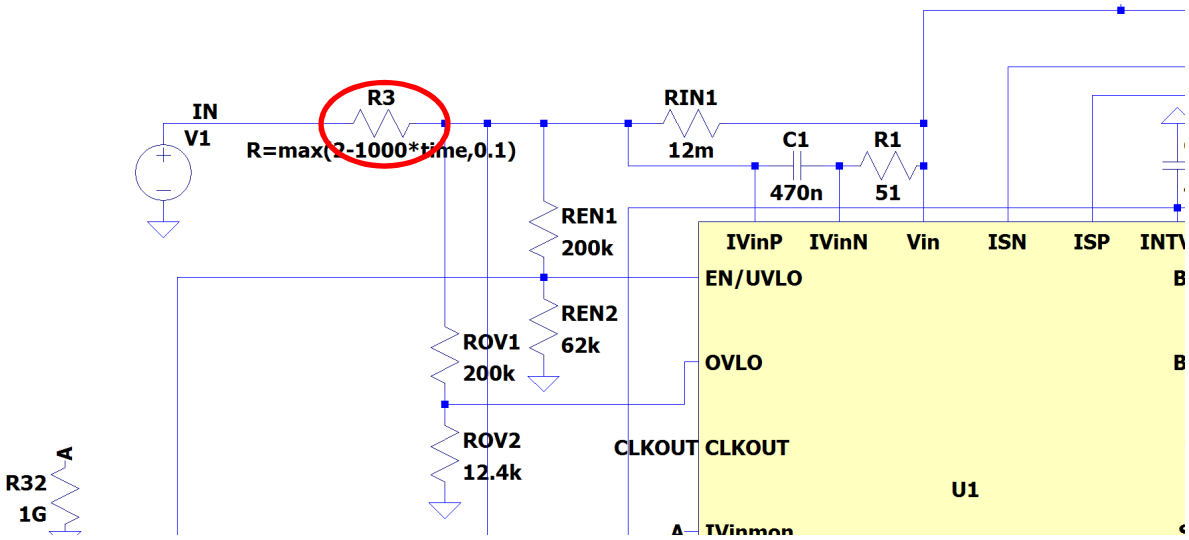

Figure 10-10: Parallel LT3791-1 Buck-Boost Converter Topology with IXTH180N10T MOSFETS decreasing input source resistance

Dr. Braun suggested implementing a decreasing input resistance to mitigate input power transients resultant of Q1 switching. The added input resistance shown in Figure 10-10 starts at 2Ω and decreases by 1Ω every millisecond because simulations generally range from 2ms to 7ms. Ideally, input resistance falls to 0.1 Ω before output voltage reaches 36V steady state.

Higher than nominal power peaks persisted despite the added input resistance. Figure 10-11 displays a 50V input case using the declining input resistance from Figure 10-10. Input power represented by the gray trace peaks above 300W near 1.5ms. The elliptical generator's output does not provide more than 250W at 50V. Furthermore, input power transients appear during system steady-state. Figure 10-12 displays a comparative green input power trace with more noticeable

transients as the device V_{OUT} charges up to 36V. Therefore, a declining input parasitic resistance was deemed not a suitable solution for limiting system input power.

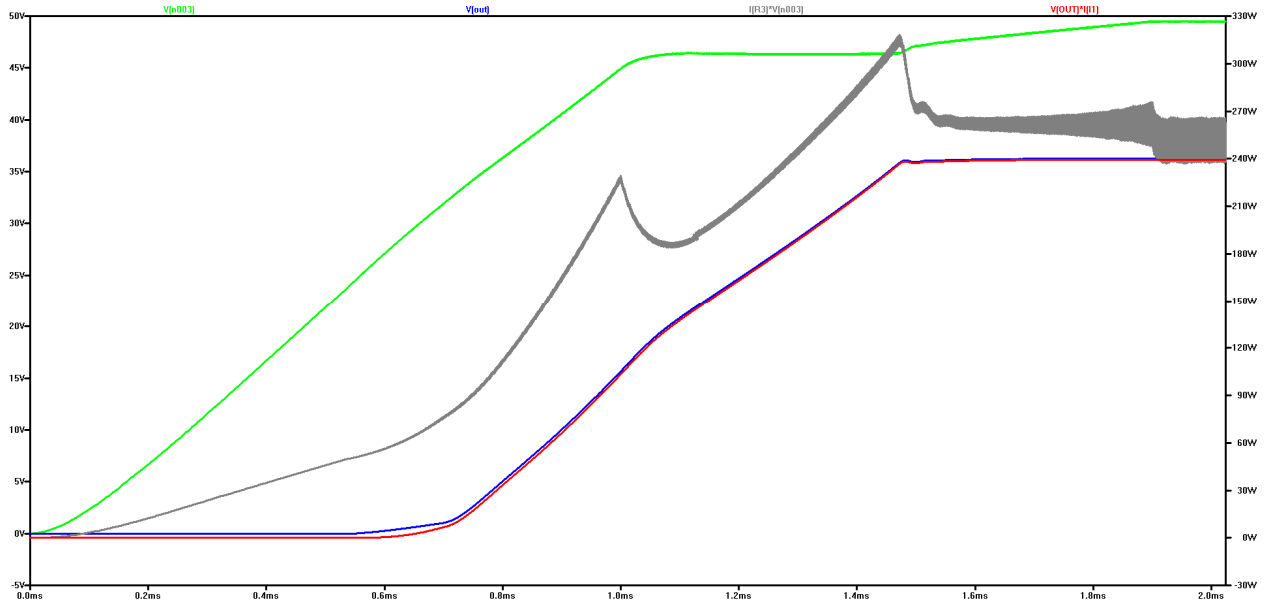

Figure 10-11: Parallel LT3791-1 Buck-Boost Converter Topology with IXTH180N10T MOSFETS with decreasing input resistance simulation, 50V, 250W input

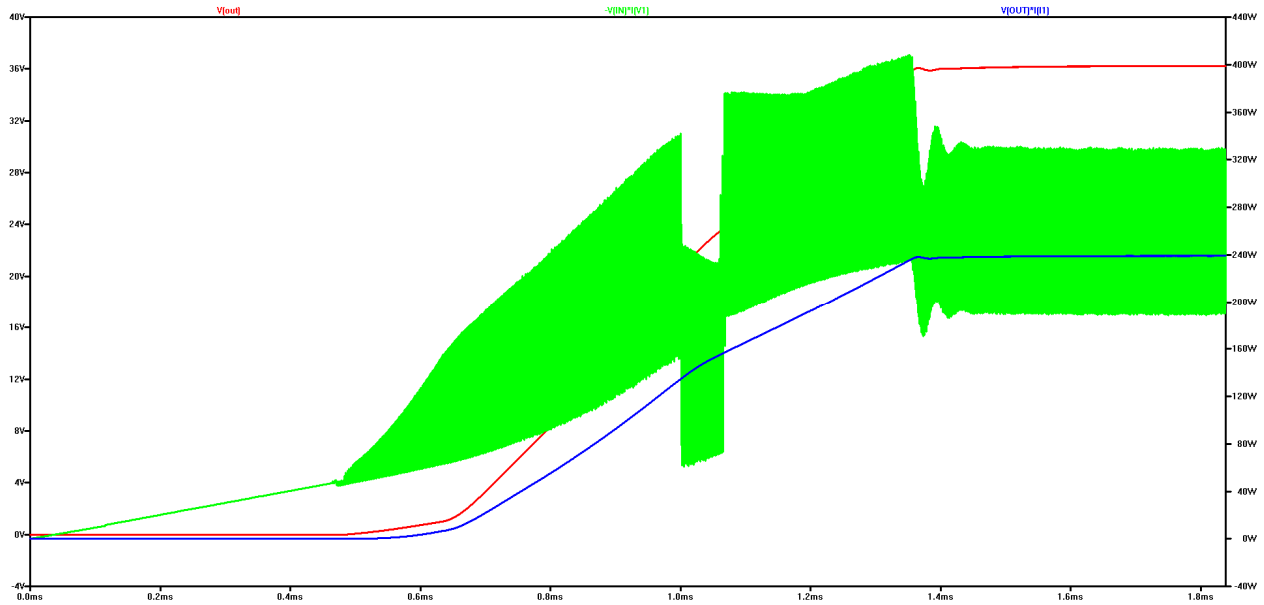

Figure 10-12: Parallel LT3791-1 Buck-Boost Converter Topology with IXTH180N10T MOSFETS without decreasing input resistance simulation, 50V, 250W input

10.6. Heat Sink Selection

Table 10-3 displays two heat sinks considered for this design. Power MOSFETs require adequate heat sinking to prevent thermal damage to the MSOFET package resulting from power dissipation. Each MOSFET requires a heat sink. Critical heat sink parameters include physical size and natural thermal resistance. Small heat sinks with low thermal resistance should are prioritized used because PCB space is limited to 2.5" by 3.8" board size based on ExpressPCB's Miniboard service.

Table 10-3: Heat Sink Comparison

Heat Sink	 Ohmite WA-T247-101E [18]	 Ohmite C247-025-1AE-ND [19]
Size	0.72" x 0.63"	0.98" x 0.785"
R_{S-A} Natural	11°C/W	Not Available
R_{S-A} Forced Air Flow	8°C/W @ 500 LFM	6°C/W @ 350 LFM
Cost per unit	$2.13	$3.77

Initially, selecting an Ohmite WA-T247-101E heat sink, featuring a 0.72" by 0.63" footprint and 11^{o}C/W natural thermal resistance, fulfilled this design. At high loads, simulated IXTH180N10T power dissipation averages 8W. Therefore, the Ohmite WA-T247-101E should maintain MOSFET temperature at high loads to 88^{o}C, or 113^{o}C considering an additional 25^{o}C ambient room temperature. 113^{o}C remains under IXTH180N10T's 175^{o}C maximum operating temperature.

However, Digikey and Mouser stock ran out of the WA-T247-101E; therefore requiring the selection of a new in-stock replacement heat sinks. Heat sink reselection proved difficult because the PCB ordering occurred before ordering parts. Thus, MOSFET spacing was not ideal for heat sinks specified larger than WA-T247-101E's footprint. Selecting an Ohmite C247-025-1AE-ND as a suitable replacement fulfilled size constraints. The C247-025-1AE-ND compares larger than the WA-T247-101E, 0.98" x 0.785" compared to 0.72" by 0.63". The newly selected heat sinks fit on the PCB layout tightly. Furthermore, the C247-025-1AE-ND's datasheet provides no natural thermal resistance rating, but lists a 6°C/W R_{SA} at 350 LFM. Therefore, a fan was highly advised fan during testing stages.

Chapter 11: Final Design

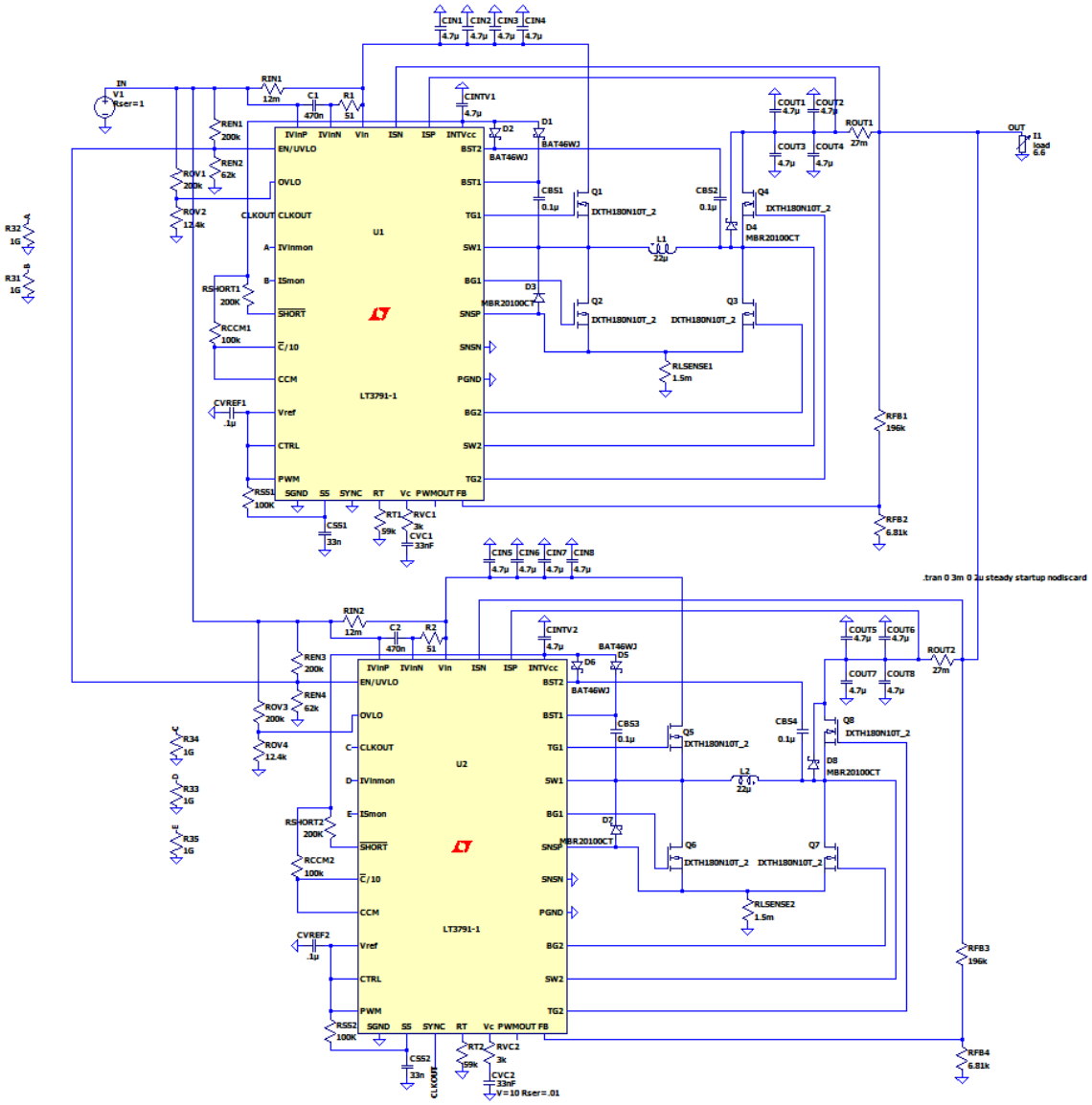

Figure 11-1: Final Parallel LT3791-1 4-Switch Buck-Boost Configuration

Figure 11-1 displays the final parallel LT3791-1 Four-Switch Buck Boost controller design including Chapter 10 MOSFET, capacitor, and inductor alterations. Section 17.F displays LTspice's steady-state Efficiency Report 6V, 10V, 20V, 30V, 40V, and 50V input cases results.

summarizes Efficiency Report results. Higher than nominal power inputs persisted despite circuit alterations and additional source parasitic resistance. Figure 11-2 displays a 50V, 250W input case with 270W input power peaks as the system charges to regulate a 36V output. Figure

11-3 displays a 10V, 1W case with 50W input power peaks as the system charges. Neither input power cases are possible in a real world scenario because the elliptical machine's on-board generator limits converter input power. Therefore, this project heavily relies upon analyzing system's steady-state operation which operates within input power parameters at all input powers. Section 17.F includes all steady-state efficiency reports and the final design's SPICE Netlist. Specifically, simulated steady-state input power should approximately equal nominal input power. Figure 11-4 presents an updated single stage schematic including updated component names for easier recognition. Future testing shall determine proper circuit operation compared to steady-state analysis reports.

Table 11-1: Final Design Test Cases

Nominal Input Cases				**Expected Output Cases**			
Input Voltage [V]	**Input Current [A]**	**Input Power [W]**	**Eff. [%]**	**Output Voltage [V]**	**Output Power [W]**	**Output Current [A]**	**Output Resistance [Ω]**
6	0.6	3.6	0.95	36	3.42	0.095	378.9
10	1	10	0.95	36	9.5	0.26	136.4
20	2	40	0.95	36	38	1.05	34.1
30	3	90	0.95	36	85.5	2.375	15.1
40	4	160	0.95	36	152	4.22	8.5
50	5	250	0.95	36	237.5	6.59	5.4

17.F Steady State Efficiency Report Summary

Nominal		**Simulation**					
Input Voltage [V]	**Input Power [W]**	**Parasitic Resistance [Ω]**	**Input Voltage [V]**	**Input Power [W]**	**Output Voltage [V]**	**Output Power [W]**	**Eff. [%]**
50	250	1	44.4	247	36.3	239	96.9
40	160	1	35.4	162	36.4	155	95.2
30	90	0.9	26.7	90.4	36.2	86.8	96
20	40	0.9	16.9	38.6	33.4	35.9	93
10	10	0.5	9.1	9.71	34.1	8.54	87.9
6	3.6	0.1	5.94	2.95	31.2	2.5	84.6

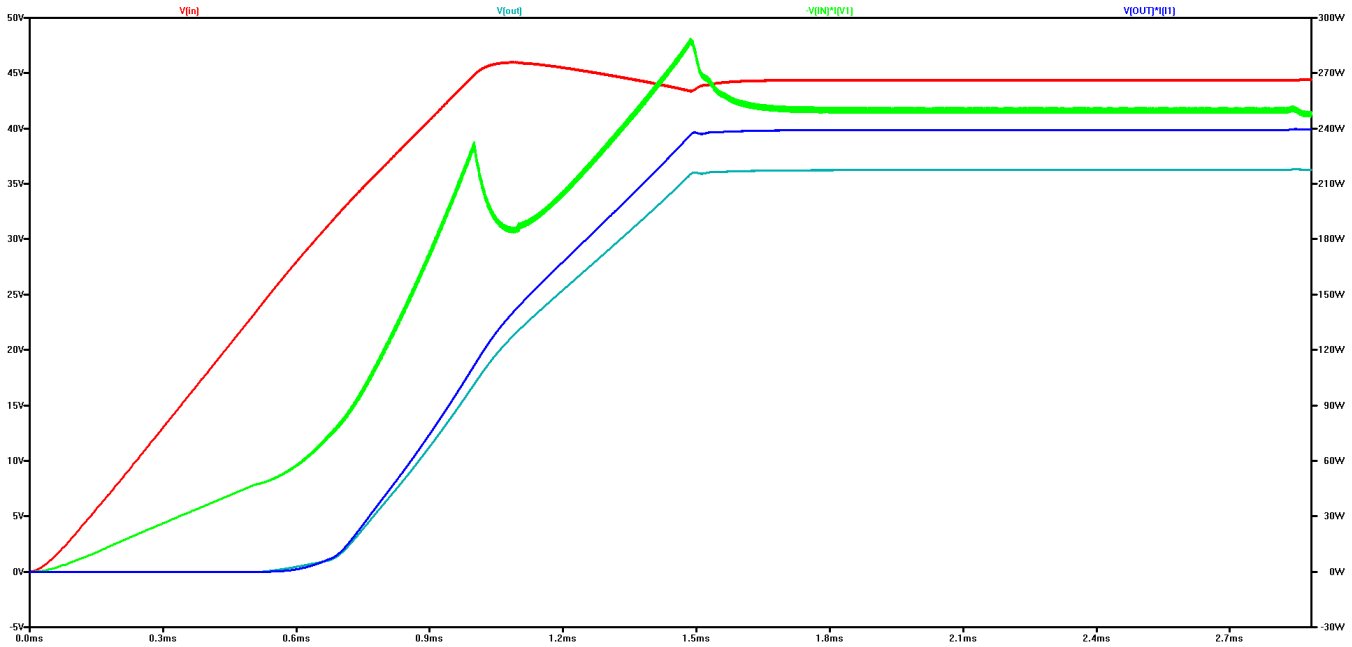

Figure 11-2: Final Parallel LT3791-1 4-Switch Buck-Boost Configuration
50V case and 1Ω parasitic input resistance
Input Voltage (Red), Output Voltage (Cyan), Input Power (Green), Output Power (Blue)

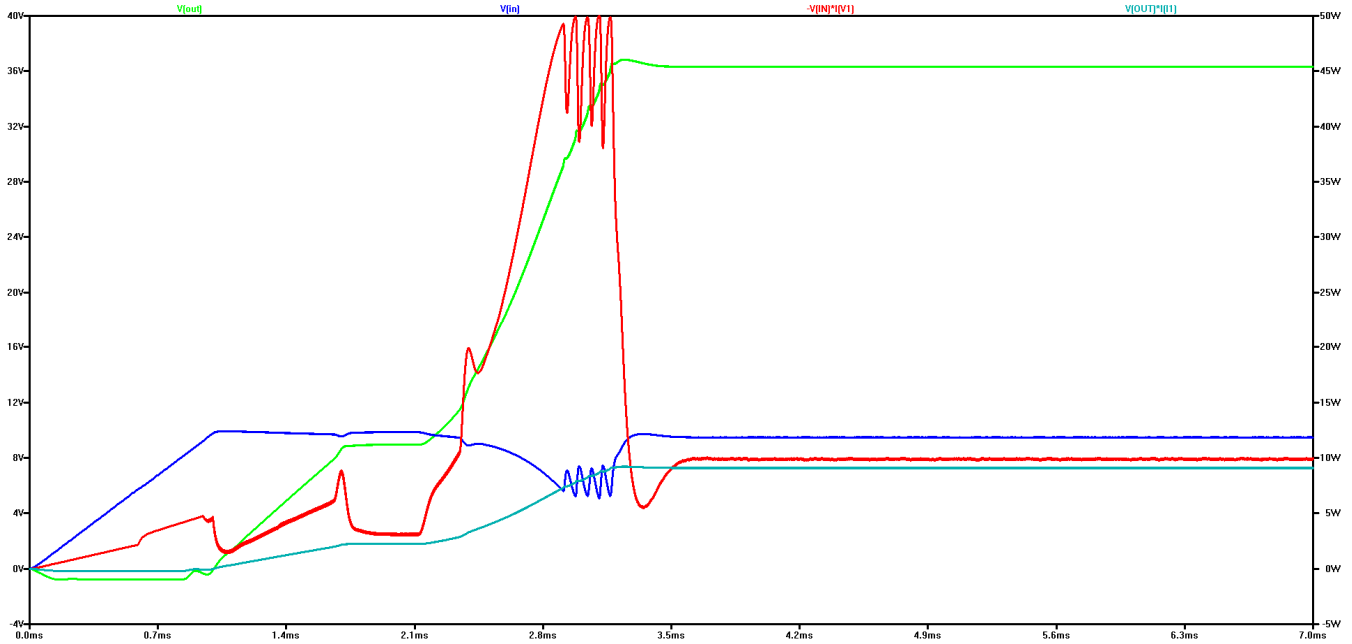

Figure 11-3: Final Parallel LT3791-1 4-Switch Buck-Boost Configuration
10V case and 0.1Ω parasitic input resistance
Input Voltage (Red), Output Voltage (Cyan), Input Power (Green), Output Power (Blue)

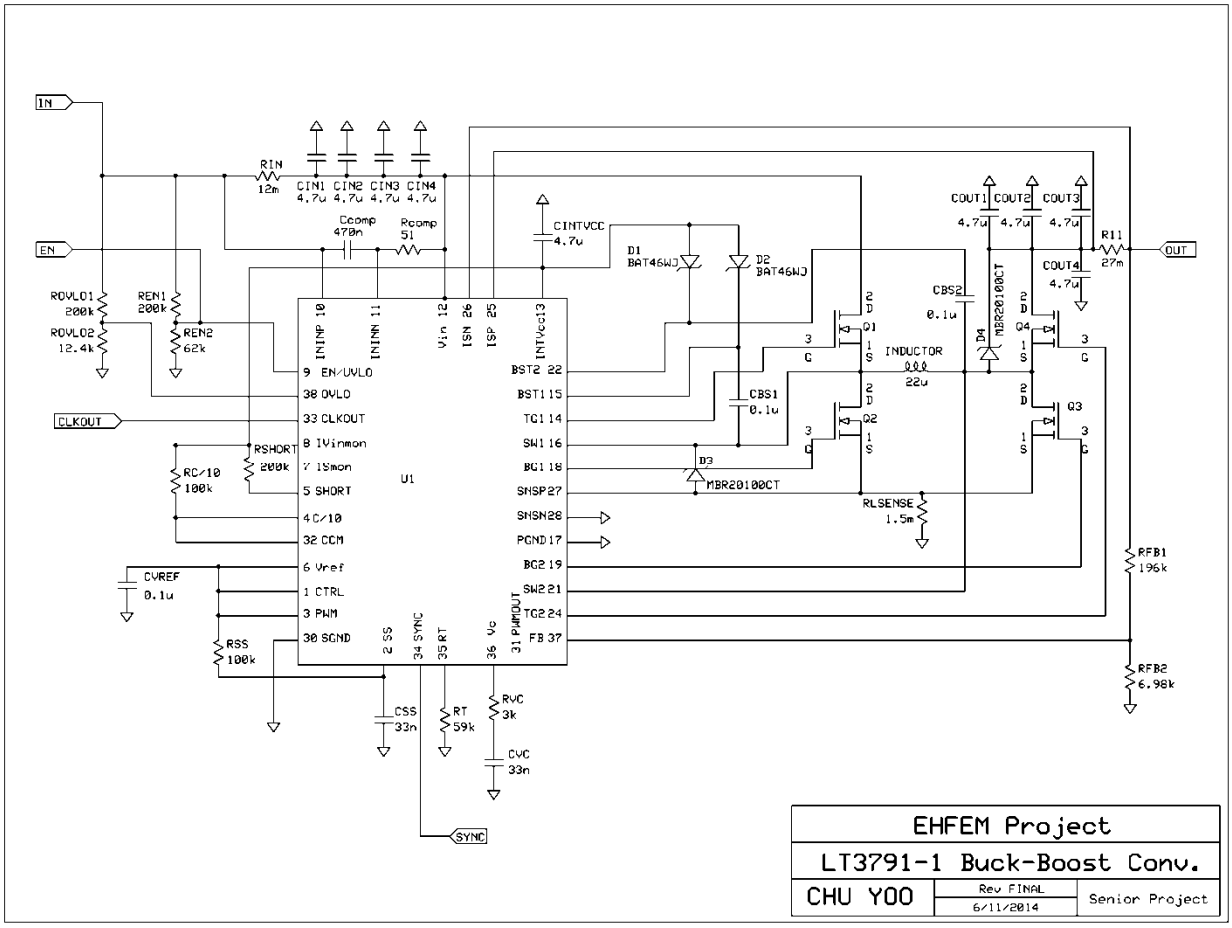

Figure 11-4: Final Single Stage LT3791-1 Design Schematic with altered component names

Chapter 12: PCB Design and Assembly

12.1. First Iteration

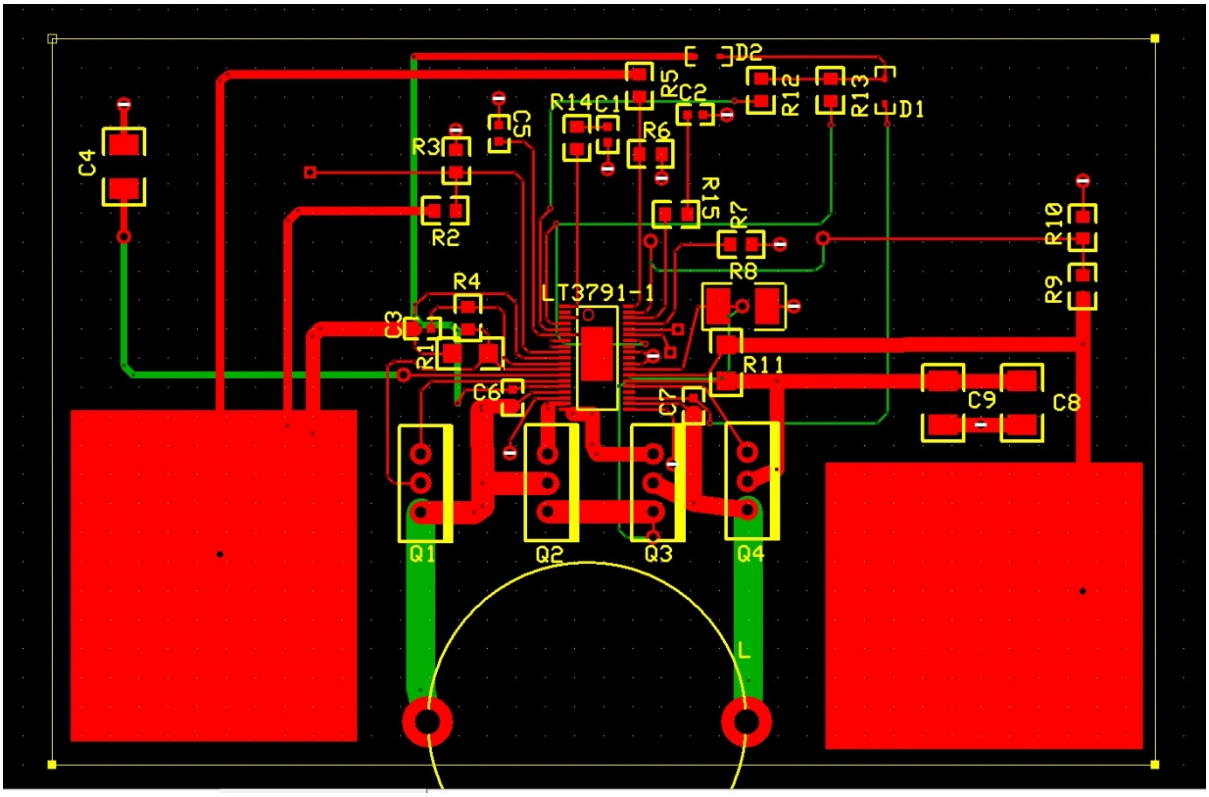

Figure 12-1: First PCB Iteration

ExpressPCB Miniboard PCB manufacturing service offers three 2-layer boards for $75.00 or three 4-layer PCB boards for $98.00 plus shipping and handling. The Miniboard option offers three identical 2.5” x 3.8” boards designed using ExpressPCB’s proprietary schematic and PCB design software. Initially selecting a two-layer design minimized PCB cost, although a costlier 4-layer board provides top and bottom layers for copper traces and two inner power or ground planes.

Figure 12-1 displays the initial PCB design using a 2-layer board. Large input and output copper filled planes handle large input and output currents. Large input and output copper planes also provide ample power plane heat dissipation. This draft, however, had various functional flaws. For example, the initial design lacked additional input capacitor pads. Furthermore, undersized

drain and source traces connected to the power MOSFETs may inadequately handle expected current flow. Most MOSFET source and drain traces face potential damage under initial design conditions because traces inadequately sized to carry expected current.

Furthermore, the initial design phase did not consider MOSFET heat sink footprints. This design lacked adequate board spacing between each MOSFET accommodating additional heat sink components. Additionally, placing power MOSFETs close to each other degrades natural airflow and decreases the natural cooling of each power MOSFET. Pin 29, TEST1, lacked a SGND connection as prescribed in LT3791-1's datasheet. Ground return paths between output sensing resistor, R11, and Q3's source were not considered and would have generated noise on the output sensing resistor's copper trace. Q3's source should connect directly to the output sensing resistor to mitigate noise. Multiple traces between LT3791-1 and Q4 interfered with straightforward connections between Q3's source and the output current sensing resistor. Using back traces connected to vias solve interference problems. Additionally, critical sensing components spread widely with long traces throughout the board generate noise problems. Traces carrying analog signals, especially from sensing components, require minimal trace lengths to minimize noise

12.2. Second Iteration

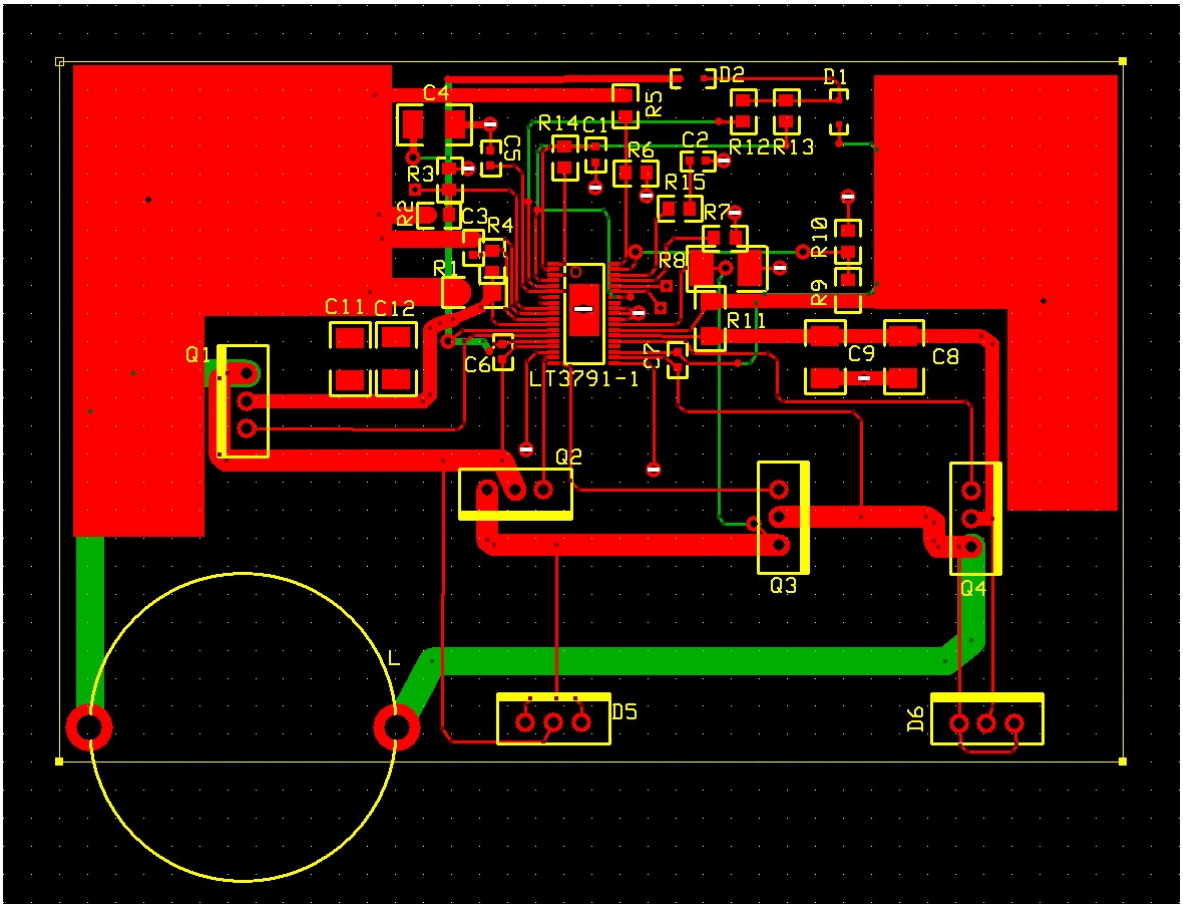

Figure 12-2: Second PCB Iteration

Figure 12-2 displays Figure 12-1's revision. Considering a 4-layer PCB design increased available copper trace, ground, and power plane space. 4-layer PCBs include a top layer, power layer, ground layer, and bottom layer. Top layer traces connect most of the power components including MOSFETs, input and output planes, power inductor, and analog signal components. Bottom layer traces connect components when components could not connect on the top layer. All components requiring ground connections connected to ground plane using direct throughput vias. The 4-layer board's ground plane allowed elimination of previous multiple ground traces using traces and vias.

Despite board space efficiency improvements, certain traces remained undersized concerning current carrying capability. Specifically, traces connecting MOSFET sources, drains, and bootstrap capacitors, C6 and C7, were too thin to handle the simulated current flowing through them. Improperly sized high-current carrying traces connected Q2 and Q3's additional Schottky diodes. Furthermore, the additional Schottky diodes interfered with connecting the inductor's traces on the top plane. However placing back-board high-current carrying traces poses may generate noise on components or traces above the inductor's traces. Relocating the MOSFETs farther apart accommodated space for potential heat sink additions. No heat sinks were selected at this point. Placing the MOSFETs farther apart to accommodate heat sinks also increased distance between LT3791-1's gate drivers and MOSFET gates. Minimal distance between the MOSFETs gates and LT3791-1's gate drivers reduces high frequency trace noise.

12.3. Third Iteration

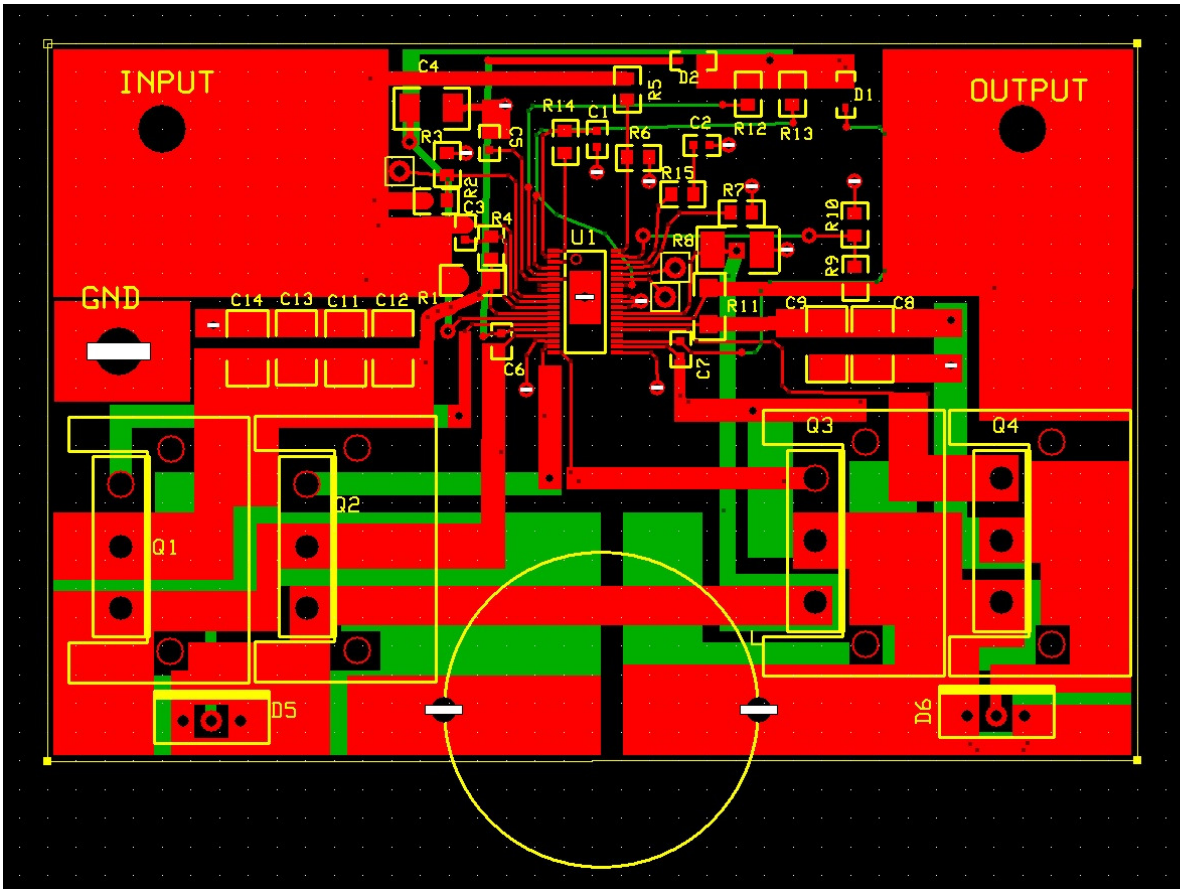

Figure 12-3: Third PCB Design Iteration

Figure 12-3 displays Figure 12-2's revision. Modifications include two extra input capacitors, decreased spacing between output capacitors, and a banana jack testing connection. Matthew Wong added additional copper to high current traces to increase trace sizes between power MOSFET sources and drains, inductor, Schottky diodes, and sensing resistors. Furthermore, additional silkscreen heat sink outlines estimate MOSFET spacing. Two MOSFETs placed close to each other increases the thermal resistance of heat sinks and decreases nearby natural airflow thereby decreasing heat sink thermal effectiveness. Increasing empty air space between heat sinks increases effective natural air flow and aid cooling. Additional bottom trace copper increases thermal dissipation generated by high current flow. Appropriate through-hole vias

connected to pins 9, 33, 34 allow header pin connections for EN, CLKOUT, and SYNC signals. Relocating power components creates direct traces from the inductor to the MOSFETs. A through-hole via facilitates a direct connection between the output sensing resistor and Q3's source which experienced interference from other traces. A direct via connects pin 39, SGND, to an SGND plane.

12.4. Fourth Iteration

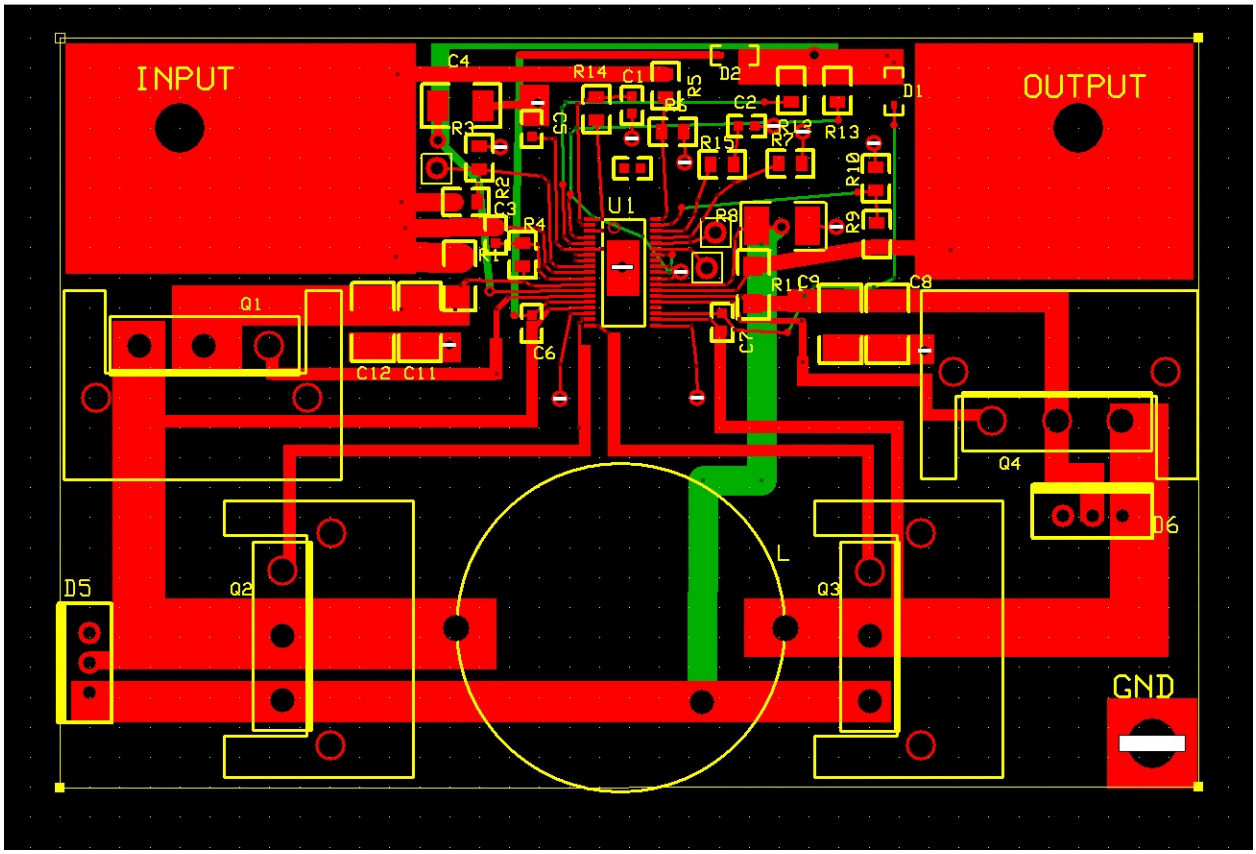

Figure 12-4: Fourth PCB Design Iteration

Figure 12-4 displays Figure 12-3's revision. Unnecessary bottom copper planes bottom layer were removed because current generally flows through the shortest path from source to destination. Relocating MOSFETs created air gaps which allow increased natural air flow with minimal heat sink contact. Moving the ground pin to the bottom right-hand side of the board

provides space for Q1. Moving Q4 higher on the board required reducing the outpour copper plane size. Q4's drain also connects directly to output capacitors C8 and C9.

12.5. Fifth Iteration

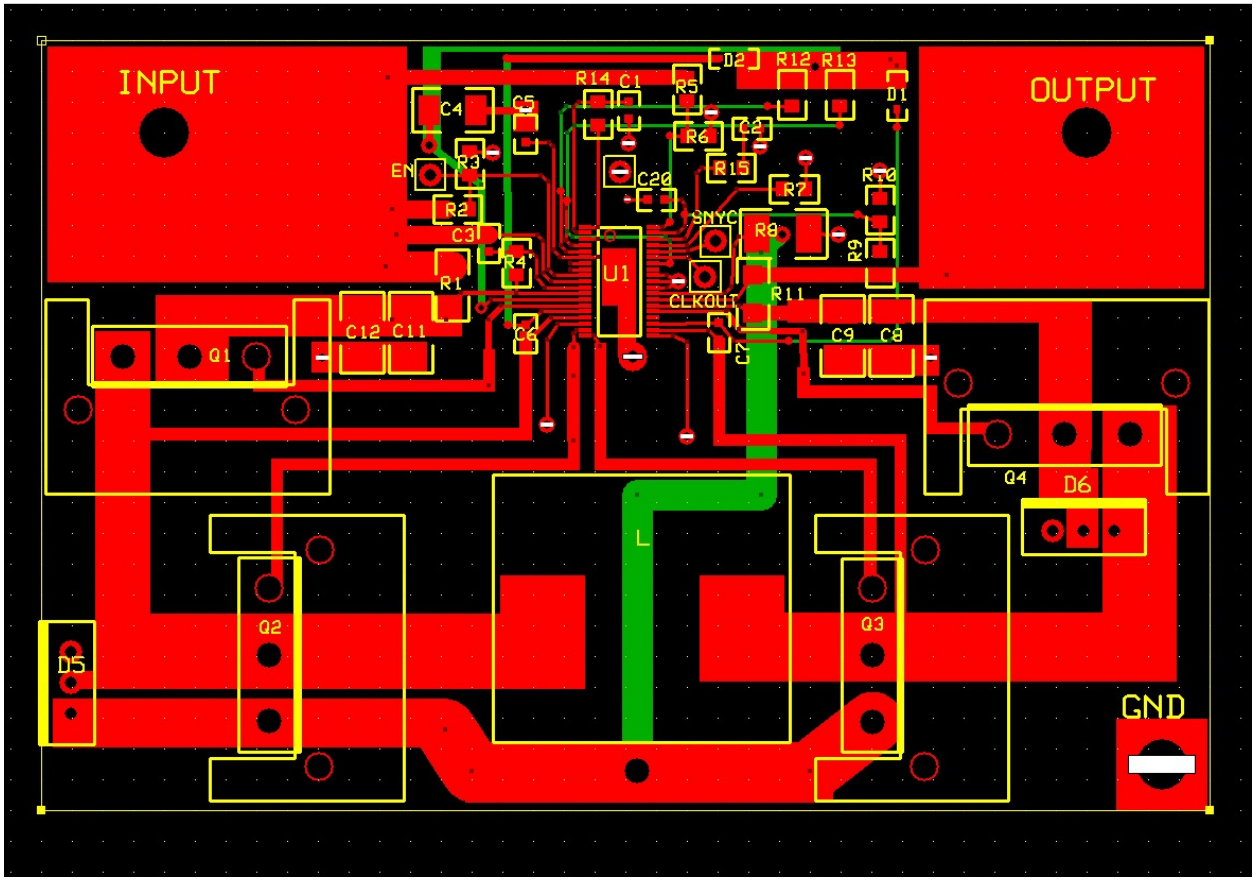

Figure 12-5: Fifth PCB Design Iteration

Figure 12-5 improves upon Figure 12-4's PCB design. A new shielded inductor prevents electromagnetic field influencing nearby traces and components. The new inductor features a low square surface mount profile. Placing traces outside of the silkscreened inductor boundaries minimizes inductive interference with traces. LT3791-1's ground through-hole via shifted below the controller to provide more pad contact.

12.6. Final Iteration

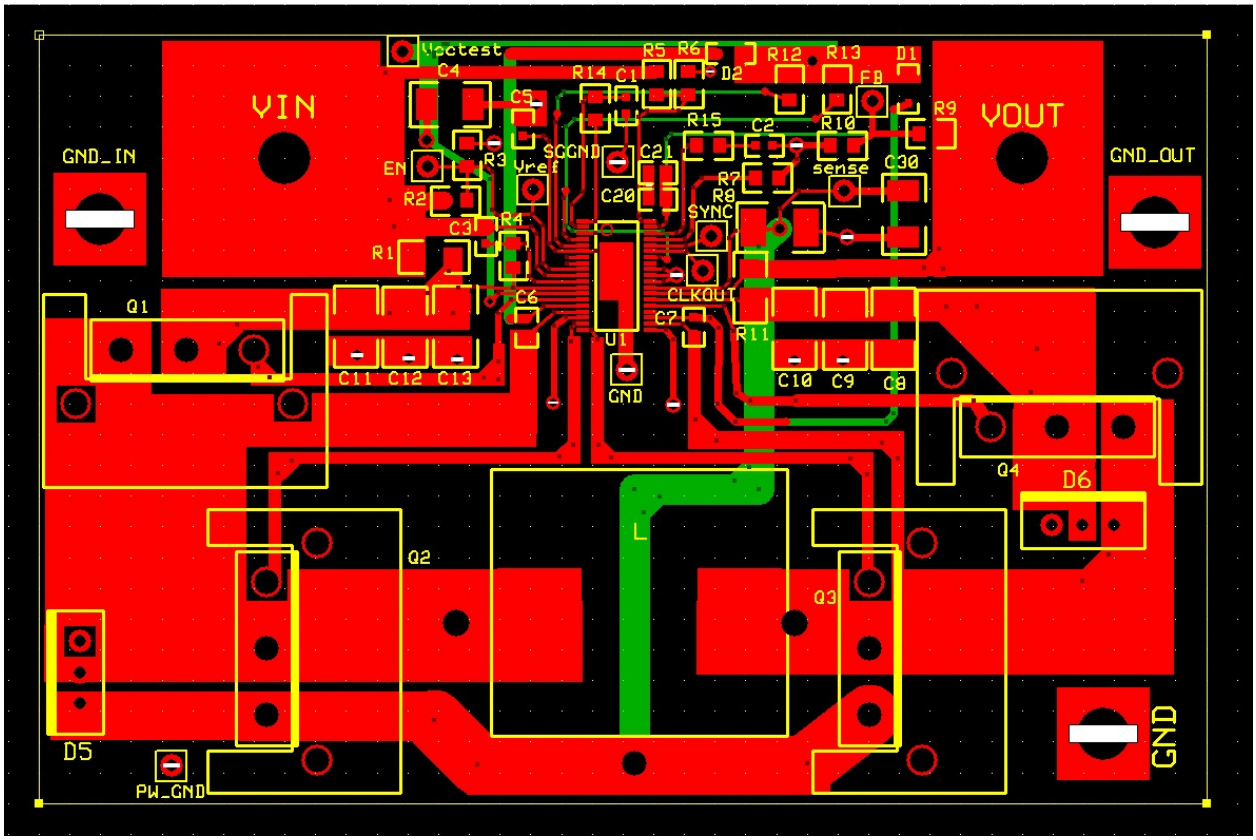

Figure 12-6: Final PCB Design Iteration

Figure 12-6 displays the final PCB design iteration. Four additional through-hole vias accommodate VREF, FB, inductor current sense, and Vcctest header pins. An additional via accommodates a header pin connected directly to SGND. Additional extra capacitors pads added to FB and output sensing resistor for future use. The final design iteration also features additional input and output capacitors pads. Since traces connecting power side of the board, mostly MOSFETs and inductor, carry a lot of current, 45 degree corners were added to every corner trace. An additional via to the bottom-left corner provides a PGND header test pin. Input and output grounds were also added adjacent to the copper input and output planes.

12.7. Solder Order and Assembly

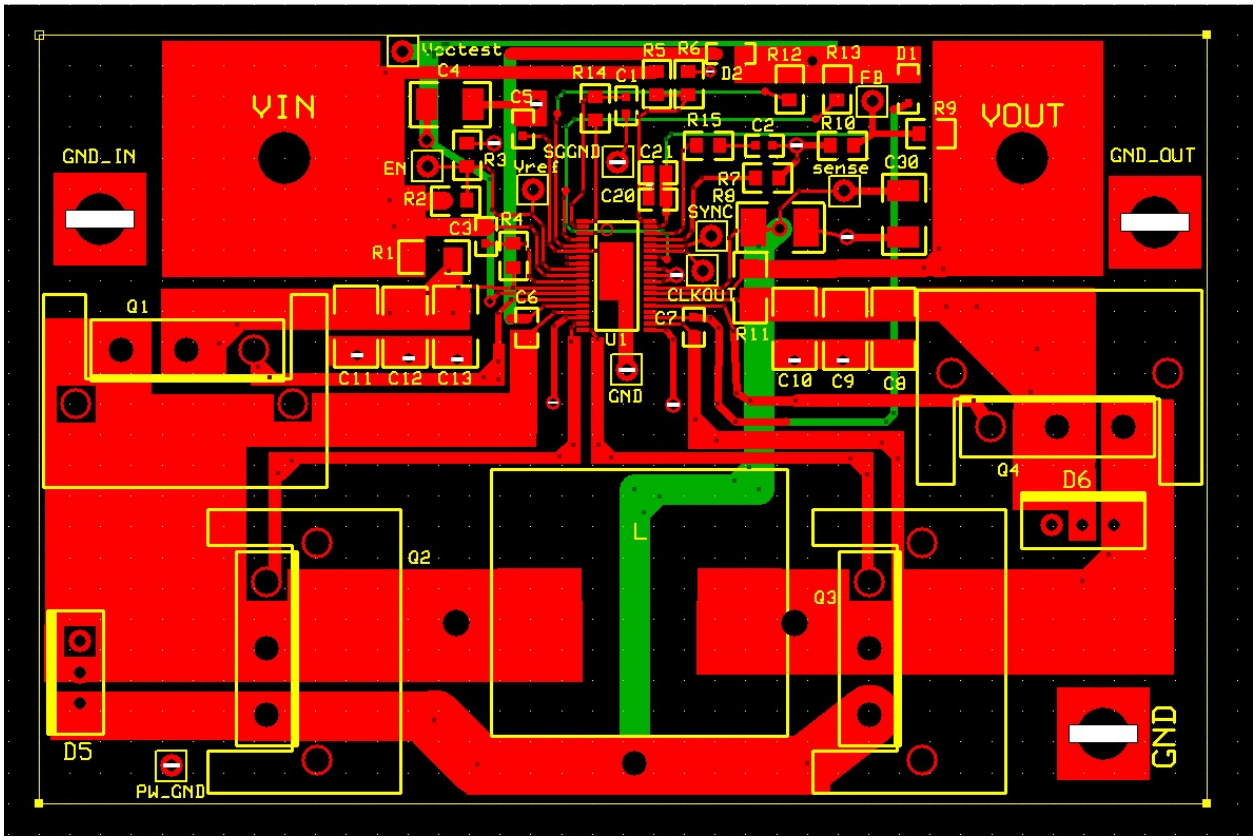

Figure 12-7: Final PCB Schematic

Table 12-1: Component Soldering Order
Red components are optional

1. LT3791-1	12. R2	23. C1	34. R9
2. C20	13. C4	24. D2	35. Inductor
3. C21	14. C5	25. R5	36. Q1
4. C11	15. C7	26. R6	37. Q2
5. C12	16. R11	27. C2	38. Q3
6. C13	17. C10	28. R15	39. Q4
7. R1	18. C9	29. R12	40. D5
8. C3	19. C8	30. R13	41. D6
9. R4	20. R8	31. D1	42. Header Pins
10. C6	21. R7	32. R10	
11. R3	22. R14	33. C30	

Table 12-1 displays component soldering order corresponding with the ease of soldering components based on Figure 12-7. Red components feature optional capacitor pads for filtering

sense resistor noise. Generally, soldering small or complex components prioritizes over larger components. Therefore soldering through-hole components, such as MOSFETs and Schottky Diodes, yield lesser priority. Complex components containing many pins, like the LT3791-1 controller, should be soldered first due to its 38-pin TFSOP design.

Prioritizing certain components increased the eased hand soldering, knowing that the soldering iron's tip would not fit certain directions. Soldering started on the left-hand side of the PCB. For example, soldering C11, C12, and C13 prioritized over R1 because soldering R1 first prohibits effectively soldering the C11, C12, and C13's top pads. Additionally, soldering R11, C11, C10, and C9 before R8 eases R11 and C11's soldered without interference from R8's package. The inductor mounted last because it was the biggest package and produced the largest soldering obstacle.

Through-hole mounted components mounted second-to-last. Q1, Q2, Q3, and Q4 mounted with their heat sinks attached. Mounting the MOSFETs without heat sinks attached proved a problem for Q3 and Q4 because their clips open or close when mounted due to conflicting and obtrusive orientation. Header pins were mounted last with their plastic bodies atop the PCB and soldered on the back board.

Soldering occurred procedurally. For example, LT3791-1's IC soldered first on all boards, then C11, then C12, then C13, etcetera until all components were mounted. Continuity checks occurred at each soldering phase. All soldered components passed continuity checks. Continuity checks involved testing for continuity between a target pin and all expected connecting pins or pads based on Figure 12-7. Figure 12-8 displays the finished PCB after soldering all components.

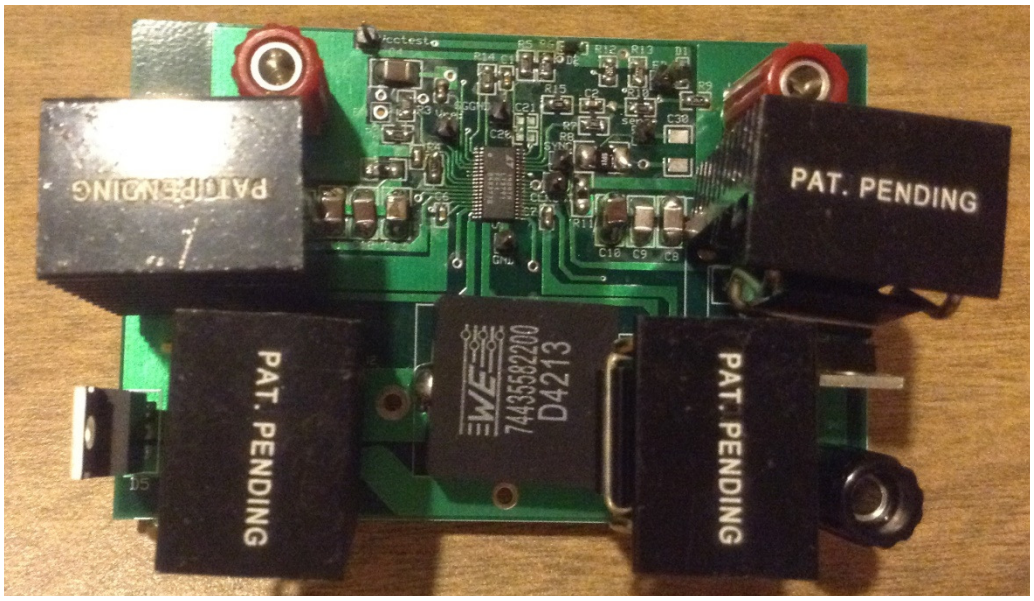

Figure 12-8: Soldered and assembled PCB

Chapter 13: Input Protection Circuit Design

13.1. Previous IPSC Design

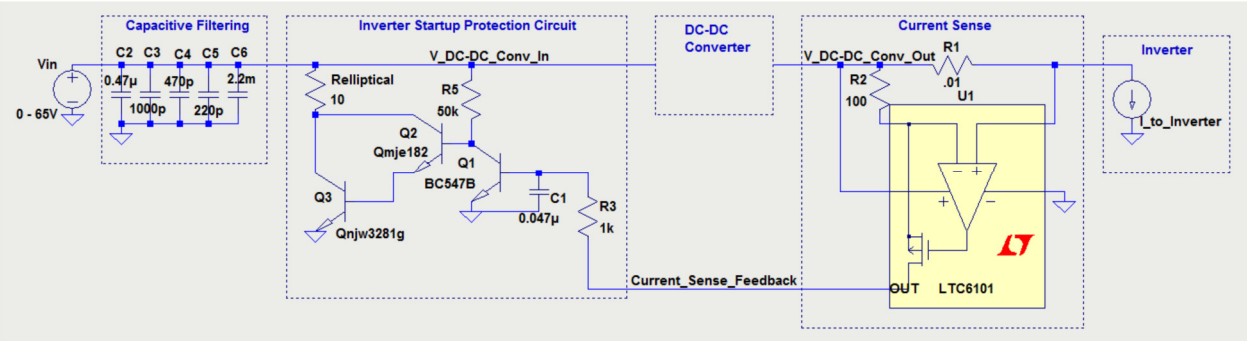

Figure 13-1: Ryan Turner and Zack Weiler's Input Protection Circuit [2]

Ryan Turner and Zack Weiler's input protection circuit provides a baseline modifiable input protection scheme. Their testing indicated the Enphase Micro-inverter effectively operates as an open load during its initial five minute start-up phase, which leads the DC-DC converter to build up charge at its input. Their IPSC design prevents adverse converter damage by providing an alternate path to dissipate excessive generated power during the inverter's start-up.

Their design utilizes a LT6101 High Voltage, High-Side Current Sense Amplifier comparator to detect changing current flow through a current sensing resistor. This sensing resistor, placed in series with the converter output and inverter input, does not experience a voltage drop during an absence of current flow due to an the open load condition at the inverter. The comparator outputs a low signal when the current sense resistor detects no current flow. This signal inverts and amplifies to become a high signal which enables an alternate path to safely dissipate excessive power instead of damaging the converter.

However, this methodology only protects the system from built up charge due to an open inverter load during start-up phase and not necessarily from overvoltage situations. Their design included a capacitor array to filter input voltage and reduce hazardous voltage transients up to 150V. Over the course of their testing they found that their capacitors innately smoothed input

voltage to approximately 60V during peak elliptical power generation. Their circuit does not hard-limit a specific voltage applied to the converter.

13.2. Modified Input Protection System Design

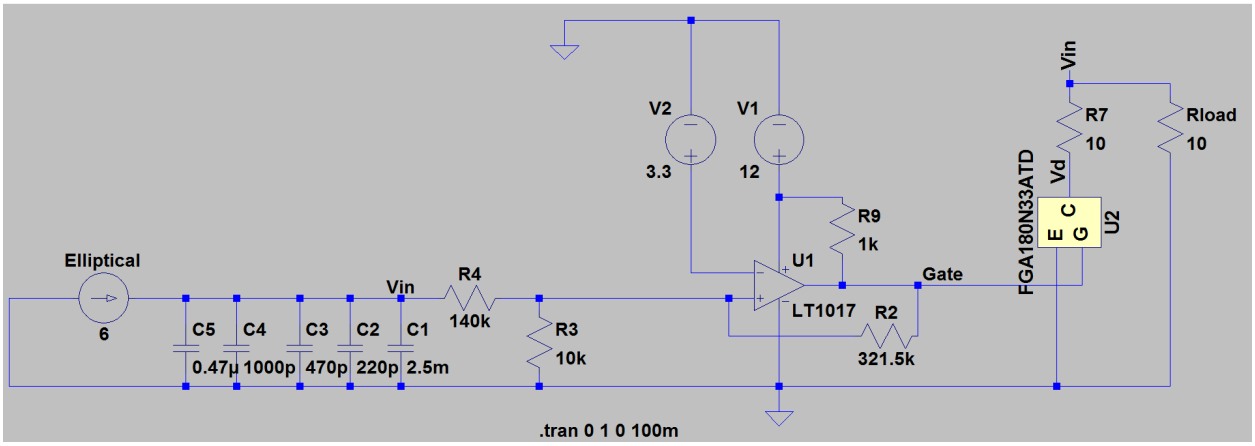

Figure 13-2: Cameron Kiddoo and Eric Funsten's Protection System

Cameron Kiddoo and Eric Funston's senior project designed a current limiter and overvoltage input protection system. Their design includes Turner and Weiler's capacitive filtering array, C1 through C5, as shown in Figure 13-2, to filter out high frequency transient responses induced by the elliptical's generator. Kiddoo and Funston's design implements an additional current limiter to protect the micro-inverter from receiving more than 8A input current from the converter. This discussion only includes their design characteristics relevant to the converter's input protection because their current limiter design diverts current away from the micro-inverter and does not directly influence converter functionality.

An LT1017 Micropower Dual Comparator controls the gate of a Fairchild Semiconductor FGA180N33ATD Insulated Gate Bipolar Transistor, or IGBT. The elliptical machine's on-board battery powers the LT1017 comparator. An input voltage divider, R3 and R4, tied to LT1017's V_+ input pin, outputs 3.3V at a 50V input. The LT1017 compares the voltage divider's output to a 3.3V reference supplied by the current limiter's microcontroller. The comparator then outputs a

high signal through a pull-up resistor, R9, when V_+ surpasses the 3.3V reference voltage. Therefore, input voltages higher than 50V causes the IBGT to turn on, thereby diverting current flow through R7 instead of the converter. The comparator outputs a low signal while input voltages remain below 50V, during which the converter functions properly. Kiddoo and Funston's design effectively filters input voltage transients and limits converter input voltage to 50V.

Chapter 14: Hardware Testing

14.1. Test Plan

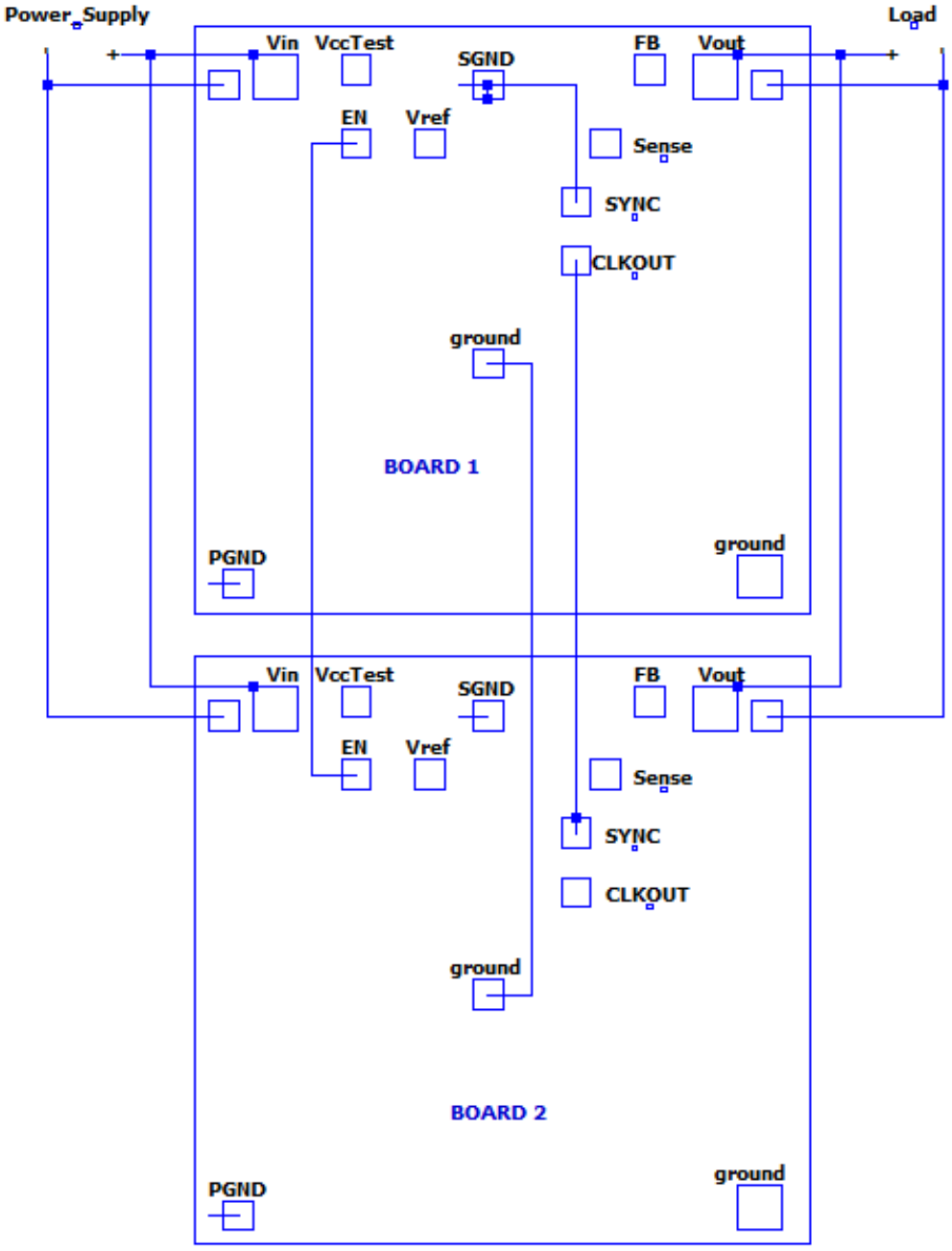

Figure 14-1: Parallel LT3791-1 4-Switch Buck-Boost Controller Test Configuration

Preemptive testing using a DC power source must occur before connecting the converter to the elliptical machine to prevent damage to the converter or other components. Figure 14-1 displays two parallel LT3791-1 4-Switch Buck Boost Controller PCBs with an input power supply and output electronic load. The following discussion outlines this project's test plan.

Setup

1. Jumper wires interconnect the following header pins:
    a. EN
    b. Grounds in center of boards
    c. Primary board CLKOUT to secondary board SYNC
    d. Primary board SYNC to SGND
2. Banana-to-spade leads interconnect:
    a. Power supply to positive and negative terminals of VIN
    b. Electronic load to positive and negative terminals of VOUT

Procedure

1. Connect pins, inputs, and outputs as described in Setup.
2. Table 14-1**Error! Reference source not found.** outlines tests cases where using a power source limiting input voltage and current l and electronic load configured for corresponding output voltage/currents.

Table 14-1: Expected Input and Output Test Cases

Input Voltage [V]	Input Current [A]	Input Power [W]	Estimated Efficiency [%]	Output Voltage [V]	Output Current [A]
6	0.6	3.6	90	36	0.09
10	1	10	90	36	0.25
20	2	40	90	36	1
30	3	90	90	36	2.5
40	4	160	90	36	4
50	5	250	90	36	6.25

3. Configure the power source's output voltage and current limit according to Table 14-1.

4. Configure the electronic load in constant-current mode to desired load current from Table 14-1.
5. Enable the power source, then enable the electronic load.
6. Record Vin, Iin, Vout, and Iout.
7. Turn off the power source then the electronic load.
8. Alter power source and electronic load parameters based on provided test cases.
9. Readings using multimeters or oscilloscopes must reference proper grounds. Probes measuring analog signal ground to SGND. Probes measuring power signals ground to PGND.

14.2. Test Results

6V Constant Voltage Load

This project's buck-boost converter design did not function properly for all test cases. The converter did not demand enough current from the power source; drawing less than 1A at all test cases. System output voltage measured 0V by the electronic load with no current drawn, indicating a malfunctioning circuit operation. The converter partially functioned correctly when the electronic load operated in constant voltage mode. In this case, the system demanded the expected amount of current from the source. The system demanded 0.6A at 6V from the power source. However, the converter's output could not maintain 36V, but output 10.36V. Setting the electronic load to constant voltage mode defeats the purpose of designing a converter to output 36V since the electronic load sets the output voltage. Testing should occur using constant-current mode so the converter self-regulates output voltage.

Multiple abnormalities presented themselves during the 6V test case under a constant-voltage load. Gate voltage of Q1, shown in Figure 14-2, suggests the system experiences

excessive MOSFET gate capacitance. High gate capacitance prohibits gate voltage from increasing to the necessary 5V gate drive output by TG1 of the LT3791-1 controller. Therefore, high gate capacitance prohibits proper MOSFET switching.

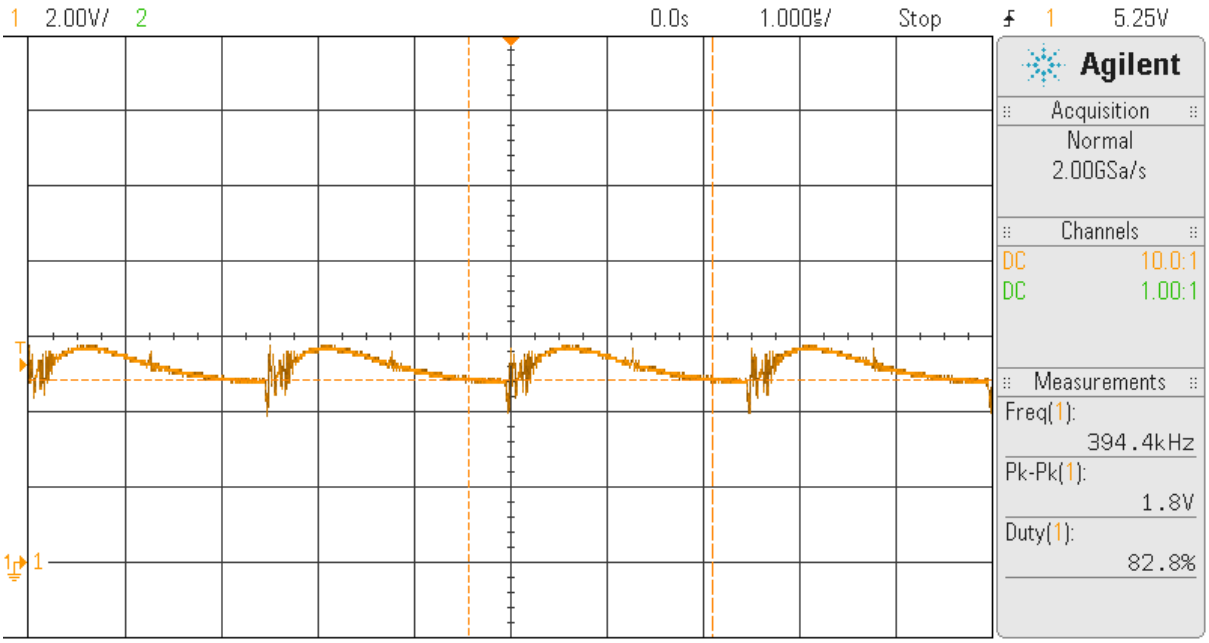

Figure 14-2: Primary Board Q1 Gate Voltage, 6V Input

Q2's drain connects to Q1's source which experienced no drain voltage because Q1 fails to switch on. Additionally, this problem signifies voltage build up across the power inductor. Q2's gate experienced gate drive problems as shown in Figure 14-3. Although a 399.7 kHz driving signal is apparent, gate voltage does not rise to 5V indicating proper gate drive from BG1 of the LT3791-1 controller.

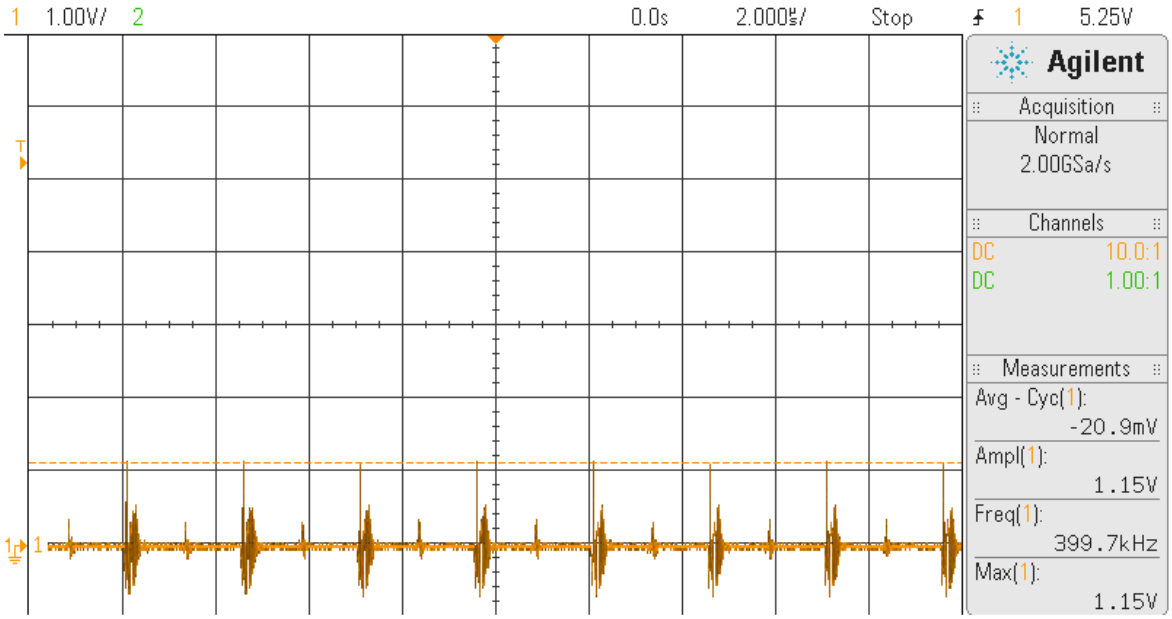

Figure 14-3: Primary Board Q2 Gate Voltage, 6V Input

Figure 14-4 indicates Q3 switching at 399.8 kHz at a 94.9% duty cycle. Q3 and Q4's gate drives mirror duty cycles. Figure 14-5 indicates Q4 switching at 399.8 kHz at a 7.6% duty cycle. This indicates that the two MOSFETs function properly.

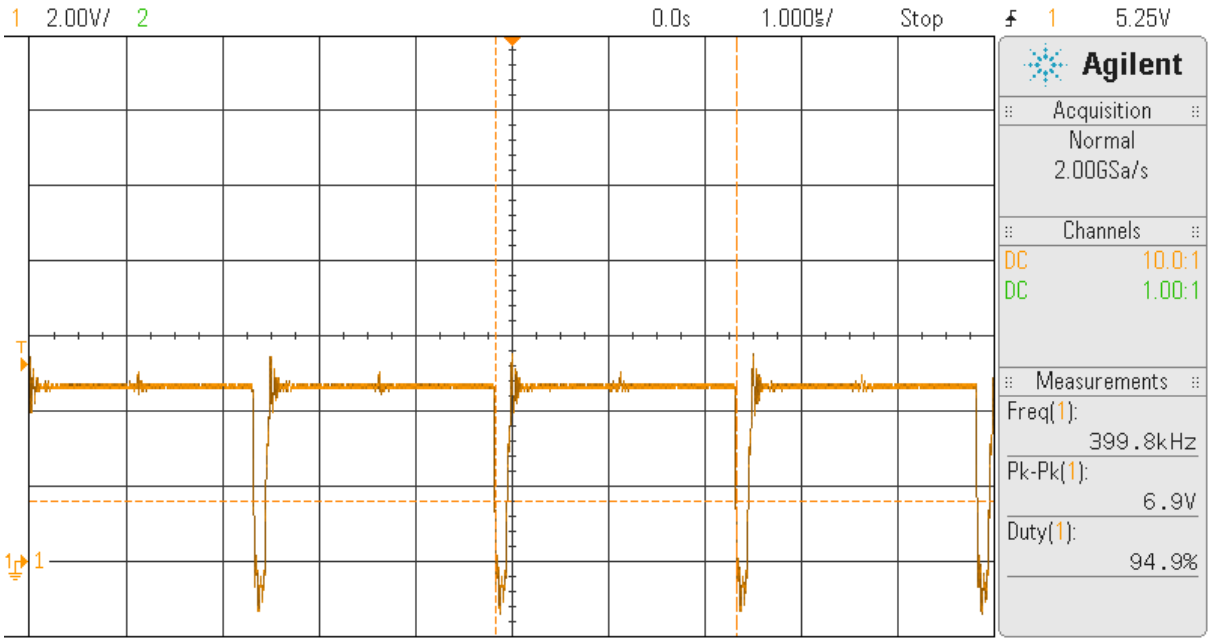

Figure 14-4: Primary Board Q3 Gate Voltage, 6V Input

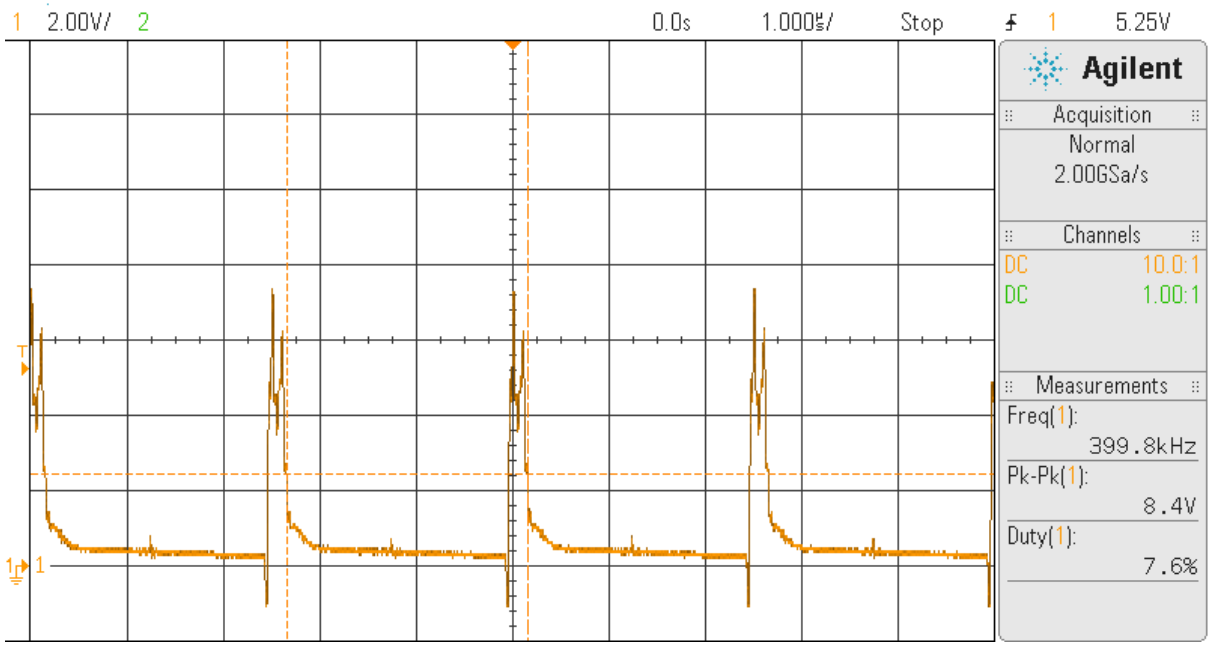

Figure 14-5: Primary Board Q4 Gate Voltage, 6V Input

30V Constant Current Load

Simulations indicate a 30V input case functions better than a 6V input case. Therefore, testing a 30V or 90W input case may yield better results than a 6V case. Similar to the 6V case, a 30V input also experienced various unexpected errors. Multiple analog signal pins were probed to determine possible malfunction causes. The following discussion addresses possible explanations of circuit faults.

Multiple measured signals behaved differently than expected from simulations. First, the system output provided no voltage or current. Accordingly, the FB pin receives no feedback because no voltage forms across the FB's voltage divider, as shown in Figure 17-3. Furthermore, LT3791-1's SHORT pin remains always active because FB receives less than 400 mV. Therefore, the system operates in DCM. Voltages at SW1 and SW2 remain at 0V due to no voltage build up across the inductor, as shown in Figure 17-11 and Figure 17-12. This problem results from switches Q1 through Q4 not switching and allowing current flow through the inductor. Damaged,

or poorly selected, MOSFETS or a non-ideal controlling CLKOUT signal may cause system abnormalities.

The first hypothesis assumes MOSFETs switching improperly. Q1's gate should experience a 33V peak-to-peak gate drive with a 92% duty cycle from TG1. TG1 superimposes 5V onto the voltage sensed at the inductor from SW1. Q1's gate, however, only received a 4.5V peak-to-peak with a 20% duty cycle as shown in Figure 17-7. Q2's gate drive, connected to BG1, delivered a 76% duty cycle instead of 27% and as shown in Figure 17-8. Q3's gate also experienced similar behavior, providing a 67% duty cycle instead of 28%. Q2 and Q3 gate voltage measures 4.5V while the simulation result expects 5V. Figure 17-8 and Figure 17-9 display proper gate drive voltages of Q2 and Q3. Q4's gate drive measures at a voltage and duty cycle dissimilar to simulation results. Figure 17-10 displays Q4's 5V peak-to-peak TG2 gate drive operating at a 30% duty cycle. Theoretically, TG2 should provide 41V peak to peak with 70% duty cycle.

The second hypothesis assumes a malfunctioning CKLOUT signal causes circuit malfunctioning. A simulated CLKOUT signal expects a 5V peak-to-peak output but measured CLKOUT provided a 2V peak-to-peak output shown in Figure 17-5. CLKOUT synchronizes the two boards to operate 180^{o} out of phase and directly influence internal buck and boost logic of the LT3791-1 controller. Therefore, a non-ideal CLKOUT signal could negatively impact the secondary board's MOSFET switching. CLKOUT controls logic which control TG1, TG2, BG1, and BG2, the four gate drive pins. However, CLKOUT of secondary board operated correctly with 5V peak to peak shown in Figure 17-6. CLKOUT cannot fully explain abnormal circuit behavior because a single LT3791-1 board does not regulate 36V.

Additional testing proved CLKOUT functions correctly at 5V peak-to-peak at 400 kHz when a single board is tested instead of two parallel boards. This test indicated a potential loading

effect between the primary CLKOUT and secondary's SYNC pins. Pin function description of LT3791-1 in datasheet states that Pin 34, SYNC, contains an internal 90 $k\Omega$ resistor terminated to ground. A loading effect insinuates that the primary's CLKOUT could only supply roughly 20uA. An internal 90 $k\Omega$ resistor loading CLKOUT is unlikely due because CLKOUT can supply more than 20uA. However, a loading theory describes the relation between master CLKOUT and slave SYNC most logically. Therefore, adding a buffer constructed using an op-amp inverter between primary and secondary boards could potentially increase the likelihood of proper operation.

Considering all other passive component selections could not cause system failure and all other passive components function as expected, another hypothesis proposes improper MOSFET operation as this problem's root cause. As described previously, improper MOSFET switching, or lack thereof, results in no inductor current and thus no functional or measureable converter output. Conducting the simulation shown in Figure 14-6 may provide an answer to improper MOSFET behavior.

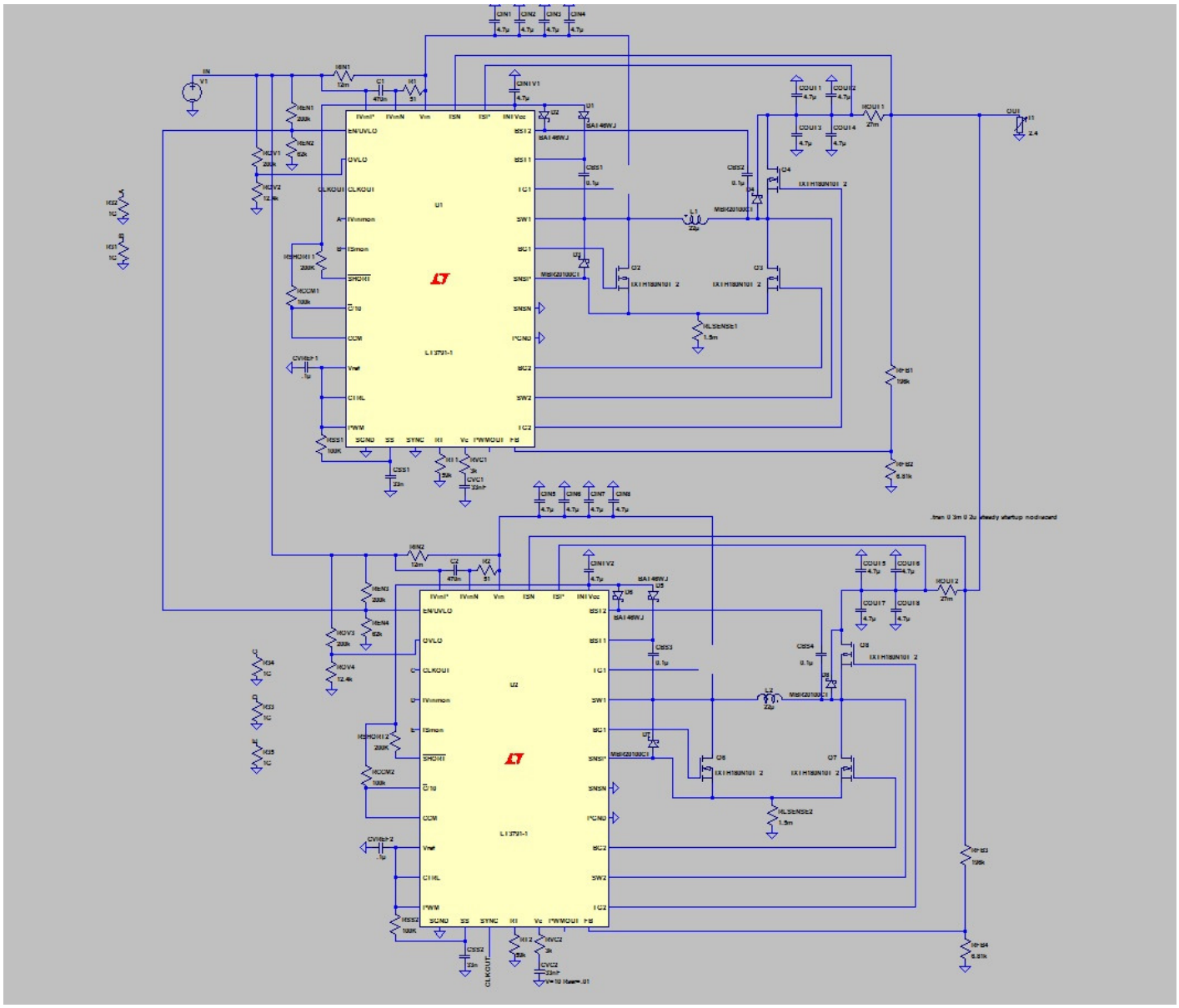

Figure 14-6: LTspice Simulation Confirming MOSFET Functionality, 30V, Q1 damaged

According to data obtained from testing, all MOSFET gates experienced 5V peak to peak with 400 kHz frequency. Also source of Q1, which supplies voltage to the inductor applies 0V at all times. If Q1 appears damaged as an open-circuit in the simulation and each node of MOSFETs provides the same result as the experiment, the simulation would confirm the hypothesis of MOSFET malfunction.

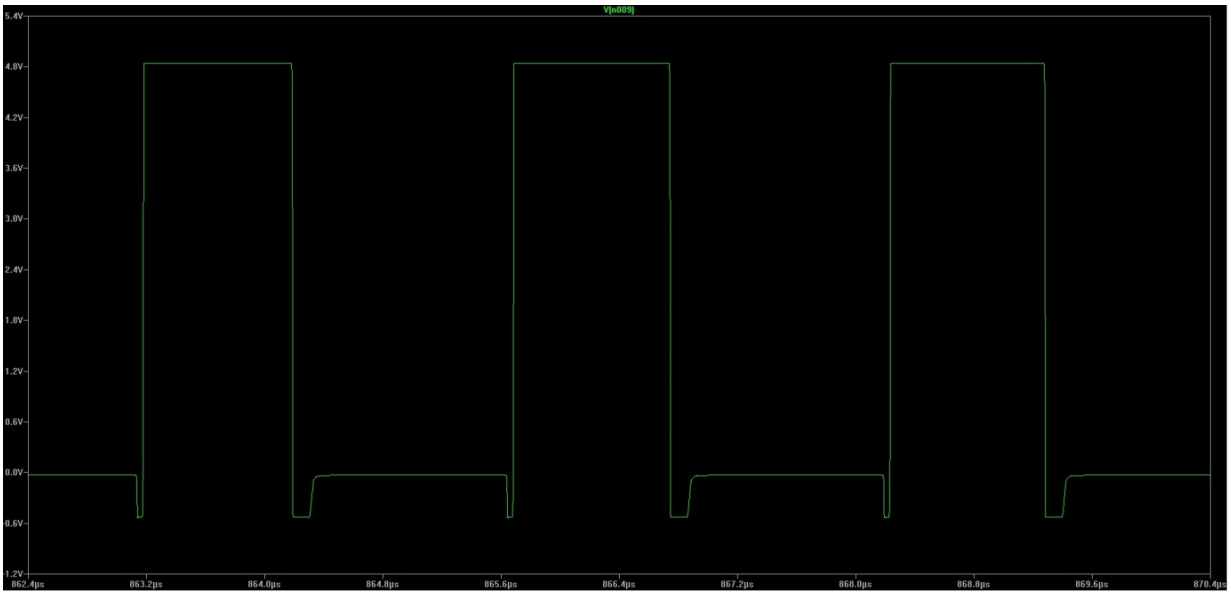

Figure 14-7: Q1 Gate Drive, TG1, Q1 damaged, $5V_{PP}$ 400 kHz

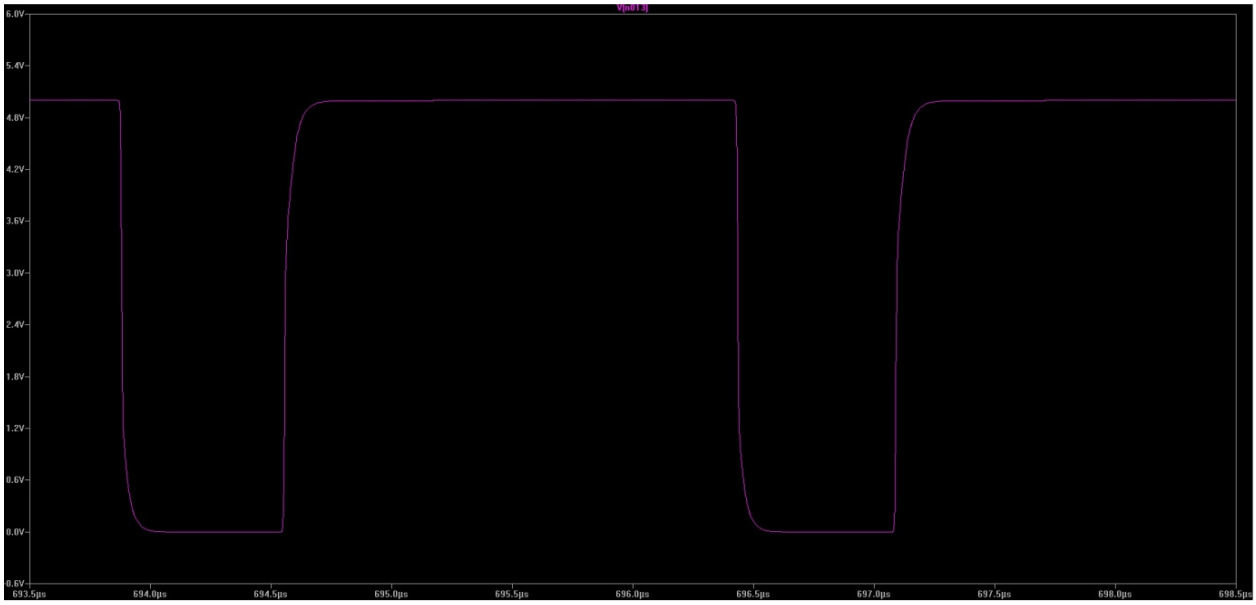

Figure 14-8: Q1 Gate Drive, TG2, Q1 damaged, $5V_{PP}$ 400 kHz

Comparing

Figure 14-7 and Figure 17-7 indicate both tested and simulated circuits experience the same TG1 voltage waveforms operating at 400 kHz. Comparing simulated versus measured TG2 waveforms from Figure 14-8 and Figure 17-10 indicate similarities between experimental and simulated results. Similarities between simulated and measured results strongly support the idea of

a damaged MOSFET. Characterizing MOSFET Q1 may help determine if Q1 was inadvertently damaged.

14.3. IXTH180N10T MOSFET Characterization

Q1was desoldered from a PCB and tested to confirm proper MOSFET operation. Prior testing hypothesized that damaged MOSFETs operated as an open-circuit, despite proper gate drive voltage. A damaged MOSFET represents a probable cause of malfunctioning converter behavior. Of four switches, Q1 maintains the highest damage probability because its drain connects directly to the power source through a current sense resistor. A damaged Q1 switch prohibits voltage forming across the inductor, and thus directly inhibits circuit operation. Therefore, Q1 was tested to confirm proper operation using a Keithley 2400 Source-Meter, an Agilent 33120A Function Generator, and an Agilent MSO-X 2012A Mixed Signal Oscilloscope.

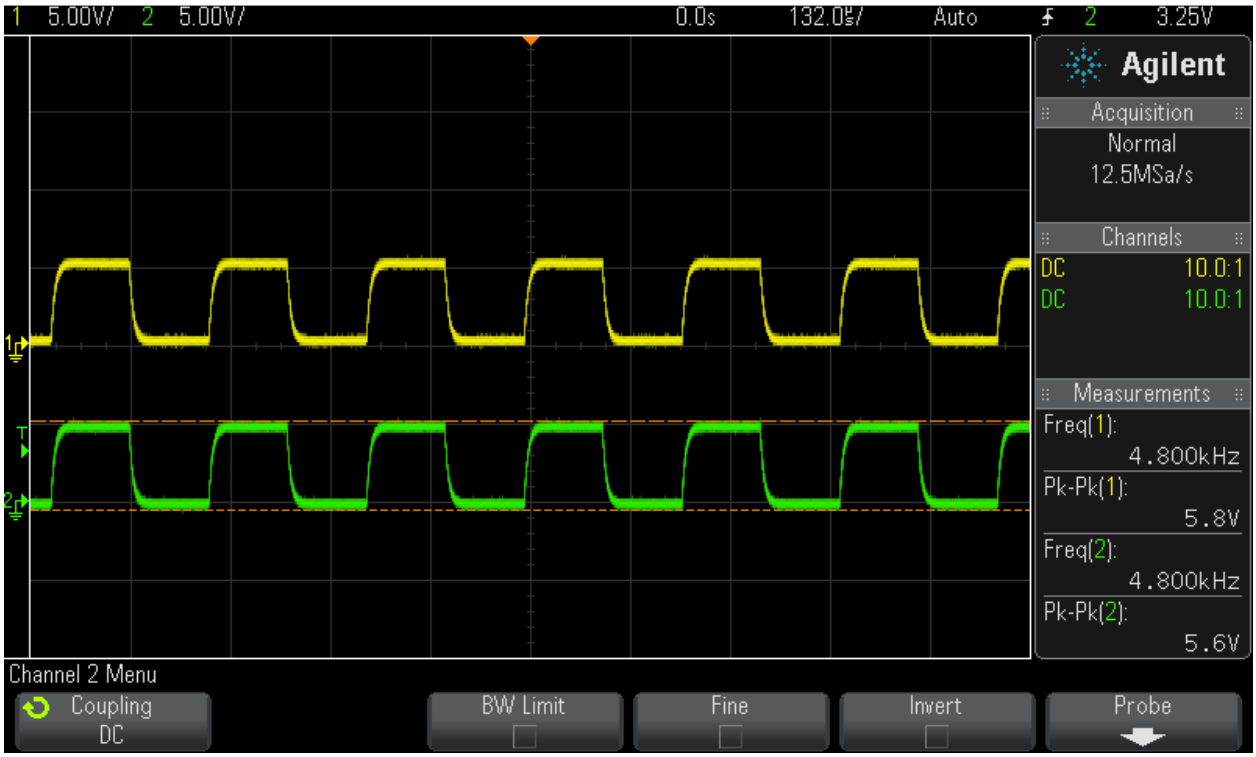

Figure 14-9: Q1 Gate Voltage vs. Source Voltage
Gate (Yellow) Source (Green)

Gate drive voltage verifies proper Q1 turns on and turn off operation. Oscilloscope probes observe Q1's drain and source voltages with Q1's source functioning as a common ground. The Agilent 33120A Function Generator applied a $5V_{pp}$, 4.8 kHz, 50% duty cycle square wave to Q1's gate while the Keithley 2400 Source-Meter supplied a 10V drain voltage. Figure 14-9's displays Q1 gate voltage and source voltage. Testing determined that Q1's gate and source appeared shorted together. Increasing or decreasing input V_{PP} of the gate directly increased observed source voltage. Figure 14-10 displays Q1 gate current (yellow trace) and drain voltage (green trace). Drain voltage does not decrease to 0V when Q1's drain is held at 5V. Testing Q2 using the same procedure observed similar results.

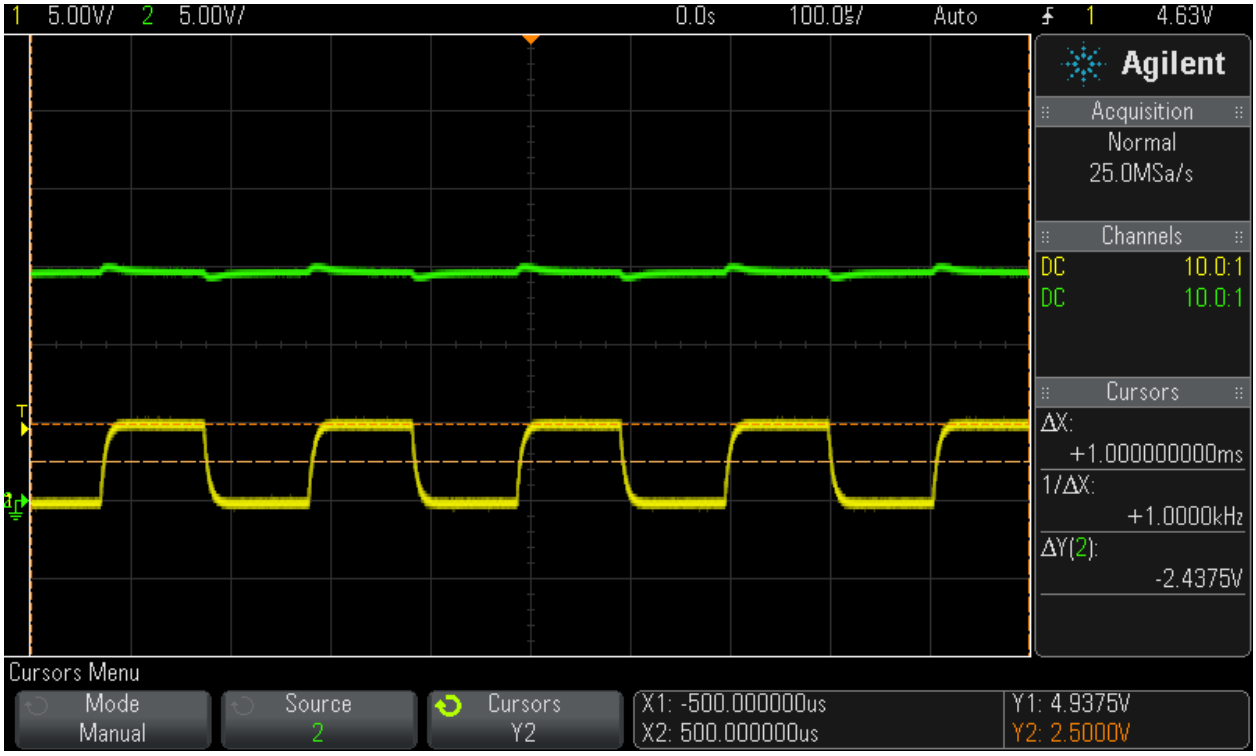

Figure 14-10: Q1 Gate Voltage vs. Drain Voltage
Q2 Gate (Yellow) Drain (Green)

Further drain current and drain-to-source resistance tested proper operation of Q1's MOSFET. Testing R_{DS} and I_D determines the threshold voltage of IXTH180N10T. Theoretically,

R_{DS} measures within a magnitude of a few MΩ when Q1 switches off and approximately 6.3mΩ when Q1switches on during proper MOSFET operation. Similarly, drain current should start to flow as V_{GS} approaches specified $V_{GS(TH)}$ but remains within a μA range until MOSFET turn on.

First, R_{DS} versus V_{GS} characteristics were tested. A Fluke Digital Multimeter measured drain-to-source resistance as the gate experienced a $5V_{pp}$, 4.8 kHz, 50% duty cycle square wave input. Q1's source functioned as a common ground. Gate voltage increased incrementally until sufficient data characterized a drain-to-source resistance versus V_{GS} curve with 0V drain voltage. Figure 14-11 plots measured R_{DS} versus V_{GS}. The MOSFET turns on when VGS nears 3.75V, a value within the 2.5 to 4.5V range specified by IXTH180N10T's datasheet. R_{DS} decreases from 6MΩ to 1kΩ during turn-on at a 0V drain voltage.

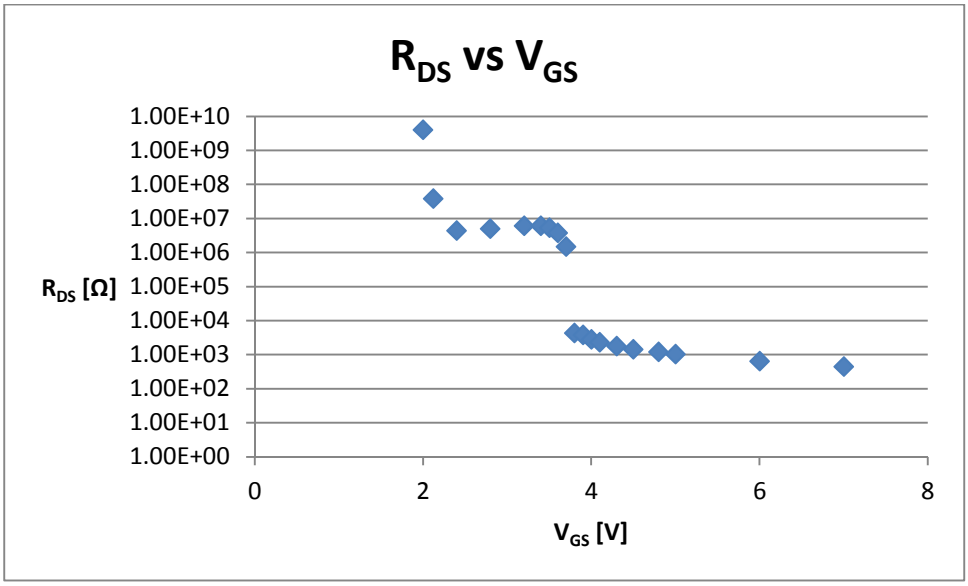

Figure 14-11: Drain-to-Source Resistance Characterization

I_D versus V_{GS} characteristics was also tested. Again, Q1's source functioned as a common ground. The Keithley Source-Meter set to 0.4V and a 1A current compliance at the drain. The function generator controlled Q1's gate with a 4.8 kHz, 50% duty cycle square wave of varying magnitude. Initially with V_{GS} below its threshold value, μA measured drain current indicated an

off-state MOSFET. Gate voltage increased until drain current begins flowing. Figure 14-12 and Figure 14-13 display I_D vs V_{GS} tested at 0.4V and 6V drain voltage. I_D vs. V_{GS} tests indicate I_D starts to flow when V_{GS} nears 4V. However, these characteristics may differ at higher drain voltages.

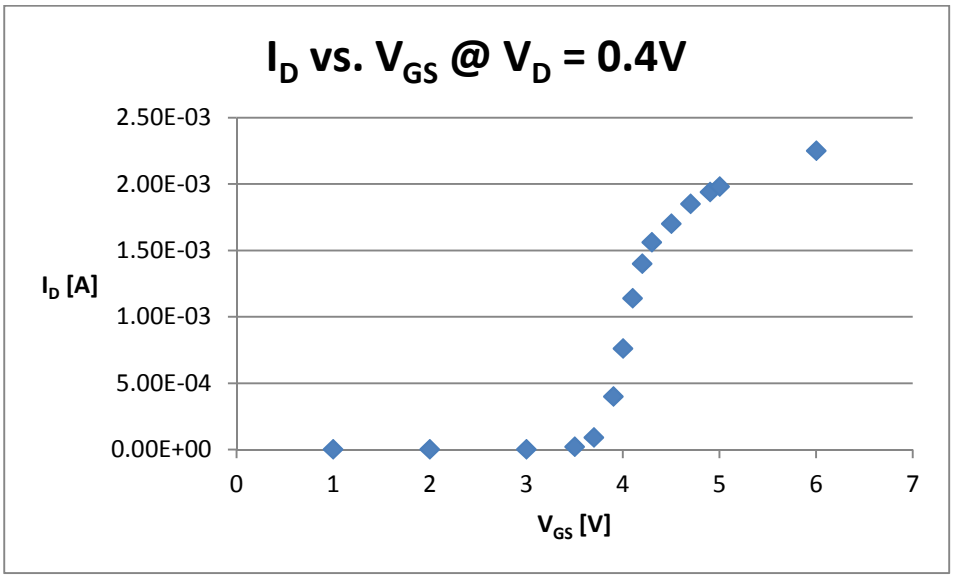

Figure 14-12: Drain Current Characterization, $V_D = 0V$

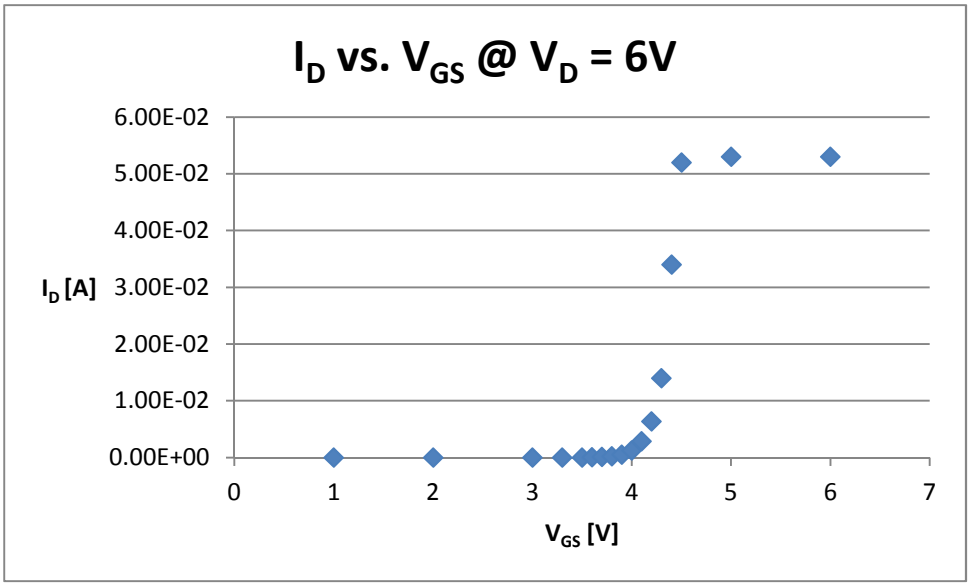

Figure 14-13: Drain Current Characterization, $V_D = 6V$

Chapter 15: Conclusion

The total cost for this project summed to $275.60 which is significantly cheaper than that of Martin Kou's $404.99 SEPIC topology. This cost reduction from results from the fewer components needed to build this project's design. Kou's SEPIC topology required 152 total components whereas this design required 117 components. This project, however, was significantly more expensive than that of Alvin Hilario who built working system under $80. An LT3791-1 topology may be a viable converter design with ample cost effectiveness if mass produced because a majority of the building cost consisted of PCB manufacturing.

Redesigning the PCB layout to fit components properly is highly recommended for future use. The current PCB design uses a smaller heat sink than the model currently selected. Larger air gaps between adjacent MOSFETs and heat sinks increase natural air circulation and cooling. Increasing board dimensions may also help to alleviate component crowding and increases surface area thereby allowing larger high-current carrying power traces.

Multiple operational errors occurred during this design including possible malfunction of MOSFETs and improper operation of CLKOUT. Characterization of MOSFETs before assembling the board would be recommended to avoid confusion in determining the cause of faulty components. An additional recommendation involves adding a buffer or inverter between the CLKOUT and SYNC of primary and secondary boards to decrease CLKOUT loading and increase the likelihood of proper operation.

Overall, this project determined that a Buck-Boost DC-DC Converter based on a parallel LT3791-1 4-Switch Buck-Boost Controller topology is a viable converter design. Simulations indicated efficient circuit operation between 6V and 50V input voltages, signifying 3.6W and 250W inputs, with simulated efficiencies ranging from 84.6% at 6V to 96.9% at 50V. Overall

system efficiency averages to 92.28%. Thus, this design theoretically operates slightly more efficiently than Martin Kou's 92.4% overall efficient SEPIC converter at maximum load although not as efficiently as Alvin Hilario's 95% overall efficient 4-Switch Buck Boost converter design.

Further project testing must occur to produce a fully functioning Paralleled LT3791-1 4-Switch Buck-Boost DC-DC Converter. Additional required testing should also verify converter compatibility with Cameron Kiddoo and Eric Funsten's input protection circuit and current limiter. Both the input protection and converter systems must function cohesively before attaching to the Precor EFX 546i Elliptical Trainer's generator and the Enphase M175 Micro-Inverter. Ensuring proper system functionality greatly increases the odds of a well-protected, highly efficient, exercise energy harvesting system.

Chapter 16: References

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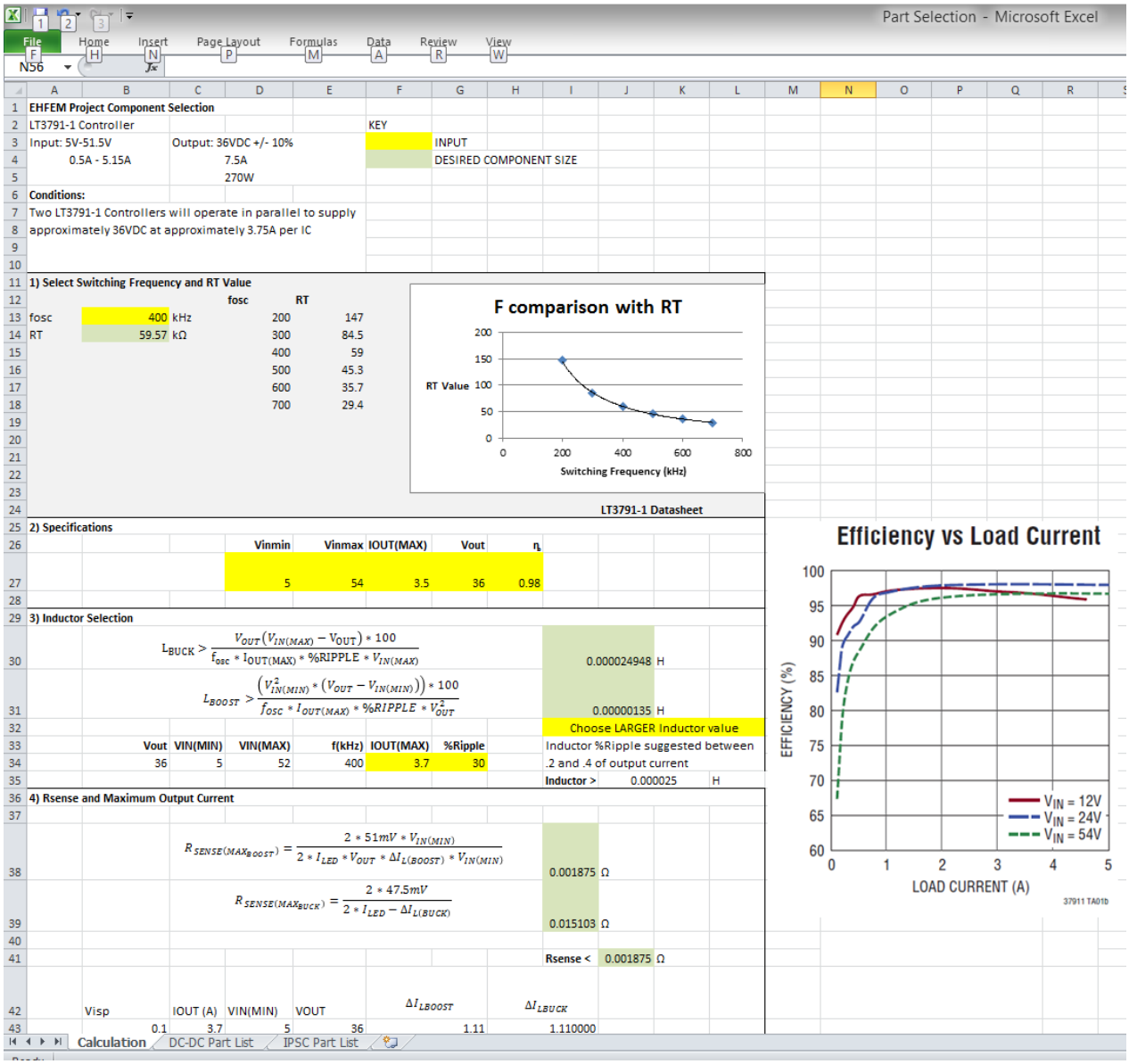
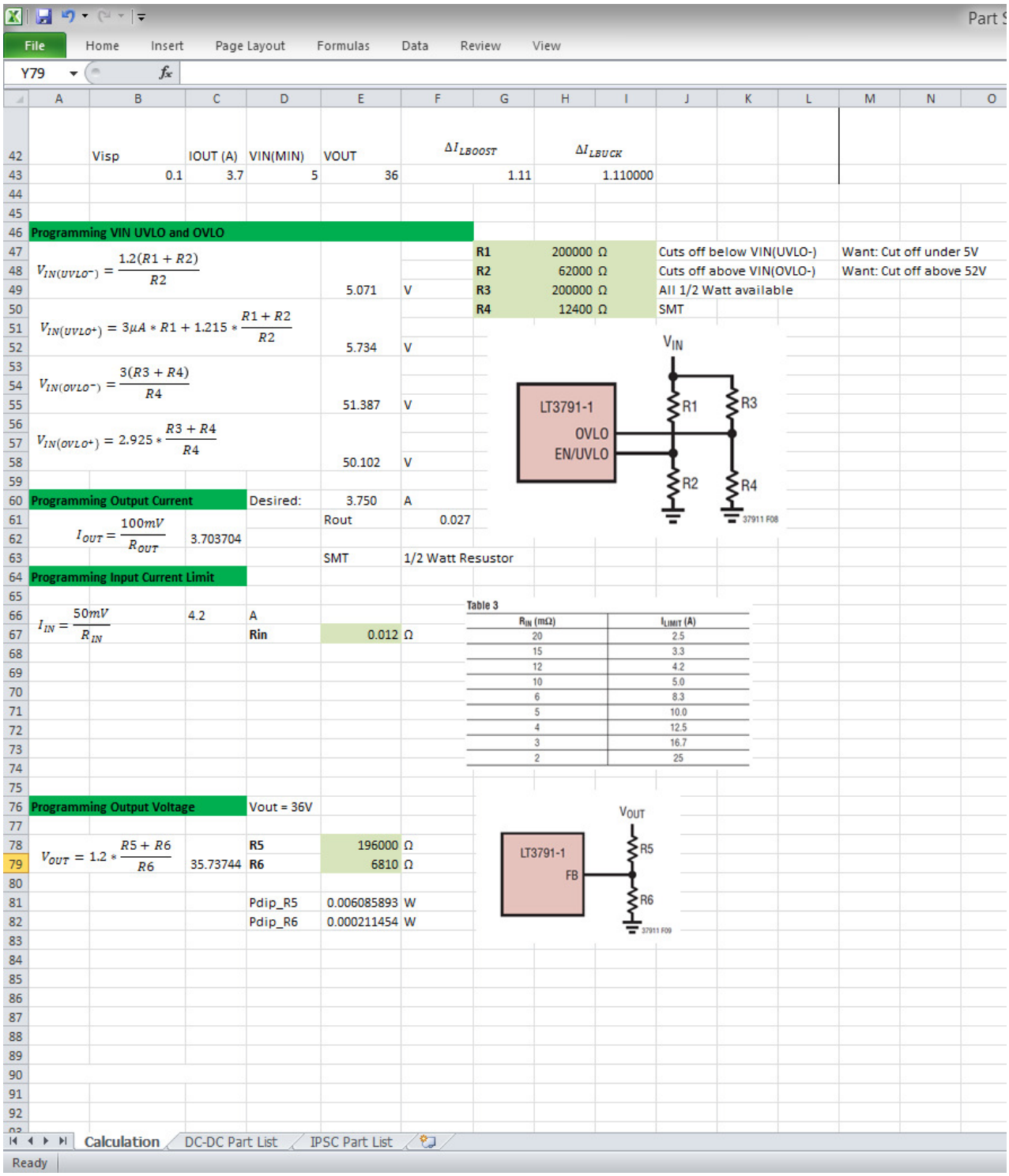
Chapter 17: Appendix

A. Excel Component Sizing Calculation Spreadsheet

A custom-made Microsoft Excel spreadsheet aided omponent selection for the LT3791-1 4-Switch Buck-Boost Controller. LT3791-1's datasheet included numerous equations converted into Excel formulas. Using an Excel spread sheet sped up calculations passive components such as resistor and inductor sizing without the need to hand-calculate component values.





42		Visp	IOUT (A)	VIN(MIN)	VOUT		ΔI_{LBOOST}		ΔI_{LBUCK}					
43		0.1	3.7	5	36		1.11		1.110000					
46	**Programming VIN UVLO and OVLO**													
47								**R1**	200000 Ω	Cuts off below VIN(UVLO-)			Want: Cut off under 5V	
48	$V_{IN(UVLO^-)} = \frac{1.2(R1+R2)}{R2}$							**R2**	62000 Ω	Cuts off above VIN(OVLO-)			Want: Cut off above 52V	
49					5.071	V		**R3**	200000 Ω	All 1/2 Watt available				
50								**R4**	12400 Ω	SMT				
51	$V_{IN(UVLO^+)} = 3\mu A * R1 + 1.215 * \frac{R1+R2}{R2}$													
52					5.734	V								
53														
54	$V_{IN(OVLO^-)} = \frac{3(R3+R4)}{R4}$													
55					51.387	V								
56														
57	$V_{IN(OVLO^+)} = 2.925 * \frac{R3+R4}{R4}$													
58					50.102	V								
59														
60	**Programming Output Current**			Desired:	3.750	A								
61					Rout		0.027							
62	$I_{OUT} = \frac{100mV}{R_{OUT}}$		3.703704											
63					SMT		1/2 Watt Resustor							
64	**Programming Input Current Limit**													
65														
66	$I_{IN} = \frac{50mV}{R_{IN}}$		4.2	A										
67				**Rin**	0.012	Ω								
68														
69														
70														
71														
72														
73														
74														
75														
76	**Programming Output Voltage**			Vout = 36V										
77														
78	$V_{OUT} = 1.2 * \frac{R5+R6}{R6}$			**R5**	196000	Ω								
79			35.73744	**R6**	6810	Ω								
80														
81				Pdip_R5	0.006085893	W								
82				Pdip_R6	0.000211454	W								

Table 3

R_{IN} (mΩ)	I_{LIMIT} (A)
20	2.5
15	3.3
12	4.2
10	5.0
6	8.3
5	10.0
4	12.5
3	16.7
2	25

B. Final Project Gantt Chart

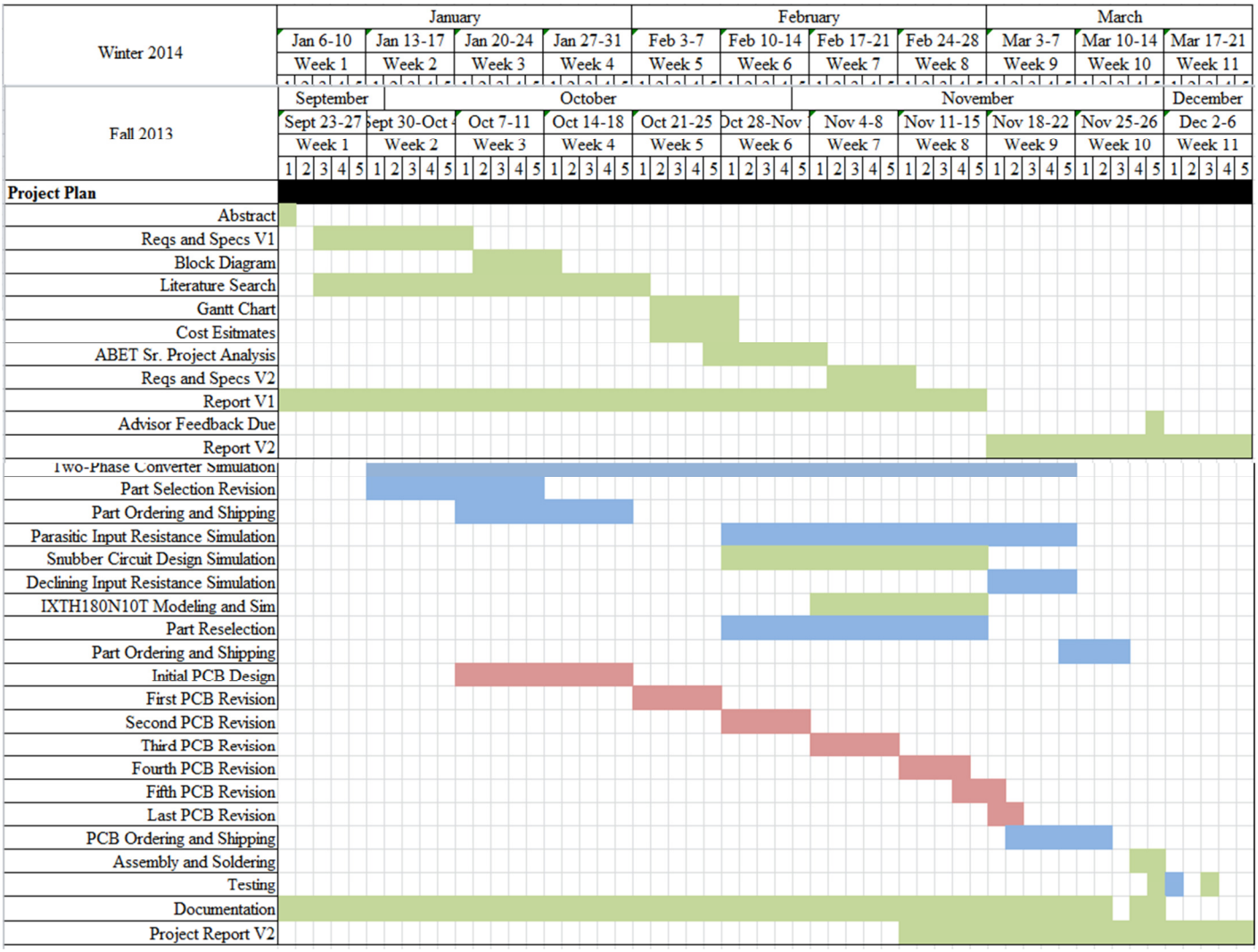


Figure 17-1: Final Project Gantt Chart

C. Final Bill of Materials

Type	Schematic Name	Value	Component	$/unit	QTY	Sum	P/N	Description	Company
Inductor	Inductor	22u	Inductor	$7.83	2	$15.66	AIRD-03-270K	INDUCTOR PWR DRUM CORE 27UH	Abracon
Resistors	RLSENSE	12m	R1	$1.17	2	$2.34	ERJ-8BWFR012V	RES 0.012 OHM 1W 1% 1206 SMD	Panasonic
	REN1	200k	R2	$0.10	2	$0.20	RC2012F204CS	RES 200K OHM 1/8W 1% 0805	Samsung
	REN2	62k	R3	$0.10	2	$0.20	ERJ-6ENF6202V	RES 62K OHM 1/8W 1% 0805 SMD	Panasonic
	Rcomp	51	R4	$0.10	2	$0.20	ERJ-6ENF51R0V	RES 51 OHM 1/8W 1% 0805 SMD	Panasonic
	ROVLO1	200k	R5	$0.10	2	$0.20	ERJ-6ENF2003V	RES 200K OHM 1/8W 1% 0805 SMD	Panasonic
	ROVLO2	12.4k	R6	$0.10	2	$0.20	ERJ-6ENF1242V	RES 12.4K OHM 1/8W 1% 0805 SMD	Panasonic
	RT	59k	R7	$0.10	2	$0.20	ERJ-6ENF5902V	RES 59K OHM 1/8W 1% 0805 SMD	Panasonic
	Rsense	1.5m	R8	$1.11	2	$2.22	ERJ-M1WTF1M5U	RES 0.0015 OHM 1W 1% 2512 SMD	Panasonic
	RFB1	196k	R9	$0.10	2	$0.20	ERJ-6ENF1963V	RES 196K OHM 1/8W 1% 0805 SMD	Panasonic
	RFB2	6.81k	R10	$0.10	2	$0.20	ERJ-6ENF6811V	RES 6.81K OHM 1/8W 1% 0805 SMD	Panasonic
	ROUT	27m	R11	$1.17	2	$2.34	ERJ-8BWFR027V	RES 0.027 OHM 1W 1% 1206 SMD	Panasonic
	RSHORT	200k	R12	$0.10	2	$0.20	ERJ-6ENF2003V	RES 200K OHM 1/8W 1% 0805 SMD	Panasonic
	RC/10	100k	R13	$0.10	2	$0.20	ERJ-6ENF1003V	RES 100K OHM 1/8W 1% 0805 SMD	Panasonic
	RSS	100k	R14	$0.10	2	$0.20	ERJ-6ENF1003V	RES 100K OHM 1/8W 1% 0805 SMD	Panasonic
	RVC	3k	R15	$0.10	2	$0.20	ERJ-6ENF3001V	RES 3K OHM 1/8W 1% 0805 SMD	Panasonic
Switches			Q1-Q8	$4.03	8	$32.20	IXTH180N10T	MOSFET N-CH 100V 180A TO-247	IXYS
Capacitors	CSS	33nF	C1	$0.24	2	$0.48	C0603C333K8RACTU	CAP CER 0.033UF 10V 10% X7R 0603	Kemet
	CVC	33nF	C2	$0.24	2	$0.48	C0603C333K8RACTU	CAP CER 0.033UF 10V 10% X7R 0603	Kemet
	Ccomp	470n	C3	$0.41	2	$0.82	C0603C474K8RACTU	CAP CER 0.47UF 10V 10% X7R 0603	Kemet
	CINTVCC	4.7u	C4	$1.40	2	$2.80	C3225X7S2A475M200AB	CAP CER 4.7UF 100V 20% X7S 1210	TDK
	CVREF	0.1uF	C5	$0.10	2	$0.20	C1608X7R1E104K080AA	CAP CER 0.1UF 25V 10% X7R 0603	TDK
	CBS	0.1uF	C6 and C7	$0.10	4	$0.40	C1608X7R1E104K080AA	CAP CER 0.1UF 25V 10% X7R 0603	TDK
	COUT	4.7u	COUT	$1.23	8	$9.84	C3225X7S2A475K200AB	CAP CER 4.7UF 100V 10% X7S 1210	TDK
	CIN	4.7u	CIN	$1.23	8	$9.84	C3225X7S2A475K200AB	CAP CER 4.7UF 100V 10% X7S 1210	TDK
Schottky	D1, D2		D1,D2,D5,D6	$0.44	4	$1.76	BAT46WJ,115	DIODE SCHOTKY 100V 0.25A SOD323F	NXP Semicond.

	D3, D4		D3,D4,D7,D8	$1.23	4	$4.92	MBR20100CTTU	DIODE SCHOTTKY 100V 10A TO220	Fairchild Semi
Controller	LT3791-1		Controller	$11.21	3	$33.63	LT3791IFE-1#PBF	IC REG CTRLR BUCK BST 38TSSOP	Linear Tech
Heat Sink				$3.09	8	$24.72	C247-025-1AE	HEATSINK FOR TO-247 WITH 1 CLIP	Ohmite
Header Pins				$0.13	18	$2.30	961102-6404-AR	CONN HEADER VERT SGL 2POS GOLD	3M
POSTS	RED			$4.05	4	$16.20	111-0702-001		Emerson
	BLACK			$4.05	6	$24.30	111-0703-001		Emerson
PCB	4-Layer		PCB	$32.67	2	$65.33			ExpressPCB
					TOTAL	**$255.19**			
					TAX	$275.60			

D. LTspice Netlist

Initial Design Netlist

```
* C:\Users\Sheldon\Desktop\Senior Project\Final DC DC Design\Power Trace Cases\LT3791-1_Parallel_50V.asc
C1 N050 0 33n V=10 Rser=.01
R1 IN N026 12m
R2 IN N005 200k tol=1
R3 N005 0 62k tol=1
R4 N028 N026 51 tol=1
C3 IN N028 470n
C4 N029 0 4.7µ V=100 Rser=.001
R5 IN N031 200k tol=1
R6 N031 0 12.4k tol=1
R7 N046 0 59k tol=1
C5 N045 0 .1µ V=25 Rser=.01
L2 N037 N038 27µ Rser=.012
C6 N032 N037 .47µ V=25 Rser=.01
D3 N029 N032 BAT46WJ
C7 N030 N038 .47µ V=25 Rser=.01
D4 N029 N030 BAT46WJ
R8 N043 0 1.5m tol=1
R9 OUT N049 196k tol=1
R10 N049 0 6.81k tol=1
R11 N027 OUT 27m tol=1
C8 N027 0 4.7µ V=50 Irms=0 Rser=0.1 Lser=0
XU2 N045 N050 N045 N044 N042 N045 N039 N036 N005 IN N028 N026 N029 N034 N032 N037 0 N040 N041
MP_01 N038 N030 MP_02 N035 N027 OUT N043 0 MP_03 0 N048 N044 N033 N009 N046 N047 N049 N031
LT3791-1
R12 N029 N042 200K tol=1
R14 N045 N050 100K tol=1
C11 N026 0 4.7µ x2 V=100 Rser=0.1
C14 N025 0 33n V=10 Rser=.01
C15 P001 0 33nF V=10 Rser=.01
R17 IN N001 12m tol=1
R18 IN N005 200k tol=1
R19 N005 0 62k tol=1
R20 N003 N001 51 tol=1
C16 IN N003 470n V=10 Rser=.01
C17 N004 0 4.7µ V=100 Rser=.01
R21 IN N007 200k tol=1
R22 N007 0 12.4k tol=1
R23 N021 0 59k tol=1
C18 N020 0 .1µ V=25 Rser=.01
M§Q1 N001 N010 N013 N013 IPI045N10N3
L1 N013 N014 27µ Rser=.012
C19 N008 N013 .47µ V=25 Rser=.01
D1 N004 N008 BAT46WJ
C20 N006 N014 .47µ V=25 Rser=.01
D2 N004 N006 BAT46WJ
R24 N018 0 1.5m tol=1
R25 OUT N024 196k
R26 N024 0 6.81k tol=1
R27 N002 OUT 27m tol=1
C21 N002 0 4.7µ V=50 Irms=0 Rser=0.1 Lser=0
```

```
XU1 N020 N025 N020 N019 N017 N020 NC_01 N012 N005 IN N003 N001 N004 N010 N008 N013 0 N015 N016
MP_04 N014 N006 MP_05 N011 N002 OUT N018 0 MP_06 0 N023 N019 N009 0 N021 N022 N024 N007
LT3791-1
R28 N004 N017 200K tol=1
R29 N020 N025 100K tol=1
C24 N001 0 4.7µ x2 V=100 Rser=.1
V1 IN 0 PWL(0 0 0.5m 50) Rser=.2
R13 N022 P001 3k tol=1
C2 N051 0 33nF V=10 Rser=.01
R15 N047 N051 3k tol=1
I§LOAD OUT 0 6.94
R16 N004 N019 100k
R30 N029 N044 100k
M§Q2 N013 N015 N018 N018 IPI045N10N3
M§Q3 N014 N016 N018 N018 IPI045N10N3
M§Q4 N002 N011 N014 N014 IPI045N10N3
M§Q5 N026 N034 N037 N037 IPI045N10N3
M§Q6 N037 N040 N043 N043 IPI045N10N3
M§Q7 N038 N041 N043 N043 IPI045N10N3
M§Q8 N027 N035 N038 N038 IPI045N10N3
C22 N001 0 4.7µ x2 V=100 Rser=.1
C23 N001 0 4.7µ x2 V=100 Rser=.1
C25 N001 0 4.7µ x2 V=100 Rser=.1
C26 N026 0 4.7µ x2 V=100 Rser=0.1
C27 N026 0 4.7µ x2 V=100 Rser=0.1
C28 N026 0 4.7µ x2 V=100 Rser=0.1
C9 N002 0 4.7µ V=50 Irms=0 Rser=0.1 Lser=0
C10 N002 0 4.7µ V=50 Irms=0 Rser=0.1 Lser=0
C12 N002 0 4.7µ V=50 Irms=0 Rser=0.1 Lser=0
C13 N027 0 4.7µ V=50 Irms=0 Rser=0.1 Lser=0
C29 N027 0 4.7µ V=50 Irms=0 Rser=0.1 Lser=0
C30 N027 0 4.7µ V=50 Irms=0 Rser=0.1 Lser=0
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.mos
.tran 0 3m 0 2u steady startup nodiscard
.lib LT3791-1.sub
.backanno
.end
```

Final Design Netlist

```
* C:\Users\Sheldon\Desktop\Senior Project\LTSpice\IXTH180N10T_50V_22uH.asc
CSS2 N045 0 33n V=10 Rser=.01
RIN2 IN N024 12m
REN3 IN N005 200k tol=1
REN4 N005 0 62k tol=1
R2 N026 N024 51 tol=1
C2 IN N026 470n V=10 Rser=0.01
CINTV2 N027 0 4.7µ V=100 Rser=.001
ROV3 IN N029 200k tol=1
ROV4 N029 0 12.4k tol=1
RT2 N041 0 59k tol=1
CVREF2 N040 0 .1µ V=25 Rser=.01
L2 N033 N034 22µ Ipk=15 Rser=0.007
CBS3 N030 N033 0.1µ V=25 Rser=.01
D5 N027 N030 BAT46WJ
CBS4 N028 N034 0.1µ V=25 Rser=.01
D6 N027 N028 BAT46WJ
RLSENSE2 N037 0 1.5m tol=1
RFB3 OUT N044 196k tol=1
RFB4 N044 0 6.81k tol=1
ROUT2 N025 OUT 27m tol=1
XU2 N040 N045 N040 N039 N036 N040 E D N005 IN N026 N024 N027 N032 N030 N033 0 N035 N038 MP_01
N034 N028 MP_02 N031 N025 OUT N037 0 MP_03 0 N043 N039 C CLKOUT N041 N042 N044 N029 LT3791-1
RSHORT2 N027 N036 200K tol=1
RSS2 N040 N045 100K tol=1
CSS1 N023 0 33n V=10 Rser=.01
CVC1 P001 0 33nF V=10 Rser=.01
RIN1 IN N001 12m tol=1
REN1 IN N005 200k tol=1
REN2 N005 0 62k tol=1
R1 N003 N001 51 tol=1
C1 IN N003 470n V=10 Rser=.01
CINTV1 N004 0 4.7µ V=100 Rser=.01
ROV1 IN N007 200k tol=1
ROV2 N007 0 12.4k tol=1
RT1 N019 0 59k tol=1
CVREF1 N018 0 .1µ V=25 Rser=.01
M§Q1 N001 N009 N011 N011 IXTH180N10T_2
L1 N012 N011 22µ Ipk=15 Rser=0.007
CBS1 N008 N011 0.1µ V=25 Rser=.01
D1 N004 N008 BAT46WJ
CBS2 N006 N012 0.1µ V=25 Rser=.01
D2 N004 N006 BAT46WJ
RLSENSE1 N015 0 1.5m tol=1
RFB1 OUT N022 196k
RFB2 N022 0 6.81k tol=1
ROUT1 N002 OUT 27m tol=1
COUT4 N002 0 4.7µ V=50 Irms=0 Rser=0.1 Lser=0
XU1 N018 N023 N018 N017 N014 N018 B A N005 IN N003 N001 N004 N009 N008 N011 0 N013 N016 MP_04
N012 N006 MP_05 N010 N002 OUT N015 0 MP_06 0 N021 N017 CLKOUT 0 N019 N020 N022 N007 LT3791-1
RSHORT1 N004 N014 200K tol=1
RSS1 N018 N023 100K tol=1
V1 IN 0 PWL(0 0 1m 50) Rser=1
RVC1 N020 P001 3k tol=1
CVC2 N046 0 33nF V=10 Rser=.01
```

```
RVC2 N042 N046 3k tol=1
RCCM1 N004 N017 100k
RCCM2 N027 N039 100k
M§Q2 N011 N013 N015 N015 IXTH180N10T_2
M§Q3 N012 N016 N015 N015 IXTH180N10T_2
M§Q4 N002 N010 N012 N012 IXTH180N10T_2
M§Q5 N024 N032 N033 N033 IXTH180N10T_2
M§Q6 N033 N035 N037 N037 IXTH180N10T_2
M§Q7 N034 N038 N037 N037 IXTH180N10T_2
M§Q8 N025 N031 N034 N034 IXTH180N10T_2
COUT3 N002 0 4.7µ V=50 Irms=0 Rser=0.1 Lser=0
COUT1 N002 0 4.7µ V=50 Irms=0 Rser=0.1 Lser=0
D3 N015 N011 MBR20100CT
D7 N037 N033 MBR20100CT
D8 N034 N025 MBR20100CT
D4 N012 N002 MBR20100CT
R31 B 0 1G
R32 A 0 1G
R33 D 0 1G
R34 C 0 1G
R35 E 0 1G
I1 OUT 0 6.6 load
CIN3 N001 0 4.7µ V=100 Rser=0.1
CIN4 N001 0 4.7µ V=100 Rser=0.1
CIN7 N024 0 4.7µ V=100 Rser=0.1
CIN8 N024 0 4.7µ V=100 Rser=0.1
CIN1 N001 0 4.7µ V=100 Rser=0.1
CIN2 N001 0 4.7µ V=100 Rser=0.1
COUT2 N002 0 4.7µ V=50 Irms=0 Rser=0.1 Lser=0
CIN5 N024 0 4.7µ V=100 Rser=0.1
CIN6 N024 0 4.7µ V=100 Rser=0.1
COUT8 N025 0 4.7µ V=50 Irms=0 Rser=0.1 Lser=0
COUT7 N025 0 4.7µ V=50 Irms=0 Rser=0.1 Lser=0
COUT5 N025 0 4.7µ V=50 Irms=0 Rser=0.1 Lser=0
COUT6 N025 0 4.7µ V=50 Irms=0 Rser=0.1 Lser=0
.model D D
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.dio
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Program Files (x86)\LTC\LTspiceIV\lib\cmp\standard.mos
.tran 0 3m 0 2u steady startup nodiscard
.lib LT3791-1.sub
.backanno
.end
```

E. Initial Design Results

Based on (Figure 9-1) and Initial Design Netlist (Section D)

Table 17-1: Power dissipation and efficiency, $V_{IN} = 6V$

Efficiency: 83.0%
Input: 4.31W @ 6V
Output: 3.57W @ 35.7V

Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	0mA	0mA	0mW
C3	0mA	0mA	0mW
C4	37mA	627mA	0mW
C5	0mA	0mA	0mW
C6	0mA	0mA	0mW
C7	3mA	198mA	0mW
C8	270mA	10284mA	0mW
C11	13mA	33mA	0mW
C14	0mA	0mA	0mW
C15	0mA	0mA	0mW
C16	0mA	0mA	0mW
C17	37mA	628mA	0mW
C18	0mA	0mA	0mW
C19	0mA	0mA	0mW
C20	3mA	198mA	0mW
C21	267mA	10212mA	0mW
C24	13mA	35mA	0mW
D1	0mA	0mA	0mW
D2	3mA	198mA	0mW
D3	0mA	0mA	0mW
D4	3mA	198mA	0mW
L1	379mA	610mA	2mW
L2	381mA	602mA	2mW
Q1	379mA	610mA	4mW
Q2	0mA	26mA	-0mW
Q3	423mA	10695mA	276mW
Q4	278mA	10542mA	36mW
Q5	381mA	602mA	4mW
Q6	0mA	24mA	0mW
Q7	425mA	10423mA	277mW
Q8	279mA	10277mA	37mW

Ref.	Irms	Ipeak	Dissipation
R1	383mA	598mA	880µW
R2	0mA	0mA	105µW
R3	0mA	0mA	32µW
R4	0mA	0mA	0µW
R5	0mA	0mA	160µW
R6	0mA	0mA	10µW
R7	0mA	0mA	17µW
R8	434mA	10898mA	282µW
R9	0mA	0mA	6mW
R10	0mA	0mA	212µW
R11	52mA	432mA	72µW
R12	0mA	0mA	0µW
R13	0mA	0mA	0µW
R14	0mA	0mA	0µW
R15	0mA	0mA	0µW
R16	0mA	0mA	245µW
R17	381mA	607mA	872µW
R18	0mA	0mA	105µW
R19	0mA	0mA	32µW
R20	0mA	0mA	0µW
R21	0mA	0mA	160µW
R22	0mA	0mA	10µW
R23	0mA	0mA	17µW
R24	431mA	11168mA	279µW
R25	0mA	0mA	6mW
R26	0mA	0mA	212µW
R27	51mA	377mA	71µW
R28	0mA	0mA	0µW
R29	0mA	0mA	0µW
R30	0mA	0mA	245µW
U1	54mA	788mA	40mW
U2	54mA	789mA	40mW

Table 17-2: Power dissipation and efficiency, $V_{IN} = 10V$

Efficiency: 90.9%			
Input: 10.9W @ 10V			
Output: 9.94W @ 35.7V			
Ref.	**Irms**	**Ipeak**	**Dissipation**
C1	0mA	0mA	0mW
C2	0mA	0mA	0mW
C3	0mA	0mA	0mW
C4	36mA	628mA	0mW
C5	0mA	0mA	0mW
C6	0mA	0mA	0mW
C7	4mA	207mA	0mW
C8	371mA	13020mA	0mW
C11	31mA	57mA	0mW
C14	0mA	0mA	0mW
C15	0mA	0mA	0mW
C16	0mA	0mA	0mW
C17	36mA	628mA	0mW
C18	0mA	0mA	0mW
C19	0mA	0mA	0mW
C20	4mA	207mA	0mW
C21	365mA	12852mA	0mW
C24	32mA	57mA	0mW
D1	0mA	0mA	0mW
D2	4mA	207mA	0mW
D3	0mA	0mA	0mW
D4	4mA	207mA	0mW
L1	576mA	902mA	4mW
L2	578mA	896mA	4mW
Q1	576mA	902mA	8mW
Q2	0mA	37mA	-0mW
Q3	562mA	13427mA	314mW
Q4	398mA	13191mA	102mW
Q5	578mA	896mA	8mW
Q6	0mA	34mA	-0mW
Q7	564mA	13211mA	315mW
Q8	399mA	12983mA	102mW

Ref.	**Irms**	**Ipeak**	**Dissipation**
R1	580mA	880mA	4mW
R2	0mA	0mA	291µW
R3	0mA	0mA	90µW
R4	0mA	0mA	0µW
R5	0mA	0mA	443µW
R6	0mA	0mA	27µW
R7	0mA	0mA	17µW
R8	571mA	13667mA	488µW
R9	0mA	0mA	6mW
R10	0mA	0mA	212µW
R11	140mA	619mA	530µW
R12	0mA	0mA	0µW
R13	0mA	0mA	0µW
R14	0mA	0mA	0µW
R15	0mA	0mA	0µW
R16	0mA	0mA	245µW
R17	578mA	889mA	4mW
R18	0mA	0mA	291µW
R19	0mA	0mA	90µW
R20	0mA	0mA	0µW
R21	0mA	0mA	443µW
R22	0mA	0mA	27µW
R23	0mA	0mA	17µW
R24	568mA	13883mA	484µW
R25	0mA	0mA	6mW
R26	0mA	0mA	212µW
R27	139mA	555mA	525µW
R28	0mA	0mA	0µW
R29	0mA	0mA	0µW
R30	0mA	0mA	245µW
U1	55mA	791mA	57mW
U2	55mA	791mA	57mW

Table 17-3: Power dissipation and efficiency, $V_{IN} = 15V$

Efficiency: 93.8%
Input: 23.8W @ 15V
Output: 22.3W @ 35.7V

Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	0mA	0mA	0mW
C3	0mA	0mA	0mW
C4	36mA	635mA	0mW
C5	0mA	0mA	0mW
C6	0mA	0mA	0mW
C7	4mA	225mA	0mW
C8	533mA	17987mA	1mW
C11	1mA	10mA	0mW
C14	0mA	0mA	0mW
C15	0mA	0mA	0mW
C16	0mA	0mA	0mW
C17	36mA	635mA	0mW
C18	0mA	0mA	0mW
C19	0mA	0mA	0mW
C20	4mA	226mA	0mW
C21	525mA	17706mA	1mW
C24	2mA	13mA	0mW
D1	0mA	0mA	0mW
D2	4mA	226mA	0mW
D3	0mA	0mA	0mW
D4	4mA	225mA	0mW
L1	823mA	1226mA	8mW
L2	827mA	1217mA	8mW
Q1	823mA	1226mA	17mW
Q2	0mA	59mA	-0mW
Q3	719mA	18207mA	393mW
Q4	618mA	17804mA	232mW
Q5	827mA	1217mA	17mW
Q6	0mA	60mA	0mW
Q7	723mA	18139mA	395mW
Q8	622mA	17739mA	233mW

Ref.	Irms	Ipeak	Dissipation
R1	5mA	13mA	0µW
R2	0mA	0mA	656µW
R3	0mA	0mA	203µW
R4	0mA	0mA	0µW
R5	0mA	0mA	1mW
R6	0mA	0mA	60µW
R7	0mA	0mA	17µW
R8	728mA	18564mA	795µW
R9	0mA	0mA	6mW
R10	0mA	0mA	212µW
R11	314mA	990mA	3mW
R12	0mA	0mA	0µW
R13	0mA	0mA	0µW
R14	0mA	0mA	0µW
R15	0mA	0mA	0µW
R16	0mA	0mA	245µW
R17	5mA	14mA	0µW
R18	0mA	0mA	656µW
R19	0mA	0mA	203µW
R20	0mA	0mA	0µW
R21	0mA	0mA	1mW
R22	0mA	0mA	60µW
R23	0mA	0mA	17µW
R24	724mA	18633mA	787µW
R25	0mA	0mA	6mW
R26	0mA	0mA	212µW
R27	312mA	912mA	3mW
R28	0mA	0mA	0µW
R29	0mA	0mA	0µW
R30	0mA	0mA	245µW
U1	55mA	803mA	79mW
U2	55mA	803mA	79mW

Table 17-4: Power dissipation and efficiency, $V_{IN} = 20V$

Efficiency: 96.5%

Input: 40.8W @ 20V
Output: 39.3W @ 35.7V

Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	0mA	0mA	0mW
C3	0mA	0mA	0mW
C4	37mA	647mA	0mW
C5	0mA	0mA	0mW
C6	0mA	0mA	0mW
C7	35mA	648mA	0mW
C8	658mA	21021mA	1mW
C11	35mA	56mA	0mW
C14	0mA	0mA	0mW
C15	0mA	0mA	0mW
C16	0mA	0mA	0mW
C17	37mA	647mA	0mW
C18	0mA	0mA	0mW
C19	0mA	0mA	0mW
C20	35mA	648mA	0mW
C21	648mA	20775mA	1mW
C24	35mA	65mA	0mW
D1	0mA	0mA	0mW
D2	7mA	244mA	1mW
D3	0mA	0mA	0mW
D4	7mA	244mA	1mW
L1	1036mA	1441mA	13mW
L2	1043mA	1443mA	13mW
Q1	1036mA	1441mA	26mW
Q2	0mA	70mA	-0mW
Q3	797mA	21134mA	450mW
Q4	855mA	20513mA	39mW
Q5	1043mA	1443mA	27mW
Q6	0mA	69mA	-0mW
Q7	802mA	21212mA	453mW
Q8	861mA	20587mA	40mW

Ref.	Irms	Ipeak	Dissipation
R1	1048mA	1421mA	13mW
R2	0mA	0mA	1mW
R3	0mA	0mA	361µW
R4	0mA	0mA	0µW
R5	0mA	0mA	2mW
R6	0mA	0mA	110µW
R7	0mA	0mA	17µW
R8	808mA	21619mA	978µW
R9	0mA	0mA	6mW
R10	0mA	0mA	212µW
R11	553mA	1315mA	8mW
R12	0mA	0mA	0µW
R13	0mA	0mA	0µW
R14	0mA	0mA	0µW
R15	0mA	0mA	0µW
R16	0mA	0mA	0µW
R17	1042mA	1423mA	13mW
R18	0mA	0mA	1mW
R19	0mA	0mA	361µW
R20	0mA	0mA	0µW
R21	0mA	0mA	2mW
R22	0mA	0mA	110µW
R23	0mA	0mA	17µW
R24	802mA	21541mA	965µW
R25	0mA	0mA	6mW
R26	0mA	0mA	212µW
R27	549mA	1223mA	8mW
R28	0mA	0mA	0µW
R29	0mA	0mA	0µW
R30	0mA	0mA	0µW
U1	55mA	817mA	153mW
U2	55mA	817mA	153mW

Table 17-5: Power dissipation and efficiency, $V_{IN} = 25V$

Efficiency: 97.1%
Input: 63.7W @ 25V
Output: 61.8W @ 35.7V

Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	0mA	0mA	0mW
C3	0mA	0mA	0mW
C4	37mA	651mA	0mW
C5	0mA	0mA	0mW
C6	0mA	0mA	0mW
C7	34mA	637mA	0mW
C8	780mA	27308mA	1mW
C11	32mA	56mA	0mW
C14	0mA	0mA	0mW
C15	0mA	0mA	0mW
C16	0mA	0mA	0mW
C17	37mA	652mA	0mW
C18	0mA	0mA	0mW
C19	0mA	0mA	0mW
C20	34mA	636mA	0mW
C21	768mA	27218mA	1mW
C24	33mA	88mA	0mW
D1	0mA	0mA	0mW
D2	7mA	268mA	1mW
D3	0mA	0mA	0mW
D4	7mA	268mA	1mW
L1	1280mA	1672mA	20mW
L2	1288mA	1676mA	20mW
Q1	1280mA	1673mA	40mW
Q2	0mA	105mA	-0mW
Q3	868mA	27501mA	570mW
Q4	1163mA	26528mA	60mW
Q5	1288mA	1676mA	41mW
Q6	0mA	99mA	0mW
Q7	873mA	27412mA	573mW
Q8	1170mA	26446mA	61mW

Ref.	Irms	Ipeak	Dissipation
R1	1294mA	1655mA	20mW
R2	0mA	0mA	2mW
R3	0mA	0mA	564µW
R4	0mA	0mA	0µW
R5	0mA	0mA	3mW
R6	0mA	0mA	172µW
R7	0mA	0mA	17µW
R8	879mA	27782mA	1mW
R9	0mA	0mA	6mW
R10	0mA	0mA	212µW
R11	868mA	1859mA	20mW
R12	0mA	0mA	0µW
R13	0mA	0mA	0µW
R14	0mA	0mA	0µW
R15	0mA	0mA	0µW
R16	0mA	0mA	0µW
R17	1286mA	1655mA	20mW
R18	0mA	0mA	2mW
R19	0mA	0mA	564µW
R20	0mA	0mA	0µW
R21	0mA	0mA	3mW
R22	0mA	0mA	172µW
R23	0mA	0mA	17µW
R24	874mA	27872mA	1mW
R25	0mA	0mA	6mW
R26	0mA	0mA	212µW
R27	863mA	1738mA	20mW
R28	0mA	0mA	0µW
R29	0mA	0mA	0µW
R30	0mA	0mA	0µW
U1	55mA	836mA	187mW
U2	55mA	837mA	186mW

Table 17-6: Power dissipation and efficiency, $V_{IN} = 30V$

Efficiency: 95.1%			
Input: 94W @ 30V			
Output: 89.4W @ 35.7V			
Ref.	**Irms**	**Ipeak**	**Dissipation**

Ref.	Irms	Ipeak	Dissipation

C1	0mA	0mA	0mW
C2	0mA	0mA	0mW
C3	0mA	3mA	0mW
C4	55mA	1058mA	0mW
C5	0mA	0mA	0mW
C6	39mA	1339mA	0mW
C7	33mA	615mA	0mW
C8	1546mA	51367mA	5mW
C11	968mA	45318mA	4mW
C14	0mA	0mA	0mW
C15	0mA	0mA	0mW
C16	0mA	0mA	0mW
C17	36mA	652mA	0mW
C18	0mA	0mA	0mW
C19	1mA	37mA	0mW
C20	25mA	586mA	0mW
C21	542mA	7970mA	1mW
C24	2mA	14mA	0mW
D1	1mA	37mA	0mW
D2	5mA	193mA	0mW
D3	18mA	1024mA	2mW
D4	8mA	381mA	1mW
L1	78mA	187mA	0mW
L2	3384mA	4034mA	137mW
Q1	0mA	0mA	0mW
Q2	72mA	186mA	15mW
Q3	157mA	8013mA	67mW
Q4	147mA	7725mA	78mW
Q5	3452mA	61885mA	1471mW
Q6	1490mA	58246mA	118mW
Q7	2026mA	53766mA	1474mW
Q8	3105mA	50420mA	326mW

R1	3229mA	16597mA	125mW
R2	0mA	0mA	3mW
R3	0mA	0mA	812µW
R4	0mA	3mA	2µW
R5	0mA	0mA	4mW
R6	0mA	0mA	247µW
R7	0mA	0mA	17µW
R8	2518mA	58161mA	10mW
R9	0mA	0mA	6mW
R10	0mA	0mA	212µW
R11	2560mA	3074mA	177mW
R12	0mA	0mA	0µW
R13	0mA	0mA	0µW
R14	0mA	0mA	0µW
R15	0mA	0mA	0µW
R16	0mA	0mA	205µW
R17	7mA	18mA	1µW
R18	0mA	0mA	3mW
R19	0mA	0mA	812µW
R20	0mA	0mA	0µW
R21	0mA	0mA	4mW
R22	0mA	0mA	247µW
R23	0mA	0mA	17µW
R24	162mA	8459mA	39µW
R25	0mA	0mA	6mW
R26	0mA	0mA	212µW
R27	524mA	1643mA	7mW
R28	0mA	0mA	0µW
R29	0mA	0mA	1µW
R30	0mA	0mA	0µW
U1	53mA	788mA	181mW
U2	58mA	976mA	420mW

Table 17-7: Power dissipation and efficiency, $V_{IN} = 36V$

Efficiency: 95.4%
Input: 135W @ 36V
Output: 129W @ 35.8V

Ref.	**Irms**	**Ipeak**	**Dissipation**
C1	0mA	0mA	0mW
C2	0mA	0mA	0mW

Ref.	**Irms**	**Ipeak**	**Dissipation**
R1	1974mA	13657mA	47mW
R2	0mA	0mA	4mW

C3	0mA	3mA	0mW
C4	57mA	944mA	0mW
C5	0mA	0mA	0mW
C6	39mA	1277mA	0mW
C7	32mA	714mA	0mW
C8	1064mA	47973mA	2mW
C11	642mA	37853mA	2mW
C14	0mA	0mA	0mW
C15	0mA	0mA	0mW
C16	0mA	0mA	0mW
C17	57mA	975mA	0mW
C18	0mA	0mA	0mW
C19	39mA	1298mA	0mW
C20	32mA	714mA	0mW
C21	1051mA	47576mA	2mW
C24	837mA	50162mA	0mW
D1	18mA	940mA	2mW
D2	11mA	350mA	1mW
D3	18mA	910mA	2mW
D4	11mA	351mA	1mW
L1	2048mA	2795mA	50mW
L2	2055mA	2802mA	51mW
Q1	2123mA	51346mA	1005mW
Q2	954mA	48810mA	55mW
Q3	1020mA	49057mA	956mW
Q4	2091mA	46643mA	356mW
Q5	2131mA	51480mA	1007mW
Q6	957mA	48938mA	55mW
Q7	1024mA	49212mA	959mW
Q8	2099mA	46789mA	358mW

R3	0mA	0mA	1mW
R4	0mA	3mA	1µW
R5	0mA	0mA	6mW
R6	0mA	0mA	356µW
R7	0mA	0mA	17µW
R8	1407mA	49458mA	3mW
R9	0mA	0mA	6mW
R10	0mA	0mA	212µW
R11	1804mA	3622mA	88mW
R12	0mA	0mA	0µW
R13	0mA	0mA	0µW
R14	0mA	0mA	0µW
R15	0mA	0mA	0µW
R16	0mA	0mA	0µW
R17	1962mA	2805mA	46mW
R18	0mA	0mA	4mW
R19	0mA	0mA	1mW
R20	0mA	0mA	1µW
R21	0mA	0mA	6mW
R22	0mA	0mA	356µW
R23	0mA	0mA	17µW
R24	1402mA	49302mA	3mW
R25	0mA	0mA	6mW
R26	0mA	0mA	212µW
R27	1797mA	3333mA	87mW
R28	0mA	0mA	0µW
R29	0mA	0mA	0µW
R30	0mA	0mA	0µW
U1	58mA	946mA	486mW
U2	58mA	947mA	485mW

Table 17-8: Power dissipation and efficiency, $V_{IN} = 40V$

Efficiency: 95.5%
Input: 165W @ 40V
Output: 157W @ 35.8V

Ref.	**Irms**	**Ipeak**	**Dissipation**
C1	0mA	0mA	0mW
C2	0mA	0mA	0mW
C3	0mA	2mA	0mW
C4	58mA	944mA	0mW

Ref.	**Irms**	**Ipeak**	**Dissipation**
R1	2178mA	12646mA	57mW
R2	0mA	0mA	5mW
R3	0mA	0mA	1mW
R4	0mA	2mA	1µW

C5	0mA	0mA	0mW
C6	39mA	1294mA	0mW
C7	32mA	711mA	0mW
C8	1023mA	47456mA	2mW
C11	707mA	35560mA	2mW
C14	0mA	0mA	0mW
C15	0mA	0mA	0mW
C16	0mA	1mA	0mW
C17	58mA	941mA	0mW
C18	0mA	0mA	0mW
C19	39mA	1292mA	0mW
C20	32mA	707mA	0mW
C21	1011mA	47546mA	2mW
C24	919mA	46655mA	0mW
D1	18mA	914mA	2mW
D2	13mA	341mA	1mW
D3	18mA	918mA	2mW
D4	13mA	341mA	1mW
L1	2333mA	2654mA	65mW
L2	2336mA	2657mA	66mW
Q1	2348mA	47622mA	1243mW
Q2	1177mA	45429mA	73mW
Q3	1036mA	47614mA	1097mW
Q4	2430mA	45344mA	430mW
Q5	2351mA	48183mA	1242mW
Q6	1178mA	45952mA	73mW
Q7	1037mA	47519mA	1099mW
Q8	2433mA	45257mA	430mW

R5	0mA	0mA	7mW
R6	0mA	0mA	440µW
R7	0mA	0mA	17µW
R8	1575mA	47773mA	4mW
R9	0mA	0mA	6mW
R10	0mA	0mA	212µW
R11	2202mA	3955mA	131mW
R12	0mA	0mA	0µW
R13	0mA	0mA	0µW
R14	0mA	0mA	0µW
R15	0mA	0mA	0µW
R16	0mA	0mA	0µW
R17	2172mA	2649mA	57mW
R18	0mA	0mA	5mW
R19	0mA	0mA	1mW
R20	0mA	1mA	1µW
R21	0mA	0mA	7mW
R22	0mA	0mA	440µW
R23	0mA	0mA	17µW
R24	1573mA	47866mA	4mW
R25	0mA	0mA	6mW
R26	0mA	0mA	212µW
R27	2199mA	3728mA	131mW
R28	0mA	0mA	0µW
R29	0mA	0mA	0µW
R30	0mA	0mA	0µW
U1	58mA	941mA	541mW
U2	58mA	941mA	540mW

Table 17-9: Power dissipation and efficiency, $V_{IN} = 45V$

Efficiency: 96.8%
Input: 207W @ 45V
Output: 200W @ 35.8V

Ref.	**Irms**	**Ipeak**	**Dissipation**
C1	0mA	0mA	0mW
C2	0mA	0mA	0mW
C3	0mA	3mA	0mW
C4	43mA	963mA	0mW
C5	0mA	0mA	0mW
C6	40mA	1302mA	0mW

Ref.	**Irms**	**Ipeak**	**Dissipation**
R1	2512mA	14082mA	76mW
R2	0mA	0mA	6mW
R3	0mA	0mA	2mW
R4	0mA	3mA	3µW
R5	0mA	0mA	9mW
R6	0mA	0mA	556µW

C7	1mA	711mA	0mW
C8	193mA	1851mA	0mW
C11	815mA	39583mA	3mW
C14	0mA	0mA	0mW
C15	0mA	0mA	0mW
C16	0mA	1mA	0mW
C17	43mA	961mA	0mW
C18	0mA	0mA	0mW
C19	40mA	1300mA	0mW
C20	1mA	711mA	0mW
C21	190mA	1797mA	0mW
C24	1056mA	52643mA	0mW
D1	18mA	941mA	2mW
D2	0mA	25mA	0mW
D3	18mA	943mA	2mW
D4	0mA	25mA	0mW
L1	2807mA	3246mA	95mW
L2	2807mA	3238mA	95mW
Q1	2719mA	53800mA	1627mW
Q2	1541mA	51191mA	106mW
Q3	1mA	1792mA	-0mW
Q4	2807mA	4615mA	812mW
Q5	2720mA	53649mA	1626mW
Q6	1542mA	51050mA	106mW
Q7	1mA	1859mA	-0mW
Q8	2807mA	4672mA	811mW

R7	0mA	0mA	17µW
R8	1540mA	50966mA	4mW
R9	0mA	0mA	6mW
R10	0mA	0mA	212µW
R11	2800mA	2834mA	212mW
R12	0mA	0mA	0µW
R13	0mA	0mA	0µW
R14	0mA	0mA	1µW
R15	0mA	0mA	0µW
R16	0mA	0mA	0µW
R17	2510mA	3228mA	76mW
R18	0mA	0mA	6mW
R19	0mA	0mA	2mW
R20	0mA	1mA	3µW
R21	0mA	0mA	9mW
R22	0mA	0mA	556µW
R23	0mA	0mA	17µW
R24	1539mA	51107mA	4mW
R25	0mA	0mA	6mW
R26	0mA	0mA	212µW
R27	2800mA	2827mA	212mW
R28	0mA	0mA	0µW
R29	0mA	0mA	1µW
R30	0mA	0mA	0µW
U1	58mA	962mA	354mW
U2	58mA	962mA	353mW

Table 17-10: Power dissipation and efficiency, $V_{IN} = 50V$

Efficiency: 96.7%
Input: 256W @ 50V
Output: 248W @ 35.8V

Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	0mA	0mA	0mW
C3	0mA	3mA	0mW
C4	43mA	1075mA	0mW
C5	0mA	0mA	0mW
C6	40mA	1403mA	0mW
C7	2mA	721mA	0mW
C8	271mA	1826mA	0mW
C11	961mA	44736mA	4mW
C14	0mA	0mA	0mW
C15	0mA	0mA	0mW
C16	0mA	1mA	0mW
C17	43mA	1079mA	0mW
C18	0mA	0mA	0mW
C19	40mA	1407mA	0mW
C20	2mA	721mA	0mW
C21	268mA	1782mA	0mW
C24	1242mA	58819mA	0mW
D1	19mA	1063mA	2mW
D2	0mA	25mA	0mW
D3	19mA	1059mA	2mW
D4	0mA	25mA	0mW
L1	3480mA	4029mA	145mW
L2	3482mA	4043mA	146mW
Q1	3195mA	60190mA	2163mW
Q2	2114mA	57093mA	169mW
Q3	1mA	1810mA	-0mW
Q4	3480mA	5246mA	826mW
Q5	3197mA	60706mA	2160mW
Q6	2116mA	57573mA	169mW
Q7	1mA	1862mA	-0mW
Q8	3482mA	5302mA	827mW

Ref.	Irms	Ipeak	Dissipation
R1	2950mA	15981mA	104mW
R2	0mA	0mA	7mW
R3	0mA	0mA	2mW
R4	0mA	3mA	6µW
R5	0mA	0mA	11mW
R6	0mA	0mA	687µW
R7	0mA	0mA	17µW
R8	2113mA	57482mA	7mW
R9	0mA	0mA	6mW
R10	0mA	0mA	212µW
R11	3471mA	3510mA	325mW
R12	0mA	0mA	0µW
R13	0mA	0mA	0µW
R14	0mA	0mA	0µW
R15	0mA	0mA	0µW
R16	0mA	0mA	0µW
R17	2947mA	4000mA	104mW
R18	0mA	0mA	7mW
R19	0mA	0mA	2mW
R20	0mA	1mA	6µW
R21	0mA	0mA	11mW
R22	0mA	0mA	687µW
R23	0mA	0mA	17µW
R24	2112mA	57001mA	7mW
R25	0mA	0mA	6mW
R26	0mA	0mA	212µW
R27	3469mA	3489mA	325mW
R28	0mA	0mA	0µW
R29	0mA	0mA	0µW
R30	0mA	0mA	0µW
U1	59mA	980mA	399mW
U2	59mA	981mA	398mW

F. Finalized LTspice Simulation Results

Based on Figure 11-1 and Initial Design Netlist (Section D)

Table 17-11: Power dissipation and efficiency, $V_{IN} = 6V$ and 0.1Ω input parasitic

Efficiency: 84.6%			
Input: 2.95W @ 5.94V			
Output: 2.5W @ 31.2V			
Ref.	**Irms**	**Ipeak**	**Dissipation**
C1	0mA	0mA	0mW
C2	0mA	0mA	0mW
CBS1	6mA	605mA	0mW
CBS2	1mA	27mA	0mW
CBS3	7mA	604mA	0mW
CBS4	1mA	27mA	0mW
CIN1	19mA	116mA	0mW
CIN2	19mA	116mA	0mW
CIN3	19mA	116mA	0mW
CIN4	19mA	116mA	0mW
CIN5	19mA	118mA	0mW
CIN6	19mA	118mA	0mW
CIN7	19mA	118mA	0mW
CIN8	19mA	118mA	0mW
CINTV1	58mA	682mA	0mW
CINTV2	61mA	716mA	0mW
COUT1	52mA	531mA	0mW
COUT2	52mA	531mA	0mW
COUT3	52mA	531mA	0mW
COUT4	52mA	531mA	0mW
COUT5	51mA	525mA	0mW
COUT6	51mA	525mA	0mW
COUT7	51mA	525mA	0mW
COUT8	51mA	525mA	0mW
CSS1	0mA	0mA	0mW
CSS2	0mA	0mA	0mW
CVC1	0mA	0mA	0mW
CVC2	0mA	0mA	0mW
CVREF1	0mA	0mA	0mW
CVREF2	0mA	0mA	0mW
D1	3mA	373mA	0mW
D2	1mA	27mA	-0mW
D3	0mA	5mA	0mW

Ref.	**Irms**	**Ipeak**	**Dissipation**
D4	265mA	2782mA	28mW
D5	5mA	376mA	0mW
D6	1mA	27mA	0mW
D7	0mA	5mA	0mW
D8	261mA	2757mA	28mW
L1	686mA	2827mA	3mW
L2	685mA	2802mA	3mW
Q1	686mA	2828mA	7mW
Q2	6mA	911mA	0mW
Q3	631mA	3275mA	125mW
Q4	48mA	2025mA	1mW
Q5	685mA	2802mA	7mW
Q6	8mA	930mA	0mW
Q7	631mA	3254mA	123mW
Q8	48mA	2027mA	1mW
R1	0mA	0mA	0µW
R2	0mA	0mA	0µW
R31	0mA	0mA	0µW
R32	0mA	0mA	0µW
R33	0mA	0mA	0µW
R34	0mA	0mA	0µW
R35	0mA	0mA	0µW
RCCM1	0mA	0mA	0µW
RCCM2	0mA	0mA	0µW
REN1	0mA	0mA	103µW
REN2	0mA	0mA	32µW
REN3	0mA	0mA	103µW
REN4	0mA	0mA	32µW
RFB1	0mA	0mA	5mW
RFB2	0mA	0mA	161µW
RFB3	0mA	0mA	5mW
RFB4	0mA	0mA	161µW
RIN1	648mA	2632mA	5mW

Ref.	Irms	Ipeak	Dissipation
RIN2	646mA	2604mA	5mW
RLSENSE1	634mA	3481mA	603µW
RLSENSE2	635mA	3461mA	604µW
ROUT1	110mA	778mA	329µW
ROUT2	110mA	772mA	328µW
ROV1	0mA	0mA	156µW
ROV2	0mA	0mA	10µW
ROV3	0mA	0mA	156µW
ROV4	0mA	0mA	10µW
RSHORT1	0mA	0mA	0µW
RSHORT2	0mA	0mA	0µW

Ref.	Irms	Ipeak	Dissipation
RSS1	0mA	0mA	16µW
RSS2	0mA	0mA	16µW
RT1	0mA	0mA	17µW
RT2	0mA	0mA	17µW
RVC1	0mA	0mA	0µW
RVC2	0mA	0mA	0µW
U1	98mA	812mA	51mW
U2	98mA	813mA	52mW

Table 17-12: Power dissipation and efficiency, $V_{IN} = 10V$ and 0.5Ω input parasitic

Efficiency: 87.9%			
Input: 9.71W @ 9.1V			
Output: 8.54W @ 34.1V			
Ref.	**Irms**	**Ipeak**	**Dissipation**
C1	0mA	1mA	0mW
C2	0mA	1mA	0mW
CBS1	0mA	0mA	0mW
CBS2	2mA	147mA	0mW
CBS3	1mA	526mA	0mW
CBS4	2mA	146mA	0mW
CIN1	98mA	1004mA	1mW
CIN2	98mA	1004mA	1mW
CIN3	98mA	1004mA	1mW
CIN4	98mA	1004mA	1mW
CIN5	98mA	1030mA	1mW
CIN6	98mA	1030mA	1mW
CIN7	98mA	1030mA	1mW
CIN8	98mA	1030mA	1mW
CINTV1	57mA	706mA	0mW
CINTV2	64mA	729mA	0mW
COUT1	127mA	1346mA	2mW
COUT2	127mA	1346mA	2mW
COUT3	127mA	1346mA	2mW
COUT4	127mA	1346mA	2mW
COUT5	115mA	1324mA	1mW
COUT6	115mA	1324mA	1mW
COUT7	115mA	1324mA	1mW
COUT8	115mA	1324mA	1mW
CSS1	0mA	0mA	0mW
CSS2	0mA	0mA	0mW
CVC1	0mA	0mA	0mW
CVC2	0mA	0mA	0mW
CVREF1	0mA	0mA	0mW
CVREF2	0mA	0mA	0mW
D1	0mA	0mA	0mW
D2	2mA	147mA	0mW
D3	0mA	0mA	0mW
D4	700mA	5928mA	150mW
D5	1mA	184mA	0mW
D6	2mA	146mA	0mW

Ref.	**Irms**	**Ipeak**	**Dissipation**
D7	2mA	527mA	0mW
D8	609mA	5850mA	94mW
L1	1487mA	5980mA	15mW
L2	1316mA	5900mA	12mW
Q1	1487mA	5980mA	32mW
Q2	0mA	4mA	0mW
Q3	1311mA	6402mA	394mW
Q4	80mA	3203mA	1mW
Q5	1316mA	5901mA	25mW
Q6	1mA	665mA	0mW
Q7	1164mA	6365mA	173mW
Q8	59mA	3156mA	1mW
R1	0mA	0mA	0µW
R2	0mA	0mA	0µW
R31	0mA	0mA	0µW
R32	0mA	0mA	0µW
R33	0mA	0mA	0µW
R34	0mA	0mA	0µW
R35	0mA	0mA	0µW
RCCM1	0mA	0mA	196µW
RCCM2	0mA	0mA	196µW
REN1	0mA	0mA	244µW
REN2	0mA	0mA	76µW
REN3	0mA	0mA	244µW
REN4	0mA	0mA	76µW
RFB1	0mA	0mA	6mW
RFB2	0mA	0mA	198µW
RFB3	0mA	0mA	6mW
RFB4	0mA	0mA	198µW
RIN1	1438mA	6317mA	25mW
RIN2	1251mA	6196mA	19mW
RLSENSE1	1313mA	6590mA	3mW
RLSENSE2	1165mA	6553mA	2mW
ROUT1	315mA	1867mA	3mW
ROUT2	268mA	1893mA	2mW
ROV1	0mA	0mA	371µW

Ref.	Irms	Ipeak	Dissipation
ROV2	0mA	0mA	23µW
ROV3	0mA	0mA	371µW
ROV4	0mA	0mA	23µW
RSHORT1	0mA	0mA	0µW
RSHORT2	0mA	0mA	0µW
RSS1	0mA	0mA	1µW
RSS2	0mA	0mA	1µW
RT1	0mA	0mA	17µW
RT2	0mA	0mA	17µW
RVC1	0mA	0mA	0µW
RVC2	0mA	0mA	0µW
U1	102mA	813mA	99mW
U2	102mA	813mA	95mW

Table 17-13: Power dissipation and efficiency, $V_{IN} = 20V$ and 0.9Ω input parasitic

Efficiency: 93.1%
Input: 38.6W @ 16.9V
Output: 35.9W @ 33.4V

Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	0mA	0mA	0mW
CBS1	6mA	543mA	0mW
CBS2	2mA	31mA	0mW
CBS3	6mA	540mA	0mW
CBS4	4mA	685mA	0mW
CIN1	85mA	465mA	1mW
CIN2	85mA	465mA	1mW
CIN3	85mA	465mA	1mW
CIN4	85mA	465mA	1mW
CIN5	85mA	465mA	1mW
CIN6	85mA	465mA	1mW
CIN7	85mA	465mA	1mW
CIN8	85mA	465mA	1mW
CINTV1	57mA	859mA	0mW
CINTV2	62mA	879mA	0mW
COUT1	185mA	716mA	3mW
COUT2	185mA	716mA	3mW
COUT3	185mA	716mA	3mW
COUT4	185mA	716mA	3mW
COUT5	184mA	710mA	3mW
COUT6	184mA	710mA	3mW
COUT7	184mA	710mA	3mW
COUT8	184mA	710mA	3mW
CSS1	0mA	0mA	0mW
CSS2	0mA	0mA	0mW
CVC1	0mA	0mA	0mW
CVC2	0mA	0mA	0mW
CVREF1	0mA	0mA	0mW
CVREF2	0mA	0mA	0mW
D1	4mA	262mA	0mW
D2	2mA	31mA	0mW
D3	34mA	1445mA	1mW
D4	1316mA	4068mA	467mW
D5	4mA	261mA	0mW
D6	2mA	31mA	0mW

Ref.	Irms	Ipeak	Dissipation
D7	31mA	1436mA	1mW
D8	1325mA	4070mA	472mW
L1	1887mA	4109mA	25mW
L2	1899mA	4111mA	25mW
Q1	1887mA	4109mA	52mW
Q2	26mA	1633mA	0mW
Q3	1351mA	4102mA	481mW
Q4	91mA	2829mA	1mW
Q5	1898mA	4111mA	52mW
Q6	26mA	1623mA	0mW
Q7	1359mA	4104mA	484mW
Q8	95mA	2838mA	1mW
R1	0mA	0mA	0µW
R2	0mA	0mA	0µW
R31	0mA	0mA	0µW
R32	0mA	0mA	0µW
R33	0mA	0mA	0µW
R34	0mA	0mA	0µW
R35	0mA	0mA	0µW
RCCM1	0mA	0mA	0µW
RCCM2	0mA	0mA	0µW
REN1	0mA	0mA	837µW
REN2	0mA	0mA	259µW
REN3	0mA	0mA	837µW
REN4	0mA	0mA	259µW
RFB1	0mA	0mA	5mW
RFB2	0mA	0mA	188µW
RFB3	0mA	0mA	5mW
RFB4	0mA	0mA	188µW
RIN1	1862mA	3711mA	42mW
RIN2	1873mA	3711mA	42mW
RLSENSE1	1353mA	4250mA	3mW
RLSENSE2	1361mA	4254mA	3mW
ROUT1	734mA	1738mA	15mW
ROUT2	741mA	1748mA	15mW
ROV1	0mA	0mA	1mW

Ref.	Irms	Ipeak	Dissipation
ROV2	0mA	0mA	79µW
ROV3	0mA	0mA	1mW
ROV4	0mA	0mA	79µW
RSHORT1	0mA	0mA	0µW
RSHORT2	0mA	0mA	0µW
RSS1	0mA	0mA	3µW
RSS2	0mA	0mA	3µW
RT1	0mA	0mA	17µW
RT2	0mA	0mA	17µW
RVC1	0mA	0mA	0µW
RVC2	0mA	0mA	0µW
U1	103mA	813mA	208mW
U2	103mA	813mA	207mW

Table 17-14: Power dissipation and efficiency, $V_{IN} = 30V$ and 0.9Ω input parasitic

Efficiency: 96.0%
Input: 90.4W @ 26.7V
Output: 86.8W @ 36.2V

Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	0mA	0mA	0mW
CBS1	4mA	542mA	0mW
CBS2	23mA	802mA	0mW
CBS3	3mA	541mA	0mW
CBS4	23mA	763mA	0mW
CIN1	73mA	384mA	1mW
CIN2	73mA	384mA	1mW
CIN3	73mA	384mA	1mW
CIN4	73mA	384mA	1mW
CIN5	73mA	386mA	1mW
CIN6	73mA	386mA	1mW
CIN7	73mA	386mA	1mW
CIN8	73mA	386mA	1mW
CINTV1	58mA	882mA	0mW
CINTV2	63mA	898mA	0mW
COUT1	170mA	831mA	3mW
COUT2	170mA	831mA	3mW
COUT3	170mA	831mA	3mW
COUT4	170mA	831mA	3mW
COUT5	169mA	834mA	3mW
COUT6	169mA	834mA	3mW
COUT7	169mA	834mA	3mW
COUT8	169mA	834mA	3mW
CSS1	0mA	0mA	0mW
CSS2	0mA	0mA	0mW
CVC1	0mA	0mA	0mW
CVC2	0mA	0mA	0mW
CVREF1	0mA	0mA	0mW
CVREF2	0mA	0mA	0mW
D1	3mA	274mA	0mW
D2	9mA	138mA	0mW
D3	41mA	2686mA	2mW
D4	1528mA	4205mA	654mW
D5	2mA	275mA	0mW
D6	9mA	140mA	0mW

Ref.	Irms	Ipeak	Dissipation
D7	33mA	2690mA	2mW
D8	1530mA	4269mA	653mW
L1	1880mA	4229mA	25mW
L2	1882mA	4293mA	25mW
Q1	1880mA	4230mA	52mW
Q2	26mA	2852mA	0mW
Q3	1008mA	4353mA	581mW
Q4	442mA	2885mA	8mW
Q5	1882mA	4295mA	50mW
Q6	26mA	2857mA	0mW
Q7	1010mA	4427mA	580mW
Q8	441mA	2909mA	7mW
R1	0mA	0mA	0µW
R2	0mA	0mA	0µW
R31	0mA	0mA	0µW
R32	0mA	0mA	0µW
R33	0mA	0mA	0µW
R34	0mA	0mA	0µW
R35	0mA	0mA	0µW
RCCM1	0mA	0mA	0µW
RCCM2	0mA	0mA	0µW
REN1	0mA	0mA	2mW
REN2	0mA	0mA	643µW
REN3	0mA	0mA	2mW
REN4	0mA	0mA	643µW
RFB1	0mA	0mA	6mW
RFB2	0mA	0mA	217µW
RFB3	0mA	0mA	6mW
RFB4	0mA	0mA	217µW
RIN1	1888mA	3581mA	43mW
RIN2	1888mA	3585mA	43mW
RLSENSE1	1013mA	4553mA	2mW
RLSENSE2	1014mA	4626mA	2mW
ROUT1	1273mA	2502mA	44mW
ROUT2	1272mA	2542mA	44mW
ROV1	0mA	0mA	3mW

Ref.	Irms	Ipeak	Dissipation
ROV2	0mA	0mA	196µW
ROV3	0mA	0mA	3mW
ROV4	0mA	0mA	196µW
RSHORT1	0mA	0mA	0µW
RSHORT2	0mA	0mA	0µW
RSS1	0mA	0mA	2µW
RSS2	0mA	0mA	2µW
RT1	0mA	0mA	17µW
RT2	0mA	0mA	17µW
RVC1	0mA	0mA	0µW
RVC2	0mA	0mA	0µW
U1	104mA	844mA	368mW
U2	104mA	846mA	367mW

Table 17-15: Power dissipation and efficiency, $V_{IN} = 40V$ and 1Ω input parasitic

Efficiency: 95.2%
Input: 162W @ 35.4V
Output: 155W @ 36.4V

Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	0mA	0mA	0mW
CBS1	64mA	540mA	0mW
CBS2	73mA	804mA	0mW
CBS3	64mA	537mA	0mW
CBS4	73mA	771mA	0mW
CIN1	136mA	399mA	2mW
CIN2	136mA	399mA	2mW
CIN3	136mA	399mA	2mW
CIN4	136mA	399mA	2mW
CIN5	137mA	402mA	2mW
CIN6	137mA	402mA	2mW
CIN7	137mA	402mA	2mW
CIN8	137mA	402mA	2mW
CINTV1	115mA	922mA	0mW
CINTV2	119mA	930mA	0mW
COUT1	172mA	546mA	3mW
COUT2	172mA	546mA	3mW
COUT3	172mA	546mA	3mW
COUT4	172mA	546mA	3mW
COUT5	172mA	547mA	3mW
COUT6	172mA	547mA	3mW
COUT7	172mA	547mA	3mW
COUT8	172mA	547mA	3mW
CSS1	0mA	0mA	0mW
CSS2	0mA	0mA	0mW
CVC1	0mA	0mA	0mW
CVC2	0mA	0mA	0mW
CVREF1	0mA	0mA	0mW
CVREF2	0mA	0mA	0mW
D1	49mA	289mA	8mW
D2	34mA	180mA	5mW
D3	577mA	2552mA	85mW
D4	669mA	2892mA	105mW
D5	49mA	290mA	8mW
D6	34mA	181mA	5mW

Ref.	Irms	Ipeak	Dissipation
D7	579mA	2549mA	86mW
D8	671mA	2889mA	104mW
L1	2497mA	2902mA	44mW
L2	2496mA	2899mA	44mW
Q1	2376mA	3301mA	896mW
Q2	453mA	2723mA	39mW
Q3	980mA	3257mA	807mW
Q4	2208mA	2900mA	122mW
Q5	2373mA	3305mA	896mW
Q6	458mA	2720mA	38mW
Q7	979mA	3252mA	792mW
Q8	2207mA	2896mA	121mW
R1	0mA	0mA	0µW
R2	0mA	0mA	0µW
R31	0mA	0mA	0µW
R32	0mA	0mA	0µW
R33	0mA	0mA	0µW
R34	0mA	0mA	0µW
R35	0mA	0mA	0µW
RCCM1	0mA	0mA	0µW
RCCM2	0mA	0mA	0µW
REN1	0mA	0mA	4mW
REN2	0mA	0mA	1mW
REN3	0mA	0mA	4mW
REN4	0mA	0mA	1mW
RFB1	0mA	0mA	6mW
RFB2	0mA	0mA	219µW
RFB3	0mA	0mA	6mW
RFB4	0mA	0mA	219µW
RIN1	2335mA	3265mA	65mW
RIN2	2332mA	3237mA	65mW
RLSENSE1	1232mA	3464mA	2mW
RLSENSE2	1233mA	3459mA	2mW
ROUT1	2158mA	2987mA	126mW
ROUT2	2156mA	2994mA	126mW
ROV1	0mA	0mA	6mW

Ref.	Irms	Ipeak	Dissipation
ROV2	0mA	0mA	344µW
ROV3	0mA	0mA	6mW
ROV4	0mA	0mA	344µW
RSHORT1	0mA	0mA	0µW
RSHORT2	0mA	0mA	0µW
RSS1	0mA	0mA	0µW
RSS2	0mA	0mA	0µW
RT1	0mA	0mA	17µW
RT2	0mA	0mA	17µW
RVC1	0mA	0mA	0µW
RVC2	0mA	0mA	0µW
U1	104mA	864mA	1557mW
U2	104mA	862mA	1558mW

Table 17-16: Power dissipation and efficiency, $V_{IN} = 50V$ and 1Ω input parasitic

Efficiency: 96.9%
Input: 247W @ 44.4V
Output: 239W @ 36.3V

Ref.	Irms	Ipeak	Dissipation
C1	0mA	0mA	0mW
C2	0mA	0mA	0mW
CBS1	66mA	527mA	0mW
CBS2	12mA	651mA	0mW
CBS3	66mA	527mA	0mW
CBS4	12mA	659mA	0mW
CIN1	202mA	448mA	4mW
CIN2	202mA	448mA	4mW
CIN3	202mA	448mA	4mW
CIN4	202mA	448mA	4mW
CIN5	204mA	452mA	4mW
CIN6	204mA	452mA	4mW
CIN7	204mA	452mA	4mW
CIN8	204mA	452mA	4mW
CINTV1	96mA	942mA	0mW
CINTV2	100mA	956mA	0mW
COUT1	34mA	85mA	0mW
COUT2	34mA	85mA	0mW
COUT3	34mA	85mA	0mW
COUT4	34mA	85mA	0mW
COUT5	33mA	85mA	0mW
COUT6	33mA	85mA	0mW
COUT7	33mA	85mA	0mW
COUT8	33mA	85mA	0mW
CSS1	0mA	0mA	0mW
CSS2	0mA	0mA	0mW
CVC1	0mA	0mA	0mW
CVC2	0mA	0mA	0mW
CVREF1	0mA	0mA	0mW
CVREF2	0mA	0mA	0mW
D1	51mA	307mA	8mW
D2	0mA	0mA	0mW
D3	762mA	3463mA	116mW
D4	1362mA	3655mA	339mW
D5	52mA	308mA	8mW
D6	0mA	0mA	0mW

Ref.	Irms	Ipeak	Dissipation
D7	769mA	3456mA	118mW
D8	1380mA	3650mA	345mW
L1	3318mA	3780mA	77mW
L2	3318mA	3774mA	77mW
Q1	3041mA	3955mA	1618mW
Q2	1045mA	3644mA	54mW
Q3	0mA	11mA	-0mW
Q4	3025mA	3780mA	142mW
Q5	3032mA	3951mA	1615mW
Q6	1065mA	3637mA	57mW
Q7	0mA	11mA	-0mW
Q8	3017mA	3774mA	141mW
R1	0mA	0mA	1µW
R2	0mA	0mA	1µW
R31	0mA	0mA	0µW
R32	0mA	0mA	0µW
R33	0mA	0mA	0µW
R34	0mA	0mA	0µW
R35	0mA	0mA	0µW
RCCM1	0mA	0mA	0µW
RCCM2	0mA	0mA	0µW
REN1	0mA	0mA	6mW
REN2	0mA	0mA	2mW
REN3	0mA	0mA	6mW
REN4	0mA	0mA	2mW
RFB1	0mA	0mA	6mW
RFB2	0mA	0mA	218µW
RFB3	0mA	0mA	6mW
RFB4	0mA	0mA	218µW
RIN1	2899mA	4152mA	101mW
RIN2	2888mA	4154mA	100mW
RLSENSE1	1294mA	4022mA	3mW
RLSENSE2	1314mA	4021mA	3mW
ROUT1	3302mA	3469mA	294mW
ROUT2	3302mA	3466mA	294mW
ROV1	0mA	0mA	9mW

Ref.	Irms	Ipeak	Dissipation
ROV2	0mA	0mA	541µW
ROV3	0mA	0mA	9mW
ROV4	0mA	0mA	541µW
RSHORT1	0mA	0mA	0µW
RSHORT2	0mA	0mA	0µW
RSS1	0mA	0mA	1µW
RSS2	0mA	0mA	1µW
RT1	0mA	0mA	17µW
RT2	0mA	0mA	17µW
RVC1	0mA	0mA	0µW
RVC2	0mA	0mA	0µW
U1	104mA	933mA	1078mW
U2	104mA	933mA	1089mW

G. IXTH180N10T Characterization Data

Table 17-17: V_{GS} vs. R_{DS}
V_D = 10V

VGS [V]	RDS [Ω]
2	4.00E+09
2.12	3.86E+07
2.4	4.47E+06
2.8	5.00E+06
3.2	6.16E+06
3.4	6.10E+06
3.5	5.37E+06
3.6	3.77E+06
3.7	1.50E+06
3.8	4.30E+03
3.9	3.80E+03
4	2.80E+03
4.1	2.30E+03
4.3	1.77E+03
4.5	1.45E+03
4.8	1.20E+03
5	1.03E+03
6	6.50E+02
7	4.50E+02

Table 17-18: V_{GS} vs. I_D
VD = 0V

V_{GS} [V]	I_D [A]
1	7.00E-07
2	1.30E-06
3	1.30E-06
3.5	2.00E-05
3.7	9.00E-05
3.9	4.00E-04
4	7.61E-04
4.1	1.14E-03
4.2	1.40E-03
4.3	1.56E-03
4.5	1.70E-03
4.7	1.85E-03
4.9	1.94E-03
5	1.98E-03
6	2.25E-03

Table 17-19: V_{GS} vs. I_D
V_D = 6V

V_{GS} [V]	I_D [A]
1	2.80E-08
2	3.30E-08
3	1.20E-06
3.3	5.00E-06
3.5	2.00E-05
3.6	4.70E-05
3.7	1.00E-04
3.8	2.30E-04
3.9	5.00E-04
4	1.26E-03
4.1	2.85E-03
4.2	6.40E-03
4.3	1.40E-02
4.4	3.40E-02
4.5	5.20E-02
5	5.30E-02
6	5.30E-02

H. Testing Oscilloscope Captures

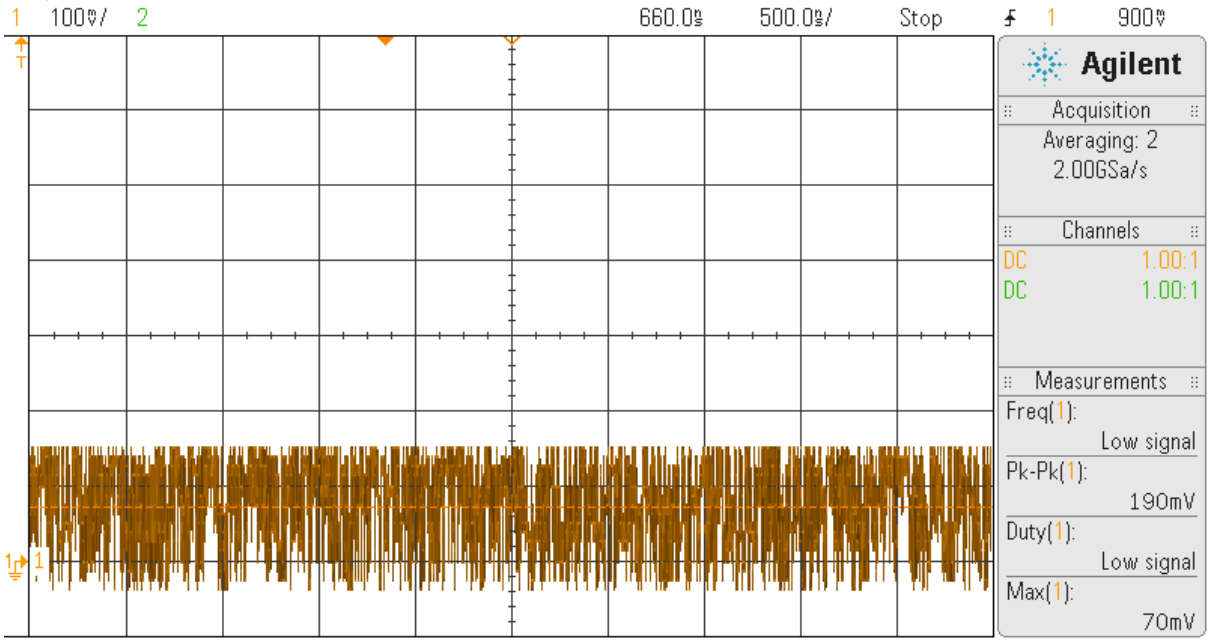


Figure 17-2: Hardware Testing, Primary SHORT Pin, Pin 5, 30V Case

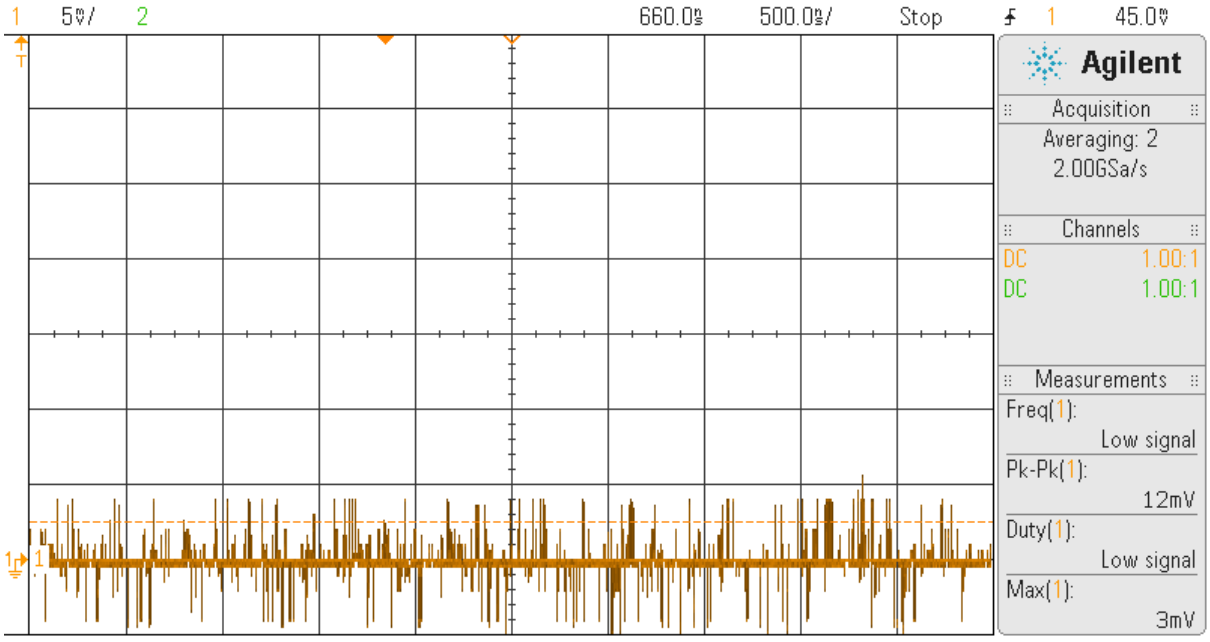


Figure 17-3: Hardware Testing, Primary FB Pin, Pin 37, 30V Case

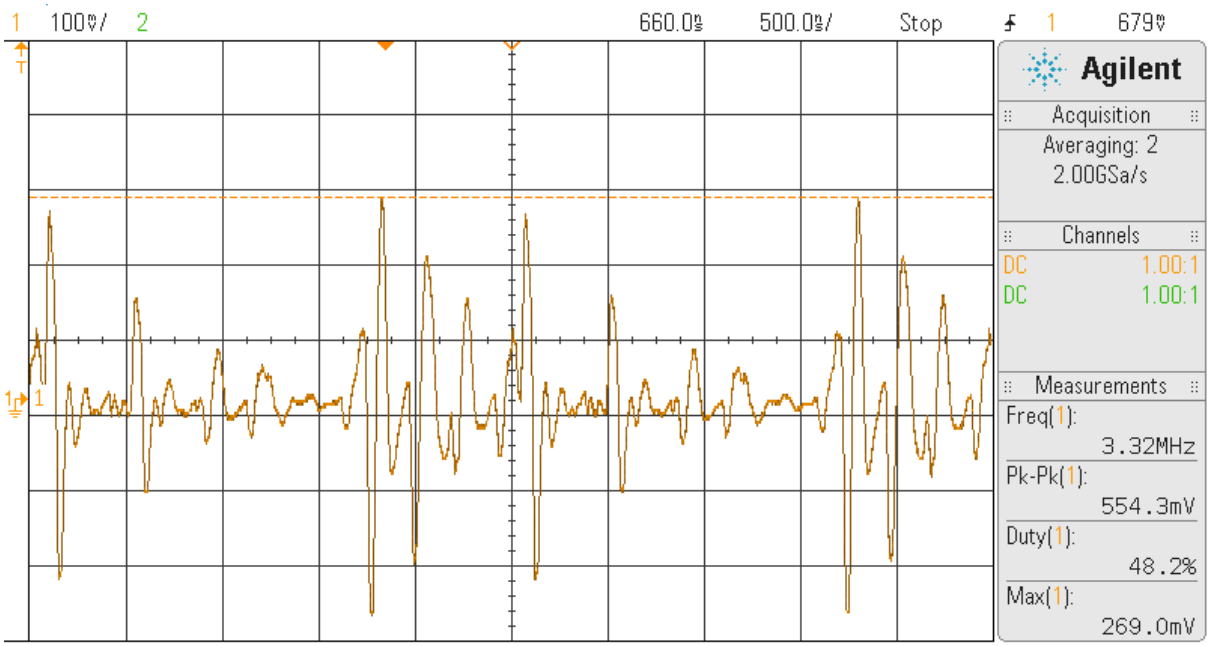


Figure 17-4: Hardware Testing, Primary SNSP Pin, Pin 27, 30V Case

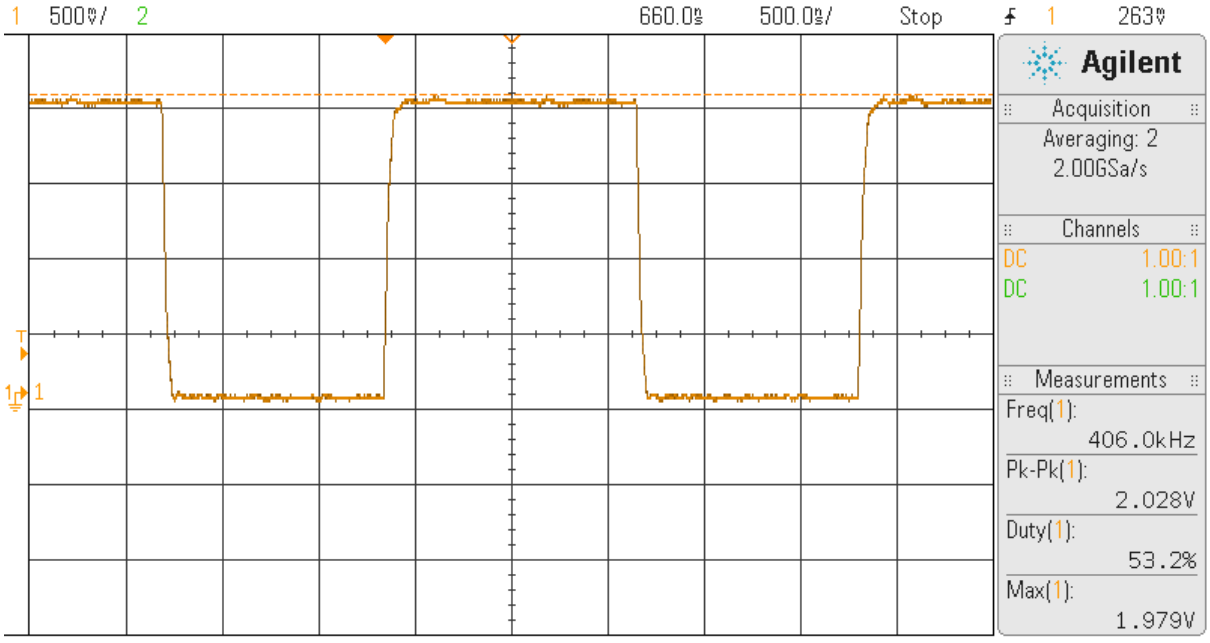


Figure 17-5: Hardware Testing, Primary CLKOUT Pin, Pin 33, 30V Case

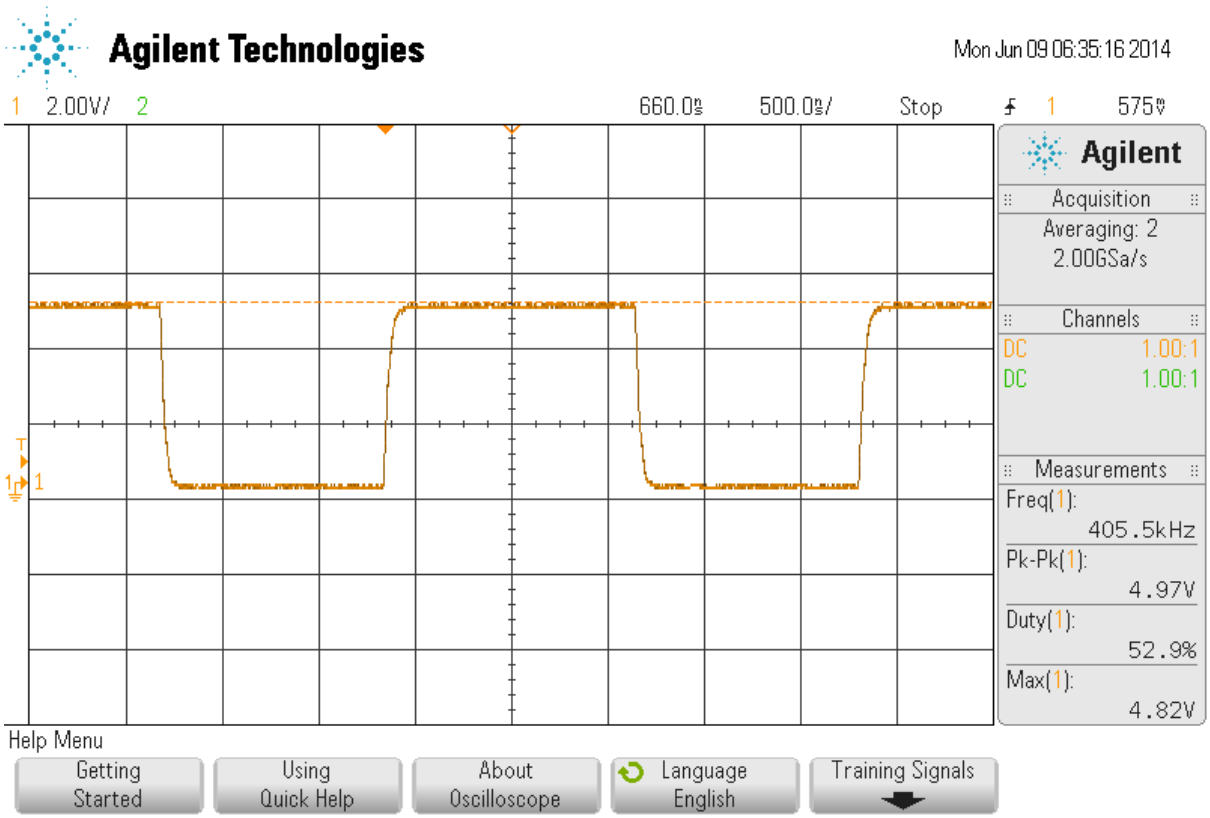


Figure 17-6: Hardware Testing, Secondary CLKOUT Pin, Pin 33, 30V Case

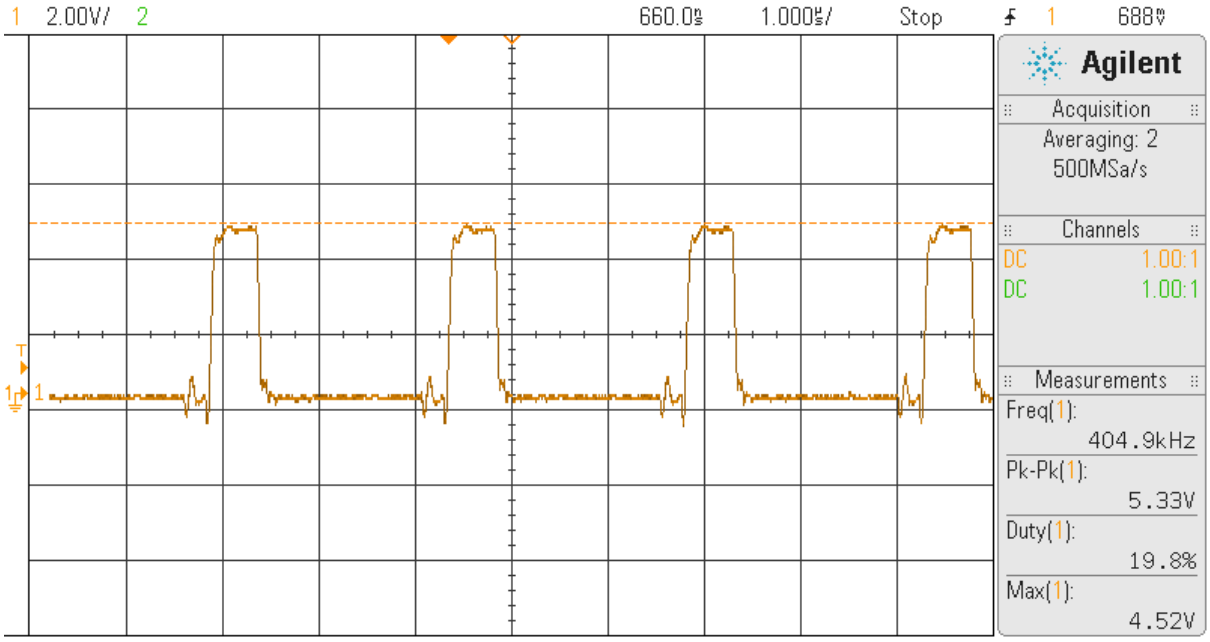


Figure 17-7: Hardware Testing, Primary TG1 Pin, Pin 14, 30V Case

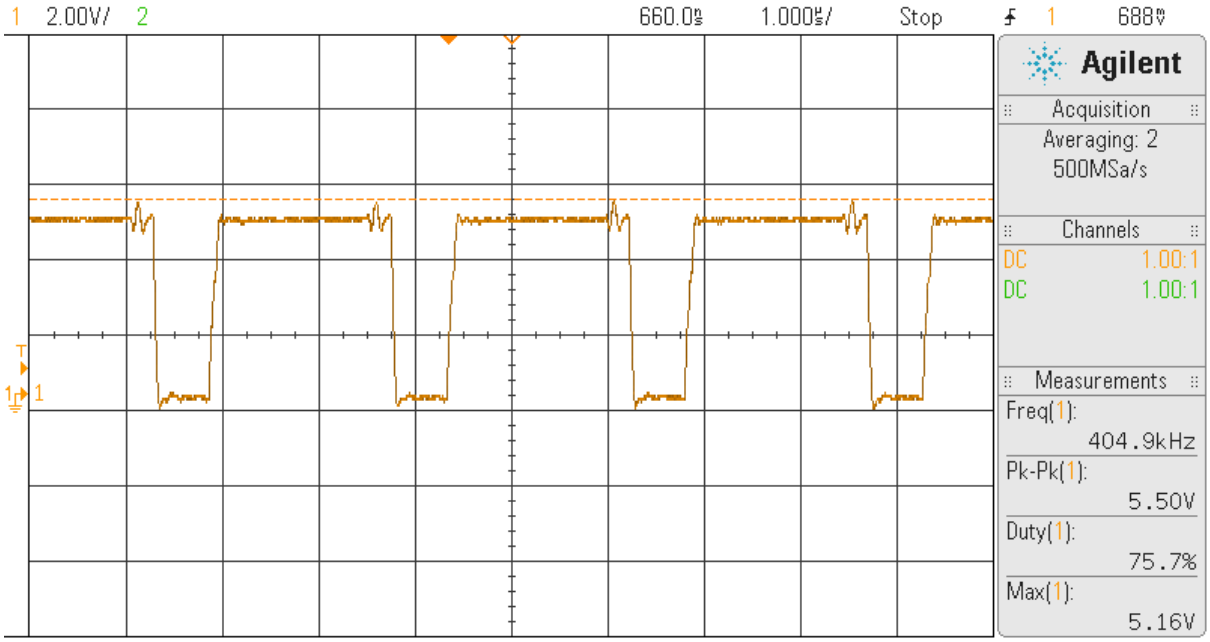


Figure 17-8: Hardware Testing, Primary BG1 Pin, Pin 18, 30V Case

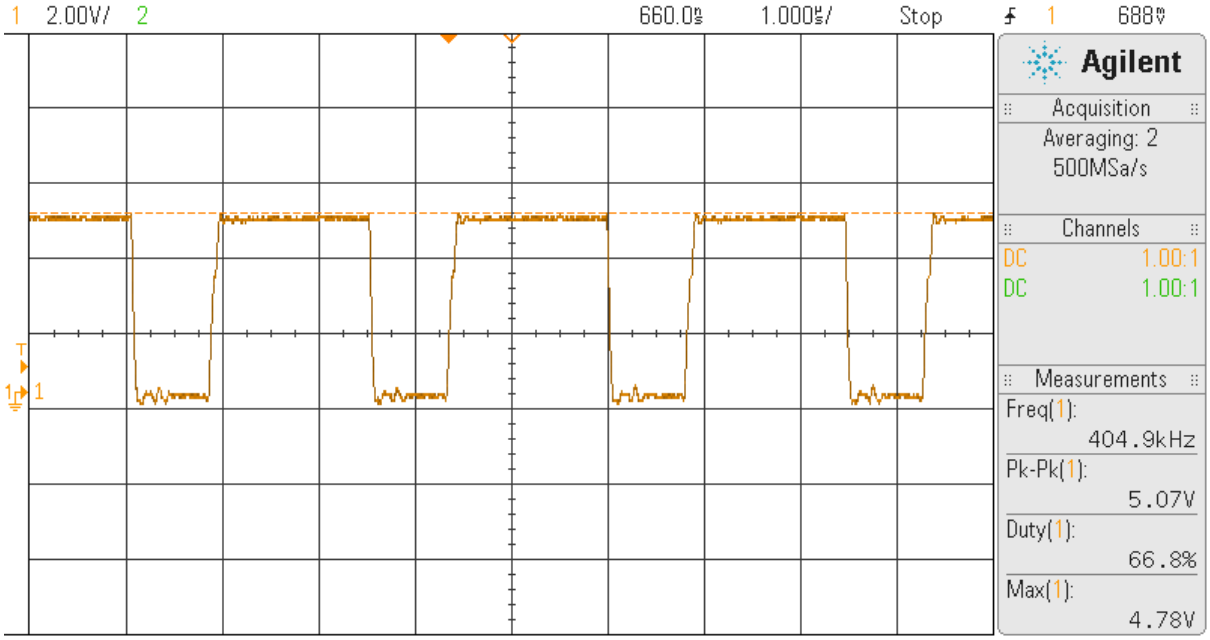


Figure 17-9: Hardware Testing, Primary BG2 Pin, Pin 19, 30V Case

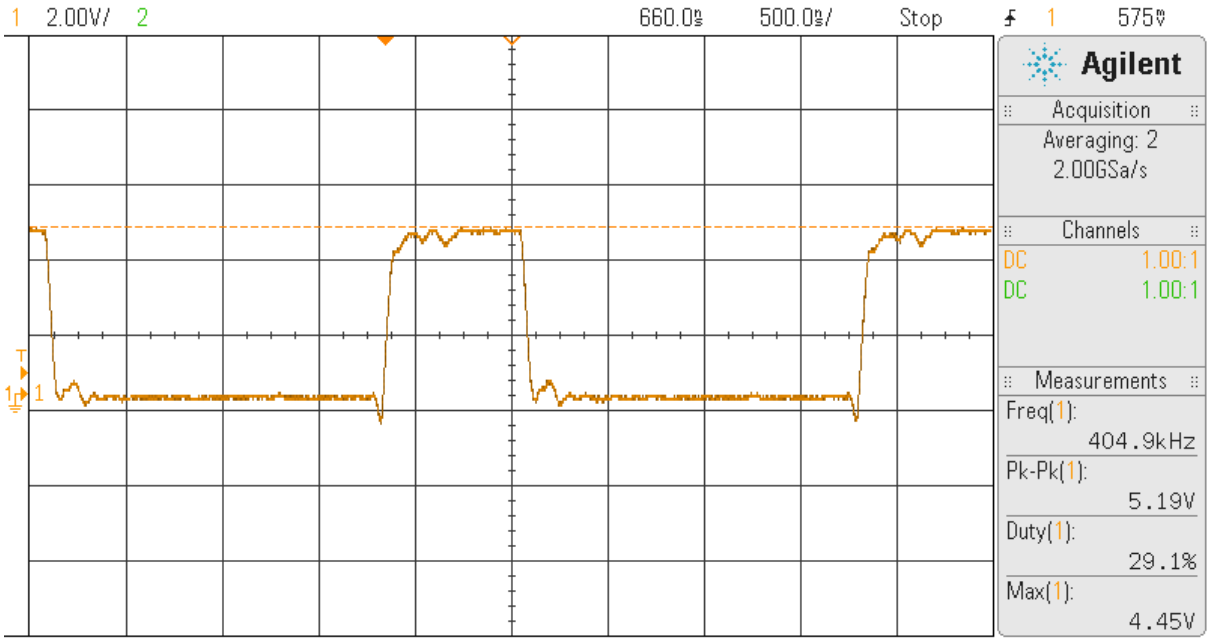


Figure 17-10: Hardware Testing, Primary TG2 Pin, Pin 24, 30V Case

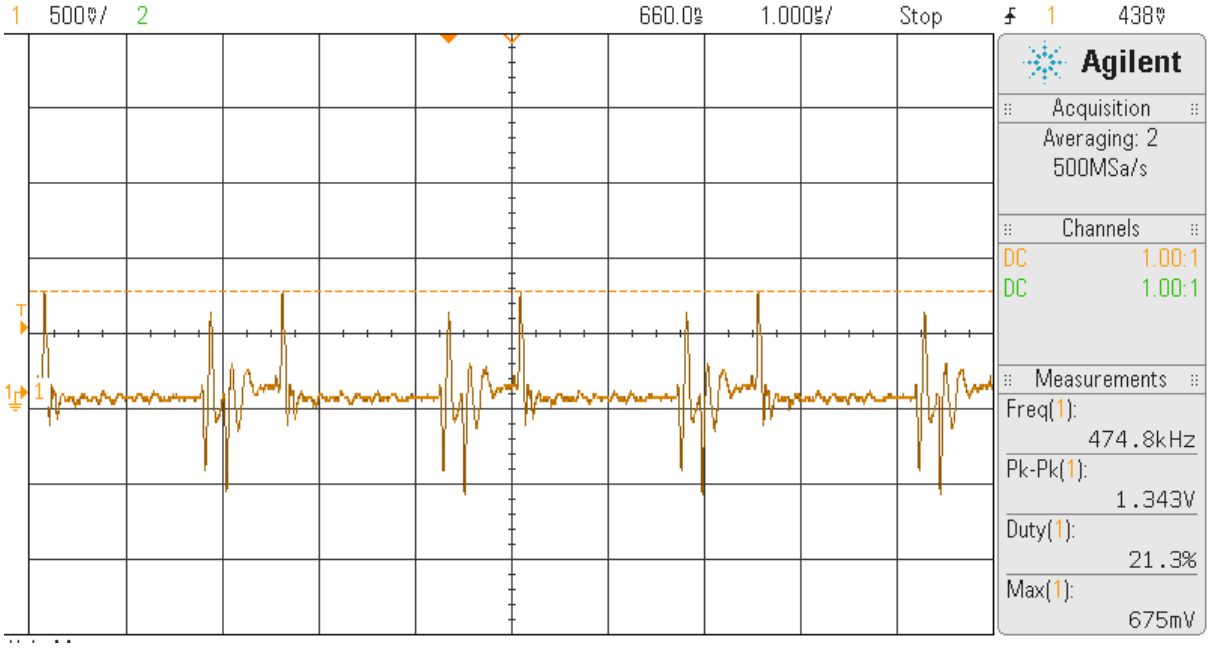


Figure 17-11: Hardware Testing, Primary SW1, Pin 16, 30V Case

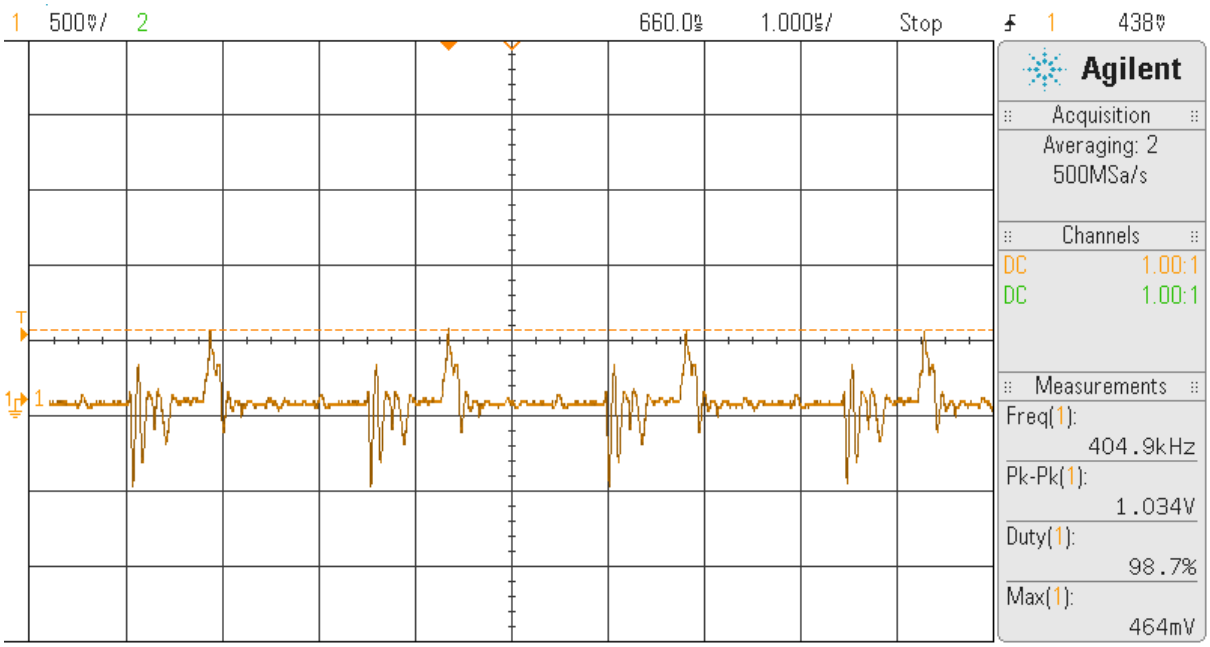


Figure 17-12: Hardware Testing, Primary SW2 Pin, Pin 21, 30V Case

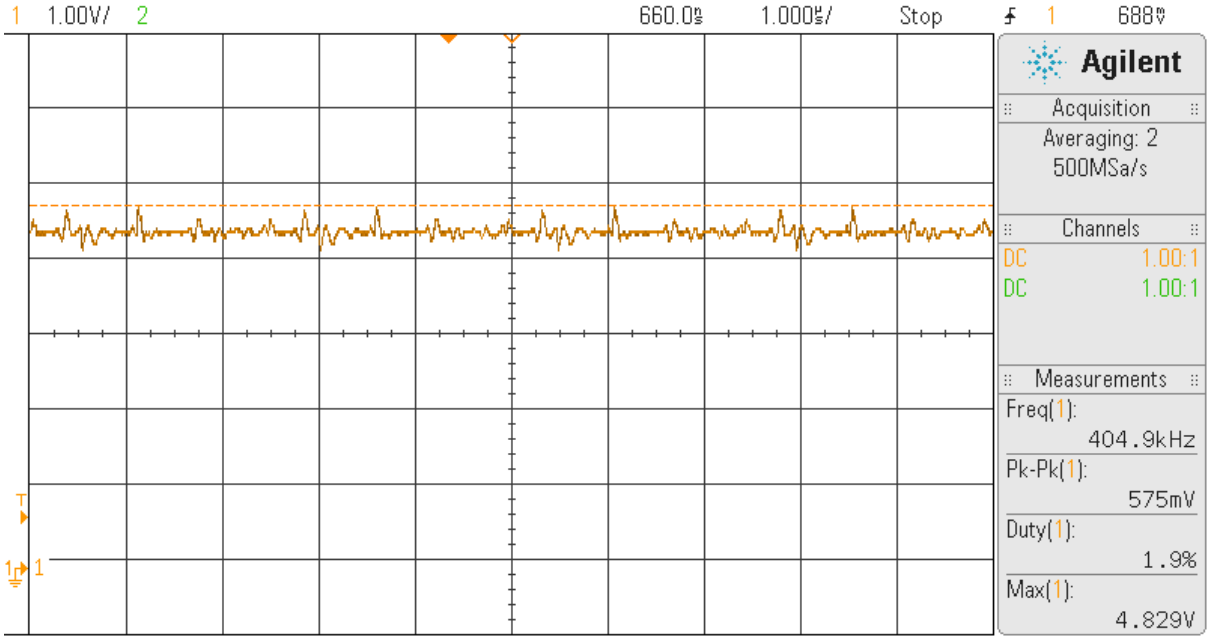


Figure 17-13: Hardware Testing, Primary BST1 Pin, Pin 15, 30V Case

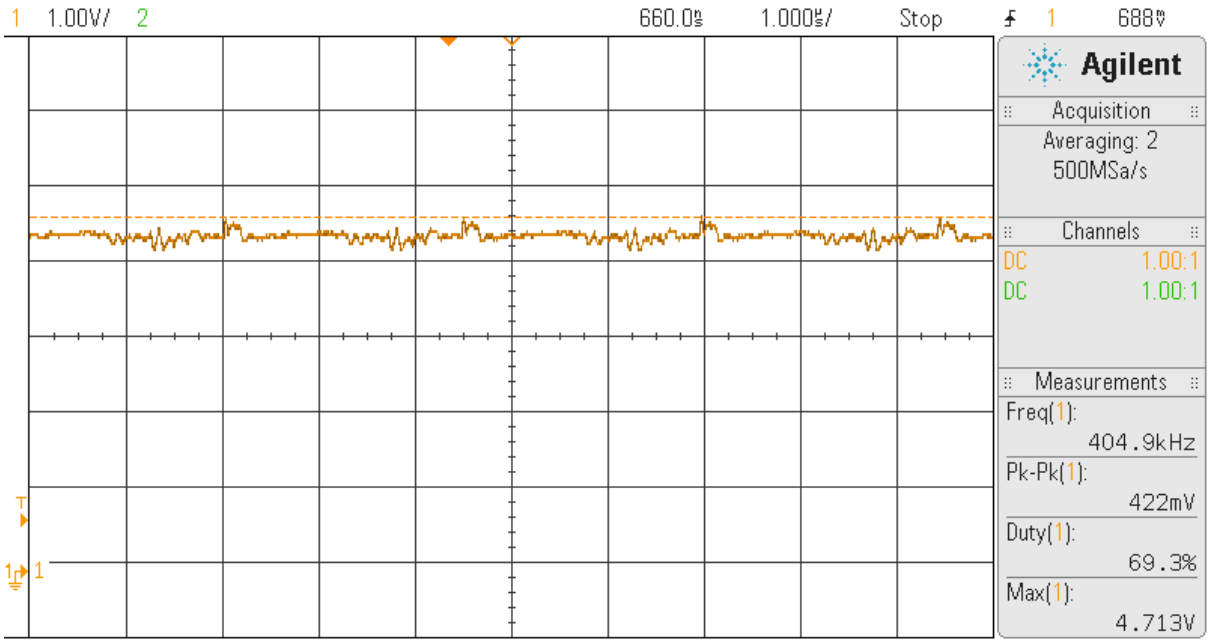


Figure 17-14: Hardware Testing, Primary BS2 Pin, Pin 22, 30V Case

I. Analysis of Senior Project Design

Project Title: EHFEM Buck-Boost DC/DC Converter Using LT3791-1 with Input Protection System

Student's Name: Sheldon Chu, Byung-Jae David Yoo **Student Signatures:**

Advisor's Name: David Braun **Advisor's Initials:** **Date:**

Summary of Functional Requirements

Cal Poly's Energy Harvesting from Exercise Machines (EHFEM) project comprises of multiple subprojects seeking to effectively create a sustainable energy source through harvesting electrical energy generated from physical exercise machines. This project designs and implements a Buck-Boost DC-DC converter using a LT3791-1 4-Switch Buck-Boost Controller, replacing the previous SEPIC design. The DC-DC converter must operate within limits set by the maximum input range of the LT3791-1 controller. An input protection system prevents inputs higher than rated values, which may adversely damage the Buck-Boost DC-DC converter. These inputs include overvoltage transients, average voltage, and current output by the Precor EFX 561i elliptical generator. Therefore, integrating a modified version of Ryan Turner and Zack Weiler's DC-DC Converter Input Protection System prevents system damage if generator outputs stray beyond safe operational range. This system also provides charge accumulation protection generated during an open-load phase during start-up of the Enphase M175 Micro-Inverter. Additionally, the DC-DC converter's output must provide a voltage within the micro-inverter's input voltage range to apply $240V_{RMS}$ power back to the electrical grid.

Primary Constraints

The EHFEM project's existing components, namely the Precor EFX 561i elliptical's generator and Enphase M175 Micro-Inverter place limitations on the buck-boost DC-DC converter design. Ryan Turner and Zack Weiler's DC-DC Converter Input Protection System project details output characteristics of the elliptical's generator. on average, the elliptical generates 6V to 65V and 0.6A to 6.5A through minimum and maximum exercise resistance levels (1-20) and speeds (100 SPM - 230+ SPM). Overvoltage transient measure up to 150V, generating current spikes of up to 15A. Additionally, the Enphase M175 Micro-Inverter accepts a maximum input current of 8A with 36V as the nominal input voltage to provide an output of $240V_{RMS}$. Therefore, up to 288W of power feeds to the inverter. Further limitations spawn from the LT3791-1 IC's characteristics. for example, the LT3791-1's input voltage may range from 4.7V to 60V.

In summary, the generator and inverter place various electrical limitations upon the designed system. The input protection system must not only protect the DC-DC converter from overvoltage transients of up to 150V, but must also limit its maximum input voltage to 60V. The output of the DC-DC converter must also nominally output 36V with a maximum current output of 8A to the inverter.

Additionally, the final physical design must fit into the Precor EFX 561i elliptical's enclosure. The equivalent input impedance of the design must also equal 10Ω to preserve the physical exercise experience of the user.

Simulating a working design proved challenging and added more project difficult than expected. Specifically, no suitable approach limited simulated input power to the

converter. Simulations using ideal voltage source inputs indicated high input power transients due to MOSFET switching. Simulation design alterations attempted input power problem amendment, including adding a series input parasitic resistance, snubber cells, and a declining input resistance. Although these additional components did mitigate input power transients, they did not limit input power to the system.

Furthermore, selecting parts based on LT3791-1's datasheet equations and parameters proved challenging. Ambiguous datasheet parameters produced confusion when selecting inductor and current sense resistor sizes. Specifically, certain variables such as %Ripple remained ambiguous within LT3791-1's datasheet. Datasheet ambiguity required exterior research to select proper components.

Additionally, selecting improper MOSFETs generated numerous problems. Simulations indicated high current and power dissipation during MOSFET switching. Various snubber circuits were considered and tested to reduce the excessive power dissipated on MOSFETs. However, results concluded a new MOSFET with better parameters proved a better and easier option.

The newly selected MOSFETs, however, did not have a public spice model to accurately simulate its behavior. A model was constructed based upon a preliminary datasheet but with questionable reliability and accuracy. Every simulation results held potential abnormalities with unknown variables. MOSFETs did not switch correctly during the hardware testing. Characterization of these MOSFETs was conducted but there were too many variables to deduce the problem's root cause.

Designing the PCB layout was especially difficult due to lack of PCB design knowledge and experience. The PCB design underwent multiple revisions. A majority of signal traces and power traces were redrawn multiple times due to lacking understanding of the relationship between high frequency traces and return ground path. A 4-layer PCB layout was selected instead of 2-layer board to reduce the difficulty of tracing paths. Drawing proper trace thickness to handle high current was exceptionally difficult due to lack of space.

Economic

Human Capital

Production requires the time of skilled laborers to assemble and solder components onto a PCB. Each component involved also requires the time of skilled workers to be designed, manufactured, and shipped by the various companies that supply them. Furthermore, the assembled product requires the time of skilled laborers to install the product into the enclosure of the elliptical machine.

Financial Capital

The production process requires the necessary monetary funds to pay skilled workers to assemble, transport, and install the system into the elliptical machines. The product's production also requires the necessary monetary funds to buy the components necessary for the design. Systems modified with the final project reduce the operating electricity costs of exercise facilities during and after its fulfillment of its zero cost lifecycle.

Manufactured or Real Capital

The product requires numerous components generated by the efforts of various companies and individuals including ICs, resistors, capacitors, inductors, PCBs, solder, heat sinks, and shipping materials.

Natural Capital

The production of this project requires the use of Earth's resources in the production of its components. This includes rare earth metals like silicon, copper, aluminum, oil (plastic and gasoline/diesel), and wood (cardboard). Harvesting and producing these resources result in toxic emissions and numerous other byproducts of industrial production that negatively impact Earth.

• When and where do costs and benefits accrue throughout the project's lifecycle?

Costs accrue during the production of the finalized product. Such costs include the cost to manufacture each component and to ship the component(s) to the place of final assembly, in addition to the cost of final assembly, shipping, and installation. Cost benefits start to accrue during the operational use of the elliptical machines outfitted with the EHFEM system which feeds generated electricity back to the power grid and reduces the energy bought from power companies.

• What inputs does the experiment require? How much does the project cost? Who pays?

This experiment requires various component inputs for the design and testing of the system, including the components required for the initial design and final design. This

project's cost estimates $3866.67 as projected in Table D1. Cal Poly: San Luis Obispo pays the final cost for the project in order to outfit existing Precor EFX 561i elliptical trainers with energy generating systems. by doing so, it cuts operational electrical costs of its recreational center. Table A displays estimated project costs.

Table A: Estimated Project Cost

<table>
<tr><th>Costs</th><th>Optimistic</th><th>Most Likely</th><th>Pessimistic</th><th>Estimated</th></tr>
<tr><td>Total Component (Fixed)
<table>
<tr><th>Component</th><th>Cost</th></tr>
<tr><td>LT 3791</td><td>$ 22.50</td></tr>
<tr><td>LT 4356</td><td>$ 8.49</td></tr>
<tr><td>Input Protection System and
DC-DC converter circuit components</td><td>$ 70-90</td></tr>
<tr><td>Converter PCB</td><td>$ 100-300</td></tr>
<tr><td>Protection Circuit PCB</td><td>$ 5-80</td></tr>
<tr><td>Controllers for LT 3791</td><td>$ 10-20</td></tr>
<tr><td>Total Component Cost</td><td>Min = $ 215.99
Max = $ 520.56</td></tr>
</table></td><td>$215.00</td><td>$300</td><td>$520.00</td><td>$272.50</td></tr>
<tr><td>Total Labor (Variable)
$16 per hour</td><td>$2,400.00
150 Hrs</td><td>$3,200.00
200 Hrs</td><td>$6,400.00
400 Hrs</td><td>$3600.00</td></tr>
<tr><td>Total Cost</td><td></td><td></td><td></td><td>$3,872.50</td></tr>
</table>

Table B: Final Project Cost

Type	Schematic Name	Value	Component	$/unit	QTY	Sum	P/N	Description	Company
Inductor	Inductor	22u	Inductor	$7.83	2	$15.66	AIRD-03-270K	INDUCTOR PWR DRUM CORE 27UH	Abracon
Resistors	RLSENSE	12m	R1	$1.17	2	$2.34	ERJ-8BWFR012V	RES 0.012 OHM 1W 1% 1206 SMD	Panasonic
	REN1	200k	R2	$0.10	2	$0.20	RC2012F204CS	RES 200K OHM 1/8W 1% 0805	Samsung
	REN2	62k	R3	$0.10	2	$0.20	ERJ-6ENF6202V	RES 62K OHM 1/8W 1% 0805 SMD	Panasonic
	Rcomp	51	R4	$0.10	2	$0.20	ERJ-6ENF51R0V	RES 51 OHM 1/8W 1% 0805 SMD	Panasonic
	ROVLO1	200k	R5	$0.10	2	$0.20	ERJ-6ENF2003V	RES 200K OHM 1/8W 1% 0805 SMD	Panasonic
	ROVLO2	12.4k	R6	$0.10	2	$0.20	ERJ-6ENF1242V	RES 12.4K OHM 1/8W 1% 0805 SMD	Panasonic
	RT	59k	R7	$0.10	2	$0.20	ERJ-6ENF5902V	RES 59K OHM 1/8W 1% 0805 SMD	Panasonic
	Rsense	1.5m	R8	$1.11	2	$2.22	ERJ-M1WTF1M5U	RES 0.0015 OHM 1W 1% 2512 SMD	Panasonic
	RFB1	196k	R9	$0.10	2	$0.20	ERJ-6ENF1963V	RES 196K OHM 1/8W 1% 0805 SMD	Panasonic
	RFB2	6.81k	R10	$0.10	2	$0.20	ERJ-6ENF6811V	RES 6.81K OHM 1/8W 1% 0805 SMD	Panasonic
	ROUT	27m	R11	$1.17	2	$2.34	ERJ-8BWFR027V	RES 0.027 OHM 1W 1% 1206 SMD	Panasonic
	RSHORT	200k	R12	$0.10	2	$0.20	ERJ-6ENF2003V	RES 200K OHM 1/8W 1% 0805 SMD	Panasonic
	RC/10	100k	R13	$0.10	2	$0.20	ERJ-6ENF1003V	RES 100K OHM 1/8W 1% 0805 SMD	Panasonic
	RSS	100k	R14	$0.10	2	$0.20	ERJ-6ENF1003V	RES 100K OHM 1/8W 1% 0805 SMD	Panasonic
	RVC	3k	R15	$0.10	2	$0.20	ERJ-6ENF3001V	RES 3K OHM 1/8W 1% 0805 SMD	Panasonic
Switches			Q1-Q8	$4.03	8	$32.20	IXTH180N10T	MOSFET N-CH 100V 180A TO-247	IXYS
Capacitors	CSS	33nF	C1	$0.24	2	$0.48	C0603C333K8RACTU	CAP CER 0.033UF 10V 10% X7R 0603	Kemet
	CVC	33nF	C2	$0.24	2	$0.48	C0603C333K8RACTU	CAP CER 0.033UF 10V 10% X7R 0603	Kemet
	Ccomp	470n	C3	$0.41	2	$0.82	C0603C474K8RACTU	CAP CER 0.47UF 10V 10% X7R 0603	Kemet
	CINTVCC	4.7u	C4	$1.40	2	$2.80	C3225X7S2A475M200AB	CAP CER 4.7UF 100V 20% X7S 1210	TDK
	CVREF	0.1uF	C5	$0.10	2	$0.20	C1608X7R1E104K080AA	CAP CER 0.1UF 25V 10% X7R 0603	TDK
	CBS	0.1uF	C6 and C7	$0.10	4	$0.40	C1608X7R1E104K080AA	CAP CER 0.1UF 25V 10% X7R 0603	TDK
	COUT	4.7u	COUT	$1.23	8	$9.84	C3225X7S2A475K200AB	CAP CER 4.7UF 100V 10% X7S 1210	TDK
	CIN	4.7u	CIN	$1.23	8	$9.84	C3225X7S2A475K200AB	CAP CER 4.7UF 100V 10% X7S 1210	TDK
Schottky	D1, D2		D1,D2,D5,D6	$0.44	4	$1.76	BAT46WJ,115	DIODE SCHOTKY 100V 0.25A SOD323F	NXP Semicond.
	D3, D4		D3,D4,D7,D8	$1.23	4	$4.92	MBR20100CTTU	DIODE SCHOTTKY 100V 10A TO220	Fairchild Semi

Controller	LT3791-1		Controller	$11.21	3	$33.63	LT3791IFE-1#PBF	IC REG CTRLR BUCK BST 38TSSOP	Linear Tech
Heat Sink				$3.09	8	$24.72	C247-025-1AE	HEATSINK FOR TO-247 WITH 1 CLIP	Ohmite
Header Pins				$0.13	18	$2.30	961102-6404-AR	CONN HEADER VERT SGL 2POS GOLD	3M
POSTS	RED			$4.05	4	$16.20	111-0702-001		Emerson
	BLACK			$4.05	6	$24.30	111-0703-001		Emerson
PCB	4-Layer		PCB	$32.67	2	$65.33			ExpressPCB
					TOTAL	**$255.19**			
					TAX	$275.60			

• How much does the project earn? Who profits?

The EHFEM project indirectly profits Cal Poly by reducing its operating electricity costs at its recreational center. The EHFEM projects to achieve a zero system lifecycle cost after 10 years of use as outline in Martin Kou's thesis [9]. The estimated profit per year of the EHFEM project of $39.26/year provided a nominal 100W generated from exercise at a power degradation of 0.5% at 12 hours per day for 41 weeks at $0.12 per kWh of electricity. Any electricity generated after the ten year period generates profit to Cal Poly with respect to the cost required to implement the EHFEM system.

• Timing

Products emerge after the final design of the product, in addition to the manufacturable final design of its individual components. The product final product has a lifecycle of approximately ten years to reach zero system lifecycle cost. Therefore, each component in the product must sustain proper operation for at least ten years without maintenance or replacement.

Figure A displays the original initial estimated development time of this project while Figure B displays actual project development time.

Figure A: Initial Estimated Project Plan Gantt Chart

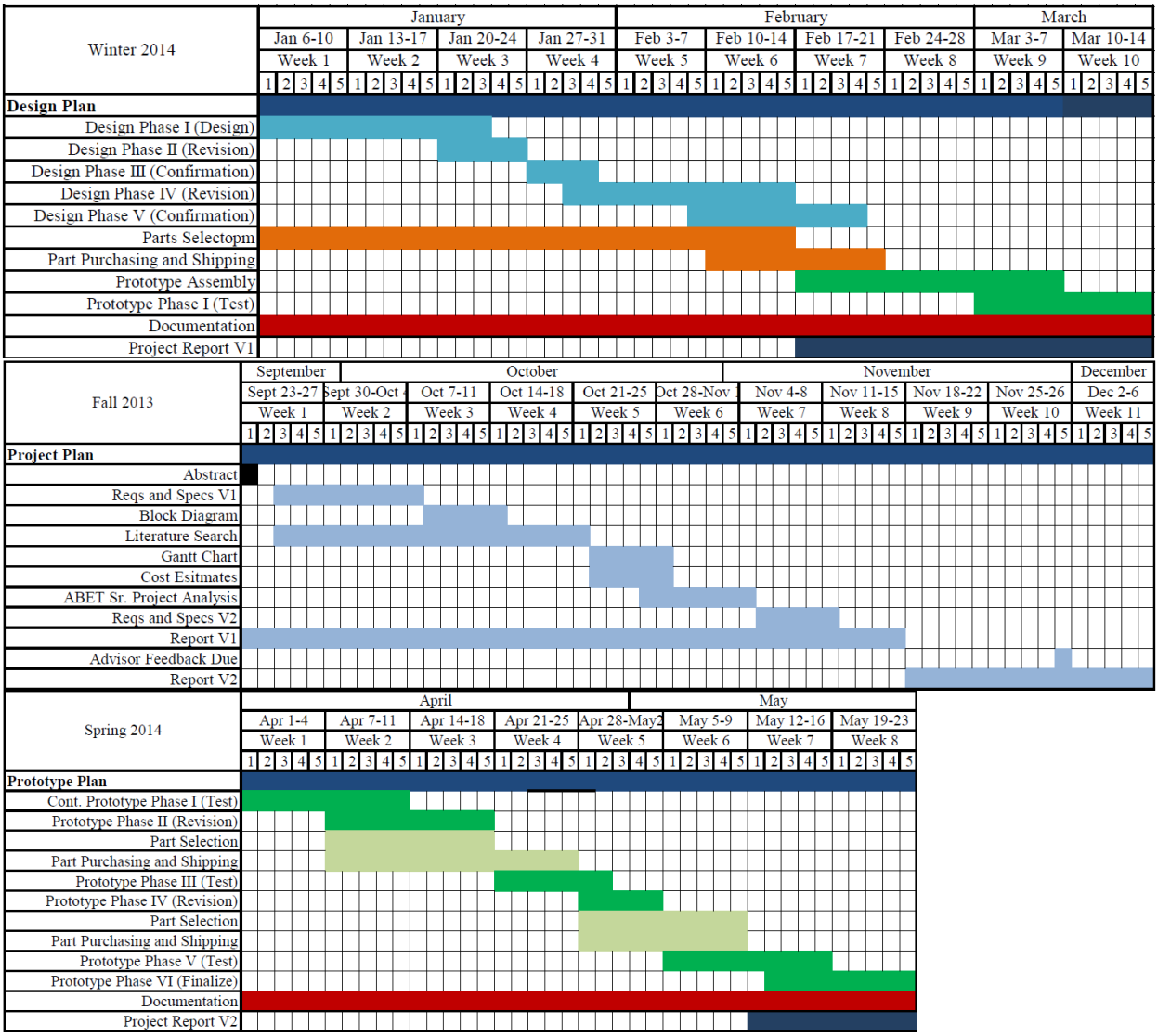
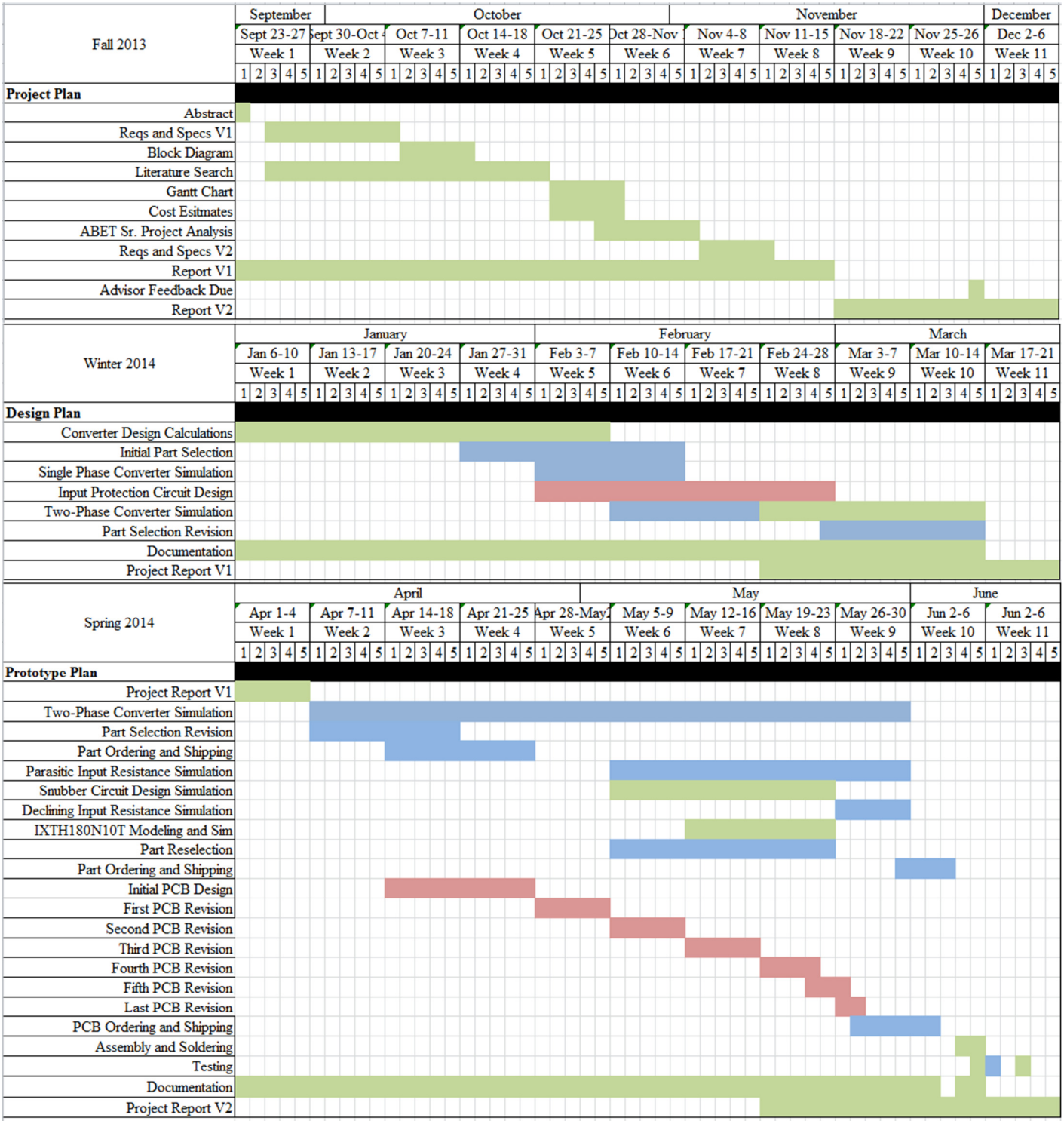


Figure B: Actual Project Plan Gantt Chart



Commercial Manufacture

This project considers devices sold primarily to middle and large sized recreational centers, not individual consumers. Considering a sale of 25 devices per recreational facility at a per-unit cost of $325.00 with an estimated manufacturing cost of $266.67, each facility generates $1458.25. These values do not take into account significant labor costs or taxes. Considering that an average of 20 facilities/year, or 500 units/year, purchase the product, total profit estimates to $29,165 per year. Theoretically, operation incurs no fees to the owner for the first ten years due to its design for a zero system lifecycle cost of 10 years. During the event of component failure, replacement parts should cost under 5% of the product cost, or $16.25. This value covers individual component costs outside of PCB printing.

Environmental

This project generates negative environmental impacts during its production. Such negative impacts include the generation of carbon dioxide, carbon monoxide, and other pollutants generated during manufacturing and shipping stages. Additionally, the components required by this product directly impacts earth's natural resources and ecosystem services as they require harvesting Earth's natural resources. Such resources include copper, aluminum, silicon, and the drilling of oil. Mining and drilling requires energy to purify and transport materials and produces industrial byproducts which harm surrounding ecosystems. Harvesting methods also produce environmentally harmful toxic byproducts. Furthermore, disposal of its components after failure or replacement may negatively affect the environment. Components selected in this design fulfill RoHS compliance to ensure minimal environmental impact upon their disposal based. This

project has a positive impact acts as a source of renewable energy, thereby reducing power plant emissions in a wider prospective. in doing so, this project positively impacts other species by reducing the effects of harmful or toxic emissions.

Manufacturability

Drawbacks of the scale of this project include difficulties in hand-soldering components to printed circuit boards. Inadvertent damage may occur during soldering process, especially to components such as SMT devices. Such devices require precision soldering using a magnifying glass. Such difficulties may result in the accumulation of damaged components. Additionally, the quality of testing equipment supplied by the Electrical Engineering department's laboratories constrains system testing quality. Testing equipment often limits digits of resolution. for example, if current measurements in µA are limited to mA due to equipment supporting only mA.

Sustainability

The system's designed lifespan of at least ten years provides 65,700 operating hours with no additional required maintenance. Therefore, no further natural resources are required for ten years by each unit, thereby minimizing environmental impact in the process of harvesting and disposal of resources. in the event of components failure, individual components may be desoldered and replaced instead of requiring the manufacture of a new unit, further reducing environmental impact. Further upgrades to the design of this project that would improve sustainability include minimizing its PCB footprint and minimizing power dissipation by components. Minimizing the projects PCB footprint decreases the amount of copper and plastic required by the project, thereby

decreasing its ecological footprint. Minimizing the PCB footprint may prove difficult as components vary in size.

Ethical

Based on the Utilitarian ethical framework, this project benefits a wide range of groups by generating renewable energy with zero emission as waste or byproduct. This results in an eco-friendly source of energy generation, thereby decreasing the overall environmental impact generated from non-renewable energy sources to produce similar quantities of energy. Although often seen in a positive light, green-energy may make some users feel uncomfortable with paying the same rates for gym memberships at gyms outfitted with EHFEM machines than those without. Users may feel disgruntled knowing that their fitness center pays less for their utilities but charging users the same amount in comparison to competitors without EHFEM machines. Additionally, users may feel disgruntled if left uninformed of EHFEM machines installed for solely for the profit margin benefit of the fitness center.

Numbers 1, 3, 7, and 9 of the IEEE Code of Ethics [11] most apply to this project. The safety and wellbeing of the user and laborers manufacturing the device apply statements 1 and 9. All aspects of the project that may pose a danger to the public must be properly noted or remedied, whether mechanical or electrical hazards. Additionally, statements 3 and 7 apply to the design and manufacturing of the product. Proper claims regarding the function and safety of the product must be issued and proper acknowledgement of groups who have contributed to the EHFEM project. It's highly important to constructively criticize the development of the buck-boost DC-DC converter system promote an efficient and safe system.

Health and Safety

Overall, the implementation of the EHFEM system should not alter the user's exercise experience or safety. The design and use of this product requires mechanical input by a user to operate the elliptical machine. Proper exercise safety practices prevent physical injury to the user. Additionally, the EHFEM system generates electrical energy. Proper precautions or implementations must prevent electrical shock to the user. A user's safety should be maintained in the case water is spilled on the equipment. Accidental spillage of liquids onto the device must not jeopardize the safety of the user. Circuit components also dissipate heat during normal use, so proper implementation of heat dissipaters prevent component failure or physical harm to the user. Manufacturing and testing requires human labor to solder and test components. Soldering releases hazardous noxious fumes and involves using tools operating at high temperatures. Proper ventilation and equipment practices minimize hazards during the manufacturing process.

Social and Political

This project may generate positive public social interest in renewable energy sources as it demonstrates to Cal Poly's community that the university actively seeks ways to become a greener campus. Implementing the EHFEM project in the form of numerous elliptical machines, or other exercise machines, directly reduces Cal Poly's spending on energy over a period of time, which indirectly reduces the consumption of Earth's natural resources used to generate energy (i.e. coal, oil). The direct stakeholders of this project include Cal Poly. Its indirect stakeholders include power plants and power companies. Using elliptical machines modified using the EHFEM project equally benefits both stake holders as Cal Poly spends on electrical energy, correlating with less energy

demand from power plants. Cal Poly benefits more than power plants as Cal Poly pays less overall for electricity costs while the power not consumed from the power plant(s) is redirected and consumed elsewhere. Additionally, Cal Poly's presence and reputation as a green campus improves which may foster innovations in green energy-producing technologies in the future.

Development

The Monte-Carlo technique was learned to analyze circuit simulations taking into account component tolerance, temperature variations, and parasitic characteristics. Additionally, this project required learning to operate and design DC-DC converters and its protection system as designed by Turner and Weiler [2]. Furthermore, selection methods for proper heat sinking, MOSFET, and power inductor sizing were learned for low-power systems. Basic operational information about snubber circuits was also learned. This project also provided an opportunity to learn about PCB layout and design considerations as well as hands-on soldering experience.