Encryption on Microcontrollers

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Abstract

This project concentrates on the security of simple embedded systems that sends data wirelessly. For example, a WIFI home security camera. The algorithm, Advanced Security Standard (AES), is chosen since it is a common and efficient algorithm. The processor of a simple embedded system has limited processing power and some applications are real time, so reducing the usage of the processor and time efficiency are important. The goals are achieved by minimizing processor memory usage and iteration of AES.

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Introduction

An FPGA could be used to minimize processor memory usage. However, an FPGA holds an additional cost for the embedded system. FPGA can encrypt the data faster due to parallel computing. However, encryption would be the last stage of the processing and after that data is transferred through serial communication. Thus, time is not very critical here and performing AES inside a microprocessor is a better option. Secure communication with sensitive information is necessary for military and government institutions but also for business sectors and private individuals [1]. The Rijndael algorithm was chosen by National Institute of Standards and Technology (NIST) for the new Advanced Encryption Standard in conjunction with scalability, security, simplicity, and strength. It is an iterative, symmetric block cipher operating on 128-bit block sizes with key sizes of 128, 196, and 256 bits.

Background

The 21st century relies heavily on networked infrastructure. Steps must be taken to protect data from intruders. Data encryption has the ability to defend unauthorized use of data. However, cryptology has weaknesses such as security vulnerabilities such as sending encryption keys over networks. Another weakness was found in the Data Encryption Standard (DES) 56-bit key initially adopted in 1977. The Advanced Encryption Standard (AES) was designed in response to the weak and slow DES algorithm [2]. The design methodology was for resilience against known attacks (exhaustive key search, etc) and encryption speed on CPUs, while staying as simplistic as possible [3].

Design Module

Hardware	Software
Laptop	Advanced port terminal
Atmega328 microcontroller	C-code to implement the algorithm
USB cable	C-code to display data on the screen

Software flow diagram:



Figure 1: Traditional AES 128-bit Encryption Scheme

Traditional AES uses a repetitive encryption process to diffuse the data as shown in Figure 1. The input data will be passed through four types of stages: SubBytes, ShiftRows, MixColumns, and AddRoundKey [4].

Sub Bytes

The first stage, called Sub Bytes, is a non-linear byte substitution that acts on every byte of the state in isolation to produce a new byte value using anSbox substitution table shown in Figure 1. The corresponding replacement byte is found by matching the first nibble of an input byte to a look-up table row, and the second nibble for the look-up table column. This step helps avoid attacks based on algebraic properties.

State is represented as in Figure 2:

S _{0,0}	S _{0,1}	S _{0,2}	S _{0,3}
S _{1,0}	S _{1,1}	S _{1,2}	S _{1,3}
S _{2,0}	S _{2,1}	S _{2,2}	S _{2,3}
S _{3,0}	S _{3,1}	S _{3,2}	S _{3,3}

Figure 2: Example of the state

Figure 3 shows the Sbox of the. The first 4 bits in the byte (the first hexadecimal value, hence) individual the row, the last 4 bits individuate the column)

		х															
		0	1	2	3	4	5	6	7	8	9	a	Ъ	c	d	٠	f
	0	63	7c	77	7ь	£2	6Ъ	6f	c٥	30	01	67	2Ъ	fe	d 7	ab	76
	1	ca	82	c9	7 d	fa	59	47	f0	ad	d4	a2	af	9c	a4	72	c0
	2	Ъ7	fd	93	26	36	3f	f7	cc	34	a٥	65	fl	71	dß	31	15
	3	04	c7	23	c3	18	96	05	9a	07	12	80	•2	eb	27	ь2	75
	4	09	83	2c	la	1Ь	6e	Sa	a0	52	ЗЪ	d6	Ъ3	29	e3	2f	84
	5	53	dl	00	ed	20	fc	Ъ1	56	6a	cb	be	39	4a	4c	58	cf
	6	d0	of	aa	fb	43	4d	33	85	45	Ð	02	7f	50	3с	9f	a8
	7	51	a3	40	8f	92	9d	38	Ð	bc	b6	da	21	10	ff	ß	d2
x	8	cd	0c	13	ec	Sf	97	44	17	c4	a7	7e	3d	64	Sd	19	73
	9	60	81	4f	dc	22	2a	90	88	46	8	Ъ8	14	de	50	0Ъ	db
	a	•0	32	3a	0a	49	06	24	Se	c2	d3	ac	62	91	95	e 4	79
	ь	e 7	c8	37	6d	8d	d5	4e	a9	6c	56	f 4	93	65	7a	ae	08
	с	ba	78	25	2e	lc	a6	Ъ4	сб	e 8	dd	74	lf	4 b	bd	8 b	8a
	d	70	3e	65	66	48	03	£6	0e	61	35	57	Ъ9	86	cl	1d	9e
	٠	el	fS	98	11	69	d9	Se	94	9Ъ	le	87	•9	ce	55	28	df
	f	8c	al	89	0d	bf	e6	42	68	41	99	2 d	Of	ъо	54	ьь	16

Figure 3: Sbox Values for all 256 Combinations in Hexadecimal Format

An array with all 256 hexadecimal values in C code:

uint8_t s[256] = {

0x63, 0x7C, 0x77, 0x7B, 0xF2, 0x6B, 0x6F, 0xC5, 0x30, 0x01, 0x67, 0x2B, 0xFE, 0xD7, 0xAB, 0x76, 0xCA, 0x82, 0xC9, 0x7D, 0xFA, 0x59, 0x47, 0xF0, 0xAD, 0xD4, 0xA2, 0xAF, 0x9C, 0xA4, 0x72, 0xC0, 0xB7, 0xFD, 0x93, 0x26, 0x36, 0x3F, 0xF7, 0xCC, 0x34, 0xA5, 0xE5, 0xF1, 0x71, 0xD8, 0x31, 0x15, 0x04, 0xC7, 0x23, 0xC3, 0x18, 0x96, 0x05, 0x9A, 0x07, 0x12, 0x80, 0xE2, 0xEB, 0x27, 0xB2, 0x75, 0x09, 0x83, 0x2C, 0x1A, 0x1B, 0x6E, 0x5A, 0xA0, 0x52, 0x3B, 0xD6, 0xB3, 0x29, 0xE3, 0x2F, 0x84, 0x53, 0xD1, 0x00, 0xED, 0x20, 0xFC, 0xB1, 0x5B, 0x6A, 0xCB, 0xBE, 0x39, 0x4A, 0x4C, 0x58, 0xCF, 0xD0, 0xEF, 0xAA, 0xFB, 0x43, 0x4D, 0x33, 0x85, 0x45, 0xF9, 0x02, 0x7F, 0x50, 0x3C, 0x9F, 0xA8, 0x51, 0xA3, 0x40, 0x8F, 0x92, 0x9D, 0x38, 0xF5, 0xBC, 0xB6, 0xDA, 0x21, 0x10, 0xFF, 0xF3, 0xD2, 0xCD, 0x0C, 0x13, 0xEC, 0x5F, 0x97, 0x44, 0x17, 0xC4, 0xA7, 0x7E, 0x3D, 0x64, 0x5D, 0x19, 0x73, 0x60, 0x81, 0x4F, 0xDC, 0x22, 0x2A, 0x90, 0x88, 0x46, 0xEE, 0xB8, 0x14, 0xDE, 0x5E, 0x0B, 0xDB, 0xE0, 0x32, 0x3A, 0x0A, 0x49, 0x06, 0x24, 0x5C, 0xC2, 0xD3, 0xAC, 0x62, 0x91, 0x95, 0xE4, 0x79, 0xE7, 0xC8, 0x37, 0x6D, 0x8D, 0xD5, 0x4E, 0xA9, 0x6C, 0x56, 0xF4, 0xEA, 0x65, 0x7A, 0xAE, 0x08, 0xBA, 0x78, 0x25, 0x2E, 0x1C, 0xA6, 0xB4, 0xC6, 0xE8, 0xDD, 0x74, 0x1F, 0x4B, 0xBD, 0x8B, 0x8A, 0x70, 0x3E, 0xB5, 0x66, 0x48, 0x03, 0xF6, 0x0E, 0x61, 0x35, 0x57, 0xB9, 0x86, 0xC1, 0x1D, 0x9E, 0xE1, 0xF8, 0x98, 0x11, 0x69, 0xD9, 0x8E, 0x94, 0x9B, 0x1E, 0x87, 0xE9, 0xCE, 0x55, 0x28, 0xDF, 0x8C, 0xA1, 0x89, 0x0D, 0xBF, 0xE6, 0x42, 0x68, 0x41, 0x99, 0x2D, 0x0F, 0xB0, 0x54, 0xBB, 0x16 };

Shift Rows

The second technique, Shift Rows, circular left shift a number of bytes equal to the row number. Figure 4 illustrates the process of shift rows. Sample code 1 shows the coded process.

S _{0,0}	S _{0,1}	S _{0,2}	S _{0,3}		S _{0,0}	S _{0,1}	S _{0,2}	S _{0,3}	
S _{1,0}	S _{1,1}	S _{1,2}	S _{1,3}		S _{1,1}	S _{1,2}	S _{1,3}	S _{1,0}	
S _{2,0}	S _{2,1}	S _{2,2}	S _{2,3}		S _{2,2}	S _{2,3}	S _{2,0}	S _{2,1}	
S _{3,0}	S _{3,1}	S _{3,2}	S _{3,3}		S _{3,3}	S _{3,0}	S _{3,1}	S _{3,2}	

Figure 4: Shift row of the State

C code:



Mix Columns

The third, Mix Columns, takes a column of data, multiplies it by a matrix, and stores the resulting column of data as shown in Figure 5. Each column of State is replaced by another column obtained by multiplying that column with a matrix in a particular field. The "mixing" helps diffuse the data. Sample code 2 shows the coded mixed columns.



Figure 5: example of mix columns

C code:

```
//mix column
if(round cnt<9){</pre>
int column, row, element;
for(column =0; column <4; column++) {</pre>
for(row =0; row <4; row++) {</pre>
for(element =0; element <4; element ++) {</pre>
*(d temp+element)=((*(state temp+element+4*column)<</pre>
((*(column val+element+4*row)>>1)&0x01))*
((*(column val+element+4*row)>>1) &0x01))
^(((*(state temp+element+4*column)>>7)&
(0x01)&(*(column val+element+4*row)>>1))*(0x1B))
^(((*(column val+element+4*row))&(0x01))*
(*(state temp+element+4*column));
}
*(state+row+column*4)=(*(d temp))^(*(d temp+1))^
(*(d temp+2))^(*(d temp+3))^(*(cypher+row+column*4));
}
}
```

Sample code 2: Mix Columns

Add Round Key

The last step, called Add Round Key, performs an XOR operation of the data with corresponding values in the Round Key. Each block of input data is passed through the "main round" nine times for 128-bit encryption. The cipher key is user generated and, in conjunction with the Rijndael key schedule, generates the round keys. This process is shown in Figure 6 and coded in Sample code 3 (adding key) and 4 (generating key).



Figure 6: The process of Add Round Key

C code:

```
//add initial round key
voidadd_initial_rkey(uint8_t *state, uint8_t *cypher){
inti;
for(i=0;i<16;i++){
*(state+i)=*(state+i)^*(cypher+i);
}
}</pre>
```

Sample code 3: Adding round key

```
voidrkey_gen(uint8_t *cypher, uint8_t *s, uint8 t *Rcon,
uint8_t round_cnt) {
int k, i;
for(k =0; k <16; k++) {</pre>
if(k <4){
if(k ==3){
*(d temp+k)=(*(cypher+k))^(*(s+(*(cypher+12))))^(0x00);
}
elseif(k ===0) {
*(d temp+k)=(*(cypher+k))^(*(s+(*(cypher+k+13))))^
(*(Rcon+round cnt));
}
else{
*(d temp+k)=(*(cypher+k))^(*(s+(*(cypher+k+13))))^
(0x00);
}
}
else{
(d_temp+k) = (*(d_temp+k-4))^{(*(cypher+k))};
}
}
for(i=0;i<16;i++) {</pre>
*(cypher+i)=*(d temp+i);
}
}
```

Sample code 4: Round key generator

AES Mix-Columns Transformation calculation



Figure 7: example matrix

 $r1 = \{01.d4\} + \{02.bf\} + \{03.5d\} + \{01.30\}$

1. {02.bf}

 $\{bf\} . \{02\} = 1011 \ 1111 << 1$

= 0111 1110 XOR 0001 1011

 $= 0110\ 0101$

2. {03.5d}

 $\{5d\}$. $\{03\} = \{0101 \ 1101 \ . \ 02\} \ XOR \ \{ \ 0101 \ 1101 \}$

= 1011 1010 XOR 0101 1101

 $= 1110\ 0111$

Therefore,

 $r1 = \{01.d4\} + \{02.bf\} + \{03.5d\} + \{01.30\}$

= 1101 0100 XOR 0110 0101 XOR 1110 0111 XOR 0011 0000

= 0110 0110

= 66 (in Hex)

[5]

Sample inputs and outputs

Figure 8 illustrates an example data and cypher. In Figure 9 and 10, the 10 rounds of processes are shown.



Figure 8: example Input of State and Cipher Key

	Round 2	Round 3	Round 4	Round 5	Round 6			
	49 45 75 77	ac ef 13 45	52 85 e3 f6	e1 e8 35 97	a1 78 10 4c			
After	de db 39 02	73 cl b5 23	50 a4 11 cf	4f fb c8 6c	63 4f e8 d5			
SubBytes	d2 96 87 53	cf 11 d6 5a	2f 5e c8 6a	d2 fb 96 ae	a8 29 3d 03			
	89 £1 1a 3b	7b df b5 b8	28 d7 07 94	9b ba 53 7c	fc df 23 fe			
	49 45 72 77	ac ef 13 45	52 85 e3 f6	e1 e8 35 97	a1 78 10 4c			
After	db 39 02 de	c1 b5 23 73	a4 11 cf 50	fb c8 6c 4f	4f e8 d5 63			
ShiftRows	87 53 d2 96	d6 5a cf 11	c8 6a 2f 5e	96 ae d2 fb	3d 03 a8 29			
	3b 89 f1 1a	b8 7b df b5	94 28 d7 07	7c 9b ba 53	fe fc df 23			
	58 1b db 1b	75 20 53 bb	0f 60 6f 5e	25 bd b6 4c	4b 2c 33 37			
After	4d 4b e7 6b	ec 0b c0 25	d6 31 c0 b3	dl 11 3a 4c	86 4a 9d d2			
tixColumns .	ca 5a ca b0	09 63 cf d0	da 38 10 13	a9 d1 33 c0	8d 89 f4 18			
	f1 ac a8 e5	93 33 7e de	a9 bf 6b 01	ad 68 8e b0	6d 80 e8 d8			
	£2 7a 59 73	3d 47 1e 6d	ef al b6 db	d4 7c ca 11	6d 11 db ca			
Round Key	e2 96 35 59	80 16 23 7a	44 52 71 Ob	d1 83 12 19	88 0b 19 00			
(indiana ready	95 b9 80 16	47 fe 7e 88	a5 5b 25 ad	ne 9d bi 15	a3 3e 86 93			
	£2 43 7a 7f	7d 3e 44 3b	41 7f 3b 00	£8 87 bc bc	7# fd 41 fd			
	aa 61 82 68	48 67 4d d6	e0 c8 d9 85	f1 c1 7c 5d	26 3d e8 fd			
After	8f dd d2 32	6c 1d e3 5f	92 63 b1 b8	00 92 c8 b5	0e 41 64 d2			
ddRoundKey	5f e3 4a 46	4e 9d b1 58	7f 63 35 be	6f 4c 8b d5	2e b7 72 8b			
	03 ef d2 9a	ee 0d 38 e7	e8 c0 50 01	55 ef 32 0c	17 7d a9 25			

Figure 9: Round 2, 3, 4, 5, and 6 of the process

	Round 7	Round 8	Round 9	Round 10	
	£7 27 95 54	be d4 0a da	87 12 40 97	e9 cb 3d af	
After	ab 83 43 b5	83 3b e1 64	ec 6e 4c 90	09 31 32 2e	
sanation	31 a9 40 3d f0 ff d3 3f	2c 86 d4 f2 c8 c0 4d fe	4a c3 46 e7 Bc d8 95 a6	89 07 7d 2e 72 5f 94 b5	
	£7 27 9b 54	be d4 0a da	87 12 4d 97	e9 cb 3d af	
After	83 43 b5 ab	3b e1 64 83	6e 4c 90 ec	31 32 2e 09	
ShiftRows	40 3d 31 89 3f f0 ff d3	1e c8 c0 4d	46 e7 48 c3 a6 8c d8 95	b5 72 51 94	
	14 46 27 34	00 b1 54 fa	47 40 a3 4c		
After	15 16 46 2a	51 c8 76 1b	37 d4 70 9f		
(1xColumns	bf ec d7 43	dl ff cd ea	ed a5 a6 bc		
	4e 5f 84 4e	ea b5 31 7£	ac 19 28 57	d0 c9 e1 b6	
Round Key	54 5£ a6 a6	d2 8d 2b 8d	77 fa d1 5c	14 00 32 53	
	0e f3 b2 41	21 d2 60 2f	E3 21 41 6e	a8 89 C8 46	
	5a 19 a3 7a	ea 04 65 85	eb 59 8b 1b	39 02 dc 19	
After	41 49 e0 8c	83 45 5d 96	40 2e a1 c3	25 dc 11 6a Cipherte	ext
AddRoundKey	42 de 19 04	5C 33 98 b0	10 84 07 42	84 09 85 0E	222

Figure 10: Round 7, 8, 9, and 10 of the process

Therefore, 32, 43 f6, a8, 88, 5a, 30, 8d, 31, 31, 98, a2, e0, 37, 07, 34 is the data, 2b, 7e, 15, 16, 28, ae, d2, a6, ab, f7, 15, 88, 09, cf, 4f, 3c is the cypher, and 39, 25, 84, 1d, 02, dc, 09, fb, dc, 11, 85, 97, 19, 6a, 0b, 32 is the expected ciphertext.

Display and testing results

A USART is used as an interface with a PC for display purposes. A USART (Universal Synchronous Asynchronous Receiver Transmitter) available on the AVR ATmega 328 is widely used for serial communication purposes. Sample code 5 shows the code used to initialize USART's send and receive features. C code of USART initialization, send, and receive:



Sample code 5: USART initialization, send, and receive

Advanced Serial Port Terminal 6 by Eltin	na Software - [COM3] 🛛 🛛 🗖 🗙
File Edit View Terminal Help	
: Ca 🔍 🛠 📑 💼 💼 👘 🧈 La 💀 😨 🐨 🖉	
Baudrate 9600 T Data bits 8 T Parity None T Stop bits 1 T Flow con	trol None 🔹 🕘
4 🔍 сомз	⊳ × ∢
Read data: 000000000: 45 6e 74 65 72 20 31 36 20 63 68 61 72 61 63 74 000000010: 65 72 73 3a 0a 0d 32 43 f6 a8 85 30 8d 31 31 000000020: 98 a2 e0 37 07 34 0a 0d 45 6e 74 65 72 20 31 36 000000030: 20 63 79 70 68 65 72 73 3a 0a 0d 2b 7e 15 16 28 000000040: ae d2 a6 ab f7 15 88 09 cf 4f 3c 0a 0d 45 6e 63 000000060: 72 79 <t< td=""><td>Enter 16 charact ers:2C痔山0?1 嗓?.4Enter 16 cyphers:+~(^??螼<enc rypted data:9% ?.? .厳.j.2</enc </td></t<>	Enter 16 charact ers:2C痔山0?1 嗓?.4Enter 16 cyphers:+~(^??螼 <enc rypted data:9% ?.? .厳.j.2</enc
Send	Ψ×
	v
☑ Global history	⊖String ●Hex ⊖Oct ⊖Bin ⊖Dec Send
	Loop this command sending every 1000 🚖 ms Start loop
👻 RTS 🔶 CTS 🔵 DTR 🛑 DSR 🛑 DCD 🗬 Ring 🛑 Break	Read: 110 Write: 32 Echo: off COM3: 9600,N,8,1

Figure 11: Advanced Serial Port terminal program

By using advanced port terminal 6, verification in terms of data, cypher, and final results are implemented. Figure 11 shows the final encrypted data which was 39, 25, 84, 1d, 02, dc, 09, fb, dc, 11, 85, 97, 19, 6a, 0b, 32

System integration



Figure 12: System integration of the project

In Figure 12, the system integration is shown. It consists of a laptop with Advanced serial port terminal program and an ATmega328 microcontroller.

Conclusion

The encryption was verified by using a terminal software to send data and cypher keys from a computer. With combination of the steps in the algorithm, the iteration and register usage were kept minimal. This project could be done by using an FPGA through VHDL. In the future, the use of USART in FPGA could be used to accomplish the same task. It is ready to be used as part of a large scale firmware to ensure data safety before transmitting. Overall, what was understood was the difference between using an FPGA and a microcontroller to implement the algorithm.

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