Fast Commutation of DC Current into a Capacitor Using Moving Contacts

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Abstract—**The article describes a method of fast commutation of DC current into a capacitor. Theoretical study is provided which enables evaluation of commutating DC current for the given contact velocity, capacitance and dielectric strength. It is concluded that a non-zero contact velocity at separation is required, and a corresponding switch design is proposed.**

Experimental results on a laboratory set up illustrate successful DC current commutation up to 400 A, with voltages rising to 1.3 kV. Further experiments demonstrate that parasitic parameters reduce the magnitude of the current that can be commutated.

A detailed non-linear PSCAD model and a linear model for the parasitic circuit are presented to enable prediction of the success of commutation. The model accuracy is confirmed with experimental tests.

The DC current commutation in the proposed method occurs 5-10 μs after the contact separation, which is much faster than with other methods employing moving contacts. A further benefit of the extremely short arcing is elimination of thermal issues on contacts, and possible simplified design of the mechanical switch.

***Index Terms*-- DC switchgear, HVDC protection, DC Circuit Breakers.**

I. Introduction

There has been renewed interest in DC circuits recently, because of the growing application of DC in transmission (e.g. HVDC and DC grids [1]) and distribution/collection systems. At low DC voltages (say below 1 kV) the arc voltage is comparable with system voltage and no commutation is usually required. At higher voltages, DC current commutation is required in all DC CB (Circuit Breakers) technologies [2],[3], and sometimes multiple commutations are needed. Solid state switches represent an elegant solution to interrupt DC current without any arcing and to provide adequate counter-voltage to commutate DC current into another circuit of practically any voltage magnitude [4]-[7]. Semiconductors are used for this purpose with all converters but if only occasional commutation is required (like with DC CBs), then the cost, losses and size of semiconductor valves are difficult to justify.

When moving contacts (mechanical switches) are used for DC commutation, arcing becomes inevitable. In passive DC CBs [8], [9] electrode separation creates arc with increasing voltage as the electrodes move apart. Increasing arc voltage creates equivalent negative resistance and it may take 20-50ms for the growing oscillations to cause current zero crossing and interruption of arc. The latest DC CBs based on moving contacts (active or current injection DC CBs) employ pre-charged capacitor which shortens the arcing time to 8-10 ms [10]. The arcing time in the range of tens of ms coupled with the high recovery voltages (over 100 kV) in these commutating circuits, lead to high energy dissipation and require special switches with arcing chambers and heavy electrodes. The high recovery voltages are result of insertion of surge arresters necessary to provide counter voltage in faulted DC circuit.

The arcing across a mechanical switch can be shorter if a semiconductor is placed in parallel [11], however semiconductor valve should be rated for full DC voltage.

The commutation of large DC currents between two DC busses in future DC substations has been extensively analyzed recently [12]. In this case DC CB are not necessary and DC disconnectors would be sufficient since recovery voltage is low (below 100 V) and load currents are moderate (1-2 kA). However, arcing is also expected in the time frame of 10 ms.

The commutation of DC current into a capacitor has been studied in the early DC CB designs [8] and [9], since it provides gradual and well defined recovery voltage which reduces occurrence of re-striking. SF_6 breaker commutates DC current into a capacitor in [8], but it has low opening speed and requires another switch to insert capacitor after 10-20 ms of arcing when contacts achieve adequate separation distance. With air-blast breaker [9] an inductor is inserted in the commutating circuit to shape LC oscillation, and arcing of 10-20 ms is also present. The DC current commutation into a capacitor using semiconductor switches is also used in the recent DC CB [6].

Recent research in [13] proposes series LC DC CB which commutates 130 A current into a capacitor, but commutation is not analyzed and parasitic parameters are neglected.

The high-speed mechanical switches with Thomson coil actuators have been known for many years [14],[15], but only recently they have been developed to commercial products with very impressive operating speeds. The GIS 320 kV disconnector operates in 2 ms [16] and has been employed in the DC CB in [4]. The vacuum disconnector of 40 kV operates in 2 ms [17] and has been employed in DC CB in [5]. A similar 120 kV disconnector is used in DC CB [6]. These fast disconnectors exclusively open at zero currents.

This research studies in depth DC current commutation into a capacitor. Fast disconnector switch with specific design features will be used. The aim is to reduce commutation time and to reduce or eliminate arcing. Analytical methods will develop theoretical basis for the commutation process, while non-linear simulation provides a more accurate model. The study is supported with substantial experimental results on a laboratory hardware of around 400-500 A DC current.

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II. FAST DC CURRENT COMMUTATION INTO A CAPACITOR

A. Circuit description

The circuit of interest is shown in Fig. 1, which resembles the study in [13]. Switch S_1 is of mechanical design (disconnector), which is initially closed and takes full current i_{dc}. The challenge is to understand the conditions for current commutation to capacitor when S_1 opens and in particular:

- Will dielectric breakdown and arcing across S_1 contacts occur and for how long?
- What is the required switch topology?
- What magnitude of current i_{dc} can be commutated?
- What would be the required capacitance Cs?

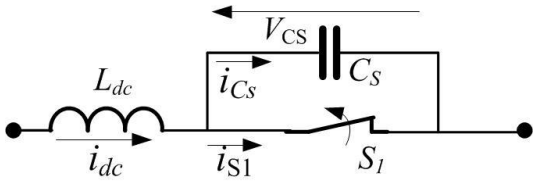


Fig. 1. DC current commutation circuit of interest.

B. Theoretical conditions for ideal circuit

It is assumed that the distance between electrodes of S_1 is z which is in the range $0<z<z_{max}$ while contacts are moving apart. z_{max} is the maximal electrode gap which occurs at time t_{max}. At any instant while contacts are moving apart, the contacts are capable of withstanding voltage v_b which is assumed:

$$v_b = zE_b, \quad 0 < z < z_{\max} \tag{1}$$

where E_b is the dielectric strength of insulating medium, which for air is E_{b_air}=3kV/mm, while for SF_6 it is E_{b_SF6} =7.5kV/mm (at 1bar). Dielectric strength is assumed constant since no thermal phenomena are considered, although impact of contact geometry is neglected. In order to avoid breakdown, the following critical dielectric condition should be satisfied:

$$zE_b > v_{cs}, \quad 0 < z < z_{\max} \tag{2}$$

where the capacitor voltage v_{Cs} is assumed identical to the contact gap voltage (recovery voltage). In this section the circuit is assumed ideal, with no parasitic inductances.

It is also of interest to express derivative of contact distance:

$$v = \frac{dz}{dt}, \quad 0 < z < z_{\max}, \quad 0 < t < t_{\max} \tag{3}$$

where v is the contact velocity. The derivative of v_{Cs} is:

$$\frac{dv_{Cs}}{dt} = \frac{i_{Cs}}{C_s}, \quad 0 < t < t_{\max} \tag{4}$$

Replacing (3) and (4) into inequality (2):

$$E_b \int_0^{t_{\max}} v\,dt > \int_0^{t_{\max}} \left(\frac{dv_{Cs}}{dt}\right) dt, \quad 0 < t < t_{\max} \tag{5}$$

The above equation is valid for any final time t_{max} including the instant of contact separation (commutation) at t=0. Replacing t_{max}=0 in (5):

$$v_0\, E_b > \frac{I_0}{C_s}, \quad z = 0,\ t = 0 \tag{6}$$

where v_0 is the contact velocity at the separation instant and I_0 is the current magnitude at the separation instant.

Equation (6), is valid for ideal conditions, and it is observed that the conditions to commutate non-zero current I_0 are [13]:

- Contacts have non-zero velocity at separation v_0,
- There is a finite capacitance C_s across contacts.

C. Switch design

The commutating switch employed in [8][9], [12] and many commercial switchgear cannot satisfy (6). They have butt contacts with springs facilitating adequate closed contact force. These switches have zero contact velocity at z=0, and this results in very gradual contact gap increase in the initial period.

The condition of $v_0>0$ can be satisfied if switch S_1 has lateral contact overlap in closed state which is shown in a simplified diagram in Fig. 2. The disconnector in [14] and many conventional SF_6 switches have similar construction. The lateral overlap of contacts in closed state is denoted as OL and enables contacts to accelerate to a non-zero velocity before separation. The contact separation distance z is determined using the contact positions x_1 and x_2, as shown in Fig. 2:

$$z = x_1 + x_2 - OL \tag{7}$$

A high-speed switch will be commonly driven by a pair of TCs (Thomson coil), as shown in Fig. 2, which provide fast acceleration. By knowing dynamics of switch contacts and the repulsive force of Thomson coils, the velocity of contacts can be determined [7], including crucial velocity at separation v_0.

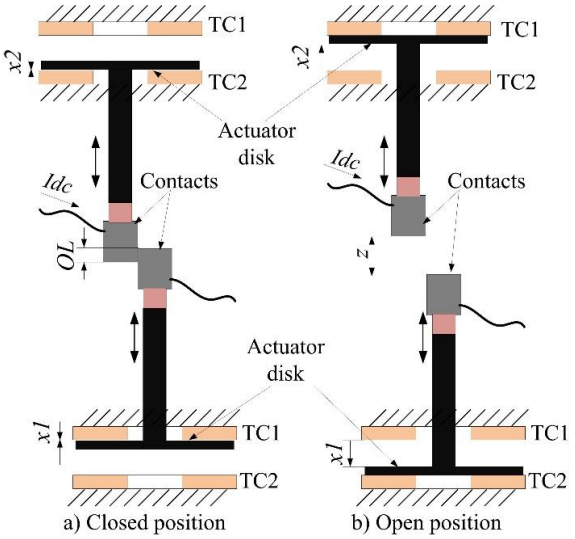


Fig. 2. Structure of a high-speed switch with lateral contact overlap.

D. Condition to avoid post-commutation re-strike

The equation (1) should be satisfied in every instant of the contact stroke, and at the maximum distance it becomes:

$$z_{\max} E_b > v_{Cs\max} \tag{8}$$

where the voltage v_{Csmax} can be determined from the arrester voltage. The instant when maximum voltage occurs will be dependent on the capacitance and current using (8):

$$z_{\max} E_b > \frac{1}{C_s}\int_0^{t_{\max}} i_{cs}\,dt, \quad 0 < t < t_{\max} \tag{9}$$

It is not intension of this article to analyze in depth the full trajectory of the contact movement and the capacitor current waveform. As the first approximation, an average current while contacts are moving I_{Csav} can be used for initial dimensioning:

$$z_{\max} E_b > \frac{I_{Csav}}{C_s} t_{\max} \tag{10}$$

III. Experimental Testing

A. Experimental circuit

Fig. 3 shows the schematic of the complete test circuit and it gives the test circuit parameters.

The DC CB testing rig at the Aberdeen HVDC laboratory has been used previously for testing hybrid and mechanical DC CBs, and it is described in [7] and [18]. It controls DC voltage to 0.9 kV - 1 kV, and supplies fault current of over 500 A.

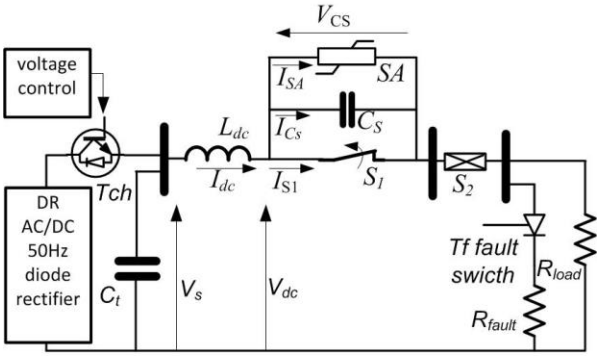
Fig. 4 shows the photograph of the commutating circuit (S_1, L_{dc} Cs and energy absorbers). The residual switch S_2 is a commercial AC circuit breaker (Kilovac) which is used to interrupt LC oscillations after the commutation. The capacitor bank is purposely located close to the commutating switch to reduce parasitic inductance.

Fig. 5 shows the fast disconnector S_1 separately. The high-speed disconnector operates in around 1-2ms with 3mm separation in air, and it is described in [19]. A theoretical E_b=3kV/mm may not be valid because of contact geometry and some bounce, and therefore a conservative peak stress of 1.2-1.5 kV is applied. Copper contacts of 20 mm width are used, while the closed-state overlap is OL=1.5 mm. Thomson coils are described in [19], and they have adjustable driver voltage which enables changes in the contact speed and opening time.

Fig. 6 shows the capacitor bank C_s (with four capacitors) and the energy absorbers. Bus bars are used to reduce inductance.

The measurements of variables are achieved as:

- The contact position x is measured using hall-effect sensors [19]. Contact separation z is estimated using (7) . Contact velocity is calculated by differentiating z.
- Currents i_{dc} and i_{s1} are measured using identical Agilent, 2 MHz, 500 A DC probes. It is not possible to measure i_{Cs} because of close location of capacitors. Arrester current i_{SA} is measured using a standard AC probe.
- Voltages are measured using TESTEC, 100MHz, differential probes.
- Data is captured at 2000 points on Agilent 200 MHz oscilloscope. The time is synchronized with S_1 trigger.



DR - Diode rectifier (1170V, 30A),
T_{ch} - Chopper IGBT, (1700V, 300A),
T_f - Fault thyristor, (1800V, 273A),
C_t - Storage Capacitor, (7080μF, 1200V),
L_{dc} - Series inductor, (0.0038H),
R_{load} - Load Resistor, (99Ω),
R_{fault} - Fault Resistor, (0.4Ω),
SA - Surge arrester (1200V, TDK 2xB60K275)
S_2 - Residual switch (AC CB, Kilovac EV200HAANA)
S_1 - Fast disconnector,
C_s - Commutating capacitor.

Fig. 3. Experimental test circuit.

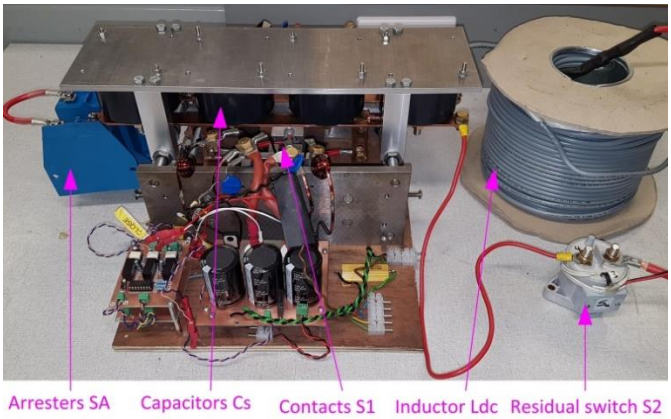


Fig. 4. Photograph of the experimental test circuit.

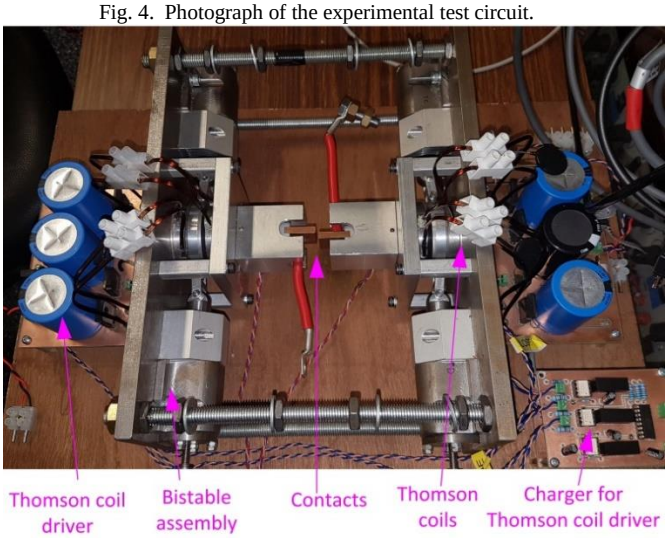


Fig. 5. Fast disconnector S_1.

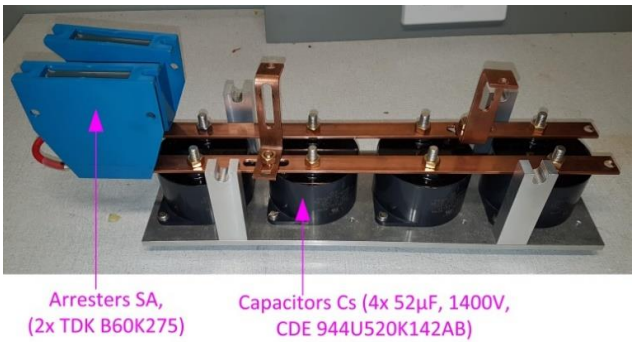


Fig. 6. Commutating capacitor *Cs* and arrester SA.

B. *Experimental results*

The first goal was to evaluate validity of equation (6). The following test plain is adopted:

1. For a fixed capacitance C_s and commutating current I_0 the responses are observed/recorded when S_1 opens. Note is taken if commutation is successful or if it fails.
2. Current I_0 is increased in a small step and test repeated. Current is further increased until commutation fails. This enables testing the impact of commutating current.
3. Capacitance is increased and steps 1-2 repeated.

A 52µF, 1400V capacitor is used as the basic unit and four test sets are performed with 52µF, 104µF, 156µF and 208µF (Fig. 6 shows all four capacitors in the circuit).

Fig. 7 shows commutation of 400A DC current, using 208µF capacitance. It is seen that 400 A current is transferred from the switch to the capacitor practically instantaneously. Voltage across switch raises to 1.3 kV in around 1 ms and no arcing is observed. Voltage magnitude is limited by arresters. It is seen that commutation occurs around 350 µs after the trip signal. Contacts are sliding for 350 µs (including a dead-time of 50-100 µs before they begin to move) while conducting current.

Fig. 8 shows the contact position measurements which is same for all tests. The distance between contacts z is calculated using measured position of each rod (shown as x_1 and x_2) and calibrated to indicate separation at the instant of voltage increase. It is seen that sepration occurs at around 350µs and that gap velocity at separation is v_0=2.5m/s.

Fig. 9 shows the summary of measurements for different capacitances. The failed commutation is marked with "x" which always occurs at somewhat larger current than the last successful commutation. Many tests have been performed with different capacitances and different currents. The results have been reliable and largely predictable. Experience shows that tests are repeatable with only a very small uncertainty (it fails for the same or very similar current magnitude for repeated tests). No re-striking is observed or stochastic phenomena.

Each time the failure occurs, a substantial arc for around 3-4 ms is observed and substantial contact damage occurs. Replacement of contacts has been necessary after each failure.

The curves "ideal model" in Fig. 9 is obtained using (6). It is seen that these curve are overly optimistic in predicting the maximum commutating current for the given parameters.

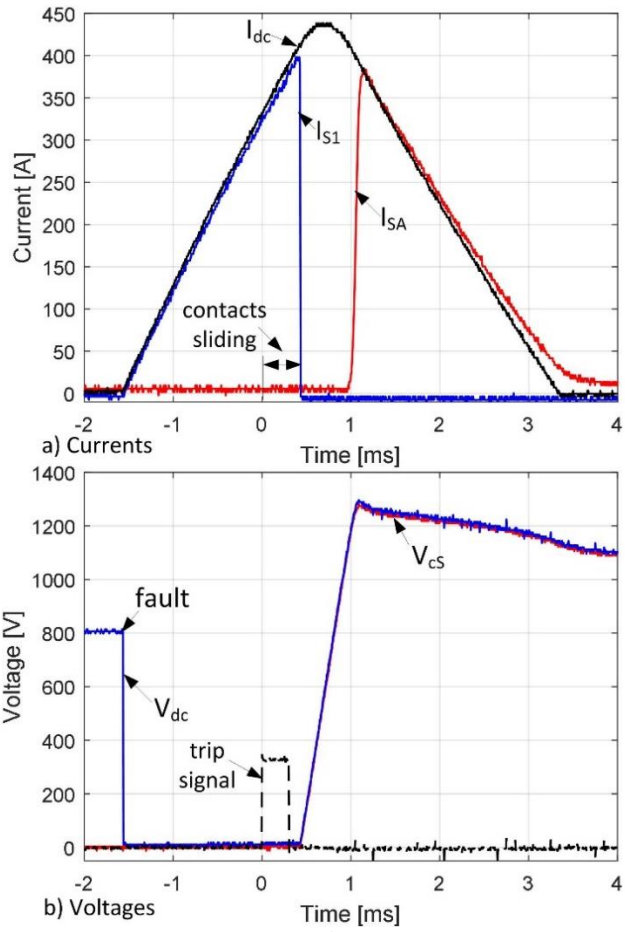


Fig. 7. Experimental measurement of 400A commutation (*Cs=208µF*).

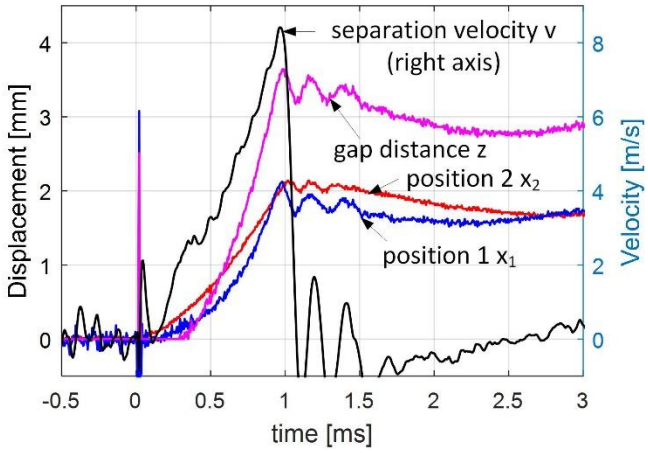


Fig. 8. Contact position, gap distance and velocity.

It is suspected that the commutation fails at lower-than-expected currents because of parasitic inductance and resistance in the commutating circuit. This can be confirmed by observing responses for failed commutation at 430 A with 208 µF, which are shown in Fig. 10. The switch current i_{S1} reduces rapidly but it fails to reach zero and continues to oscillate. The damped oscillations are of high frequency (over 20 kHz) and are caused by parasitics in the commutating circuit.

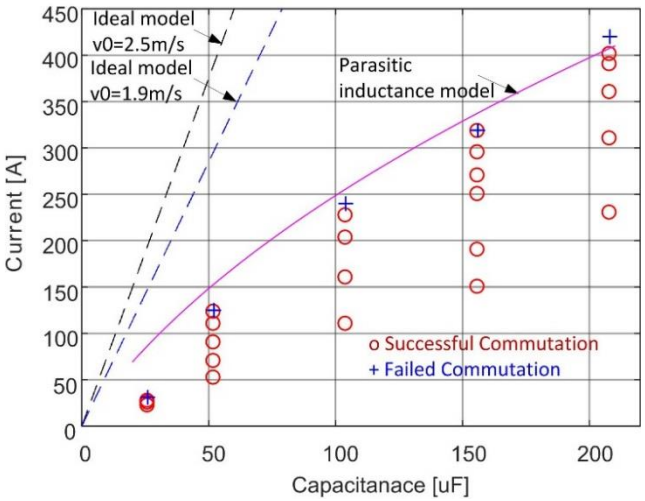


Fig. 9. Experimental measurements for different capacitances.

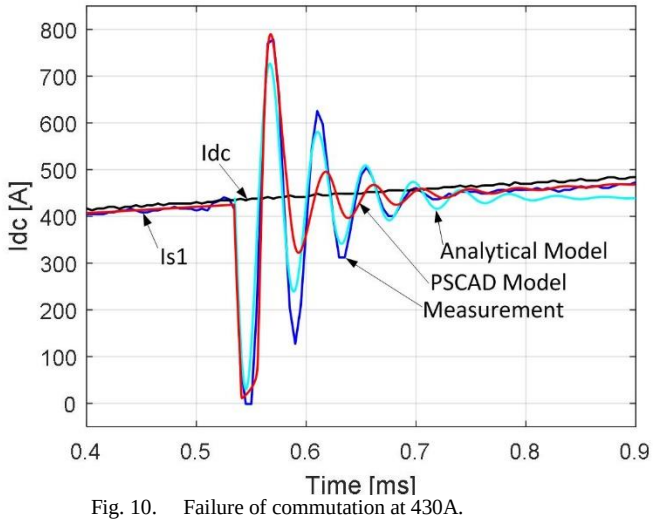


Fig. 10. Failure of commutation at 430A.

Fig. 10 also helps understanding the commutation process. The commutation is successful if the first peak of the parasitic oscillating current falls below zero, since this interrupts arc current. Therefore the gap medium conducts current (arcing time) only for the first ¼ of the parasitic oscillation. In the demonstrated successful commutation tests the arcing lasts for around 5-10 μs. This is 3 orders of magnitude shorter than arcing in the commercial mechanical DC CBs in [8]- [10]. Since arcing period is so short, minimal energy is dissipated and thermal phenomena are not important for the analysis (dielectric phenomena are crucial). The arcing of several μs is practically unmeasurable [12] and is not likely to cause any contact wearing. It is therefore believed that common disconnectors would be suitable switches for this commutation method. In practical terms, since arcing is so short, contacts can be lighter, and may operate at higher speeds.

A. *Tests with different contact velocity*

Contact velocity at separation instant v_0 is the key parameter in this design as it is seen in (6). Beside the illustrated tests with v_0=2.5m/s (opening in 1ms) further tests were also performed with lower speed of v_0=1.9m/s (opening in 2ms). At lower speed the "ideal model" curve has lower slope as shown in Fig. 9, but it is still above the current limits caused by parasitics, and therefore similar results are obtained. As it will be illustrated below, contact velocity has no influence on the parasitic circuit.

B. *Arc voltage tests without capacitor Cs*

The study in [12] concludes that the comparison of arc voltage and the voltage across parasitic elements determines success of DC current commutation. In order to measure te arc voltage, the commuating capacitor is removed from the circuit and measurements are taken at various current levels. Without capacitor, the arc voltage is more stable and enables understanding the electrode fall (intial arc voltage).

The measurements of arc voltage at 2 different currents (2 A and 180 A) are shown in Fig. 11. It is seen that this switch is unable to interrupt 1.3 A DC current without DC capacitor. It is also observed that the DC current drops from 2 A to 1.3 A while contacts are sliding, because of marginally increased resistance. This is the consequence of slight increase in contact resistance while contacts are sliding, however such drop is not noticable at higher currents. At low currents the electrode fall is larg (20-30 V) which explains the negative resistance slope and is consistent with measurements in [20].

In Fig. 11b) for 180 A current, and in general for all currents over 20 A, the arc voltage is around 15-18 V at separtion z=0. The arc voltage then slightly increases as gap distance incrases. These measuremest are in general agreement with results from [12] and [20].

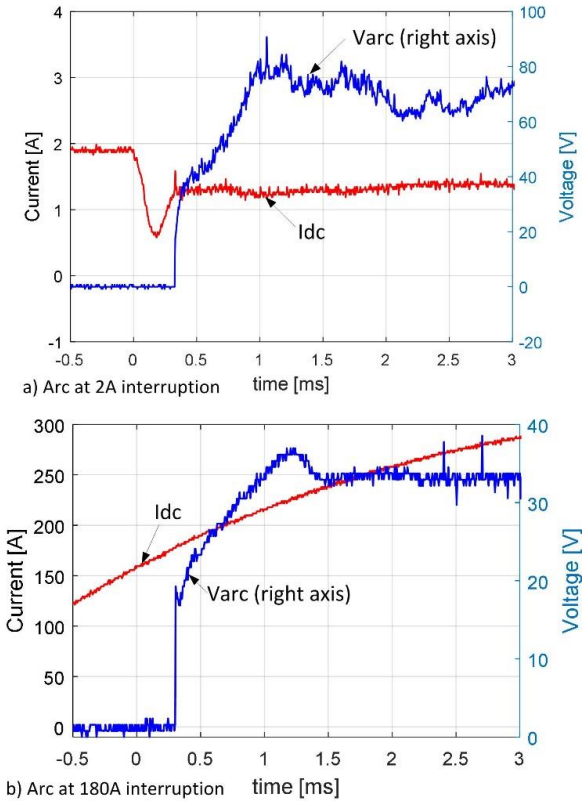


Fig. 11. Arc voltage experimental measurements.

IV. MODEL OF PARASITIC CIRCUIT

A. *Non-linear model in PSCAD*

A detailed circuit model including parasitics is developed in PSCAD, and Fig. 12 shows just the model of the commutating

circuit. PSCAD has a only a simple switch model, and the arcing switch is represented with two switches (S_{1a} and S_{1b}) and a non-linear resistor R_{arc}. Both switches are commanded to open on the trip signal, however they respond differently:

- S_{1a} is an ideal switch capable of opening only at zero current, which provides isolation when arc current reduces to zero.
- S_{1b} is an ideal switch capable of opening at any current, which will interrupt current immediately and insert R_{arc}.

Once S_{1b} opens, current i_{S1} falls, and if it reduces to zero S_{1a} opens and commutation is successful.

The value for R_{arc} is adjusted to match the experimental results as shown in Table I. Non-linear R_{arc} enables accurate representation of the arc voltage dependency on the current.

L_{p1} represents capacitor parasitic inductance, while L_{p2} represents the copper bus bar inductance. R_{p1} is the capacitor series resistance. At each topology (with different capacitance) the period and damping of the parasitic oscillating circuit are calculated using measurements of the oscillating response for the failed case (as in Fig. 10). Then, curve fitting is used to estimate the values for L_{p1} and L_{p2}, as shown in Fig. 13. The period of parasitic oscillations is also shown in Fig. 13, and can be used for estimation of the arcing duration (1/4 of the period).

The parameters of this model are shown in Table II. The testing of this model against experimental results is shown in Fig. 10, and it is seen that model accuracy is good.

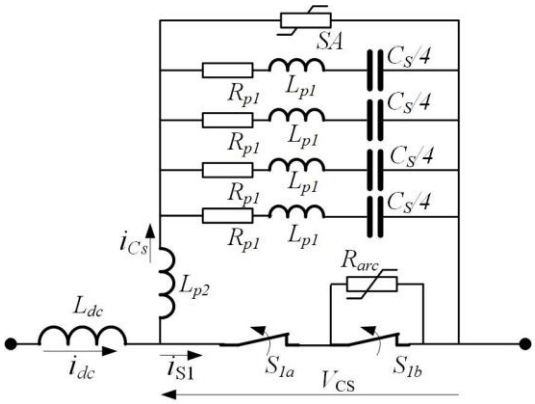


Fig. 12. Commutating circuit model in PSCAD.

Table I Arc resistance in the PSCAD model.

Current	Resistance		Current	Resistance
0.5A	50Ω		200A	0.08Ω
1A	100Ω		300A	0.053Ω
2A	25Ω		500A	0.035Ω
10A	16Ω		600A	0.033Ω0
100A	0.16Ω		10000A	0.002Ω

Table II Parameters of the commutating circuit model.

PSCAD model		Analytical model	
Rp1	0.03Ω	Rp	$R_{p1}/(C_s/52\mu F)$
Lp1	130nH	Lp	$L_{p1}+L_{p2}/(C_s/52\mu F)$
Lp2	195nH	Varc0	16V

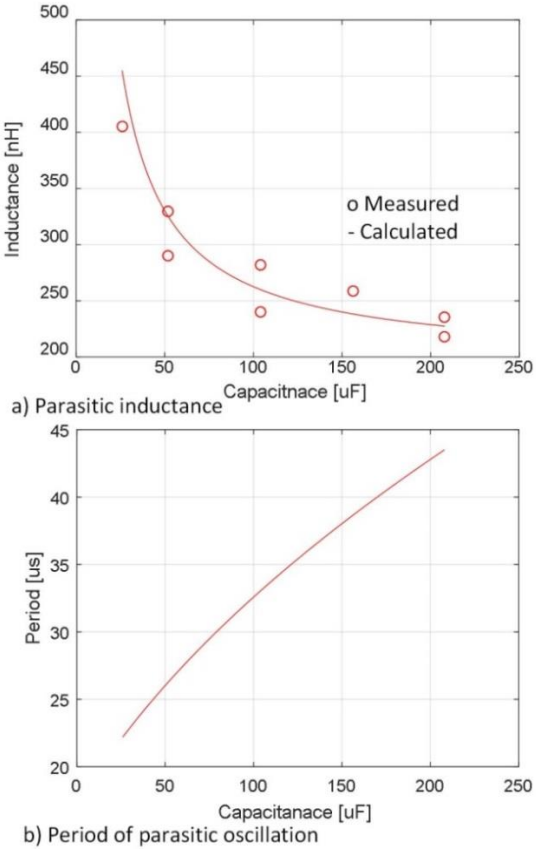


Fig. 13. Estimation of parasitic inductances and the period.

B. Analytical model

The analytical modeling of DC current commutation through parasitic circuit is well described in [12]. Similar approach is used here but capacitor is included in the circuit as shown in Fig. 14. This model enables fast parametric studies. Instead of non-linear resistance, in this linear model a simple constant voltage V_{arc0}=16V is used to represent arc. This is justified since gap distance changes only marginally (around 40 μm) for the short arcing duration, and has no noticeable impact on the arc voltage. A single Lp is used for simplicity.

Using circuit theory, the time domain expression for the current i_{S1} after S_1 opens, can be derived as:

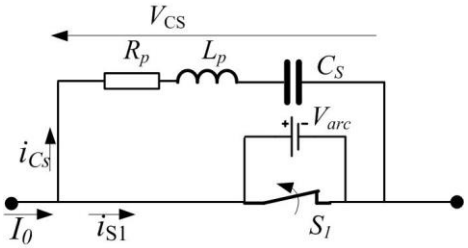


Fig. 14. Analytical model of commutating circuit.

$$i_{S1} = I_0 - \frac{V_{arc0}}{z_p\sqrt{1-\zeta^2}} e^{-\zeta\omega_{pd}t}\sin\left(\omega_{pd}t\right), \qquad (11)$$

where subscript 0 denotes values at commutation, and:

$$\omega_{pd} = \omega_p \sqrt{1-\zeta^2}, \quad \omega_p = 1/\sqrt{L_p C_s}, \\ \zeta = R_p/(2Z_p), \quad Z_p = \sqrt{L_p/C_s}, \tag{12}$$

The value of the first peak of the oscillating current in (11) is:

$$I_{P1} = \frac{V_{arc0}}{e^{\frac{\pi R_p}{4}\sqrt{\frac{C_s}{L_p}}} \sqrt{\frac{L_p}{C_s} - \left(\frac{R_p}{2}\right)^2}} \tag{13}$$

If this peak current I_{p1} is larger than I_0 then current crosses zero and commutation is successful. The parameters of this model are shown in Table II.

The accuracy of this model has been confirmed by testing against experimental results is shown in Fig. 10. Equation (13) is also verified for other values of capacitance and the curve is shown as "Parasitic inductance model" in Fig. 9. It is seen that this model quite accurately predicts maximum current that can be commutated. Because of arc voltage increase for low currents, this model is inaccurate for I_0<20 A.

Therefore, the ideal model in (6) gives only necessary condition. The commutation is successful if both: ideal and parasitic model conditions are satisfied.

C. Commutating higher DC current and practical design

Of primary practical importance for a possible DC CB design is the magnitude of the DC current that can be commutated. Considering (13), DC current magnitude can be increased by:

- Increasing C_s,
- Increasing V_{arc0},
- Reducing L_p,
- Reducing R_p.

The arc voltage can be increased in various ways like using different medium, contact geometry or using multiple break points. The benefit of two breaking points is in doubling the arc voltage, as it has been experimentally confirmed in [9]. Fig. 15 shows the required arc voltage to commutate larger currents for a range of parasitic inductances, and capacitances (the base case is C_s=208 μF, L_p=233 nH, R_p=0.0092 Ω, V_{arc}=16 V). As an example, with approximately 4 break points it might be possible to commutate around 2000 A on this test circuit assuming all other parameters are unchanged.

The methods for reducing parasitic inductances also exist, like for example sandwich bus bar commonly used with Voltage Source Converters.

Considering (6), higher current can be commutated by:

- Increasing velocity at separation v_0,
- Increasing capacitance C_s,
- Increasing dielectric strength E_b.

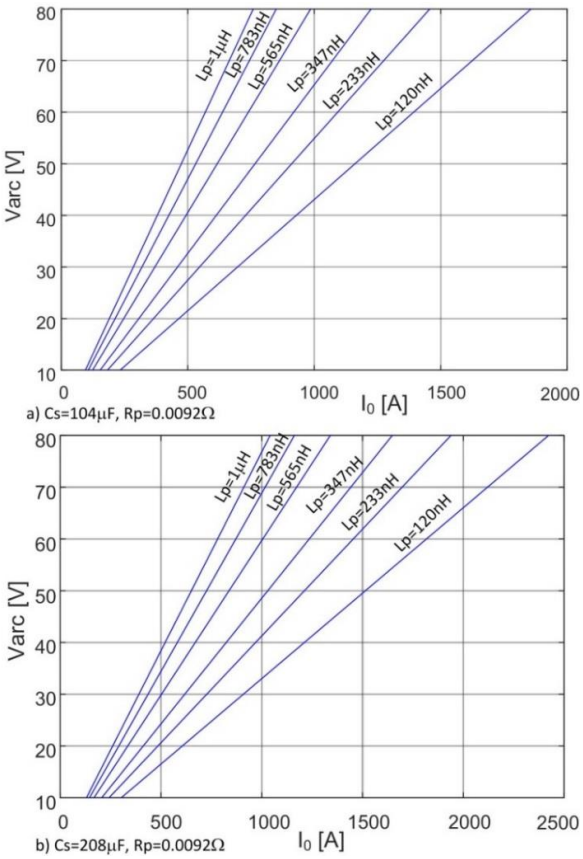


Fig. 15. Arc voltage versus commutating current.

V. SCALING FOR HIGH VOLTAGES AND CURRENTS

No tests have been performed at higher currents/voltages or cost evaluations for scaling to transmission-level voltages. However it might be of benefit to evaluate some key parameters for a transmission-level case using the developed models.

Table III shows the basic parameters for practical 320kV SF_6 disconnector from [14], and the calculated capacitance according to (6), with presumed 4 kA commutating current. The obtained value for capacitance is 14.5 μF which is acceptable.

The parasitic parameters are very difficult to evaluate, and [12] recommends inductance of 200 nH/m while resistance is 10 μΩ/m for bus bars. Parasitic inductance for the capacitors should be added. Fig. 16 shows the required arc voltage versus commutating current, assuming a more conservative capacitance of 50 μF. It shows that with L_p=5 μH the arc voltage of 1.1 kV could commutate current of 4 kA.

Table III Estimated parameters for 320kV, 4kA commutation.

Peak voltage	Contact distance	Contact velocity v	Current I_0	Capacitance C_s
550kV	*0.073m*	*37m/s*	*4000 A*	*14.5 μF*

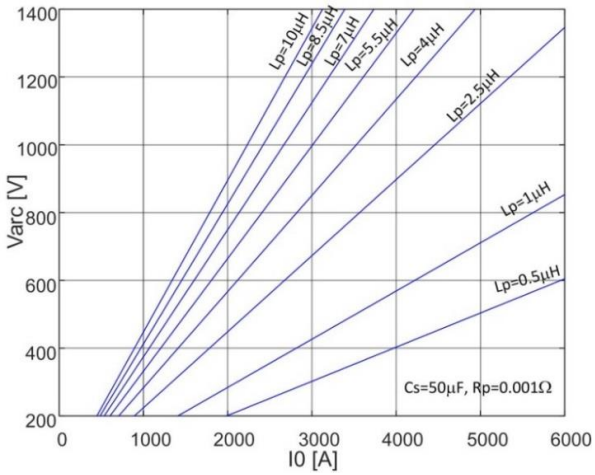


Fig. 16. Arc voltage versus commutating current for HV application.

VI. Conclusion

The article describes a method of fast commutation of DC current into a capacitor. Theoretical study concludes that non-zero contact velocity at separation is required, and a particular switch design is proposed to meet this requirement. A simple equation enables evaluation of commutating current for the given contact velocity, capacitance and dielectric strength.

Experimental results on a laboratory set up illustrate successful DC current commutation up to 400 A, with voltages of 1.3 kV. It is concluded that parasitic parameters reduce the magnitude of the current that can be commutated, and both: ideal and parasitic model conditions should be satisfied.

A detailed non-linear PSCAD model and linear model for the parasitic circuit are presented and evaluated. It is confirmed that the models enable accurate prediction of the commutation.

The DC current commutation in the proposed method occurs 5-10 μs after the contact separation, which is much faster than with other methods with moving contacts. In practical terms, this method has no arcing which eliminates thermal issues and simplifies mechanical design of the switch.

VII. Acknowledgment

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IX. Biography

Dragan Jovcic (S'97-M'00-SM'06) obtained a Diploma Engineer degree in Control Engineering from the University of Belgrade, Serbia in 1993 and a Ph.D. degree in Electrical Engineering from the University of Auckland, New Zealand in 1999. He is currently a professor with the University of Aberdeen, Scotland where he has been since 2004. In 2008 he held visiting professor post at McGill University, Montreal, Canada. He also worked as a lecturer with University of Ulster, in the period 2000-2004 and as a design Engineer in the New Zealand power industry, Wellington, in the period 1999-2000. His research interests lie in the HVDC, FACTS, dc grids and control systems.