A Novel Fault Let-through Energy based Fault Location for LVDC Distribution Networks

Dong Wang, *Student Member, IEEE,* Vasileios Psaras, *Student Member, IEEE,* Abdullah A. S Emhemed, *Member, IEEE* and Graeme. M. Burt, *Member, IEEE*

***Abstract*—Low Voltage Direct Current (LVDC) distribution systems have recently been considered as an alternative approach to electrical system infrastructure as they provide the additional flexibility and controllability required to facilitate the integration of more low carbon technologies (LCTs). However, DC protection systems and, more specifically high accuracy DC fault location, have been recognised as a key challenge to facilitating post-fault network maintenance. Most of the existing fault location techniques rely on current derivative or communications-based methods that are either very sensitive to noise or require a high level of data synchronisation. Fault energy has been recognized as a reliable indicator of more accurate fault location estimations. Therefore, this paper develops a mathematical model for describing fault energy during the transient period of DC faults. The method subsequently proposes a new fault let-through energy based DC fault location working strategy to facilitate post-fault network maintenance. The proposed method does not require data synchronisation regardless of the voltage, current, and the size of the converters connected to the LVDC feeder. The capabilities of the proposed fault location strategy are validated against different faults applied on an LVDC test network in PSCAD/EMTDC and shown to be more reliable and accurate than existing methods.**

***Index Terms*—Fault let-through energy, Fault location, LVDC**

I. Introduction

EXISTING low voltage (LV) AC distribution networks are already under pressure to connect growing numbers of low carbon technologies (LCT) such as electric vehicles, heat pumps, micro winds turbines, and solar photovoltaics (PVs) [1]. The ongoing electrification of transport and heat will add significant additional demand to the LV networks. For example, under a future low carbon scenario in the UK, high penetration of electric vehicles with an annual demand of up to 90TWh is expected by 2050, representing an increase of 30% from the 2017 total demand [2]. Also, heat pumps are predicted to dominate the UK heat sector by 2050 with the expectation that the utilization of gas boilers will fall by 70% of the present volume [2]. As a result, these changes to the energy system require the implementation of new solutions on LV networks to ensure electricity is delivered cost effectively.

LVDC distribution systems are being considered as an appropriate solution for increasing the capacity of existing LV networks to meet the anticipated growth in transport and heat demands while also facilitating the integration of LCTs. Currently, the design and implementation of LVDC distribution systems are being investigated, including examples in Finland, Japan, Korea, and China [3]. Benefits such as energy saving, enhanced controllability, and extra capacity have been reported as outcomes from these projects [3]. Also, these efforts have been recently supported by the International Electrotechnical Commission (IEC) [4]. However, one of the key challenging areas identified by researchers as reported by IEC is the need for reliable DC protection solutions that provide fast and discriminative fault detection and precise fault location [4].

Several DC protection solutions have been proposed that can provide fast fault detection and a good level of fault discrimination [5]. As opposed to DC fault detection requirements for fast and selective performance, DC fault location requires high accuracy in order to facilitate post-fault maintenance, especially for cable replacement and network reconfiguration. Most of the existing fault location techniques are based on external discharge devices that are connected offline (i.e. after protection operates, the faulted section is isolated) [6]. However, these methods require the faulted section to be isolated first to avoid interaction between the external discharging device and the grid power supply, while extra operating time is also required [7]. Besides offline fault location methods, a few online (i.e. fault location scheme operates during the fault period) techniques have been proposed in [8][9]. However, these techniques assume the remote end converter is identical to the main converter. This is less likely to happen in LVDC distribution networks as varying quantities of renewables and end-user devices (e.g. electric vehicle chargers, solar generation, and micro winds) are connected.

Also, the majority of DC fault location methods currently rely on the relationship between transient voltage, current and current derivative. However, the magnitude of the current derivative is difficult to capture and very sensitive to noise, while high fidelity data acquisition is challenging [10]. Fault let-through energy (FLTE) is based on the integration of instantaneous current that has been widely used for traditional LV overcurrent protection, and has the potential to be used as a more reliable fault location indicator to provide fault distance estimation and mitigate significantly the noise effect during the integration period.

The authors are with Institute for Energy and Environment, Department of Electrical and Electronic Engineering, University of Strathclyde, Glasgow G1 1XW, UK. (e-mail: d.wang@strath.ac.uk; vasileios.psaras@strath.ac.uk, graeme.burt@strath.ac.uk) and WSP, UK (Abdullah.emhemed@wsp.com)

Therefore, this paper develops a mathematical model to describe the energy relationship during the transient period of DC faults and analyses the impact of remote converters on fault location accuracy. Based on this analysis, a novel FLTE based fault location strategy is proposed. Furthermore, the estimation error is optimized using the critical point (i.e. based on the ratio of local and remote end converter capacitor size) as a reference to select the most suitable side of the feeder to successfully locate the fault. The proposed fault location method does not require data synchronisation. The paper is structured as follows. Section II reviews the existing fault location techniques and outlines the key fault location challenges associated with LVDC distribution networks. Section III introduces the novel fault location technique. Section IV describes models for evaluating the proposed fault location method. Section V presents simulation studies under different fault scenarios for validating the proposed technique. Finally, conclusions of the paper are drawn in section VI.

II. Limitations of Existing Fault Location Methods

Existing fault location methods can be classified into offline and online techniques, where, the former requires an additional external device to inject current into the isolated faulted cable. By analysing the dynamic response of the injected current and the related voltage signals, the fault distance can be estimated. For example, research in [11] proposed the use of a probe unit to locate faults for DC traction power systems. A more accurate noniterative algorithm, which considers the damping frequency and attenuation constant of the probe currents has been proposed in [6] to improve the accuracy of the original algorithm. The probe unit has also been used in DC marine distribution systems [12] using Fast Fourier Transforms to derive an active impedance estimation, and the impedance of the faulted path to estimate the fault distance. Generally, with the probe unit, the main component used for fault location is the predesigned resistor-inductor-capacitor (RLC) circuit which generates the predictable voltage and current waves [12]. Nevertheless, the faulted DC circuit is also an RLC circuit, thus providing opportunities for fault distance estimation based on the transient RLC fault response during fault period.

Research in [13] has proposed an online method that relies on the transient RLC response using the local voltage, current and current derivative (i.e. *dI/dt*) measurements to estimate the impedance within the faulted path. However, this method only focuses on DC systems without fault current contributions from the remote ends of the feeders. This is less likely to happen in LVDC distribution networks when it is widely integrated with LCTs. When LVDC feeders' remote ends are integrated with converters, the downstream fault current contribution is difficult to predict as it is dependent on the impedance within the fault path. Also, different smoothing capacitors of remote end converters have different impact on fault location estimation. The most straightforward method to eliminate this impact is to use a communication link to synchronise the measurements from both sides of the cable as illustrated in [14]. However, the reliance on communication links potentially leads to additional cost and reliability issues.

Recently, methods based exclusively on local measurements have been proposed in order to provide accurate fault location estimation, even in LVDC distribution networks with remote fault current contributions. For example, the method presented in [8] uses the "Prony" method to extract the attenuation factor and resonance angular frequency to determine the impedance of the faulted path. Also, the method in [9] introduces an improved mathematical model that considers remote end fault current contributions and improves the accuracy of fault distance estimation when the fault is located within 50% of the entire cable length. However, both of these two methods assume that the remote end converter has the same filter capacitor size as the main terminal converter. In fact, the size of the smoothing capacitor is dependent on the rating of the power converter [15]. In LVDC distribution networks, the power ratings of the converter at the customer end are expected to vary depending on the local demand and power sources. Thus, the assumption made in [9] is not sufficient for representing the impact of the remote end fault current contribution.

The challenges of existing fault location estimation methods are not only related to the impact of the remote end fault current contributions, but also to the original current derivative based mathematical model. Several existing fault location methods rely on the current derivative [12]-[14]. As the current derivative is very sensitive to noise (e.g. transducer noise), using this mathematical relationship to estimate the fault distance could lead to significant reliability issues and consequently to misrepresentation of the *dI/dt*. For example, Fig. 1 demonstrates the significant impact that noise can have on the current derivative. Even though the noise magnitude is only ±0.3% of the original current signal (from an LVDC test bed [16]), the calculated current derivative significantly deviates from the actual current derivative signal (e.g. ±85% as shown in Fig. 1). This will significantly mitigate the accuracy of the fault location estimation method. Filters have been introduced in [10] in effort to eliminate the noise impacts, but the filter design process can be complicated.

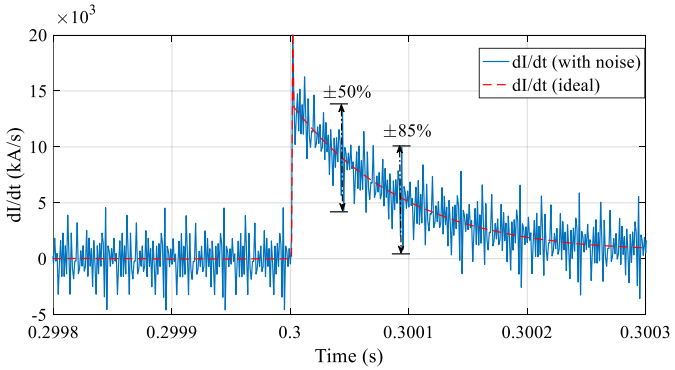

Fig. 1. Comparison of *dI/dt* with and without noise

FLTE, defined as $\int I^2 \bullet dt$ [17], is the integration of the square of instantaneous current that is a more reliable parameter than using the current derivative, and has been widely used in existing inverse-time AC overcurrent protection for fault detection and discrimination. However, it has not been used for locating DC feeder faults (i.e. fault distance estimation). In

contrast to the current derivative, FLTE offers the capability to eliminate noise impact and reduce or avoid the requirement for additional filters. For example, in the original current signal of Fig. 1, the variation of FLTE in a 100μs window is only 0.03% when there is ±0.3% noise in the current signals. Therefore, the proceeding section develops an FLTE based fault location method for LVDC distribution networks. Using local voltage and current along with the calculated transient FLTE, the fault location can be estimated during fault transient period.

III. A New Transient Fault Let-through Energy based Fault Location Method

A. Description of a mathematical model for DC fault location based on FLTE

During the fault transient period (i.e. capacitor discharge period), an equivalent RLC circuit is established as shown in Fig. 2, where, C_l and C_r represent the capacitors within the local and remote converters which are considered as the dominant capacitive elements in the fault circuit. This assumption is justified by the fact that the equivalent capacitance of LVDC cables (e.g. 0.1μF/km [18], 12.1nF/km [19], 8.34nF/km [20]) is much smaller than the converter capacitor (e.g. 12mF [21]), and therefore can be neglected without significantly affecting the performance of the method. R_l and L_l are the fault upstream impedance up to the local converter, R_r and L_r are the fault downstream impedance down to the remote end converter.

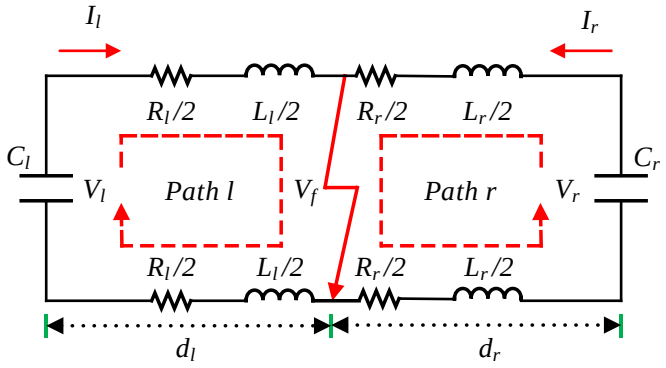

Fig. 2. Simplified faulted circuit during converter capacitor discharge stage

The relationship between voltage and current at the upstream side (i.e. left side in Fig. 2) can be described in (1), where, (V_l, I_l) and (V_r, I_r) are the upstream and downstream (i.e. with respect to the fault) voltages and currents respectively, V_f is the voltage at the fault point, L_l and R_l are the total inductance and resistance between the capacitor C_l to the fault point. To obtain the energy expression, both sides of equation (1) are multiplied by $I_l \bullet \Delta t$ and subsequently integrated for the time period t_1-t_2 (i.e. t_1-t_2 is the first fixed time window for calculating the energy, t_1 is selected based on the overcurrent detection). The resulting energy equation is illustrated in (2). In the right side of (2), the first term indicates the FLTE in the resistance within the *Path l* as shown in Fig. 2, the second term illustrates the energy in the inductance within the *Path l*, where $I_{l\text{-}t2}$ and $I_{l\text{-}t2}$ are the currents recorded at time t_1 and t_2, while the final term is the energy in the fault resistance contributed by both upstream (i.e. I_l) and downstream (i.e. I_r) currents.

$$V_l - V_f = V_l - (I_l + I_r)\cdot R_f = L_l \cdot \frac{dI_l}{dt} + I_l \cdot R_l \tag{1}$$

$$\rightarrow V_l = L_l \cdot \frac{dI_l}{dt} + I_l \cdot R_l + (I_l + I_r)\cdot R_f$$

$$\rightarrow V_l \cdot I_l \cdot \Delta t = L_l \cdot \frac{dI_l}{dt} \cdot I_l \cdot \Delta t + I_l \cdot R_l \cdot I_l \cdot \Delta t + (I_l + I_r)\cdot R_f \cdot I_l \cdot \Delta t$$

$$\rightarrow \int_{t1}^{t2} V_l \cdot I_l \cdot dt = L_l \cdot \int_{t1}^{t2} \frac{dI_l}{dt} \cdot I_l \cdot dt + (R_l + R_f)\cdot \int_{t1}^{t2} I_l^2 \cdot dt + R_f \cdot \int_{t1}^{t2} I_l \cdot I_r \cdot dt$$

$$\int_{t1}^{t2} V_l \cdot I_l \cdot dt = (R_l + R_f)\cdot \int_{t1}^{t2} I_l^2 \cdot dt + L_l \cdot \frac{1}{2}\cdot (I_{l-t2}^2 - I_{l-t1}^2) + R_f \cdot \int_{t1}^{t2} I_l \cdot I_r \cdot dt \tag{2}$$

To determine the impedance of the fault path, the energy equation is also applied for the time period t_1-t_3 (i.e., t_1-t_3 is the second fixed time window for calculating the energy). Time t_1 is selected based on overcurrent detection. By combining the two energy balance equations, the inductance of the fault path can be derived by (3). Each term in (3) is defined in (4). Where, $I_{l\text{-}t3}$ is the current recorded at time t_3. Also, in (3), A_1 is the FLTE, B_1 is the energy contribution to the cable inductance, C_1 is the energy dissipated in the upstream side during t_1-t_2, and D_1 is the fault energy in the fault resistance contributed from upstream and downstream fault currents. Similarly, A_2, B_2, C_2, and D_2 are the corresponding parameters during time t_1-t_3. Regarding the right side of (3), only the first part can be calculated based on local measurements, while the second part is dependent on the remote end fault current (I_r) and fault resistance (R_f).

$$L_l = \frac{C_1 - C_2 \cdot \frac{A_1}{A_2}}{B_1 - B_2 \cdot \frac{A_1}{A_2}} - R_f \cdot \frac{D_1 - D_2 \cdot \frac{A_1}{A_2}}{B_1 - B_2 \cdot \frac{A_1}{A_2}} \tag{3}$$

$$\begin{cases} A_1 = \int_{t1}^{t2} {I_l}^2 \cdot dt \\ B_1 = \int_{t1}^{t2} I_l \cdot \frac{dI_l}{dt} \cdot dt \approx \frac{1}{2}\cdot (I_{l-t2}^2 - I_{l-t1}^2) \\ C_1 = \int_{t1}^{t2} V_l \cdot I_l \cdot dt \\ D_1 = \int_{t1}^{t2} I_l \cdot I_r \cdot dt \\ A_2 = \int_{t1}^{t3} {I_l}^2 \cdot dt \\ B_2 = \int_{t1}^{t3} I_l \cdot \frac{dI_l}{dt} \cdot dt \approx \frac{1}{2}\cdot (I_{l-t3}^2 - I_{l-t1}^2) \\ C_2 = \int_{t1}^{t3} V_l \cdot I_l \cdot dt \\ D_2 = \int_{t1}^{t3} I_l \cdot I_r \cdot dt \end{cases} \tag{4}$$

B. Optimizing location accuracy with critical point

If the fault location relies only on local measurements of one side, the latter part of (3) is recognized as the estimation error that can be written as (5). If the ratio of the fault currents (i.e. I_l/I_r) is a constant, the error is theoretically zero. Thus, this fault distance is regarded as the critical distance and is defined as the fault location where the fault current ratio of upstream and downstream is constant. It is necessary to know the critical point before a DC fault happens. Using (1) and the similar equation based on V_r, the relationship between the voltage and the ratio between upstream to downstream current can be illustrated in (6).

$$error = R_f \cdot \frac{\dfrac{\int_{t1}^{t2} I_l \cdot I_r \cdot dt}{\int_{t1}^{t2} I_l \cdot I_l \cdot dt} - \dfrac{\int_{t1}^{t3} I_l \cdot I_r \cdot dt}{\int_{t1}^{t3} I_l \cdot I_l \cdot dt}}{\dfrac{\int_{t1}^{t2} I_l \cdot \frac{dI_l}{dt} \cdot dt}{\int_{t1}^{t2} I_l \cdot I_l \cdot dt} - \dfrac{\int_{t1}^{t3} I_l \cdot \frac{dI_l}{dt} \cdot dt}{\int_{t1}^{t3} I_l \cdot I_l \cdot dt}} \tag{5}$$

$$V_l - V_r = L_l \cdot \frac{dI_l}{dt} + I_l \cdot R_l - (L_r \cdot \frac{dI_r}{dt} + I_r \cdot R_r) \tag{6}$$

Equation (6) can also be expressed as in (7). If the voltages on the upstream and downstream sides are equal during the transient fault period, the current ratio is equal to the ratio of the fault distance as seen from the upstream side (i.e. d_l, as shown in Fig. 2) to that seen from the downstream side (i.e. d_r, as shown in Fig. 2) and is shown in (8).

$$\frac{V_l - V_r}{(L_r \cdot \frac{dV_r}{dt} + I_r \cdot R_r)} = \frac{L_l \cdot \frac{dI_l}{dt} + I_l \cdot R_l}{(L_r \cdot \frac{dI_r}{dt} + I_r \cdot R_r)} - 1 \tag{7}$$

$$\frac{d_l}{d_r} \approx \frac{I_r}{I_l} \tag{8}$$

Assuming the fault current from the capacitor dominates the fault current within the fault path during the transient period, there is a relationship between the voltage and current of upstream and downstream converters as shown in (9). Combining (8) and (9), and assuming the voltages from upstream and downstream sides are equal, the critical distance can be derived as the capacitor ratio shown in (10). This means that, theoretically, the critical distance is dominated by the size of capacitors connected at both sides of the faulted feeder.

$$\begin{cases} I_l = -C_l \cdot \dfrac{dV_l}{dt} \\ I_r = -C_r \cdot \dfrac{dV_r}{dt} \end{cases} \tag{9}$$

$$\frac{d_l}{d_r} = \frac{C_r}{C_l} \tag{10}$$

The following analysis is based on the aforementioned critical distance and focuses on the remote end fault current contributions when capacitor at both ends are the same and local measurements at the upstream side as shown in Fig. 2 are considered. Moreover, the time period t_1-t_2 and t_2-t_3 are assumed equal to the sampling time Δt. If the fault distance is less than the critical fault distance, current I_l is always bigger than current I_r during the capacitor discharge stage. The numerator of (5), defined as *error-num* can be evaluated based on Riemann sums left rule [22] as shown in (11). During the DC fault transient period (i.e. capacitor discharge phase), the fault current derivative decreases. As the fault path impedance in the upstream side (i.e. *Path l* as shown in Fig. 2) is smaller than the downstream side (i.e. *Path r* as shown in Fig. 2), the current derivative of the upstream side reduces faster than the downstream side. Thus, from time t_1 to t_2, the ratio I_r/I_l is increasing as illustrated in (12). As a result, the second term in (11) becomes increasingly greater than the first term, causing (11) to be negative when the fault distance is less than the critical point. In contrast, when the fault distance is beyond the critical point, the sign of (11) is positive. Meanwhile, when the fault is located closer to the local converter, the current derivative of the upstream side has the highest transient peak compared to the other fault location. That results in the biggest value of *error-num* with the negative sign. Similarly, when the fault is located closer to the remote end converter, the *error-num* has the highest value with positive sign. Thus, the *error-num* is a monotonic increasing function that is zero at the critical point.

$$\begin{aligned} error-num &= \frac{\int_{t1}^{t2} I_l \cdot I_r \cdot dt}{\int_{t1}^{t2} I_l \cdot I_l \cdot dt} - \frac{\int_{t1}^{t3} I_l \cdot I_r \cdot dt}{\int_{t1}^{t3} I_l \cdot I_l \cdot dt} \\ &\approx \frac{I_r(t_1)}{I_l(t_1)} - \frac{I_l(t_1) \cdot I_r(t_1) + I_l(t_2) \cdot I_r(t_2)}{I_l(t_1) \cdot I_l(t_1) + I_l(t_2) \cdot I_l(t_2)} \end{aligned} \tag{11}$$

$$\frac{I_r(t_2)}{I_l(t_2)} > \frac{I_r(t_1)}{I_l(t_1)} \tag{12}$$

The denominator of the later term of (5), is also given by (13). In the time domain, from time t_1 to t_2, as the current derivative is reducing and current is increasing during the fault transient period, the ratio of current derivative to the current (i.e. $(dI/dt)/I$) is decreasing as illustrated (14).

$$\begin{aligned} error-den &= \frac{\int_{t1}^{t2} I_l \cdot \frac{dI_l}{dt} \cdot dt}{\int_{t1}^{t2} I_l \cdot I_l \cdot dt} - \frac{\int_{t1}^{t3} I_l \cdot \frac{dI_l}{dt} \cdot dt}{\int_{t1}^{t3} I_l \cdot I_l \cdot dt} \\ &\approx \frac{\frac{dI_l}{dt}(t_1)}{I_l(t_1)} - \frac{I_l(t_1) \cdot \frac{dI_l}{dt}(t_1) + I_l(t_2) \cdot \frac{dI_l}{dt}(t_2)}{I_l(t_1) \cdot I_l(t_1) + I_l(t_2) \cdot I_l(t_2)} \end{aligned} \tag{13}$$

$$\frac{\frac{dI_l}{dt}(t_1)}{I_l(t_1)} > \frac{\frac{dI_l}{dt}(t_2)}{I_l(t_2)} \tag{14}$$

As a result, the sign of *error-den* is always positive. Considering the distance to the fault and the fact that the current derivative is directly influenced by the fault distance, the ratio between current derivative and current magnitude reduces for increasing distance. This in turn causes the *error-den* to

decrease and behaves as a monotonic decreasing function as fault distance increases far away from local converters.

Table I summarises the above analysis related to the remote fault current contribution on fault location estimation errors. As the fault moves further, if the fault distance is less than the critical point, the estimated fault distance is less than the actual fault distance. Otherwise, the estimated fault location is further than the actual fault location.

Table I Summary of behaviours of online fault location errors as fault distance is increasing

Fault distance	Sign of error	Magnitude of error
<critical point	-	decreasing
>critical point	+	increasing

Fig. 3 shows an example of estimation errors for different faults (fault distance is assumed with respect to C_l) on the simplified circuit shown in Fig. 2, 500m cable length connected with the same capacitors at both ends. In this case, the mid-point is the critical fault location as the *Path l* and *Path r* are symmetrical as shown in Fig. 2. For the fixed time window t_1-t_2 and t_1-t_3, during which the fault current increases rapidly for any faults along the feeder, the absolute values of *error-num* are symmetrical around the critical fault distance. Moreover, since the *error-den* is a positive monotonic decreasing function, the value of *error-den* for faults before the critical distance is averagely higher than the one for faults after critical distance. The above characteristics of *error-num* and *error-den* make the estimation error for faults happening at the upstream side of the critical distance relatively smaller than faults at the downstream side. This is also illustrated in Fig. 3, where the average error of the fault location estimation is significantly smaller for faults before the critical point. Thus, by combining the fault location estimations of both sides based on the critical point, a more accurate fault estimation result is possible. In detail, the strategy is as follows,

- If the local estimated fault distance is less than critical distance, then this side's estimation is selected.
- Otherwise, the remote side's distance estimation is selected as a reference.

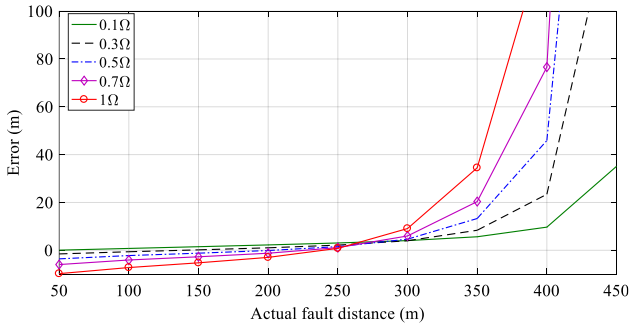

Fig. 3. An example of fault location errors for faults on an ideal circuit with the same capacitors are connected at both ends

C. Description of an FLTE based fault location algorithm

Based on the previous analysis, a novel fault location technique based on FLTE is proposed. The distance estimation is optimized by the critical point based working strategy. The proposed method does not require any data synchronisation and relies only on local measurements. The flow chart of the proposed fault location algorithm is shown in Fig. 4.

The key parameters used by the local fault location devices are the DC voltages, currents, and the calculated FLTE. The calculation of the injected energy into the fault path is based on the integration of the voltage-current product (i.e. $E_{in}=\int V \bullet I \bullet dt$).

As discussed in the previous section, the proposed fault location technique is dependent on the capacitor discharge stage. It is necessary to set criteria for initializing the fault location algorithm when it is required and for selecting an appropriate window to calculate the FLTE. For this purpose, a combination of overcurrent and a fixed time period is used. Time t_1 is considered as the time instant where the fault current first exceeds the selected threshold (i.e. $I_{threshold}$, 1.2p.u. in this case). The time 100μs later of time t_1 is recorded as time t_2, while the time 200μs later of time t_1, is recorded as time t_3. The window selection is mainly required to ensure the captured data is within the initial stage of the DC fault transient period.

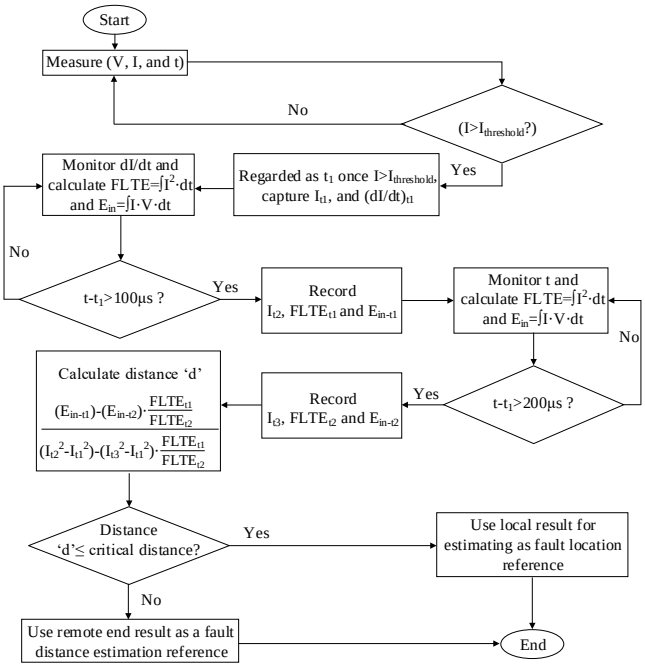

Fig. 4. Flow chart of the proposed online fault location strategy

IV. Model for Evaluating the Proposed Fault Location Method

A. Test Network Modelling

An LVDC test network is developed as shown in Fig. 5. The parameters of the developed test network are given in Table II.

Table II Parameters of the LVDC test network

Parameter	Value
AC supply	11kV
Fault level	156MVA [23]
Transformer	11kV/0.4kV
VSC	1MVA, 5mF
LVDC distribution voltage	±0.75kV (pole-to-pole)
LVDC feeder	0.164 Ω/km, 0.00024 H/km [5], 500m
DAB converter	±0.75kV kV/±0.2kV, 200kW, 2.5mF
DC customers	200 kW

The LVDC is interfaced to an AC grid through a two-level voltage source converter (VSC). The VSC provides ±0.75kV DC pole-to-pole voltage. The LVDC feeders are modelled as an equivalent R-L circuit with 500m. The LVDC network supplies four aggregated end users (200kW each) that are interfaced through a dual active bridge (DAB) converter.

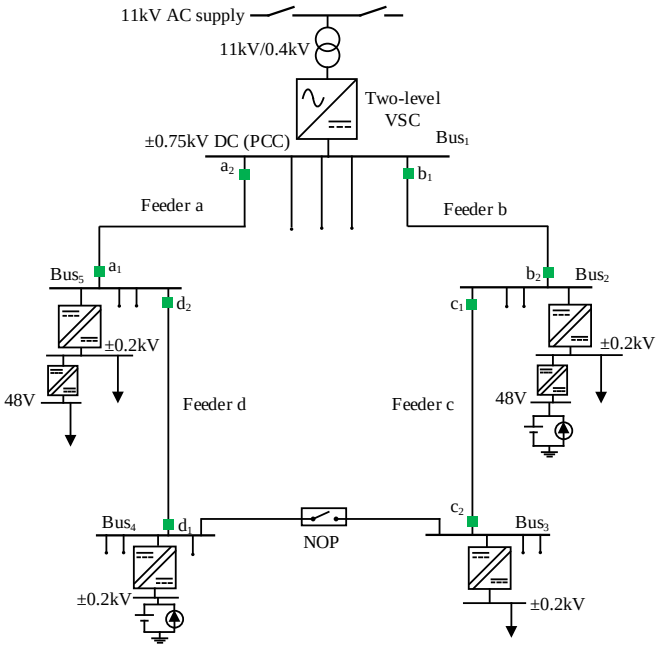

Fig. 5. A test model of an LVDC distribution network

B. Model of FLTE based fault location

The model developed for the implementation of the proposed fault location algorithm is illustrated in Fig. 6.

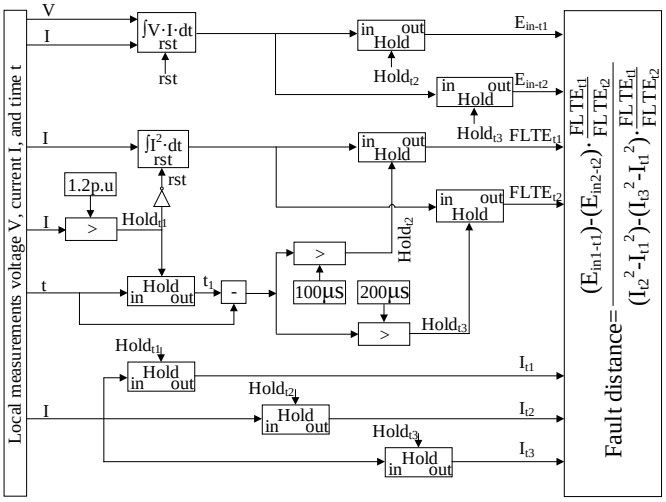

Fig. 6. Model of fault let-through energy based fault location

Devices 'b_1', and 'b_2' shown in Fig. 5 are fault location devices. For each fault location device, only voltage, current, and time are monitored with 1MHz sampling frequency [10]. Each device is updated with the associated critical point (i.e. 'b_1' is 167m, 'b_2' is 333m). To add the credibility to the simulation results, voltage and current measurements are contaminated with noise signal (±0.3% variations) captured from a real LVDC testbed [16].

V. Validation of the Proposed Fault Location Technique

In the simulation studies, DC pole-to-pole faults are applied along the 0.5km cables with 0.1Ω fault resistance intervals in the range from 0.1Ω to 1Ω. Faults are applied on feeder 'b' to test the case where the feeder has converters of different size connected to its ends.

A. Fault location estimation accuracy

Fig. 7 shows the fault location errors of device 'b_1' for faults on feeder 'b' for different fault distances and fault resistances. Within 167m, the fault location estimation of device 'b_1' has a relatively small error (1.7m, 3%, the fault at 50m away device 'b_1'). When the fault moves beyond 167m, the fault location error increases significantly (up to 393m, 87%, the fault at 450m away device 'b_1').

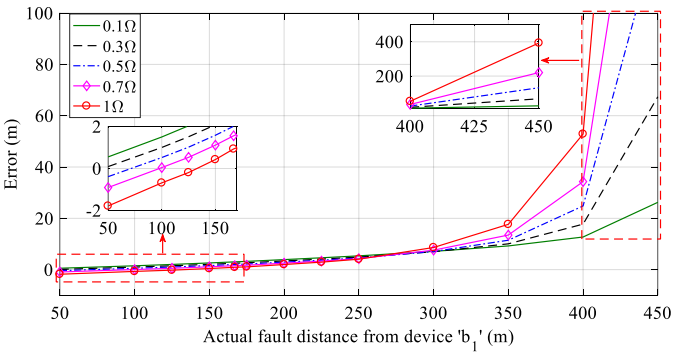

Fig. 7. Fault location errors of device 'b_1' when fault distance and fault resistance change on feeder 'b'

For device 'b_2', the fault location error is relatively small (up to 3.5m (i.e. 0.7%), for a fault at 450m away device 'b_1') for faults that occur within the critical point (333m away from device 'b_2') as shown in Fig. 8.

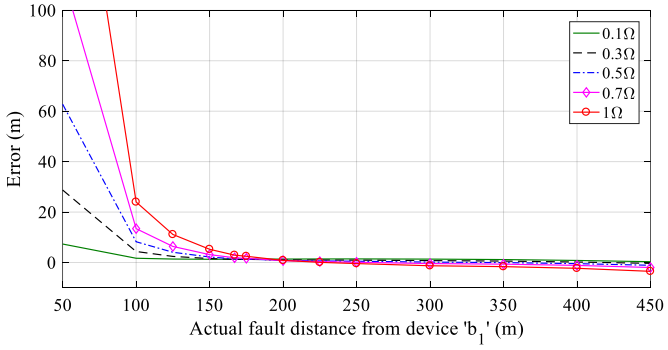

Fig. 8. Fault location errors of device 'b_2' for different fault distances and fault resistances on feeder 'b'

When the fault occurs beyond the critical point, the estimation error can reach up to 213m, representing 426% distance error for the fault 50m away from device 'b_1'. It is evident that the fault location estimations from both sides of the cable are significantly different when the LVDC feeder is connected with different converters at each end. It is therefore necessary for a workable estimation algorithm to select the appropriate device ('b_1' or 'b_2') to be used as a reference for

locating the DC fault. The existing strategy for locating DC faults as proposed in [9], namely the 50% rule, relies on each protective relay being responsible for locating DC faults in the first half of the feeder. Nevertheless, if this strategy is used in this particular example, errors will arise because device 'b_1' can provide more accurate fault location estimation for the first 33.3% of the feeder rather than the rest 66.7% of the feeder.

For example, considering Bus_1 as a reference, Fig. 9 shows the errors of the proposed estimation method for a 500m connected with converters (local to remote capacitor ratio is 2:1). Its estimation errors are within the range of (-2.5m to 3.5m, average 0.6%). In terms of the improvements of fault location working algorithm, compared to the existing 50% fault location strategy, the proposed critical point based strategy has smaller estimation errors and provides more accurate fault location estimation especially for the faults located in the range of 167m to 250m away from device 'b_1'. For example, when fault resistance is 0.1Ω, using capacitor ratio based fault location strategy, fault estimation error can be reduced up from 2.1% (i.e. 5.4m) to 0.5% (i.e. 1.4m). The simulation results of this basic case illustrate the effectiveness of the proposed method that is using FLTE and critical point based fault location working algorithm.

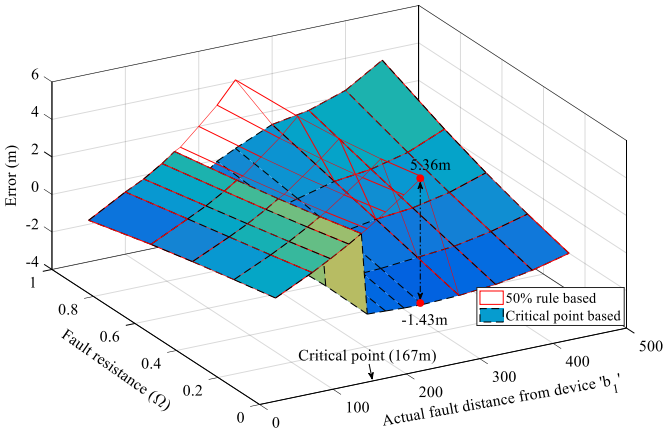

Fig. 9. Fault location errors based on 50% rule and critical point for a 500m feeder with converter capacitor ratio 2:1

B. *Stability and reliability analysis*

The following section will validate their stability and reliability against different converter capacitor ratios, different length of cable, and noises. To investigate the stability of the proposed fault location strategy, the ratio of capacitor size of local and remote converters increases to 4:1. Fig. 10 shows the errors of the proposed estimation method for a 500m connected with converters (local to remote capacitor ratio is 4:1). Its estimation errors are within the range of (-0.9m to 10.3m, average 1.6%). In term of the improvements of fault location working algorithm, compared to the existing 50% fault location strategy, when the fault resistance is relatively small (≤0.2Ω), the proposed critical point based strategy provides more accurate fault location estimation in this case. For example, when fault resistance is 0.1Ω, using the critical point based fault location working strategy, fault estimation error can be reduced from 2.4% (i.e. 6m) to 0.3% (i.e. 0.9m). However, as fault resistance increases, it dominates the estimation error more than the remote fault current contribution (see (5)), and the errors of the distance estimation are getting negatively affected leading to increased errors when local and remote estimations are combined based on the critical point based working strategy.

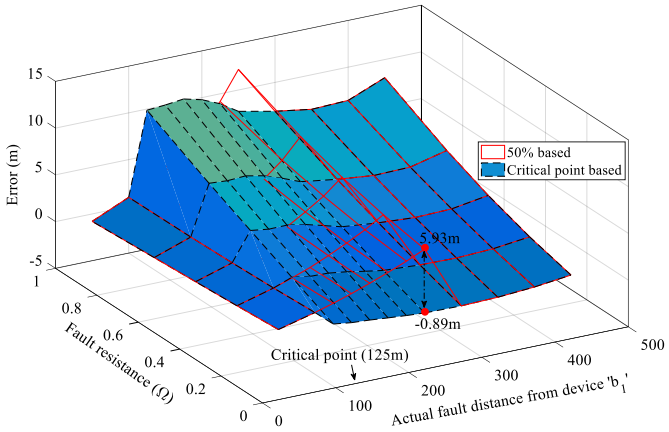

Fig. 10. Fault location errors based on 50% rule and critical point for a 500m feeder with converter capacitor ratio 4:1

The increasing estimation errors for highly resistive faults becomes less when locating faults for a 1000m feeder connected with different converters (local to remote capacitor ratio is 4:1). In this case, the critical distance is 200m away from device 'b_1'. Fig. 11 shows that the errors of using the proposed fault location strategy in this case are within the range of (-1.4m to 4.6m, average 0.4%). Also, the estimation errors are smaller than the ones from the existing 50% based fault location working algorithm. For example, for a 0.1Ω fault, the estimation error can be reduced from 3% (i.e. 15m) to 0.12% (i.e. 0.6m). Compared to the results in the 500m feeder case shown in Fig. 10, the reduced fault estimation errors are mainly caused by the increased cable impedance. The impact of the increasing fault resistance in the total fault estimation error (as illustrated in (5)) becomes less significant than the remote fault current contributions.

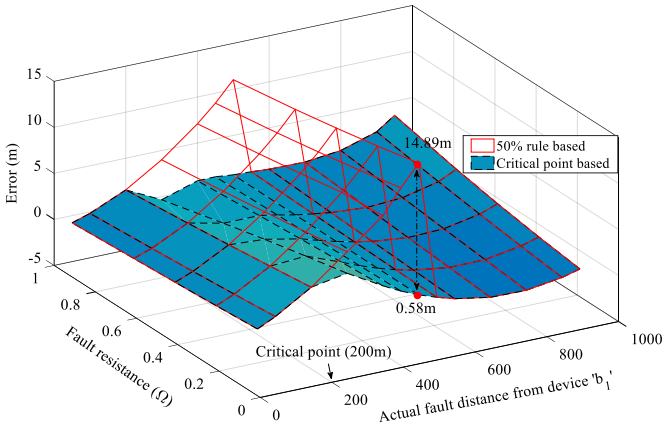

Fig. 11. Fault location errors based on 50% rule and critical point for a 1000m feeder with converter capacitor ratio 4:1

From the above analysis, it can be summarised that the ratio of capacitor size and cable length will influence the performance of the proposed fault location algorithm compared to the existing 50% rule. However, for a relatively small fault resistance (e.g. 0.1Ω), the proposed algorithm is always more accurate (e.g. error reduction up to 15m, 3%) among the studies.

Apart from the improved accuracy, enhanced reliability against noise impact is another key improvement. For example, Fig. 12 shows the behaviours of current, current derivative, and FLTE with white Gaussian noise (signal-to-noise ratio (SNR) 40dB and 20dB) under a 250m 0.1Ω fault (at 0.2s) on a 500m feeder. It can be seen that current derivative signals are almost destroyed with SNR 40dB and 20dB noise signals. Comparatively, the SNR 40dB white noise has negligible impacts on the FLTE as shown in Fig. 12 (c). Even for the significant SNR 20dB white noise, it only creates a small range of FLTE variations (≤0.23%). The high reliability of FLTE allows the proposed FLTE based fault location technique to provide fault distance estimation with a good level of accuracy under significant noise conditions.

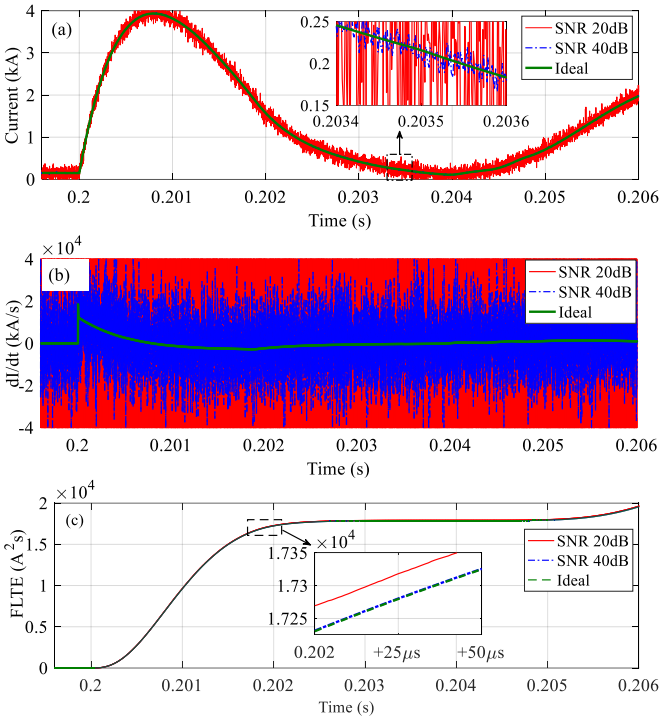

Fig. 12. Response of current (a), current derivative (b), and FLTE (c) with noise signals under a 250m 0.1Ω fault on a 500m LVDC feeder.

Table III illustrates the average estimation errors for estimating faults (≤1Ω) on 500m and 1000m feeders with white Gaussian noise signals (SNR 60dB, 40dB, and 20dB). The estimation error of the proposed method is within 5% for a 500m feeder and 2.5% for a 1000m feeder, which is less likely to be achieved by the existing current derivative based fault location techniques without using additional complicated filters. In particular, the current derivative based method with filtering discussed in [9] has been included in the comparative results shown in Table III. It can be seen that even with properly designed filters, the estimation errors of the current derivative based fault location technique can be up to 18.85% for a 500m feeder and 24.88% for a 1000m feeder with 20dB noise signals. These errors are mainly originating from the distortion of current and voltage signals caused by the use of filters. The comparison between the two methods highlights the significantly greater reliability and accuracy of the proposed FLTE based method at different noise levels.

Table III Average estimation errors of the proposed method under different noise levels and comparison with current derivative (*dI/dt*) based method

SNR (dB)	Average Estimation Error (≤1Ω)			
	500m feeder		1000m feeder	
	Proposed (FLTE)	Existing (*dI/dt*)	Proposed (FLTE)	Existing (*dI/dt*)
60	0.58%	1.1%	0.65%	3.42%
40	2.5%	7.6%	0.94%	11.80%
20	4.7%	18.85%	2.54%	24.88%

VI. Conclusions

This paper has developed a fault let-through energy based fault location technique that can be applied successfully for LVDC fault location estimation. An analytical method has been presented for assessing the fault location estimation errors and the critical distance beyond which the error increases significantly. Based on the critical distance, the device of the more suitable end of the feeder is selected in order to minimize the estimation error. Its high accuracy has been verified against different cable lengths with fault resistance less than 1Ω (e.g. average error 0.6%, with a maximum 3.5m for a 500m feeder and 0.4% average error, 4.6m maximum error for a 1000m). The proposed critical point based working algorithm can reduce estimation errors up to 15m (3%) for a 1000m feeder compared to the existing 50% rule. The improved accuracy allows DC faults to be located within area shorter range and facilitates rapid post fault cable maintenance where different converters are installed at each end of a feeder. In addition, the high reliability and satisfying accuracy of the technique have been verified under a significant noisy environment.

Future work will focus on testing the proposed method in a wider range of LVDC networks, while steps will also be taken towards validation and demonstration in real networks to further assess the practical feasibility of the method.

References

[1] V. Vossos, K. Johnson, K. Margarita, M. Khattar, D. Gerber, and B. Rich, "Lawrence Berkeley National Laboratory Review of DC Power Distribution in Buildings: A Technology and Market Assessment," 2017. [Online]. Available: https://eta.lbl.gov/publications/review-dc-power-distribution. [Accessed: 05-Apr-2020]

[2] "Future Energy Scenarios 2017," 2017. [Online]. Available: http://fes.nationalgrid.com/fes-document/fes-2017/.

[3] A. Emhemed, D. Wang, G. Burt, J. Zafar, and A. Kazerooni, "Multi-zone LVDC distribution systems architecture for facilitating low carbon technologies uptake," in *15th IET ACDC*, 2019.

[4] IEC, "LVDC: electricity for the 21st century," 2017. [Online]. Available: http://www.iec.ch/technologyreport/pdf/IEC_TR-LVDC.pdf.

[5] D. Wang, A. Emhemed, P. Norman, and G. Burt, "Evaluation of existing DC protection solutions on an active LVDC distribution network under different fault conditions," in *CIRED 2017*, 2017.

[6] R. Mohanty, U. Balaji, and A. Pradhan, "An Accurate Noniterative Fault-Location Technique for Low-Voltage DC Microgrid," *IEEE Trans. Power Deliv.*, vol. 31, no. 2, pp. 475–481, 2016.

[7] W. Javed, D. Chen, M. Farrag, and Y. Xu, "System Configuration, Fault Detection, Location, Isolation and Restoration: A Review on LVDC Microgrid Protections," *Energies*, vol. 12, no. 6, p. 1001, 2019.

[8] K. Jia, M. Li, T. Bi, and Q. Yang, "A voltage resonance-based single-ended online fault location algorithm for DC distribution networks," *Sci. China Technol. Sci.*, vol. 59, no. 5, pp. 721–729, 2016.

[9] A. Meghwani, S. Srivastava, and S. Chakrabarti, "Local measurement-based technique for estimating fault location in multi-source DC microgrids," *IET Gener. Transm. Distrib.*, vol. 12, no. 13, pp. 3305–3313, 2018.

[10] C. Li, P. Rakhra, P. Norman, G. Burt, and P. Clarkson, "Metrology requirements of state-of-the-art protection schemes for DC microgrids,"

J. Eng., vol. 2018, no. 15, pp. 987–992, 2018.
[11] J. Do Park, "Ground fault detection and location for ungrounded DC traction power systems," *IEEE Trans. Veh. Technol.*, vol. 64, no. 12, pp. 5667–5676, 2015.
[12] K. Jia, T. Bi, B. Liu, E. Christopher, D. Thomas, and M. Sumner, "Marine Power Distribution System Fault Location Using a Portable Injection Unit," *IEEE Trans. Power Deliv.*, vol. 30, no. 2, pp. 818–826, 2015.
[13] X. Feng, L. Qi, and J. Pan, "A Novel Fault Location Method and Algorithm for DC Distribution Protection," *IEEE Trans. Ind. Appl.*, vol. 53, no. 3, pp. 1834–1840, 2017.
[14] L. Zhang, N. Tai, W. Huang, and Y. Wang, "Fault distance estimation-based protection scheme for DC microgrids," in *14th IET ACDC*, 2018.
[15] Y. Zhong, N. Roscoe, D. Holliday, T. Lim, and S. Finney, "High-Efficiency MOSFET-Based MMC Design for LVDC Distribution Systems," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 321–334, 2018.
[16] A. Emhemed, K. Fong, S. Fletcher, and G. Burt, "Validation of fast and selective protection scheme for an LVDC distribution network," *IEEE Trans. Power Deliv.*, vol. 32, no. 3, pp. 1432–1440, 2017.
[17] BS7671, "Requirements for Elecrical Installations," 2018.
[18] S. Dhar, R. K. Patnaik, and P. K. Dash, "Fault Detection and Location of Photovoltaic Based DC Microgrid Using Differential Protection Strategy," *IEEE Trans. Smart Grid*, vol. 9, no. 5, pp. 4303–4312, 2018.
[19] Y. Yang, C. Huang, and Q. Xu, "A Fault Location Method Suitable for Low-Voltage DC Line," *IEEE Trans. Power Deliv.*, vol. 35, no. 1, pp. 194–204, 2020.
[20] K. Jia, Q. Zhao, T. Feng, and T. Bi, "Distance protection scheme for dc distribution systems based on the high-frequency characteristics of faults," *IEEE Trans. Power Deliv.*, vol. 35, no. 1, pp. 234–243, 2020.
[21] P. Nuutinen, T. Kaipia, P. Peltoniemi, and et al., "Research site for low-voltage direct current distribution in a utility network-structure, functions, and operation," *IEEE Trans. Smart Grid*, vol. 5, no. 5, pp. 2574–2582, 2014.
[22] S. Stewart, "How to Integrate It: A Practical Guide to Finding Elementary Integrals,". *Cambridge University Press*, 2017.
[23] SP Energy Networks, "Distribution long term development statement-Appendix 4 Fault Levels Table 4," 2017.