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Low-Pass Filtering or Gain Tuning Free Simple DC Offset Rejection Technique for Single and Three-Phase Systems

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Abstract

This paper aims to address the DC offset rejection problem in grid synchronization algorithm. A simple approach to estimate the unknown grid frequency in the presence of DC offset is proposed for this purpose. Some of the existing techniques available in the literature use either low-pass filter or an additional integrator to eliminate the DC offset. Both approaches require an additional parameter to tune. However, tuning the additional parameter is not straightforward. Moreover, tuning the overall system can be complicated due to the presence of DC offset rejection part. The proposed approach does not require any additional parameter to tune. By considering the orthogonal signal instead of the DC offset as an additional state, the proposed technique can efficiently estimate the unknown frequency of the grid. Application to both single and three-phase grids are provided. Comparative experimental results with DC offset rejection capable second-order generalized integrator (SOGI) phase-locked loop (PLL) (SOGI-PLL) demonstrate the effectiveness and suitability of the proposed technique.

Keywords: Phase Estimation, Frequency Estimation, DC Offset

1. Introduction

Many applications in power electronics, machine and drives (PEMD) area require accurate information of the grid voltage signal. Some of the application examples are: grid-connected converter [1–14], active power filter [15], dynamic voltage restorer [16, 17], electric vehicle on-board charger [18], motor drive as smart load [19], to name a few. These applications require fast and accurate estimation of single and three-phase grid voltage parameters.

Existing literature on the accurate estimation of grid voltage parameter is huge and covers a wide variety of techniques. Some of the most popular techniques are: Kalman filter [20, 21], discrete Fourier transform (DFT) [22, 23], linear and nonlinear regression [21, 24], adaptive notch filter (ANF) [25, 26], second order generalized integrator (SOGI) [27–33], Luenberger observer [34–36], open-loop techniques [37, 38], phase-locked loop [39–44], to name a few.

DC offset presents a significant challenge for many of the techniques mentioned so far as they do not consider the presence of DC offset explicitly. As such, the presence of DC offset will give rise to steady-state ripple in the estimated parameters. There are two main sources of DC offset. Firstly, DC offset can be introduced due to current transformation saturation [45]. Secondly, signal conversion process (analog to digital) can also introduce DC offset [43]. Since DC offset will introduce steady-state ripple, proper care needs to be taken to eliminate the effect of DC offset.

Many successful attempts have been made so far on adding DC offset rejection capability to grid synchronization techniques. Some of the commonly used approaches are: frequency adaptive pre-loop filtering [46–48], low-pass filtering [27, 43], delayed signal cancellation (DSC) operator [49], additional integrator-based DC offset estimation [50, 51], to name a few. Many of these techniques increase the overall system order by at least two and/or has large memory requirements. This increase the computational complexity of the overall closed-loop system. Moreover, parameter tuning can also be complicated. Out of the various techniques, low-pass filtering [27, 43] and additional integrator-based DC offset estimation [50] are two of the simplest technique available in the literature. Both techniques are first-order approach and has only one additional parameter to tune w.r.t. the standard approach i.e. without DC offset. However, tuning of the additional parameter is not straightforward.

In the case of low-pass filtering [27, 43], the tuning parameter is the filter cut-off frequency. Cut-off frequency

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needs to be selected as lower than the nominal frequency of the grid. Low cut-off frequency increase the convergence time and decrease the disturbance sensitivity. As such cut-off frequency needs to be selected as trade-off between the transient performance and sensitivity to disturbance. Additional integrator-based DC offset estimation [50] technique considers the DC offset as an additional state. This approach is commonly used in state-space filtering techniques as well e.g. Kalman filter. This approach also requires an additional tuning parameter that controls the convergence of the DC offset estimation error. If this approach is used in conjunction with other notch filter (e.g. SOGI), then the DC offset estimation gain needs to be significantly smaller than that of the notch filter gain. In the literature, the DC offset estimation tuning parameter is selected as approximately one-fifth or smaller than the notch filter gain. In the presence of additional integrator, obtaining an accurate small-signal model for the gain tuning of the closed-loop system (including proportional integral controller of the PLL) can be difficult.

To overcome the limitation of the simple DC offset rejection techniques, a novel approach is considered in this work. In the proposed approach, no low-pass filtering or additional integrator-based DC offset estimation are involved. Instead of considering the DC offset as an additional state, the orthogonal signal is considered as an additional state. This eliminates the need of any additional tuning gain similar to [50, 52, 53] or low-pass filtering similar to [27, 43]. Once the orthogonal signal is generated, then the frequency can be estimated using any standard approach available in the literature. Tuning gain or low-pass filtering free orthogonal signal generation can be considered as a significant improvement over the existing literature.

The main contribution of this paper is the novel computationally simple DC offset rejection technique. The proposed technique does not require any gain tuning unlike [50, 52, 53]. It is also free from any filtering unlike [27, 43]. The proposed technique has 1 gain to tune whereas PLL-based techniques have 4 and FLL-based techniques have 3 parameters to tune. This is an important advantage of the proposed technique over the existing literature.

The rest of this paper is organized as follows: Sec. 2 describes the development of the proposed technique. This Section also includes a short summary of two existing DC offset rejection techniques. Extension of the proposed technique to three-phase system is given in Sec. 3. Experimental results are discussed in sec. 4. Finally, Sec. 5 concludes this paper.

2. Simple DC Offset Rejection Technique Development

A single-phase grid voltage signal with DC offset can be written as:

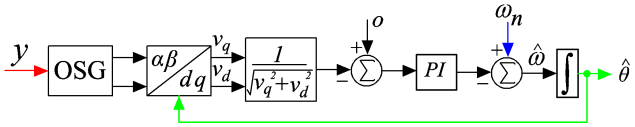


Figure 1: Basic overview of orthogonal signal generator-based single-phase PLL.

$$y = y_0 + A\sin\left(\underbrace{\omega t + \phi}_{\theta}\right) \tag{1}$$

where y_0, A, ω, ϕ, and θ are the DC offset, amplitude, angular frequency, initial phase-angle, and the instantaneous phase, respectively. In grid synchronization application, the problem is to estimate the unknown angular frequency ω and the instantaneous phase θ from the measured grid voltage signal y. The unknown frequency is typically modeled as $\omega = \omega_n + \Delta\omega$, where ω_n is the nominal frequency (typically $\omega_n = 100\pi$ or 120π) and $\Delta\omega$ is the deviation from the nominal frequency. When the grid voltage signal does not contain any DC offset, there are plenty of techniques available in the literature to estimate ω and θ. However, the presence of DC offset limits the applications of many of those techniques. In this Section, two simple techniques will be summarized that add DC offset rejection capability to grid synchronization algorithms.

2.1. Review of Two Existing Methods

2.1.1. Low-pass filtering-based DC offset rejection

Many single-phase PLL techniques rely on the idea of synchronous reference frame - PLL (SRF-PLL) [54]. However, SRF-PLL uses Park transformation that requires two signals that are orthogonal. Single-phase system has only one measured signal. To overcome this limitation, single-phase PLL employs orthogonal signal generator (*cf.* Fig. 1). However, in the presence of DC offset, traditional orthogonal signal generators (OSG) can not accurately generate the orthogonal signal resulting in estimation ripple in the estimated instantaneous phase and frequency. To overcome the effect of DC offset in second-order generalized integrator (SOGI)-type OSG, low-pass filtering (LPF) is first reported in [43]. Later on, some other modifications of this technique are also proposed in the literature e.g. [27]. Two demonstrate the working principle of this technique, let us consider the grid voltage signal $y = y_0 + A\sin(\theta)$ and its orthogonal signal $y^{\perp} = -A\cos(\theta)$. To estimate $y^{\perp}$ from y, SOGI takes the following form:

$$\dot{x}_1 = x_2\omega \tag{2a}$$

$$\dot{x}_2 = -x_1\omega + k\left(\underbrace{y - x_2}_{\varepsilon}\right)\omega \tag{2b}$$

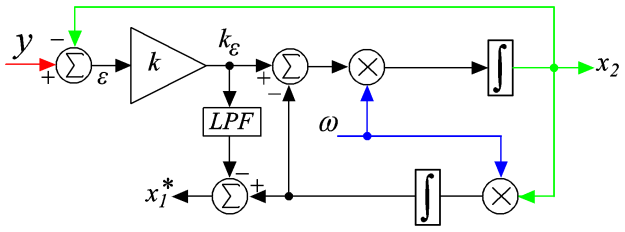


Figure 2: Low-pass filter-based DC offset rejection technique [43].

where x_1 and x_2 are the estimates of $y^\perp$ and y and $k_s > 0$ is the filter gain. When $y_0 = 0$, x_1 and x_2 asymptotically estimates $y^\perp$ and y as the feedback error term ε will converge to zero. However, in the presence of y_0, although x_2 will be able to estimate y, however, $x_1$will not be able to estimate exactly $y^\perp$. It will estimate $y^\perp$ with some offset. In the presence of y_0, the solution of x_1 can be written as:

$$\begin{aligned} x_1 &= \omega \int_0^t \underbrace{x_2(\tau)}_{\hat{y}(\tau)} d\tau \\ &= -A\cos(\theta) + \omega \int_0^t \hat{A}_0(\tau) d\tau \end{aligned} \tag{3}$$

Eq. (3) shows that x_1 is estimating $y^\perp$ with some offset. A simple low-pass filter can be used to eliminate the offset term from eq. (3). The block diagram of the LPF-based DC offset rejection technique applied to SOGI filter is given in Fig. 2. The transfer function of the filter can be chosen as $\text{LPF}(s) = \omega_c/(s+\omega_c)$, where ω_c is the cut-off frequency. Transfer functions of the estimated signals in this case are given below:

$$\frac{x_2}{y}(s) = \frac{k\omega s}{s^2 + k\omega s + \omega^2} \tag{4a}$$

$$\frac{x_1^\star}{y}(s) = \frac{-k\omega_c s^2 + k\omega^2 s}{s^3 + (k\omega + \omega_c)s^2 + (\omega^2 + k\omega\omega_c)s + \omega^2\omega_c} \tag{4b}$$

The gain of the transfer function (4b) is zero at $s = 0$ (i.e. the frequency of the offset term). As such the LPF can completely eliminate the DC offset at $x_1^\star$. However, in addition to the filter gain k, this technique introduces one more gain to tune which is the filter cut-off frequency. The cut-off frequency significantly affect the performance of this technique. Moreover, this technique can be prone to error due to high frequency harmonics.

2.1.2. Extended state-based DC offset rejection

This technique was first reported in [50]. In this case, the DC offset is considered as an additional state. To demonstrate the working principle of this technique, let us consider the state variables as $x_1 = -A\cos(\theta)$, $x_2 = A\sin(\theta)$, and $x_3 = y_0$. The following SOGI filter can be considered to estimate the orthogonal signal:

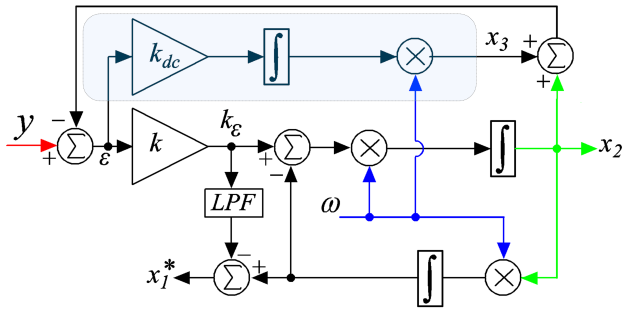


Figure 3: Extended state-based DC offset rejection technique [43].

$$\dot{x}_1 = x_2\omega \tag{5a}$$

$$\dot{x}_2 = -x_1\omega + k\,(y - x_2 - x_3)\,\omega \tag{5b}$$

$$\dot{x}_3 = k_{dc}(y - x_2 - x_3)\omega \tag{5c}$$

where k is SOGI gain and k_{dc} is the DC offset estimation gain. Block diagram of this technique is given in Fig. 3. The transfer functions in this case are given below:

$$\frac{x_1}{y}(s) = \frac{k\omega^2 s}{s^3 + (k + k_{dc})\omega s^2 + \omega^2 s + k_{dc}\omega^3} \tag{6a}$$

$$\frac{x_2}{y}(s) = \frac{k\omega s^2}{s^3 + (k + k_{dc})\omega s^2 + \omega^2 s + k_{dc}\omega^3} \tag{6b}$$

$$\frac{x_3}{y}(s) = \frac{k\omega(s^2 + \omega^2)}{s^3 + (k + k_{dc})\omega s^2 + \omega^2 s + k_{dc}\omega^3} \tag{6c}$$

From the transfer functions (6a) and (6b), one can see that both acts as a band-pass filter and x_1 introduces 90° phase-shift i.e. generates orthogonal signal. Similar to LPF-based technique, this technique has also one additional gain to tune w.r.t. standard SOGI filter. It is suggested in the literature that the gain k_0 should be chosen significantly smaller than k to obtain a trade-off between fast dynamic response and good transient performance. Moreover, when this filter will be used inside single-phase SRF-PLL (Fig. 1), tuning the closed-loop system (including PI controller gains) can be very complicated. In order to introduce a systematic gain-tuning procedure, first a small-signal model of the PLL system needs to be developed. To do this, time-domain solutions of the state variables x_1 and x_2 are to be obtained from eq. (6a) and (6b). However, by substituting the value of $y(s)$ in these equations, one get a fifth-order denominator polynomial. Obtaining the inverse Laplace solution of such a high-order polynomial is not straightforward. This limits the development of systematic design procedure. Moreover, tuning k and k_0 are also not straightforward.

2.2. Proposed Technique

The proposed technique uses state-space method. To develop the estimator, let us consider the state variables

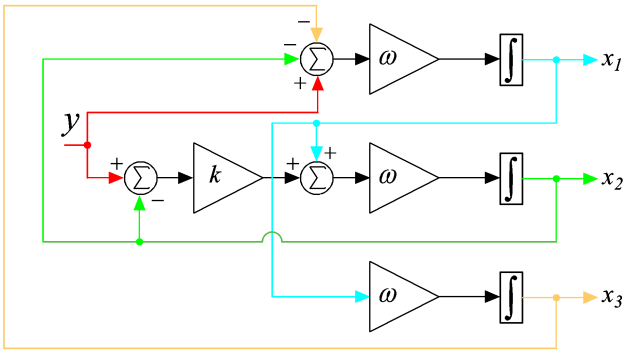


Figure 4: Proposed DC rejection capable orthogonal signal generator.

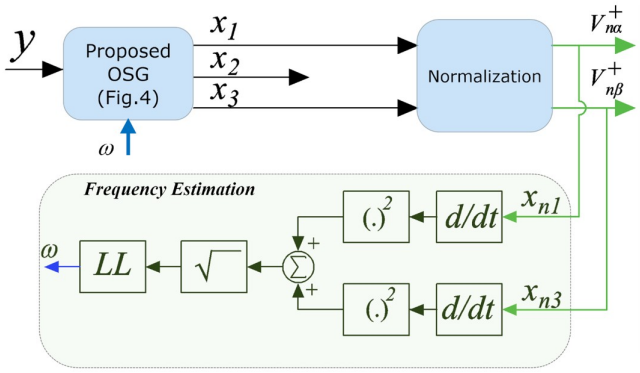


Figure 5: Block diagram of the proposed technique for a single-phase system.

as, $x_1 = -A\cos(\theta)$, $x_2 = y_0 + A\sin(\theta)$ and $x_3 = A\sin(\theta)$. Then the following estimator can be designed to generate orthogonal signal:

$$\dot{x}_1 = x_2\omega - (y - x_3)\,\omega \tag{7a}$$
$$\dot{x}_2 = -x_1\omega + k\,(y - x_2)\,\omega \tag{7b}$$
$$\dot{x}_3 = -x_1\omega \tag{7c}$$

where $k > 0$ is the tuning gain. Block diagram of the proposed orthogonal signal generator is given in Fig. 4. Unlike the reviewed techniques in Sec. 2.1, proposed technique has only one gain to tune. Its transfer functions are given below:

$$\frac{x_1}{y}(s) = \frac{-\omega s^2}{s^3 + k\omega s^2 + 2\omega^2 s + k\omega^3} \tag{8a}$$
$$\frac{x_2}{y}(s) = \frac{k\omega s^2 + \omega^2 s + k\omega^3}{s^3 + k\omega s^2 + 2\omega^2 s + k\omega^3} \tag{8b}$$
$$\frac{x_3}{y}(s) = \frac{\omega^2 s}{s^3 + k\omega s^2 + 2\omega^2 s + k\omega^3} \tag{8c}$$

From the transfer functions (8a) and (8c), it can be seen that they act as a band-pass filter and generates the orthogonal signal without any additional gain or low-pass filtering. As such, the proposed technique can be considered as a significantly simpler approach than similar other techniques reported in the literature.

2.2.1. Frequency estimation

The proposed technique requires the angular frequency of the grid voltage signal which is unknown in practice. To estimate that unknown frequency, a PLL or FLL can be connected to the proposed OSG as shown in Fig. 1. However, this will require the tuning of the PLL gains or the FLL gain. This necessitates the development of a small-signal model of the closed-loop system. To overcome this issue, derivative-based frequency estimation technique can be used. This type of approach is often used in various variants of open-loop grid synchronization technique e.g. [37, 38]. This approach will be considered here as well. State variables x_1 and x_3 can be directly used in estimating the frequency. However, this will make the convergence slower in the presence of voltage sag. This can be avoided by using normalization. Normalization will give two signals with unitary amplitude. The normalization process can be written as:

$$x_{n1} = \frac{x_1}{\sqrt{x_1^2 + x_3^2}} = -\cos(\omega t + \phi) \tag{9a}$$
$$x_{n3} = \frac{x_3}{\sqrt{x_1^2 + x_3^2}} = \sin(\omega t + \phi) \tag{9b}$$

By calculating the time-derivative of the normalized signals given in eq. (9), the following signals can be obtained:

$$\dot{x}_{n1} = \omega\sin(\omega t + \phi) \tag{10a}$$
$$\dot{x}_{n3} = \omega\cos(\omega t + \phi) \tag{10b}$$

Then the unknown frequency ω can be obtained by using the following formula:

$$\omega^2 = x_{n1}^2 + x_{n3}^2 \tag{11}$$

The frequency obtained through direct derivative estimation may show some fluctuations. A lead-lag smoother can be used to reduce the fluctuation. The following lead-lag filter is recommended in [38]:

$$LL(s) = \frac{1 + 5\times10^{-3}s}{1 + 20\times10^{-3}s} \tag{12}$$

Lead-lag filter (12) can be used if fluctuation reduction is required. An overview of the proposed grid synchronization scheme is given in Fig. 5.

3. Extension to Three-Phase Case

The proposed technique as developed in Sec. 2.2 can be easily applied to a three-phase system. For this purpose,

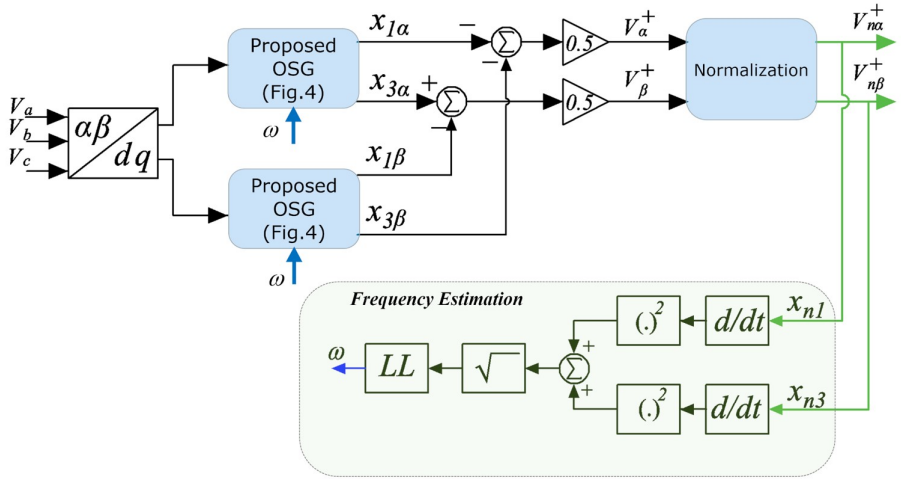


Figure 6: Block diagram of the proposed technique for a three-phase system.

let us consider the following unbalanced three-phase grid voltage signals with DC offset:

$$V_a = V_{a0} + V^+ \sin(\underbrace{\omega t + \phi^+}_{\theta^+}) + V^- \sin(\underbrace{\omega t + \phi^-}_{\theta^-}) \quad (13a)$$

$$V_b = V_{b0} + V^+ \sin(\theta^+ - \frac{2\pi}{3}) + V^- \sin(\theta^- + \frac{2\pi}{3}) \quad (13b)$$

$$V_c = V_{c0} + V^+ \sin(\theta^+ + \frac{2\pi}{3}) + V^- \sin(\theta^- - \frac{2\pi}{3}) \quad (13c)$$

where V^+ and V^- are the positive and negative sequence amplitudes, ϕ^+ and ϕ^- are the positive and negative sequence initial phase-angles, and V_{a0}, V_{b0}, V_{c0} are the DC offsets in phase a, b, and c, respectively. By applying the Clarke transformation [55], three-phase grid voltages as given in eq. (13) can be reduced to the following two signals:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \underbrace{\frac{2}{3}\begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix}}_{T_{\alpha\beta}} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (14)$$

$$V_\alpha = V_{\alpha 0} + \underbrace{V^+ \sin(\theta^+)}_{V_\alpha^+} + \underbrace{V^- \sin(\theta^-)}_{V_\alpha^-} \quad (15a)$$

$$V_\beta = V_{\beta 0} + \underbrace{V^- \cos(\theta^-)}_{V_\beta^-} - \underbrace{V^+ \cos(\theta^+)}_{V_\beta^+} \quad (15b)$$

where $V_{\alpha 0} = \frac{1}{3}(2V_{a0} - V_{b0} - V_{c0})$ and $V_{\beta 0} = \frac{1}{\sqrt{3}}(V_{b0} - V_{c0})$. In the case of unbalanced three-phase voltages, the objective is to estimate the positive sequence components (PSC) i.e. V_α^+ and V_β^+. The proposed technique can be used to extract the PSC from the unbalanced three-phase voltages. By passing V_α and V_β individually through the proposed orthogonal signal generator, the following signals can be obtained:

$$x_{1\alpha} = -V^+ \cos(\theta^+) - V^- \cos(\theta^-) \quad (16a)$$

$$x_{3\alpha} = V^+ \sin(\theta^+) + V^- \sin(\theta^-) \quad (16b)$$

$$x_{1\beta} = V^- \sin(\theta^-) - V^+ \sin(\theta^+) \quad (16c)$$

$$x_{3\beta} = V^- \cos(\theta^-) - V^+ \cos(\theta^+) \quad (16d)$$

From the signals obtained by eq. (16), the PSC can be calculated as:

$$V_\alpha^+ = \frac{x_{3\alpha} - x_{1\beta}}{2}, V_\beta^+ = -\frac{x_{1\alpha} + x_{3\beta}}{2} \quad (17)$$

Once the positive sequence components are obtained, the unknown frequency ω can be calculated using the same approach as described in Sec. 2.2.1. For this purpose, normalized signals need to be computed and are given below:

$$V_{n\alpha}^+ = \frac{V_\alpha^+}{\sqrt{V_\alpha^+ + V_\beta^+}} = \sin(\omega t + \phi^+) \quad (18a)$$

$$V_{n\beta}^+ = \frac{V_\beta^+}{\sqrt{V_\alpha^+ + V_\beta^+}} = \cos(\omega t + \phi^+) \quad (18b)$$

Then the time-derivative of the normalized signals can be computed as:

$$\dot{V}_{n\alpha}^+ = \omega \cos(\omega t + \phi^+) \quad (19a)$$

$$\dot{V}_{n\beta}^+ = -\omega \sin(\omega t + \phi^+) \quad (19b)$$

Finally, the unknown frequency can be computed as:

$$\omega^2 = \left(\dot{V}_{n\alpha}^+\right)^2 + \left(\dot{V}_{n\beta}^+\right)^2 \quad (20)$$

An overview of the proposed technique for the three-phase case is given in Fig. 6.

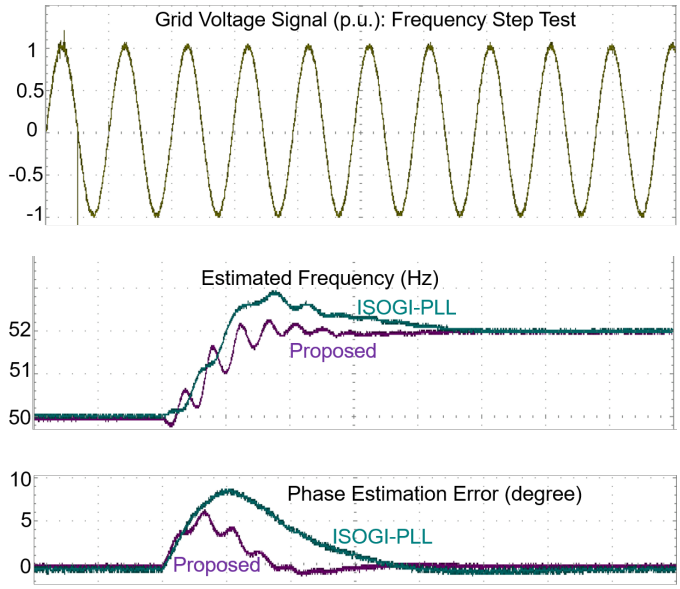


Figure 7: HIL experimental results for Test SP1: +2Hz frequency jump.

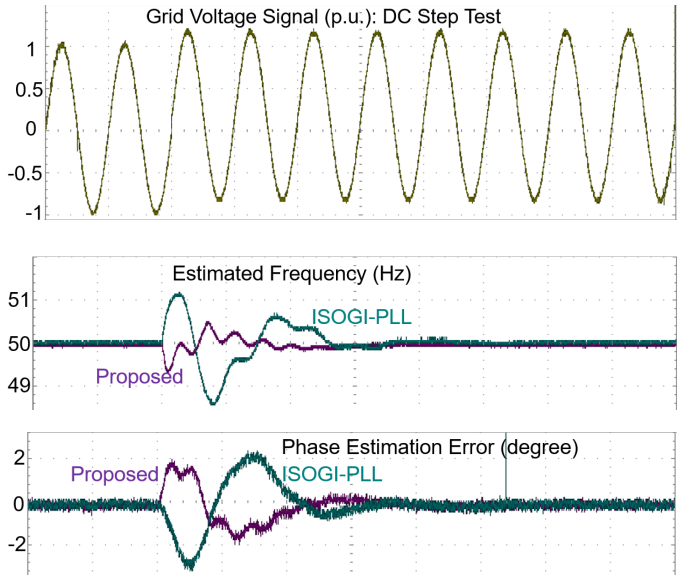


Figure 8: HIL experimental results for test case SP2: +0.15p.u. DC offset jump.

4. Results and Discussions

To verify the effectiveness of the proposed technique, in this Section experimental studies are considered. As a comparative technique, an improved extended SOGI PLL (as described in Sec. 2.1.2) [52, 53] is considered. Improved SOGI-PLL (ISOGI-PLL) parameters are chosen as: $k = \sqrt{2}$, $k_{dc} = 0.22$,$k_p = 4/t_s$, and $k_i = k_p^2/4\zeta^2$ where $t_s = 60$msec. and the damping ratio $\zeta = 1/\sqrt{2}$. The parameter of the proposed technique is selected as the same as improved SOGI-PLL i.e. $k = \sqrt{2}$. Both techniques are implemented in Matlab/Simulink with a sampling frequency of 10kHz and Trapezoidal method has been selected as the discretization technique for the continuous integrators.

4.1. Hardware-in-the loop Experimental Study

This section presents dSPACE 1104 board-based Hardware-in-the-loop (HIL) experimental study.

4.1.1. Single-Phase Grid Voltage

To test the performance of the proposed technique, four challenging test scenarios are considered in the single-phase case. The considered test-cases are:

- SP1:+2Hz frequency jump
- SP2: +0.15p.u. DC offset jump
- SP3: $+45^{\circ}$ phase jump
- SP4: -0.4p.u. voltage sag

Figure 7 shows the grid voltage signal, estimated frequencies, and the phase estimation errors for test case SP1. Results show that both techniques reacted very fast to

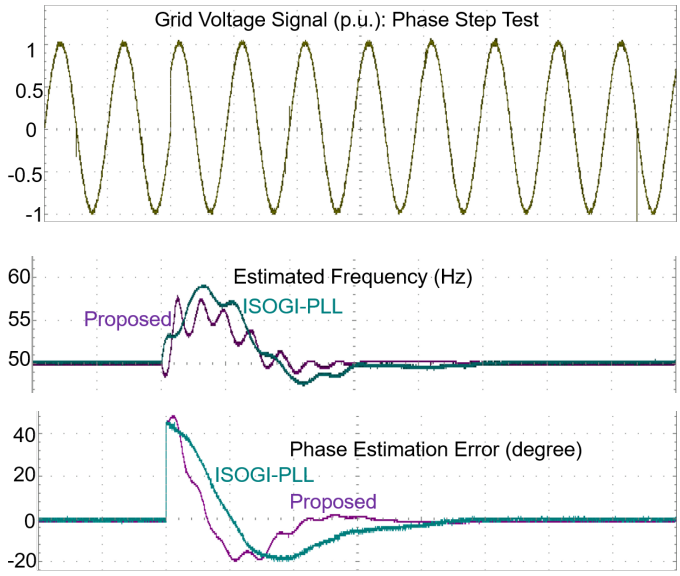


Figure 9: HIL experimental results for test case SP3: $+45^{\circ}$ phase jump.

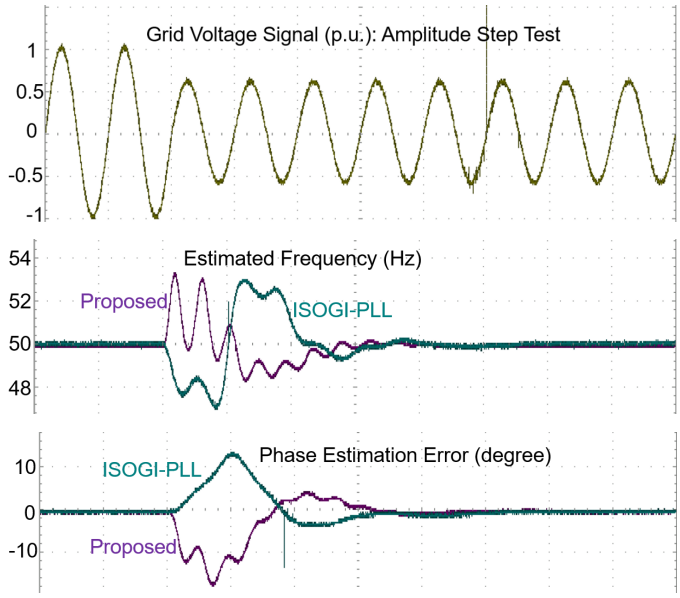


Figure 10: HIL experimental results for test case SP4: −0.4p.u. voltage sag.

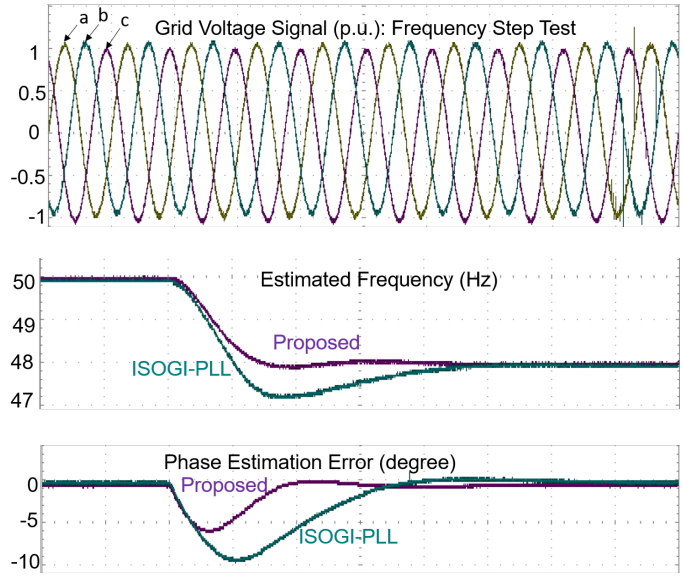


Figure 11: HIL experimental results for test case TP1: −2Hz frequency jump.

the change in grid frequency. By considering a steady-state band of ±0.1Hz, the proposed technique converged in ≈ 1.5 cycles while the ISOGI-PLL took ≈ 3 cycles. The proposed technique demonstrated insignificant peak overshoot, however, the same can not be said for ISOGI-PLL. ISOGI-PLLs convergence time can be reduced by selecting a lower settling time for the PI controller tuning. However, this will deteriorate the transient performance. Fast convergence of the frequency generally implies fast convergence for the instantaneous phase estimation error. This is clearly demonstrated in Fig. 7. The phase estimation error for the proposed technique converged in ≈ 1.5 cycles with peak overshoot of 6.2° while ISOGI-PLLs peak overshoot is 1.5 times of the proposed technique.

The next test considers DC offset. In this case, a DC offset of +0.15p.u. is suddenly added to the grid voltage signal. Figure 8 shows the grid voltage signal, estimated frequencies, and the phase estimation errors for the case SP2. Both techniques quickly detected the change in DC offset value and reacted accordingly. The frequency estimated by the proposed technique converged in ≈ 1.25 cycles with a peak overshoot of 0.48Hz while ISOGI-PLL converged in ≈ 2.5 cycles with a peak overshoot of 1.4Hz. This implies that the proposed technique converged two times faster with 67% less peak overshoot in frequency. The proposed techniques peak overshoot is 1.88° while for ISOGI-PLL the peak overshoot is 2.8° which is ≈ 1.5 times more than the proposed technique.

Due to fault in the grid, the phase-angle may experience sudden jump. This situation is considered in test case SP3 where the grid voltage's phase-angle suddenly experienced +45° jump. Figure 9 shows the grid voltage signal, estimated frequencies, and the phase estimation errors for test case SP3. The frequency estimated by the proposed technique converged in ≈ 3 cycles with a peak overshoot of 7.5Hz while ISOGI-PLL took ≈ 5 cycles with a peak overshoot of 8.8Hz. Phase estimation errors convergence times are similar to frequency estimation case. Experimental results as shown in Fig. 9 demonstrate the suitability of the proposed technique over ISOGI-PLL.

The final test case considers voltage sag. Figure 10 shows the grid voltage signal, estimated frequencies, and the phase estimation errors for test case SP4. Experimental results show that both techniques have similar peak overshoot in the frequency estimation case, however, the proposed technique converged faster. In the case of phase estimation error, both techniques have similar performances. It is to be noted here that the proposed technique has only one parameter to tune while ISOGI-PLL has two parameters to tune in the ISOGI part.

All the experimental results shown in this Section demonstrate the effectiveness and suitability of the proposed technique. The proposed technique either performed better or similar to ISOGI-PLL despite having only one parameter to tune.

4.1.2. Three-Phase Grid Voltages

In this Section, the performance of the proposed technique will be considered for a three-phase system. For this purpose, the following test cases are considered:

- TP1:−2Hz frequency jump
- TP2: −0.1p.u. DC offset in phase b and c.
- TP3: Balanced to unbalanced step test
- TP4: Harmonics step test

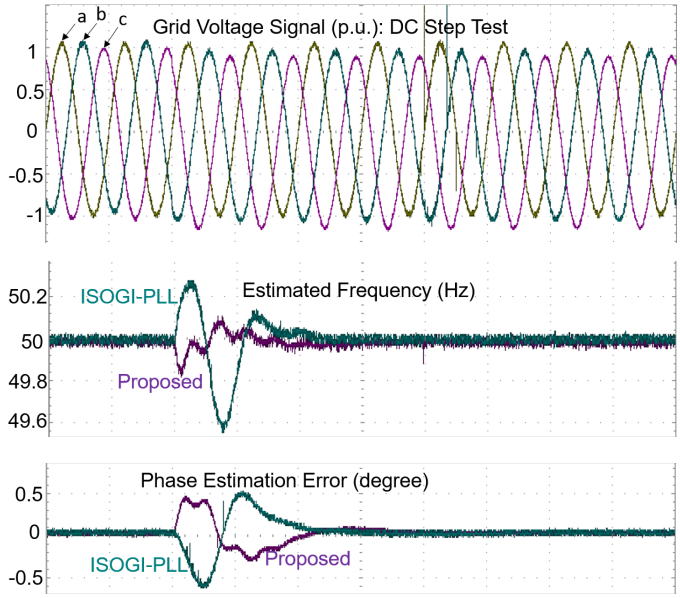


Figure 12: HIL experimental results for test case TP2: −0.1p.u. DC offset jump in phase b and c.

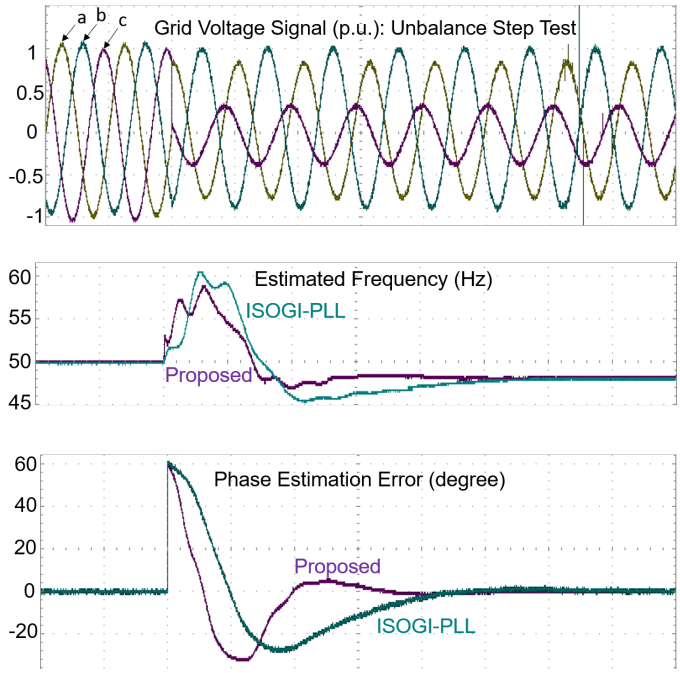


Figure 13: HIL experimental results for test case TP3: Balanced to unbalanced voltages step test.

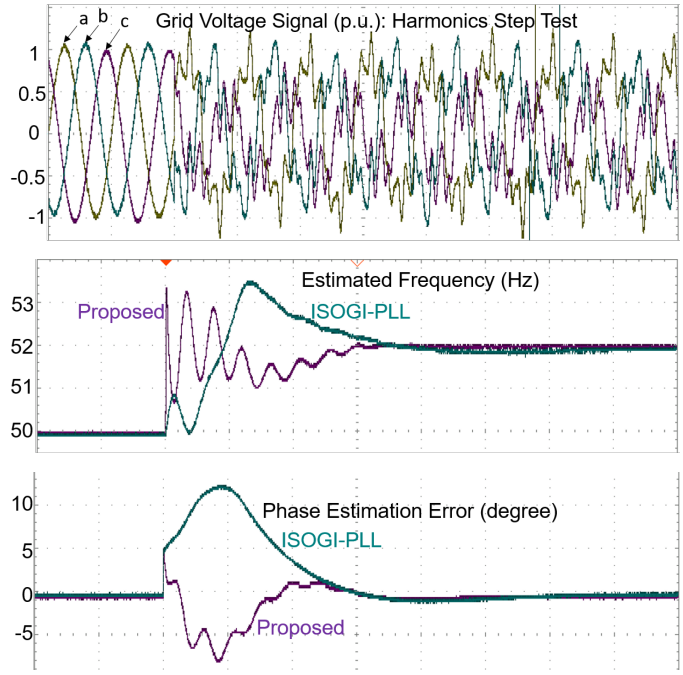


Figure 14: HIL experimental results for test case TP4: Harmonics step test.

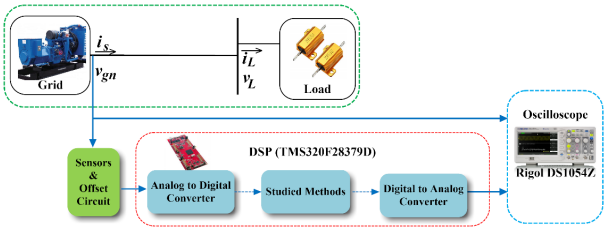
Figure 11 shows the grid voltage signal, estimated frequencies, and the phase estimation errors for the test case TP1. Results show that the frequency estimated by the proposed technique converged in ≈ 1.5 cycles with negligible overshoot. However, ISOGI-PLL took more than ≈ 3 cycles with ≈ 0.75Hz overshoot. As the proposed technique converged significantly faster than ISOGI-PLL, the phase estimation error by the proposed technique also converged significantly faster with lower peak overshoot w.r.t. ISOGI-PLL. As a result, it can be said that the proposed technique is not only easy to tune but also has fast convergence.

DC offset may not be avoided in many cases. The next test case considers sudden addition of DC offset to phase b and c while phase a remains unaffected. Figure 12 shows the grid voltage signal, estimated frequencies, and the phase estimation errors for test case TP2. The frequency estimated by the proposed technique permanently entered within the band ±0.1Hz within just 4msec. with a peak overshoot of only 0.14Hz. The frequency estimated by the ISOGI-PLL converged in ≈ 1.25 cycle with a peak overshoot of 0.4Hz. Since the estimated frequencies did not deviate much from the actual frequency, the phase estimation error also did not deviate much from the actual value. The proposed technique showed a peak overshoot of 0.4° while the peak overshoot of ISOGI-PLL is ≈ 1.5 times higher at $\approx 0.62^{\circ}$.

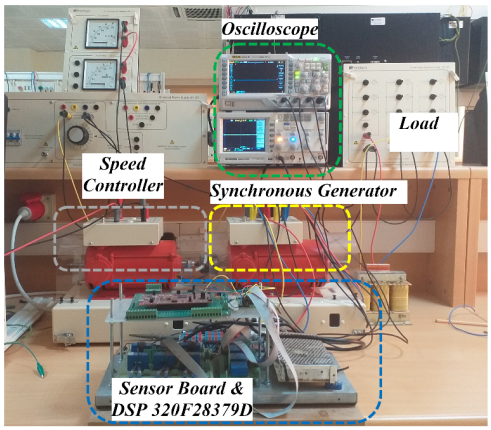
Unbalanced three-phase voltages are not that uncommon in power grid. As such any grid synchronization algorithm should be able to handle unbalanced voltages in three-phase system. Test case TP3 considers unbalanced

Table 1: Details of the distorted grid voltages used in test case TP4

Component	Magnitude (p.u.)	Phase
Positive sequence (50Hz)	0.711	5°
Negative sequence (50Hz)	0.232	50.1°
3^{rd} harmonics	0.15	40°
5^{th} harmonics	0.18	40°
7^{th} harmonics	0.17	180°
11^{th} harmonics	0.08	180°
Subharmonic (30Hz)	0.07	0°
Interharmonic (160Hz)	0.06	-45°



(a)



(b)

Figure 15: Considered experimental setup - (a) Block diagram of the experimental setup and (b) Experimental platform.

voltages. Initially, the grid voltages had only positive sequence component $V^{+} = 1\angle 0^{\circ}$. Suddenly, after the fault, negative sequence voltages are introduced in the grid. The post-fault grid voltages are comprised of positive sequence $0.65\angle 60^{\circ}$ and negative sequence $0.35\angle -40^{\circ}$. In addition, the frequency also jumped -2Hz. Figure 13 shows the grid voltage signal, estimated frequencies, and the phase estimation errors for test case TP3. Experimental results show that both techniques quickly detected the unbalanced voltages and the change in frequency. The frequency estimated by the proposed technique converged in ≈ 3 cycles while it is ≈ 5 cycles for ISOGI-PLL. Moreover, the peak frequency overshoot is also two times more for the ISOGI-PLL. These results show the effectiveness of the proposed technique in the case of unbalanced step test.

Harmonics is another important factor that may be unavoidable in some cases. Test case TP4 considers distorted grid voltages. Considered harmonics voltages are given in Table 1. In addition, frequency jump of $+2$Hz is considered as well. Figure 14 shows the grid voltage signal, estimated frequencies, and the phase estimation errors for test case TP4.Experimental results show that both techniques have similar convergence time for frequency estimation, however, the proposed technique has lower peak overshoot. The phase estimation error convergence time is also very similar for the comparative techniques, however, the peak overshoot is 7.3° for the proposed technique while it is 12.5° for ISOGI-PLL. This shows the performance improvement by the proposed technique in terms of peak overshoot.

All the experimental results presented in this Section show that similar to the single-phase case, proposed technique either performed better or similar to ISOGI-PLL in the three-phase case. This demonstrates the suitability and effectiveness of the proposed technique.

4.2. Experimental Study

The experimental setup used in this work is given in Fig. 15. To emulate the adverse grid voltage signal, a DC motor is coupled to the synchronous generator. Voltage at the load side is measured by a LEM LV25-P sensor. The experimental data of the grid voltage is processed by using a Texas Instruments TMS320F28335 digital signal processor. The sampling frequency is set to 10 kHz. The studied techniques are implemented in Simulink and embedded into the DSP by using Matlab2017b/Simulink and C2000 Code Generation Tools v6.0.0 software. The results are observed in a digital storage oscilloscope (Rigol DS1054Z) connected to Digital to Analog Converter (DAC) module.

In the first test, sudden change of -2Hz in frequency is considered. Experimental results in this case are given in Fig. 16 (a). They show that the proposed technique converged rapidly within 50msec. whereas ISOGI-PLL took 80msec. Moreover, ISOGI-PLL has significant peak overshoot compared to the proposed technique. It should be noted that the proposed technique is showing second-order response with peak overshoot. This was not the case in HIL experimental study. This is because the frequency change happened together with phase change as shown in the grid voltage signal of Fig. 16 (a).

In the second test, harmonics robustness of the two techniques are considered. In this test, the grid voltage is suddenly corrupted with harmonics. Experimental results in this case are given in Fig. 16 (b). They show that both techniques have similar performance in presence of harmonics. It is to be noted here that the proposed technique has 1 parameter to tune while ISOGI-PLL has 4.

5. Conclusions

This paper was dedicated to unknown grid frequency estimation in the presence of DC offset. A low-pass filtering or additional tuning parameter free simple technique

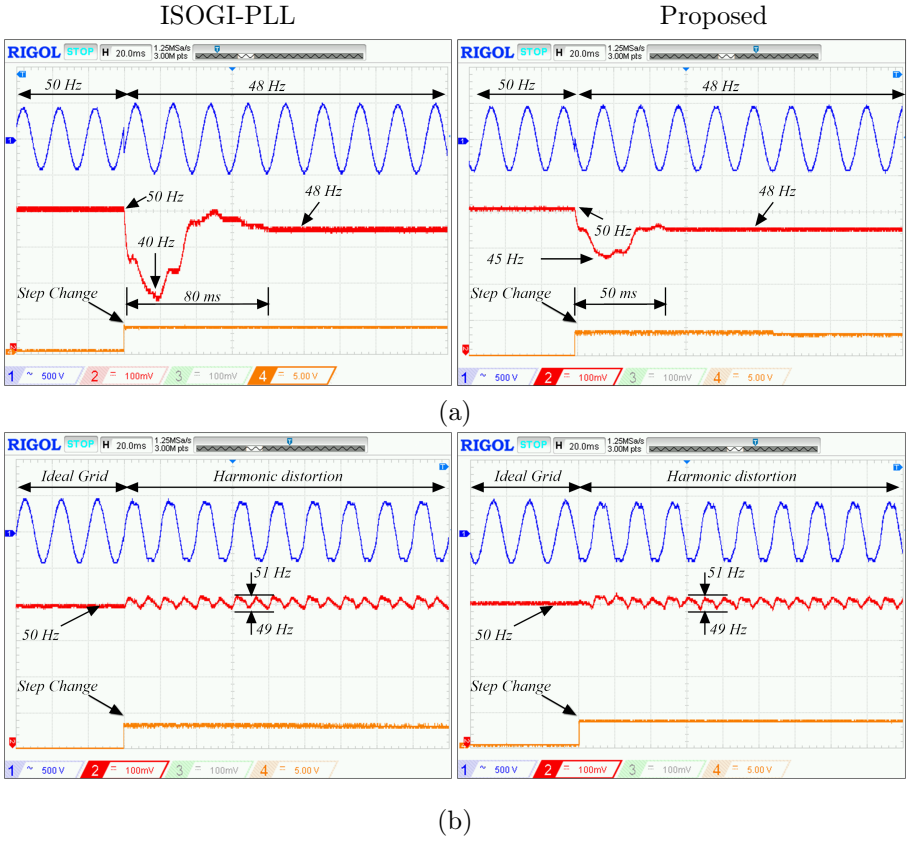


Figure 16: Experimental test results using the setup in Fig. 15: (a) Frequency step test and (b) Distorted grid voltage test.

was proposed for this purpose. The proposed technique has simple structure and overcome the tuning limitation of similar other techniques available in the literature. It is easy-to-implement and suitable for both single and three-phase grid voltages. Comparative experimental results demonstrated that the proposed technique performs either better or similar to another state-of-the-art technique without any additional tuning gain. This clearly demonstrates the suitability of the proposed technique.

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