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硕 士 学 位 论 文

基于Vivado HLS的时域有限差分算法硬件加速研究

Research on Acceleration Technology for FDTD Based on Vivado HLS

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摘 要

时域有限差分法(Finite difference time domain method，FDTD)是一种电磁学计算的基本方法，通过空间内电场和磁场的交替计算，得到整个研究空间的电磁分布情况。对于很多电磁学问题，不论从概念上还是可实现性上来讲，时域有限差分方法都是最简单的计算方法。时域有限差分法可以解决复杂的电磁计算问题，但同时要消耗大量的计算机资源，并且花费较长的计算时间。为了更快速高效地得到计算结果，可以利用硬件技术进行加速，这也是近年来FDTD方法研究领域比较受关注的部分。Xilinx公司新推出的高级综合工具Vivado HLS(High Level Synthesis)，直接通过C/C++语言开发硬件系统，根据算法模型自动生成时序，相比于传统的硬件工程师设计时序更加简单高效。

为了提高FDTD算法的计算速度，本文在仔细研究FDTD算法原理的基础上，从算法上分析了FDTD的速度瓶颈，使用HLS工具进行一维和二维的FDTD的优化设计，并进行了一维和二维算例验证，结果证明了方法的有效性和优势。本文的主要工作有：

首先，本文全面分析了FDTD算法的基本原理，推导了一维和二维FDTD算法的迭代公式。研究了吸收边界条件，着重介绍了PML边界条件，研究了FDTD算法的数值稳定性以及高级综合工具的多种优化策略。

其次，提出了一种流水的FDTD算法实现架构，将FDTD算法中的电场计算和磁场计算进行流水化，完成了一维和二维的FDTD算法C模型实现。针对提出的FDTD实现架构，使用HLS工具进行综合分析，通过调度和绑定，对算法在占用资源和处理速度方面进行优化：对数组添加 partition约束以提高数据访问速度，对循环体添加unroll约束以并行执行缩短时延，对循环添加pipeline约束建立循环流水线。最后通过HLS测试台工具进行RTL功能仿真验证，并应用MATLAB对仿真数据结果进行成像。

最后，选取一维和二维算例来验证所提出设计方法的正确性与高效性。结果表明，该设计具有较高的数据吞吐率，充分发挥了FPGA的并行、流水计算优势。同时该设计实现复杂度低，成本耗费低，在时域有限差分算法的硬件加速方面，具有很高的实际应用价值。

关键词：电磁计算；时域有限差分法；高级综合；硬件加速；现场可编程门阵列

Abstract

In the field of computational electromagnetics, finite difference time domain method (FDTD) has been widely used. Using FDTD, the electromagnetic distribution of the whole field is obtained by alternating calculation of the electric and magnetic field. For many electromagnetical computational problems, FDTD is the simplest method, in consideration of conception and achievability. Although FDTD can solve complex electromagnetic computational problems, it consumes substantial computer resources and plenty of time. To obtain fast and efficient results, hardware acceleration needs to be used. In recent years, researchers concern about combining hardware acceleration with FDTD in the research area of computational electromagnetics. Various methods have been proposed to improve the computing speed of FDTD. Recently Xilinx introduced a new advanced synthesis tool, Vivado High Level Synthesis (HLS), which develops hardware system through C/C++ Systems. Tools in HLS automatically generate timing according to the algorithms, which is much more simple and efficient compared to traditional hardware design.

To accelerate the calculation of FDTD algorithm, in this paper we analyze the computing bottleneck of FDTD based on some of the principle of it. We use HLS tools to optimize the design of one and two dimensional (1D/2D) FDTD, and verify the effectiveness and advantages of the method through a few examples. The main works of this paper are described as following:

First, we analyze the basic principle of FDTD algorithms and deduce the iterative formulas of the 1D/2D FDTD. We study the absorption boundary conditions (ABCs), and emphatically introduce the perfect matching layer (PML BCs). The numerical stability of the FDTD algorithm is discussed. Besides, the optimization strategies for synthesis are studied.

Secondly, we propose a pipelined FDTD algorithm architecture to realize the calculation of the electric and magnetic field. We discuss 1D/2D FDTD algorithm with C model. Based on the FDTD architecture, HLS tools are used to conduct the analysis. By scheduling and binding, we optimize the algorithm as follows: adding array partition constraints to improve data access speed, adding unroll constraints into the loop to shorten the latency, adding pipeline constraints into the loop to establish a pipeline structure. Besides, the RTL function simulation is carried out through testbenching and imaging the date result by using MATLAB. Finally, we optimize the 1D/2D FDTD examples to validate the correctness and efficiency of the proposed optimization programs. Our final results show that the method has a high data throughput and fully uses the parallel and pipeline computing advantages of FPGA. Besides, the design method has the characters of low complexity and low cost. Both aspects show practical applications in the hardware acceleration of the finite difference time domain method.

Keywords: Electromagnetic calculation; Finite difference time domain method; High level synthesis; Hardware acceleration; FPGA

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