A Closed-Loop Capacitance to Pulse-Width Converter for Single Element Capacitive Sensors

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Abstract — **A novel closed-loop capacitance-to-pulse width converter (CPC) suitable for single element capacitive sensors that use sinusoidal excitation is presented in this paper. Its operation is realized using a new configuration based on a simple, yet effective, auto-balancing scheme. The hardware prototype of the proposed CPC is relatively less complex to implement than those presented so far in the literature. It provides a quasi-digital output at a high update rate. Additionally, the output is insensitive to parasitic capacitances of the sensor. The output possesses high linearity, with respect to change in the sensor capacitance, ranging +/-5 pF, with a nominal capacitance as high as 200 pF. It exhibits a maximum non-linearity error of 0.061%FS. The output of the prototype has a resolution of 13.31 bits. Also, its response time for a step-change in the sensor capacitance is about 13 ms. This sophisticated and inexpensive closed-loop CPC is a perfect fit as an interfacing circuit for single element capacitive sensors.**

Keywords-Capacitance to pulse-width converter; Capacitive Sensor; Sinusoidal excitation; Closed-loop; Digitizer.

I. INTRODUCTION

Capacitive sensors have myriad applications in the fields ranging from consumer electronics to automobiles, healthcare, and automation [1]. They are used to measure displacement [2], acceleration [3], flow-rate [4], and humidity [5] and perform motion tracking [6]. The interfacing circuits that translate the change in the capacitance value to data in either an analogue or a digital domain, follow conversion paradigms that convert the sensor capacitance to either voltage [7], current [8], phase [9], frequency [10], time period [11][12] or pulse-width [13]. Choosing the appropriate conversion technique depends on factors such as the type of excitation source employed, the nature of the dielectric used in the sensor, desired resolution, and update rate.

Some capacitive sensors, such as the ones used to measure humidity [5] or evaluate agricultural biomass flow [13], require sinusoidal excitation to effectively sense the measurand. Circuits in [4], [5] and [14]-[18] which have used an ac excitation source, have not used a closed-loop configuration. However, the closed-loop approach enables the circuit to achieve higher accuracy, and update rate, compared to an open-loop configuration [19]. The circuits in [10] and [11], though designed as closed loops, are meant for differential and lossy capacitive sensors, respectively. In addition to this, these attempts have not explored the possibility of capacitance to pulse width conversion, which could be achieved with minimal components, keeping the complexity low. The few works that have adopted pulse width

modulation, based on the change in sensor capacitance, as the method of capacitance to digital conversion such as [13], [20] and [21] are not suitable for conversion of the output of a single element capacitive sensor connected to a sinusoidal excitation source. For instance, in [13] a square-wave is used instead of a sinusoidal excitation source, [20] uses a dc source and [21] neither uses a sinusoidal excitation source nor is designed for a single element capacitor. Also, these have not been designed as closed-loop circuits.

In this paper, a novel closed-loop capacitance-to-pulse width converter (CPC) for single element capacitive sensors is presented. The proposed circuit employs sinusoidal ac excitation to the sensor. It is based on an auto-balancing circuit configuration, providing an output in a quasi-digital format, which can be easily interfaced with digital systems [22]. The update rate possible in this approach is relatively high and the output is highly linear with respect to the change in the sensor capacitance. The output is insensitive to parasitic capacitance. The new CPC, its operation, simulation, and experimental results are presented in sequel.

II. CAPACITANCE TO PULSE-WIDTH CONVERTER

The circuit diagram of the proposed capacitance to pulse-width converter (CPC) is shown in Fig. 1. Here, the sensor capacitance C_x, feedback capacitor C_{F1} and opamp OA$_1$ constitute a charge amplifier. Similarly, the reference capacitance C_R, feedback capacitor C_{F2} and opamp OA$_2$ form another charge amplifier. The sinusoidal excitation signal $v_s = \sqrt{2}V_S sin\omega t$ is given to both C_x and C_R. $\omega = 2\pi f_s$, where f_s the frequency of excitation, and V_S is the root mean square (rms) voltage. The outputs v_{oi1} and v_{oi2} of the charge amplifiers, can be written as in (1).

$$v_{oi1} = -\frac{C_x}{C_{F1}}\sqrt{2}V_S sin\omega t \text{ and } v_{oi2} = -\frac{C_R}{C_{F2}}\sqrt{2}V_S sin\omega t \quad (1)$$

As in Fig. 1, v_S is also given to the non-inverting terminal of the comparator OC$_1$. Its output v_{c1} is high during the positive half cycles of v_S. It is low otherwise. v_{c1} controls the SPDT switches, S$_1$ and S$_2$. The inputs to S$_1$ are v_{oi1}, and inverted v_{oi1}. Similarly, v_{oi2} and $-v_{oi2}$ are the inputs to the switch S$_2$, as shown in Fig. 1. The output of S$_1$ is connected to another SPDT switch S$_3$, which is controlled by the feedback pulse signal, v_{c2}. The outputs of S$_3$ and S$_2$ are given to a summing integrator consisting of input resistors R_1 and R_2 ($R_1 = R_2 = R$), feedback capacitor C_{F3} and opamp OA$_3$. The output v_{oi3} of this integrator is connected to the non-inverting terminal of the comparator OC$_2$. It is compared with a
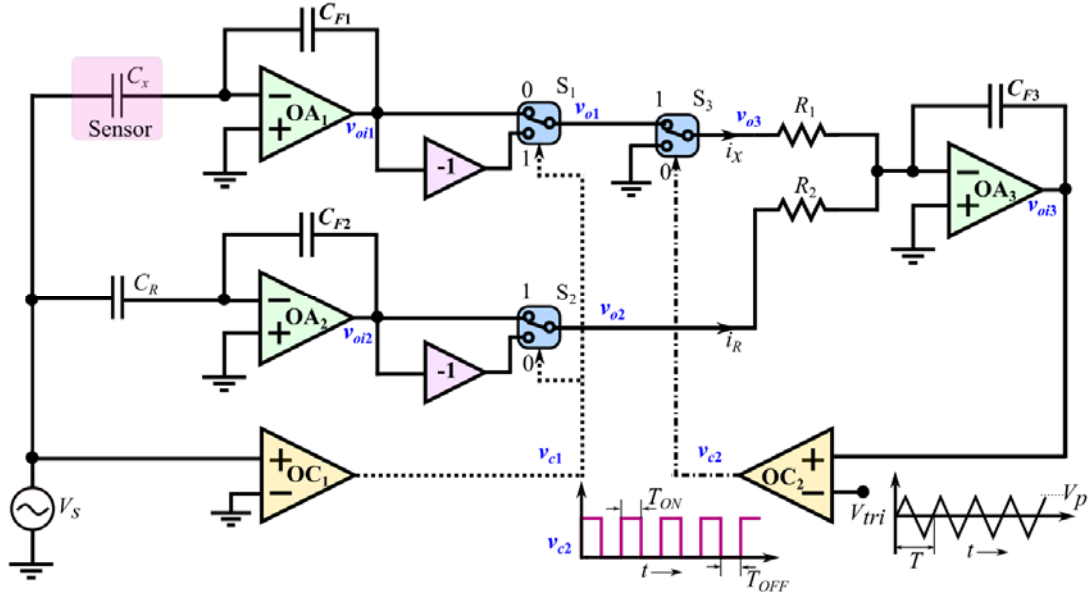
Fig. 1. Block diagram of the proposed capacitance to pulse-width converter. C_x is the sensor capacitance.

triangular signal V_{tri} with time period, $T = 1/f_{tri}$, and peak value V_p. v_{c2} is high for $V_{tri} < v_{oi3}$, and low otherwise. In the proffered CPC, $f_{tri} \gg f_s$. When $v_{oi3} = 0$, the pulse width of v_{c2} is $T/2$. As v_{oi3} increases in the positive direction, the duration T_{ON}, for which v_{c2} is high, increases, and the duration T_{OFF}, for which v_{c2} is low, decreases. The opposite occurs if v_{oi3} decreases from zero and goes negative.

A. *Theory of Operation*

In the proposed CPC, given in Fig. 1, the feedback capacitors C_{F1} and C_{F2} are chosen such that $C_{F2} = 2C_{F1}$, in order to have a duty cycle of 50 % when $C_x = C_R$. Initially, let $C_x = C_R$. Under this condition, output v_{o1} of S_1 and output v_{o2} of S_2 can be written as in (2).

$$v_{o1} = \left| \frac{C_x}{C_{F1}} \sqrt{2} V_S sin\omega t \right| \text{ and } v_{o2} = -\left| \frac{C_R}{2C_{F1}} \sqrt{2} V_S sin\omega t \right| \quad (2)$$

v_{o2} will drive a current i_R to the summing integrator as shown in Fig. 1. The average value, $\bar{i}_R$, of i_R for one cycle of v_S is

$$\bar{i}_R = \frac{1}{T_s} \int_0^{T_s} -\left| \frac{C_R}{2C_{F1}R_2} \sqrt{2} V_S sin\omega t \right| dt = -C_R k, \quad (3)$$

where $k = \frac{\sqrt{2} V_S}{\pi C_{F1} R_2}$ and $T_s = 1/f_s$.

The signal v_{o1} goes to one of the input terminals of S_3, which is controlled by v_{c2}. Output v_{o3} of S_3 is v_{o1}, whenever v_{c2} is high, and zero, otherwise. Thus, the average value, $\bar{i}_x$, of current i_x, shown in Fig. 1, for one cycle of v_S can be written as in (4). In (4), the duty cycle $D = T_{ON}/(T_{ON} + T_{OFF})$ and $T = (T_{ON} + T_{OFF})$.

$$\bar{i}_x = \frac{T}{T_s} \sum_{j=0}^{j=\frac{T_s}{T}} \frac{1}{T} \int_{jT}^{DT+jT} \left| \frac{C_x}{C_{F1}R_1} \sqrt{2} V_S sin\omega t \right| dt \quad (4)$$

As in (4), $\bar{i}_x$ is directly proportional to C_x. In addition, it is a function of D. For $D = 100\%$, the S_3 is always at position-1 and so, the waveform of v_{o3} will be the same as that of v_{o1}. For $D = 50\%$, since $T_s \gg T$, the v_{o3} waveform will be close to a digital to analog converter output waveform, following the absolute value of v_{o1} whenever v_{c2} is high and zero otherwise. This is illustrated in Fig. 2. If the top portions of each non zero segment of v_{o3} is assumed to be flat, the segments become rectangular blocks. This approximation will introduce negligible error for $T_s \gg T$. Under this condition, the average value of v_{o3} will vary proportional to D of v_{c2}. Thus, the value of $\bar{i}_x$ computed using (4) can be made directly proportional to D. This is illustrated in Fig. 3 which is computed by varying D, while maintaining a fixed value of C_x. It can be seen that the curve is linear once the condition $T_s \gg T$ is satisfied.

As indicated in Fig. 3, for the case $T_s \gg T$, $\bar{i}_x$ is directly proportional to D. It is a straight line passing through origin, with maximum value equal to $2C_R k$. For $D = 50\%$, $|\bar{i}_x| =$
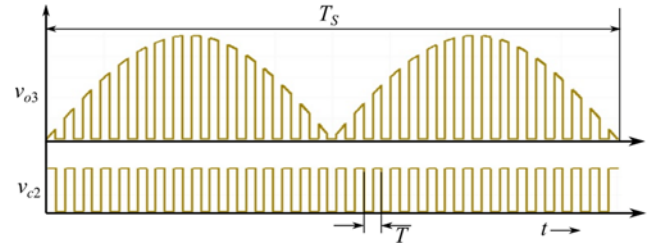

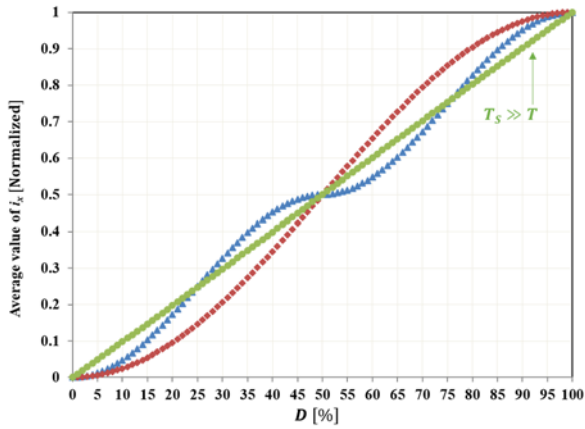Fig. 2. Output of switch S_3, for a v_{c2} with $D = 50\%$.

Fig. 3. Average value of i_x computed as per (4), for different values of D (in %) starting from 0 to 100 in steps of 1. It is a straight line for $T_s \gg T$. The relationship is non-linear otherwise as seen by the blue ($T_s = T$) and red ($T_s = 2T$) curves.

TABLE-I: PROTOTYPE

Component	Part/Value	Component	Part/Value
v_S	5 V$_{pp}$, Using AFG3022B	f_S	500 Hz
V_{tri}	Using AFG3022B	f_{tri}	10 kHz
$S_1 - S_3$	MAX4709	V_p	5 V
C_R	200 pF	OA_1 to OA_3	OP07
OC	LM311	C_{F1}	2 nF
R_1, R_2	100 kΩ	C_{F3}	1 nF

$2C_x kD = C_R k = |\overline{\iota_R}|$. In this condition, $v_{oi3} = 0$ and v_{c2} will be high for 50% of T. When $C_x > C_R$, initially $|\overline{\iota_x}| > |\overline{\iota_R}|$. This will drive v_{oi3} into negative side. Hence, T_{ON} of v_{c2} will decrease and T_{OFF} increase, decreasing D. This process will continue until $|\overline{\iota_x}| = -|\overline{\iota_R}|$ and v_{oi3} settles at a constant voltage. For $C_x < C_R$, the opposite occurs.

Since $\overline{\iota_x}$ is directly proportional to C_x and D, when C_x increases there will be a corresponding decrease in D, due to the negative feedback, to ensure that $|\overline{\iota_x}| = -|\overline{\iota_R}|$. Under this condition, $C_x 2D = C_R$. For a sensor with linear characteristic $C_x = C_O(1 \pm kx)$, where x is the measurand, k, the transformation constant of the sensor, and C_O, its nominal capacitance, keeping $C_O = C_R$, $C_x 2D = C_R$ can be rewritten as $(1 \pm kx)2D = 1$ for $D \neq 0$. Or $\pm kx$ can be expressed as in (5).

$$\pm kx = \frac{1}{2D} - 1 = \frac{T_{OFF} - T_{ON}}{2T_{ON}}. \tag{5}$$

The output signal v_{c2} can be given to a digital system, e.g., a timer module in a suitable microcontroller to measure the time T_{ON} and T_{OFF} and (5) can be computed in the digital system to get the digital value of the measurand kx. In certain application, the absolute value of C_x or the change ΔC_x in C_x will be required. C_x and ΔC_x can be obtained in terms of T_{ON} and T_{OFF} as given in (6) and (7) respectively.

$$C_x = \frac{C_R}{2D} = \left(\frac{C_R T}{2}\right)\frac{1}{T_{ON}} \tag{6}$$

$$\pm \Delta C_x = C_R \frac{T_{OFF} - T_{ON}}{2T_{ON}} \tag{7}$$

III. EXPERIMENTAL SETUP AND RESULTS

The prototype of the proposed CPC was realized using the components and ICs, given in Table-I, according to the circuit diagram in Fig. 1. C_x was emulated using a variable reference capacitor, with negligible leakage conductance. The entire system was powered by ±10 V power supply. During the experiment, the important waveforms of the prototype were observed using a digital oscilloscope. A screenshot of the oscilloscope is shown in Fig. 4. v_{o2}, v_{o3}, v_{oi3} and v_{c2}

corresponding to $C_x > C_R$, are visible in Fig. 4. Since $C_x > C_R$, the amplitude of the v_{o3} is higher than that of v_{o2}. This causes v_{oi3} to be negative and thus, $T_{ON} < T_{OFF}$.

A. Testing the Linearity and Accuracy

In order to test the linearity, the prototype was operated with C_R = 200 pF and C_x was varied from 195 pF and 205 pF in steps of 1 pF. For each value of C_x, the T_{ON} and T_{OFF} were measured using the 32-bit timer module of microcontroller ATSAM3X8E, from Atmel. This was also simultaneously measured and verified using an oscilloscope. The duty cycle, D, in each case was determined. The plot of C_x/C_R vs $1/2D$ is given in Fig. 5. The relationship between these two was observed to be highly linear, with the maximum non-linearity error (NLE) being 0.061%FS, also indicated in Fig. 5. The output has high accuracy, with the maximum percentage error being 0.062%FS.

B. Testing the SNR, Resolution, and Repeatability

The tests to ascertain the signal-to-noise ratio (SNR), the resolution (in terms of effective number of bits (ENOB)) and the repeatability, were conducted by setting C_x = 150 pF, recording the output of the CPC for 50 consecutive measurements, followed by using the appropriate formulae given in Table-II. The results are presented in the same table.
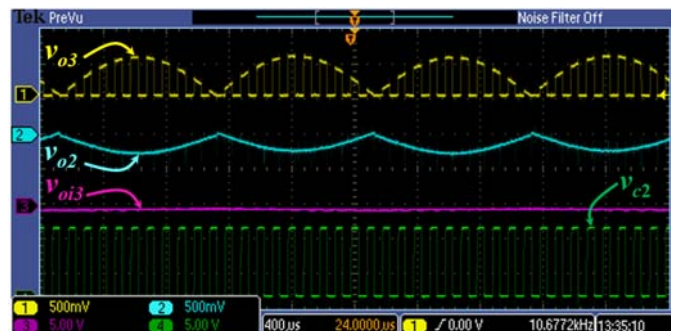
C. Rise Time

Fig. 4. Screenshot of the oscilloscope showing the important waveforms from the prototype developed. The frequency of V_s was set at 500 Hz, and that of V_{tri} was set at 10 kHz while recording this waveform.
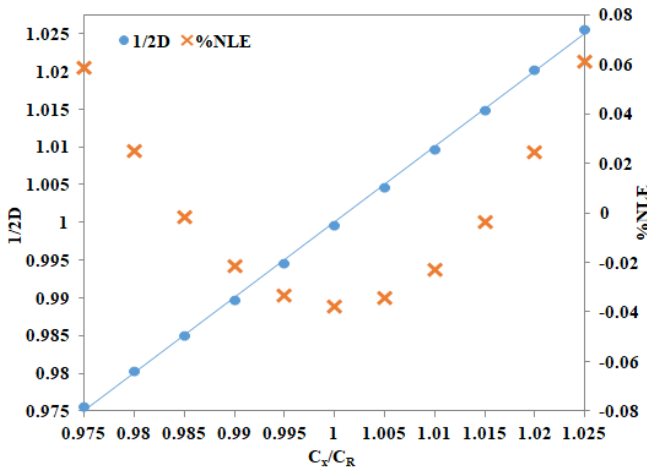
Fig. 5. Results obtained on testing the prototype CPC. The observed percentage non-linearity error (NLE) for each measurement is also shown.

In order to determine the rise time of the proposed CPC a new capacitance, $C_{new} = 68$ pF, was introduced in parallel to C_x and then removed using an SPDT switch controlled by a signal v_{sw}. C_x was fixed to 200 pF. C_{new} was added to C_x, when v_{sw} was low, and removed when v_{sw} was high. v_{oi3} goes to a negative value when C_{new} is added, because $C_x > C_R$, and returns to zero when C_{new} is removed as then $C_x = C_R$. The screenshot of the oscilloscope indicating v_{sw} and v_{oi3} is given in Fig. 6. The time taken for v_{oi3} to rise from 10% to 90% of its final value was found to be 13 ms.

TABLE-II: REPEATABILITY STUDY

Parameter	Formula	Value
Signal-to-noise ratio (SNR)	$SNR = 10\ log\ \dfrac{\sum_{i=1}^{M} X(i)^2}{\sum_{i=1}^{M}[X(i) - \bar{X}]^2}$	81.88 dB
Resolution (ENOB), n bits	$n = \dfrac{(SNR - 1.76)}{6.02}$	13.31 bits
Repeatability, d	$d = \dfrac{\Delta_{rmax}}{C_u - C_l} \times 100\%$	0.018%

$X(i) = i^{th}$ measurement

$\bar{X}$ = average value of the measured data

M = total number of measurements recorded for the repeatability study

C_u = upper limit of measurement range of CPC

C_l = lower limit of measurement range of CPC

Δ_{rmax} = maximum difference between repeated measurements

Fig. 6. Screenshot of the oscilloscope showing v_{sw} and v_{oi3}, during the test conducted to measure the rise time.

IV. CONCLUSION

A novel closed loop capacitance to pulse-width converter (CPC) is presented in this paper. This is suitable for single element capacitive sensors with sinusoidal excitation. The proposed CPC is designed based on an auto-balancing scheme. It provides a quasi-digital output, which is insensitive to parasitic capacitance, at an update rate of 10 kHz. The update rate can be further increased by increasing the frequency f_{tri} of the triangular waveform. The results from the hardware prototype developed and tested showed high linearity with a percentage non-linearity error of 0.061%FS, with respect to the sensor capacitance varied by +/-5 pF, with an offset or nominal capacitance 200 pF. The CPC does not use any expensive components or ICs and yet, provided a resolution of 13.31 bits (ENOB). The response time was in the range of 13 ms. The proffered simple and inexpensive closed-loop CPC is an efficient interfacing scheme for capacitive sensors in applications such as proximity sensing [17], humidity [5], flow rate [13] and displacement measurements [23].

V. ACKNOWLEDGMENTS

VI. REFERENCES

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