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Practical Submodule Capacitor Sizing for Modular Multilevel Converter Considering Grid Faults

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Abstract: Submodule (SM) capacitors are key elements in the modular multilevel converter (MMC), the design of which influences the entire system performance. In practical cases, SM capacitor sizing must consider the abnormal system operation (e.g., grid faults). In order to find a clear design boundary for SM capacitors, a practical capacitor sizing method is presented for the first time in this paper, considering the grid-fault-ride-through operation of the MMC, impact of MMC control system, and aging mechanism of capacitors. The SM capacitor rated voltage, capacitance, ESR, thermal resistance, and lifetime can be decided to ensure reliable operations of the MMC during grid faults. The effectiveness of the proposed method has been verified through experimental tests on a down-scale MMC system.

Keywords: modular multilevel converter (MMC); submodule capacitor design; grid faults; transient state; reliability

1. Introduction

Several commercial modular multilevel converter (MMC) projects have been deployed in the past few decades [1–3]. Compared with the traditional line-commutated converter (LCC), the MMC has many competitive advantages, e.g., low switching frequency, high conversion efficiency, strong scalability and reduced harmonic distortion [4–9]. As a key part in the MMC, the SM capacitors must achieve high reliability in industrial projects, due to their high-voltage and high-power operating environment. Moreover, according to the national grid code shown in [10], the ability of grid-fault-ride-through is required for grid-tied MMCs. Especially in countries such as Germany and Canada, the converters must stay connected to the grid when a 100% voltage dip [11,12] appears. These unexpected grid fault operation will bring extra voltage stress on SM devices (IGBTs and capacitors), which is one of the critical reasons leading to system-level failure [13–16]. To avoid this problem, the SM capacitor is normally over-designed in practical cases, causing the rise of size and cost of the overall system. Thus, an optimized SM capacitor sizing method considering grid fault conditions is necessary for the practical MMC design.

Some efforts have been devoted to the SM capacitor sizing to ensure the steady-state operation of MMCs [17–20]. For instance, an SM capacitor sizing method is given in [17], based on the energy storage requirement of each SM. Dimensioning of SM capacitors considering energy fluctuation, ripple voltage is given in [18]. The minimum size for the SM capacitors to keep their voltage fluctuation is given in [19]. A computational design procedure in the aspects of maximum SM voltage, SM ripple voltage, and current stress is given in [20], considering the impact of the modulation index and the instantaneous power output. However, these methods assume that the system operates in steady-state

with normal grid conditions, which cannot be used to predict the SM voltage during grid faults. To solve this problem, the control method of the MMC under unbalanced grid conditions is discussed in [21] and the literature [22] gives the mathematical model of the SM voltage, considering the positive- and negative-sequence of grid voltages and the MMC arm currents.

The above solutions can be used for SM capacitor sizing when the system operates in steady-state. However, the SM voltage is also affected by other factors, such as control strategies, modulation methods, circuit configurations, etc. For instance, the impact of the circulating current suppresion control (CCSC) on SM capacitor voltage ripples under different unbalanced AC grid conditions is discussed in [23]. With a second-order circulating current control [24], the SM voltage ripple can be reduced, i.e., a lower SM capacitance is required. An improved DC-loop regulator is proposed in [25] to suppress the capacitor voltage fluctuations. Considering unbalanced grid conditions, the DC-link voltage ripple is regulated through an arm voltage feed-forward control [26]. The interaction between the MMC modulation methods and the SM voltage stress is discussed in [27]. By applying a power decoupling circuit to each SM, the voltage ripple can be suppressed [28]. Hence, the sizing of SM capacitor should take the system control schemes into consideration.

In addition, the SM capacitor sizing should also consider the transient state of the MMC during grid faults, which may induce catastrophic damage to the SM. To study the transient behavior of MMC system, a few literature works have been conducted [16,29,30]. A time-domain transient SM voltage analysis is shown in [16]. By taking the grid current control into account, the transient SM voltage response during grid faults is discussed in [29]. In Ref. [30], the transient response of CCSC and its impact on SM voltage are analyzed.

Considering the impact factors above, the aim of this paper is ensure the reliability of SM capacitors when the system operates both in normal and grid fault states. Thus, a practical SM capacitor sizing method is proposed in this paper. Accordingly, the SM capacitor rated voltage and capacitance are chosen based on the grid fault operation principle of the MMC, including the transient voltage stress on SM. Moreover, the ESR, thermal resistance, and rated lifetime of the SM capacitor is chosen considering the aspect of reliability requirement. The rest of this paper is structured as follows: Section 2 discusses the operation principles and control schemes of the MMC system. The transient state SM voltage is analyzed in Section 3, where an analytical model is proposed. Design considerations of the MMC system are provided in Section 4, while the SM capacitor selection procedure is given in Section 5. A detailed design example of a down-scale MMC system is given in Section 6, where experimental tests are performed to validate the proposed method. Finally, concluding remarks are presented.

2. Steady-State Analysis of SM Capacitor Voltage

A three-phase MMC topology is shown in Figure 1. Each arm of the MMC contains N identical half-bridge SMs and one series-connected arm inductor L_a. The SM is formed by two IGBTs and a parallel SM capacitor C_{sm}. The SM voltage v_{sm} is defined as the voltage across each SM capacitor, while the DC-bus voltage is considered as a constant denoted by V_{dc}.The AC output of the MMC is connected to the grid through a three-phase Δ/Y transformer. Thus, there will not be any zero-sequence currents on the converter side during grid fault conditions.

To simplify the analysis, it is assumed that the voltage across each SM is well-balanced. Thus, an equivalent circuit can be derived for each phase-leg of the MMC, as shown in Figure 2. All the SMs in each arm are combined into a single equivalent capacitor being $C_{eq} = C_{sm}/N$. The equivalent capacitors hold the total voltage stress of the upper arm v_{uj} and lower arm v_{lj}, where j indicates the phase ($j = a, b, c$). The switching devices of each SM are replaced by a pair of equivalent controlled-sources. The grid phase voltage and output current of each phase are represented by v_j and i_j. The circulating current is denoted as i_{cj}. The insertion index of the upper and lower arms is represented by n_{uj} and n_{lj}, while the arm current is defined as i_{uj} and i_{lj}. Due to the symmetrical characteristic of the MMC system, only the expression of upper arm is given.

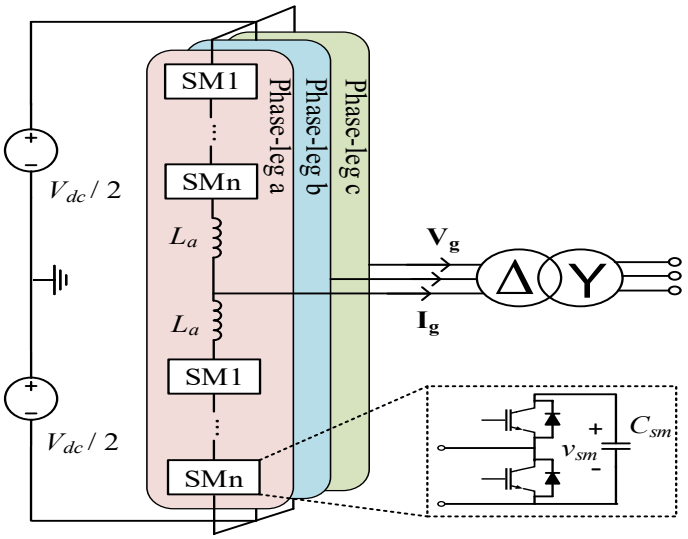


Figure 1. Schematic of a three-phase modular multilevel converter.

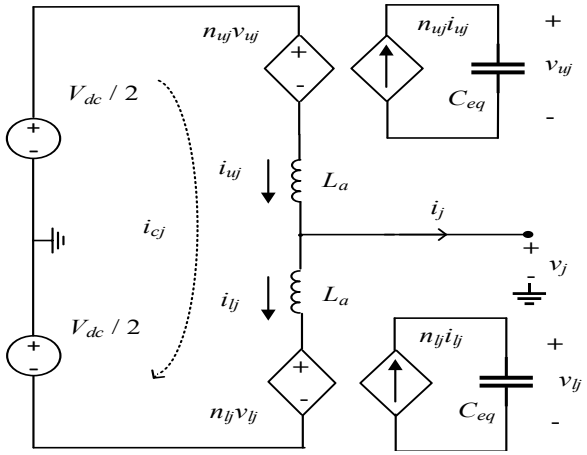


Figure 2. Equivalent circuit of each phase-leg of the MMC.

In steady-state, the grid voltage and current of each phase can be expressed as

$$v_j = \hat{V}_j \cos(\omega_1 t) \tag{1}$$

$$i_j = \hat{I}_j \cos(\omega_1 t - \phi_j) \tag{2}$$

where ω_1 is the fundamental line frequency, ϕ_j is the power factor angle, and $\hat{V}_j$ and $\hat{I}_j$ are the peak value of grid voltage and current.

The total energy variation of the upper arm is analyzed in [17] with

$$e_{uj} = \frac{C_{sm}V_{dc}^2}{2N} + \frac{V_{dc}\hat{I}_j}{16\omega_1}[4\sin(\omega_1 t - \phi_j) - m\sin(2\omega_1 t - \phi_j) - 2m^2\sin(\omega_1 t)\cos(\phi_j)] \tag{3}$$

where m is the modulation index, given by $m = 2\hat{V}_j / V_{dc}$.

Meanwhile, the energy storage in the upper arm can be represented as

$$e_{uj} = \frac{1}{2}C_{eq}v_{uj}^2 = \frac{1}{2}NC_{sm}v_{sm}^2 \tag{4}$$

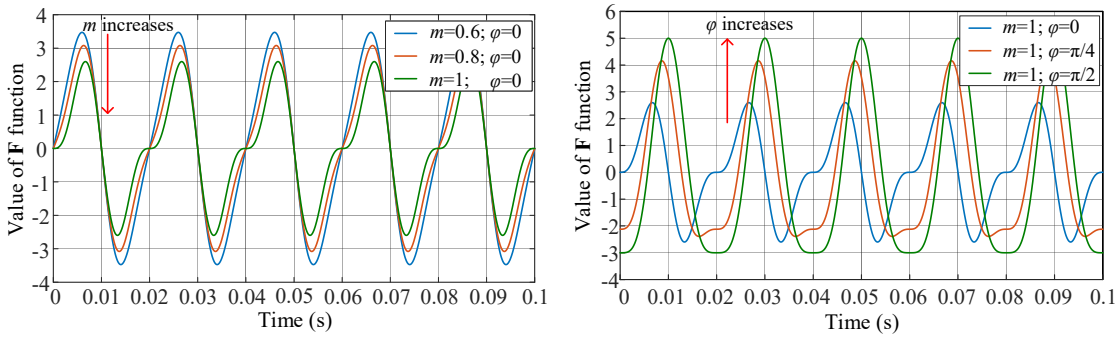
Combining Equations (3) and (4), the voltage stress of an SM capacitor in the upper arm can be given as

$$v_{smj} = \sqrt{\frac{V_{dc}^2}{N^2} + \frac{V_{dc}\hat{I}_j}{8NC_{sm}\omega_1}\mathbf{F}} \tag{5}$$

where

$$\mathbf{F} = 4\sin(\omega_1 t - \phi_j) - m\sin(2\omega_1 t - \phi_j) - 2m^2\sin(\omega_1 t)\cos(\phi_j) \tag{6}$$

To study the steady-state SM voltage ripple, the waveform of **F** function under different operating point is shown in Figure 3. Hence, the operating voltage boundary of SM capacitors in steady-state can be obtained as



(**a**) (**b**)

Figure 3. Waveforms of the **F** function with (**a**) $\phi = 0$, m = 0.6, 0.8, 1 and (**b**) m = 1, $\phi = 0, \pi/4, \pi/2$.

$$V_{ssmax} = \sqrt{\frac{V_{dc}^2}{N^2} + \frac{V_{dc}\hat{I}_j}{8NC_{sm}\omega_1}\mathbf{F}_{max}} \tag{7}$$

$$V_{ssmin} = \sqrt{\frac{V_{dc}^2}{N^2} + \frac{V_{dc}\hat{I}_j}{8NC_{sm}\omega_1}\mathbf{F}_{min}} \tag{8}$$

where $\mathbf{F}_{max}$ and $\mathbf{F}_{min}$ are the maximum and minimum value of the **F** function.

3. Transient SM Capacitor Voltage during Grid Faults

3.1. System Dynamics and Control Schemes

Based on Figure 2, the dynamics of an MMC can be described as

$$L_a\frac{di_{cj}}{dt} = \frac{V_{dc}}{2} - v_{cj} \tag{9}$$

$$\frac{L_a}{2}\frac{di_j}{dt} = v_{sj} - v_j \tag{10}$$

$$C_{eq}\frac{dv_{uj}}{dt} = n_{uj}i_{uj} \tag{11}$$

$$i_{uj} = i_{cj} + \frac{1}{2}i_j \tag{12}$$

where v_{cj} is the voltage driving the circulating current through each phase-leg, and v_{sj} is the differential voltage controlling the current injected into the grid. Accordingly, v_{cj} and v_{sj} are given as

$$v_{cj} = \frac{n_{uj}v_{uj} + n_{lj}v_{lj}}{2} \tag{13}$$

$$v_{sj} = \frac{-n_{uj}v_{uj} + n_{lj}v_{lj}}{2} \tag{14}$$

By applying the Park transformation on Formula (10), the output current dynamic can be described in the dq-frame as

$$\frac{L_a}{2}\frac{d}{dt}\begin{bmatrix} i_{d+} \\ i_{q+} \end{bmatrix} = \begin{bmatrix} v_{sd+} \\ v_{sq+} \end{bmatrix} - \begin{bmatrix} v_{d+} \\ v_{q+} \end{bmatrix} + \frac{L_a}{2}\begin{bmatrix} 0 & \omega_1 \\ -\omega_1 & 0 \end{bmatrix}\begin{bmatrix} i_{d+} \\ i_{q+} \end{bmatrix} \tag{15}$$

$$\frac{L_a}{2}\frac{d}{dt}\begin{bmatrix} i_{d-} \\ i_{q-} \end{bmatrix} = \begin{bmatrix} v_{sd-} \\ v_{sq-} \end{bmatrix} - \begin{bmatrix} v_{d-} \\ v_{q-} \end{bmatrix} + \frac{L_a}{2}\begin{bmatrix} 0 & -\omega_1 \\ \omega_1 & 0 \end{bmatrix}\begin{bmatrix} i_{d-} \\ i_{q-} \end{bmatrix} \tag{16}$$

where v_{sd+}, v_{sq+}, v_{sd-}, and v_{sq-} are the positive- and negative-sequence components of v_{sj} in the *dq*-frame.

According to Equations (15) and (16), a typical output control loop can be constructed for the MMC as shown in Figure 4. A positive-sequence control and a negative-sequence control using PI regulators are adopted, where K_{op} and K_i are the gains. The positive- and negative-sequence components of the grid voltage can be extracted with methods in [31] and used as the input of a grid current reference generator, which is applied to provide the active and reactive current references (i^*_{d+}, i^*_{q+}, i^*_{d-}, i^*_{q-}) for the controller.

According to Equation (14), a circulating current suppression control (CCSC) of the MMC can be designed as shown in Figure 5 [14]. A PR controller is applied to eliminate the dominant double-line frequency ripple in the circulating current, where K_{cp} and K_r represent its gains. The DC reference of the circulating current control will be given by a circulating current reference generator.

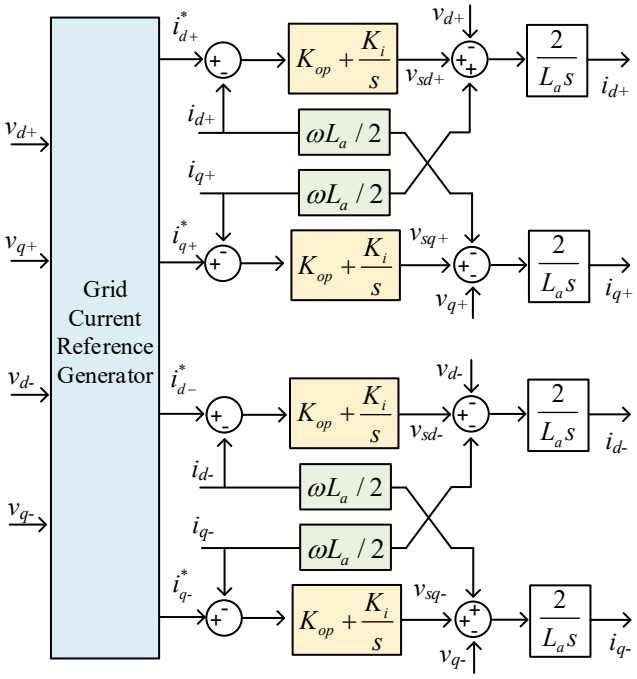


Figure 4. Positive- and negative-sequence current control of the MMC.

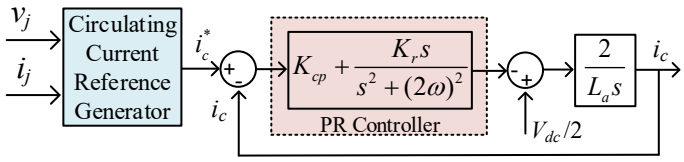


Figure 5. The circulating current control of the MMC.

3.2. Grid Fault SM Voltage Estimation

Based on the dynamics of the SM voltage shown in Equation (11), the SM voltage stress of each phase-leg is governed by the arm currents (i_{uj} and i_{lj}) and its insertion indexes (n_{uj} and n_{lj}). According to Equation (12), the arm currents are composed of the circulating current and phase output current.

As shown in Figure 4, the state functions of the positive current sequence can be represented as

$$\dot{\mathbf{X}} = \mathbf{AX} + \mathbf{BU} \tag{17}$$

where

$$\dot{\mathbf{X}} = \begin{bmatrix} \dot{i}_{d+} & \dot{i}_{q+} & \dot{\alpha}_{d+} & \dot{\alpha}_{q+} \end{bmatrix}^{\mathrm{T}}$$

$$\mathbf{A} = \begin{bmatrix} -\frac{2K_{op}}{L_a} & \omega_1 & K_i & 0 \\ -\omega_1 & -\frac{2K_{op}}{L_a} & 0 & K_i \\ -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix}$$

$$\mathbf{X} = \begin{bmatrix} i_{d+} & i_{q+} & \alpha_{d+} & \alpha_{q+} \end{bmatrix}^{\mathrm{T}}$$

$$\mathbf{B} = \begin{bmatrix} K_{op} & 0 & -1 & 0 \\ 0 & K_{op} & 0 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}$$

$$\mathbf{U} = \begin{bmatrix} i^*_{d+} & i^*_{q+} & v_{d+} & v_{q+} \end{bmatrix}^{\mathrm{T}}$$

in which $\alpha_{d+} = i^*_{d+} - i_d$ and $\alpha_{q+} = i^*_{q+} - i_q$.

According to Formula (17), the transfer functions of the positive-sequence current can be written as $\mathbf{X}(s) = \mathbf{CU}$ with matrix $\mathbf{C} = (s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B}$. Based on this method, the transfer functions of output current control can be represented as

$$\begin{cases} i_{d+}(s) = H_1(s)i^*_{d+} + H_2(s)i^*_{q+} - H_3(s)v_{d+} - H_4(s)v_{q+} \\ i_{q+}(s) = -H_2(s)i^*_{d+} + H_1(s)i^*_{q+} + H_4(s)v_{d+} - H_3(s)v_{q+} \\ i_{d-}(s) = H_1(s)i^*_{d-} - H_2(s)i^*_{q-} - H_3(s)v_{d-} + H_4(s)v_{q-} \\ i_{q-}(s) = H_2(s)i^*_{d-} + H_1(s)i^*_{q-} - H_4(s)v_{d-} - H_3(s)v_{q-} \end{cases} \tag{18}$$

in which $H_1(s)$, $H_2(s)$, $H_3(s)$, $H_4(s)$ are given in Formula. (19), respectively:

$$\begin{cases} H_1(s) = \dfrac{K_{op}L_a^2s^3 + (2K_{op}^2L_a + K_iL_a^2)s^2 + (K_{op}K_iL_a^2 + 2K_{op}K_iL_a)s + K_i^2L_a^2}{L_a^2s^4 + 4K_{op}L_as^3 + (4K_{op}^2 + L_a^2\omega_1^2 + 2K_iL_a^2)s^2 + 4K_{op}K_iL_as + K_i^2L_a^2} \\ H_2(s) = \dfrac{K_{op}\omega_1L_a^2s^2 + K_i\omega_1L_a^2s}{L_a^2s^4 + 4K_{op}L_as^3 + (4K_{op}^2 + L_a^2\omega_1^2 + 2K_iL_a^2)s^2 + 4K_{op}K_iL_as + K_i^2L_a^2} \\ H_3(s) = \dfrac{L_a^2s^3 + 2K_{op}L_as^2 + K_iL_a^2s}{L_a^2s^4 + 4K_{op}L_as^3 + (4K_{op}^2 + L_a^2\omega_1^2 + 2K_iL_a^2)s^2 + 4K_{op}K_iL_as + K_i^2L_a^2} \\ H_4(s) = \dfrac{L_a^2\omega_1s^2}{L_a^2s^4 + 4K_{op}L_as^3 + (4K_{op}^2 + L_a^2\omega_1^2 + 2K_iL_a^2)s^2 + 4K_{op}K_iL_as + K_i^2L_a^2} \end{cases} \tag{19}$$

Meanwhile, the dynamic response of the circulating current can be derived according to Figure 5:

$$i_{cj}(s) = \frac{K_{cp}s^2 + K_rs + 4K_{cp}\omega_1^2}{L_as^3 + K_{cp}s^2 + (K_r + 4L_a\omega_1^2)s + 4K_{cp}}i^*_{cj} \tag{20}$$

$$v_{cj}(s) = \frac{K_{cp}L_as^3 + K_rL_as^2 + 4K_{cp}L_a\omega_1^2s}{L_as^3 + K_{cp}s^2 + (K_r + 4L_a\omega_1^2)s + 4K_{cp}}i^*_{cj} \tag{21}$$

To describe the system dynamics during grid faults, Table 1 indicates the operation point of the MMC system during normal state and grid fault conditions. By applying the reverse Laplace transformation on Equation (18), the time-domain transient response of the system in the *dq*-frame can be obtained as

Table 1. Quiescent operation point of the MMC.

Normal Operation Point	Grid Fault Operation Point
$v_{d+\_normal} = V_{d+}$	$v_{d+\_fault} = V'_{d+}$
$v_{q+\_normal} = 0$	$v_{q+\_fault} = V'_{q+}$
$v_{d-\_normal} = 0$	$v_{d-\_fault} = V'_{d-}$
$v_{q-\_normal} = 0$	$v_{q-\_fault} = V'_{q-}$
$i^*_{d+\_normal} = I_{d+}$	$i^*_{d+\_fault} = I'_{d+}$
$i^*_{q+\_normal} = 0$	$i^*_{q+\_fault} = I'_{q+}$
$i^*_{d-\_normal} = 0$	$i^*_{d-\_fault} = I'_{d-}$
$i^*_{q-\_normal} = 0$	$i^*_{q-\_fault} = I'_{q-}$
$i^*_{cj\_normal} = I_{cj}$	$i^*_{cj\_fault} = I'_{cj}$

$$\begin{cases} i_{d+\_tran}(t) = I_{d+} + \mathcal{L}^{-1}[i_{d+}(s)] \\ i_{q+\_tran}(t) = \mathcal{L}^{-1}[i_{q+}(s)] \\ i_{d-\_tran}(t) = \mathcal{L}^{-1}[i_{d-}(s)] \\ i_{q-\_tran}(t) = \mathcal{L}^{-1}[i_{q-}(s)] \\ i_{cj\_tran}(t) = \mathcal{L}^{-1}[i_{cj}(s)] \\ v_{cj\_tran}(t) = \mathcal{L}^{-1}[v_{cj}(s)] \end{cases} \tag{22}$$

where the input of the system can be regarded as a series of step signals in the s-domain

$$\begin{cases} i^*_{d+}(s) = \dfrac{I'_{d+} - I_{d+}}{s} \\ i^*_{q+}(s) = \dfrac{I'_{q+}}{s} \\ i^*_{d-}(s) = \dfrac{I'_{d-}}{s} \\ i^*_{q-}(s) = \dfrac{I'_{q-}}{s} \\ v_{d+}(s) = \dfrac{V'_{d+} - V_{d+}}{s} \\ v_{q+}(s) = \dfrac{-V'_{q+}}{s} \\ v_{d-}(s) = \dfrac{-V'_{d-}}{s} \\ v_{q-}(s) = \dfrac{-V'_{q-}}{s} \\ i^*_{cj}(s) = \dfrac{I'_{cj} - I_{cj}}{s} \end{cases} \tag{23}$$

According to [32], the dynamics of the output current can be calculated as

$$\begin{aligned} i_{j\_tran}(t) = {} & i_{d+\_tran}\cos(\omega_1 t - \varphi_j) + i_{q+\_tran}\sin(\omega_1 t - \varphi_j) \\ & + i_{d-\_tran}\cos(\omega_1 t + \varphi_j) + i_{q-\_tran}\sin(\omega_1 t + \varphi_j) \end{aligned} \tag{24}$$

By applying the direct modulation [33], the insertion indexes of the upper and lower arms can be calculated as

$$n_{uj\_tran} = \frac{v_{cj\_tran} - v_{j\_fault}}{V_{dc}} \tag{25}$$

$$n_{lj\_tran} = \frac{v_{cj\_tran} + v_{j\_fault}}{V_{dc}} \tag{26}$$

According to Equation (11), the dynamic response of the total SM voltage can be obtained as

$$v_{uj\_tran} = v_{uj}(t_0) + \frac{1}{C_{eq}} \int (i_{cj\_tran} + \frac{1}{2} i_{j\_trans}) n_{uj\_tran} \tag{27}$$

$$v_{lj\_tran} = v_{lj}(t_0) + \frac{1}{C_{eq}} \int (i_{cj\_tran} - \frac{1}{2} i_{j\_trans}) n_{lj\_tran} \tag{28}$$

where t_0 is the initial time of the grid fault. As the voltage across each SM in the same arm is assumed to be balanced, the voltage stress on each SM can be given as

$$v_{smuj\_tran}(t) = \frac{v_{uj\_tran}(t)}{N} \tag{29}$$

Thus, the maximum SM voltage stresses during the grid fault transient can be predicted as

$$V_{tmax} = \max[v_{smuj\_tran}(t), v_{smlj\_tran}(t)] \tag{30}$$

4. Design Consideration of SM Capacitors

4.1. Energy Storage Requirement

According to [17], the energy stored in each arm of the MMC must be larger than the required energy by the grid. In steady-state, the required inserted voltage for the upper arm can be expressed as

$$v_{uj\_req} = \frac{V_{dc}}{2} - v_j \tag{31}$$

By substituting Equation (31) into (5), the energy requirement of SM capacitor can be given as

$$e_{uj} \geq \frac{1}{2N} C_{sm} (\frac{V_{dc}}{2} - v_j)^2 \tag{32}$$

By taking Equation (3) into (32), the required SM capacitance for each phase-leg can be obtained as

$$C_{sm\_enj} \geq \max\{\frac{2NV_{dc}\hat{I}_j}{16\omega_1[(\frac{V_{dc}}{2} - v_j)^2 - V_{dc}^2]}\mathbf{F}\} \tag{33}$$

4.2. SM Ripple Voltage Requirement

To ensure the stability and efficiency of the MMC, the SM voltage ripple must be kept in a safe range during steady-state operation. Defining the allowable peak-to-peak voltage ripple as V_{rip}, the following condition should be satisfied:

$$V_{ssmax} - V_{ssmin} \leq V_{rip} \tag{34}$$

Solving Equation (34) yields the minimum capacitance requirement as

$$C_{sm\_ripj} \geq \frac{V_{dc}\hat{I}_j(\mathbf{F}_{\max} - \mathbf{F}_{\min})}{8N\omega_1 V_{rip}^2} \tag{35}$$

4.3. Transient SM Voltage Constraint

For industrial MMC projects, a series of protection strategies are embedded in the control system to avoid switching devices (e.g., IGBTs) getting over-stressed. Once the operating SM voltage reaches a preset threshold V_{th}, the SM will be bypassed by the control blocks [34]. If a large amount of SMs get over-charged at the same time, a system-level shutdown may be triggered. Thus, the transient SM voltage V_{tmax} must be constrained under the threshold V_{th}, which can be written as $V_{tmax} < V_{th}$.

By substituting Equations (27) and (28) into the equation, it can be obtained as

$$C_{sm\_tj} \geq \frac{\max[\int (i_{cj\_tran} + \frac{1}{2}i_{j\_trans})n_{uj\_tran}]}{V_{th} - \max[\frac{v_{uj}(t_0)}{N}]} \tag{36}$$

$$C_{sm\_tj} \geq \frac{\max[\int (i_{cj\_tran} - \frac{1}{2}i_{j\_trans})n_{lj\_tran}]}{V_{th} - \max[\frac{v_{lj}(t_0)}{N}]} \tag{37}$$

It should be noted that the maximum transient SM voltage for upper and lower arms can be different during grid faults. The selected SM capacitance should fulfill the Equations (49) and (50) in the meantime.

4.4. ESR, Thermal Resistance, and Lifetime Assessment

To ensure a long-term reliable operations of the MMC, the thermal stresses of SM capacitors must be evaluated. According to [35], a simple lifetime model of SM capacitors can be given as

$$L_{life} = L_0 \times \left(\frac{V_{dc}}{NV_{rated}}\right)^{-\delta} \times 2^{\frac{T_0 - T_h}{10}} \tag{38}$$

where L_0 is the lifetime of the capacitor under rated voltage V_{rated} and testing temperature T_0; the exponent δ is normally selected from 7 to 9.4 for metallized polypropylene film (MPPF) capacitor; T_h is the operating hot-spot temperature of the capacitors.

In order to study the thermal behavior of the SM capacitors, a lumped thermal model of film capacitors are given in Figure 6 [36], where the steady-state hot-spot temperature of capacitors can be expressed as

$$T_h = R_{th}P_{loss} + T_a \tag{39}$$

The thermal resistance of the capacitor R_{th} relates to the material of the capacitor. T_a is the ambient temperature, P_{loss} is the power losses of the SM capacitor.

By neglecting the harmonics on the circulating current, the SM capacitor charging current can be decomposed by a fundamental line frequency component and a double-line frequency component, which can be expressed as [37]

$$i_{smj} = \beta_{\omega 1}\hat{I}_s + \beta_{\omega 2}\hat{I}_s \tag{40}$$

$$\beta_{\omega_1} = \frac{1}{8}[2\cos(\omega_1 t - \varphi_j) - m^2\cos(\omega_1 t)\cos(\varphi_j)] \tag{41}$$

$$\beta_{\omega_2} = -\frac{m}{8}[\cos(2\omega_1 t - \varphi_j)] \tag{42}$$

With different modulation index and phase angle, the RMS value of β_{ω_1} is shown in Figure 7, while the RMS value of β_{ω_2} equals $m/(8\sqrt{2})$. Thus, the power losses for SM capacitors can be calculated as

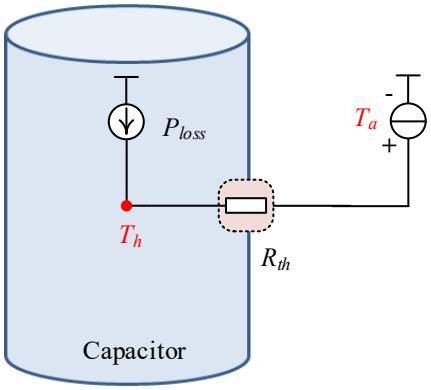


Figure 6. A lumped thermal model of SM capacitors.

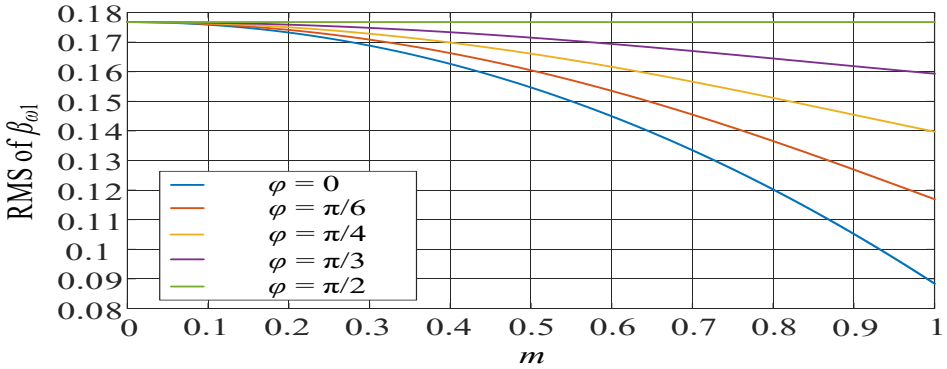


Figure 7. The RMS value of β_{ω_1} at different operating points.

$$P_{loss} = (R_{esr\_\omega 1} \times \beta^2_{\omega 1\_rms} + R_{esr\_\omega 2} \times \beta^2_{\omega 2\_rms})\hat{I}_s^2 \tag{43}$$

where $R_{esr\_\omega 1}$ is the equivalent-series-resistance (ESR) of the SM capacitor under fundamental line frequency, $R_{esr\_\omega 2}$ is the ESR under double line frequency.

5. SM Capacitor Selection

5.1. SM Capacitance Selection

According to Equations (33), and (35)–(37), the design boundary of the SM capacitance can be obtained. Considering the capacitance losses caused by aging of capacitors [38], an extra design margin must be guaranteed. Thus, the SM capacitance can be chosen as

$$sC_{sm} = \eta \times \max(C_{sm\_enj}, C_{sm\_ripj}, C_{sm\_tj}) \tag{44}$$

where η is the redundancy factor of SM capacitance selection. Normally, η is chosen from 1.2 to 2.

5.2. Rated Voltage Selection

According to characteristics of film capacitors [39], the peak value of the operating voltage must not exceed their rated DC voltage. Thus, the rated voltage of the SM capacitor can be chosen as

$$V_{rated} \geq \max(V_{ss\,\max}, V_{t\,\max}) \tag{45}$$

where the maximum voltage stress on SM capacitors can be calculated according to Equations (10) and (38)–(42).

5.3. Design Flowchart

Based on the analysis above, a design procedure flowchart is shown in Figure 8. First, some basic parameters are required, which includes the DC-link voltage (V_{dc}), number of SMs in each arm (N), arm inductance (L_a), AC-side fundamental angular frequency (ω_1), gain of the MMC control loops (K_{op}, K_{cp}, K_i, and K_r) allowable peak-to-peak SM voltage ripple (V_{rip}), maximum SM voltage threshold (V_{th}), expected SM capacitor lifetime (L_{exp}), and system operating points in normal and grid fault conditions. Then, the minimum SM capacitance that satisfies the energy storage, voltage ripple, and transient SM voltage requirements can be calculated using the Equations (33) and (35)–(37). After that, the SM capacitance C_{sm} can be decided by adding a proper redundancy to the highest value among C_{sm_enj}, C_{sm_ripj}, C_{sm_tj}. Based on the selected capacitance, the rated voltage of SM capacitor V_{rated} can be obtained using Formula (45). Since the capacitance and rated voltage have been decided, a certain type of capacitor product can be selected in the market. In the end, the lifetime of the selected capacitor product needs to be checked using Equations (38) and (43). It should be noted that the MMC system may encounter different fault conditions. Thus, this design process may be conducted multiple times based on different grid fault operating points. Through comparison, the maximum calculation value of C_{sm} and V_{rated} can be chosen as the final result.

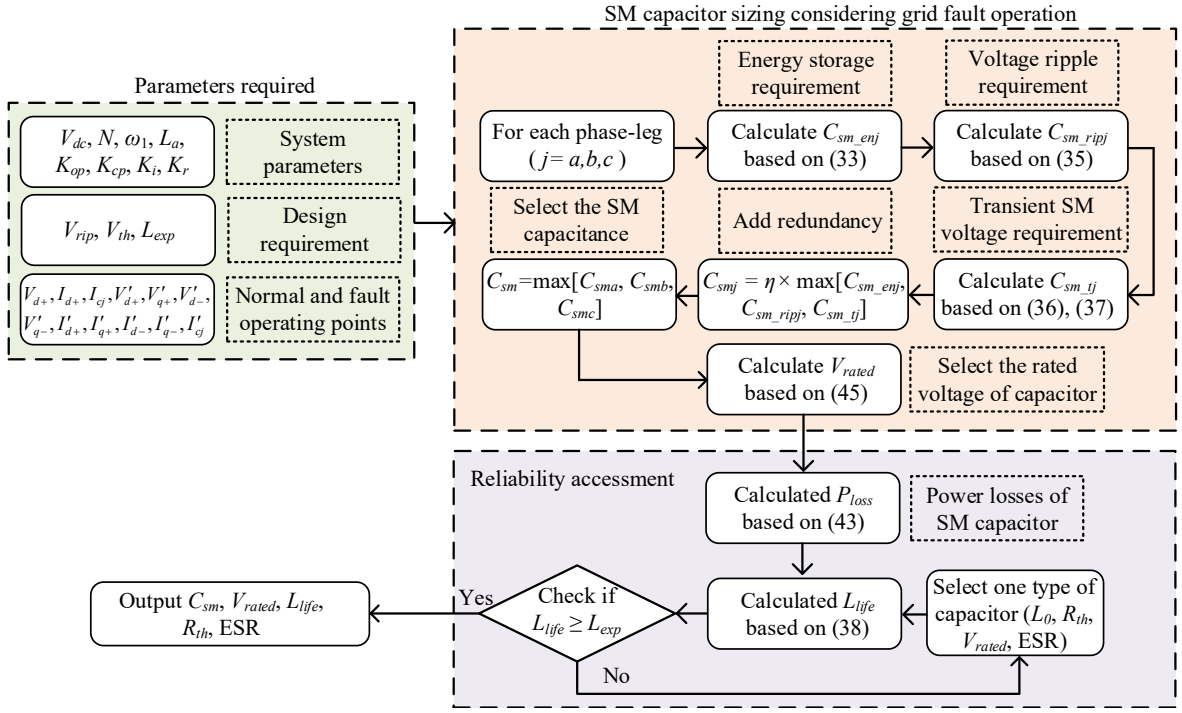


Figure 8. Design flowchart of SM capacitors.

6. Case Study

6.1. Design Example

To verify the correctness of the proposed method, a down-scale three-phase MMC design case is given. Key system parameters and design requirement were as shown in Table 2. The maximum SM voltage ripple V_{rip} should be limited within 10% of the SM DC-bias, while the allowable SM voltage V_{th} is selected 25% higher than the SM DC-bias. Two common grid fault conditions are selected for SM capacitor sizing: single-line-to-ground fault and three-phase short-circuit fault. Both positive- and negative-sequence currents will be injected into the grid when the grid fault is detected. The reactive current injection strategy follows the German grid code, as shown in [40]. Thus, the MMC operating points during the normal state and grid fault conditions are shown in Table 3.

By putting the design parameters above into Formulas (33) and (35), the SM capacitance demand for energy storage requirement and ripple voltage requirement can be calculated as: $C_{sm\_enj} = 250.8$ µF, $C_{sm\_ripj} = 857.7$ µF. According to Equations (38)–(39), the relationship between SM capacitance C_{sm} and the maximum transient SM voltage stress V_{tmax} can be calculated and shown in Figure 9. To keep the SM voltage in a safety range during both grid fault conditions, C_{sm_tj} is selected as 1.14 mF. With a 20% extra design margin ($\eta = 1.2$), the final SM capacitor is chosen as 1.36 mF, formed by two 680 µF capacitors connecting in parallel. By setting the rated voltage of the SM capacitor at 100 V, the information of the selected product is given in Table 4. By taking the ESR value into Formula (43), the power losses of the SM capacitor is around 0.1 W, which is relatively small. Thus, the hot-spot temperature of the SM capacitor is considered as equal to the ambient temperature in this case study. Assuming the operating ambient temperature is 60 °C, the SM capacitor lifetime can be estimated using Equation (51) as 2.7×10^5 h.

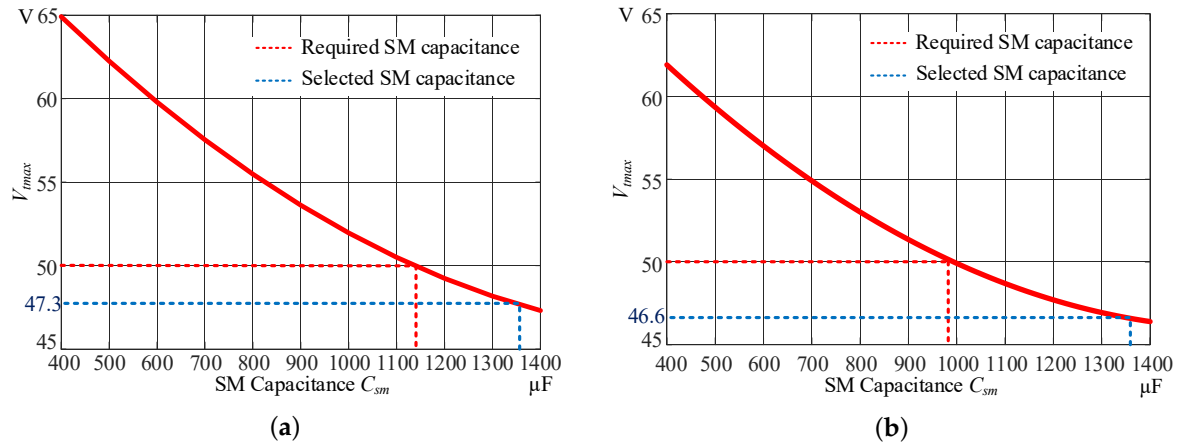


Figure 9. The maximum SM voltage under different grid faults: (**a**) single-line-to-ground condition and (**b**) three-phase short-circuit condition.

Table 2. System parameters and design requirement.

System Parameters	
SM number in each arm (N)	3
Arm Inductance (L_a)	5 mH
Grid frequency	50 Hz
Switching frequency	8 kHz
DC-bus voltage	120 V
K_{op}	10
K_i	60
K_{cp}	5
K_r	35
Design Requirement	
Peak-to-peak SM voltage ripple (V_{rip})	4 V
Maximum SM voltage threshold (V_{th})	50 V
Capacitance redundancy factor (η)	1.2

Table 3. Possible operation points of the MMC.

Normal Operation Point	
Grid voltage	$V_{d+} = 50$ V
Grid current injection	$I_{d+} = 5$ A ; $I_{q+} = 0$
Circulating current reference	$I_{cj} = 0.417$ A
Single-Line-to-Ground Condition	
Grid voltage	$V'_{d+} = 33.5$ V
	$V'_{d-} = 16.5$ V
Grid current injection	$I'_{d+} = 1.67$ A
	$I'_{q+} = 2.875$ A
	$I'_{d-} = 0$; $I'_{q-} = -3.5$ A
Three-Phase Short-Circuit Condition	
Grid voltage	$V'_{d+} = 0$; $V'_{d-} = 0$
Grid current injection	$I'_{d+} = 0$; $I'_{q+} = 4.5$ A
	$I'_{d-} = 0$; $I'_{q-} = 0$

Table 4. Key parameters of the selected capacitor product.

Part Number	UBY2A681MHL
Capacitance	680 µF
ESR	28 mΩ at 50 Hz; 14 mΩ at 100 Hz
Thermal resistance	1.5 °C/W
Reference lifetime	3000 h at 125 °C, 20–5 0V

6.2. Experimental Verification

By using the selected components given in Table 4, an experiment platform has been assembled, the structure of which is shown in Figure 10. The platform is formed with three phase-legs. The DC-side voltage of the MMC is provided by a constant DC source. A dSPACE system is used as the controller of the MMC, while an auxiliary DC supply is used to provide power for the sensors and gate drivers in the system. The AC side of the platform is connected to a grid simulator, which is used to generate the grid fault signal. The system operation waveforms during grid fault conditions are shown in Figure 11, where the system state during single-line-to-ground condition and three-phase short-circuit condition is shown in Figure 11a,b, respectively. Due to the symmetrical characteristic, only the SM voltage of upper arm is given.

It can be seen that the circulating current through each phase-leg is well-suppressed when the system operates in steady-state. During normal operation, the peak-to-peak SM voltage ripple is 3.5 V, which is well constrained within the design limit. During the transient state of both grid fault conditions, an obvious voltage over-shoot appears on each SM capacitor, which is caused by the dynamic response of the control system [30]. In Figure 11a, the maximum SM voltage in three phase-legs is 48.8 V, which is 1.5 V higher than the model-estimated value shown in Figure 9a. For three-phase short circuit condition, the maximum SM voltage is close to the expectation, with only a 1 V difference. These estimation errors are caused by the signal coupling within the MMC control system. However, all SM voltage is limited under 40 V, which proves the effectiveness of the proposed SM capacitor selection method.

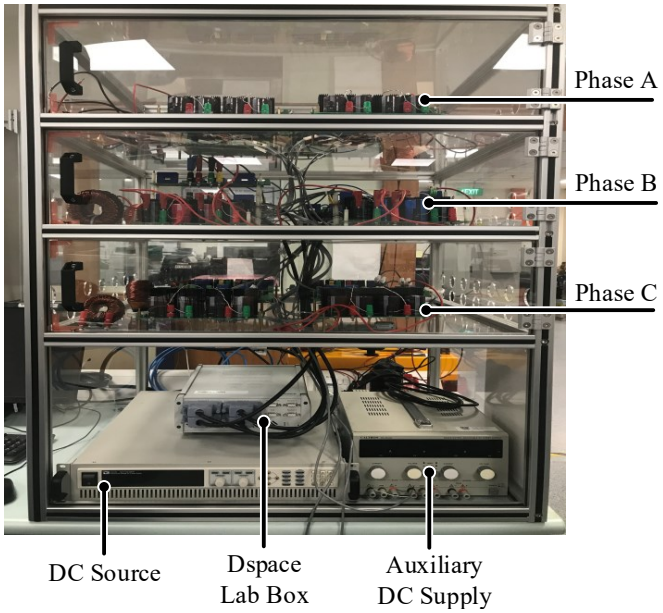


Figure 10. A photo of the down-scale MMC experimental platform.

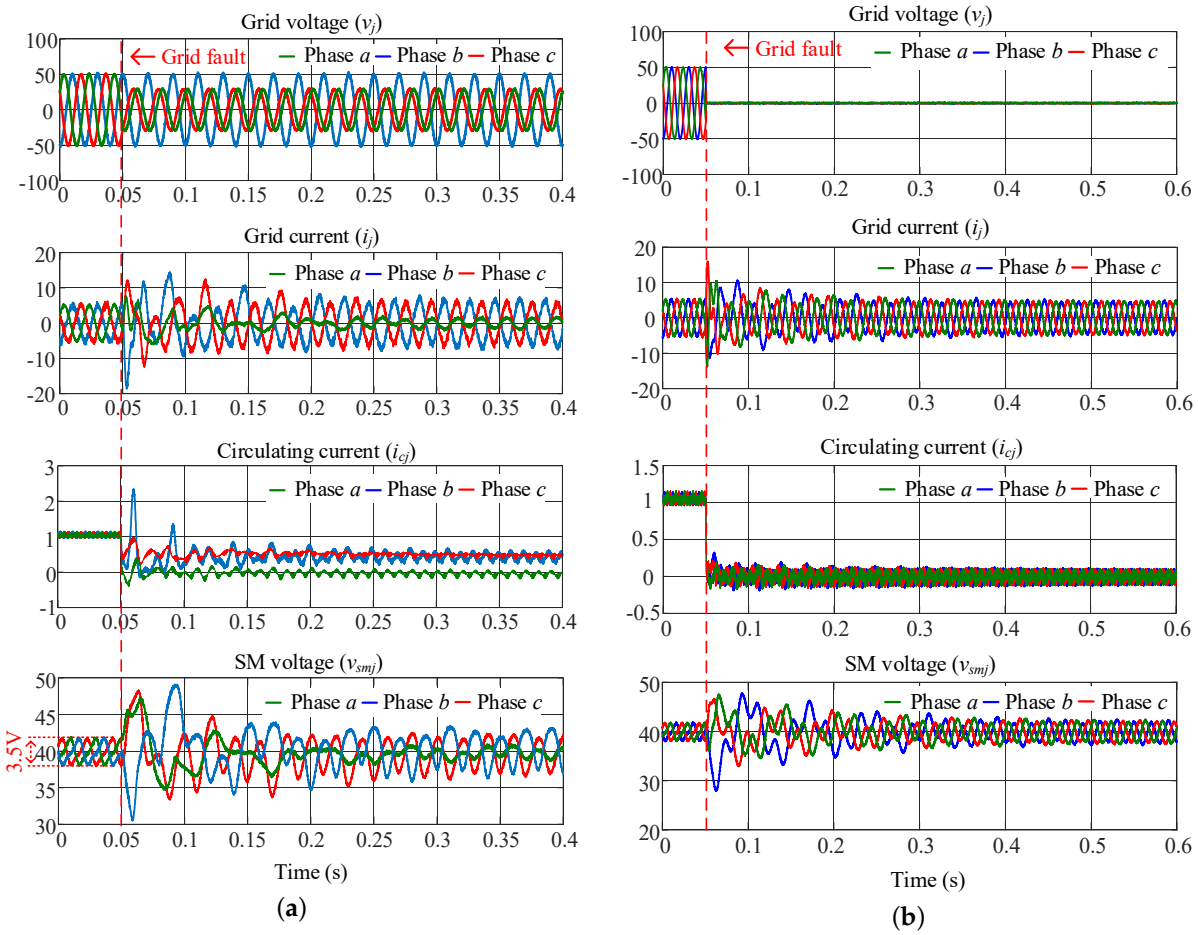


Figure 11. The experiment waveform of the MMC platform under different grid faults: (**a**) single-line-to-ground condition and (**b**) three-phase short-circuit condition.

7. Conclusions

A straightforward practical SM capacitor sizing method is proposed in this paper for MMC systems. Compared with the existing solutions, the proposed method is more applicable for a grid-connected MMC project, especially for cases requiring grid-fault-ride-through ability, such as static synchronous compensator (STATCOM) and the MMC-based HVDC system. A reliable path is given to select the capacitance, rated voltage, ESR, thermal resistance, and rated lifetime of the SM capacitor, considering the system requirement during normal operation state and grid-fault-ride-through conditions. Through analyzing the control loop, a quantitative estimation method of the maximum voltage stresses was given, which provides an insight into the impact of different control schemes on the SM capacitor design and improves the reliability of the MMC operating under grid fault conditions. A down-scale MMC experimental platform is designed and assembled. By comparing the experiment results with the design requirement, all design parameters are well achieved, which proves the effectiveness of the proposed design method.

Author Contributions: Z.Y. is mainly in charge of the conceptualization, methodology, theoretical modelling, and manuscript preparation. H.Q. is involved in the process of software programming and data acquisition. Y.T., Y.Y., and H.W. contribute to the project administration and supervision. All authors have read and agreed to the published version of the manuscript.

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