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Xenon difluoride etching of amorphous silicon for release of piezoelectric micromachined ultrasonic transducer structures

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ABSTRACT OF THE MASTER'S THESIS

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Abstract

Piezoelectric micromachined ultrasonic transducers (PMUT) are devices, which are based on the piezoelectric effect and are used for sensing applications. A typical PMUT structure has diaphragm with a piezoelectric material between thin high conductivity electrode layers. There are several methods which can be used for PMUT structure fabrication, including back- and front-side etching, wafer bonding, and sacrificial layer release. The state-of-the-art methods used currently for PMUT structure fabrication still face several problems.

Xenon difluoride (XeF_2) etching is a fluorine-based dry vapour etch method that provides highly selective isotropic etch. It is an ideal solution for the release of self-supporting layers within MEMS devices. In this work, XeF_2 etching of amorphous silicon (a-Si) for the release of PMUT structures was investigated. Different designs with varying dimensions were tested and characterized. The XeF_2 etching process demonstrated to be efficient and very fast compared to other methods used for PMUT/MEMS release etching. Results from the optimization tests on the XeF_2 process demonstrated total etching of 2 µm thick a-Si. Structures with sizes from 50 to 500 µm diameter were completely released after only 20 minutes of etching. Additionally, this work demonstrates that the etching rate of XeF_2 is also influenced by the size, shape and location of the via openings.

Furthermore, sputtered aluminium nitride AlN piezo layer process optimization and residual stress control contributed to the fabrication of suspended structures. All observed structures from 50 to 500 µm diameter which used AlN in the structural layer were suspended after release.

Keywords Pizoelectric ultrasonic transducers (PMUT), xenon difluoride (XeF_2), PECVD amorphous silicon (a-Si), aluminium nitride (AlN), thin film stress, sacrificial layer

Foreword

First, I would like to thank Anu Kärkkäinen and Tuomas Pensala for giving me the opportunity to be a part of VTT's MEMS research team. My participation on the project and this thesis work would not have happened without your confidence in me.

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I wish to acknowledge the support of my friends Kellen and Lia. They kept me going on and this work would not have been possible without their input. Additionally, I am grateful for the love of my family, my parents, sister and my dearest Vesa. They were always there to listen and help when needed.

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Symbols and abbreviations

Symbols

d	[µm]	diameter
D_i	$[C \cdot m^{-2}]$	electric displacement
e_{ik}	$[m/V]$	piezoelectric coefficient tensor
E_k		electric field tensor
E_s	[Pa]	Young's modulus
P	[Torr]	pressure
R_f		radii of curvature of the film
R_s		radii of curvature of the substrate
T	[°C]	Temperature
T_c	[°C]	Curie temperature
t	[µm]	thickness
t_f	[Å]	thickness of the film
t_s	[Å]	thickness of the substrate
v_s		Poisson's ratio
x_k		strain tensor
σ_{film}	[MPa]	thin film stress
σ_k	$[N/m^2]$	stress tensor

Abbreviations

Al	Aluminium
AlN	Aluminium Nitride
Ar	Argon
a-Si	Amorphous Silicon
BHF	Buffered Hydrofluoric Acid
CMOS	Complementary Metal Oxide Semiconductor
CVD	Chemical Vapour Deposition
DC	Direct Current
DOE	Design of Experiments
DR	Deposition Rate
DRIE	Deep Reactive Etching
EDP	Ethylene Diamine Pyrocatechol
HF	Hydrogen Fluoride
KOH	Potassium Hydroxide
LPCVD	Low Pressure Chemical Vapour Deposition
LTO	Low Temperature Oxide
MBE	Molecular Beam Epitaxy
MEMS	Microelectromechanical Systems
MOCVD	Metal Organic Chemical Vapour Deposition
N_2	Nitrogen
PECVD	Plasma Enhanced Chemical Vapour Deposition
PMUT	Piezoelectric Micromachined Ultrasonic Transducers
PVD	Physical Vapour Deposition

PZT	Lead Zirconate Titanate
RF	Radio Frequency
Si	Silicon
a-Si:H	Hydrogenated amorphous-Silicon
SiH_4	Silane
SiO_2	Silicon Dioxide
SOI	Silicon on Insulator
UV	Ultra Violet
XeF_2	Xenon Difluoride
ZnO	Zinc Oxide

1 Introduction

Devices that use ultrasonic waves for the measurement of certain parameters are called ultrasonic transducers. [1] Ultrasonic transducers are key components in sensors for distance, flow, and level measurement as well as in power, biomedical, and other applications of ultrasound. Piezoelectric micromachined ultrasonic transducers (PMUT) are microelectromechanical systems (MEMS)-based devices. A piezoelectric membrane is the key element in such devices and it is made with materials that exhibit the piezoelectric effect. The Piezoelectric Effect is when electrical charge is produced as a result of applied mechanical strain and the Reverse Piezoelectric Effect is the opposite. [1] A typical PMUT structure has a layer of a piezoelectric material between thin high conductivity electrode layers. [2] Although, twenty different crystal systems can exhibit piezoelectricity, the most used piezoelectric thin film materials in MEMS applications have either the wurtzite (AlN and ZnO) or the perovskite (PZT) structure. Aluminium nitride (AlN), belongs to groups III-V of the semiconductor family and its crystal structure consists of a hexagonal closed-packed wurtzite structure. High-quality AlN films can be deposited by sputtering at relatively low temperatures. This makes AlN suitable for complete integration with complementary metal oxide semiconductor (CMOS) technology, as well as for the use of Al for metallization layers (electrodes). [3]

There are several methods which can be used for fabricating PMUT devices. These methods include back- and front-side etching, wafer bonding and sacrificial layer release. Back-side etching is a bulk micromachining process and is a common method utilized for PMUT fabrication. In the process, the PMUT diaphragm is defined by etching the back side of the wafer. Possible methods for back-side releasing include using either anisotropic wet etching or deep reactive etching (DRIE). However, there are many difficulties associated with this process. Bulk micromachining involves extensive silicon (Si) consumption. In the process of creating small cavities, a large amount of Si is etched away and the resulting device becomes fragile. Another challenge is the difficulty to etch uniform membrane dimension across the wafer. [4]

Front-side release etching is carried out on the surface of the wafer. In the process, the structural layer is first deposited on the substrate and patterned. Then, small via openings are etched on the films and the silicon substrate under the films is etched in order to form the diaphragm cavity. Both back-side and front-side etching techniques can utilize the advantages of wet etching processes which are low cost manufacturing methods and easy to use. However, wet anisotropic etching depends on the crystalline structure of the substrate and in isotropic etching it is not possible to control the shape of the cavity. Therefore, device design is very limited. [5]

Another approach to diaphragm formation is to fabricate the cavity of the PMUT and the device layer on two separate wafers and then bond the two parts together. This is called wafer bonding method. [2] For this method silicon on insulator (SOI) wafers are used. However, SOI wafers cost approximately tenfold more than the cost of bulk wafers. This cost disadvantage must be compensated by other factors such as smaller chip size, higher performance, and easier processing (less process steps). Another concern is the availability of SOI wafers. [5]

Sacrificial layer release is a method in which the cavity is formed by the release of a sacrificial film. The sacrificial film is deposited and patterned before the deposition of the structural layer. After patterning of the sacrificial layer, the structural layer is deposited and small via holes are etched. The sacrificial layer is then removed through the via openings leaving a cavity under the structural layer. This method is widely used with silicon dioxide (SiO_2) as the sacrificial film. In this case, typically, silicon nitride is used in the structural layer of the device. The SiO_2 is released using hydrogen fluoride (HF) vapour or liquid. Silicon nitride is a challenging material in the HF vapour process. This is because the silicon nitride is attacked and converted into hexafluoroammonium silicate salt, which occupies a larger area than the original material. The salt is volatile and can be removed with baking. [6]

Recently, interest in the use of amorphous silicon (a-Si) as sacrificial layer has been increasing. The etching of a-Si can be carried out using xenon difluoride (XeF_2), which is a vapour phase isotropic etchant with extensive selectivity to many materials. Furthermore, XeF_2 was

found to have high silicon etching rates. [6] This makes possible the use of SiO_2 as passivation protective layer and in the structural layer of the device. Moreover, sacrificial release of a-Si by XeF_2 offers more possibilities for diaphragm design and low attack to AlN as well as to metal electrodes. For these reasons, interest in a-Si release by XeF_2 in micromachining applications has been increasing. [7] [8]

This MSc thesis demonstrates the use of XeF_2 etching method for the release of a-Si sacrificial layer for different structure designs, which can be used for PMUT device fabrication. The work presents two structure designs, which were tested using different diaphragm dimensions, and via openings of several sizes and geometries. Typically, in a PMUT structure, the structural layer is composed of an insulator and a piezoelectric material. The insulator material used for the experiments is SiO_2 and the piezoelectric material, AlN. The layers were tested both separately and together, in order to obtain better understanding of the results. The goals of this research were the creation of PMUT structures based on XeF_2 release method, optimization of etching process parameters, use of developed plasma enhanced chemical vapour deposition (PECVD) a-Si film as sacrificial layer, and AlN stress optimization for suspended device layer.

After XeF_2 etching optimization, it was possible to release a-Si from structures up to 500 µm in diameter. The XeF_2 etching process was demonstrated to be efficient and very fast compared to other methods used for PMUT/MEMS release etching. Furthermore, AlN optimization and stress control was effective and contributed to the fabrication of suspended structures.

2 Piezoelectric Micromachined Ultrasonic Transducers: structure and materials

This section consists of a literature review covering the main topics relating to the fabrication of PMUT structures. First, the characteristics and role of piezoelectric materials for PMUTs are discussed. Second, state-of-the-art methods for PMUT manufacturing are presented. To conclude, the advantages of the XeF_2 etching method for PMUT diaphragm fabrication are explained.

2.1 Piezoelectric materials

The Piezoelectric Effect has been known since 1880. [2] It consists of electrical charge which is produced as a result of applied mechanical strain and the Reverse Piezoelectric Effect is the opposite. The effects described are easily achieved at ultrasonic frequencies. For this reason, piezoelectricity is the basis of most ultrasonic transducers. [1]

Piezoelectric materials are a subset of ferroelectric materials. The key property of a ferroelectric material is that it has a finite electrical polarization. This electrical polarization exists even when no external field is applied. Ferroelectric materials typically undergo a phase transition at the Curie temperature (T_c). The material goes from a high-temperature non-polarized paraelectric state to a low-temperature ferroelectric (polarized) state. The spontaneous polarization is a consequence of the structural transition that takes place at T_c and involves symmetry-breaking distortion. This polarisation is realised in the form of dipoles within the material, but it is expressed as electrical charge on the surface of the material. [9] [1]

In contrast to ferroelectric materials, in piezoelectric materials the generation of electricity is obtained by induced mechanical strain. In piezoelectric materials, the change can occur in both directions. The material can have a charge resulting from an applied mechanical strain, or stress/strain resulting from applied electric field. The charge on the surface when exposed to applied mechanical strain is called direct effect and change in dimensions due to applied

electric filed is called converse effect. The electric displacement and stress/strain are related by a linear dependence at low fields, expressed by the following equations: [3]

$$D_i = \sum_k d_{ik}\sigma_k \text{ and } D_i = \sum_k e_{ik}x_k \text{ (direct effect)} \quad (2.1)$$

$$x_i = \sum_k d_{ik}E_k \text{ and } D_i = \sum_k e_{ik}E_k \text{ (converse effect)} \quad (2.2)$$

Where,

D_i is the electric displacement
E_k is the electric field tensor
σ_k and x_k are the stress and strain tensors, respectively
d_{ik} and e_{ik} are the piezoelectric coefficient tensors

The indices used for definition of the piezoelectric coefficient tensors usually refer to the crystallographic axes of the crystal. [3]

Piezoelectric materials are divided into four groups: piezoceramics, piezocrystals, piezopolymers and piezocomposites. Although, 20 different crystal systems can exhibit piezoelectricity, the most used piezoelectric thin film materials in MEMS applications have either the wurtzite (AlN and ZnO) or the perovskite (PZT) structure. The main difference between AlN, zinc oxide (ZnO), and lead zirconate titanate (PZT) films, is that PZT films are ferroelectric. In ferroelectric materials, the polarization vector can be reoriented in different directions. For AlN and ZoN, the growth must be controlled in order to provide the alignment for the polar direction across the film. [3]

AlN, belongs to groups III-V of the semiconductor family and its crystal structure consists of a hexagonal closed-packed wurtzite structure. The AlN polar and piezoelectric response lies along the $[0001]_{\text{hexagonal}}$ direction. As already described, AlN is not ferroelectric. This means that in order to achieve a good piezoelectric coefficient, crystals of certain type must result from deposition. A good piezoelectric coefficient comes from homogeneous nucleation of grains with same $(0001)_{\text{hexagonal}}$ out of plane texture and identical polar direction. High-quality AlN films can be obtained by reactive sputtering at relatively low temperatures. This makes AlN suitable for complete integration with CMOS technology, as well as for the use of Al for metallization layers (electrodes). [3]

Sputtering is a physical vapour deposition method (PVD), in which argon ions (Ar^+) from a glow discharge plasma hit the negatively biased target and eject typically one target atom. The ejected atoms are transported to the substrate wafer in a vacuum. An illustration of the sputtering process is shown in Figure 2.1. For the AlN deposition, the gas inlet feeds (Ar) and nitrogen (N_2) gases. The gasses inside the chamber are ionised by a glow discharge plasma. The positive ions are accelerated to the target, which is an aluminium disc. The forceful collision between the target and these ions causes Al ions to eject. The ions are then transported to the wafer substrate in a vacuum and AlN thin film is formed on the wafer surface. [5] [10]

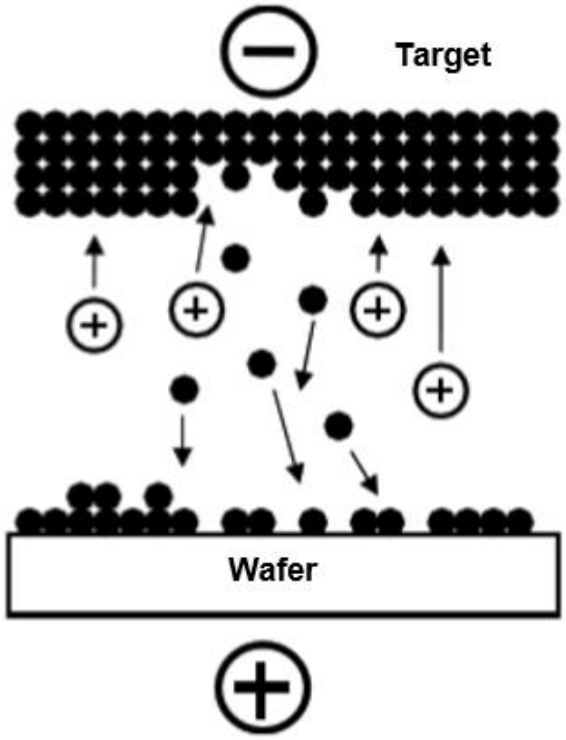

Figure 2.1: Simple schematic of a sputtering system. Accelerated ions hit the solid negatively biased target, the target atom is then eject and transported to the substrate wafer in a vacuum. The film is formed on the wafer surface. Image taken from: [5]

AlN can be deposited using several different methods. Including metal organic chemical vapour deposition (MOCVD), molecular beam epitaxy (MBE), electron cyclotron resonance dual-ion beam sputtering, and pulsed laser ablation (PLD). However, these methods are expensive and in the case of MOCVD and MBE, high processing temperatures are required.

Direct current (DC) and radio frequency (RF) sputtering have the advantages of low temperature and low cost processes. [10]

2.2 PMUT fabrication methods

A typical PMUT structure has a layer of a piezoelectric material between thin high conductivity electrode layers. A schematic is presented on the following figure. [2]

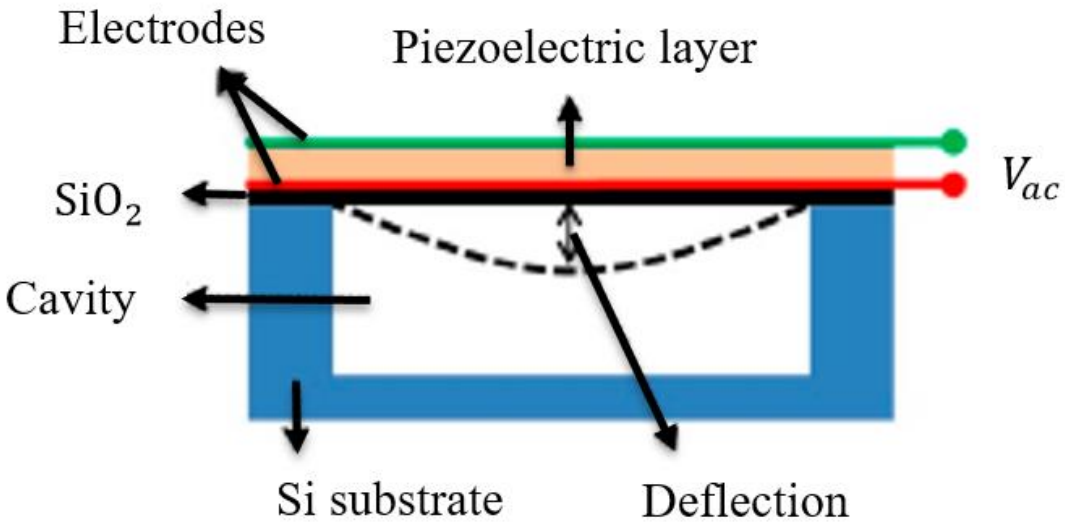

Figure 2.2: Schematic of a PMUT structure made by a silicon substrate, silicon dioxide and a piezoelectric layer between electrodes. The cavity provides space for the deflection of the membrane. Image taken from: [2]

In this section, state-of-the-art methods to fabricate PMUT structures will be summarized and their advantages and disadvantages will be explained.

2.2.1 Back-side etching

Bulk micromachining is a process in which the bulk of a substrate is etched, cut, or modified to create the diaphragm. Back-side etching is a bulk micromachining process which is widely used in microfabrication. [4] [11] [2] The process can be made either using anisotropic wet etching or DRIE. In wet anisotropic etching, the side walls of the cavity are sloped (Fig.2.4). Wet anisotropic etching is carried out on single crystal silicon wafer substrates. A wide variety of anisotropic etching solutions can be found. Ethylene diamine pyrocatechol (EDP) and potassium hydroxide (KOH) are the most used. [4] Back-side etching of the can also be

made by DRIE. In this case, vertical walls are obtained. [12] [13] Figure 2.3 shows an illustration of a PMUT structure in which the diaphragm was defined by back-side etching.

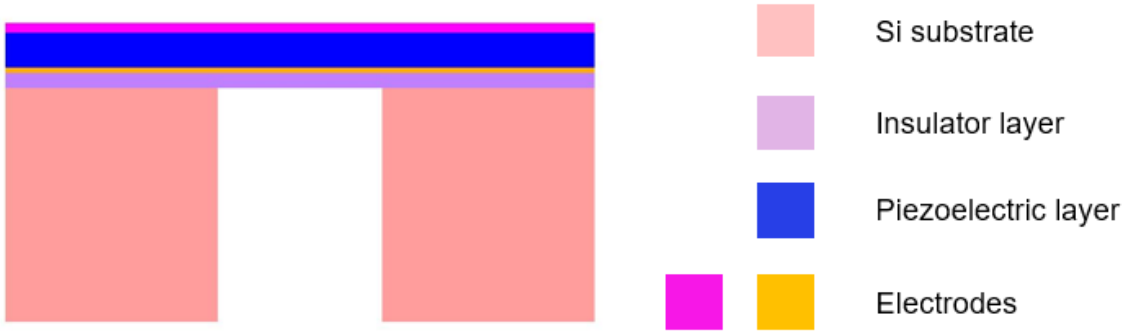

Figure 2.3: Schematic of a PMUT structure in which the diaphragm was defined by etching the back-side of the wafer. The vertical walls are obtained by DRIE etching.

The device shown in Figure 2.3 illustrates a cavity with vertical walls, which is obtained by DIRE etching. The cavity of the device in Figure 2.4 has sloped side-wall profile. The figure is an example of a diaphragm defined by anisotropic wet etching.

Figure 2.4: Schematic of a PMUT structure in which the diaphragm was defined by etching the back side of the wafer. The side-walls profile in the image are obtained by anisotropic wet etching. Image taken from: [2]

Back-side etching technique may result in certain problems. Bulk micromachining involves extensive Si consumption. In the process to create small membranes, a large amount of silicon area is wasted and the resulting device becomes fragile. [4]

2.2.2 Front-side etching

In this process, the etching is carried out on the surface (front-side) of the wafer. First, the thin films are deposited on the silicon substrate. Later, via openings are patterned and etched. The silicon substrate under the films is then released opening the cavity for the diaphragm formation. The silicon substrate is etched away in a controlled manner. [4] Figure 2.5 shows the process flow for a PMUT structure in which the diaphragm was defined by a front-side etching fabrication method. Front-side etching of the diaphragms can be made using both isotropic and anisotropic wet etching processes. [2] [4]

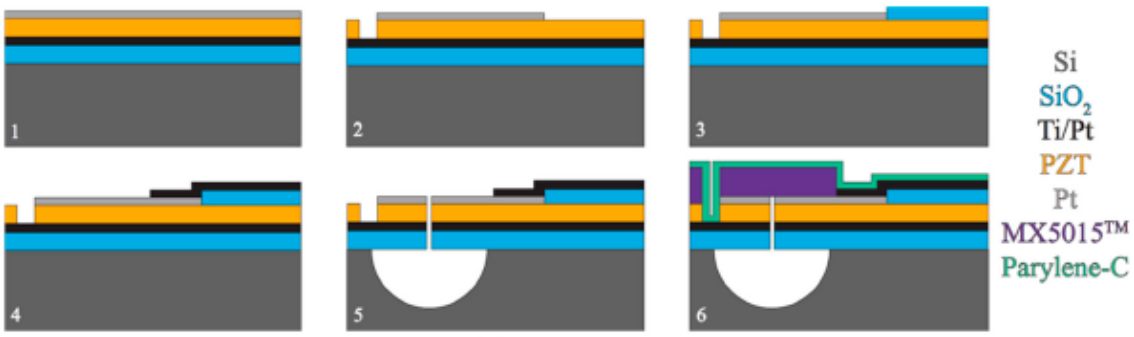

Figure 2.5: Process flow for a PMUT structure fabrication using front-side etching release. Step 5 illustrates the release of the silicon substrate through a via hole opening. Image taken from: [2]

The advantage of front-side etching in comparison to back-side etching is the consumption of smaller areas. This allows the fabrication of cavities of relatively smaller diameters. [4], [2] Both back-side and front-side etching techniques can utilize the advantages of wet etching processes which are low cost and easy to use. In addition, a benefit of anisotropic etching is that it can provide very smooth surfaces. However, anisotropic etching depends on the crystalline structure of the substrate, limiting device design. In the case of isotropic etching, it is not possible to control the shape of the cavity. [5] [6]

2.2.3 Wafer bonding

Another approach to diaphragm formation is to fabricate the cavity of the PMUT membrane and the device layer on two separate wafers and then to bond the two parts together. [2] [14] A schematic illustration of a bonded device is shown in Figure 2.6.

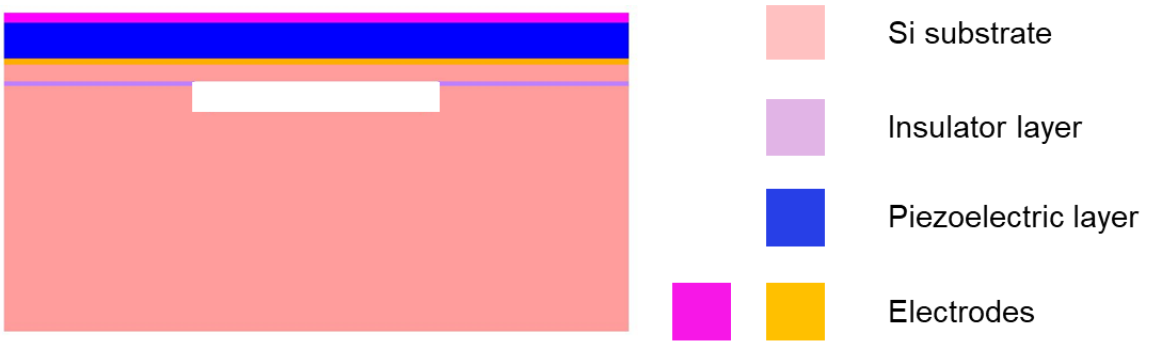

Figure 2.6: Schematic of a PMUT structure in which the diaphragm was defined by a wafer bonding method. The cavity and the device are fabricated on two separate wafers and then bonded together.

In this method, SOI wafers are utilized. SOI wafer is a structure consisting of a layer of single crystalline silicon separated from the bulk substrate by a thin layer of insulator. SOI technology offers improvements in many ways, such as a reduction in the number of processes steps. However, SOI wafers cost approximately tenfold more than the cost of bulk wafers. This cost disadvantage must be compensated by other factors such as smaller chip size, higher performance and easier processing (less process steps). Another issue is the availability of SOI wafers. [5] [6]

2.2.4 Sacrificial layer release

Another method and the one of greatest importance for this work is the creation of diaphragm cavity defined by sacrificial layer release. Sacrificial layer release is a method in which the cavity is formed by the release of a sacrificial film. The sacrificial film is deposited and patterned before the deposition of the structural layer. After patterning of the sacrificial layer, the structural layer is deposited and small via holes are etched. The sacrificial layer is then removed through the via openings leaving a cavity under the structural layer. [15] An illustration of a device in which the diaphragm was defined by sacrificial layer release is shown in Figure 2.7. This method is widely used with SiO_2 as sacrificial layer and typically, silicon nitride is used as the structural layer. [15]- [18]

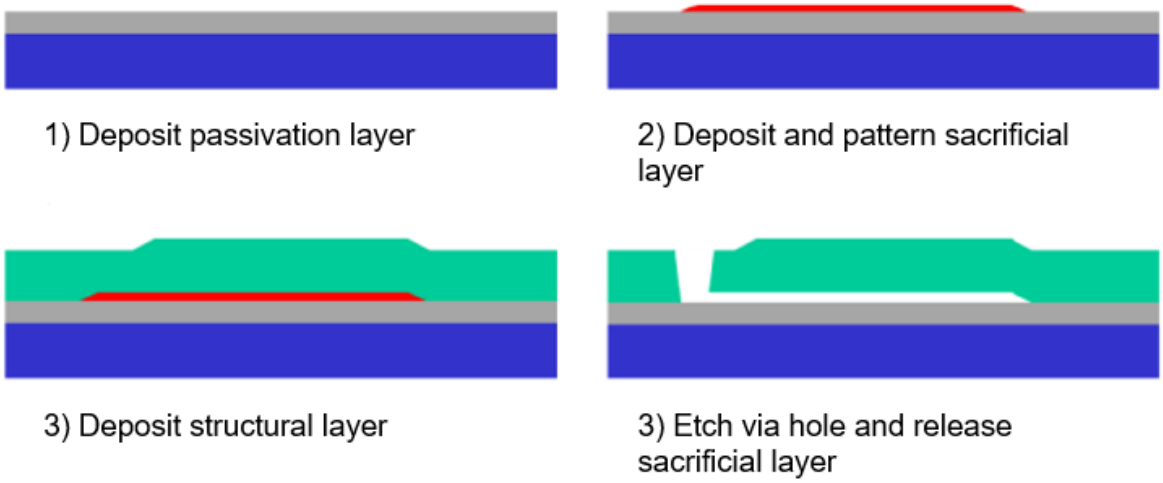

Figure 2.7: Schematic of a PMUT structure in which the diaphragm was defined by sacrificial layer release method. The sacrificial layer is grown or deposited on the silicon substrate and then etched away through via openings. Image taken from: [19]

On processes in which SiO_2 is used as sacrificial layer, the film is released using hydrogen fluoride (HF) vapour. However, if the structural layer is made with silicon nitride, some challenges may be encountered. Silicon nitride is a challenging material in the HF vapour process. This is because the silicon nitride is attacked and converted into hexafluoroammonium silicate salt, which occupies a larger area than the original material. The reaction is as follows: [6] [20]

$$Si_3N_4 + 16HF \rightarrow 2(NH_4)_2[SiF_6] + SiF_4 \tag{2.3}$$

The salt is volatile and can be removed with baking. Different silicon nitride types exhibit different selectivities, with silicon-rich low pressure chemical vapour deposition (LPCVD) silicon nitride having the best overall performance. [6]

Recently, interest in the use of a-Si as sacrificial layer has been increasing. a-Si sacrificial layers can easily be removed by dry etching. The dry etching of a-Si can be carried out using XeF_2, which is a vapour phase isotropic etchant with wide selectivity. Furthermore, XeF_2 was found to have high silicon etching rates and small reaction to SiO_2. [6] This makes possible the use of SiO_2 both as passivation and structural layer. Moreover, sacrificial release of a-Si by XeF_2 offers more possibilities for diaphragm design and low attack to AlN as well as to metal electrodes. For these reasons, interest in a-Si release by XeF_2 in micromachining

applications has been increasing. [7] [21] [8] The advantages of XeF_2 etching will be discussed further in the following section.

2.3 XeF_2 advantages for release of PMUT structures

This work is based on the development of PMUT structures using sacrificial layer release with an XeF_2 etching method. This section summarizes the different types of etching and the advantages of XeF_2 in comparison with other methods for the fabrication of PMUT devices.

Etching is surface modification of a material by dissolving it using liquid or gaseous chemically aggressive compounds (etchants). The areas which are not to be attacked by the etchant are masked by a protective layer, which in the case of micro- and nanofabrication is generally composed of photoresists. These protective masks are usually removed after the etching process is completed. The use of masks and etchants allows the practice of etching processes for patterning micro- and nanostructures. [22]

The etching of solid surfaces can be divided into two categories: wet processes (wet-chemical etching or electrochemical) or dry processes (physical, chemical, or a combination of both). In wet etching a liquid is used, whereas in dry etching processes the etchant can be a vapour or gas in a state of plasma. For a wet etching process to be efficient, the product formed by the target material must be soluble in the etchant medium. For dry etching processes, the reaction product must be sufficiently volatile. However, if the membrane layer only reacts and is not removed, the reaction products will eventually form a passivation layer. [22]

The direction resulting from etching is classified as the etch profile. Figure 2.8 illustrates different etch profiles. Isotropic profile is the type of etching which occurs in all directions and it is the most commonly encountered. Most wet etchants result in an isotropic profile, although it is also encountered in plasma and dry etching. Anisotropic etching results in a vertical or almost vertical profile. Anisotropic processes are spatially directional, but there are two different usages of the term anisotropic etching: anisotropic wet etching and anisotropic plasma etching. Anisotropic wet etching is dependent on crystal planes of silicon. EDP and KOH are the most widely used anisotropic wet etchants. [4] [5] [22]

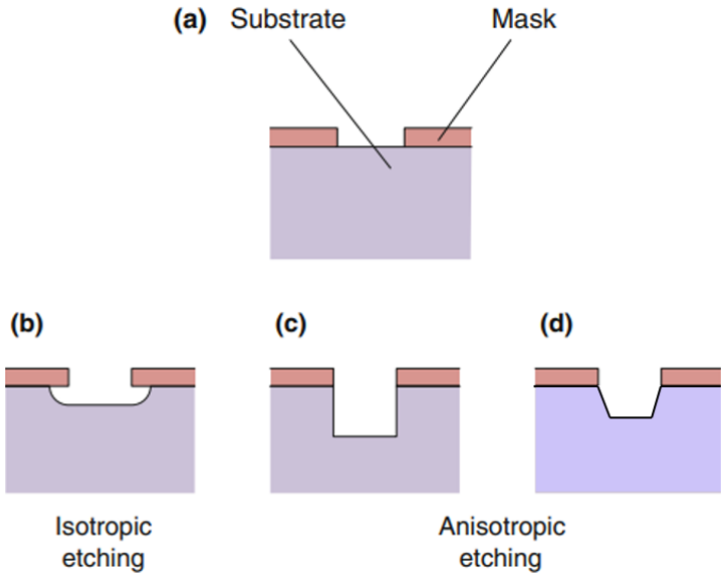

Figure 2.8: Schematics of etching profiles. (a) Substrate before etching with a patterned mask, (b) isotropic etching profile. In isotropic etching the shape resulting from etching cannot be controlled, (c) vertical wall profile resulting from anisotropic etching, and (d) wet anisotropic etching, which is based on crystal direction. Image taken from: [22]

Vapour phase etching methods are widely used for sacrificial layer release processes. [6] [22]- [24] A particular advantage of vapour phase etching is that it avoids stiction issues frequently experienced in wet etching processes. [22] XeF_2 is a vapour phase isotropic etchant and it has wide selectivity. [6] Selective etching is based on the application of etchants with different etching rates for alternative species. The necessity for a selective etching arises from the requirement of a (more or less) exclusive attack of an etchant on only one of the species present in a micro- or nanostructure. XeF_2 etches polycrystalline, amorphous and single crystal silicon, but also germanium, tantalum and tungsten. [22] [5]

XeF_2 etching can be carried out in either continuous or pulsed flow. Systems with the highest etching rate utilize a continuous flow. In this case, the process chamber utilizes showerhead gas distribution. In certain cases, a pulsed flow approach can offer significant performance advantages. The basic methodology is to have an isolated reservoir prior to the process chamber. This reservoir is filled with XeF_2 vapour (or a mixture of XeF_2 vapour and another gas) at a certain pressure. With the process chamber under vacuum, the reservoir is quickly opened up to the process chamber allowing a “pulse” of the reactant or mixture to enter and initiate the etching. Once all the XeF_2 is consumed, the chamber is evacuated. The same

cycle is repeated until the desired amount of silicon has been etched away. [6] Figure 2.9 illustrates a simple schematic of the XeF_2 etch system.

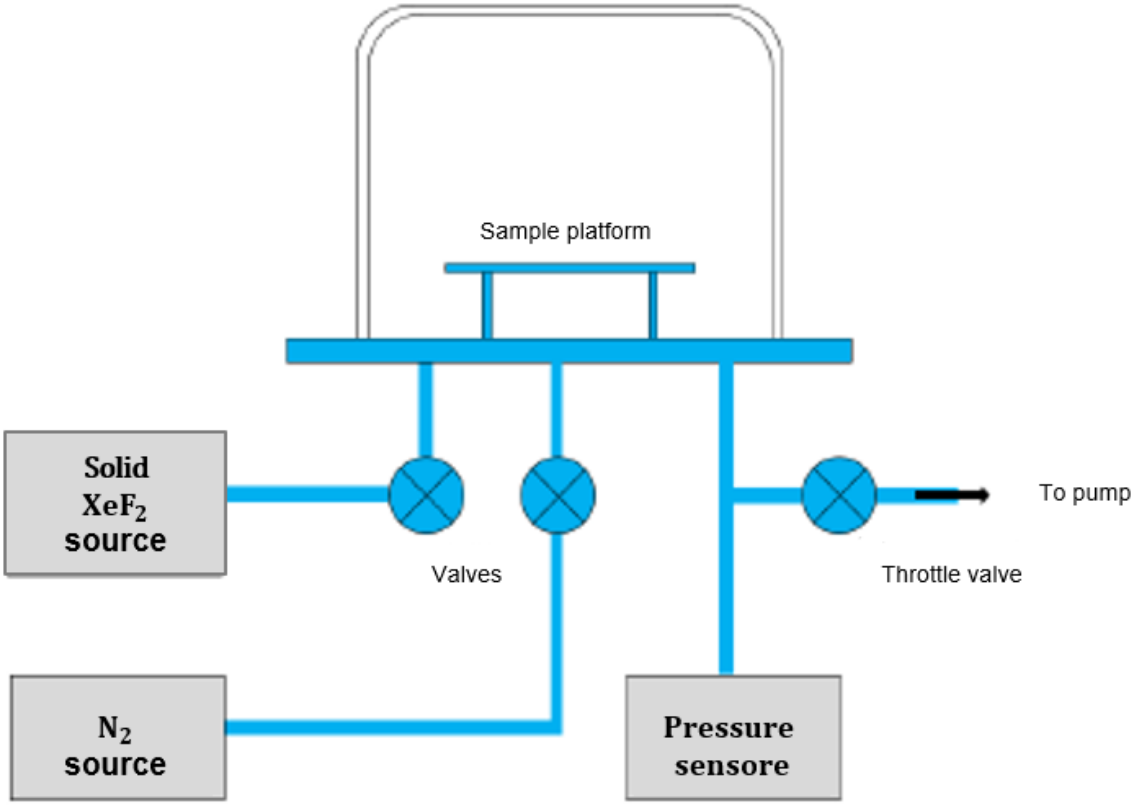

Figure 2.9: Schematic of XeF_2 etch system. During the etching process, the XeF_2 valve is opened first. The pump is throttled simultaneously to achieve the desired pressure. XeF_2 then sublimes from solid to gas and etching of the sample starts. In a continuous flow, pumping of the gas with N_2 happens simultaneously with the etching process. In pulsed flow, the pumping of the gas happens only after the end of the etching cycle. Image taken from: [25]

The amount of exposed area is an important factor in determining etching rate; a secondary factor is opening size. Large areas such as whole wafers, consume almost all of the XeF_2 available on contact. For very small exposed areas, XeF_2 is consumed slowly and the etch rate is roughly proportional to pressure. In the case of very narrow opening areas, pulsed flow offers an advantage over continuous flow. Flowing a rapid pulse in and then evacuating the process chamber repeatedly pushes XeF_2 deep into long/narrow spaces and removes effluents between cycles. Another advantage of pulsed flow is maximum efficiency. When throughput is not a concern, the time between pulses can be set such that almost 100% of the XeF_2 is consumed in the process reaction. [6]

As already described, XeF_2 is a fluorine-based silicon etchant. XeF_2 was found to have high silicon etching rates and reaction probabilities at room temperature, with high selectivity to many metals, dielectrics, and polymers used in traditional semiconductor processing. Its use can easily be integrated with other processes. At room temperature, XeF_2 sublimes at about 4 Torr, and therefore equipment designed to use XeF_2 for silicon etching needs vacuum process capability. The overall Si/XeF_2 reaction is exothermic and it is described by the following equation: [6]

$$2\,XeF_2 + Si \rightarrow 2\,Xe + SiF_4 \tag{2.3}$$

Figure 2.10 presents a schematic of the Si/XeF_2etching reaction. The key variables in the XeF_2 silicon etching process are exposed silicon area and XeF_2 flow rate. The XeF_2 etching process is exothermic, and the etching rate varies inversely with temperature. Therefore, etching rates can be maximized if wafers are processed on a cooled chuck. [6]

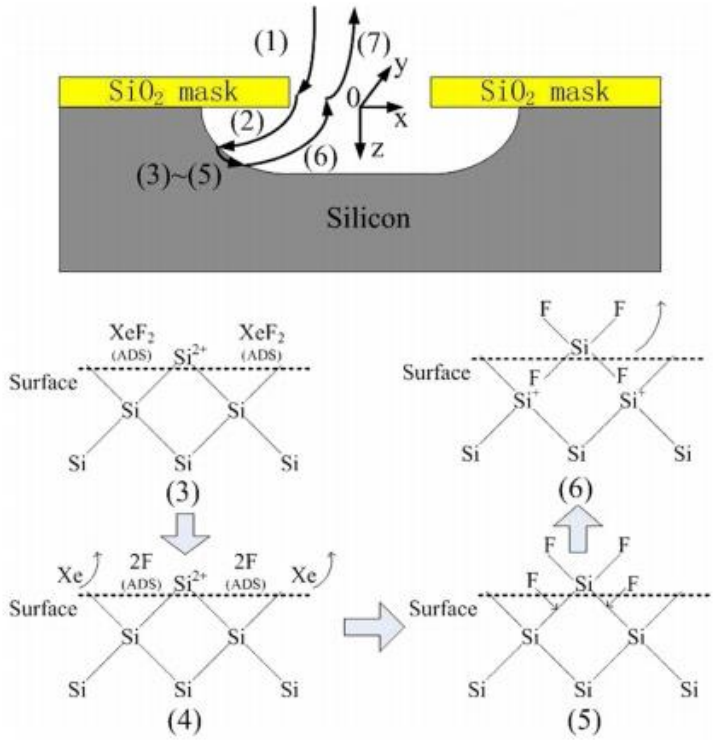

Figure 2.10: Schematic of XeF_2 etching mechanisms on silicon. The etching process occurs through the following steps: (1) Mass diffusion of the XeF_2 gas from the reactor to open surface. (2) Diffusion of XeF_2 from the open surface through the etched silicon cavity. (3) XeF_2 gas is adsorbed at the silicon surface. (4) XeF_2 molecule dissociates into adsorbed fluorine (F) atoms and Xe gas. (5) A bond between Si and F atoms is formed and SiF_4 is adsorbed at the silicon surface. (6) Desorption of SiF_4 molecules at the external surface. (7) Purge of the desorbed gases. Image taken from: [23]

XeF_2 has been extensively used for etching sacrificial silicon for many years. In some cases XeF_2 offers advantages when compared to other vapour gases etchants, such as HF release processes. One of the advantages which is important for this work is that XeF_2 is better compatible with piezoelectric materials. Additionally, XeF_2 has a low level of attack on silicon dioxide. Several piezoelectric MEMS devices including bulk acoustic wave filters [26], pumps, [27], resonators [28] and switches [29] have been fabricated using XeF_2. The low level of attack on piezoelectric materials and metal electrodes makes XeF_2 etching beneficial for piezoelectric MEMS application. [6] The following image summarizes the selectivity of XeF_2 for different materials used in microelectronic devices fabrication.

Vertical etch rates scaled to 1 cm^2 [nm / min]	
Al_2O_3	0
AlN	0
LPCVD-Si_3N_4	137
LPCVD-TEOS-SiO_2	4
LTO-SiO_2	24
PECVD-Si_3N_4	194
Poly-Si	3930
Ti/Mo	1370
TiW/W	613

Figure 2.11: Vertical etch rates for common materials used for MEMS applications. The etch rate is based on 1 cm^2 exposed area. Image taken from: [25]

3 Experimental Methods

In this section, the experiments performed for this work will be described. First, the design of the tested structures is presented and explained. Second, each process step is thoroughly elucidated. Then, the design used for the diaphragms and for the via openings is discussed. To conclude, the characterization and analysis methods are demonstrated.

3.1 PMUT structure design

The experimental part of this research is composed of developing structures which can be used for the fabrication of a PMUT device. The developed structures use a-Si sacrificial layer release by XeF_2 to define the diaphragm. The experiments consisted of testing two different structure designs denoted as A and B (Figure 3.1). The stability of the structures was checked by testing different diameter dimensions. The a-Si etching rate was characterized using via openings of different shapes and sizes.

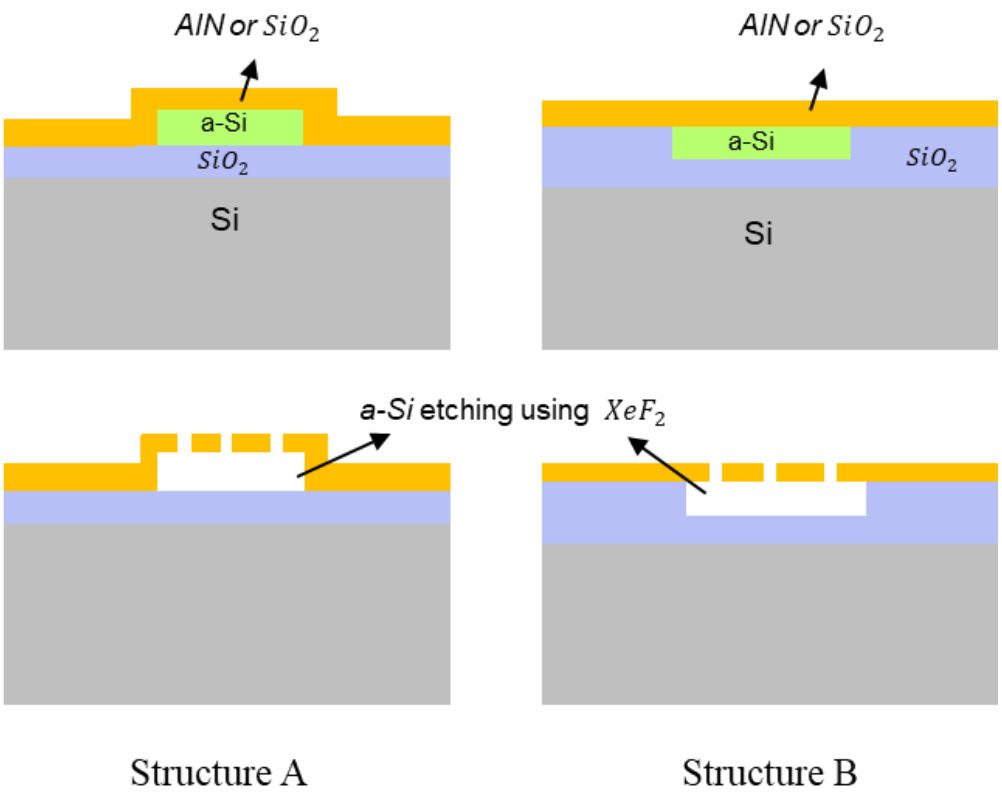

Figure 3.1: Schematic drawing of the tested structure designs. Structure A: the suspended membrane structure was tested using a hill shape design. Structure B: the suspended membrane structure was tested using a valley shape design.

Structure A consists of a silicon substrate, SiO_2 as passivation layer, a-Si as the sacrificial layer and AlN/SiO_2 as the structural layer. Typically, in a PMUT structure, the structural layer is composed of an insulator and a piezoelectric material. The insulator material used for the demonstrated structures is SiO_2 and the piezoelectric material AlN. In structure A, the samples were divided into two groups. In one group, only AlN was used in the structural layer and in the other, only SiO_2. This was made with the goal to observe the residual stress influence after sacrificial layer release on the structural layer of each film separately.

The same process was used for structure B however, in structure A, the diaphragm cavity was made into a hill shape and in structure B into a valley shape. Furthermore, in structure B, the materials for the membrane layer were tested both separately and together.

In total, fourteen wafers were fabricated. Eight wafers were used to fabricate structure A, and six wafers for structure B.

3.2 PMUT structure fabrication process

In this section, the process steps will be presented and explained. First, the general process that was carried out for both structures is presented. Then, the continuation process for structure A is described and finally, the continuation process for structure B. The schematic for the general process flow, which was the starting point for both structures, is presented in Figure 3.2. The complete process flow for structure A is sown in Figure 3.4 and for structure B in Figure 3.6.

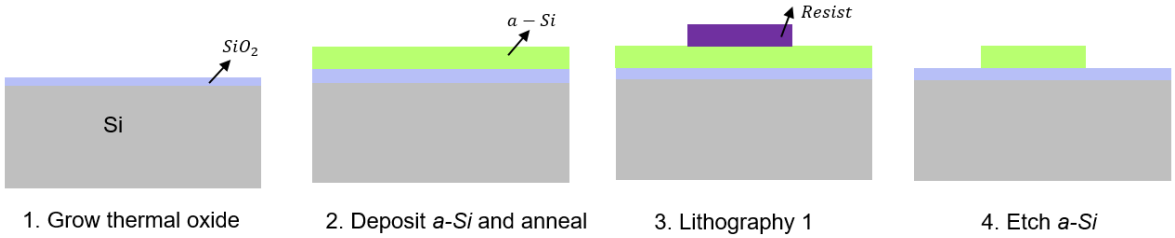

Figure 3.2: Schematic of the starting process flow steps for structure A and B. The process steps are: 1. 1 µm thick layer of thermal SiO_2 grown on a (100) silicon substrate. 2. 1 µm and 2 µm thick deposition of a-Si followed by annealing at 700 °C for 60 min. 3. Resist spin coating, patterning and development of the a-Si layer. 4. a-Si DRIE etching and resist removal.

The substrate used was 675 µm thick single side polished (SSP), boron doped (p-type) silicon wafers. The wafers were single crystal produced by Czochralski (CZ) growth, with <100> crystal direction. Each wafer was marked with an ID number using a diamond pen. Fourteen samples were fabricated (T1-T14). Wafers T1-T8 were used for structure A, and wafers T9-T14 for structure B. All the wafers required the same preparatory steps, which were ID marking and the standard cleaning sequence SC1 + HF + SC2, which is also known as RCA cleaning. [5] SC1 and SC2 cleaning were performed at 65 °C for 10 min and HF at room temperature for 30 seconds.

Thermal oxide was grown in step 1. The process was carried out using wet oxidation with a *Centrotherm horizontal furnace*. The wet oxide reaction growth is as follows: [5]

$$\mathrm{Si\ (s) + \ 2H_2O\ (g) \Longrightarrow SiO_2\ (s) + 2H_2\ (g)} \tag{3.1}$$

The thermal oxide was used as a passivation protection layer. Passivation layers are often used as a strategy to reduce charge recombination at surface states and to protect from chemical corrosion. [30] In our experiments, the passivation layer was used as a stopping layer to prevent etching of the Si substrate.

In step 2 a-Si, which is used as the sacrificial layer was deposited. The sacrificial layer is used to form a cavity after its release by XeF_2 etching. At the first attempt, a-Si was deposited using *PECVD Oxford Plasmapro system* equipment with the following parameters:

Table 3.1: PECVD a-Si deposition parameters.

Dep. time [min]	***Temperature [°C]***	***Pressure [mTorr]***	***Power [W]***	***SiH_4 flow* [sccm]**
20	300	900	20	50

PECVD a-Si is referred to as hydrogenated amorphous silicon (a-Si:H) because the films are incorporated with a large amount of hydrogen. This is because silane (SiH_4) is used as the source material and the deposition temperature is low. The PECVD a-Si:H reaction is as follows: [5]

$$\mathrm{SiH_4\ (g) \Rightarrow Si\ (s) + 2\ H_2\ (g)} \tag{3.2}$$

PECVD is a chemical vapour deposition process (CVD) with the addition of RF power used for parameter control. In the PECVD process, activated plasma enhances source gas decomposition and reaction. This makes PECVD suitable for low temperature processes. [5] A temperature around 300 °C is ideal in PMUT fabrication with incorporation of readout circuits. For this method, low temperatures are crucial to keep the readout circuits intact. A few challenges were, however, encountered with the use of PECVD a-Si:H for the process utilized in the experiments. The details are explained in Section 4. The fabrication process was followed using low pressure CVD (LPCVD). LPCVD a-Si also uses SiH_4 as source material. The reaction is the same as in Equation 3.2. However, higher temperatures are used.

The a-Si deposition was deposited using *Centrotherm horizontal furnace* with the parameters shown in Table 3.2. On four wafers (T1-T4) 1 µm thick a-Si was deposited. On wafers T5-T14 the deposited thickness was 2 µm. The wafers were then annealed at 700 °C for 60 min in N_2 flow in the same equipment. Annealing was performed for hydrogen release.

Table 3.2: LPCVD a-Si deposition parameters.

Temperature [°C]	*Pressure [mTorr]*	SiH_4 *flow [sccm]*
574	300	200

After a-Si deposition, photolithography was performed for patterning of the a-Si in step 3. These steps were carried out using a standard lithography process (Table 3.3). Spin coating was made using a positive resist.

When photoresist is exposed to ultra violet (UV) light, its chemical structure changes. The exposed areas on a positive resist will become soluble after exposure. With negative resist, the situation is the opposite. The exposed areas cause the photoresist to polymerize and it becomes difficult to dissolve. The *SPR700* positive photoresist is used to create the hill shape in structure A and *ma-N-1420* negative resist is used to create the valley in structure B (Fig. 3.1).

Exposure was carried out, followed by development and backing. After exposure, the a-Si was etched in step 4 by DRIE.

Table 3.3: Lithography and etching steps, parameters and equipment carried out to pattern the a-Si sacrificial layer.

Step	***Equipment***	***Parameters***
Spin coating	*Coater Developer EVG120*	SPR700
Exposure	*Wafer stepper CANON i3* i-line lithography	Wavelength = 365 nm Energy = 1500 J/m^2, Focus = 0.5 µm
Development	*Coater Developer EVG120*	110 °C 1 min
a-Si (1 um) Etching	*Silicon ICP etcher (Aviza)*	Standard Bosch process

The steps described so far were made for both structures. In the following sections, the continuation process for structures A and B will be explained separately.

3.2.1 Structure A: process fabrication

The continuation process steps for structure A will be presented here. The schematic with the process steps is presented in Figure 3.3.

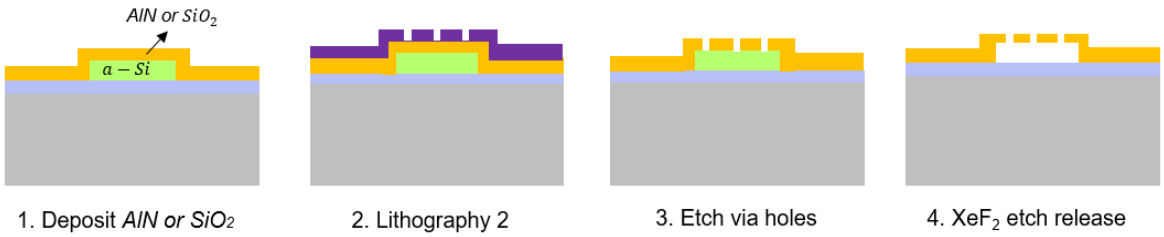

Figure 3.3: Schematic of the structure A fabrication process. The process steps are: 1. 1 µm deposition of either PECVD SiO_2 or sputtered AlN. 2. Resist spin coating, patterning and development of the via openings. 3. Plasma etching of via openings. 4. XeF_2 release of a-Si.

After a-Si patterning and etching, the membrane layer was deposited (step 1). Eight wafers (T1-T8) were used for the fabrication of structure A. On four wafers (T1, T2, T5 and T6) 1 µm thick layer of SiO_2 was deposited. The deposition was carried out using standard silane-based PECVD SiO_2. On the other half, wafers T3, T4, T7 and T8, a 1 µm layer of AlN was deposited. The aim was to deposit each membrane film on two wafers containing 1 µm thick a-Si and on two wafers with 2 µm thick a-Si. Therefore, four wafers were used for each membrane film. The parameters used for the SiO_2 and AlN depositions are shown in Table 3.4. SC1 cleaning was performed before each deposition.

Table 3.4: SiO_2 and AlN deposition parameters.

Equipment (AlN)	***Pressure [mbar]***	***Power [kW]***	***Ar [sccm]***	***N_2 [sccm]***	***Time [s]***
AlN Sputtering System AMS2004	$4.25\ X\ 10^{-3}$	7	18	40	850
Equipment (SiO_2)	***Pressure [mTorr]***	***Power [W]***	***SiH_4 [sccm]***	***N_2O [sccm]***	***N_2 [sccm]***
PECVD Oxford Plasmapro system	1000	20	8.5	710	161.5

After membrane layer deposition, the second lithography and etching processes were carried out in step 2 and 3 to pattern and etch the via holes on the structural layer. The steps, equipment and parameters are shown in Table 3.5.

Table 3.5: Lithography and etching steps, equipment and parameters to pattern the via openings on the structural layer.

Step	***Equipment***	***Parameters***
Spin coating	*Coater Developer EVG120*	AZ9235 4.8 μm
Exposure	*Wafer stepper CANON i3 i-line lithography*	Wavelength = 365 nm Energy = 3500 J/m^2, Focus = 0.5 μm
Development	*Coater Developer EVG120*	Develop only 4 min
AlN (1 μm) Etching	*Metal etcher LAM TCP 9600*	180 s approx. etch rate: 400 nm/min, $BCl_3 + Cl_2$
SiO_2 (1 μm) etching	*Oxide etcher LAM 4520*	150 s approx. etch rate: 500 nm/min, CHF_3 + Ar

In the last process step (step 4), the a-Si was released from the structure using XeF_2 etching. The etcher was running in pulse mode with the following parameters:

Table 3.6: XeF_2 etching process parameters for release of a-Si

Equipment	***number of pulses***	***pulse time [s]***	***XeF_2 pressure [Torr]***	***N_2 pressure [Torr]***
SPTS Xactix Xetch X4 Series XeF_2 Etcher	40	30	3.0	10

The XeF_2 etching was carried out on four wafers, two wafers containing SiO_2 as membrane layer and two containing AlN (one with 1 µm thick a-Si wafer and the other with 2 µm thick a-Si).

The complete process flow steps for structure A is presented in Figure 3.4.

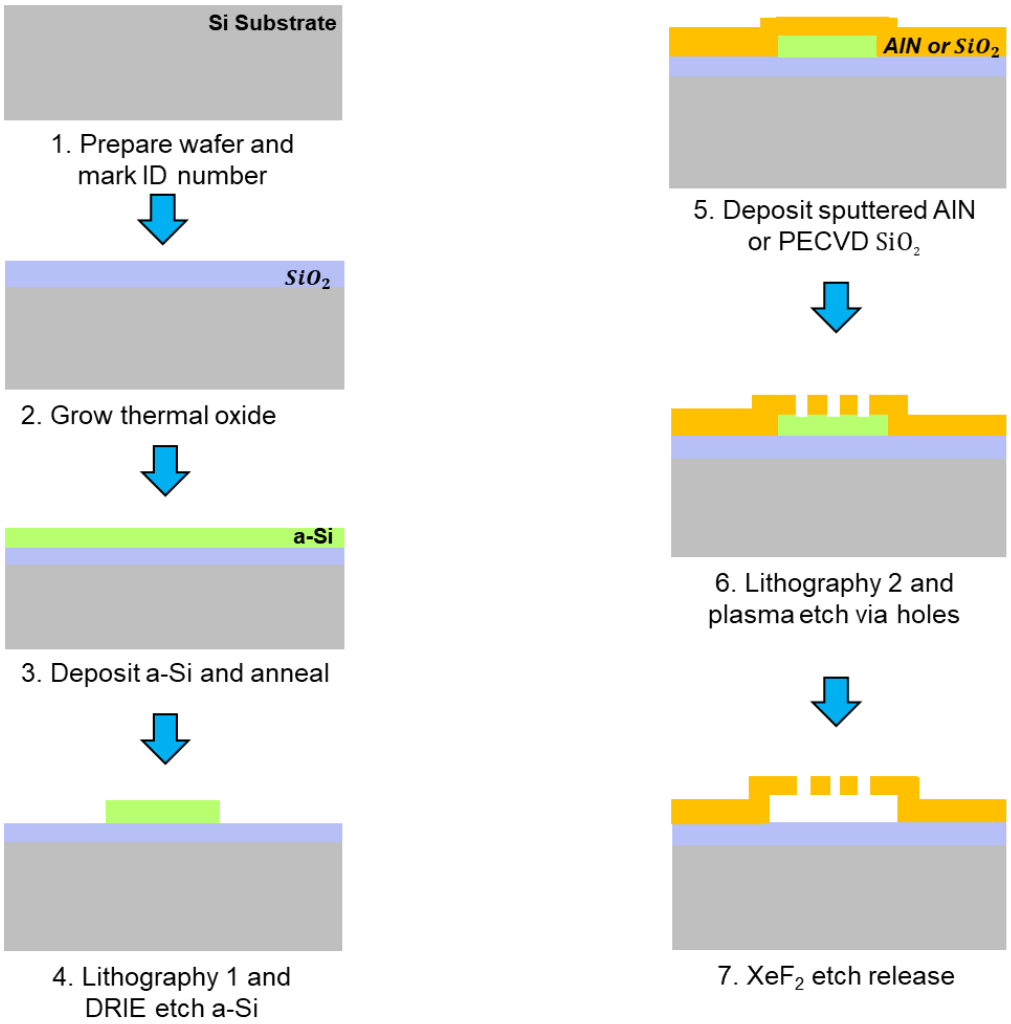

Figure 3.4: Schematic of process flow for structure A. Steps 1 to 4 are the general process steps used for structures A and B. Steps 5 to 7 are the steps carried out only for structure A.

After a-Si release, the samples with structure A were ready for analysis. In the following section, the continuation process steps for structure B will be explained.

3.2.2 Structure B: process fabrication

Here, the continuation process steps for structure B will be presented. The starting process for structure B was the same as for structure A (Figure 3.2). The schematic with the continuation process steps is presented in Figure 3.5 and the complete process flow in Figure 3.6.

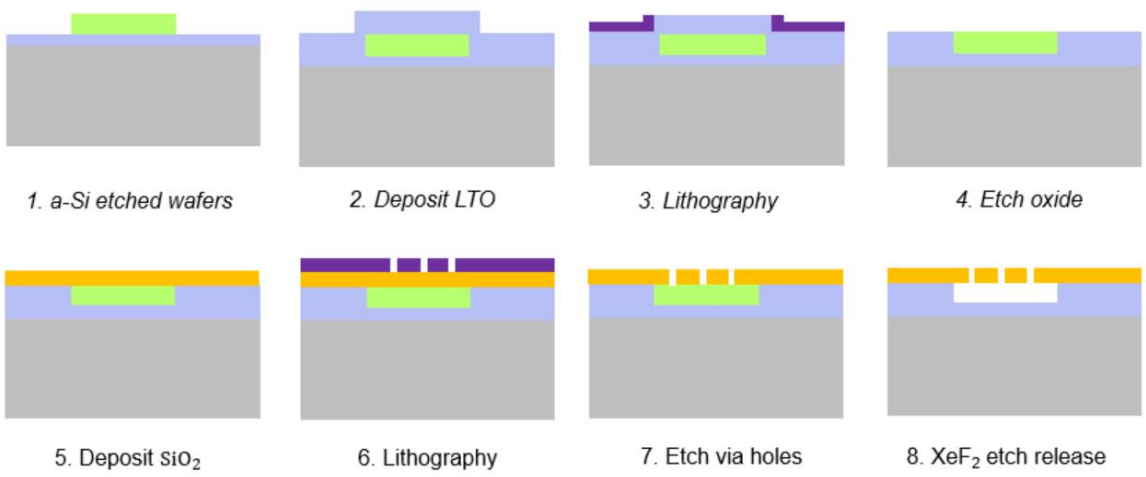

Figure 3.5: Schematic of the structure B fabrication process. The process steps are: 1. Wafer after DRIE etching of a-Si. 2. 2 µm thick deposition of PECVD SiO_2. 3. Resist spin coating, patterning and development of the SiO_2. 4. SiO_2 plasma etching. 5. 2 µm deposition of PECVD SiO_2 only or followed by 1 µm thick sputtered AlN. 6. Resist spin coating, patterning and development of via openings. 7. Plasma etching of via openings. 8. XeF_2 release of a-Si.

In total, six wafers (T9-T14) were utilized to fabricate structure B. After DRIE etching of the a-Si, SC1 cleaning was carried out followed by SiO_2 deposition (step 2). The SiO_2 was deposited using same parameters as in Table 3.4.

In step 3, a negative resist was used to pattern the SiO_2 layer. Standard lithography patterning was carried out and the SiO_2 was etched down using the *Oxide etcher LAM 4520* standard SiO_2 etching process (step 4). The lithography and etching steps, and parameters are shown in Table 3.7. SC1 cleaning was carried out once more and another 2 µm layer of PECVD SiO_2 was deposited on step 5. On one wafer, an additional layer of AlN was sputtered on top of the SiO_2 using the same equipment and parameters shown in Table 3.4. On this wafer the via holes were first etched on the AlN layer then on the oxide layer using the same steps shown in Table 3.5.

Table 3.7: Lithography and etching steps, equipment and parameters to etch down the silicon dioxide.

Step	***equipment***	***Parameters***
Priming	*Primer oven YES-3*	HDMS 150 °C 20 min
Spin coating	*Manual spinner LSM 200*	ma-N-1420
Soft bake	*Coater Developer EVG120*	100 °C 3 min
Exposure	*Wafer stepper CANON i3* i-line lithography	Wavelength = 365 nm Energy =1200 J/m^2, Focus = 0.5 μm
Development	*Fumehood DEVELOP*	2 min
Etching	*Oxide etcher LAM 4520*	CHF_3 + Ar

The patterning and etching steps were carried out the same manner as in steps 2, 3 and 4 described in the structure A: process fabrication Section and shown in Figure 3.3. The complete process flow for structure B is presented in Figure 3.6.

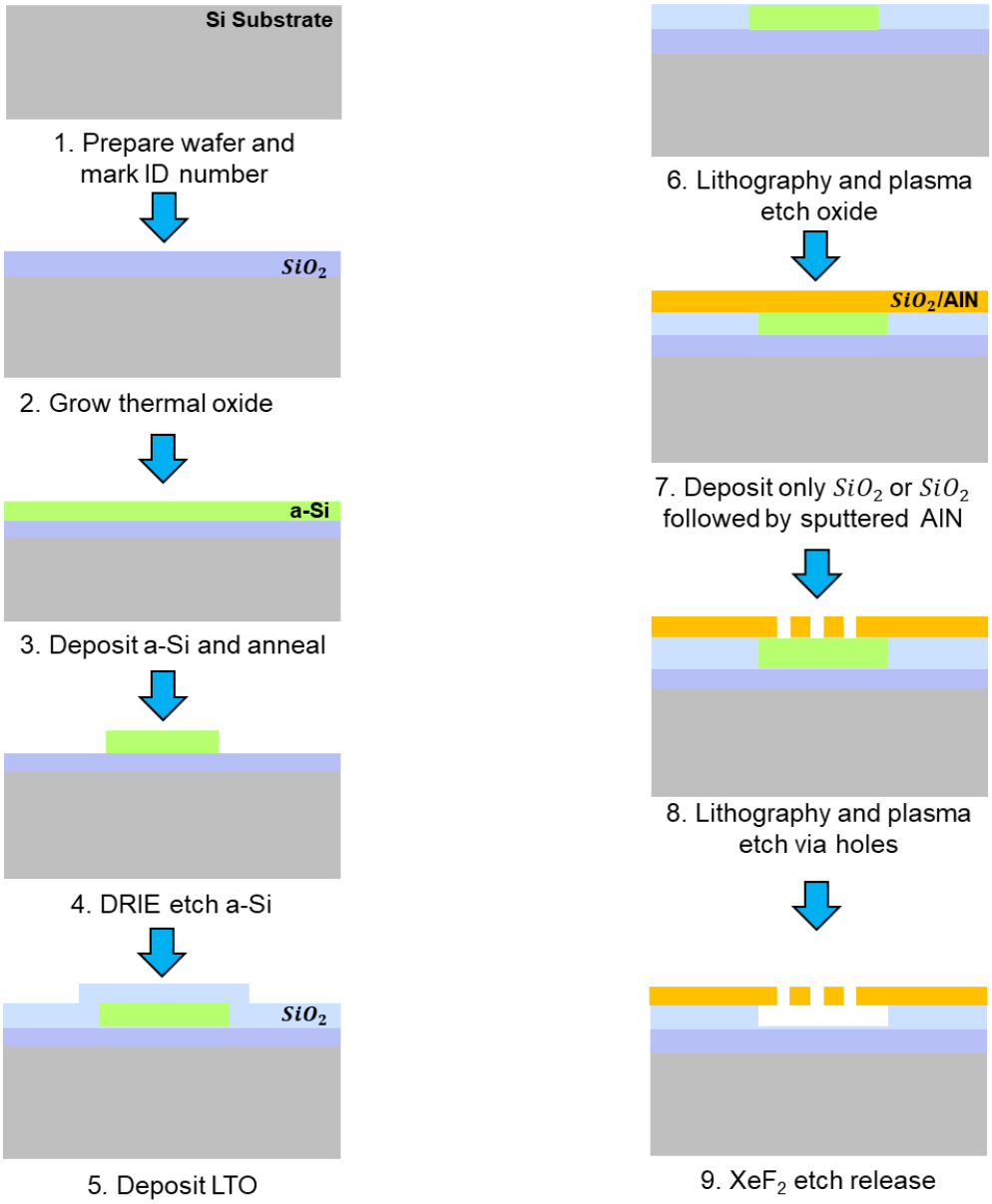

Figure 3.6: Schematic of process flow for the structure B. Steps 1 to 4 are the general process steps used for structures A and B. Steps 5 to 9 are the steps carried out only for structure B.

After XeF_2 release of the a-Si, the samples with structure B were ready for analysis. The following sections explain in more in detail the designs used for the diaphragm and for the via openings.

3.3 Diaphragm and via opening design

The structures described in the previous section were made using several cavities diameters. Additionally, the a-Si etching rate was tested using via openings of different numbers, shapes

and dimensions. In this section, the design used for the diaphragm and for the via openings will be explained.

Two mask processes were used for the fabrication of the structures:

1. a-Si patterning and etching
2. Patterning and etching of via openings for XeF_2 release

The reticle utilized for the patterning of these structures is shown in Figures 3.7 a and b.

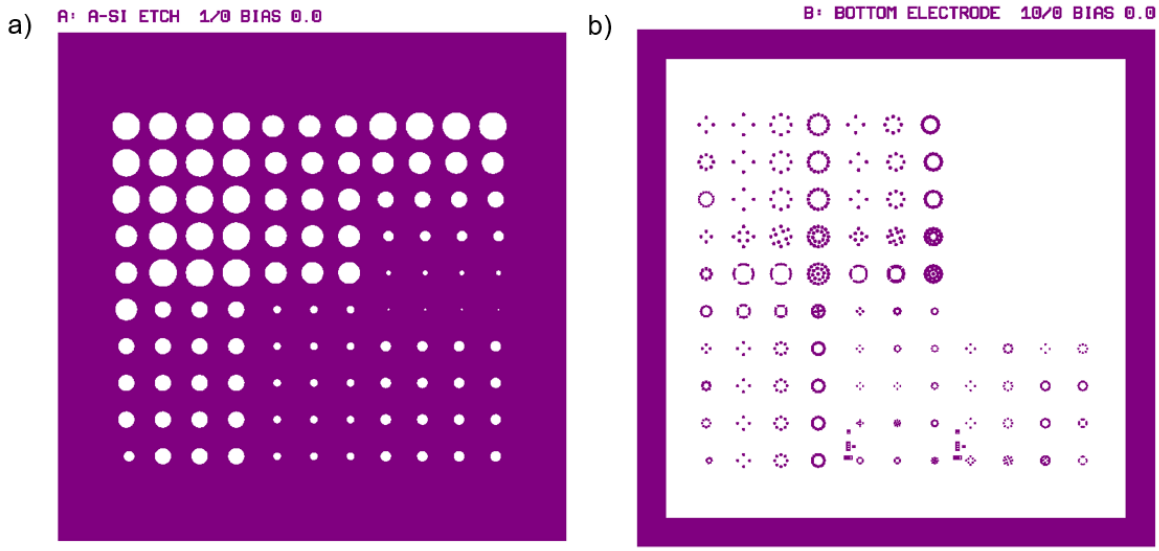

Figure 3.7: Reticle used in the fabrication of structures. The mask consists of: a) Patterns used for diaphragm lithography and b) Patterns used for via openings lithography.

The structures on the mask shown in Fig. 3.7a consist of a single chip pattern with several circles. This pattern is used to define the diaphragm of the PMUT structure. The experimental part of this work consists of testing the structures with cavities of different dimensions. Diameters from 50 to 500 µm were used, as it can be seen from Figure 3.8.

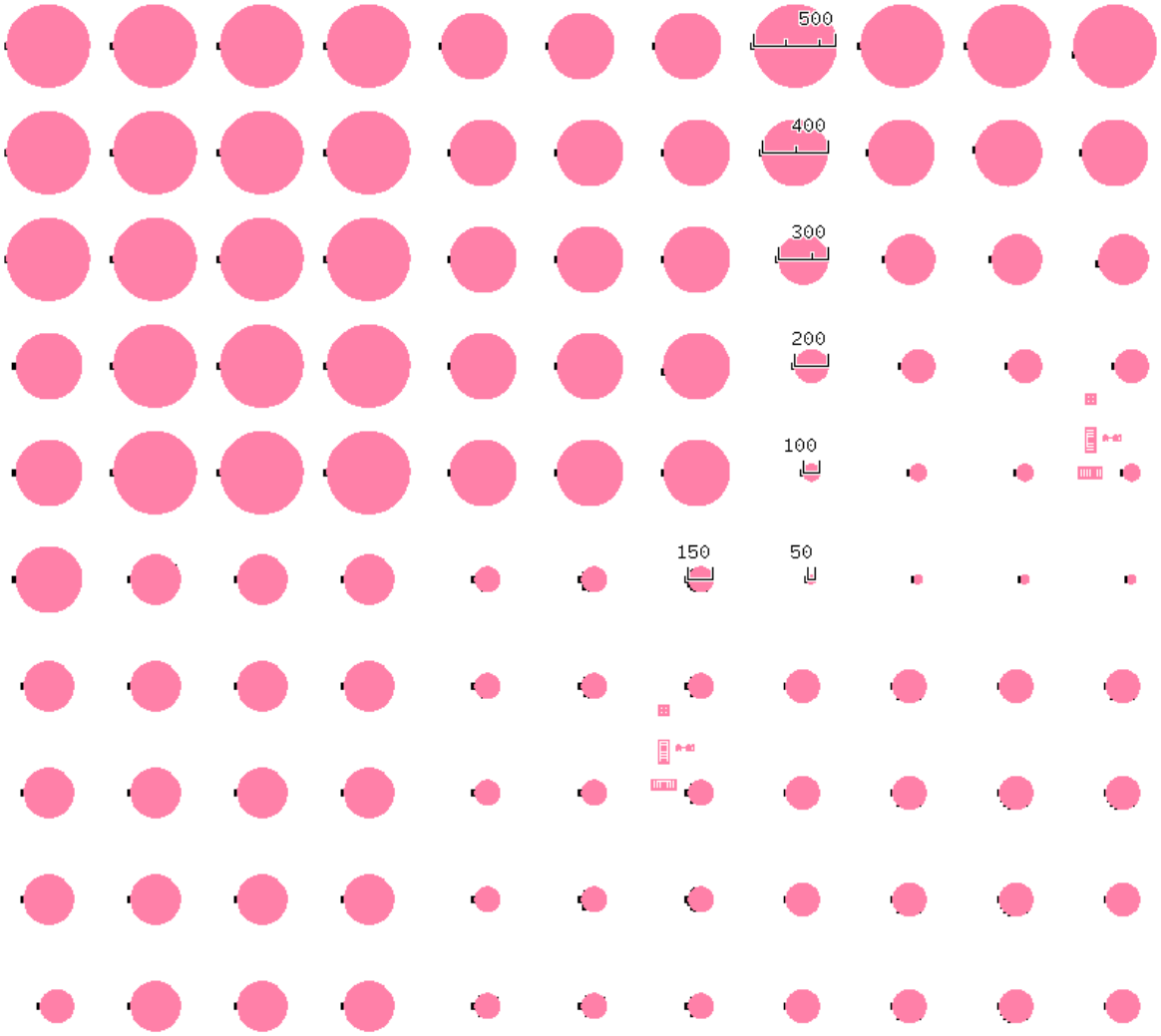

Figure 3.8: Mask with diaphragm pattern. The pattern consists of circles used for lithography of the diaphragms on the a-Si layer. Several dimensions were utilized with diameters of 50, 100, 150, 200, 300, 400 and 500 µm.

The PMUT structures tested in this work are intended to be used for air-coupled and water-coupled device applications. The aim is to obtain air-coupled devices with frequencies in the range of 100 to 200 kHz and water-coupled devices with frequencies around 2 to 3 MHz. The size of the cavity defines the device frequency. Hence, the structures are tested with several dimensions. The size of the cavity is inversely proportional to the frequency: the bigger the cavity the lower the frequency.

Figure 3.7b, shows the via opening patterns. The via openings were tested in three different shapes, presented in Figure 3.9.

Figure 3.9: Via opening patterns used for the XeF_2 release. a) Circular-shaped via for top release. b) Arc-shaped via for top release. c) Square-shaped via for side release.

From Figure 3.7b it is possible to observe that the pattern for the holes consists of different numbers and dimensions. The release of the structures was tested with via openings of different numbers. The tested numbers were 4, 8, and 16. The experiments were also carried out with openings with diameter/thickness of 2.5 µm, 5 µm, 10 µm and 20 µm. This method was used to verify which via opening size, geometry and number would allow better and faster release of the a-Si by XeF_2.

3.4 Characterization methods

In this section, the characterization methods used for the structures will be presented and explained. Several characterization steps were carried out to analyse film thickness, film stress, etching rate and uniformity, and released structure profile.

3.4.1 Film thickness and stress

The thickness and thickness uniformity of the deposited thin films were characterized using a *Reflectometer FilmTek 2000M* equipment.

The stress of the films was measured using an *FLX-2320-S Thin-film stress measurement instrument.* The FLX-2320-S is a thin film stress measurement instrument, which measures the changes in the radius of curvature of the substrate caused by the deposition of a stressed film on the substrate. [31] The stress was defined by scanning the wafer to obtain first the bow after a-Si deposition and then the stress caused by the membrane films after deposition.

The stress is calculated from the thin film stress equation:

$$\sigma_{film} = \frac{1}{6}\frac{E_s}{1-v_s}\frac{t_s^2}{t_f}\left[\frac{1}{R_f} - \frac{1}{R_s}\right] \quad (3.3)$$

Where, E is the Young's modulus, defined as stress/strain, v is Poisson's ratio, t_s is substrate thickness and t_f is film thickness, R_s is substrate radius of curvature and R_f is film radius of curvature.

3.4.2 XeF_2 etching characterization

The release of the a-Si was observed using an optical microscope. With an optical microscope, it is possible to visualize submicron structures, determine surface profile and observe selected cross sections without cutting the sample into thin slices. [32] [33] For this reason, it is possible to observe the a-Si release within the structures without having to cut the samples.

Typically, on a single sample wafer, several chips are fabricated. For each analysed sample, five chips were observed under the microscope. The locations of the observed chips on the sample wafer can be seen in Figure 3.10.

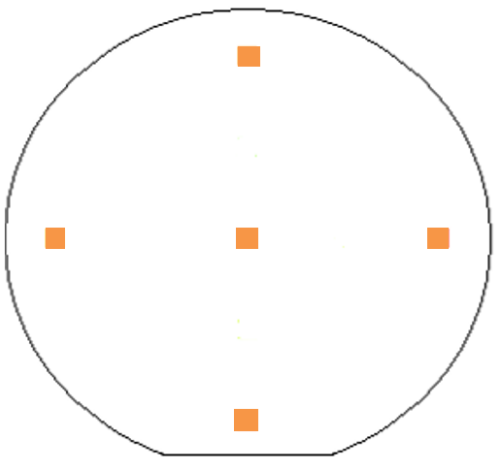

Figure 3.10: Sample wafer illustration with the location of the analysed chips. Five chips were observed with the optical microscope for each sample. One on the left, one on the right, one in the middle, one at the top, and one at the bottom.

Each chip observation was made in sections. In each section, it was possible to observe around 12 structures. A picture was taken from each section and a whole image of the chip was formed using a total of twelve images. One example is shown in Figure 3.11.

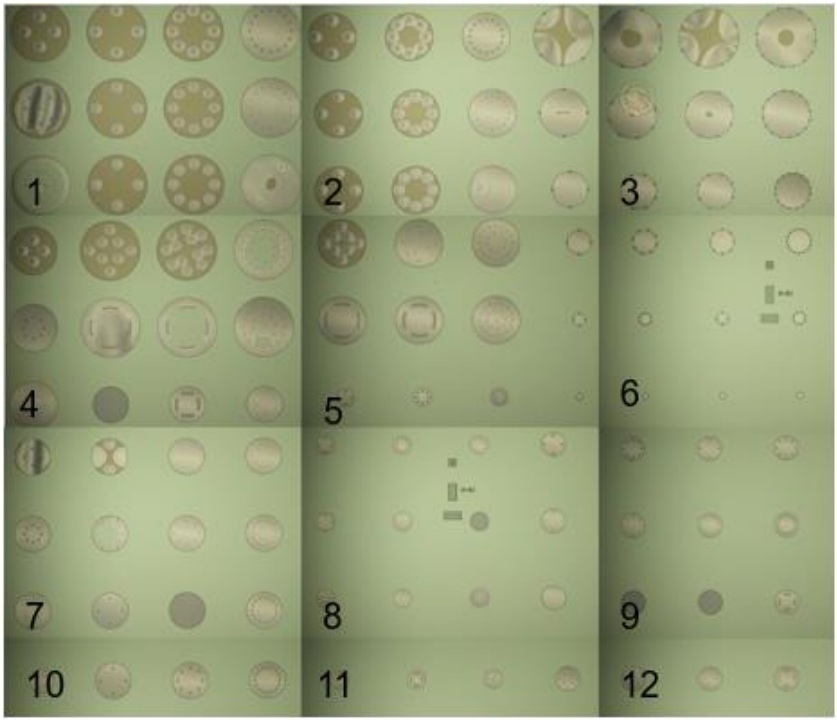

Figure 3.11: Optical microscope images of sections attached together to form a picture of the whole chip. Twelve images were taken from twelve sections of the chip to form a single image.

Once the images were attached as a whole, the etching uniformity of the structures and etching rate were analysed. The vertical etching rate of the a-Si was characterized by measuring the thickness difference and the lateral etching rate, by measuring the etching distance. The etching distance was obtained on the microscope images by using a length ruler measurement on the *Nikon microscope Eclipse L200* software.

3.4.3 Structures profile characterization

The obtained structures profile was characterized with an optical profilometer using *Profilometer Veeco Dektak V200Si* equipment. Profilometry is a technique used to extract topographical data from a surface. With profilometry it is possible to obtain surface morphology, step heights and surface roughness. An optical profilometer uses light instead of a physical probe as in contact profilometry. [34] To perform the structure characterization, around 21

structures were observed. A smaller number of structures were characterized in case of difficulties to find 21 intact or etched structures. The structures were located on the chip using an x-y coordinate graph as shown in Figure 3.12. The analysed structures coordinates are as follows: (1,3), (2,1), (2,5), (2,6), (4,7), (5,1), (5,4), (5,5), (5,6), (6,3), (7,8), (7,9), (8,2), (8,3), (8,4), (8,5), (8,6), (8,7), (8,8), (9,5), and (11,1). The circles on the images represent each coordinate. The idea was to measure at least one or two structures of each dimension and via opening.

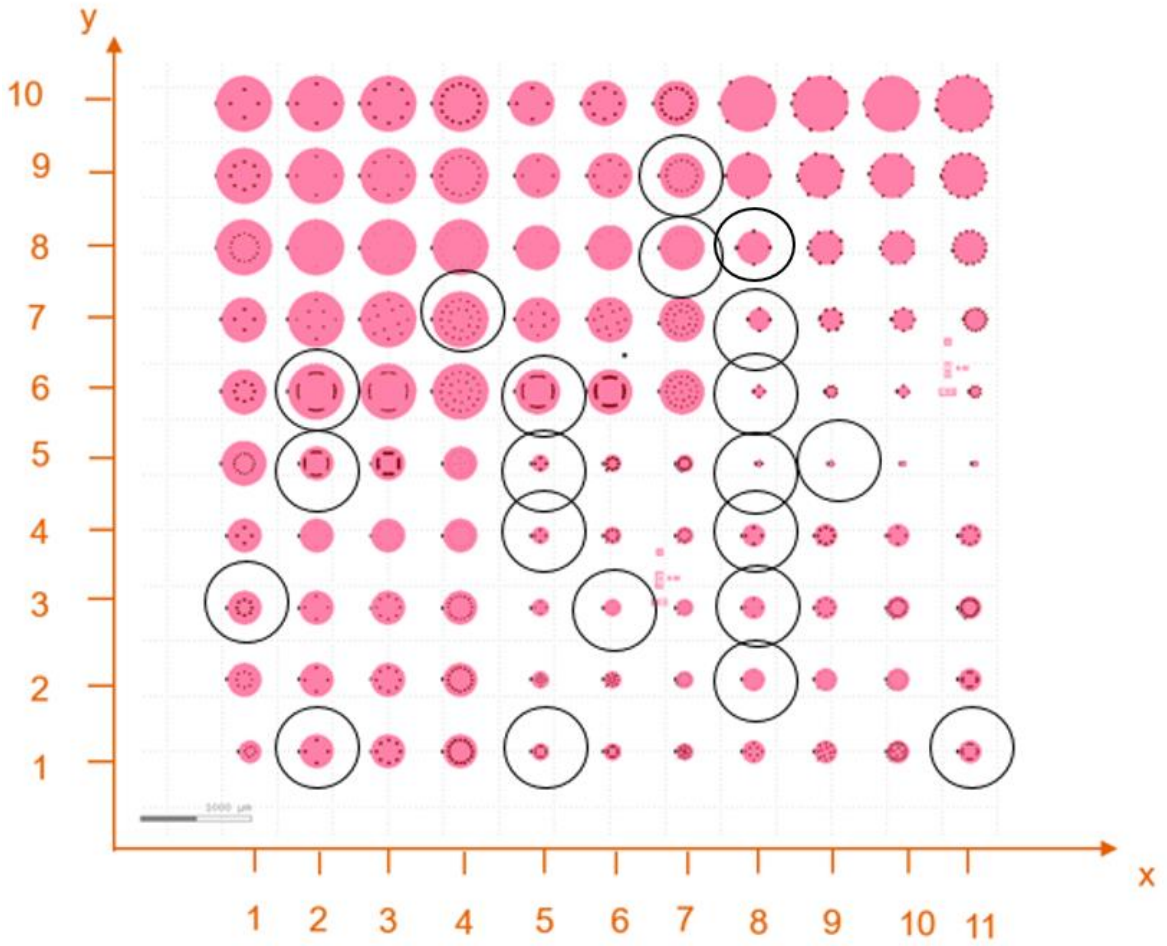

Figure 3.12: x-y coordinate graph made for optical profilometer characterization. All the analysed structures and their respective coordinates are marked on the image.

With the optical profilometer analysis, it was possible to observe where the structures were intact or if they collapsed after etching.

4 Results and Discussion

This section presents the results obtained from the performed experiments. The results are presented, explained and discussed. The section is divided into two parts. In the first part, the results involving a-Si deposition, diaphragm etching profile and XeF_2 etching rate are presented and deliberated. In the second part, the final structures after XeF_2 etching are presented.

4.1 a-Si deposition, diaphragm etching profile and XeF_2 etching rate

This part of the work is reserved to discuss the results relating to a-Si deposition, diaphragm profile after DRIE etching and the release rate of a-Si from the structures using XeF_2 etching method.

4.1.1 a-Si film deposition method

The PECVD a-Si deposition process was optimized in order to obtain a-Si film with low stress and good uniformity. The optimization was made using design of experiments (DOE) analysis method. The DOE was based on the Taguchi L9 method. The process development was carried out using three factors: chamber pressure (mTorr) during deposition, SiH_4 flow (sccm) and radio frequency (RF) power (W). For each factor, three levels were used: low, middle and high. In total nine depositions were carried out, followed by more three depositions repeating the process parameters which gave best results. The parameters levels for each factor is shown in Table 4.1.

Table 4.1: Factors and parameter changes performed during DOE analysis.

Input	*Low*	*Mid*	*High*
Pressure [mTorr]	700	900	1100
RF Power [W]	10	20	30
SiH_4 [sccm]	25	30	50

The parameter levels for pressure were changed in steps of 200 mTorr per run starting from 700 mTorr for the lowest level and 1100 mTorr for the highest level. RF power was changed

in steps of 10 W with 10 W for the lowest level and 30 W for the highest. The silane flow was intended to be changed in steps of 20 sccm per run, however, flows under 20 sccm is not supported by the equipment. Therefore, the parameter level was adapted to the lowest possible flow.

In total, nine depositions were carried out. The result for each run can be seen from Table 4.2.

Table 4.2: DOE test run parameters and results. Run 8 with the best results is highlighted.

Run number	*Wafer ID*	*Pressure [mTorr]*	*RF Power [W]*	*SiH_4 [sccm]*	*Thickness [nm]*	*Thickness uniformity [%]*	*Stress [MPa] 0°*	*Stress [MPa] 90°*	*DR [nm/min]*
1	4	700	10	50	383	7.08	287	295	19
2	5	900	10	50	374	4.62	257	247	19
3	6	1100	10	50	142	15.56	340	268	7
4	7	900	10	50	240	4.15	-316	-326	12
5	8	900	20	50	1217	3.2	49	49	61
6	9	900	30	50	1696	1.94	105	100	85
7	10	900	20	25	1362	0.74	-31	-31	68
8	**12**	**900**	**20**	**30**	**1252**	**0.61**	**17**	**15**	**63**
9	11	900	20	50	1119	0.69	61	66	56

In the first three runs, RF power and SiH_4 flow were fixed, and pressure was changed. The best results were obtained in run number 2. Therefore, the pressure was set to 900 mTorr for the subsequent runs.

For the second test, pressure and SiH_4 flow parameters were fixed and RF power values were altered. Run number 5 gave the best stress and uniformity values. The RF power was then fixed to 20 W.

In the final run, pressure and RF power were fixed and SiH_4 flow was changed. Test run number 8, with pressure at 900 mTorr, RF power at 20 W and SiH_4 flow at 30 sccm gave the best results. The parameters used for this run presented the lowest stress and the best thickness uniformity, as well as high deposition rate. These result values are better than the results presented in [35] using the same equipment.

Residual stress control, film thickness and thickness uniformity of the sacrificial layer have a great impact on the diaphragm of the PMUT. The residual stress can affect the final stress on the structural layer after release, as demonstrated in [36]. Additionally, the thickness of

the sacrificial layer defines the depth of the cavity. The possibility to deposit thicker films expands design possibilities.

The parameters used for test run number 8 were repeated for three more wafers. The results are presented in the following table:

Table 4.3: Results obtained from repetition of the parameters used in test run number 8.

Wafer ID	*Stress Avg. [MPa]*	*Thickness [nm]*	*Thickness uniformity [%]*	*Deposition rate [nm/min]*	*Deposition time [min]*
12	16	1252	0.6	63	20
13	0	1161	4.7	58	20
14	3	1180	4.6	59	20

For all the repeated samples the residual stress continued as tensile and low, varying from 0 to 16 MPa as shown in Table 4.3.

Although good results were obtained with the developed PECVD a-Si deposition, some challenges were encountered throughout the process.

The AlN film was deposited following the PECVD a-Si deposition process. After AlN deposition, bubbles and peeling of the a-Si film were observed. The described phenomena can be seen in the following figure:

Figure 4.1: Sample wafer with annealed PECVD a-Si film. The a-Si was deposited on top of SiO_2 using PECVD at 300 °C and then annealed at 450 °C for 60 minutes.

Fig. 4.1 is from a sample wafer containing a layer of PECVD a-Si on SiO_2 deposited on a Si wafer. The sample was annealed after film deposition. Based on the results of previous investigations, the cause relating to this problem is associated with outgassing of hydrogen. The utilized PECVD a-Si has a high hydrogen content, since the source gas was SiH_4. The a-Si deposition temperature was 300 °C and the tested structures were subjected to higher temperature during post deposition annealing and AlN deposition. When there is an increase in temperature in the steps following a-Si deposition, e.g. annealing or processes with higher temperatures, this results in the release of hydrogen bonds. This outgassing effect results in bubbles under the film. Studies on the effects of temperature on a-Si by methods of annealing have demonstrated that the release of hydrogen bonds occurs at temperatures around 400 °C. [37] In studies performed on annealing effects on hydrogenated a-Si, [38] it was shown that outgassing can occur in three stages with thresholds at 350°C, 450°C and 575°C.

When peeling of a-Si was observed, annealing tests were performed to determine whether the bubble formation was related to the difference in temperature. Figure 4.1 presents one sample wafer which went through the annealing process. After the annealing time, several bubbles could be seen throughout the wafer as well as peeling on the corners. The annealing test was carried out on two sample wafers which returned similar results.

In previous investigations, PECVD a-Si was used together with low temperature AlN. [19] [7] In these papers, both the a-Si and the AlN deposition processes are CMOS compatible and no outgassing of the a-Si is reported.

Because of aforementioned problems, the process was adapted with the use of LPCVD. In LPCVD deposition of a-Si, silane is also used as source material, however, temperatures between 540 and 640 °C are used. Furthermore, post deposition annealing of the film was carried out at 750 °C. The higher temperature deposition and annealing processes prevent outgassing of the film during AlN deposition.

4.1.2 DRIE etching of a-Si for diaphragm profile

The results relating to DRIE etching of the a-Si are presented here. DRIE etching was performed to create the diaphragm shape on the a-Si. The a-Si profile after etching determines

the device cavity dimensions such as diameter and depth. DRIE etching is an anisotropic etching method, which allows a vertical sidewall profile. Figure 4.2 shows an SEM image of a-Si after DRIE etching.

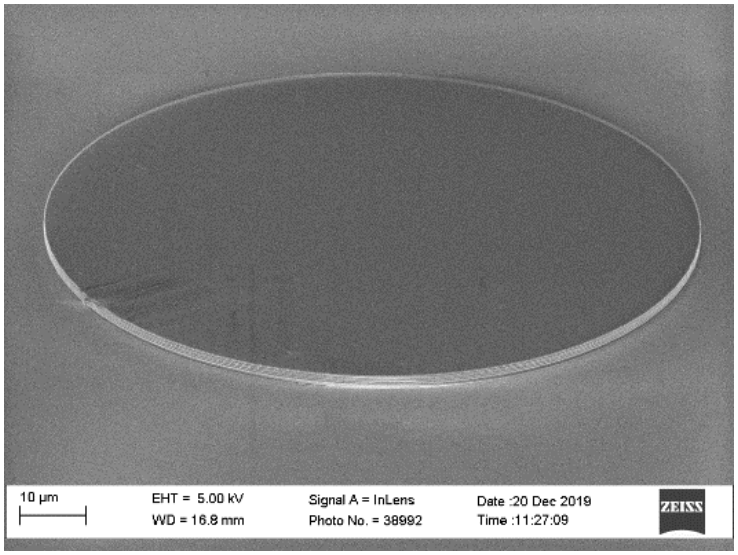

Figure 4.2: SEM image after deposition, patterning and DRIE etching of a-Si. This image shows the pattern formed after the lithography step on the a-Si layer before deposition of the structural layer. The image shows a single pattern from structure design A. The pattern height is 1 µm which, after a-Si release, will give 1 µm depth to the cavity defining the diaphragm.

The etching method defining the diaphragm profile is important because the shape and thickness of the sacrificial layer defines the shape and depth of the device cavity after release. This is crucial because the resulting PMUT performance is dependent on the diaphragm geometry.

Before choosing DRIE as the etching method, two other different etching processes were tested: wet etching using standard buffered hydrofluoric acid (BHF) and plasma etching with *LAM poly-Si etcher*. BHF was used to test a-Si selectivity. Plasma etching was made with the aim of achieving a slope on the sidewalls of the diaphragm.

As expected, wet etching using BHF did not etch a-Si. BHF is mainly used to etch SiO_2 and it has a relatively low etching rate on Si, as it is demonstrated in [39]. Therefore, no changes were observed in the a-Si thickness.

The results from plasma etching were not as expected. The utilized process was not suitable and problems were encountered during the etching process. After etching, resist formed particles on the sample wafer surface and its removal was challenging. Optimization of the process was not carried out and therefore, further studies are necessary. However, sidewalls slope was already demonstrated to be possible in previous studies. [40]- [42].

After the attempt to etch sloped sidewalls by LAM poly-Si plasma etching, DRIE etching method was tested and used.

4.1.3 Diaphragm release by XeF_2

The etching results of a-Si by XeF_2 are presented in this section. Experimental tests of the XeF_2 etching process were made in order to identify the most suitable recipe for release of the structures. Uniform release was required to characterize the etching rate of the structures by their respective dimensions. The performed steps and parameters are presented in the following table:

Table 4.4: XeF_2 etching process parameters.

	Number of cycles	***cycle time [s]***	***Etch delay [s]***	***XeF_2 Pressure [Torr]***	***N_2 Pressure [Torr]***
Test 1	20	30	5	3.0	0
Test 2	10	15	5	3.0	10
Chosen parameters	40	15	5	3.0	10

The parameters used were based on previously developed recipe. In the first step, the process was performed without N_2 pressure and with a longer etching time per pulse (30s). In the second test, N_2 pressure was added and the etching time per pulse was decreased (15s). The parameters were then set as shown in Table 4.4.

Before release of a-Si from the structures, the vertical etching rate of a-Si by XeF_2 etching was verified. For the experiment a test mask was used. With the test mask, small squares were patterned on the wafer sample and the a-Si was released from these squares. The total etching time was 10 minutes and the thickness was verified always after 1 minute of etching. The thickness difference was measured and the data was used to create a graph representing

thickness as a function of etching time. The graph is presented in Figure 4.3. A linearization of the points was made and the etching rate was obtained from the slope.

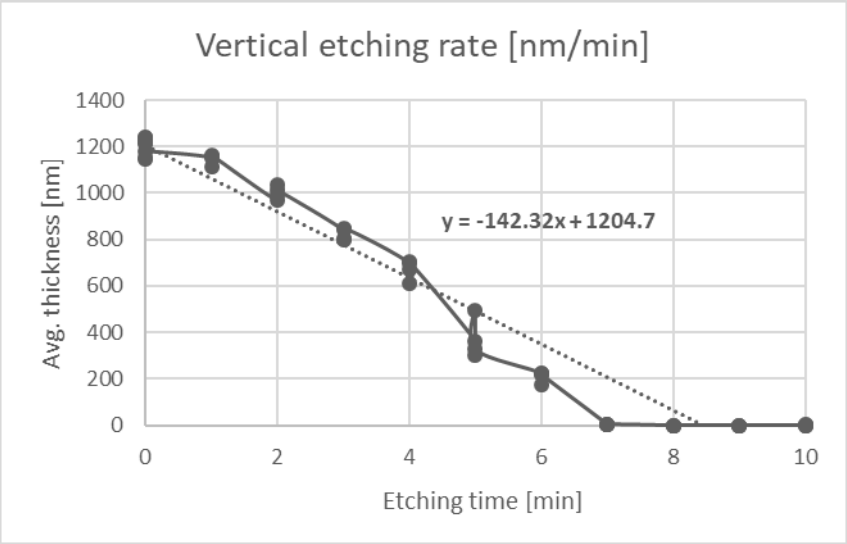

Figure 4.3: Graph representing the average thickness of a-Si as a function of etching time. After linearization of the data, it was possible to obtain the etching rate from the slope represented in the equation.

After the vertical etching rate was verified, the release of the a-Si from the structures was carried out using the parameters shown in Table 4.4. The release was characterized using an optical microscope. Figure 4.4 shows two microscope images after XeF_2 release of a-Si from the structures.

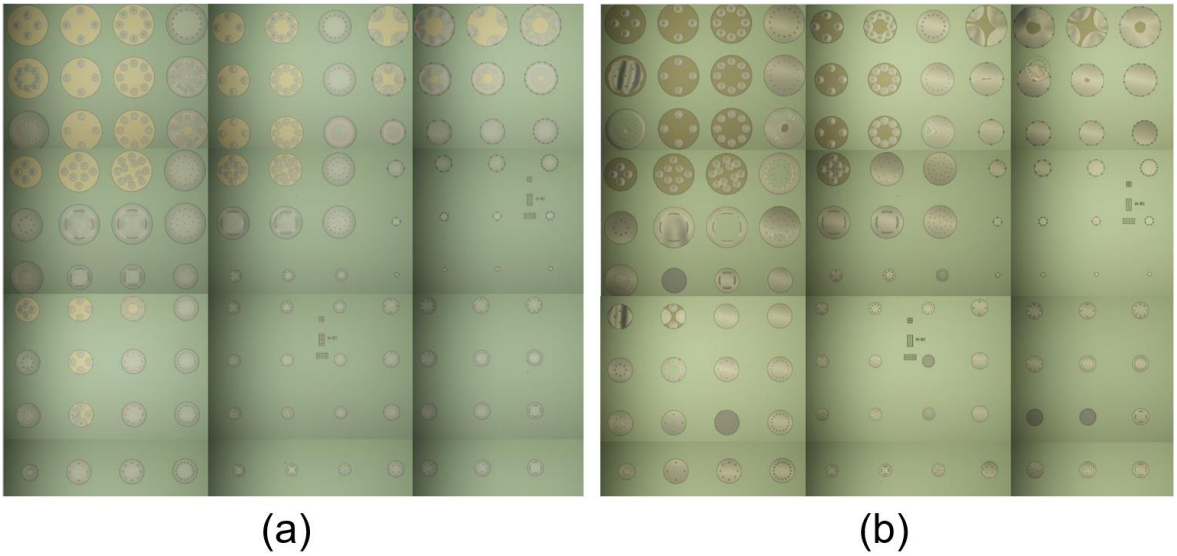

Figure 4.4: Microscope images of the structures after XeF_2 release of the a-Si sacrificial layer. The images consist of: (a) a single chip image from a sample wafer with SiO_2 as structural layer after the release of 2 µm thick a-Si and (b) a single chip image from a sample wafer with AlN as structural layer after the release of 2 µm thick a-Si.

For each analysed wafer, five chips were observed under the microscope. The location area of each observed chip is shown in Figure 3.10 (Section 3). A collection of twelve images was put together to create a single chip image (Figure 3.11). The pictures in Figure 4.4, show two different chips belonging to two different sample wafers. The chips in these images were taken from the middle area of the wafers. Both images are from sample wafers in which structure A design was fabricated. The samples in both images were observed under the microscope after 20 minutes of exposure to XeF_2. The grey colours are the areas without a-Si and the yellowish/brown areas are the areas where a-Si was not released.

The images containing 1 µm a-Si are not presented here for comparison because the amounts of released a-Si for both thicknesses are very similar. This is because the etching rate of XeF_2 is affected more by the exposed area than by the thickness. [6] Therefore, it is of more interest to compare the obtained etching results based on structural layer material rather than on a-Si thickness.

From Figure 4.4 (a) and (b), it is possible to observe that a-Si release was achieved almost on all structures after only 20 minutes of etching. Even for some structures with bigger dimensions, it was possible to obtain total release. This shows that with longer time, it would be possible to fully release bigger structures with less and smaller via openings. This is similar to results reported in [19].

The amount of exposed area is an important factor in the etching rate of XeF_2. The size of the area is inversely proportional to the etching rate. Bigger areas take longer to etch. For this reason, it was already expected that bigger structures containing small openings and less holes would be more challenging to etch. The area dependence for etch rate characterization is demonstrated in [7] and [29].

To analyse the etching rate for each design, the lateral etching distance was measured. From Figure 4.4, it is possible to observe that most structures with diameter of 500 µm did not etch completely. These structures were used to analyse the etching distance, by measuring the radius length from the via opening to where the etching stopped. The method is illustrated in Figure 4.5.

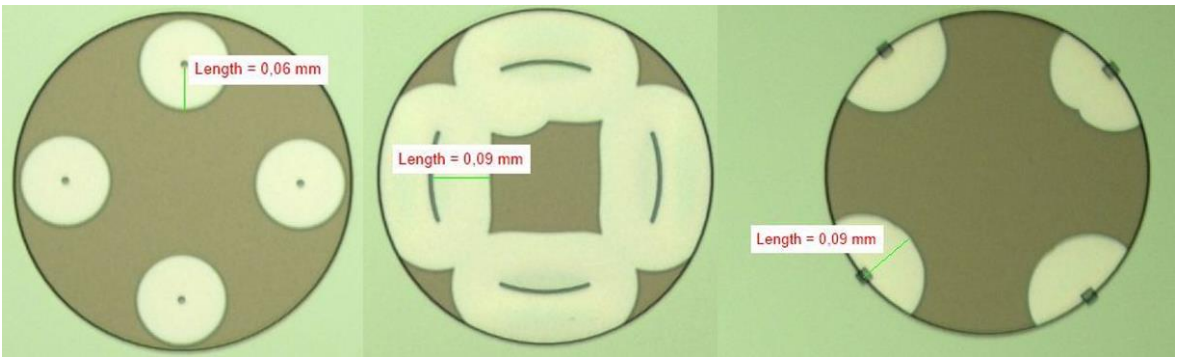

Figure 4.5: Etching radius length measurement made for each via hole design to analyse the lateral etching rate.

The structures in the image were observed under the microscope after 15 minutes of etching. The light colours are the areas without a-Si and the brown areas are the areas where a-Si was not released.

The etched radius length was measured after 15 and 20 minutes of etching. The data was used to create a graph representing the etching distance as a function of etching time. After linearization, the etching rate was determined from the slope (Fig. 4.6).

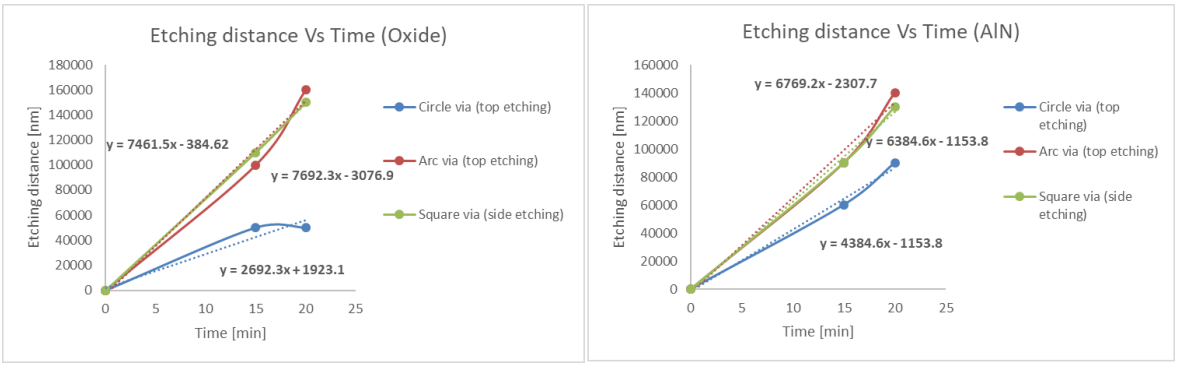

Figure 4.6: Graph representing the etching distance as a function of etching time. After linearization of the data, it was possible to obtain the etching rate from the slope represented in the equations. The graph in the left is from structures containing only silicon dioxide in the structural layer and the graph in the right only AlN.

The etching distance was measured for each via geometry and dimension. The diameter of the smallest opening was 2.5 µm and the biggest 20 µm however, the etching distance between the different hole sizes was the same. In XeF_2 etching the etching rate can be determined either by the size of the holes or by the exposed area of the structure under the via opening. When the opening is small, the etching rate is determined by the size of the opening. However, if the opening is big enough, the etching rate is defined by the total area of the structure. [6] Here, it is demonstrated that the XeF_2 vapour can spread evenly through openings as small as 2.5 µm and etch as fast as structures with via diameter of 20 µm.

In this work, it is shown that the etching rate is also related to the shape of holes and where they are located. This is based on the results presented in Fig. 4.6. This is because the etching uniformity is dependent on how well the XeF_2 gas is spread under the holes. When comparing the shapes, the arc-shaped via openings (top etching) gave the best results. This is because the open area of the arc-shaped via is greater than the circular and square via geometries. The location and shape of the arc holes allowed the gas to spread evenly throughout the structure. The square-shaped holes (side etching) gave similar etching rates as the arc holes, however etching in the middle of the structure was challenging. The circular holes had the slowest lateral etching rate. The circular via openings were efficient only for small structures and for structures in which more than eight via openings were used. An additional observation is that when comparing the two etching rates for the circular via openings (Table 4.5), it can be seen that the wafer with AlN as membrane layer has better release than the wafer with SiO_2. XeF_2 can also react with SiO_2, although the level of attack is very small when compared to Si. [6] [25] If a reaction occurs between XeF_2 and SiO_2, the amount of exposed material on these structures is greater and thus the etching process becomes slower.

A summary containing the vertical etching rate and the lateral etching rate is presented in Table 4.5. The table is divided into two parts: vertical etching rate and lateral etching rate for each via opening geometry and structural layer.

Table 4.5: Vertical and lateral etching rates for XeF_2 etching of a-Si, summary.

Vertical etching rate [nm/min]	*142*	
Lateral etching rate [nm/min]	Structural layer with only SiO_2	Structural layer with only AlN
Circle-shaped via (top etching)	2692	4384
Arc-shaped via (top etching)	7692	6769
Square-shaped via (side etching)	7461	6384

XeF_2 etching was carried out on 8 sample wafers, all of which exhibited similar results. The lateral etching rate was characterized by measuring the etching distance after 15 and 20 minutes of etching. To obtain the etching rate, the data measured after the etching time was used to create a graph and measuring the slope. For better understanding of the results, it

would be ideal to collect more data points as it was done for the vertical etching rate characterisation.

4.2 Structures profile after sacrificial layer release

In this section, the resulting structures after a-Si release by XeF_2 are presented and discussed. First, the results relating to structure A are described. Then, the results from structure B are presented and commented.

4.2.1 Structure A

The final structures were characterized with an optical profilometer. Two methods were used to fabricate structure A. The difference between the two methods was the structural layer material. In one method only SiO_2 was used and in the other, only AlN. Figures 4.7, 4.8 and 4.9 are from sample wafers in which structure A was tested.

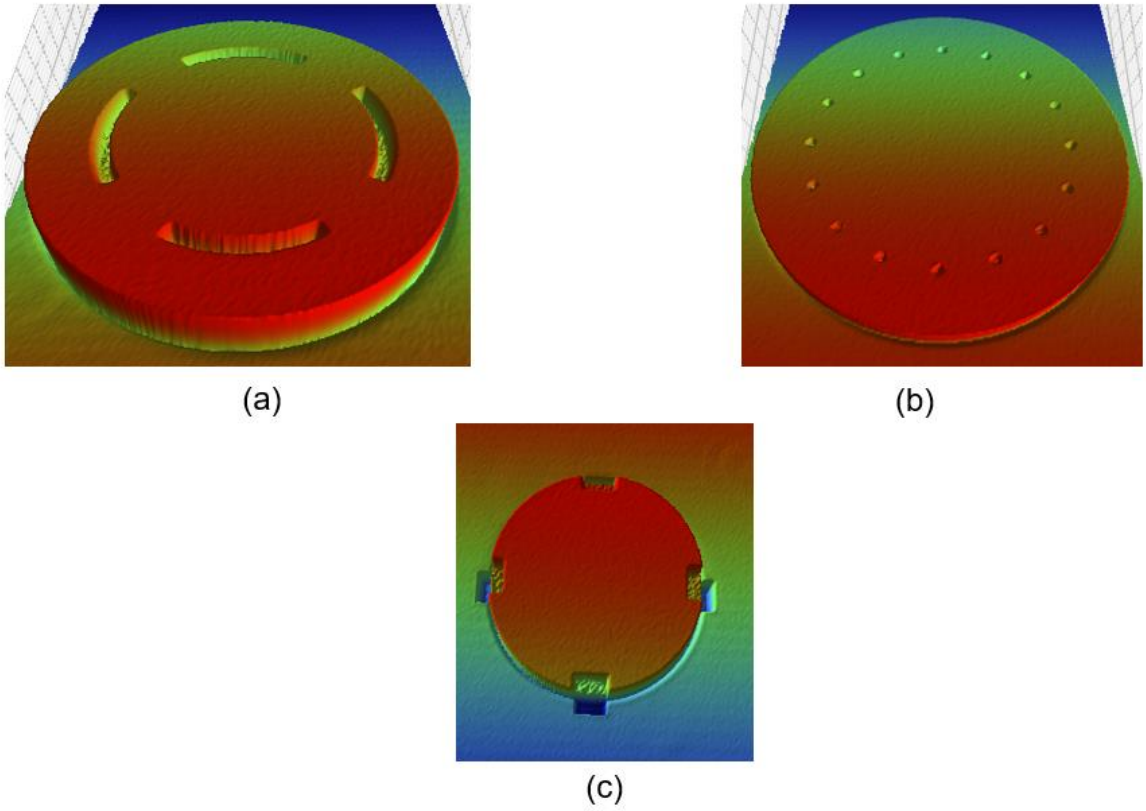

Figure 4.7: Optical profile of structures with AlN as structural layer before XeF_2 release. The structures are based on: (a) 150 µm diameter structure with 4 arc-shaped via openings with 5 µm width, (b) 400 µm diameter

structure with 16 circular-shaped via openings with 10 µm diameter, and (c) 150 µm diameter structure with 4 square-shaped via openings with 15 µm thickness.

The images presented in Fig. 4.7 are from structures before a-Si release. The images in (a) and (b) consist of via openings for top etching and in (c) via openings for side etching. These images will be used to compare the changes on the structures after XeF_2 etching. The released structures are presented in Figures 4.8 and 4.9.

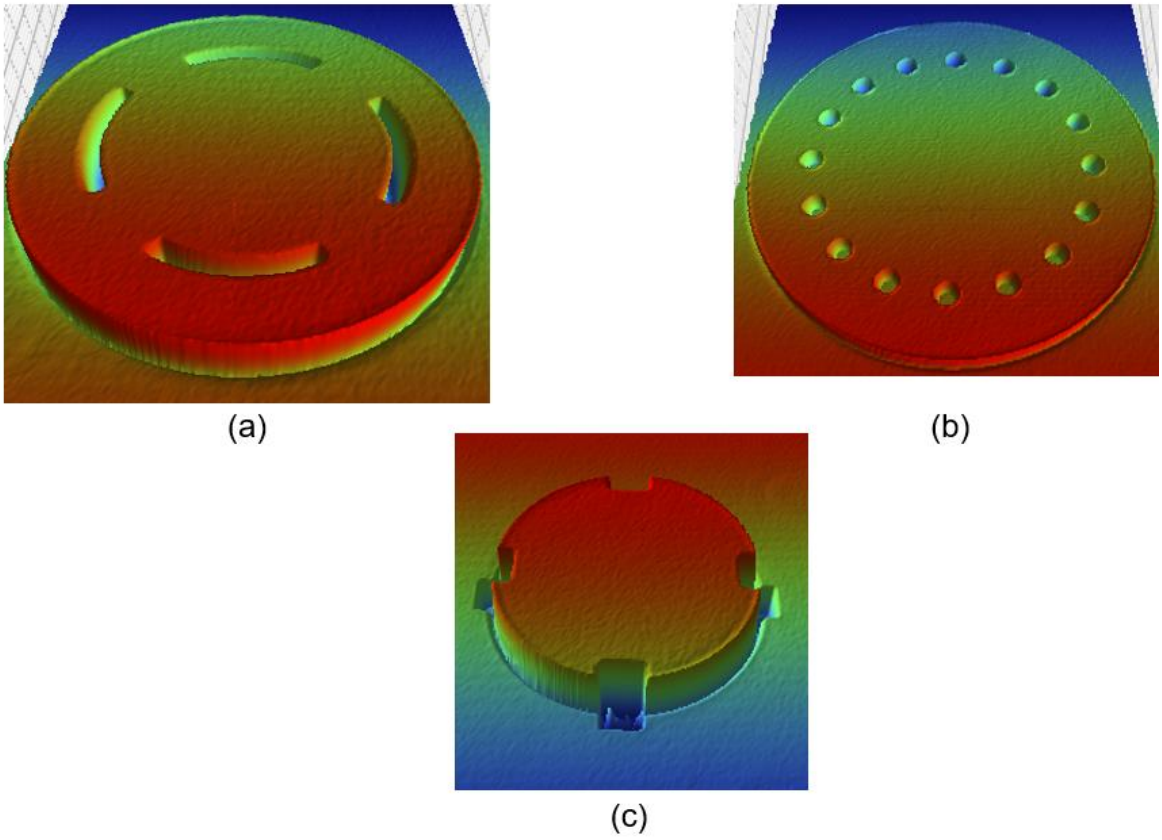

Figure 4.8: Optical profile of structure A design with AlN as the structural layer after XeF_2 release. The structures are based on: (a) 150 µm diameter structure with 4 arc-shaped via openings with 5 µm width, (b) 400 µm diameter structure with 16 circular-shaped via openings with 10 µm diameter, and (c) 150 µm diameter structure with 4 square-shaped via openings with 15 µm thickness.

The images above are from samples in which AlN was used as the structural layer. As can be seen from Fig. 4.8, the structures were intact after a-Si release. All observed structures from 50 to 500 µm, with via openings of different shapes and dimensions, were suspended. By contrast, the structures with SiO_2 as membrane layer collapsed. 20 SiO_2 structures were observed with the optical profilometer after sacrificial layer release. Of these 20, only one

structure with a diameter of 50 µm was suspended. The image below shows an example of a collapsed structure where SiO_2 was used as structural layer material.

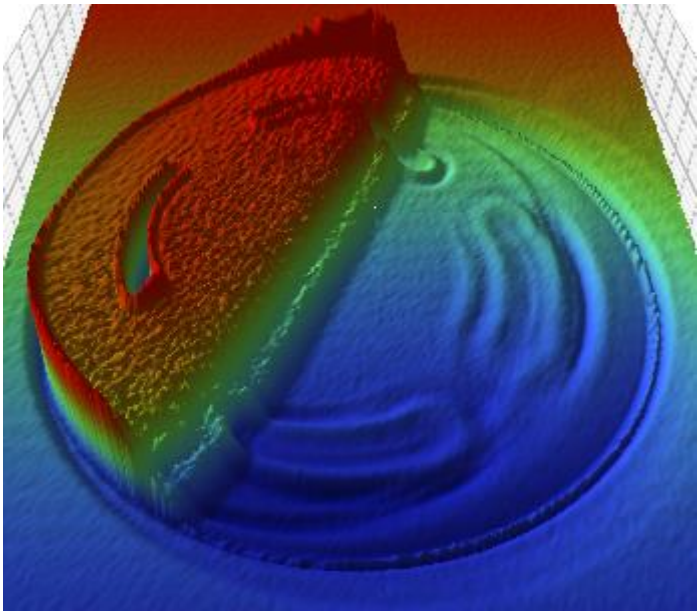

Figure 4.9: Optical profile of structure A with SiO_2 as strucural layer after XeF_2 etching. The structure has a diameter of 150 µm and it consists of 4 arc-shaped via openings with 5 µm thickness.

The results presented in Figures 4.8 and 4.9 were as expected. This is because the tensile stress from the AlN acts in favour of the structure, keeping it stretched and intact. By contrast, SiO_2 films tend to be compressive. [43] Table 4.6 shows the film stress results from the sample wafers after AlN and SiO_2 deposition. The positive values represent tensile stress and the negative values compressive stress.

Table 4.6: AlN and SiO_2 residual stress on sample wafers after deposition.

Wafer ID	*Measured film*	*Stress [MPa]*	*Orientation [°]*
T4x	AlN	25	0
T4y	AlN	21	90
T5x	AlN	29	0
T5y	AlN	31	90
T8x	AlN	11	0
T8y	AlN	12	90
T9x	AlN	22	0
T9y	AlN	17	90
T2x	SiO_2	-183	0
T2y	SiO_2	-185	90
T3x	SiO_2	-182	0
T3y	SiO_2	-183	90

T6x	SiO_2	-178	0
T6y	SiO_2	-181	90
T7x	SiO_2	-182	0
T7y	SiO_2	-181	90

The deposition parameters used in this work were based on a previously developed AlN deposition process. The existing process deposited AlN films with tensile properties. Therefore, the optimization was made with the aim of decreasing the stress values. The experiments were made by keeping the N_2 flow fixed and changing the Ar flow. The final flow ratio between Ar and N_2 was adjusted to 1:2, the obtained results is similar to [50].

The AlN deposition parameters were controlled in order to obtain low tensile stress. In the experimental process, all the parameters were kept constant and the Ar flow was changed. It was observed that by increasing the Ar flow the stress becomes tensile and by decreasing the flow the stress becomes compressive. The stress and other properties of AlN such as optical electrical properties can also be optimized as a function of N_2 concentration, this is demonstrated in [44]- [46].

There are key challenges in the fabrication of microstructures using surface micromachining. The control and minimization of stress and stress gradient in the structural layer is of vital importance. The control is applied in order to avoid bending or buckling of the released microstructure. [43] [36] [47] [48].

Decrease of SiO_2 compressive stress can also be made through annealing. [5] [49] However, this was not tested in the present work.

The stress and structure characterization was performed with several sample wafers and the obtained stress results were all within same range as shown in Table 4.6.

4.2.2 Structure B

The resulting structures from the samples containing structure B design are presented in this section. Two methods were used to fabricate structure B. In one method, only SiO_2 was used as the structural layer. In the other, the structural layer was fabricated with SiO_2 together with AlN. Figure 4.10 shows the structures before a-Si release.

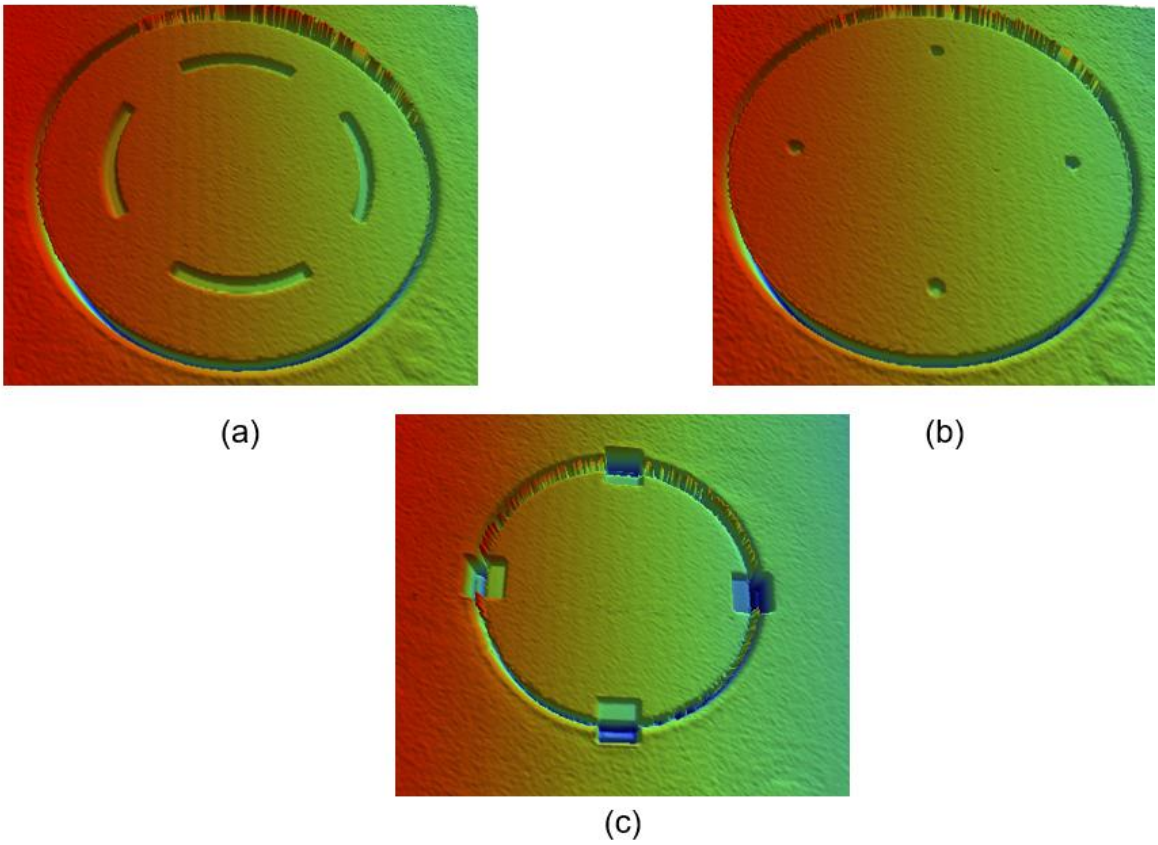

Figure 4.10: Optical profile of test structure B before XeF_2 release. The structures are based on: (a) 4 arc-shaped via openings for top release, (b) 8 circular-shaped via openings for top release, and (c) 4 square-shaped via openings for side release.

The dimensions of the structures in Fig. 4.10 are not specified because the images will only be used as reference for the results obtained after a-Si etching. Based on the images above, it is possible to observe whether any changes occurred after sacrificial layer release. Fig. 4.11 shows the results obtained from the structures utilizing only SiO_2 as structural layer.

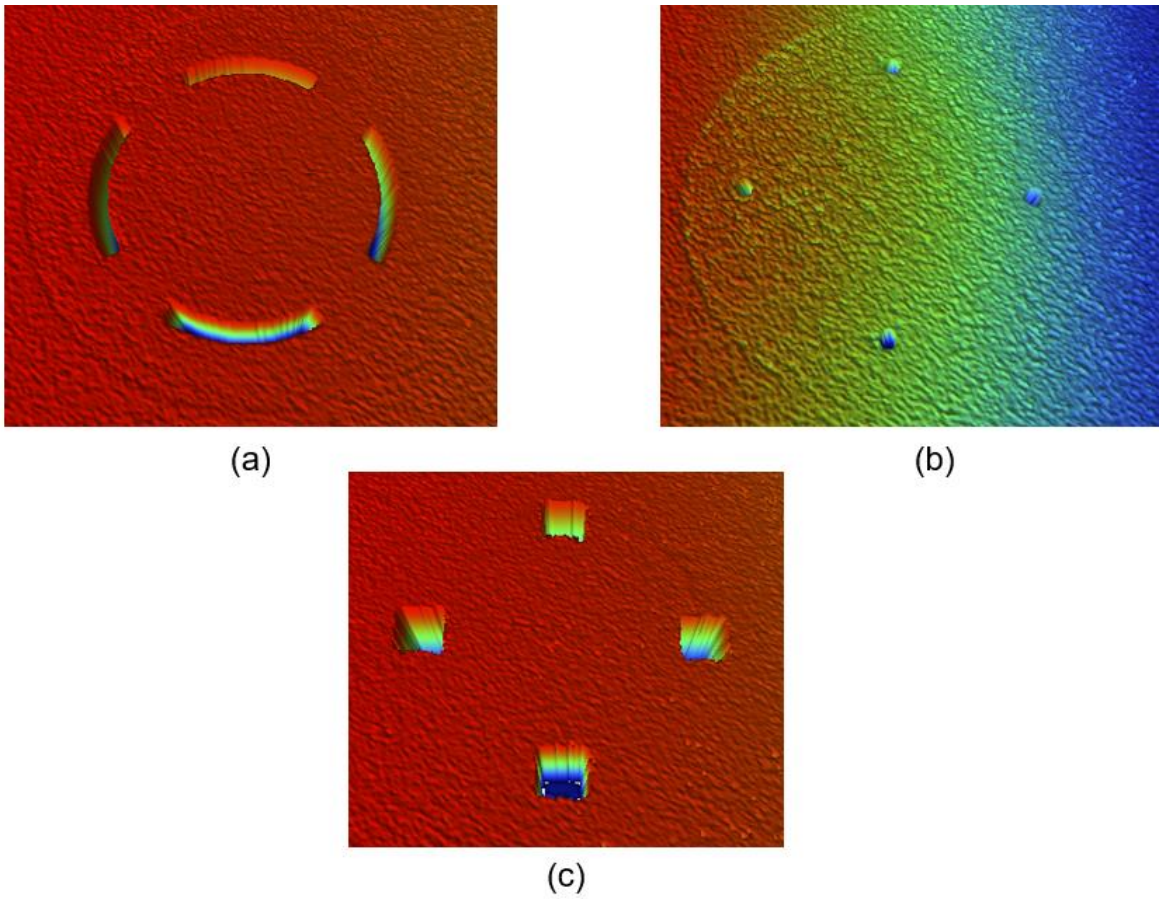

Figure 4.11: Optical profile of structure B with SiO_2 as structural layer after XeF_2 release. The structures are based on: (a) 150 µm diameter structure with 4 arc-shaped via openings with 5 µm arc width, (b) 150 µm diameter structure with 4 circular-shaped via openings with 10 µm diameter, and (c) 100 µm diameter structure with 4 square-shaped via openings with 15 µm thickness.

In total, 12 structures were observed of which 6 did not collapse. As well as in the case of structure A, the SiO_2 film in structure B had a compressive stress, which contributed to the collapsing of the structures. However, structure B design proved to be more resistant than structure A, with half of the observed structures intact after a-Si release.

Figure 4.12 presents the results obtained from the structures utilizing SiO_2 and AlN as structural layers. In total, 16 structures were observed of which 10 did not collapse.

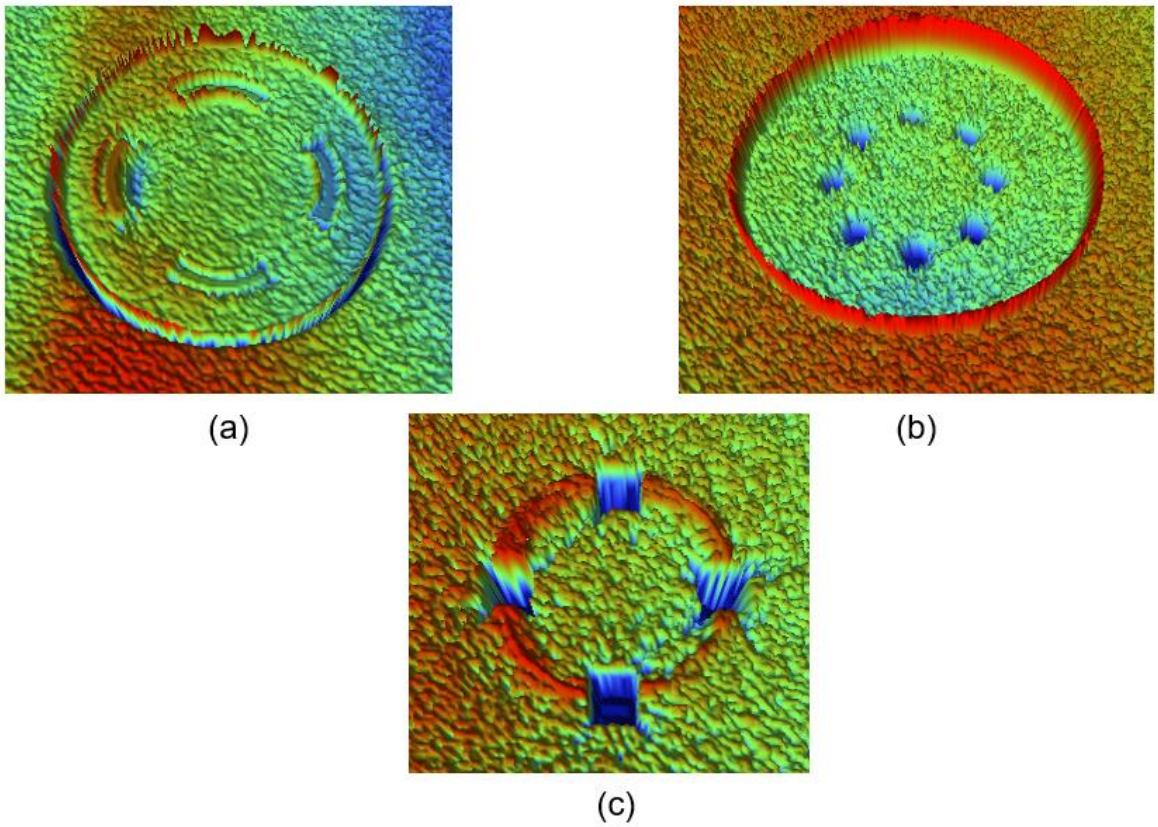

Figure 4.12: Optical profile of structure B with AlN as structural layer after XeF_2 release. The structures are based on: (a) 200 µm diameter structure with 4 arc-shaped via openings with 10 µm width, (b) 300 µm diameter structure with 8 circular-shaped via openings with 20 µm diameter, and (c) 50 µm diameter structure with 4 square-shaped via openings with 10 µm thickness.

It can be observed that the surface profile of the structures presented in Figures. 4.11 and 4.12 are rather rough. The reason for this is that the resist used to pattern the via openings was not removed after etching, making the surface very irregular.

The results obtained from this design are of considerable interest, because the SiO_2/AlN structural layer combination follows the standard PMUT structure.

Fromm all the 16 observed structures, the ones with diameters from 50 to 300 µm were stable and did not collapse. No intact 400 and 500 µm structures were observed.

The membrane layer of this structure combines both SiO_2 and AlN, and as already stated SiO_2 is under compressive stress and AlN under tensile stress. A film under tensile stress will result in a concave shape and a compressively stressed film in a convex shape. [5] When a tensile film is deposited on top of a compressive film, the compressive forces of the film

below balance the tensile forces of the film above. This technique of film stress control is used in microstructure fabrication to engineer novel and more efficient structures. [50]

Because of the high compressive stress values of the SiO_2 film, it is more challenging to obtain intact structures with bigger dimensions. The results in Table 4.6 show that the difference between the stress of SiO_2 and AlN films is very extensive. To obtain mechanical equilibrium between the two films, the net force and bending moment must vanish at the cross section. This is achieved when zero stress is obtained after combining both films. However, if the combination is not prevented from moving, it will bend elastically. Therefore, the combination is still not in mechanical equilibrium, because of the uncompensated end moments. [50] In this case, what can be done is to engineer the stresses on both films in such a way that the stress is balanced enough to keep the structures from collapsing. Studies using similar idea was carried out to investigate PMUTs with self-curved diaphragms. [47]

The a-Si release of structure B design, in which the structural layer material was tested using both SiO_2 and AlN was carried out only on one wafer. Testing of more sample wafers would be beneficial for a clear interpretation of the results.

5 Conclusion

In this thesis, the use of an XeF_2 etching method for the release of a-Si sacrificial layer for different structure designs was demonstrated which could be used for PMUT device fabrication. This work presents two structure designs. The designs were tested using different diaphragm dimensions and via opening of different sizes and geometries. Typically, in a PMUT structure, the structural layer is composed of an insulator material and a piezoelectric material. In the studies carried out, the structural layer materials were tested both separately and together in order to obtain better understanding of the results. The goals of this research comprised creating PMUT structures based on a XeF_2 release method, optimization of etching process parameters, use of developed PECVD a-Si film as sacrificial layer, and AlN stress optimization for suspended device structural layer.

Experimental tests using XeF_2 process for a-Si release demonstrated that 2 µm thick a-Si can be released from SiO_2 and AlN structures of sizes varying from 50 to 500 µm after 20 minutes of etching. Additionally, in this work it was demonstrated that the etching rate of XeF_2 is also influenced by the shape and location of the via openings and not only by film thickness, exposed area and etching parameters. Furthermore, it was verified that when the structural layer of the structure contains SiO_2, the etching release process can be slower. It is believed that even though the attack of XeF_2 to SiO_2 is of low level it is enough to slow down the etching process. However, the etching rate difference between the samples with oxide membrane and the samples with AlN membrane was relatively small. Therefore, it is still possible to obtain fast release of the a-Si layer even for devices using SiO_2 films on the structural layer.

Two structure designs were tested. Two methods were used to fabricate structure A and to fabricate structure B. In structure A, the difference between the two procedures was the structural layer material. In one experiment only SiO_2 was used and in the other only AlN. In structure B, one approach used only SiO_2 and in the other the structural layer was fabricated with SiO_2 together with AlN. All observed structures from 50 to 500 µm, with via opening of different shapes and dimensions were suspended for the structures with only AlN as membrane material. By contrast, most structures with SiO_2 as membrane layer collapsed.

For the structures using both materials, all the structures from 50 to 300 µm were suspended. This result difference is because the residual tensile stress from the AlN film acts in favour of the structure, keeping it stretched and intact. By contrast, SiO_2 films tend to be compressive what makes the film to collapse. The AlN deposition parameters were controlled in order to obtain low tensile stress. Decrease of SiO_2 compressive stress can also be achieved through annealing. However, this was not carried out. Achieving stress reduction on AlN films was of most interest in this work. This is because stress reduction of SiO_2 through annealing is a common practice; therefore, more attention was given to AlN stress optimization. As well as for structure A, most of the observed structure B samples with only SiO_2 as membrane material collapsed. However, structure B design proved to be more resistant than structure A, with half of the observed structures intact after a-Si release. This could be related to how the structural layer is shaped on the structure. In structure A the structural layer is suspended in a sort of hill shape, whereas in B the structural layer is stretched in a flat shape throughout the surface. Therefore, in structure B, the membrane film has more support to keep itself suspended.

The initial plan for this work was to use PECVD a-Si as sacrificial layer. A deposition process was developed and low tensile stress a-Si film was obtained. However, some challenges were encountered during the process and LPCVD was used instead. Because of the difference in temperature between the a-Si and AlN deposition processes, outgassing of the hydrogen on the a-Si film caused bubbles and peeling of the film. Annealing the film at the same temperature as the AlN deposition did not solve the problem. Several bubbles were observed on the film after annealing. Previous studies have demonstrated the possibility of using PECVD a-Si film without outgassing issues after AlN deposition. The next step would be to develop ideas and methods to prevent outgassing of the a-Si film. One way would be to optimize the AlN deposition to obtain a deposition process with lower temperature. A balance between the temperatures of the two deposition processes is essential. Finding a suitable method for the use of PECVD a-Si should not be a difficult process, although time did not permit further investigation of the issue. With further experimentation, the use of a-Si PECVD could work in the process fabrication. Additionally, with PECVD a-Si, optimization of the sacrificial layer stress is possible. This is ideal for the device fabrication since the stress of the sacrificial layer also influences the final structure.

The etching of a-Si into the diaphragm shape was performed by DRIE, which gives a vertical sidewall profile to the diaphragms. The etching method defining the diaphragm profile is important because the shape and thickness of the sacrificial layer define the shape and depth of the device cavity after release. This is crucial because the resulting PMUT performance is dependent on the diaphragm geometry. Two different etching methods were also tested: BHF and plasma etching. As expected, BHF etching had no effect on a-Si. On the other hand, the experiments involving plasma etching did not result in the expected shape. The plasma etching method was used with the aim of obtaining a slope on the sidewalls of the a-Si after etching. The obtained profile was not as estimated, but no further experiments were carried out, because for this work sloped sidewalls was not of main interest. Nevertheless, sloped sidewalls are beneficial to obtain better uniformity of the membrane layer during deposition. With vertical walls, the deposited layer thickness on the top is different from the thickness on the sidewalls. Typically, on the sidewalls less material is deposited than on the top. This can cause problems when the sacrificial layer is released. If the sidewall is much thinner than the top, the structural layer can break and collapse after sacrificial layer release.

The steps following this work include finding a solution for the use of PECVD a-Si in the process fabrication, and an etching method which delivers sloped diaphragm sidewalls. Furthermore, a continuation of the experiments would include testing the membrane layer with annealed SiO_2 films in order to obtain a stress balance between SiO_2 and the AlN structural layer. Subsequently, the fabrication of working PMUT devices can be carried out. Previous researches have demonstrated the release of a-Si by XeF_2 for a PMUT device fabrication. This thesis goes a little further by demonstrating the use of XeF_2 etching for different structure designs and dimensions. Additionally, XeF_2 release of sacrificial layer and the effects of different via opening designs demonstrated in this work could be applied not only for PMUT device fabrication, but also for several different microstructures which use sacrificial layer release.

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