Ultra-low Power ADCs for Space Sensors and Instuments

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***Abstract*—A 28nm 0.1V 10-bit 2kS/s Successive Approximation Register ADC design is proposed. This design opens the doors to both low supply and low power space sensors and instruments. Due to the stringent voltage supply unique challenges arise that are met with innovation in the sample switch and comparator design. These components of the ADC architecture are optimized to perform successfully at a 0.1V supply with a sample rate suitable for most sensor applications.**

I. Introduction

A. Space Sensors and Instruments

As technology improves it becomes more viable to connect devices and understand the world better. As data communication technology improves, an increasing number of devices will become connected to satisfy the demands for data [1]. Many large and costly sensors can now be replaced with smaller, more cost effective sensors that communicate as a network. Each smaller sensor can gather data and collaborate with neighboring devices to complete a dataset of any environment [2]. These sensors are usually created using a microcontroller, an energy source, a transmitter, and sensing electronics that can interface with the environment that surrounds them.

These small sensor networks can be deployed in a variety of conditions. In Earth's atmosphere, an entire network can monitor global weather conditions to update a ground station. On exploration missions, a planet's surface could be monitored in multiple locations to provide a clearer picture of a planet's condition as shown in fig. 1 [5]. Any way they're deployed, they can help paint a better picture of places out of reach.

Small, low power sensors can also be used in other space instruments that require great power efficiency. These types of sensors have already been successfully used to monitor body vital conditions and could easily be incorporated into space suits, rover equipment, or other reconnaissance devices [3,4]. Information on long range missions is crucial, and the instruments that provide this data should be used wherever possible to make the most of costly exploration and surveillance missions.

Each of these applications benefit from a system's ability to use power efficiently while providing needed information. Existing systems need to have their components optimized to preserve power and operate for as long as possible with a given energy source.

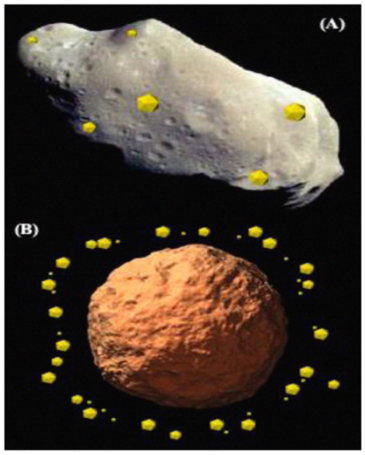

Fig. 1. Two methods of low-power sensor deployment, on surface and in orbit [5].

B. ADCs in Sensors and Instruments

Every sensor that interfaces with the natural world needs to have an Analog-to-Digital converter (ADC) to quantize the element that is being monitored. This device needs to translate an analog element, such as temperature, pressure, or light intensity, into a digital output that represents the original analog quantity. This data can then be transmitted to a receiver to be processed and analyzed.

The energy source for these small sensors is commonly an energy harvester or limited battery [6]. In either case, the power consumption requirements are very strict. Whether the energy source is a battery or a low voltage energy harvester, it is crucial that the ADC's power consumption is as low as possible. The ADC also needs to have a sample rate of around 1-

2kHz to properly function for sensing applications. We propose a 10-bit ADC that can operate at an ultra-low supply voltage of 0.1V with a sample rate that meets the requirements for space sensors and their applications.

II. ADC Design

To meet the needs for low power consumption and high resolution we chose to use the Successive Approximation Register (SAR) ADC. This architecture is simple and very power efficient. It has many variations and we will leverage it's strengths to meet our design requirements. The subsequent section describes its basic operation.

A. Standard SAR Architecture

The SAR ADC is constructed using four main components as shown in fig. 2. First, a switch samples the input and holds its value for evaluation. This sampled value is then compared to a reference voltage using a comparator. Based on the decision of the comparator, the SAR logic block will adjust the reference voltage using a digital-to-analog-converter (DAC) for additional comparisons until the digital output resembles the analog input.

This method of successive approximation is based on the binary search algorithm. An example for a 3-bit SAR ADC is shown in fig. 3, where the analog input voltage (Vin) is compared to an output code. For the first comparison, Vin is compared to a reference voltage (Vref) in the middle of the ADC, which in this case is 0. As seen in the figure, Vin < Vref, so the first bit is set to 0. Now Vref changes to a voltage in the middle of the remaining search range. In the second cycle Vin > Vref, so the second bit is set to 1. The reference voltage is updated once again to the midpoint of the remaining range and the final comparison resolves which sets the third bit to 0. This gives digital output code of 010. The code 010 maps to the analog value of .375V, and thus we see that this code resembles the analog input given.

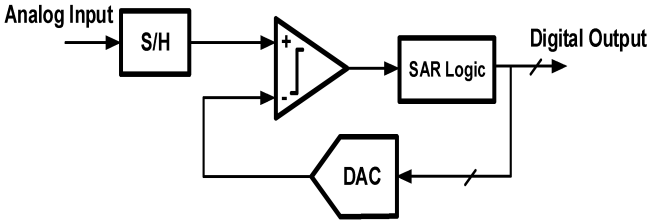

Fig. 2. SAR ADC flow of operation [7].

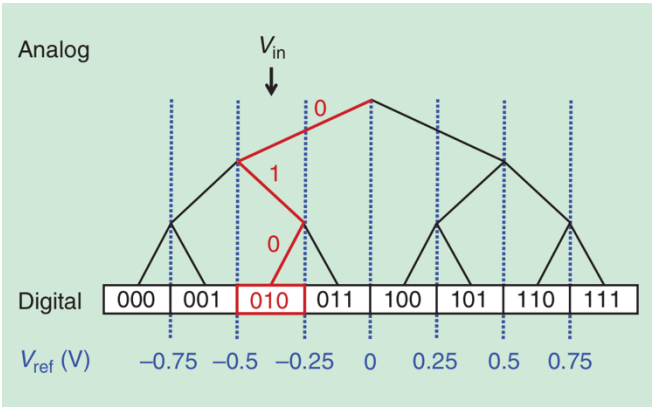

Fig. 3. 3-bit example of a binary search [8].

B. Proposed SAR Architecture

For this ADC, we plan to take advantage of the SAR ADC's high power efficiency. For this reason we chose to design a 10-bit differential SAR ADC. In order to have high resolution without requiring overly large capacitors in the switched-capacitor DAC we felt that 10-bits would be a excellent size. The ADC proposed is differential to improve noise performance at the cost of added complexity and size. The ADC will consist of a quadruple bootstrapped sample switch, a time domain comparator, and suitable digital logic. Like most recent SAR ADCs, this design will be asynchronous, meaning that all internal clock signals are self-generated. The only signal needed is a sample clock input.

C. 0.1V Supply voltage

As stated before, the SAR ADC is simple by design and many have successfully lowered the needed supply voltage below the nominal level of 1.8V [9-13]. However, in the best of these designs, the supply was lowered to 0.3V. To push these designs even further and in order to reduce power consumption and enable operation of low supply devices we intend to reduce the power supply voltage to 0.1V. This requires an unprecedented design that takes full advantage of modern process technologies such as 28nm fabrication.

D. Challenges of Low Power Supply Voltage

Designing an ADC that operates at 0.1V comes with unique problems. At this supply level, transistors conduct very little current. A simple way to illustrate this is to look at inverter delay vs. supply voltage. As seen in fig. 4, the delay increases exponentially with reduced supply. This creates challenges with the digital logic's rise and fall time. It also creates problems in the sample and hold circuit

making it difficult to charge up the switched-capacitor DAC within the allotted sample time. Simply using an existing design with a 0.1V supply is sure to fail.

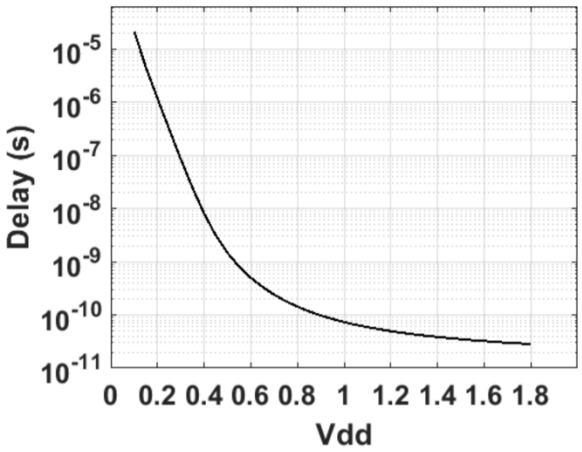

Fig. 4. Inverter delay vs. power supply voltage.

Another important consideration is noise power. With the proposed supply voltage and a 10-bit ADC, the least significant bit (LSB) voltage is given by

$$\frac{Vref}{2^{NoB}} = \Delta$$

For our design, that equates to an LSB of 0.195mV. We need to ensure that our noise voltage doesn't surpass the voltage of our LSB, or else our accuracy will be severely reduced. In the subsequent section we will explain several methods that will mitigate aforementioned problems and allow our ADC to operate accurately at 0.1V.

III. Circuit Design

A. *Quadruple Bootstrapped Switch*

Typically, the sample and hold circuit is implemented using a bootstrapped switch as seen in fig. 5. This helps tackle problems with linearity and transistor conduction by minimizing changes in resistance of the sampling transistor. During the sample phase, transistors are switched on so that the gate voltage remains constant. During the hold phase, the capacitor is recharged to VDD. For most applications this provides enough linearity to track inputs correctly.

For a 10-bit ADC, a conservative target spurious free dynamic range (SFDR) is ~73dB. However, with such low conductance at 0.1V a single bootstrap switch is not enough to meet this target. In fact, after running various simulations and trying new designs the optimal approach was to cascade the bootstrap topology four times. In this layout, four smaller capacitors are charged during the hold phase then linked in series. This not only allowed us to use relatively small internal capacitors for the bootstrap switch, but it also boosted the gate voltage on the sample transistor to ~0.4V. After size optimization of the capacitors and transistors, the target SFDR of 73dB was met as seen in fig. 6.

In order for a quadruple bootstrap switch to function, some parts of the reset circuitry had to be altered. Traditional bootstrap switches use a PMOS to pull the capacitor top plate high to VDD. For our design, this causes a leakage issue across the PMOS since it experiences a relatively large voltage drop across the drain to source. To prevent this, a huge gate voltage would need to be generated to ensure a negative source to gate voltage. To circumvent this issue, NMOS pullup transistors were used alongside a 2VDD charge pump to be able to correctly pullup the top plate voltages. This process eliminates leakage in the pullup transistors while also enabling the 4VDD boost needed for good tracking.

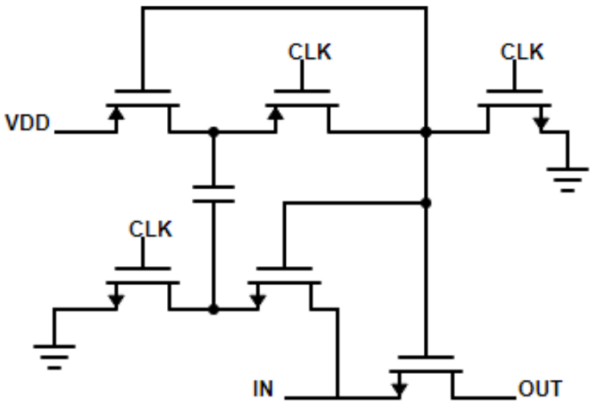

Fig. 5. A single bootstrapped switch.

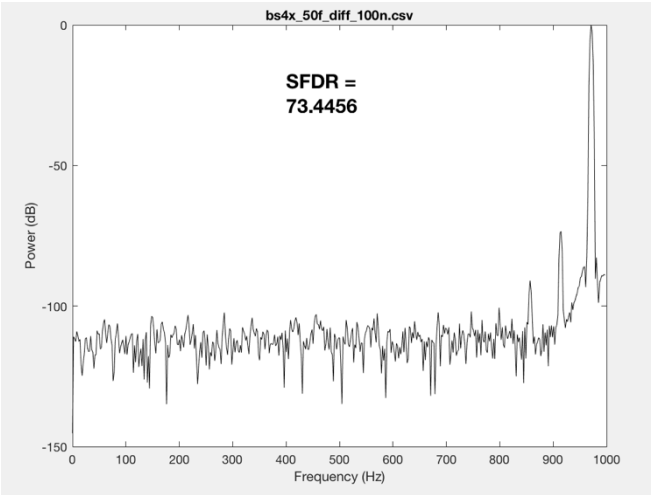

Fig. 6. SFDR of quadruple bootstrap switch at Nyquist rate.

In addition to simply cascading the bootstrap architecture, and resolving pullup leakage several key changes had to be made to prevent leakage current from the pulldown/hold transistors. This is because the design is done in 28nm technology, which is faster than more common technologies like 180nm. However, in 28nm technology the transistors leak small amounts of current from their drain to source. With a larger supply voltage this leakage is negligible but for a 0.1V supply it is significant. To prevent this leakage the NMOS transistors had to be switched to have a negative gate to source voltage as opposed to a gate to source voltage of zero. This circuit is shown in fig. 7, where an intermediate voltage between an NMOS pair is pulled high during the NMOS off state to ensure very little leakage current.

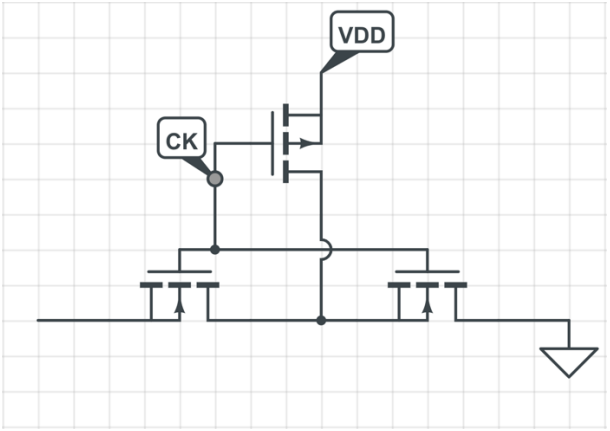

Fig. 7. Leakage lock circuit added to NMOS reset switches.

B. *Time Domain Comparator*

Voltage domain comparators are commonly used in ADCs. In order to meet quantization noise requirements, the transistors in a voltage domain comparator need to be sized according to the noise to LSB relationship given by

$$\sigma^2 \leq \frac{\Delta^2}{12}$$

where sigma squared is the standard of deviation of the input referred noise power probability density function with respect to comparator input voltage difference. With an LSB voltage of 0.195mV transistors in the voltage domain comparator must be sized unreasonably high.

To mitigate this problem, we have designed this ADC with a voltage-to-time converter (VTC) and phase detection logic. By moving the comparison to the time domain, the transistors no longer run into scaling issues that come with lowering the supply voltage.

For the VTC, we wanted to keep the circuit simple and well controlled. In order to have a time domain comparator, the information from the two previous voltage inputs needs to remain. A ring oscillator (fig. 8) oscillates at different frequencies depending on the load capacitance. In order to use this in our design we had to modify the structure of the inverters used in the ring.

To preserve the voltage information, each inverter, as shown in fig. 9, was modified with a stacked PMOS and NMOS pair which allows us to control the amount of current conducted. This in turn, varies the speed at which they oscillate. It also enable us to have a control signal that can halt the oscillation while the comparison is being made.

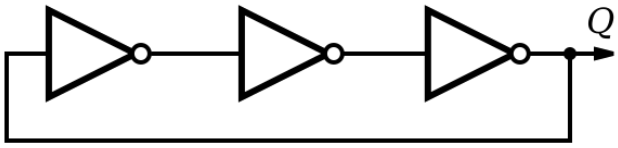

Fig. 8. A 3-stage ring oscillator.

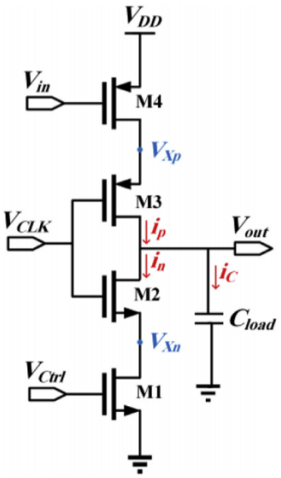

Fig. 9. Current-starved inverter [10].

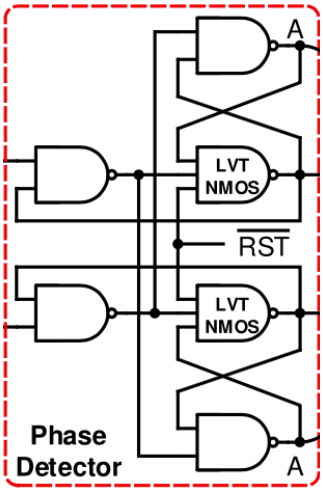

Fig. 10. Phase detection logic [10]

By using the two different voltages to generate separate oscillation frequencies, we can detect which one is faster by using the phase detection logic in fig. 10. This circuit works by checking the outputs of the two ring oscillators until one of them experiences a phase shift of 180 degrees. This then halts the oscillation cycle and provides the output of the faster oscillator.

A big challenge with using a time domain comparator is metastability. A metastability event is encountered when the comparator fails to reach a decision within a given amount of time, i.e., the VCOs are still oscillating. Metastability detection is crucial in a comparator design since it is always updating its own inputs to complete the next comparisons. One way to detect metastability is to use simple binary counters to understand the depth level of metastability. As seen in fig. 11, as Vin decreases oscillation counts also increase. A larger number indicates deeper levels of metastability and all cases where metastability is past a predetermined threshold need to be thrown out and remeasured.

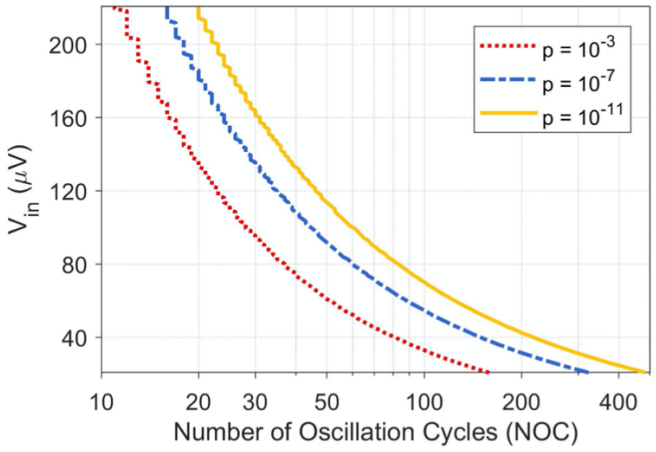

Fig. 11. Oscillation count vs. Vin [10].

IV. Conclusion

In this paper we discussed the design of a 28nm 0.1V 10-bit 2kS/s SAR ADC. By using innovative design choices in the sample and hold circuit, along with the use of a time domain comparator, the system is expected to operate correctly at 0.1V supply. With further design and testing, we feel confident that the ADC will be able to perform with a reasonable sample rate ~1-2kHz.

Our future work consists of implementing more features in the time domain comparator to improve its accuracy, speed, and noise resilience. Specifically, it takes a large amount of cycles before a change of phase is detected if the inputs are very similar. In order to successfully detect a signal, the input needs to be oversampled due to the inherit first order noise shaping of the VTC. We also need to create a calibration method to account for the non-linearity of oscillator behavior. The static properties of the ADC (INL and DNL) need to be measured and evaluation. The signal-to-noise ratio (SNR) needs to be optimized to reach within 3dB of the ideal SNR of 62 dB for a 10-bit ADC. And finally, the chip must go through tape-out and fabrication to be tested and verified. After all of this is completed, we are confident that this ADC will push the limits of technology in space to its next level. We anticipate completing the design and beginning fabrication by Spring 2021.

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