Highly Reliable and Efficient Voltage Optimizer Based on Direct PWM AC-AC Buck Converter

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Abstract—A voltage optimizer (VO) to regulate overrated electricity supply voltages to optimized values with high reliability and efficiency has been developed based on a direct PWM ac-ac buck converter. A comprehensive control strategy is proposed for the ac-ac converter to address existing commutation problems and also to offer a fault handling capability against short circuits. A number of switching states are defined depending on the input voltage, whereby continuous and reliable current paths are maintained at all times especially around voltage zero-crossing points, and safe transitions between them are achieved as well. Based on a detailed power loss analysis, a hybrid scheme with silicon carbide (SiC) MOSFETs and silicon IGBTs is proposed which significantly improves the efficiency while minimizes the cost, and simultaneously enables the use of a high switching frequency, with the potential to reduce the volume of a VO. Results from simulation and experiment confirm that the proposed strategies give reliable operation of the VO with an efficiency higher than 99%.

Index Terms—AC-AC converters, silicon carbide, soft commutation, short circuit protection, voltage optimizer.

I. INTRODUCTION

VOLTAGE amplitude is a crucial index of power quality and its sags and swells are unavoidable in a power system [1]. In addition, in many parts of the world consumers experience a distribution network voltage higher than its nominal value. For example, the single-phase mains in the UK has a voltage range of 230V +10%/–6% but the average is 242 V. The problem of overvoltage is being exacerbated by the spread of distributed generation, resulting in excess losses and premature equipment failures, with consequent financial issues [1], [2].

Power electronics systems can be utilized to tackle overvoltage issues, for example, the dynamic voltage restorer (DVR), the unified power flow controller and the solid state transformer [2], [3]. Nonetheless, these systems are relatively complicated and costly. With the particular target of reducing the overvoltage, more consideration has to be given to the reliability, efficiency, cost and volume of mitigation devices. Therefore, the present work focuses on a new design of a voltage optimizer (VO) to regulate the supply voltage to an optimized value in order for electrical devices to perform tasks more efficiently thereby returning an energy saving. It is a form of voltage management specifically designed for reducing energy consumption. This will bring considerable financial and environmental benefits, as well as preventing accelerated deterioration thus extending the life of equipment. Some VO

devices can be found in the market, but most of them are transformer based and thus are bulky, heavy, costly and have low efficiencies.

A VO can be realized using ac-ac power conversion. Some prevailing ac-ac converters have obvious disadvantages: ac choppers using thyristors have the drawback of poor power quality, matrix converters are complex in structure and control, and indirect ac-dc-ac converters are costly and bulky due to the multiple stages of power conversion [4], [5]. In contrast, direct pulse-width-modulation (PWM) ac-ac converters have the merit of a simple structure, easy control, small size, high efficiency, low cost and high power quality. These advantages make them attractive in applications where only voltage regulation is required [6], exactly the objective of the VO.

Direct ac-ac converters can be derived from the corresponding dc-dc converters, for example the buck, boost, buck-boost, and Cuk types [7], [8]. In particular, as a typical type to reduce the voltage level, the ac-ac buck converter has been widely researched [9]. Numerous converters and applications based on the buck type have been discussed in the literature, for example, multilevel ac-ac converters for high power DVRs [10], and converter topologies to obtain arbitrary amplitude, phase, and even frequency [11].

However, direct ac-ac converters have particular commutation problems related to dead times, giving rise to current and voltage transients that are harmful to power devices [12]. Several strategies have been reported to overcome the commutation problems. Adding resistor-capacitor snubbers is a possible method of allowing finite dead times but snubbers are bulky and degrade the efficiency and power quality [13]. Soft commutation methods based on the polarity of voltages have been proposed in [9], [14]-[17] to provide alternative current paths during dead times, but they all have a severe problem of unreliable operation around voltage zero-crossing points. More recently efforts have been made to reconfigure the switching legs to relieve the commutation issues [13], [18], [19]. Nonetheless, additional inductors and capacitors are necessary which increase the converter's volume, decrease efficiency and even bring stability problems [19]. In addition, in the particular solutions the input and output do not have a common neutral connection which however is a vital consideration in non-isolated single-phase line conditioners [20].

Furthermore, none of the previous work has thoroughly investigated the power loss in direct ac-ac converters, which is very important for applications where the aim is to save energy. Wide band gap semiconductors, especially silicon carbide (SiC) devices, are gaining wider adoption in power electronics

applications due to efficiency improvements [4], [21]. Nevertheless, using SiC devices could increase the overall cost due to their higher price, especially considering the large number of transistors required for ac-ac converters.

Another a critical issue is performance under abnormal conditions, especially short circuits [22], [23]. The poor overcurrent capability of semiconductors, with a typical tolerance of two to three times the nominal current for a few tens of microseconds, renders the converters susceptible to catastrophic destruction [24]. Despite this, to the knowledge of the authors, fault protection of direct ac-ac converters has not previously been investigated. Importantly VOs will have to work, without failure, with traditional ac circuit devices namely circuit breakers (CB) and/or fuses which have high fault current tolerance and response times of tens or even hundreds of milliseconds [24].

In the present work, a VO based on the ac-ac buck converter has been developed. A comprehensive control strategy with a range of switching states is proposed which overcomes the commutation issues and supports fault current handling. Unlike other work [13], [18], [19], the problem of commutation around voltage zero-crossing points is resolved without any extra circuitry. Fault currents through the power devices can be safely eliminated via dedicated switching states. Smooth transitions between different switching states are also achieved to keep continuous current paths. Furthermore, an in-depth power loss study has been carried out and from which a converter topology with hybrid SiC MOSFETs and silicon (Si) IGBTs has been conceived which significantly improves the efficiency and additionally minimizes the cost.

A detailed theoretical analysis and both simulated and experimental results validate the effectiveness of the proposed control strategy and circuit topology. The control strategy for the ac-ac buck converter has been briefly introduced in [25]. Substantive new materials, including the application of VO, systematic analysis, power loss study, new hybrid SiC & Si topology, and results, etc., are presented in this paper.
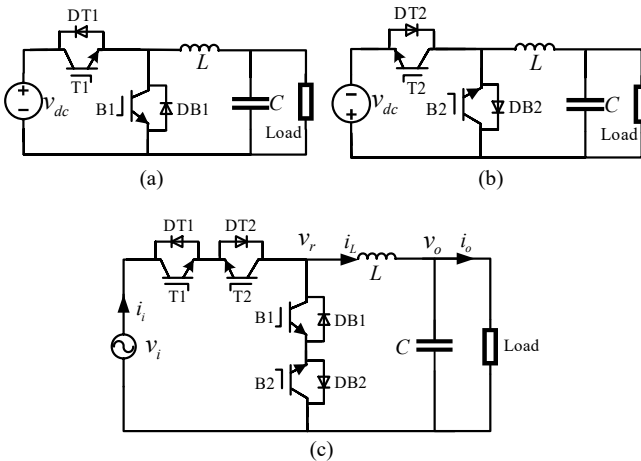

Fig. 1. Buck converters with different input voltage. (a) Positive dc voltage. (b) Negative dc voltage. (c) AC voltage.

II. PWM Switching Control of AC-AC Buck Converter

A. PWM Switching Control

A dc-dc buck converter is shown in Fig. 1(a), and its counterpart for negative dc voltage is shown in Fig. 1(b) (in this case using IGBTs). A single-phase ac-ac buck converter can be obtained by combining the two dc structures, as shown in Fig. 1(c). Consideration of these structures facilitates the analysis of soft commutation methods for ac-ac converters.
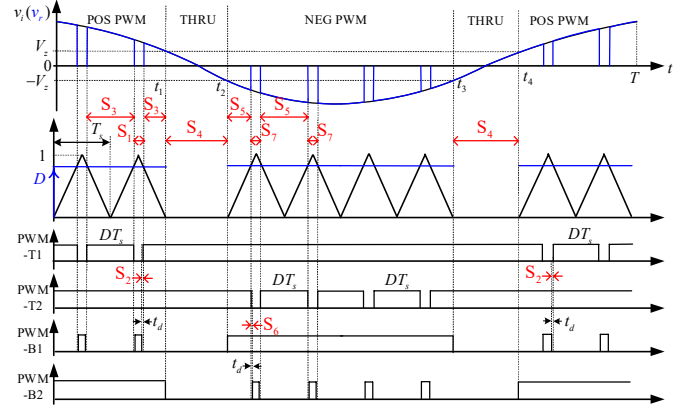
Fig. 2. PWM switching control of ac-ac buck converter.
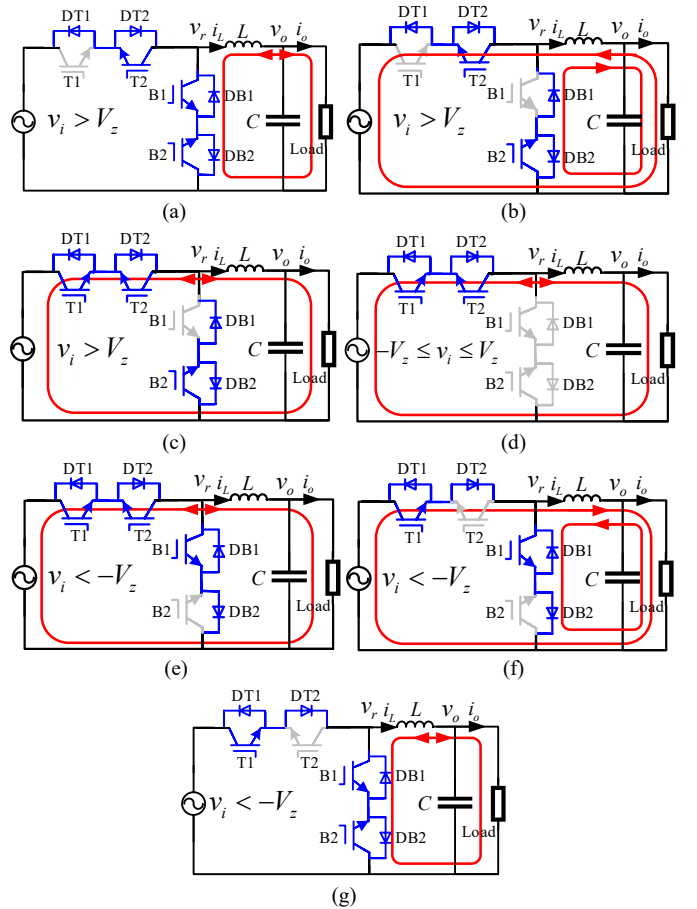
Fig. 3. Operation states and power flow in different switching states. (a)-(c) S_{1-3} in POS PWM. (d) S_4 of THRU. (e)-(g) S_{5-7} in NEG PWM.

Ideally, the top (T1, T2) and bottom legs (B1, B2) are switched complementarily and instantaneously. However, in practice, there are unavoidable dead and/or overlap times due to non-instantaneous switching of the power transistors and also delays in the gate driver circuits. During dead times, the inductor current is interrupted which can generate high voltage spikes as there is no automatic free-wheeling path, while during

overlap times the power source is shorted giving rise to high current spikes. The voltage and current spikes during commutation are likely to damage the devices [13].

The proposed PWM control method is illustrated in Fig. 2. A large switching period T_s is used for illustration purposes. There are three switching states depending on the input voltage v_i. Corresponding operation states and power flows are shown in Fig. 3. It should be noted that the sensing of the input and output voltages is generally essential for voltage regulation, hence it will not incur a cost for additional sensors.

When v_i is positive and above a value of V_z, T2 and B2 are fully turned on, and T1 and B1 are complementarily modulated with regulated duty ratios and proper dead times (t_d), i.e., to be equivalent to the positive dc voltage circuit in Fig. 1(a). This switching state is termed as POS PWM. There are three operation states: S_1 (T1 off and B1 on) where the power flows through the bottom leg, S_2 (T1 and B1 off) of dead time in which continuous current paths still exist through anti-parallel diodes and fully on switches, and S_3 (T1 on and B1 off) in which the power flows via the top leg. On the other hand, when v_i is negative and below $-V_z$, T1 and B1 are fully turned on, and T2 and B2 are complementarily modulated, named as NEG PWM, equivalent to Fig. 1(b). The operation states S_{5-7} and corresponding power flows are illustrated in Fig. 3(e)-(g). These are similar to the soft commutation methods in [14]-[17] where actually POS PWM is for $v_i > 0$ and NEG PWM for $v_i < 0$.

In the proposed control method an additional state called THRU is defined: when v_i is in the zero-crossing range $[-V_z, V_z]$, T1 and T2 are fully turned on while B1 and B2 are turned off (operation state S_4), making the power flow through the top leg. With an appropriate choice of V_z the zero-crossing commutation problems in [14]-[17] can be overcome, i.e., shoot-through issues when the voltage polarity detection around zero-crossing points is inaccurate [10], [12], [13], [18], [19]. Moreover, the high frequency harmonic content in the output voltage will be reduced because the voltage over the zero-crossing range is not chopped, and the power loss can be minimized because there are always two switches that are fully turned on and there is no switching loss in the THRU state.

It should be noted that the duty ratio needs to be updated at the beginning of each switching period (see Fig. 2), such that smooth transitions between different switching states are achieved. For example, before entering the THRU state from NEG PWM, T1 and T2 have already been turned on (S_5) and hence only B1 needs to be switched off (S_4), ensuring a safe current path through the top leg.

B. Analysis of Regulated Waveforms

In order to analyze the chopped waveform v_r (voltage across the bottom leg), the switching is assumed to be ideal and without dead time. The input voltage is defined as

$$v_i(t) = V_i \cos \omega t = V_i \cos \frac{2\pi}{T} t , \tag{1}$$

where V_i, ω, and T are the amplitude, angular frequency, and period, respectively.

For the soft commutation methods in [14]-[17] without the zero-crossing THRU state, the chopped voltage (expressed as v_{r0} in this case) can be derived as (3) by multiplying (1) with the Fourier series of the square wave control signal (2), with D and

ω_s being the duty ratio for the top leg and switching angular frequency, respectively [15]. For the VO, assuming a maximum input grid voltage of 230V +20%, i.e., $V_i = 276\sqrt{2}$ V, and the optimized output $V_o = 220\sqrt{2}$ V, the minimum value of D (= V_o/V_i) is around 0.8.

$$S(t) = D + \sum_{k=1}^{\infty} \frac{2 \sin kD\pi}{k\pi} \cos k\omega_s t \tag{2}$$

$$v_{r0}(t) = DV_i \cos \omega t + \sum_{k=1}^{\infty} \frac{V_i \sin kD\pi}{k\pi} \cos(k\omega_s \pm \omega)t \tag{3}$$

For the proposed method, the zero-crossing range of the input voltage (see Fig. 2, t_1-t_2 and t_3-t_4 of v_i) is denoted as:

$$v_{iz}(t) = \begin{cases} V_i \cos \omega t, t \in [kT + t_1, kT + t_2] \cup [kT + t_3, kT + t_4] \\ 0, t \notin (kT + t_1, kT + t_2) \cap (kT + t_3, kT + t_4), k = 0,1.. \end{cases} \tag{4}$$

The Fourier series of (4) can be derived as

$$v_{iz}(t) = \underbrace{\left(\frac{\sin 2\omega t_2}{\pi} + \frac{2t_2 - 2t_1}{T} \right)}_{A} V_i \cos \omega t +$$
$$\sum_{k=3,5,7...} \frac{2V_i}{\pi} \underbrace{\left[\frac{\sin(k+1)\omega t_2}{k+1} + \frac{\sin(k-1)\omega t_2}{k-1} \right]}_{B} \cos k\omega t, \tag{5}$$

and t_1 and t_2 are given as:

$$t_1 = \frac{1}{\omega} \arccos \frac{V_z}{V_i}, t_2 = \frac{1}{\omega} \left(\pi - \arccos \frac{V_z}{V_i} \right). \tag{6}$$

Therefore, v_r in the proposed control method can be obtained by adding (3) with an additional un-chopped part within $[-V_z, V_z]$, given as:

$$v_r(t) = v_{r0}(t) + [1 - S(t)] v_{iz}(t)$$
$$= [D + (1-D)A] V_i \cos \omega t + (1-A) \sum_{k=1}^{\infty} \frac{V_i \sin kD\pi}{k\pi} \cos(k\omega_s \pm \omega)t \tag{7}$$
$$+ (1-D) \sum_{k=3,5,7...} B \cos k\omega t - \sum_{k=1}^{\infty} \frac{2 \sin kD\pi}{k\pi} \cos k\omega_s t \sum_{k=3,5,7...} B \cos k\omega t.$$

For the maximum input voltage case with $D = 0.8$ and assuming $V_z = 30$ V, we have $A = 0.0002$ and $|B| < 1.3$. In comparison to (3), in (7) the fundamental component amplitude is slightly increased and the high order harmonics at $k\omega_s \pm \omega$ are reduced. Additional harmonics at low odd orders are also generated but their amplitudes are rather small. Furthermore, potential spikes over the zero-crossing ranges are avoided by the THRU state. As a result, the quality of the output voltage is higher than that of the soft commutation methods without the THRU state.

III. Power Loss Study and Improvement

In this section, a detailed study is carried out on the power loss of the ac-ac buck converter with the proposed PWM control method. Subsequently, a topology with hybrid SiC MOSFETs and Si IGBTs is proposed that substantially reduces the power loss while minimizes the cost.

A. Power Loss Analysis

The currents conducting through paths T1-DT2, T2-DT1, B2-DB1 and B1-DB2 are denoted as i_{TP}, i_{TN}, i_{BP} and i_{BN}, and the forward voltage drops in them (series transistor and diode) are expressed as u_{TP}, u_{TN}, u_{BP} and u_{BN}, respectively. T1 and T2 are assumed to be identical devices, as well as B1 and B2.

In the THRU state only the conduction loss in the top leg needs to be counted. The average conduction loss in one ac period is given as:

$$P_{THRU} = \frac{1}{T}\left(\int_{t_1}^{t_2} u_T i_T + \int_{t_3}^{t_4} u_T i_T\right) \approx \frac{2}{T}\int_{t_1}^{t_2} |u_T i_o|, \tag{8}$$

where u_T is either u_{TP} or u_{TN} and i_T is i_{TP} or i_{TN} depending on the actual current path.

In the NEG PWM state, i.e., $v_i < -V_z$ with T1 and B1 being fully on and T2 and B2 switched complementarily, the direction of the inductor current i_L is set by the load type. When i_L is negative, the current path in the converter is T2-DT1 (i_{TN}) or B1-DB2 (i_{BN}); when it is positive, the path is T1-DT2 (i_{TP}) or B2-DB1 (i_{BP}). The switching waveforms of the two scenarios, for simplicity approximated as piecewise-linear, are shown in Fig. 4. The power loss essentially comprises conduction and switching losses.
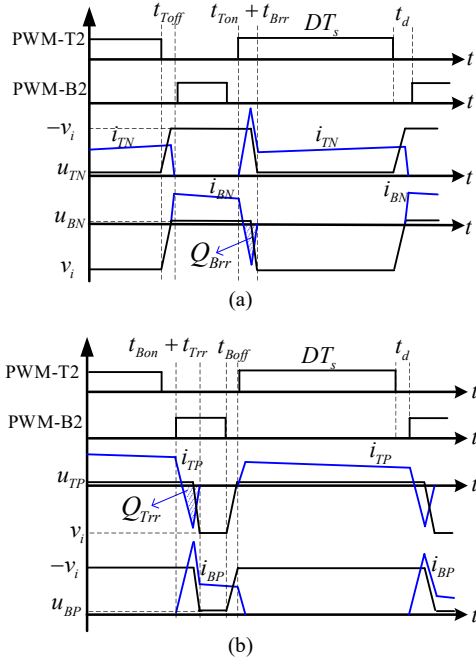

(a)

(b)

Fig. 4. Simplified switching waveforms in NEG PWM state. (a) Negative current. (b) Positive current.

When i_L is negative as in Fig. 4(a), the conduction energy loss in the k-th switching period during the interval t_2-t_3 is (t_d is ignored):

$$W_{Ncon}(k) = \int_{kT_s}^{(k+D)T_s} u_{TN} i_{TN} + \int_{(k+D)T_s}^{(k+1)T_s} u_{BN} i_{BN}. \tag{9}$$

The average conduction loss can be approximated as:

$$P_{Ncon} = \frac{1}{T}\sum_{t_2 \sim t_3}\left(\int_{kT_s}^{(k+D)T_s} u_{TN} i_{TN} + \int_{(k+D)T_s}^{(k+1)T_s} u_{BN} i_{BN}\right)$$

$$\approx \frac{1}{T}\sum_{t_2 \sim t_3}\left[|u_{TN}(k) i_o(k)|DT_s + |u_{BN}(k) i_o(k)|(1-D)T_s\right] \tag{10}$$

$$\approx \frac{1}{T}\int_{t_2}^{t_3}\left|\left[u_{TN}D + u_{BN}(1-D)\right]i_o\right| = \frac{1}{T}\int_{t_2}^{t_3}|u_N i_o|,$$

where u_N is the equivalent forward voltage drop.

The switching loss consists of turn-on and turn-off losses. The turn-off energy loss, which only occurs in the top leg, in the k-th switching period can be approximated as:

$$W_{Noff}(k) = \frac{1}{2}\left|v_i(k)\left(i_o(k) + \frac{i_r(k)}{2}\right)\right| t_{Toff}, \tag{11}$$

where t_{Toff} is the turn-off time of T2, and $i_r(k)$ is the current ripple given as

$$i_r(k) = \frac{|v_o(k)|(1-D)T_s}{L}. \tag{12}$$

The turn-on loss in a switching period, which also includes the reverse recovery loss associated with DB2 and the effect of the output capacitance of T2, can be approximated as:

$$W_{Non}(k) = |v_i(k)|\left(\frac{t_{Ton} + 2t_{Brr}}{2}\left|i_o(k) - \frac{i_r(k)}{2}\right| + Q_{Brr}\right) + \frac{1}{2}C_{oes}v_i^2(k) \tag{13}$$

where t_{Ton} is the turn-on time of T2, C_{oes} is its output capacitance and t_{Brr} and Q_{Brr} are the reverse recovery time and charge of DB2, respectively.

When i_L is positive, i.e., the load is not resistive, as shown in Fig. 4(b), the energy loss can be similarly derived. In this case, significant switching loss is induced in the bottom leg, especially reflecting the reverse recovery process of DT2. However, the power factor of the load in the VO applications is usually near unity, and in any case, the THRU state covers the region adjacent to the zero-crossing points of both the voltage and current. Hence, with a sufficiently large V_z the positive current in NEG PWM can be avoided.

For ease of calculation, assuming v_i and i_o are constant and $i_r = 0$ in a switching period, the total energy loss in the k-th period due to switching can be estimated as

$$W_{Nsw}(k) = W_{Noff}(k) + W_{Non}(k)$$

$$= \frac{1}{2}|v_i(k)i_o(k)|(t_{Toff} + t_{Ton} + 2t_{Brr}) \tag{14}$$

$$+ |v_i(k)|Q_{Brr} + \frac{1}{2}C_{oes}v_i^2(k).$$

The following average switching loss in an ac period due to NEG PWM state can then be obtained:

$$P_{Nsw} = \frac{1}{TT_s}\sum_{t_2 \sim t_3} T_s W_{Nsw}(k)$$

$$= \frac{1}{TT_s}\int_{t_2}^{t_3}\left[\frac{1}{2}|v_i i_o|(t_{Toff} + t_{Ton} + 2t_{Brr}) + |v_i|Q_{Brr} + \frac{1}{2}C_{oes}v_i^2\right]. \tag{15}$$

Because of the symmetry between positive and negative voltage ranges, the power loss in the POS PWM and NEG PWM states is the same. Therefore, the total power loss in the semiconductors can be written as:

$$P_{loss} = P_{THRU} + 2P_{Ncon} + 2P_{Nsw}$$

$$= \frac{2}{T}\int_{t_1}^{t_2}|u_T i_o| + \frac{2}{T}\int_{t_2}^{t_3}|u_N i_o| + \tag{16}$$

$$\frac{1}{TT_s}\int_{t_2}^{t_3}\left[|v_i i_o|(t_{Toff} + t_{Ton} + 2t_{Brr}) + 2|v_i|Q_{Brr} + C_{oes}v_i^2\right].$$

B. Efficiency Optimization

From the previous analysis and considering $D > 0.8$, it can be concluded that most of the total power loss arises from the top leg, while the conduction loss in the bottom leg is small and its switching loss can be neglected. Therefore, the power loss can be reduced with optimal design for the top leg. Hence SiC MOSFETs are used instead of Si transistors. As the forward

voltage of the body diode of SiC MOSFET is relatively high, fast recovery diodes (FRDs) are connected in parallel with the SiC MOSFETs. Si IGBTs are used in the bottom leg, which minimizes cost and can carry high fault currents as will be clarified in the following sections. The hybrid converter topology with SiC MOSFETs and Si IGBTs is shown in Fig. 5.
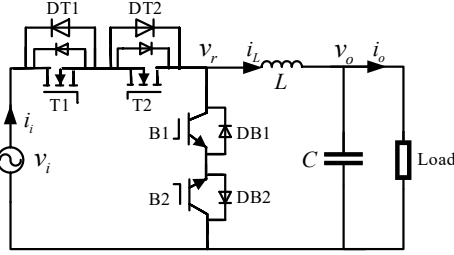

Fig. 5. Optimized ac-ac buck converter with hybrid SiC MOSFETs and Si IGBTs.

TABLE I. CIRCUIT AND CONTROL PARAMETERS

| Symbol	Variable	Value
V_i	Input voltage amplitude	342 V
ω	AC angular frequency	$2\pi \cdot 50$ rad/s
V_o	Optimized output voltage amplitude	311 V
V_z	Zero-crossing range	30 V
f_s	Switching frequency	18-60 kHz
S	Power rating	3 kW
L	Filter inductance	214 μH
C	Filter capacitance	20 μF
I_t	Fault threshold current	70 A
IGBT	FGH40T65SQD (£1.99)	650V/40A
SiC	SCT3060AL (£11.45)	650V/39A
FRD	FFH50US60S (£2.56)	600V/50A
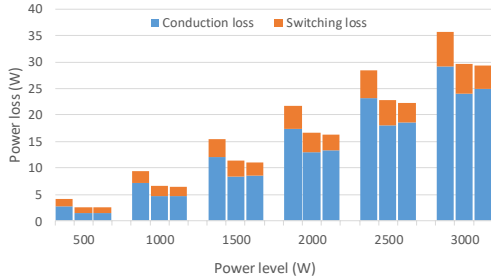
Fig. 6. Theoretical power loss comparison among Si (left), hybrid (middle), and SiC (right) structures.

As previously noted, the power loss due to the reverse recovery of DT1 (POS PWM) or DT2 (NEG PWM) and the switching loss in the bottom leg can be avoided if the THRU state accommodates the potential opposite polarities of v_i and i_L. Assuming the load power factor is λ, the following condition for V_z needs to be fulfilled:

$$V_z \geq \left| V_i \sin\left(a\cos\lambda\right) \right| = V_i \sqrt{1-\lambda^2} . \tag{17}$$

Circuit and control parameters are given in Table I with $D \approx 0.91$. To verify the power loss analysis and the improvement introduced by the hybrid scheme, an additional topology with SiC MOSFETs in both legs is also considered. For a fair comparison among the three options (Si, hybrid SiC & Si, SiC), FRDs are used in all top legs. Based on (8) - (16) and datasheets, power losses at a switching frequency of 18 kHz and different power levels (output power) are given in Fig. 6. With SiC devices, the total power loss is significantly reduced. In comparison to the hybrid topology, the switching loss of the SiC topology is slightly smaller due to the faster reverse recovery of the diodes in the bottom leg, but the conduction loss is larger because of their higher forward voltage.

Another issue is the cost of semiconductors. Using catalogue prices for the devices listed in Table III, the costs are: Si structure £13.08 (4 IGBTs + 2 FRDs), hybrid structure £32 (2 IGBTs + 2 SiCs + 2 FRDs), and SiC structure £50.92 (4 SiCs + 2 FRDs). It can be concluded that for the VO the hybrid topology is the best balance between efficiency and cost. Furthermore, the optimized efficiency allows the use of a high switching frequency, with the potential to reduce system volume using smaller inductors.

IV. FAULT HANDLING SWITCHING CONTROL

Because of the limited thermal-electrical capacity and thus poor overcurrent capability of semiconductor devices, power converters should be equipped with protection against over-currents, especially under short circuit faults [24]. In contrast to other converters such as dc-dc and dc-ac converters in which the switches can be turned off when a fault current occurs [22], direct ac-ac converters cannot be simply shut down otherwise there is no free-wheeling diode path so inductor currents would be interrupted thereby causing voltage spikes.

The faults studied in this paper are assumed to be at the load side. Several switching states are proposed in addition to the normal PWM ones to accomplish a fault handling capability. The fault handling states are activated when the load current exceeds a threshold value I_t.

If the fault occurs in the POS PWM state, T1 and B1 will remain on and the other two be off; this state is called POS RECT. If the fault is in NEG PWM, the handling state will be NEG RECT with T2 and B2 being on and the other two off. In this way, safe transitions between the states are realized and there will always be a path for inductor current. For example, for the NEG PWM, only T2 or B2 need be turned off to get to NEG RECT, and safe current paths still exist: when $i_L > 0$ it will be taken by T1-DT2, when $i_L < 0$ it will conduct through B1-DB2. In any case, the fault current will decay. (POS/NEG PWM → POS/NEG RECT)

It is more troublesome when the input voltage is in the zero-crossing range $[-V_z, V_z]$, because of the possible inaccuracy in the voltage sensing and a resultant uncertainty in sensing polarity. Therefore, in this range the bottom leg should be switched on while the top leg be off, termed as OD state. There are two scenarios regarding the transition to the OD state.

If the fault current appears in the POS or NEG PWM state and has already been dealt with by the POS or NEG RECT state but has not yet decayed to zero. To transfer to the OD state, whichever of B1 or B2 is off in the RECT states should be immediately turned on (POS or NEG OD), and after a short time T2 or T1 should be turned off. In this way, the fault current is diverted to the bottom leg. (POS/NEG RECT → POS/NEG OD → OD)

If, however, the fault is triggered in the zero-crossing range in which the PWM switching is in THRU state, ideally, if the input voltage is positive, B2 should be switched on (POS THRU), then T1 off (POS RECT). Subsequently B1 is on (POS OD) and finally T2 turns off (OD). Similarly, if the polarity is negative the OD state can be reached through a series states

(NEG THRU, NEG RECT, NEG OD) to sustain current continuity. However, these procedures take a relatively long time, and as mentioned above the polarity sensing could be inaccurate and hence the sequences would be invalid. Nonetheless, if V_z is sufficiently small, when the legs are in a shoot-through condition the leg current would be limited by the internal impedance of lines and devices. Therefore, a more effective transition is to turn all switches on (STR) for a short time and afterwards to switch the top leg off (THRU → STR → OD).

If the fault current has not died away in the OD state while the input voltage changes to be above V_z or below $-V_z$, the state needs be transferred to POS or NEG RECT. For the former, T2 should be turned on (POS OD) before B1 is turned off, and for the latter T1 needs be turned on (NEG OD) and then B2 be off. (OD → POS/NEG OD → POS/NEG RECT)

In all cases, all switches can be turned off (OFF state) once the inductor current has been safely eliminated. A summary of the switching states defined in this work is given in Table II.

In addition, VO units must support fault currents so that traditional CBs and/or fuses operate correctly. This is realized through relays working in bypass mode after all switches have been safely turned off. More details regarding the working modes will be given in the following section.

TABLE II.   SWITCHING STATES

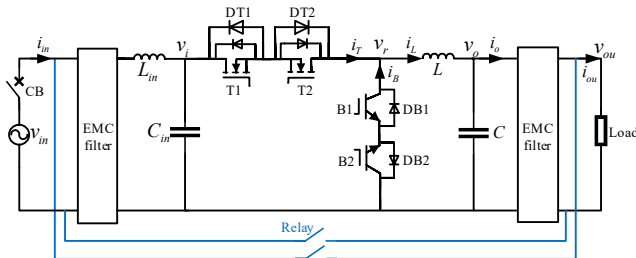| State	ON	OFF
POS PWM	T2, B2, T1/B1	B1/T1
NEG PWM	T1, B1, T2/B2	B2/T2
THRU	T1, T2	B1, B2
POS THRU	T1, T2, B2	B1
NEG THRU	T1, T2, B1	B2
POS RECT	T2, B2	T1, B1
NEG RECT	T1, B1	T2, B2
OD	B1, B2	T1, T2
POS OD	T2, B1, B2	T1
NEG OD	T1, B1, B2	T2
STR	T1, T2, B1, B2	-
OFF	-	T1, T2, B1, B2

Fig. 7.   Circuit diagram of the VO based on ac-ac buck converter.
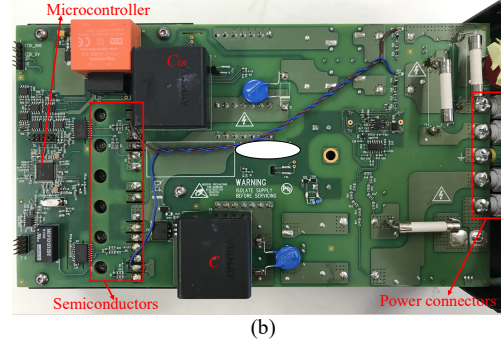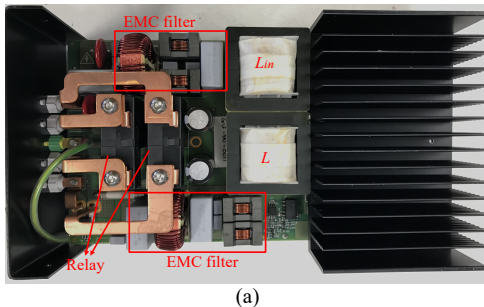

(a)

(b)

Fig. 8.   Hardware system of the VO, top (a) and bottom (b) layers.

V.   RESULTS

A VO, with the specifications given in Table I, has been fabricated. The circuit diagram with hybrid SiC & Si scheme is shown in Fig. 7 where EMC filters are used and an LC filter is also applied in the input side. The hardware system is shown in Fig. 8. Two relays are used to connect the input directly to the output to give a bypass mode. Initially the VO starts working in the bypass mode with the relays being closed and the ac-ac buck converter in OFF state. In normal conditions the relays are opened and the buck converter works, putting it in VO mode (PWM switching control). A protection scheme has been designed for the VO so that in abnormal situations like overcurrent resulting from an electrical load exceeding the unit's rating for a certain duration or when the grid input voltage is lower than the optimized value or in voltage sag conditions, the VO goes to bypass mode. The switching states during the transition between the two modes are also important to keep load current continuity, because the relays need a reaction time to close or open (about 15 ms). This is achieved through a transition stage with switching states POS THRU ($v_i > V_z$), NEG THRU ($v_i < -V_z$) or THRU ($-V_z \leq v_i \leq V_z$). It can be easily proved that safe transitions are also fulfilled. In particular, when the fault handling reacts (in VO mode only) and all switches are safely turned off, the relays will be closed to ensure that CBs and/or fuses operate correctly, and after the fault has been cleared the VO can be restarted. Simulations and experiments have been carried out to validate the proposed control strategies and efficiency study.

Simulations have been performed in Matlab/Simulink. A closed-loop proportional integral control has been implemented to optimize the output load voltage v_{ou} ($\approx v_o$). Fig. 9 shows the waveforms when there is a step change in load from 2 to 3 kW, revealing a good control performance with smooth results.
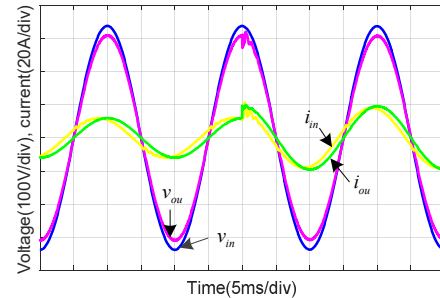

Fig. 9.   Voltage optimization in simulation with a step change in load.

All the VO variants, namely the Si, hybrid SiC & Si, and SiC units (all components are identical except for the semiconductors and their gate drivers) have been tested experimentally. Fig. 10(a) and (b) respectively show the PWM gate signals (the gate voltage of T1 & T2 SiC is 0 or 20 V, B1 & B2 IGBT is –9 or 15 V) and switch voltages (v_{sT}: voltage across the top leg, v_{sB}: voltage across the bottom leg) around a voltage zero-crossing point of the hybrid scheme at f_s = 30 kHz. Note that the two figures could not be practically synchronized because of the time delays in voltage sampling and PWM updating. These results further illustrate the PWM switching control of Fig. 2 and the operation diagrams in Fig. 3. As seen, the input voltage is not chopped in the THRU state, which successfully tackles the commutation problem due to potential voltage sensing errors.
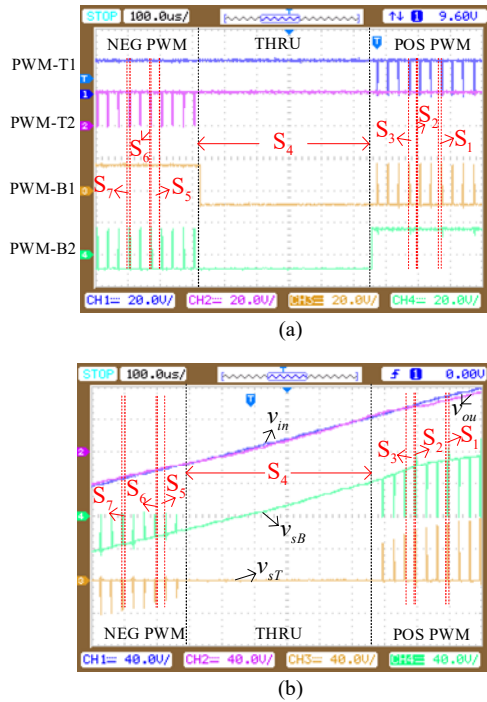

(a)

(b)

Fig. 10. PWM swiching waveforms around a voltage zero-crossing point of the hybrid unit at f_s = 30 kHz. (a) Gate signals. (b) Voltage signals.

Steady state operation at 3 kW of the Si unit with conventional soft commutation control (without the THRU state) is shown in Fig 11 (a) (f_s = 18 kHz), with substantial current ripples due to the voltage sensing issues. Under these conditions, the semiconductor devices failed frequently especially during prolonged testing. In contrast, with the new PWM control method, Fig. 11 (b) is a transient response matching the simulation in Fig. 9. As seen, the currents are smooth with much higher quality, and the VO is able to work reliably. Mild transient oscillations appear at the output voltage, with approximately a maximum amplitude of 10 V (4.55% of nominal value) and a settling time of 2 ms. The good dynamic response minimizes any sags or swells in the output voltage with consequent load disturbance. Overall, the output voltage is controlled at an optimum level from a higher input voltage. The quality of the output voltage is also improved with the proposed new control method, as clearly shown in Fig. 12 of the total harmonic distortion (THD) at different power levels (output power).

(a)

(b)

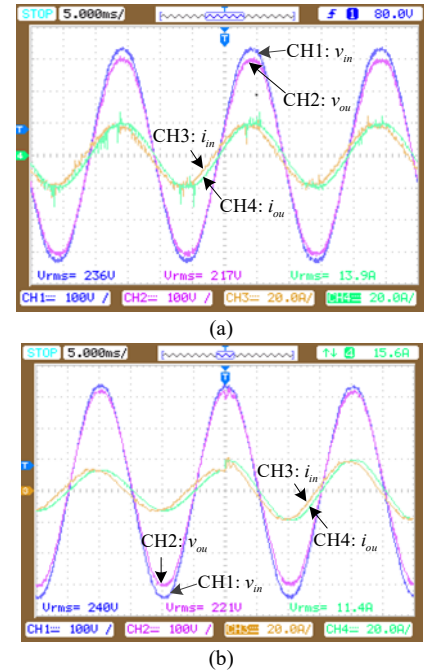Fig. 11. Voltage optimization in experiment. (a) Steady-state with coventional control method. (b) Transient response with the proposed control method.

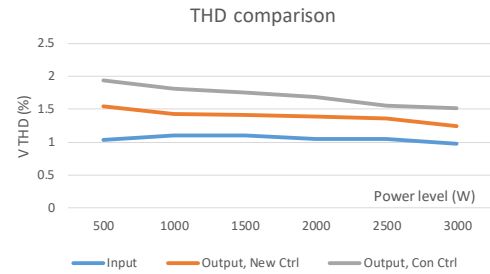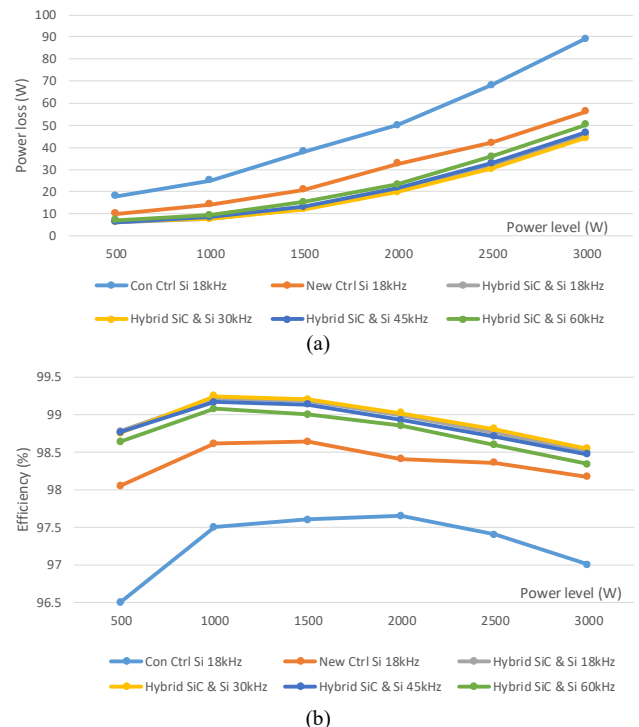Fig. 12. THD of input and output voltages with coventional and proposed PWM control methods.

(a)

(b)

Fig. 13. Total power loss (a) and efficiency (b) of Si and hybrid topologies with different control methods, power levels, and swiching frequiencies.

Total power losses (including inductor and line losses etc.) and efficiencies have also been measured by power analyzer. Results of the Si and hybrid units are shown in Fig. 13. As clearly illustrated by results from the Si topology (f_s = 18 kHz), the proposed control method reduces the power loss by almost one third that of the conventional control method, increasing the efficiency by more than one percent. Hence, the new control method was applied to the hybrid scheme. The hybrid SiC further improves the efficiency by approximately 0.5 percent, reaching 99.22% between 1 and 1.5 kW. Overall it is higher than 98.5%, a saving of 45 W at the rated power. The highest efficiency is obtained at f_s = 30 kHz, reaching 99.25% at 1 kW, a reasonable compromise between switching and inductor losses. When the switching frequency is further increased (45 and 60 kHz), the efficiency slightly decreases but is still higher than that of the Si topology at f_s =18 kHz.

The results of the SiC topology are quite similar to the proposed hybrid scheme so were not presented in Fig. 13. An example of the total power losses of the hybrid and SiC units at f_s = 30 kHz and different power levels is given in Table III. As can be seen, the power loss of the SiC topology is slightly smaller than that of the hybrid topology but the cost is much higher, in agreement with the study in Section III-B. In addition, the two VO versions with resistive-inductive (RL, L_{load} = 8 mH) loads have been tested. The power losses are also listed in Table III. As indicated, the inductor incurs additional power loss which is small at low power levels but is noticeable above 1500 W (load power factor λ < 0.997). This results from the power loss caused by the reverse recovery of FRDs in the top leg and the switching loss in the bottom leg, which cannot be accommodated by the THRU state when λ < 0.9961 as proved by (17). As a result, the SiC unit has advantage due to the SiC MOSFETs in the bottom leg. To improve the performance with reactive loads, a larger V_z can be used or SiC Schottky diodes could be employed in both legs but at higher cost.

It is difficult to provide a breakdown of the total power loss, but the power loss difference among different cases mainly originates from the switching and conduction losses of the power semiconductors which have been thoroughly analyzed in Section III. The measured results validate the theoretical power loss study and confirm the predicted efficiency improvement introduced by the hybrid scheme.

TABLE III.   POWER LOSSES OF HYBRID AND SIC VOS

Power level (W)	500	1000	1500	2000	2500	3000
Hybrid R (W)	6.37	7.6	12.1	19.8	30.4	44.2
SiC R (W)	6.2	7.5	11.8	19.4	29.9	43.8
Hybrid RL (W)	6.4	7.9	12.7	21.5	33.1	48.0
SiC RL (W)	6.1	7.6	12.2	20.3	31.4	45.9

The most extreme form of short circuit test is a direct short at the VO's output terminals when the current will only be limited by the supply impedance. For the actual short circuit test, the load side was shorted using a contactor with a total resistance of 0.08 Ω, and the impedance of the supply line is measured at about 0.12 Ω. Therefore, the theoretical peak short circuit current is approximately 1.6 kA based on a 230 V supply. Such a high current will definitely damage the devices. However, it should be noted that there are inductors in the circuit that limit the rate of rise of the fault current. More

importantly, the converter is designed with fault handling switching control with fast response, enabling it to cope with the short circuit current. Selected experimental results of the hybrid scheme with f_s = 18 kHz are provided to prove the fault handling capability of the proposed control strategy.

(a)

(b)

(c)

(d)
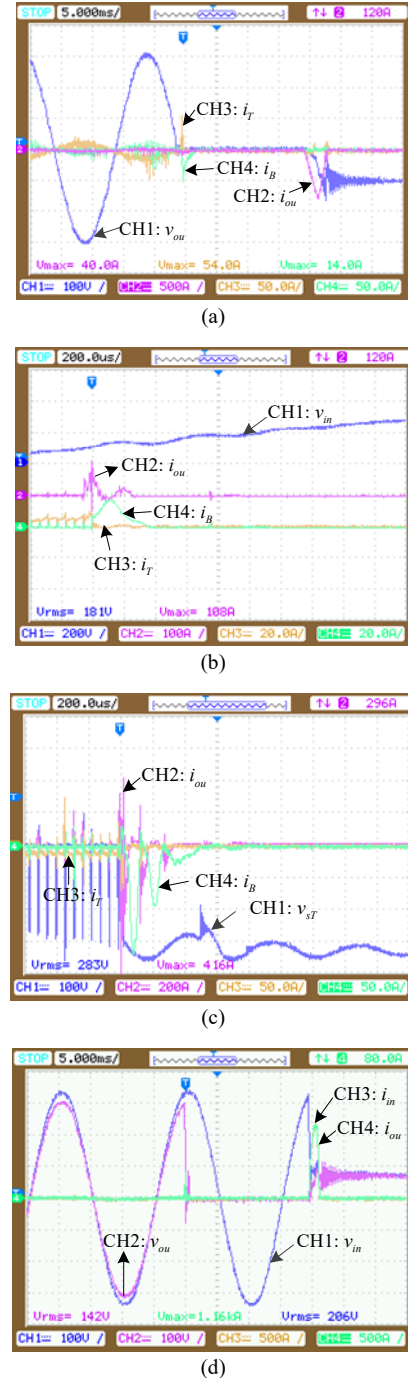
Fig. 14. Experimental short circuit tests. (a) Fault in voltage zero-crossing range. (b) Fault at low voltage. (c) Fault at high negative voltage (CH1: switch voltage v_{sT} across the top leg). (d) Fault at high positive voltage (peak tripping current 1.16 kA).

When the fault is triggered in the voltage zero-crossing range, the result shown in Fig. 14(a) indicates that the current by the shoot-through STR state is safely within the maximum overcurrent capability of the transistors (160 A for the IGBT,

500 A for the FRD, and 97A for the SiC MOSFET). The current can decay because the switching state goes to OD eventually. After all switches are turned off, the relays are closed (closing time about 15 ms) and the CB is tripped (the peak tripping current in this case is about –800 A).

When the fault occurs at a low input voltage point, the result is shown in Fig. 14(b) (bypass mode disabled). As can be observed, there is a delay time of about 10 μs for the control to respond to the fault current, mainly arising from sampling and analog-to-digital conversion. Nevertheless, the current rise in the top leg during this delay is limited by the inductors. Once the fault handling is activated, the current is taken over by the bottom leg and finally dies away because of the POS RECT state.

When the fault appears at high voltages, the currents through the legs would be high, see Fig. 14(c) (bypass mode disabled) and (d) (bypass mode enabled). As revealed, the fault currents in the output filter inductor are diverted to the bottom leg via NEG or POS RECT states. This is also a reason why IGBTs with relatively higher pulsed collector current rating are used in the bottom leg. The fault currents are finally reduced to zero within hundreds of microseconds and all switches are then turned off (the relays will then be closed to trip the CB if the bypass mode is enabled). Moreover, the corresponding gate signals and switch voltages like that of the top leg in Fig. 14(c) can be easily verified and derived.

All the simulated and experimental results confirm that the proposed control strategy manages to address the commutation issues and to provide the VO with fault handling capability to prevent damage from short circuits. High efficiency is also achieved from the proposed hybrid SiC & Si topology.

Furthermore, the VOs have passed all relevant tests including short circuit performance and have been certified at the Power Networks Demonstration Centre (PNDC, a research and demonstration facility in the UK) and the British Standards Institution (BSI).

VI. CONCLUSION

A highly reliable and efficient VO to address overvoltage issues has been developed based on a direct PWM ac-ac buck converter. The pivotal issue in the control of the VO is to maintain continuous and safe current paths. A comprehensive control method has been proposed for the ac-ac buck converter, with the ability to increase reliability, reduce power loss, and enhance power quality. Numerous switching states have been defined, without the need of extra circuitry, to resolve the commutation problems especially around voltage zero-crossing points and to provide short circuit protection. Based on a detailed power loss analysis, a converter topology with hybrid SiC MOSFETs and Si IGBTs has been proposed that achieves efficiency higher than 99%, enabling a substantial increase in energy savings through the use of VOs. Matched simulation and experiment results have validated the studies. The strategies can be applied to other ac-ac buck converter based applications and also be extended to other type of direct ac-ac converters to improve their performance especially in terms of reliability and efficiency.

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