HIGH DYNAMIC RANGE LOW NOISE AMPLIFIER AND WIDEBAND HYBRID PHASE SHIFTER FOR SiGe BiCMOS PHASED ARRAY T/R MODULES

by

CAN ÇALIŞKAN

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APPROVED BY

Prof. Dr. Yaşar GÜRBÜZ .....
(Thesis Supervisor)

Assoc. Prof Dr. Meriç ÖZCAN .....

Assoc. Prof. Dr. Erkay SAVAŞ .....

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High Dynamic Range Low Noise Amplifier and Wideband Hybrid Phase Shifter for SiGe BiCMOS Phased Array T/R Modules

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Abstract

Transmit/Receive Module (T/R Module) is one of the most essential blocks for Phased Array Radio Detection and Ranging (RADAR) system; due to being very influential on system level performance. To achieve high performance specifications, T/R Module structures are constructed with using III-V devices, which has some significant disadvantages; they are costly, and also consume too much area and power. As a result, application area of T/R Module is mainly restricted with the military and dedicated applications. In recent years, SiGe BiCMOS technology has started to be an emerging competitor to III-V devices, with the help of bandgap engineering. SiGe BiCMOS based T/R Module structures are facilitating similar or better performance parameters with a much lower cost, which gives a chance to T/R Module not only used for military purposes, but also for commercial applications. For this reason, this thesis has focused on SiGe BiCMOS based X-Band T/R Module, specifically on its two significant blocks; Low Noise Amplifier (LNA), and Phase Shifter.

Low Noise Amplifier is the first block of the receiver chain of the T/R Module; as a result its performance is very influential on the metrics of receiver, such as Noise Figure (NF), and gain. In this thesis, designing procedures for three different high dynamic range LNA structures are described, using 0.13µm SiGe IHP-Microelectronics and 0.13µm SiGe IBM technology. To achieve a high dynamic range, three different methodologies implemented and compared; single-stage cascode LNA, telescopic LNA, and two-stage cascode LNA. Among these, two-stage cascode LNA achieved better performance metrics of -3.72dBm level for input-compression point, total gain exceeding 20.5dB, a NF performance of about 2dB, and a power consumption of 115.8mW.

Phase Shifter is used both in receiver and transmitting chain, as a result it is also crucial for the performance of the T/R Module. The design, implemented in 0.13µm SiGe IBM technology, had aimed to combine advantages of different topologies, such as passive phase shifter and vector modulator, to achieve a high phase resolution in wide bandwidth, and high linearity. The designed hybrid Phase Shifter achieves 6-Bit operation with 6.75GHz of bandwidth and 15dBm of input-P1dB. Moreover, design can be switched to 7-Bit phase shifter with 4.5GHz, without requiring any additional circuitry.

Faz Dizili SiGe BiCMOS Alıcı/Verici Modülleri için Geniş Dinamik Aralıklı Düşük Gürültülü Kuvvetlendirici ve Geniş Bantlı Karma Faz Kaydırıcı

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Özet

Faz dizili Radyo Algılama ve Menzil Tayini (RADAR) sistemlerinin genel performansı üzerinde etkili olduğu için Alıcı/Verici (T/R) Modülleri, sistemin en önemli yapı taşlarından biridir. T/R Modüllerden yüksek performans beklentisi nedeniyle bu modüllerin gerçeklenmesinde yüksek güç tüketimi, geniş alan gereksimi ve yüksek maliyeti gibi birçok kusuruna rağmen, III-V yarıiletken bileşenleri kullanılmaktadır. Dolayısıyla, T/R Modülleri'nin kullanım alanı askeri uygulamalar gibi özel amaçlı alanlar ile sınırlanmıştır. Son yıllardaki gelişmeler ile SiGe BiCMOS teknolojisi, III-V teknolojisi uygulamaları için ciddi bir alternatif oluşturmaktadır. SiGe BiCMOS teknolojisi ile benzer performans diğer teknolojilere göre daha düşük maliyetle gerçeklenebiliyor olması günlük hayatta T/R modüllerinin kullanım alanlarını da genişletmiştir. Bahsedilen gelişmeler ışığında bu tez SiGe BiCMOS teknolojisi temelli X-Band T/R modüllerinin iki önemli bloğu ola Düşük Gürültülü Kuvvetlendirici (LNA) ve Faz Kaydırıcı 'nın yüksek performansla gerçeklenmesine odaklanmıştır.

Düşük Gürültülü Kuvvetlendirici T/R Modül'ün alıcı zincirine ait ilk yapıdır. Bu sebeple Gürültü Figürü (NF) ve Kazanç gibi bazı genel alıcı zinciri kriterleri üstünde direk etkisi bulunmaktadır. Bu tez çalışması kapsamında, yüksek dinamiği hedefleyen üç farklı LNA yapısı IHP Microelectronics'in ve IBM'in 0.13µm SiGe teknolojileri kullanılarak tasarlanmıştır. Tek katlı kaskod LNA, teleskopic LNA, ve iki katlı kaskod LNA yüksek kazanç ve doğrusallığı hedefleyerek tasarlanmış ve tez kapsamında performansları kıyaslanmıştır. Tercih edilen bu üç yapı arasından, iki katlı kaskod LNA daha iyi performans ölçütleri verebilmekte; -3.72dBm'lik giriş referanslı doygunluk noktasına, 20.5dB kazanç ve yaklaşık 2dB'lik NF'le ulaşırken, 115.8mW güç harcamıştır.

Faz Kaydırıcı hem alıcı hem de verici zinciri tarafından kullanlan bir yapı olduğu için, performansı T/R Modül'ün kriterleri için büyük önem taşımaktadır. Tasarımı için pasif faz kaydırıcı, vektör kipleyici (vector modulator) gibi birçok farklı yapının olumlu yanlarını öne çıkarmak amacıyla karma bir devre yapısı kullanılmıştr. IBM'e ait 0.13µm SiGe BiCMOS teknolojisinin kullanıldığı karma faz kaydırıcıda, geniş bant aralığında yüksek faz çözünürlüğü ve yüksek doğrusallık hedeflenmiştir. Tasarlanan karma faz kaydırıcı 6.75GHz'lik frekans aralığında 6-Bit'lik işlem kapasitesine ait iken, 15dBm'lik giriş referanslı doygunluk noktası, ve yaklaşık 11.25dB'lik kayba sahiptir. Bunun yanında, istenildiği taktirde dışarıdan herhangi bir devre elemanına gereksinim duymadan 7-Bit'lik işlem yapabilme özelliğine geçiş yapabilmektedir. 7-Bit için çalışma frekans aralığı 4.5GHz'tir.

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List of Abbreviations

ANT	Antenna
APAR	Active Phased Array RADAR
ADC	Analog-to-Digital Converter
AAW	Anti-Air force Warfare
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BP-LP	ByPass-Low Pass
BJT	Bipolar Junction Transistor
CB	Common-Base
CE	Common-Emitter
DAC	Digital-to-Analog Converter
DTI	Deep Trench Isolation
DPDT	Double-Pole-Double-Throw
EIRP	Equivalent Isotropic Radiated Power
FOM	Figure-of-Merit
Ge	Germanium
HBT	Heterojunction Bipolar Transistor
HFET	Heterojunction Field Effect Transistor
HB	High Breakdown-voltage
HEMT	High Electron Mobility Transistor
HP	High Performance
HP-LP	High Pass-Low Pass
IF	Intermediate Frequency
I/Q	Inphase/Quadrature
iNMOS	Isolated NMOS
LNA	Low Noise Amplifier
LP	Low Pass
LSB	Least Significant Bit
MESFET	Metal Semiconductor Field Effect Transistor
MEMS	MicroElectroMechanical System
MIM	Metal-Insulator-Metal
MSB	Most Significant Bit
NMOS	N-channel Metal Oxide Semiconductor
NF	Noise Figure
P1dB	1dB Compression Point
PA	Power Amplifier
PMOS	P-channel Metal Oxide Semiconductor
PS	Phase Shifter
RADAR	Radio Detecting And Ranging
RF	Radio Frequency
RMS	Root-Mean-Square
RTPS	Reflection Type Phase Shifter
RX	Receiver
SiGe	Silicon-Germanium
SPDT	Single-Pole-Double-Throw
T/R	Transmit/Receive
TX	Transmitter
VGA	Variable Gain Amplifier
WWII	WorldWarII

1. INTRODUCTION

1.1. Brief History of RADAR

Human kind tend to protect themselves from so-called "outside effects" with various ways, where RAdio Detection And Ranging (RADAR) can be categorized as one example for defending mechanisms. Even if RADAR systems had started to develop early 20^{th} century, and been seen as a discovery of scientists, nature itself already implements this invention as ultrasonic sensors of bats. Bats uses short screams, which can be referred as transmitter, to estimate places of different objects with the help its ears that are antenna and act like a receiver. They can also trace nutrient with the help of their own RADAR system. However, it seems evolution is not without a sense of irony; defending system for bats also exists in nature itself. Some moth species evolved an ear system that can detect and mix bat's RADAR system to protect itself [1].

It is usually thought that first RADAR concept was introduced during early period of World War II (WWII), but initiatory steps were done by German inventor Christian Hulsmeyer, at 1904. His invention "Telemobiloscop" was used to avoid collision of ships that do not have clear field of view due to poor weather conditions [2]. In early years of WWII, RADAR systems were started to be used more widely, and England used them to protect themselves from German aircrafts, which was the first time that system is used in military applications [2].

As years past, RADAR technology had evolved and expanded its market to different application areas, such as auto collision [3], and weather monitoring [4]. For some applications, especially for military, RADAR systems include mechanical equipment which enables to increase detectable area, but scanning rate of defined RADAR is determined by the mechanical system itself, which is hundreds of scans per minute [5]. With current enhancements in semiconductor technologies, mechanical parts can be replaced with electronic counterparts, which gives the chance of hundreds of

scanning per second. On the other hand, due to applying electronics solutions to RADAR concept, resultant systems will be much smaller and cheaper which gives the ability to broaden market size [6].

1.2. Phased Array RADAR

Even if its market extended with introducing new products for commercial purposes, military applications are still covering highest percentage cut in phased array RADAR systems. Active Phased Array RADAR (APAR) can be referred as one product of market, which is widely used in military applications. Not only detecting, but also tracking and neutralizing are two of the most significant features of APAR systems. One of the main reasons that APAR systems are preferred is their "track-while-scan" functionality; as a result of this property, they can perform different processes in a short time period, while it is an essential requirement for Anti-Air force Warfare (AAW) systems. SPY-1 RADAR is demonstrated in Fig.1(a)**.**

Previous generation RADAR systems utilize mechanical equipments to achieve beam scanning, while it have some advantages and disadvantages. One advantage of mechanical scanning over phased array systems is high detection range; as scanning rate increase, less time will spent to receive reflected signal, which leads to reduction in detection range. However, AAW requirements cannot be satisfied due to low data rate; they have poor tracking capability. Also, their performance can be affected from outside effects such as vibration; whole RADAR system can malfunction if motor equipment fails, which rotates antenna. Electronic-scanning gives the chance of high data rate, which results with not only detecting and tracking of an object but also responding to it. On the other hand, they are more resistant than mechanical-scanning due to having no moving equipment [5].

Phased array system also preferred to be used in commercial applications. RADARs for radio astronomy [7], automotive RADAR as assistance systems [8], Doppler weather RADAR [9], which can be seen from Fig.1 (b), are some commercial applications phased array systems. Current improvements in electronics give chance to construct thousands of Transmitter and Receiver Modules (T/R Modules) on-chip, which can be synchronized for generating multifunctional phased array system. As a

(a) (b)

Fig. 1. View of a) SPY-1 RADAR b) Doppler Weather RADAR

result, RADAR systems will be cheaper, lighter, and more functional, which will expand their market for commercial applications.

Phased array systems consist of several elements, which are working independently but coherently with each other. Electronic beam shifting mechanism can be achieved with using different radiation or transmission from each element. For receiver chain, each element in system will receive separate signals, which can be combined in desired way, due to having separate control on each element. Transmitting is similar to receiving mechanism, but signal path will be in reverse direction.

Fig.2 represents basic block diagram of phased array system that has N separate element. There will a time delay between each received signal, which depends on the distance between each component. With introducing adequate level of delay to each received signal, output of the receiver, R(t), can be founded as [10];

$$R(t) = \sum_{k=0}^{n-1} i\left(t - k\tau - (n-1-k)\frac{d\sin\theta}{c} \right) \quad (1)$$

where i(t) is incoming signal with a certain angle θ. d symbolize distance between separate elements, where multiple of delay for each element is represented with τ, and c is speed of light. Summing received signal without calibrating their delays, would end up with low level of output signal, which can be failure for receiver system. Introducing

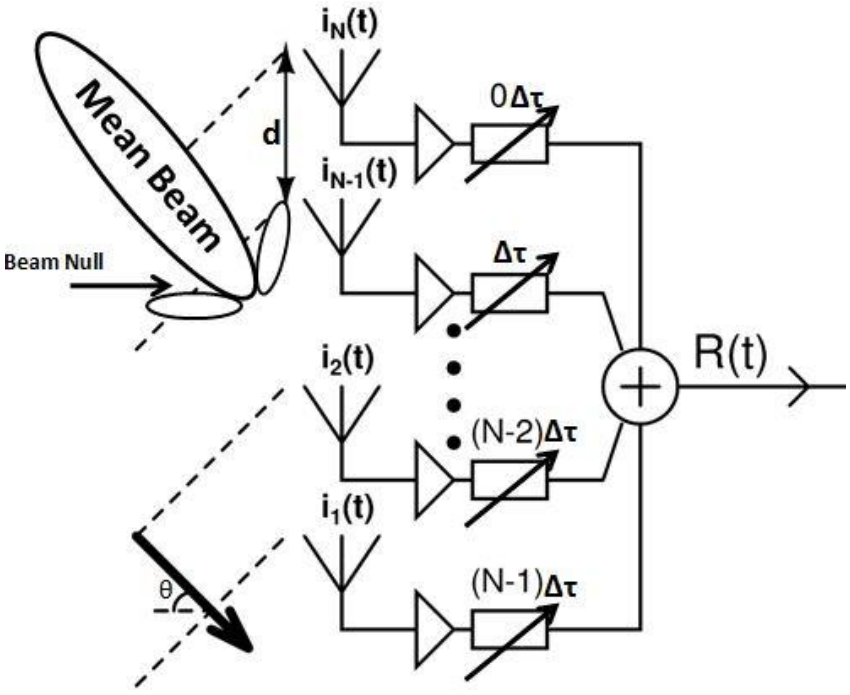


Fig. 2. N-element Phased Array system example

delay to each element regarding their distance to reference, results with higher gain at receiver output, due to adding up all elements coherently. On the other hand, unexpected signals that mainly due to side lobes, are rejected by system itself due to having much lower gain. One of the advantages of this architecture is having low noise performance; received signal firstly amplified without any other processes that may introduce noise. As a result added noise for given architecture will be smaller, which will enhance the sensitivity of the system [11].

As in receiver, similar remarks can be done for transmitter. Consistent addition of each transmitter power will result with much higher output power. If array elements are assumed to be isotropic, Effective Isotropic Radiated Power (EIRP) can be calculated as $N*P_t$, where P_t is transmitter power from a single array element, for N-element system. The reason of this enhancement is basically due to increase in number of elements; as number of elements increase, additional antenna gain and transmitting elements are introduced, which increases EIRP. As a result much higher output power can be achieved by using thousands of radiating elements.

1.3. Phased Array and T/R Module Architectures

One of the most essential requirements of on-chip phased array T/R module systems, is operating frequency range of transistors that are used in structure, but even if transistor technology improve its performance parameter, still there exits some limitations for high performance requirements, such as breakdown voltage of transistors. On the other hand, technologies that can supply high performance are expensive and occupy too much area. As a result of having different specifications and expectations, there exist various types of phased array and T/R module structures, which are used for different requirements.

When their feeding principles are considered, phased array structures can be categorized into two architectures as passive phased arrays, and active phased arrays. Passive phased array (Fig.3) systems are rely on transmitting or receiving from single source, where several antenna elements are connected to individual phase shifter elements to serve or transmit applied signal. For transmitting chain, a Power Amplifier (PA) sends high output signal to signal former, which divide incoming signal to several signal paths. When number of antenna and phase shifter elements are considered, the output power of PA should be tremendously high to satisfy system requirements. Similar concerns can be told for receiver chain. In addition, there exist single PA and LNA which may result in system failure if one of them is malfunctioned.

Active phased array architecture, as represented in Fig.3 (b), has advantages over passive ones. Each antenna element has its own phase shifter and its own amplification stage, which is different from passive phased array approach. If a failure happens for an amplification stage, only performance of related antenna element will be affected, which will not cause a malfunction for the system. Moreover, active phased array systems can perform better sensitivity; passive phased array approach introduce passive phase shifter and signal former before LNA, which increase the noise level of the system. Input signal is amplified by LNA before any other signal process in active phase shifters, which results with lower Noise Figure (NF) performance, so higher sensitivity. Similarly for transmission, less output power is expected from PA, due to including various number of radiating element. As a result, requiring low output power per element, on-chip solutions can be applied with decreased area and cost of system.

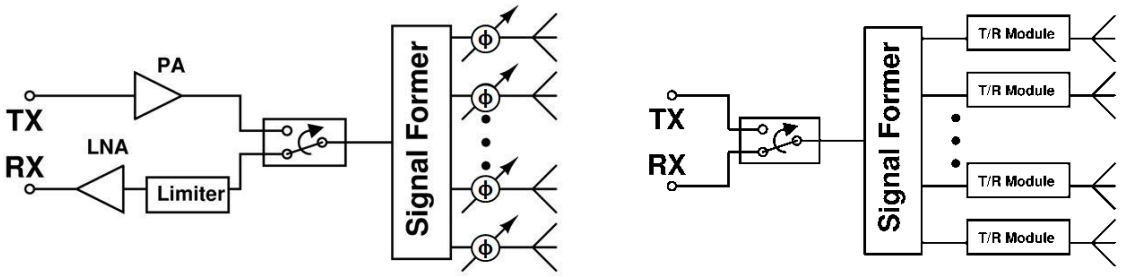


Fig. 3. Block Diagram of a) Passive Phased Array b) Active Phased Array

Mentioned two phased array approaches has a common point; shifting phase in RF frequency. There also exist other phased array approaches, which vary phase in Intermediate Frequency (IF). RF phase shifters are adding loss to system due to being designed in passive topologies, so higher gain and lower NF results can be obtained with placing phase shifter in IF bandwidth. IF has larger wavelength, which results in much larger PS; as a result IF phase shifting phased arrays consumes larger area.

Digital beam formation is another way that is used in phased array systems. Different than other phased arrays, phase shifters are removed from system. Instead of changing phase in RF, phase varied with mixers and Analog-to-Digital Converters (ADC). For this purpose each signal path should include separate mixers and ADCs, which increase power consumption.

All-RF approach has a feature that differentiates it from others; output signals are summed up before mixer. So, any interfering signal can be filtered out from resultant output, which improves linearity of design [12]. However, including phase shifter in RF domain, brings along disadvantages; due to not having high quality factor inductors, phase shifters suffer from high loss. Active phase shifter can be seen as an option for phase shifter designs, but they lack linearity. Regular active phase shifters may degrade linearity advantage of All-RF architecture. Beyond mentioned concerns, All-RF approach is one of the most suitable structures for integrated circuit applications, because RF domain requirements can be satisfied with semiconductor technology, which will lead to a cost efficient solution.

As a result of including most of the block in RF domain, T/R modules undertake critical role for phase array systems. A T/R module for All-RF approach includes Low Noise Amplifier (LNA), Power Amplifier (PA), Phase Shifter (PS), T/R Switch, Single-

Pole-Double-Throw (SPDT) switch, and Variable Gain Amplifier (VGA) or Attenuator. Fig.4 represents different T/R module examples.

One of the ways of constructing T/R module is to combine transmitting and receiving end of the paths with the help of T/R switch, as in Fig.4 (a). Proposed design includes single T/R switch, LNA, and PA, where PS and VGA are duplicated, which results with large area and high consumption.

Fig.4 (b) represents a solution for duplication of structures; combining common blocks. Different then previous example, SPDT switches direct incoming signal to appropriate paths; for received signal, switches are directed to LNA where they are switched to PA for transmitting mode. There is no switch for PS and VGA because they are common blocks; as a result covered area is decreased in compared with previous T/R module example. The drawback of this T/R module design again lies behind the common blocks; they should be operating in bidirectional way. One of the easiest ways of constructing bidirectional PS is, selecting passive phase shifter topologies, while also VGA can be converted to Attenuator. With applying mentioned approach, LNA and PA should aim much better metrics to compensate the losses of additional passive structures. On the other hand there might be an oscillation problem, if T/R switch and SPDT switch do not isolate well; transmitting signal can leak to LNA which will be amplified and introduced back to PA, due to poor isolation performance of switches.

Used SPDT switches can also be placed in a manner that they prevent bidirectional behavior; T/R module sample of Fig.4 (c) uses same components as in Fig.4 (b) but SPDT switches are located such that they prevent bidirectional behavior. As a result, design of each block become simpler, with having chance of tolerating losses of switches with using active components.

Different phased array RADAR structures can be compared with regarding some performance parameters, such as search, maximum range (R_{MAX}), track, and track accuracy. Detecting and targeting performance is defined with R_{MAX}, as a result it is one of the most significant Figure-of-Merits (FOM) for RADAR systems. Basic RADAR equation [13] can be given as:

$$P_r = P_t \frac{G_t A_r \sigma}{(4\pi)^2 R^4} \tag{2}$$

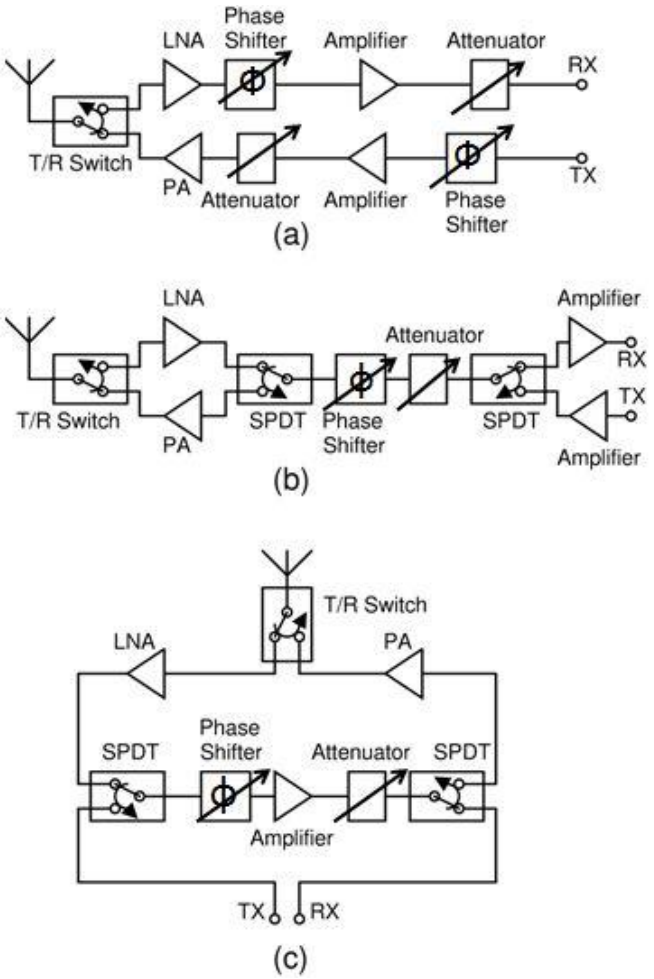


Fig. 4. Various All-RF T/R Module architectures

Equation (2) includes parameters such as receiving power (P_r), transmitted power (P_t), antenna aperature (A_r) that can be extracted from antenna gain. Distance between object and system (R) is one of the basic parameters of RADAR systems, where σ is cross-section of detected object. When transmitted power of a single element is defined as P_t, total radiating power can be calculated as NP_t, for a system that includes N-element. So, as number of elements increase total radiated power improves. Similar methodology can be applied for antenna gain (G_r) and A_r. R_{MAX} defined with maximum radar range, as a result P_r should be replaced with minimum detectable signal, P_{min}, where distance can be converted to R_{MAX} in equation (3). When defined conversions and substitutions are done, R_{MAX} can be founded as

$$R_{MAX} = \sqrt[4]{\frac{NP_t(NA_t)^2\sigma}{\lambda^2 P_{\min}}} = \sqrt[4]{\frac{N^3 P_t A_t^2 \sigma}{\lambda^2 P_{\min}}} \quad (3)$$

When (3) is analyzed, it can be observed that one of the most significant parameter of maximum RADAR detection range is not transmitted or minimum detectable signal, but number of array elements. As P_t increase R_{MAX} will improve, but it will conclude with rising heat dissipation per element, which causes system to require an improved cooling system. So increasing transmitted power may not be a feasible solution to increase R_{max}. To conclude with better RADAR performance, number of elements can be increased; number of elements is most influential parameter on R_{MAX}, but after exceeding a certain limit, rising number of elements will not satisfy phased array requirements, due to increasing weight, cost and power consumption.

In terms of the explained performance parameters, All-RF T/R Module with SiGe BiCMOS technology is one of the best solutions for phased array RADAR applications. Blocks of All-RF architecture can be satisfied with SiGe BiCMOS technology, which will also result with adequate system performance. Phased array systems may require thousands of elements to achieve certain level of performance. If III-V technology is utilized for T/R module, there will be some significant disadvantages, even system achieve expected performance level, such as high cost, large area, heavy weight, and high heat dissipation. When current trend of T/R modules for phased array RADAR application is considered, preferring All-RF architecture with utilizing SiGe BiCMOS technology can be a good alternative.

1.4. SiGe HBT BiCMOS Technology

III-V technologies are being utilized in T/R modules, due to satisfying high system performance requirements. With recent improvements in SiGe HBT technology, similar performance metrics can be caught up, without sacrificing advantages of Si-based technologies. Before explaining SiGe technology, it would be beneficial to emphasize high speed devices.

So called high frequency devices can be as described with devices that can achieve high operation speed. There exist different ways to obtain high speed of operation. Junction resistances and capacitances play a significant role on speed of operation, but to reach high frequency levels such as THz level, different approaches should be applied. One way to achieve this operation speed is to increase the carrier mobility, which will increase frequency limit of device. To achieve high operating

frequency aims, different approaches are applied in time. High Electron Mobility Transistor (HEMT) uses modulation doping technique to achieve high carrier mobility. Heterojuction Field Effect Transistor (HFET) is heterojunction version of Metal Semiconductor Field Effect Transistor (MESFET) [14].

It is important to understand the working principle of Bipolar Junction Transistor (BJT), because Heterojuction Bipolar Transistor (HBT) is based on (BJT) principles. BJT is a three terminal device, emitter and collector terminals have same type doping, while base terminal is opposite type of doping. For amplification purposes, usually BJT is biased in way that base-emitter junction is forward biased, while base-collector junction is reverse biased; described working region of BJT is named as forward-active mode. In Fig.5 (a), a npn BJT that is working in forward-active mode, is represented.

If an npn type BJT is in forward active mode, majority carriers of emitter terminal will be injected to the base terminal, with the help of base-emitter voltage (V_{BE}). Injected majority carriers of emitter, which are electrons, become minority carrier in base terminal; as a result electrons, so called minority carries for npn, are diffused into the base terminal. If diffused electrons manage to reach base-collector junction, they will be swept to collector terminal, due to reverse bias of base-collector voltage (V_{CE}). The travel of minority carries in base terminal is significant, because they can collide with majority carriers in base, and neutralized. The recombination and generation event is influential on device performance, because minority carriers are decreased during this process, which degrade current gain. Current gain (β) is a device parameter, which symbolizes amount of minority carriers that able to pass base and reach collector terminal. During diffusion process, not only minority carrier but also a majority carrier is neutralized, which should be replaced with new majority carrier; as a result base current increase with decrease β. To decrease the possible collision of minority and majority carriers, the traveling time of minority carriers should be shortened, which can be achieved with thin base terminal. As a result, minority carriers spent less time in base and more minority carriers will reach terminal, which will improve β. Current gain can be approximated as;

$$\beta_0 \approx \frac{D_{nB}}{D_{pE}} \frac{w_E}{w_B} \frac{N_{DE}}{N_{AB}} \tag{4}$$

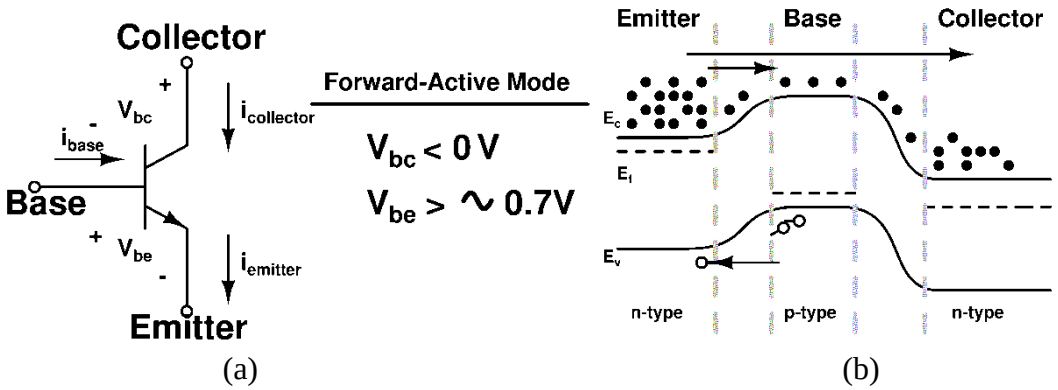


Fig. 5. a) Symbolic and b) band diagram description of BJT

When equation (4) is analyzed doping levels of emitter and base terminals are also significant, as width of base and emitter. As base doping increase, the resistance of base terminal will decrease, which will raise the number of minority carries that passes through base. On the other hand, doping of the base terminal should not exceed a certain level, because minority carries should be emitted from emitter. Increasing emitter doping can also improve the performance of device, but this time emitter-base capacitance increases, which degrades frequency performance of device directly. So, increasing base doping to a certain level, will improve device performance.

III-V semiconductors are prefered to be used for high speed devices, such as HBT, MESFET, HFET, and HEMT. Actually materials are not selected randomly, but selected with regarding system requeirements, which is named as Application-Induced Design Constraints; materials are selected with considering expected system and device performance parameters. For instance, each circuiry searches for low noise performance, but it is a more crucial parameter for Low Noise Amplifier (LNA) in compared to a microprocessor; as a result, material selection may differ from application to application. For high frequency applications, III-V devices are prefered instead of Si-based devices, because they can achieve higher frequency levels, due to having higher carrier mobility. In compared with III-V technology, Si-based devices are lacking high frequency performance.

Beside of high frequency advantages, III-V devices have significant disadvantages in compare with Si-based ones. Having no robust thermally grown oxide for III-V

technology is one of the most significant disadvantages. Also, wafers that are fabricated for III-V devices, can have larger defect density; as a result they are more incline to break. On the other hand, they are poor heat conductors, so heat dissipation for circuits with III-V devices is a serious problem that waits to be solved. As a consequence of all disadvantages, III-V technology has low device integration, and low yield; as a result cost of fabrication process is high. In other meaning, cost per die is high, which causes III-V devices more expensive than Si-based devices [15]. III-V devices are used with disregarding all mentioned disadvantages, because expected high performance can only be achieved with using III-V semiconductors. Otherwise, targeted system specifications cannot be achieved.

Then why silicon based technologies are still in use, if they cannot perform well enough? Different than other technologies, silicon based technologies have high level of integration with high yield. As a result cost per die is very low. Thus, the "beauty" of silicon is not coming from its performance, but material properties and its fabrication. Silicon is one of the most abounded and purest materials on Earth. Also, large scaled silicon wafer can be fabricated due to being defect free, which increase number of dies per fabrication, so decrease cost. Heat dissipation is significant issue for III-V devices, whereas silicon has better thermal properties. On the other hand, silicon can easily be etched, grown, and deposited. Its doping can be controllably done for both for n-type and p-type. Different than III-V semiconductors high quality dielectric, which is silicon dioxide, can easily be formed on silicon substrate for electrical isolation, surface passivation, etch stop layer, planarization layer, masking layer, or as an active layer [15].

Silicon technology is dominating major part of microelectronic industry, even it suffers from high performance requirements. When all advantages and disadvantages of both technologies are compared, it can be said that "economic issues command the driver's seat" [15]. One of the most significant parameters in semiconductor industry is its cost, because if it is not cheap, then product may not have chance to spread in different markets, even it achieves high performance. A perfect semiconductor device can be summarized with having all advantages; a device that have low noise, high linearity with low power consumption, high speed, high integration capability, high yield and low cost. Bandgap engineering's target is to achieve perfect semiconductor,

and it is defined as tailoring of semiconductors in atomic scale. SiGe HBT BiCMOS technology is a product of bandgap engineering.

Heterojunction Bipolar Transistor (HBT) has same device structure as BJT, except base terminal is heterogeneous. The energy bandgap of Germanium (Ge) is 0.66eV, while it is 1.12eV for Silicon (Si). If both materials are combined together, new material will have a bandgap energy that is between Si and Ge. SiGe HBT devices are depending on combination of two different materials to form a new device, which has a higher carrier speed in compared with BJT.

As mentioned before, travel of minority carriers in base terminal of BJT is very critical; minority carries should spend less time in base terminal for producing a high speed device. With heterogeneous base terminal high speed HBTs can be obtained. If Si and Ge are combined together throughout the terminal, the resultant will be a constant bandgap energy that is between 0.66eV and 1.12eV. Instead of introducing Ge to base terminal with a constant ratio, graded Ge doping will cause graded bandgap energy from emitter to collector junction. Minimum Ge concentration is in base-emitter junction. As traveled throughout base terminal Ge concentration increase, which decrease bandgap energy. At collector-base junction, bandgap energy will be lower than 1.12eV, which results with a certain level of potential difference between emitter and collector terminals. Existence of potential difference will cause an electric that will swept minority carriers to base-collector junction.

If τ_b and τ_c are base and collector transit times, respectively, the cut-off frequency (f_T), and oscillation frequency (f_{MAX}) of HBT can be described with,

$$f_T = \frac{1}{2\pi\tau_{EC}} \quad ; \quad f_{\max} = \sqrt{\frac{f_T}{8\pi R_B C_{cb}}} \tag{5}$$

where,

$$\tau_{EC} = \tau_b + \tau_c + \frac{1}{g_m}\left(C_\pi + C_\mu\right) + (r_e + r_c)C_\mu \tag{6}$$

As can be seen from frequency expressions, time spent is significant for the operating frequency range of device, which emphasizes the importance of swept. The word swept is referring drift effect which causes minority carriers spend less time in base terminal, which improves frequency performance of device. Fig.6 (b) demonstrates

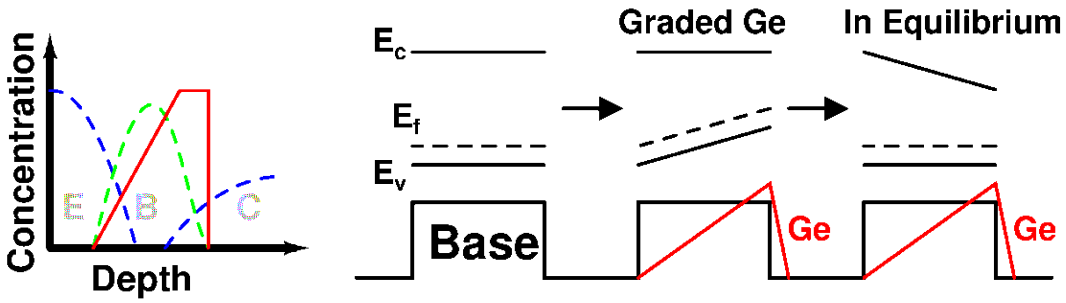


Fig. 6. a) Concentration of Ge through device and b) energy band diagram of HBT

formation of energy bandgap when Ge is introduced to base terminal. As Ge concentration increase linearly throughout the base terminal, Fermi level and valance band bend up, due to having new bandgap energy that is getting smaller as Ge concentration increase. In equilibrium Fermi level should be at its initial level; as a result, conduction band should change to protect the bandgap energy, which results with decaying conduction band, until base-collector junction. Moreover, energy gap for holes increase with introducing Ge to base terminal; as a result hole injection from base terminal decreases, which improves current gain. On the other hand, Boron doping in base terminal can extend to emitter and collector junctions, even with a small temperature variation during fabrication process, which degrades device performance, due to increasing base width. To prevent base terminal extension, base terminal is also doped with Carbon, to protect thin base width.

Forming base terminal with Ge profile result with HBT that can achieve comparable performance metrics with III-V devices, but other than high performance, its ability of integration with CMOS technology is also a very influential reason for preferring SiGe devices. Due to being processed on same substrate material, CMOS and SiGe HBT can be fabricated together, without any degradation in performances of technologies. Integration capability of SiGe brought an important advantage among III-V technologies, and it is closer to ideal semiconductor device in compared with III-V devices. As a result, it will be more favorable to use SiGe technology in commercial applications, which is also extent the market of T/R module. On the other hand, they can satisfy on-chip T/R module requirements with lower cost, higher integration, and lighter weight. So they can be utilized for next generations of T/R modules for phased array RADAR applications.

1.5. Proposed T/R Module

T/R module is one of the most essential blocks of Phased Array system, and Fig.7 represents proposed X-Band SiGe BiCMOS T/R module. All-RF architecture is chosen from different T/R module architectures that are mentioned in previous sections. All-RF T/R module combines transmitting and receiving paths without requiring bidirectional blocks. On the other hand phase shifting mechanism is introduced as a separate RF block. Preferred T/R module includes Low Noise Amplifier (LNA), Power Amplifier (PA), Phase Shifter (PS), Single-Pole-Double-Throw (SPDT) switch, and Variable Gain Amplifier (VGA). All sub-blocks will be designed in 0.13µm SiGe BiCMOS technology. For amplification purposes, such as for PA and LNA, High Performance (HP) and High Breakdown-voltage (HB) transistors will be used, while CMOS transistors are planned to be used mainly for switching purposes; selection of appropriate path for transmitting and receiver chain is done with SPDT switch, where PS and VGA is shared with both signal paths. LNA is used as the first amplification block for incoming signal, where PA is used for transmitting high power signals. SPDT is preferred for selecting signal, with proper level of isolation between transmitting and receiving chain. Electronic beam scanning mechanism is achieved with changing the phase component of signal, which is achieved with PS. VGA, is mainly used for tolerating gain errors that occur after different phase states. This section will summarize functionality of each block of T/R module, with mentioning their performance metrics.

LNA is the first block of receiver block; as a result its performance is very influential on receiver chain. Noise of LNA will directly be added on input signal, due to being first block, which makes LNA mainly decide sensitivity of whole T/R module. When similar samples are analyzed, 5dB of Noise Figure (NF) is mainly aimed for T/R module. With assuming 2dB of NF for T/R switch, at most 2dB NF performance should be aimed for LNA to achieve a state of the art T/R module performance. Input signal of LNA is in very low power levels; as a result it should be amplified with adding low noise. LNA is only amplifying block in receiver chain, if VGA is counted as a gain tolerating block. So, total gain of LNA should be high enough to result with high power signal at output terminal of receiver chain. On the other hand, with introducing high gain from LNA, noise effects that are added by other blocks of receiver chain will be suppressed.

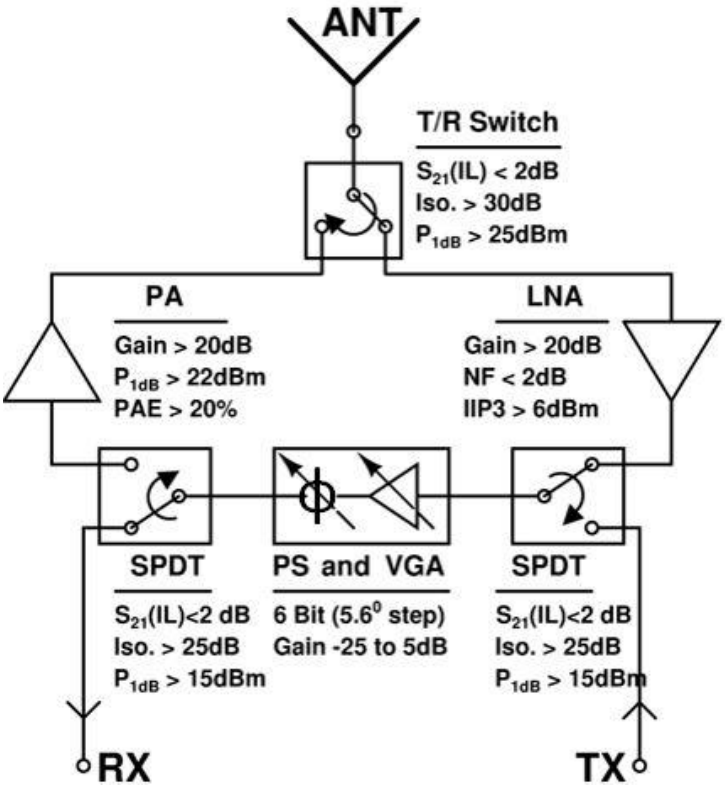


Fig. 7. Block diagram of X-Band phased array T/R Module

Dynamic range is another parameter of LNA, which can depreciate with high gain. Input-referred compression point (input-P1dB), and input-referred 3rd order intercept point (IIP_3) are two parameters that are used to define dynamic range of LNA. Received input power level is determined with mentioned two parameters, and to achieve high dynamic range with high gain in receiver chain, 6dBm of IIP_3 is targeted. Aimed performance specifications are challenging for LNA to achieve with 0.13μm SiGe BiCMOS technology.

LNA for receiver chain is equivalent to PA for transmitter chain; their functionality is mainly different, but its importance for each chain is very similar. PA is the last block of transmitting chain, which enables transmitting signals with high output power. For next generations of phased array systems that includes several elements, approximately 500mW of output power per T/R module will be required, which is equivalent to about 27dBm of output power for radiating element. When 5dB of antenna gain is assumed, at least 22dBm of output power is required for transmitting chain, which is supplied by PA. As maximum operating frequency increase, breakdown

voltage of transistors decrease; as a result achieving 22dBm of output power from 0.13μm SiGe BiCMOS technology is another challenging performance metric.

Beam scanning mechanism functionality of phased array system depends on the performance of PS block of T/R module. Resolution of phase shift determines the directivity, side-lobe and main-lobe lobe levels of beam. Linearity of T/R module mainly decided by LNA, but PS should have suitable level of input dynamic range to process incoming signal without any distortion. As a result, PS should have adequate level of linearity performance in addition to high phase resolution. For resulting high phase resolution in wide bandwidth with high linearity, hybrid PS architecture is proposed in this thesis. Hybrid PS targeted at most 5.6^0 of Root-Mean-Square (RMS) phase error, with about 15dBm of input-P1dB and at most 25dB of loss. Different phase states of PS can have different gain performances which is an undesired behavior. VGA amplifier is used for compensating gain difference of each phase states, with varying amplifier gain. PS can introduce loss to chain which may result with low gain. Other than gain error, loss of PS can also be compensated with VGA.

SPDT switch gives the chance of combining transmitter and receiver chains; it enables to combine common blocks of T/R module. As a result total module design can conclude in a smaller area. SPDT switch are leading input signal to appropriate path, with regarding control voltages. One of the most significant parameter of SPDT switch is its loss performance; due to having a single amplifier in both stages, high loss may result low output power for transmitter, and low gain for receiver chain. As a result, first concern of SPDT switch is its insertion loss. On the other hand, high loss will also affect NF performance of design. Isolation between ports is another performance metric for SPDT switch; isolation between ports should be high enough to prevent leakage. As in PS, power handling capability of SPDT switch is important to determine the linearity of receiver chain. Similarly to SPDT switch, T/R switch aims to direct signal from module to antenna or from antenna to module. Different than SPDT switch, it requires much better isolation, to prevent output signal of transmitter received by LNA, due to leakage. On the other hand, it should have low loss to keep output of TX high, and to increase loss and NF for receiver chain.

In this thesis, high dynamic range LNA, and high phase resolution hybrid phase shifter is presented, which are designed with regarding proposed T/R Module. Single-

stage cascode LNA, telescopic LNA, and two-stage cascode LNA designed with regarding mentioned performance criteria, while two-stage cascode LNA achieved more than 20dB gain, lower than 2dB NF, -3.72dBm input-P1dB while consuming 115.8mW. Hybrid phase shifter tried to combine advantages of different methodologies such as I/Q generator of vector modulator and filter type phase shifter. It achieved 6.75GHz of bandwidth for 5.6^0 of RMS phase error. On the other hand, it can perform as 7-bit phase shifter for 4.5GHz of bandwidth. It can safely be used for proposed linear T/R module, due to having at least 10dBm of input-P1dB. Much detailed description for each designed block will be given in following sections.

1.6. Motivation

Phased Array T/R modules require high performance, which can be achieved with III-V technology. Market for T/R module is limited due to high cost, high power consumption and heavy weight. Recent enhancements in SiGe BiCMOS technology extent performance of Si-based devices, and give chance to T/R module architecture to widen its market, due to being a product of Si-based technology, which is preferred for commercial application, due to its low cost. On the other hand, technological restrictions of SiGe technology is limiting factor; low breakdown voltage levels and components with low quality factor prevent T/R module to transmit high power signals. Similarly, gain and NF performance is limiting sensitivity of receiver chain, due to having transistors, which has lower cut-off frequency. As in output power, input dynamic range is restricted with low breakdown voltage level of transistors. As a result, new architectures and methodologies should be applied to realize similar performance with III-V technology based T/R modules.

Objective of this thesis is to design sub-blocks for X-Band T/R module with SiGe HBT BiCMOS technology, which will be able to compete and replace sub-blocks of III-V based T/R module. For this purpose, high dynamic range LNA designs and wideband hybrid phase shifter with high phase resolution is presented in this thesis, with regarding mentioned T/R module architecture in Fig.7.

1.7. Organization

Chapter 2 introduces different approaches for Low Noise Amplifier (LNA) that is designed for phased array T/R module. Three different LNA topologies are designed with regarding performance expectations, such as linearity. Single-stage cascode, telescopic and two-stage cascode topologies are used for achieving high linearity with high gain and low NF performance. Single-stage cascode LNA achieved -0.25dBm of input-P1dB, mean 10dB gain, with 1.9dB of NF at 9GHz, while consuming 12.5mW. Telescopic LNA design has peak 18.3dB gain, when its mean gain is about 15dB at 7.5GHz. Telescopic LNA has 2.5dBm of measured input-P1dB, while NF is lower than 2dB at 7.5GHz. Two-stage cascode LNA designed with regarding breakdown voltage variations, when size of the transistors is scaled. Each stage is designed with regarding different performance specifications; first stage for moderate gain, and low NF, while second stage stands for high linearity with low gain. Designed two-stage LNA achieved more than 20.5dB gain, lower than 2dB NF, with -3.72dBm of input-P1dB of power consumption, while consuming 115.8mW. Compared with similar works, two-stage cascode LNA with proposed linearity technique achieves one of the best results in terms of total gain, linearity and power consumption of two-stage LNA.

Chapter 3 explains a new approach to phase shifter design, which aims to take advantage of different phase shifter architectures, such as vector modulator and High Pass/Low Pass Filter type phase shifters. Passive phase shifters has narrow band phase performance, while they have high loss and consume large areas, due to including passive structures, such as inductors. However, they can achieve high linearity, which is essential for T/R module with high dynamic range receiver chain. Vector modulator can achieve low phase error in wideband, but they suffer from linearity. Hybrid phase shifter achieved 6.75GHz of bandwidth for 6-bit operation, with 10dB loss. Design also includes correction states that reduce errors if there exist any. Same correction states can be used to generate 7-bit operating phase shifter, without any additional circuitry. Hybrid phase shifter achieves about 4.5GHz of bandwidth for 7-bit operation, with at least 10dBm of input-referred compression point. Moreover, operating bit per area is larger than passive phase shifter architectures.

Chapter 4 summarizes the content of this thesis, and concludes with giving information about possible future studies and works.

2. HIGH DYNAMIC RANGE LOW NOISE AMPLIFIER FOR X-BAND SiGe T/R MODULE

2.1. Introduction

In this section, one of the essential blocks of the T/R Module is presented, which is Low Noise Amplifier (LNA). Thanks to bandgap engineering, SiGe HBT BiCMOS technology based T/R module structures had started to be more dominant, due to catching up III-V devices in terms of many performance parameters, such as high cut-off frequency (f_T), and low Noise Figure (NF). LNA is the first block for receiver chain of T/R Module; as a result it directly affects the main performance metrics of receiver.

LNA is the main gain block of whole chain; as a result its performance is very significant for receiver, due to being only block that can supply high gain. If moderate LNA gain is supplied, receiver chain will result with low gain due to including other blocks that introduce loss, such as Phase Shifter, and Single-Pole-Double-Throw (SPDT) switch. On the other hand, NF performance is very crucial for the LNA structures. It is important to add as low noise as possible to incoming input, throughout the whole structure. LNA is not only responsible for high gain response of the chain, but also introduces low NF, which prevents the incoming signal be lost in high noise. Also, noise contribution from remaining blocks is suppressed, with performing high gain. As in gain, and NF case, linearity is another metric for LNA, which defines power level that LNA can amplify without any distortion.

When all of the mentioned parameters are concerned, LNA is a block that should achieve high performance for different metrics. In this section, three different LNA structures will be described, which aim high linearity, high gain, low NF, and low power consumption. To obtain mentioned specifications single-stage cascode LNA,

telescopic LNA, and two-stage cascode LNA had designed with using 0.13µm SiGe HBT BiCMOS technology of IHP Microelectronics and IBM.

The section will start with description of used SiGe HBT BiCMOS technologies, which will continue with circuit level analysis and results for single-stage cascode LNA, telescopic LNA, and two-stage LNA, respectively. At the end of the chapter, performance comparison with similar works in literature will be done.

2.2. SiGe HBT BiCMOS Technology

For design of single-stage cascode LNA and telescopic LNA IHP Microelectronics 0.13µm SiGe HBT BiCMOS technology is used. Preferred technology provides transistors that can achieve current gain of 700, and 300/500 GHz of f_t /f_{MAX} levels. The Collector-Emitter (CE) breakdown voltage is 1.7V, while Collector-Base (CB) breakdown voltage is 5V. With using the described transistors, at least -4dBm of input-P1dB, gain level between 15-20dB, and at most 2dB NF is aimed. Described process offers two thick top metal layers, and five thin metal layers, which gives chance of designing on-chip high quality factor inductors. Technology also includes metal-isolator-metal (MIM) capacitance, and different types of resistors.

IBM's 0.13µm SiGe HBT BiCMOS technology is chosen for design of two-stage cascode LNA; technology provides high performance transistors with 210GHz of f_T. CE breakdown voltage of High Performance (HP) transistor is 1.8V, while High Breakdown (HB) transistors can achieve 3.4V of CE breakdown voltage. With using mentioned transistors at least 20dB of gain is aimed with similar NF and linearity performances of single-stage and telescopic LNA.

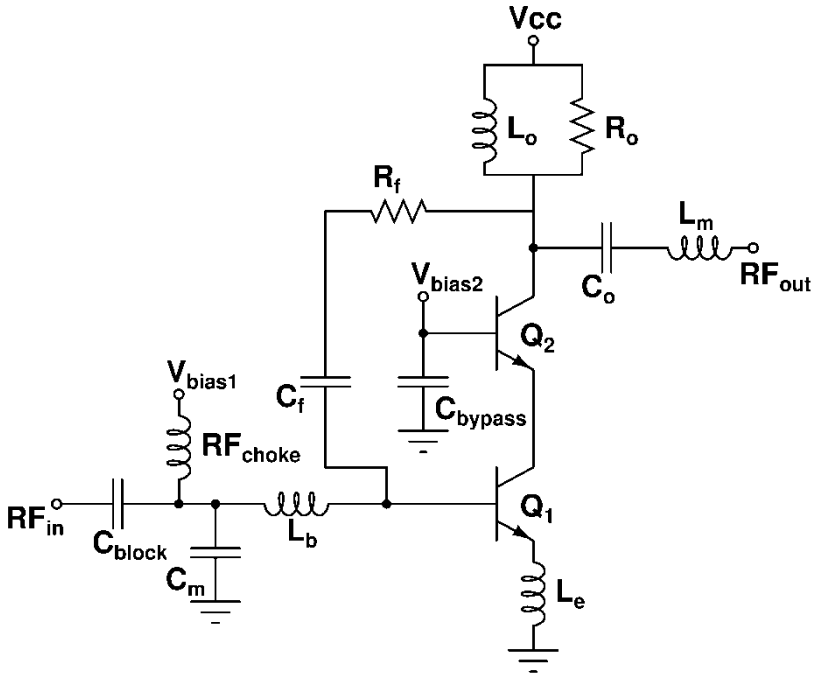


Fig. 8. Schematic view of Single-Stage Cascode Low Noise Amplifier

2.3. Single Stage Cascode LNA

2.3.1. Circuit Design and Analysis

When LNA topologies in literature are analyzed, it is observed that Common Emitter (CE), and cascode topologies are mainly chosen to be used. Cascode structure is most commonly selected design due canceling Miller affect, and its high output resistance; as a result reverse isolation performance is superior, which prevents oscillation when high gain amplifiers designed [16].

In Fig.8, schematic view of designed single-stage cascode LNA can be seen. LNA designs aim performance parameters that mainly conflict with each other, such as high linearity and power consumption. So, it would be a better choice to follow certain designing steps.

As can be understood from its name, LNA firstly aims low NF, because its NF performance it directly added to the system Noise Factor (F). When Friis equation for Noise Factor (F) (7) is analyzed, it can be observed that not only F, but also gain of LNA is very significant, to suppress F that appears due to following blocks.

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}} \quad (7)$$

Thus, it is a better choice to start the design procedure with regarding noise performance. Before NF, lowest minimum NF (NF_{min}) should be selected. When NF_{min} equation [17] is analyzed, the parameters that affects the NF performance can be seen;

$$NF_{\min} = 1 + \frac{n}{\beta_{DC}} + \sqrt{\frac{2J_C}{V_T}(r_e + r_b)_u\left(\frac{f^2}{f_T^2} + \frac{1}{\beta_{DC}}\right) + \frac{n^2}{\beta_{DC}}} \quad (8)$$

Current gain (β) has inverse effect on noise performance, while operating frequency (f) is directly influential on NF_{min}. Technology itself is also significant, because as f_T gets higher, better noise performance can be achieved. Base (r_b), and collector (r_c) resistances is another significant affect that should be concerned for noise figure performance; transistors with double base and collector contact can enhance the noise performance of the design, instead of single terminal contacts.

Other than mentioned effects, there exists a significant parameter that directly concerns the total LNA design, which is current density (J_C). To find optimum J_c for NF_{min}, bias current for the unit sized transistors of cascode design can be varied. Selecting NF_{min} is also crucial for gain performance, because selecting current density is equivalent to choosing base-emitter voltage (V_{be}). If V_{be} voltage is selected at low level to result with better NF performance, then design will suffer from low gain. So, a trade-off exists between gain and NF performance of the design.

For obtaining low NF performance, resistance of the noise source is also very significant, which is the resistance that is seen through the cascode topology. In that manner, optimum source resistance ($R_{s,opt}$) should be selected with regarding a dedicated impedance value to match NF_{min} and power, simultaneously. As can be seen from equation (9),

$$R_{s,opt} = \frac{f_T}{f}\frac{1}{L_E}\sqrt{\frac{2}{J_C}\frac{r_b L_E}{W_E}\frac{kT}{q}} \quad (9)$$

transistor parameters are directly influential on $R_{s,opt}$ [18]. J_c and emitter length (L_E) are two parameters that can be used to match $R_{s,opt}$. J_c should not be changed, because otherwise NF_{min} will veer to unmatched condition. So for matching $R_{s,opt}$ to 50Ω, which is the desired condition, L_E should be adjusted. The drawback of this parameter is increased size of the emitter area; current density will be same as before, while total

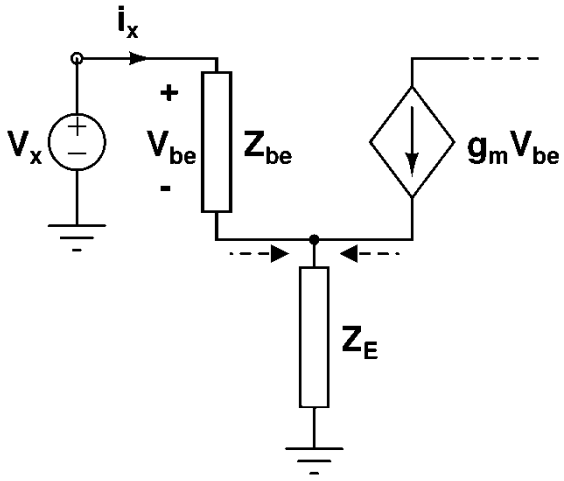


Fig. 9. Small signal representation for driver transistor of cascode design

current that flow through transistor will increase. In other meaning power consumption of design will increase as emitter area increase, which is acceptable to obtain low NF.

After selecting appropriate level of current density and transistor sizes, input matching will be the next step, which is one of the most significant milestones of LNA design, due to matching input matching and noise figure simultaneously. From Fig.9, π-model representation of driver transistor of cascode topology can be seen.

To calculate input impedance, an unknown voltage source, V_X, with an unknown current, I_X, to input terminal is connected to driver transistor. With dividing $V_X / I_X = Z_{in}$, input impedance can be found. The component Z_{be} symbolizes total impedance that occurs due to base-emitter resistance and capacitance, while Z_E is used for representing total impedance that is connected in emitter terminal. Voltage across Z_E can be expressed as,

$$V_x - V_{be} = Z_E\left(\frac{V_{be}}{Z_{be}} + g_m V_{be}\right) \tag{10}$$

where,

$$i_x Z_{be} = V_{be} \tag{11}$$

With some simple simplification, and dividing equation (10) to i_X, input impedance can be founded as

$$Z_{in} = Z_{be} + Z_E(1 + g_m Z_{be}) \tag{12}$$

For understanding the meaning of equation (12) more clearly, some assumptions should be done; base-emitter capacitance is more dominant in Z_{be}, Therefore Z_{be} is approximately equal to C_{be}. Secondly, if a series inductor (L_e) exists in emitter terminal, input impedance can be redefined as equation (13), with regarding mentioned two assumptions;

$$Z_{in} = \frac{-j}{wC_{be}} + jwL_e + g_m \frac{L_e}{C_{be}} \tag{13}$$

When total input impedance is analyzed, it can be seen that there exist a real part, which is determined with transconductance, emitter inductance L_e, and C_{be}. So, connecting a series emitter inductance will give chance of matching real part of input impedance to 50Ω. Emitter degeneration inductance majorly decides the real value of the input impedance, but it also has some affect on imaginary part, as can be seen from equation (13). For the imaginary part of input impedance, another inductor should be added in series to base terminal, to remove the effects of C_{be}.

Before designing output matching network, base voltage for the load transistor Q2 should be selected that has a high impact on linearity performance. Due to having an amplified signal at the output port, collector terminal should have high output swing to result with high linearity. If output signal pulls collector voltage close to emitter voltage level, then load transistor starts to change its region, from forward-active mode to saturation, which causes non-linearity. To prevent that, base voltage is selected in a way that the load transistor is working at CE breakdown voltage limit. In other meaning, base voltage is chosen with regarding the possible swing rate between collector and emitter terminal.

After deciding the base voltage of load transistor, designing process for output matching network can be started. An RL-tank circuitry is decided to be used for the output matching network. Resistance, R_O, is added parallel to the shunt inductor, to decrease the quality factor of the tank circuitry for wider bandwidth, which conflicts with high gain performance. When higher R_0 values are selected to improve gain, LC network will be more dominant on output matching, which will end up with narrow bandwidth.

As in NF-gain case, there exist another trade-off between output matching bandwidth and gain. To improve the bandwidth performance RC feedback is introduced

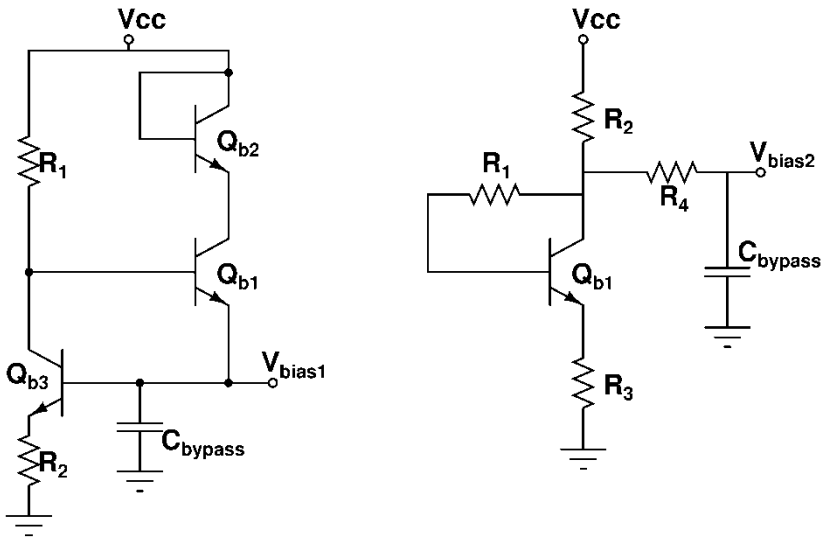


Fig. 10. Preferred active bias networks for Single-Stage cascode LNA

between base of the driver transistor and collector of the load transistor. The feedback capacitance, C_f, is used for blocking DC between base and collector terminals; as a result separate biasing between ports is possible, as can be seen from Fig.9. Feedback resistance, R_f, introduces a resistive affect on output matching; as a result the bandwidth of the output matching network will increase, due to the addition of a frequency independent component. Moreover, the role of transistors on total gain is decreased with improved linearity, when R_f is used [19]. The drawback of resistor feedback is the introduced signal path between input and output terminal; with regarding the resistor value, oscillation phenomena can occur, due to lowering isolation between two ports. On the other hand, feedback resistor not only affects output terminal, but also input terminal; as a result, NF performance degrades. Also a change in terminal will be reflected to the other one, which is another disadvantage for designing process.

For supplying appropriate voltage and current to cascode topology, two different bias networks are designed, which can be seen in Fig.10. For biasing driver transistor, bias network in Fig.10 (a) is used, while bias network in Fig.10 (b) is used for load transistor. The way of connecting bias network and driver transistor is crucial for the design. RF_{choke} components are used for preventing RF signal be leak to ground from the path of DC bias network. High value resistance can be used, which ends up with high input impedance for bias network. For high linearity applications, using resistance is not an appropriate choice as an RF_{choke}. As input signal power gets higher, RF_{choke}

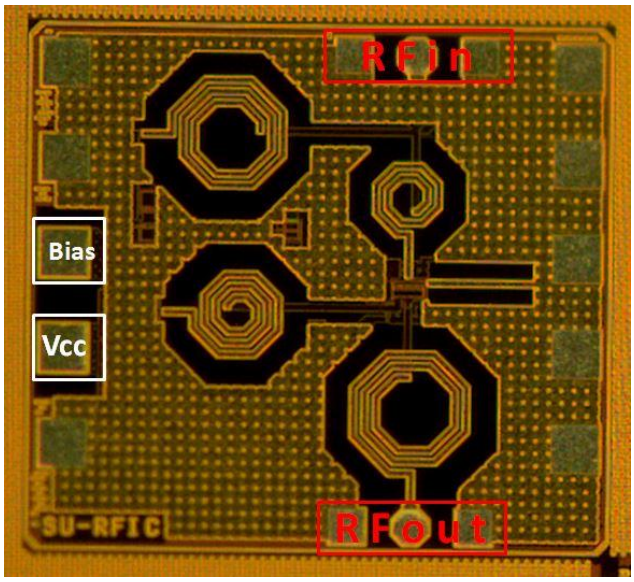


Fig. 11. Die image of Single-Stage LNA

resistance starts to reflect high input power to bias network, which limits input swing range. RF_{choke} inductors prevents distortion at input swing, therefore much higher linearity can be achieved. The disadvantage of inductor in compared to resistance, is its large area.

2.3.2. Measurement and Simulation Results

Total chip area is 830 x 920 μm^2 = 0.76 μm^2, including pads. Total die of the single-stage LNA can be seen from Fig.11. Spiral inductors are full custom designed with using top two thick metal layers, to end up with high quality factor. Emitter degeneration inductor has a small inductance value to be utilized with spiral inductors; as a result a transmission line is used for emitter inductor.

For the measurement of described LNA, fabricated Printed Circuit Boards (PCB) and on-chip measurement setup is used. DC and ground pads of LNA are wire-bonded to PCB board; as a result DC and ground terminals are supported by off-chip supplies. On the other hand, off-chip bypass capacitors are used to cancel noise affects and lower frequency oscillations. A conductive epoxy, which is composed of two parts, is used for sticking certain die to PCB. Cascade Microtech 40GHz GSG probes are used for on-chip measurement of RF pads. With described measurement setup, multiple samples are

measured, and presented measurement results are on behalf of average of all different dies.

DC power pads are connected to active networks and output matching of cascode topology. In simulations, total bias current is 2mA, while collector current is 6mA under 2.5V of supply voltage, which is equal to 20mW. When DC power levels are correctly supplied to chip, total current that flows from the collector terminal is measured as 2mA, which is low in compared with simulations. Having low collector current can have significant consequences for design; the first designing step of the LNA is to select a constant current density. Measuring a low collector current means that selected current density is diverged from designed values. As a result, deviations from input matching, NF performance and gain can be observed. LNA with higher supply voltages result with expected level of collector current; however this time, base voltage will be much different than expected.

For S-Parameter measurement, Agilent 8720ES Network Analyzer is used at room temperature. Fig.12 demonstrates return loss performance of single-stage LNA, with the comparison of its simulation results. There exist about 4dB difference for input matching between 7.5-to-20GHz. Due to having a deviation in current density, such performance degradations for input-matching can be expected. There exist two additional results of having such input return loss performance; poor NF performance, and low gain. Return loss performance for output port, is much similar to the simulation results; output return loss is better than 10dB at 6.5GHz of bandwidth.

Maximum value of total gain is simulated as 16.4dB, while it is measured mean value is about 10dB, as can be seen from Fig.13. As mentioned, low gain performance can be expected due to having a low collector current and poor input matching. Measured S12 performance achieves similar performance with simulated values at X-Band.

For the measurement setup of NF, Agilent E4407B Spectrum Analyzer is used with Agilent 346A Noise Source. A simple representation of measurement setup can be seen from Fig.14. The input of die is connected to a known noise source (Agilent 346A), while its output is connected to the Pre-Amplifier of the spectrum analyzer, which is Agilent 87405C. Before measuring, probes are shorted to each other with the help of on-chip calibration kit. The reason of this procedure is to subtract all noise effect

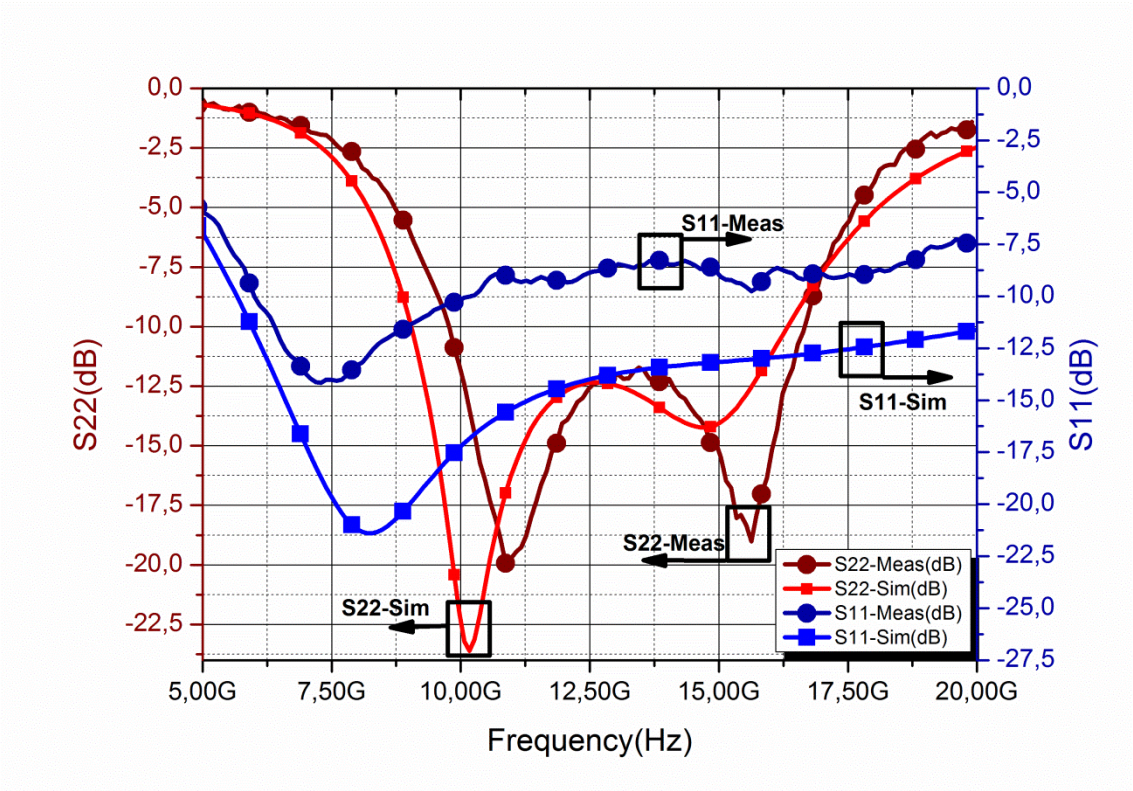


Fig. 12. Simulated and measured return loss performances of Single-Stage LNA

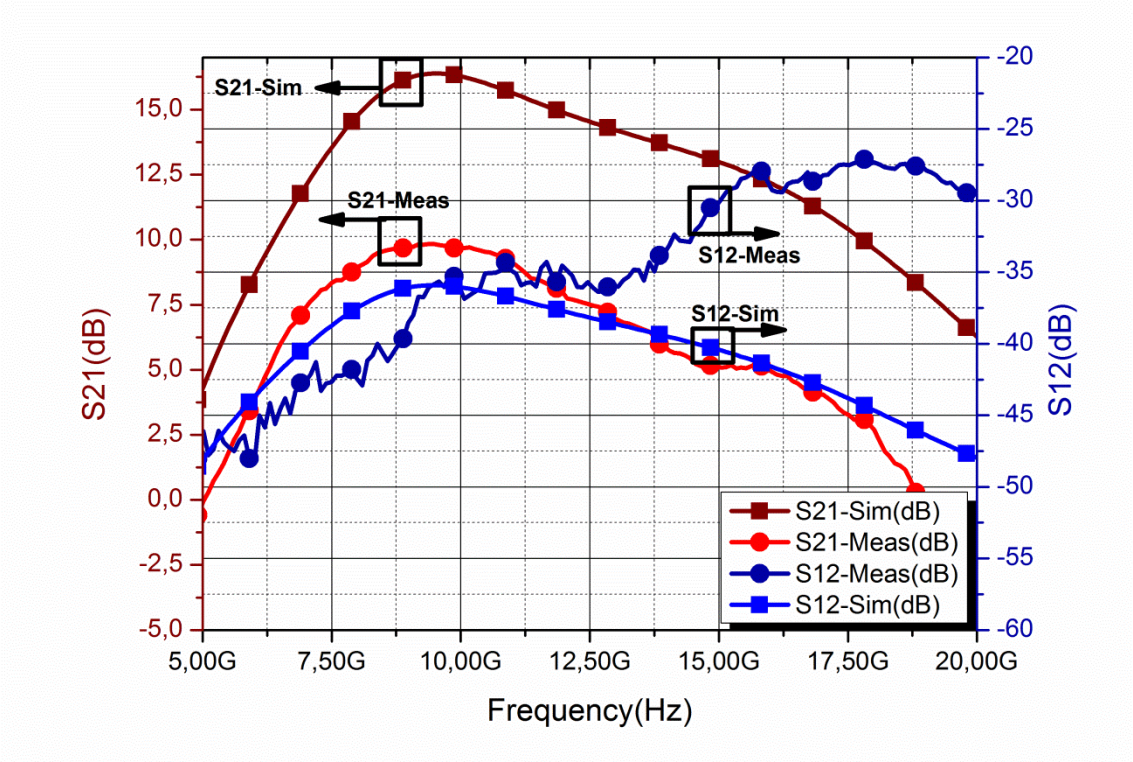


Fig. 13. Simulated and measured S21 and S12 parameter of Single-Stage LNA

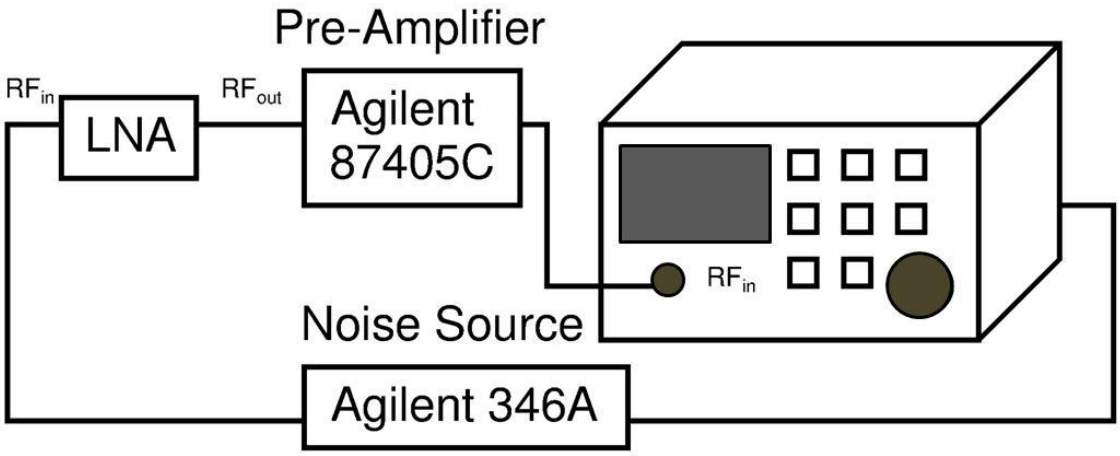


Fig. 14. Noise measurement setup representation for LNA

that occurs due to existence out sources, such as cable losses. Then, obtained NF results are then used for extracting RF probe and cable losses from measured die. Fig.15 demonstrates NF performance of measured dies with using described procedure. NF is lower than 1.9dB at 9GHz, while it is lower than 1.2dB in simulations. High NF can be explained with unmatched input impedance, and low gain performance.

For measurement of P1dB, Agilent E8267D vector signal generator is used, where Agilent E4417A power meter is used for measuring output power. Fig.16 represents P1dB measurement results, while it is simulated as -3.87dBm. In compared with simulation results, higher input-P1dB performance is expected due to having low gain performance. On the other hand high-input P1dB is measured, while consuming 12.5mW.

One of the main reasons of having a low collector current is, having an parasitic resistance that is series connected to the emitter terminal; as a result of the mentioned resistance, β_{DC} is lowered. During the procedure, test-chips are also measured, which includes different sized HBTs; DC measurements demonstrate same low collector current value phenomena. When results of single-stage LNA and test-chips are compared, it is founded that β_{DC} value is low with a similar ratio. On the other hand, when a series resistance is connected to emitter terminal in simulations, much correlated results between simulation and measurements are obtained in terms of collector current, input matching, and gain. Correlated measurement and simulation results can be seen from Fig.17.

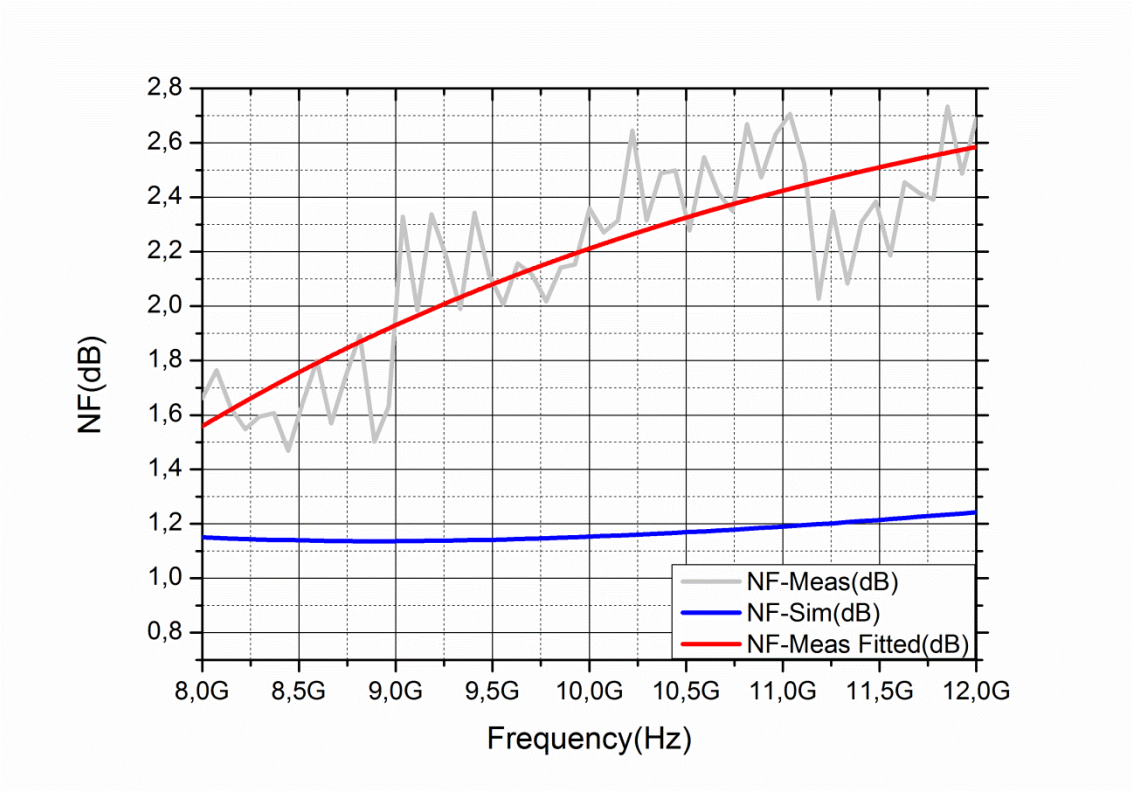


Fig. 15. Simulated and measured NF performance

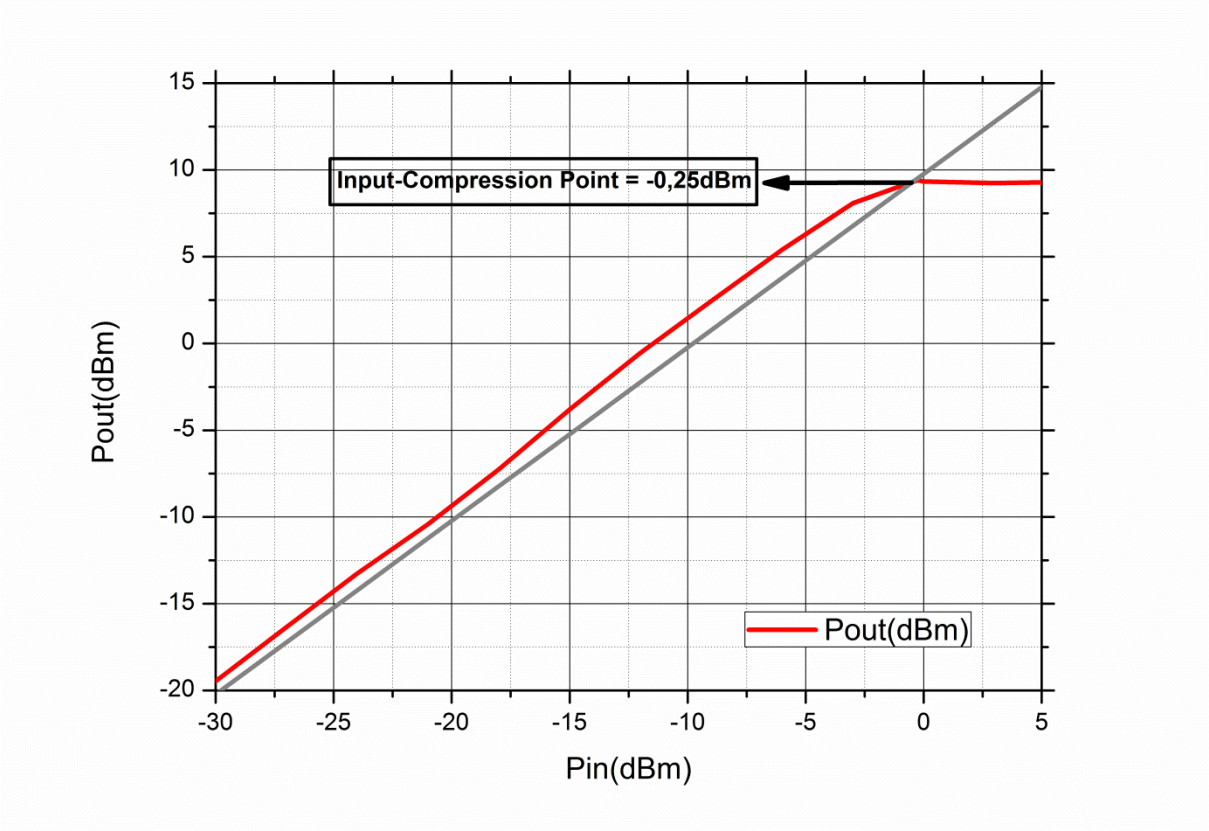


Fig. 16. Measured input-referred compression point of Single-Stage cascode LNA

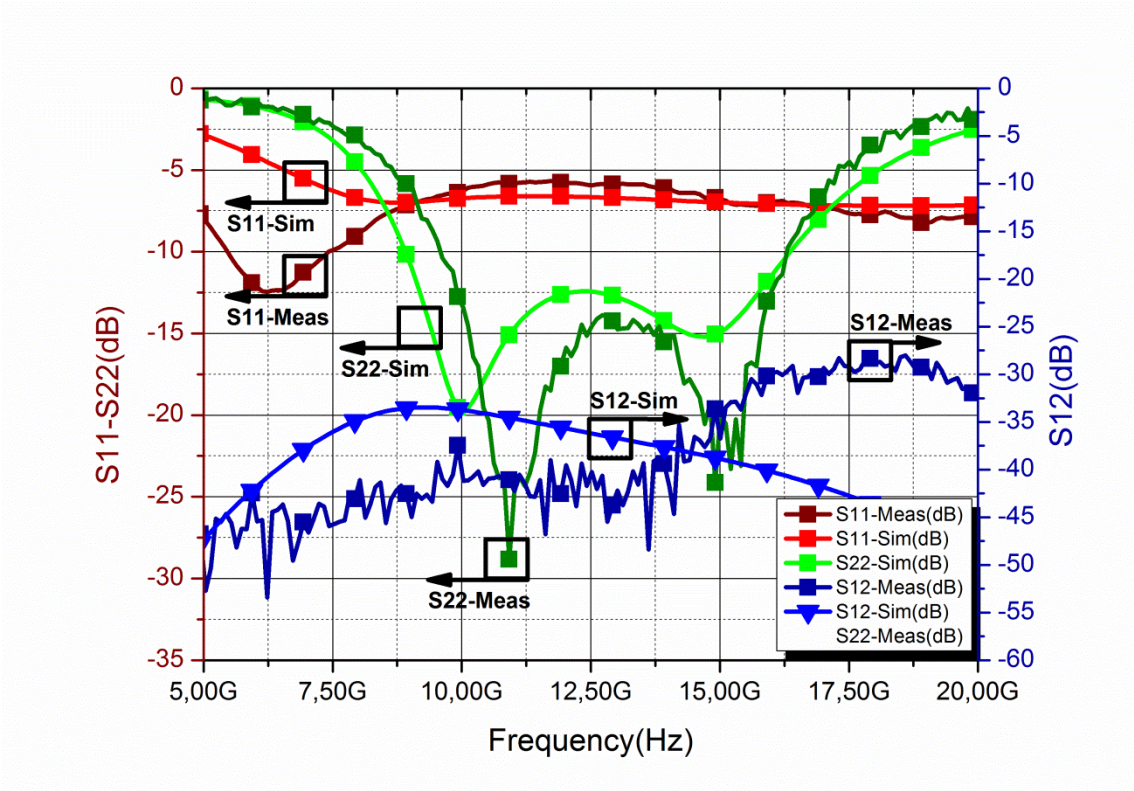


Fig. 17. Correlated measurement and simulation results for Single-Stage cascode LNA

2.4. Telescopic LNA

2.4.1. Description of Topology

When receiver chain of the T/R Module is analyzed, it can be seen that LNA mainly determines the receiver chain gain, as mentioned before. 16.5dB simulated gain can cause problems for the receiver chain, due to losses of other blocks. As a result a new LNA with similar performance metrics and higher gain performance should be targeted.

Main limiting factor for obtaining defined performance parameters is linearity. One of the main conditions of obtaining better linearity is CE breakdown voltage of the transistors, which is related with output voltage swing, as mentioned. On the other hand, as f_T gets higher, breakdown voltages of the transistors decrease, and this ends up with lower breakdown voltages for 0.13µm SiGe BiCMOS technology.

Designing two-stage cascode amplifier can be seen as an option for high dynamic range LNA, but for high linearity in two-stage designs, second stage must be much more linear than total LNA structure itself. As a result two-stage amplifier design is not

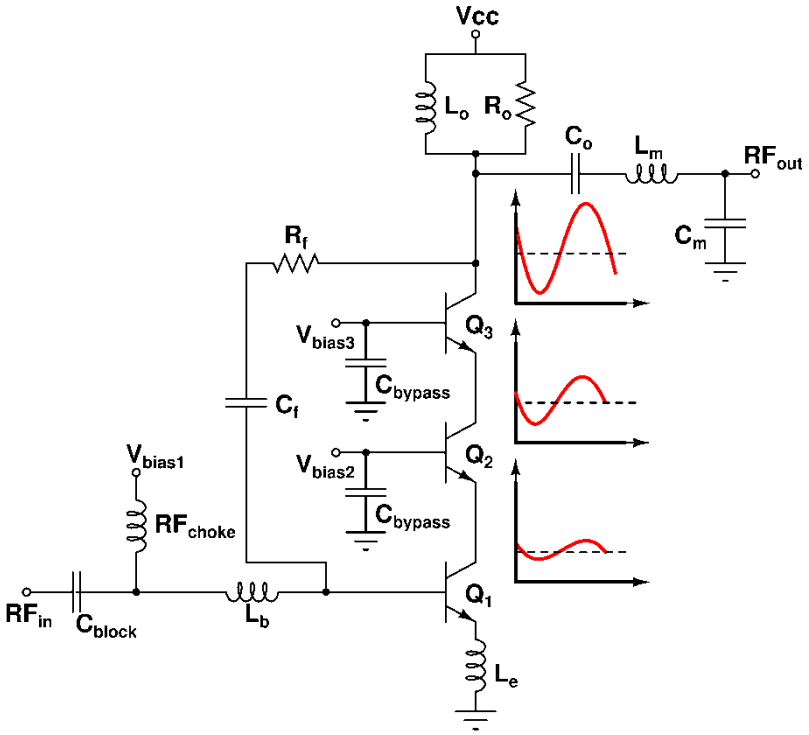


Fig. 18. Schematic view of preferred telescopic LNA

concerned for the selected technology, due to containing only HP transistors. So, an improvement in design methodology had to be applied, to achieve high gain and linearity with low NF at the same time.

Telescopic LNA design is one topology that achieves high gain with high linearity and low NF at single stage. The idea is based on increasing gain step-by-step without causing any distortion during amplification. This is achieved with introducing an additional load transistor on top of cascode architecture, which can be seen on Fig.18. CE breakdown voltage does not change for each transistor, but voltage levels are shifted up with using telescopic LNA; thus voltage swing is not restricted with the CE breakdown voltage limit.

Designing procedure of telescopic LNA is similar to the single-stage LNA, due to being cascode topology dominated. As in single-stage LNA, design starts with current density selection. For telescopic LNA design, the priority is on linearity and gain. As a result of achieving a low NF in single-stage LNA, NF performance can be sacrificed for telescopic LNA, which means that current bias is chosen with regarding two concerns; high gain, high voltage swing. Current swing is also significant for linearity performance; as a result, transistor sizes are selected as large as possible to provide high

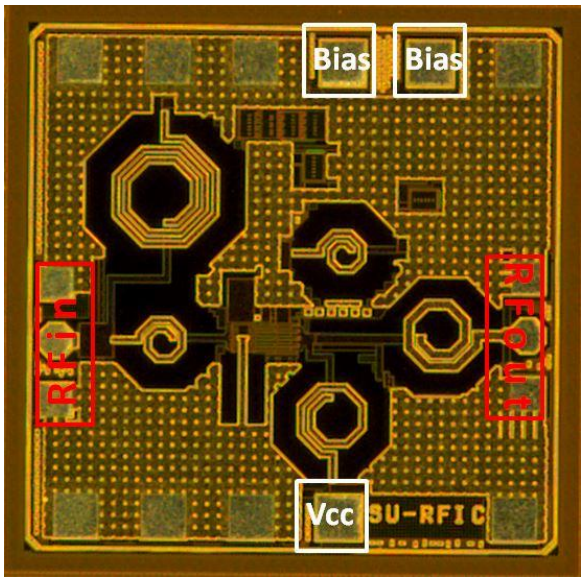


Fig. 19. Die image of Telescopic LNA

current to the design. Telescopic design utilizes one CE breakdown voltage level higher supply, due to additional load transistor, in compared with single-stage LNA. When current level is increased with both raising base voltage and using larger transistor sizes, the design suffers from high power consumption. So power consumption performance is sacrificed for high gain and high input-P1dB.

Simultaneous input and noise match is the next step which is done in a similar method with previously mentioned calculation steps. Base voltage for load transistors are selected with regarding maximum voltage swing, while LC network with shunt R_L resistance is selected as output matching network. Additional series inductor and shunt capacitance is used for better output return loss performance.

For increasing the bandwidth of the output matching network, a RC-feedback mechanism is preferred to be used as in single-stage LNA. Actually, introducing a RC-feedback has disadvantages, due to reducing the stability factor of the design. In high dynamic range amplifiers, some stability problems can be observed due to obtaining high output power. Power Amplifiers (PA) experiences this problem as oscillation that starts at a certain frequency. Telescopic LNA aims high dynamic range with high gain level, which results with high output power. However, feedback mechanism decreases the reverse isolation performance of the design, and increase the chance of oscillations. Due to not observing any oscillation behavior and obtaining adequate reverse isolation

performance, feedback mechanism is preferred for telescopic LNA, to improve the bandwidth performance.

For biasing purpose, previously mentioned active bias networks are used; bias network at Fig.10 (a) is used for driver transistor, while load transistors Q3 and Q2 utilize Fig.10 (b) for bias network. Due to introducing high current to the cascode structure, voltage swing at base terminal of load transistor Q3 is large, which causes a non-linearity at bias networks if a resistance is used for RF_{choke}. To prevent non-linearity, inductor is used for RF_{choke} component, as in single-stage LNA.

2.4.2. Measurement and Simulation Results

Telescopic LNA has 860 x 860 μm^2 = 0.741mm^2 area, including pads. Top view of die can be seen from Fig.19. As in single-stage LNA, spiral inductors are custom designed for high quality factor, where transmission line inductor is used as emitter degeneration inductor, due to requiring small inductance value. The measurement setup for telescopic LNA is identical with measurement setup for single-stage LNA. Represented results demonstrate mean outcome of different samples that are measured.

When DC measurements are done for telescopic LNA, similar low collector current behavior is observed with single-stage LNA; telescopic LNA is designed for 47mA of collector current under 4.7V of supply voltage, while it is measured as about 18mA. Low level of collector current can have significant consequences for design, as described in previously designed LNA, such as degraded input return loss performance. To have same collector current density as in simulation, supply voltage raised up to 5.6V from 4.7V, which changes the bias voltage points dramatically. On the other hand, supplying die with high voltage can result with failure of transistors, due to exceeding their CE breakdown voltage limitations.

Return loss performances of telescopic LNA are represented in Fig.20. In compared with simulation results, there exists a significant frequency shift for return loss performances. Instead of having a wideband input matching, there exists a sharp decay after 6.25GHz. As mentioned, low current density can cause depart from due to designing input matching with regarding input bias conditions. Shifted behavior of output return loss can be reflection of input matching performance to output network, because of having a feedback network.

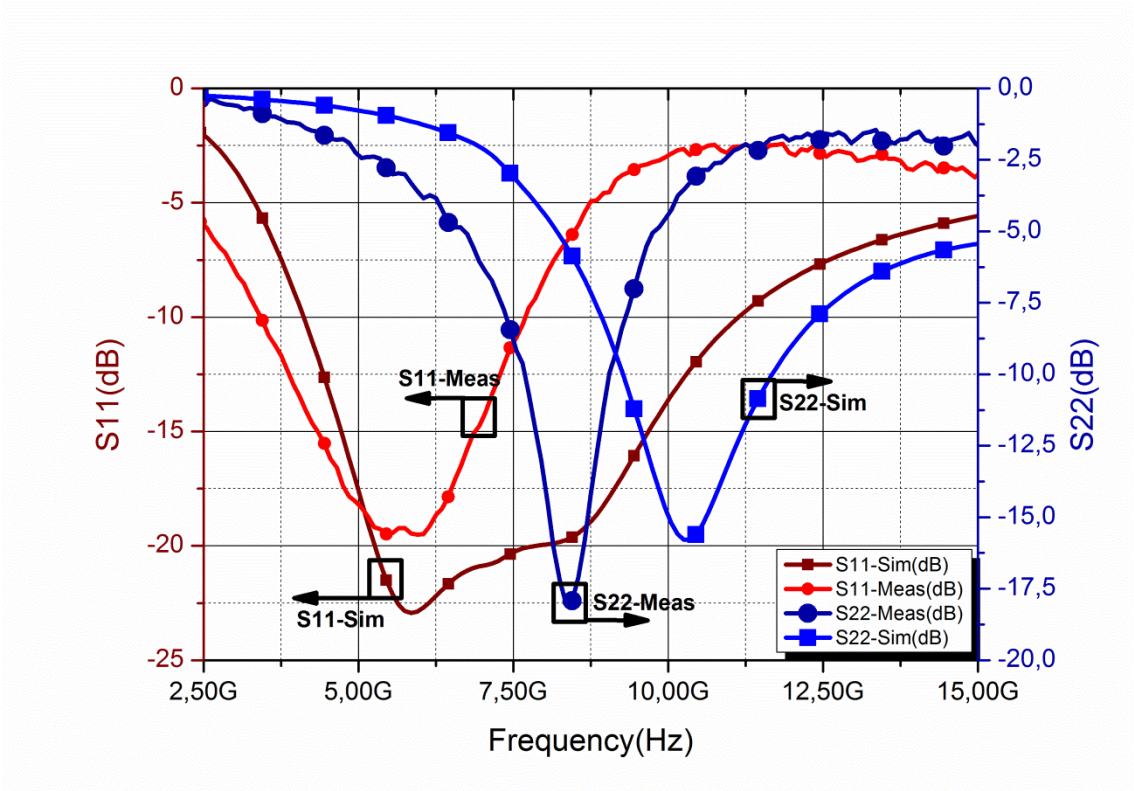


Fig. 20. Simulated and measured return loss of Telescopic LNA

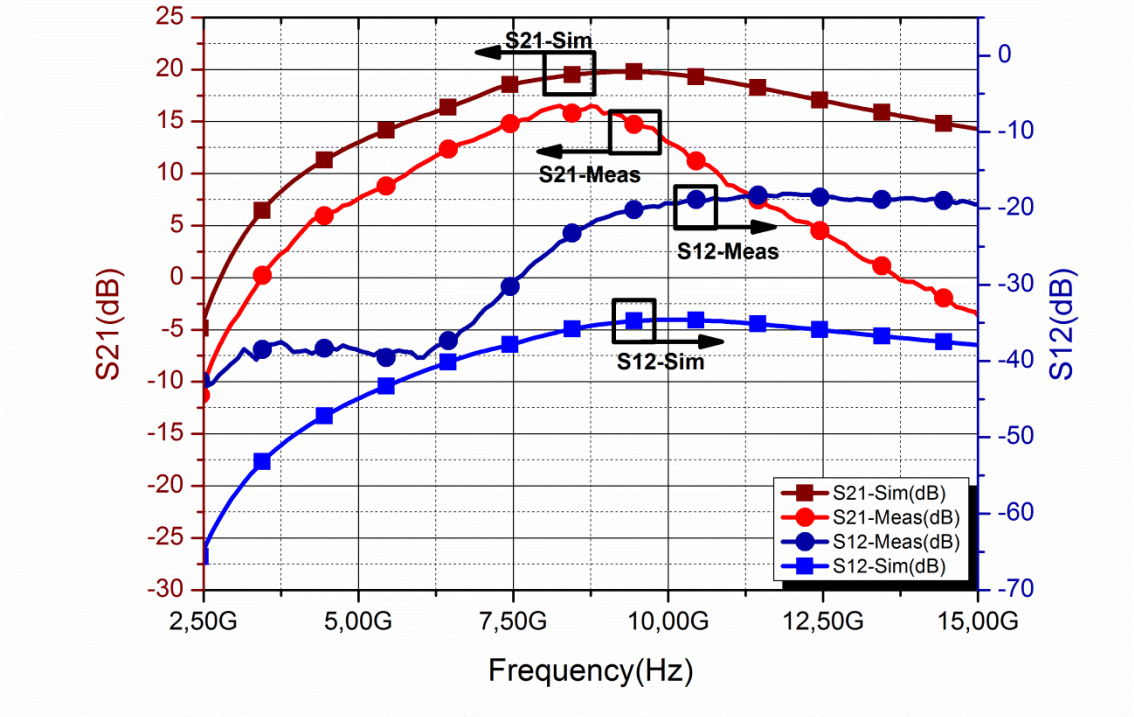


Fig. 21. Simulated and measured S21 and S12 parameters of Telescopic LNA

One of the possible reasons of having such a failure in return loss performances can be low reverse isolation, as can be seen from Fig.21. S12 is measured as -20dB, at 10GHz, while at least -34dB expected. When measurement results of S12 is analyzed, a major deviation is observed after 6GHz, which might be a possible reason for having a shifted return loss performance. Having such low isolation performance causes many other problems for telescopic design; due to having low return loss performance while having high gain at 10GHz, telescopic LNA is on the edge of oscillation. At most 18.3dB of gain is measured at 8.4GHz, while it is 16.5dB in average, as can be seen from Fig.21.

When S-Parameter results are analyzed, there exist a center frequency shift to lower frequencies; as a result center frequency is re-selected as 7.5GHz, due to having better performance in terms of return loss, isolation and gain metrics for next measurement steps.

Measured and simulated NF performance of the design can be seen from Fig.22. NF performance is close to simulation results at lower frequencies, due having best input return loss performances around 6GHz. NF starts to increase because of degradation of input return loss and isolation as frequency gets higher. NF is lower than 2dB at 7.5GHz.

Input compression point is performing better due to having lower gain at specified frequency. As can be seen from Fig.23, input-P1dB is measured about 2.5dBm. In simulations, input-referred P1dB is obtained as -0.6dBm at 7.5GHz, which means that measured and simulated output-referred P1dB is matched.

2.5. Two-Stage Cascode LNA

2.5.1. Circuit Design and Analysis

Dividing the expectations of a single-stage amplifier, into two separate stages can be seen as a good alternative to achieve high linearity, high gain, low NF, and low power consumption at the same time. With that methodology, a single stage does not aim all performance metrics, but achieve much better performance for a specific parameter. Before explaining the designing procedure for two-stage amplifier, performance specifications for each stage should be defined clearly.

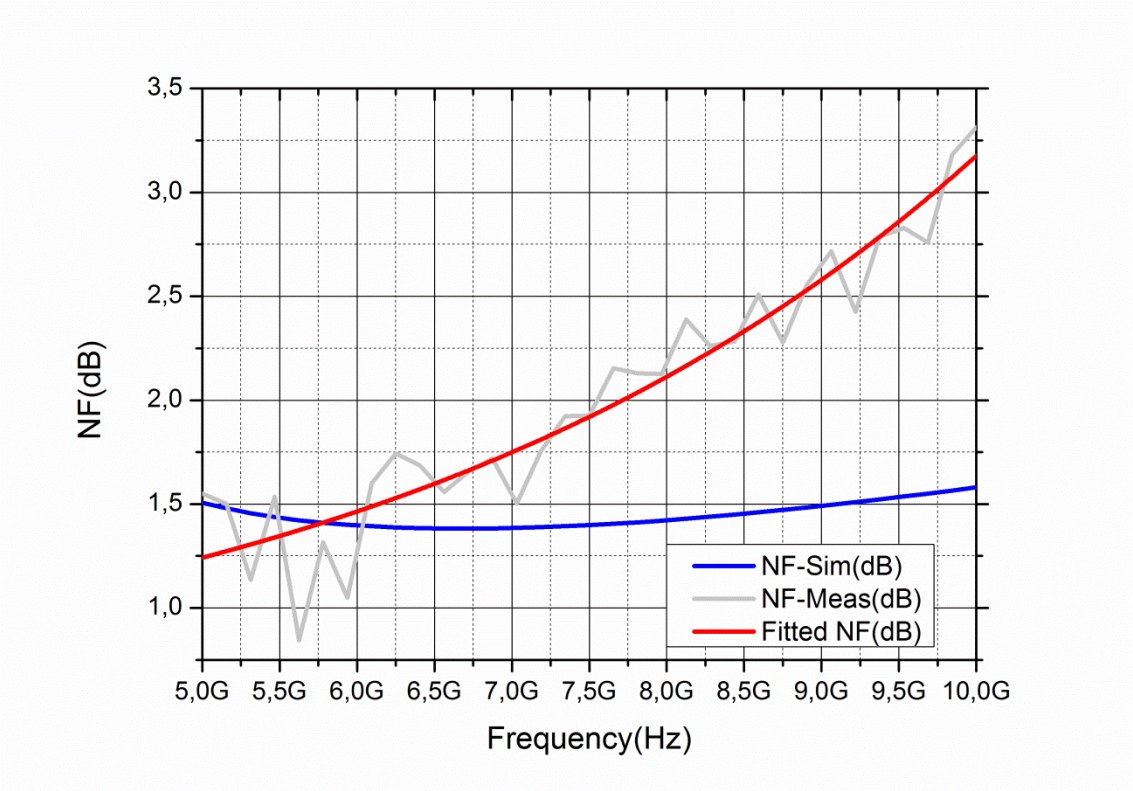


Fig. 22. Simulated and measured NF of Telescopic LNA

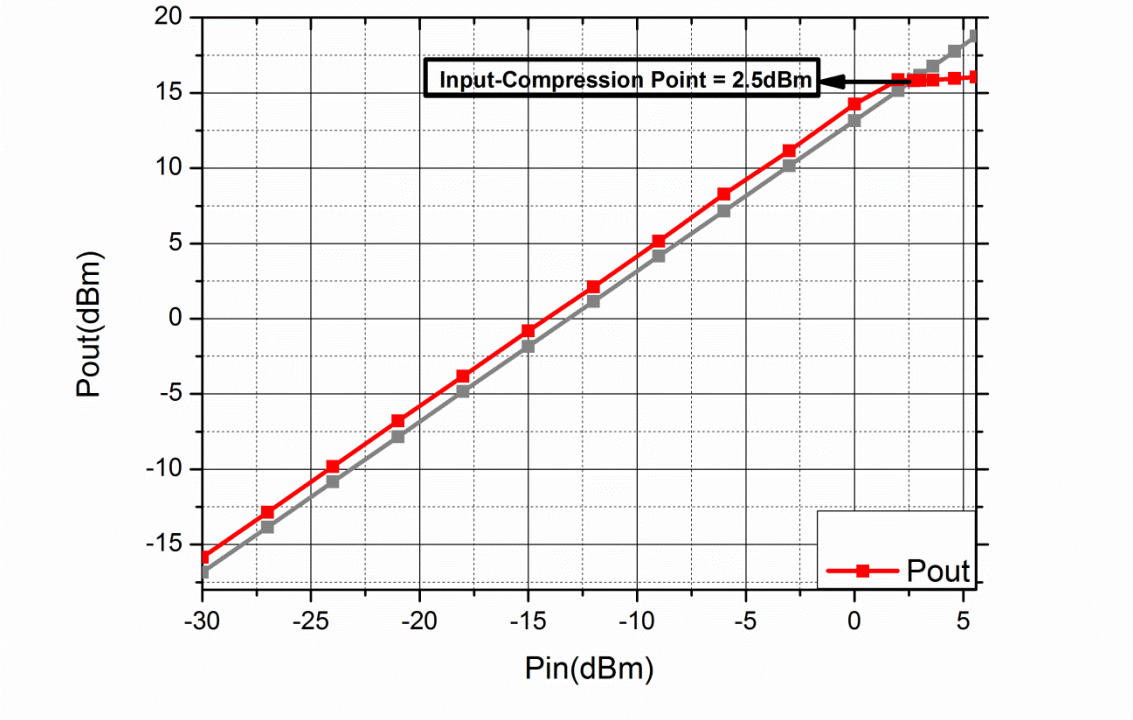


Fig. 23. Measured input-P1dB of Telescopic LNA

As mentioned, high-input P1dB is the main concern for all three different LNA structures. Output-P1dB of cascaded stages can be founded by equation below;

$$p1dB_{TOTAL} = \frac{1}{\frac{1}{p1dB_{N-1} * g_N} + \frac{1}{p1dB_N}} \quad (14)$$

where $p1dB_N$ is output-P1dB in Watts, and g_N is in linear form. When total gain of the design is subtracted from output-P1dB, input referred P1dB can be founded. As can be seen from equation (14), linearity of the incoming stages should be much higher than first stage, to obtain a P1dB that is closer to first stage. In other words, second stage should aim much higher linearity than the exact performance specification.

For input-P1dB at least -4dBm is required. When specifications for each stage are extracted, it is observed that about 10dBm of input-P1dB should be aimed for second stage of LNA. One of the main reasons that previous LNA designs are single-stage dominated are having only HP transistors that have low CE breakdown voltage. It would not be possible to achieve 10dBm of input-P1dB with using only HP transistors. IBM's 0.13µm SiGe BiCMOS technology gives the chance of using HB transistors that have 3.4V of CE breakdown voltage. Even with using HB transistors, aiming mentioned linearity level with low power consumption is a major concern of the design.

Total gain of two-stage architecture is one of the least significant concerns of the topology; design includes two separate amplifying stages, as a result high gain can be obtained with moderate and low level of gains. In total, design will have high gain due to cascading two blocks of amplifiers.

NF performance is one of the parameters that should be considered more for two-stage design, in compared with previous design approaches. Total topology includes two stages, as a result Friis equation (7) should be considered during the designing process. Due to high linearity requirement in second stage, NF performance can be degraded, which will not be a serious problem for the LNA, due to introducing moderate level of gain from first stage. In other meaning, high NF of second stage is suppressed with moderate gain of first stage.

When all of the concerns are considered, the functionality of each block is obvious; first stage should provide low NF with at least moderate gain, while second stage should perform high linearity with as high gain as possible. Regarding each

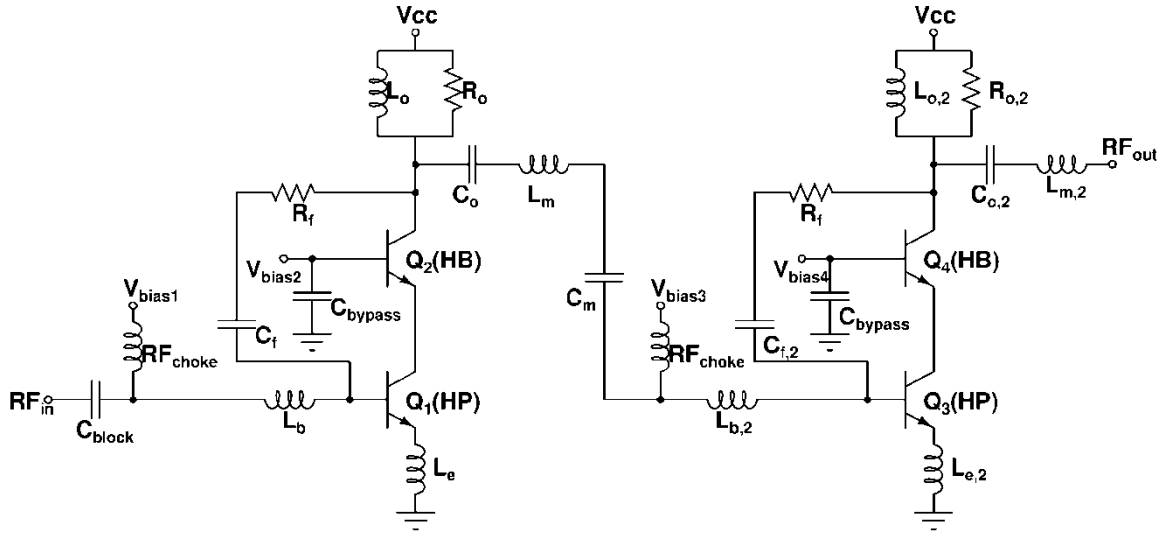


Fig. 24. Two-Stage Cascode Low Noise Amplifier Design

performance criteria, two-stage LNA is constructed as in Fig.24.

Designing procedure of the first stage is very similar to single-stage design, except performance specifications such as linearity and gain performance. Instead of using only HP transistors, HP and HB transistors are combined to form cascode topology for first stage. When HB devices are used for load transistors, output swing range can be improved with increased supply voltage. With using the mentioned methodology 6dBm better linearity performance is achieved, for the first stage. Remaining designing process is same with single-stage LNA design.

For design of second stage, design procedure is different than previous stage, due to having different performance specifications. NF performance is not as significant as previous stage, while high linearity and optimum power match is the main concern. Targeted linearity level for second stage is pushing the limits of the technology. High output power can be obtained with increasing current level, but it is not feasible to construct a LNA, which consume power as much as a PA. As a result a new methodology had to be applied, to reach high linearity with low power consumption.

When required level of performance parameters is achieved for each block, separate stages are cascaded to each other to form two-stage amplifier. As in previous LNA designs, described active bias networks are used with RF_{choke} inductors that are connected for bias of two driver transistors, and load transistor Q4.

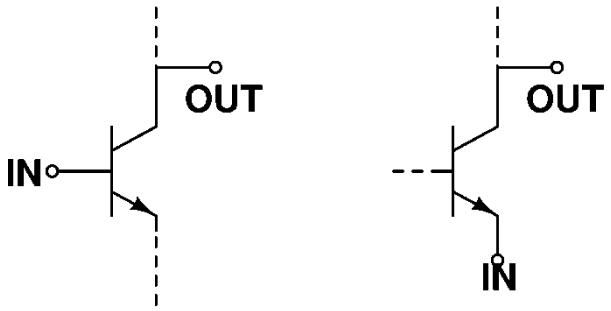


Fig. 25. Representation of Common-Base and Common-Emitter amplifiers

2.5.2. Achieving High Linearity with SiGe HBT Transistors

Output power is not only a significant concern for LNA and PA, but also a milestone for SiGe HBT BiCMOS technology too. The aim of this technology is to achieve similar device performance levels with III-V devices. Even if SiGe BiCMOS can reach up to terahertz level of cut-off frequency, there exists a significant gap in breakdown voltage limitations, which ends up with a reduction in output power. On the other hand, as cut-off frequency and maximum oscillation frequency of SiGe HBT device increase, breakdown voltage decreases [20]. As a result a new question rise up; will SiGe HBT BiCMOS devices be able to achieve similar output power performance with III-V devices?

It seems like in near future, having SiGe HBT devices that has high breakdown voltages and high cut-off frequency as III-V devices, is not possible. Interesting point is, with using some design methodologies higher breakdown levels can be obtained. This section focuses on two methodologies that can be used to improve linearity of SiGe HBT based designs.

Usual device breakdown voltages are defined from collector to emitter, but the breakdown voltage limitation can vary due to the variation between different amplifier types, which can be seen from Fig.25. CE amplifier is driven by constant DC bias current, and due to having output signal at collector terminal, limiting breakdown voltage can be told as CE breakdown voltage, while the case is different for CB amplifier. Emitter current is the limiting factor for CB amplifier, while base terminal is not fixed as CE amplifier, which causes a significant difference between amplifiers. In

CE amplifiers breakdown mechanism depends on high minority carrier injection into base terminal with fixed base current, while in CB amplifiers high hole current density, which results with impact ionization, is free to exit from base terminal; as a result CB amplifiers can perform better breakdown performance [21]. This result prompts a significant consequence; cascode amplifiers can be biased with higher voltage levels, due to existence of CB amplifier at load transistor.

In simulations, all transistors have same breakdown voltages with disregarding which amplifier type they are. As a result, biasing cascode topology without considering classical breakdown voltage can cause problems in terms of matching. Also new bias region, which CB amplifier starts to work in, is not a stable area; impact ionization is still dominant on breakdown mechanism. Impact ionization in CB amplifier, causes "pinch-in" phenomena in design, which can result with instability in transistor [21]. Even if it is not fully safe to use described voltage level, higher linearity performances can be achieved with appropriate biasing conditions. Actually, mentioned technique is tested during the measurement of telescopic and single-stage LNA designs; transistors are still functional when supply voltage is increased about 1.5V above breakdown voltage limitations, but it should be noted that during high power measurements, such as compression point, even a sudden change in RF signal cause an avalanche effect, which results with device breakdown.

There also exist some questions that can be asked about the transistor parameters, such as "how does the breakdown voltage behavior vary with changing device dimensions?". When emitter length and width of the HBT devices are varied, it is observed that there exists a certain level of dependence between breakdown voltage and emitter scale; it is measured that as emitter length increases in CB amplifiers, breakdown voltage of transistors are lowered. This is a consequence of decreasing resistance between emitter-base terminals, thus debiasing effect is reduced. Therefore as length of the emitter increases, breakdown voltage of device decreases in CB amplifiers. On the other hand, this result demonstrates that, instead of forming a long emitter region, connecting unit sized transistors in parallel to each other will result with better breakdown voltage performance [21]. In other meaning, lateral dimension of the transistor is affecting the breakdown performance of device. It may not be possible to

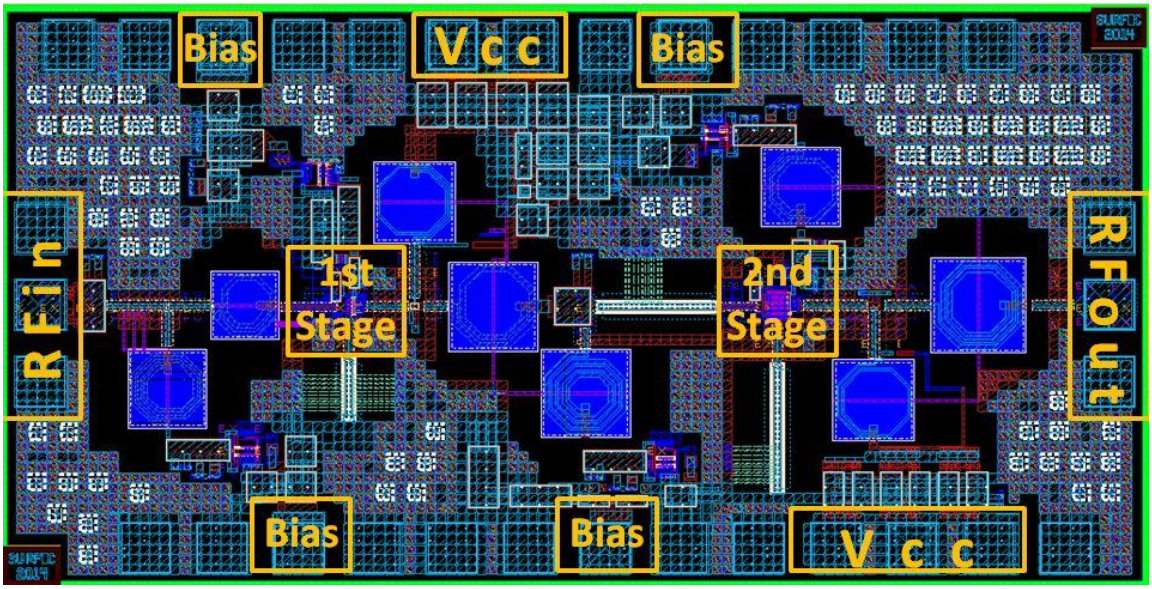


Fig. 26. Layout view of two-stage LNA

observe mentioned consequences in simulation environment, because many foundries do not take lateral instabilities of transistor into account [21].

For two-stage LNA design, size of the transistors are considered differently from single-stage and telescopic LNAs, due to previously mentioned concerns. During the designing procedure, driver transistor Q3 is selected as large as possible, while load transistor Q4 is selected as medium sized, to maximize breakdown voltage for CB transistor. With using the mentioned scaling technique for second stage, 10dBm of input-P1dB performance is achieved while having low power consumption. Layout of the total two-stage cascode LNA can be seen from Fig.26.

2.5.3. Simulation Results

Two-stage cascode topology achieves more than 20dB of gain, as can be seen from Fig.27. With having moderate and low gain performances for first and second stages respectively, high gain levels can be obtained. Designed LNA has about 3GHz of bandwidth, and mean 2dB of NF between 9-11GHz. With the help of mentioned techniques that can enhance output swing limit, two-stage LNA has -3,73dBm of input-

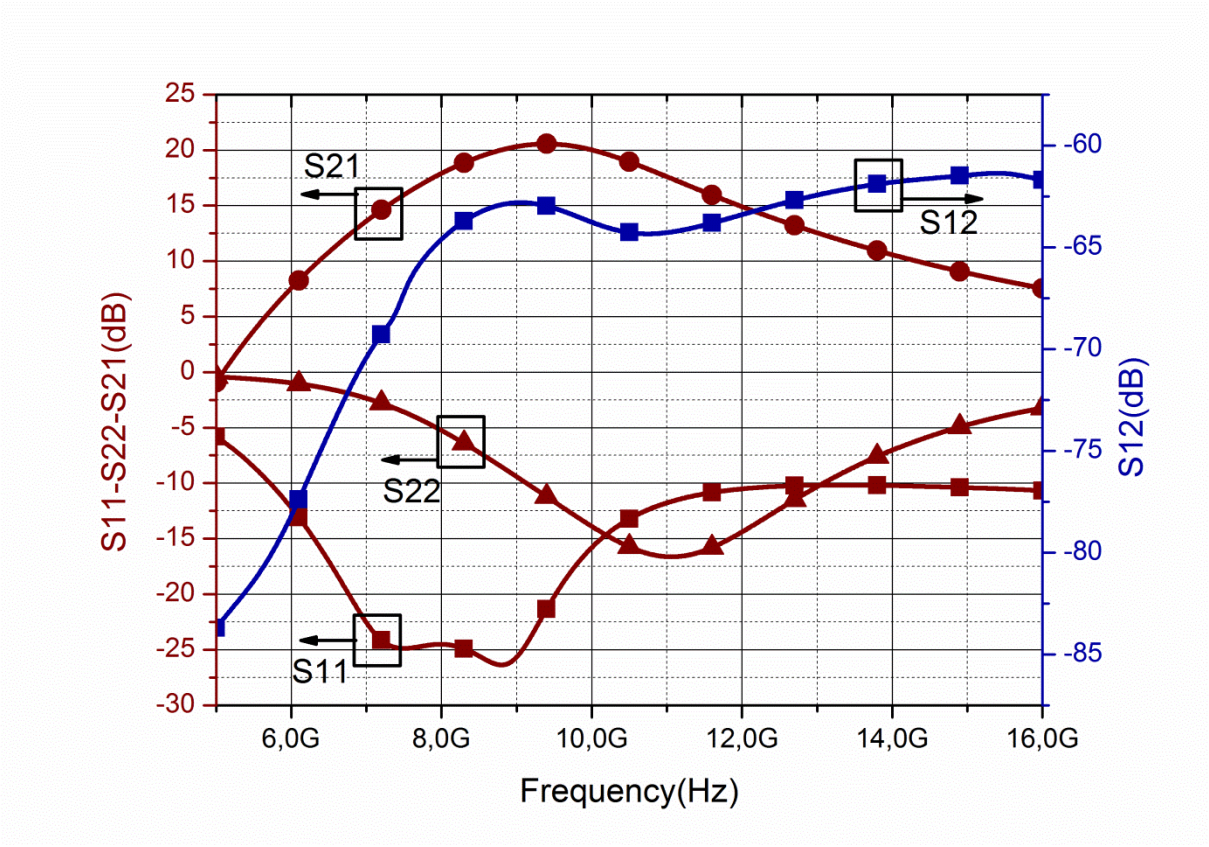


Fig. 27. S-parameter results of two-stage LNA

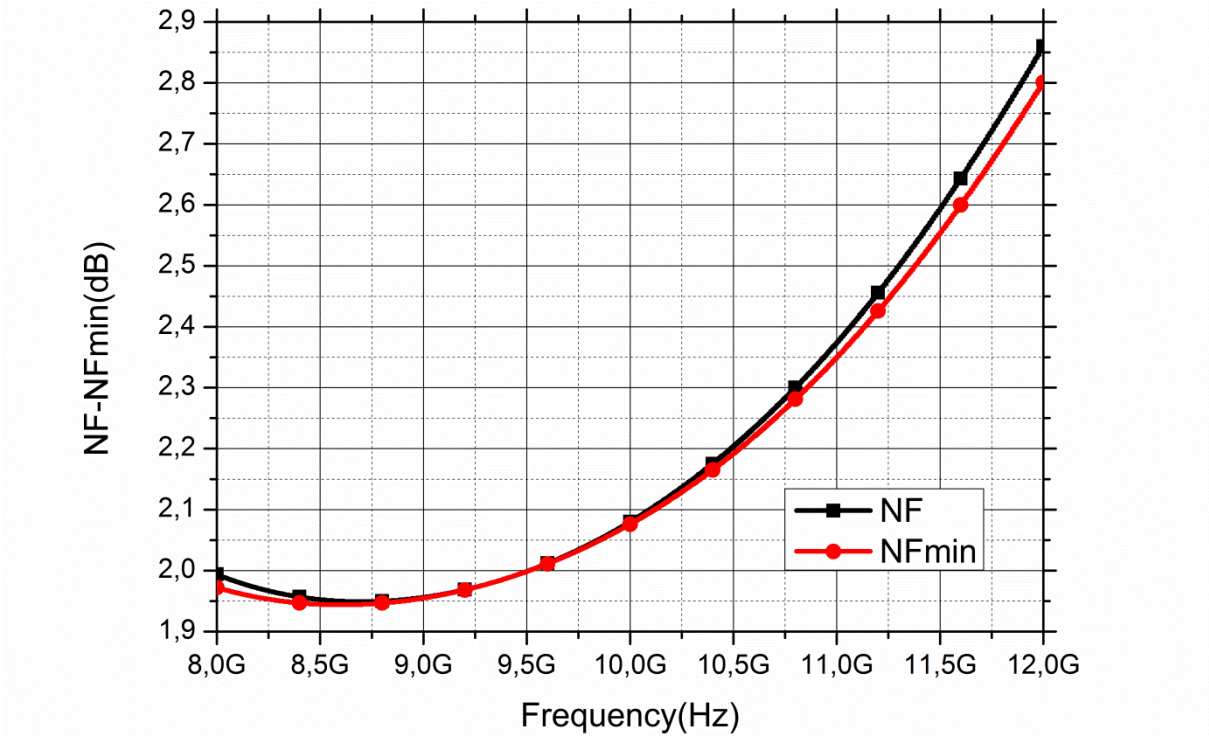


Fig. 28. NF_{min} and NF results for two-stage LNA

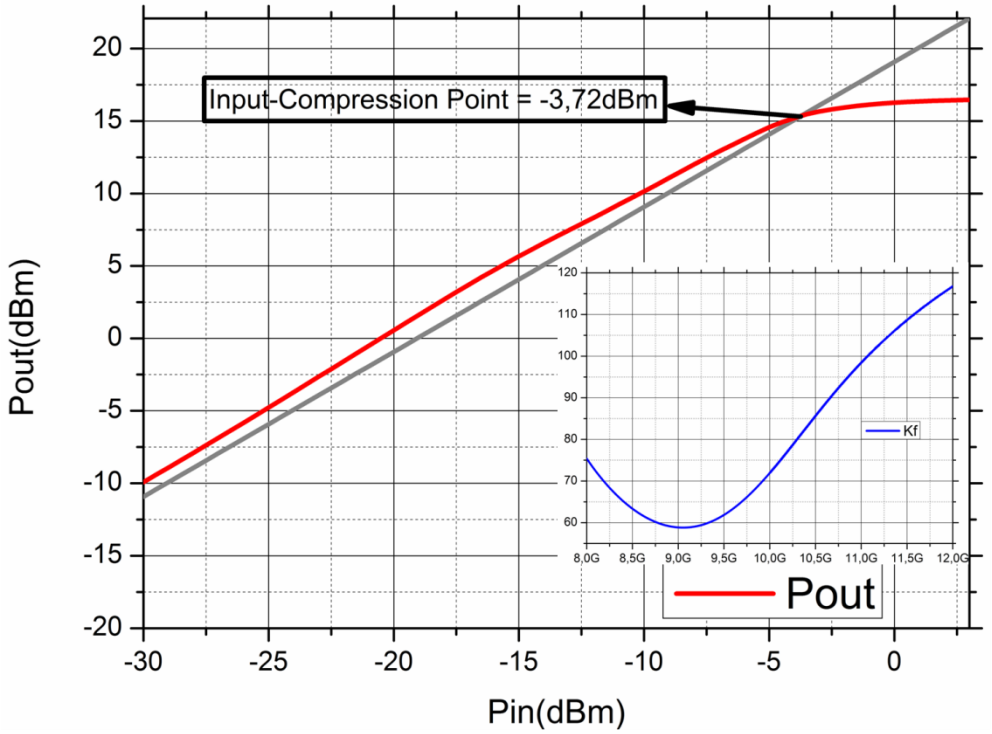


Fig. 29. Input compression point of two-stage LNA

referred compression point, while consuming 115.8mW power as can be seen from Fig.29. During designing procedure, biasing above breakdown voltage technique is not used, but supply voltages will be increased during measurement, to result with better linearity performance.

2.6. Performance Comparison

Table I represents comparison chart of presented three different LNA structures, with similar works that are designed with SiGe HBT BiCMOS technology. Using a Figure-of-Merit (FOM);

$$FOM\left[dBm\right] = -NF\left[dB\right] + IP_{1dB}\left[dBm\right] + G\left[dB\right] + 10\log\left(\frac{IP_{1dB}\left[mW\right]}{P_{DC}\left[mW\right]}\right) + 20\log\left(\frac{f_0\left[GHz\right]}{1GHz}\right) \quad (15)$$

would simplify to make comparison. Described FOM includes input-referred P1dB, instead of output-referred because input signal level is more significant than output signal level for LNA. On the other hand, with introducing output-referred P1dB and gain together will end up with counting gain twice. Also ratio of power consumption to input-P1dB is included, to demonstrate how efficient the designed LNA operates.

Single-stage LNA achieved high dynamic range with low power consumption and low NF, while telescopic LNA reaches highest input-P1dB with similar NF performance. Disadvantage of telescopic LNA is sacrificed power consumption. Two-stage amplifier achieved high dynamic range with low power consumption. Moreover, it achieves more than 20.5dB gain with mean 2dB of NF.

TABLE 1. Performance Comparison with Other Works in the Literature

	Simulation Results for Two-Stage Cascode LNA	**Telescopic LNA**	**Single-Stage LNA**	**[16]**	**[22]**	**[23]**	**[24]**
Technology	0.13µ SiGe HBT BiCMOS	0.13µ SiGe HBT BiCMOS	0.13µ SiGe HBT BiCMOS	0.13µ SiGe HBT BiCMOS	0.13µ SiGe HBT BiCMOS	0.13µ SiGe HBT BiCMOS	180GHz SiGe HBT
Frequency	10GHz	7.5GHz	9GHz	10GHz	10GHz	9.5GHz	9.5GHz
Noise Figure	2dB	1.92dB	1.9dB	1.36dB	1.98dB	2dB	2.78dB
Gain	20.53dB	15dB	10 dB	19.5dB	10dB	30dB	11dB
Input-P1dB	-3.72dBm	2.5dBm	-0.25dBm	-10dBm	-10dBm	-11.5dBm	-19.1dBm
Power Cons.	115.8mW	253.8mW	12.5mW	15mW	2mW	285mW	2,5mW
Chip Area	2.53mm^2	0.741mm^2	0.76mm^2	0.526mm^2	0.436mm^2	1.76 mm^2	0,52 mm^2
FOM	10.46dBm	11.33dBm	15.71dBm	6.38dBm	5.01dBm	-0.047dBm	-14,5dBm

3. WIDEBAND PHASE SHIFTER WITH HIGH PHASE RESOLUTION FOR X-BAND SiGe T/R MODULE

Phase shifter is used to change the phase of incoming signal, which enables the beam shift to certain directions. As a result of this functionality, phase shifter is one of the most essential blocks of T/R Module.

This section will introduce the constructed phase shifter, which can cover whole X-Band frequency with high phase resolution that can generate at least 6-bit of operation. Section starts with the phase shifter fundamentals, and basic phase shifter parameters, and then continues with different phase shifter topologies, and hybrid phase shifter topology. After describing the blocks of the used hybrid topology, the chapter ends with simulation results and comparison with similar works.

3.1. Phase Shifter Fundamentals

Phase shifter is basically a block that has the functionality to vary phase of incoming signal from 0^0 to 360^0, while magnitude of signal does not change in ideal case. Phase shifters can be categorized into two different groups; analog and digital phase shifters. Analog phase shifters can provide all phases continuously in defined phase region with the help of the control voltages, or variable components. Instead of defining all phases in continues manner, digital phase shifters provide phase steps, which are named as bit. For the digital phase shifters, number of steps or number of phase states are defined with regarding the number of bits.

For an N-bit phase shifter, there exist 2^N different phase states. For instance, there exist 64 different phase states for a 6-bit phase shifter. The step size, also named as Least Significant Bit (LSB), is calculated with the division of 360^0 to the number of

different phase states. For a 6-bit phase shifter, the LSB is 5.625^0 ($360^0/2^6$), while it is 2.8125^0 for 5-bit phase shifter.

The phase shifters can also be categorized with respect to their way of constructing phases; active and passive phase shifters. Both phase shifter types have advantages and disadvantages, for instance active phase shifters can provide gain due to including active devices, while passive phase shifters has too much loss due to constructing phase difference with the help of passive structures, which degrades the whole gain and noise figure performance of T/R Module. On the other hand, in compared with the active ones, passive phase shifters consume more area, which is another significant disadvantage. One of the most significant disadvantages of the active phase shifters is their linearity performance; due to being designed with using active devices, active phase shifters lacks from linearity performance, even they consume power. Therefore linearity of the active phase shifter can be seen as one of the main limitation to construct a high dynamic range T/R Module. Reciprocal behavior of the passive phase shifters can be seen as one advantage, because constructing bidirectional active phase shifter will harden the designing procedure, and integration with other blocks.

3.2. Basic Performance Parameters

The main purpose of the phase shifter is to create a determined level of phase difference between states; as a result the most significant specification of a phase shifter is its phase error. Some phase states will be lost, if the phase error is higher than a certain level, which changes with regarding the number of bits. Calculating Root Mean Square (RMS) Phase Error as in equation (16)

$$RMS-Phase\ \ Error(f)=\sqrt{\frac{\sum_{n=1}^{N}\left(\Delta\phi_n(f)\right)^2}{N}} \tag{16}$$

is one of the ways to understand the phase performance of the design. RMS phase error of a phase shifter should be lower than half of LSB, to construct all phase states correctly. When RMS error is lower than LSB, the phase shifter starts to lose some states, but it is still functional; in physical meaning, some states of the phase shifter

collide with one and another, so number of effective states starts to decrease. The critical limit for the phase shifter is LSB; if RMS error is higher than LSB, then phase shifter starts to lose one remaining bit. For instance 6-bit phase shifter lose one bit of operation, if RMS phase error is about 5.8^0, due to being higher than the LSB.

Similar to the phase error, gain error is another parameter for phase shifters. Ideal phase shifters should only have an influence on phase of the incoming signal, but the gain of the block also varies with frequency. RMS gain error equation (17) is used to understand

$$RMS-Gain \quad Error(f)=\sqrt{\frac{\sum_{n=1}^{N}\left(\Delta G_n(f)\right)^2}{N}} \tag{17}$$

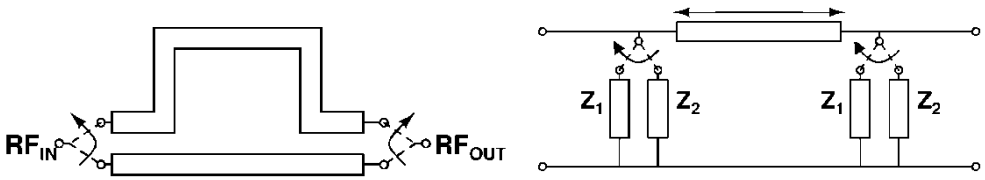
the variation of gain with changing frequency. RMS gain error is not directly affecting the phase shifter performance, but it affects the system gain; due to have a varying gain between different phase states, system level performance can degrade.

3.3. Phase Shifter Topologies

There exist different types of phase shifting mechanisms with respect to their way of generating phase difference. In this section, five different types of mechanisms will be discussed with reporting their working principles.

3.3.1. Switched Line Phase Shifter

Switched line phase shifter, demonstrated in Fig.30 (a), depends on a basic principle; if signal pass through a different path from original one, there will be a certain phase difference between two different paths. In other meaning with selecting different paths, a time delay is introduced to the signal itself. Due to working with time-delay principle, switched line phase shifter is appropriate for wideband applications. [34]. Drawback of this topology is the loss performance that varies according to selected paths, which will end up with high RMS gain error. Also, there should be a switching mechanism to select one of the paths, which will increase the loss. On the other hand, switched line phase shifter will consume more area, due to requiring separate signal paths for different phase states.



(a) (b)

Fig. 30. Representation of a) Switched Line and b) Load Line Phase Shifters

3.3.2. Load Line Phase Shifter

Different than switched line, load line phase shifter has only one signal path, as can be seen Fig.30 (b). The phase difference is created with utilizing the switches that are located at the loads; to change the phase of the mechanism, the circuit switches to other load. The load line phase shifter can be seen as a good alternative when compared with switched line design, but there exists a significant problem that waits to be solved; the return loss will vary with different phase states. While load lines are switched to obtain certain level of phase difference, input matching starts to vary due to changing the load impedance. As a result, return loss performance of the load line phase shifter is poor in compared with other phase shifter types [34]. On the other hand, succeeding blocks will be affected from the return loss of the load line phase shifter, due to having various return loss performances at different phase states, which can be named as loading-effect.

3.3.3. Filter Type Phase Shifter

Filter Type Phase Shifter depends on selection of a path, as in switched line phase shifter. Different than switched line type, filter type phase shifter generate phases with the help of filters, which can be High-Pass (HP) filter and Low-Pass (LP) filter. There exist mainly two ways of creating phase difference between states with using filter type topology; HP-LP filter type, and Bypass (BP)-LP filter type. In HP-LP filter type as Fig.31 (a), there exist two separate filters which generates two different phases. For filtering mechanism, π-type and T-type networks can be preferred that are constructed with inductors and capacitors. With using two different filter types, the phase has less variation across the frequency due to inversely behavior of both filter types. As a drawback of this mechanism, the design should include many inductors and

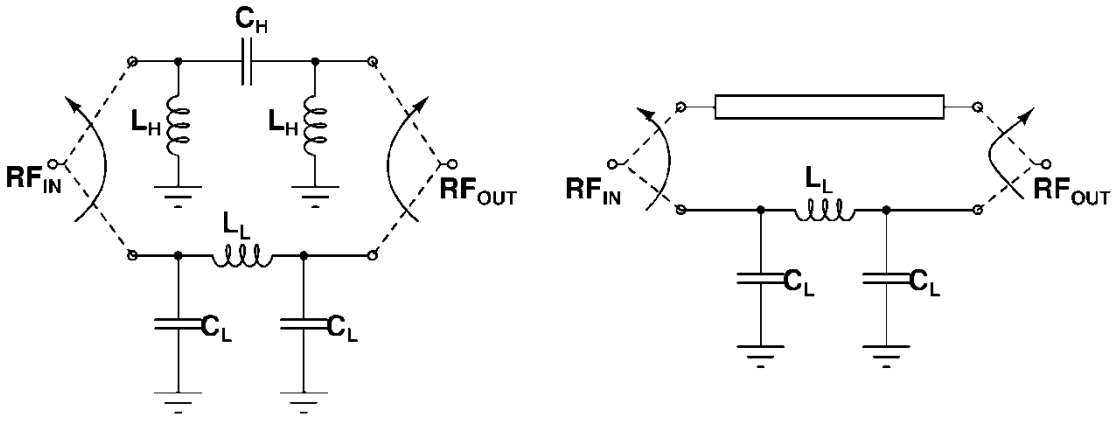


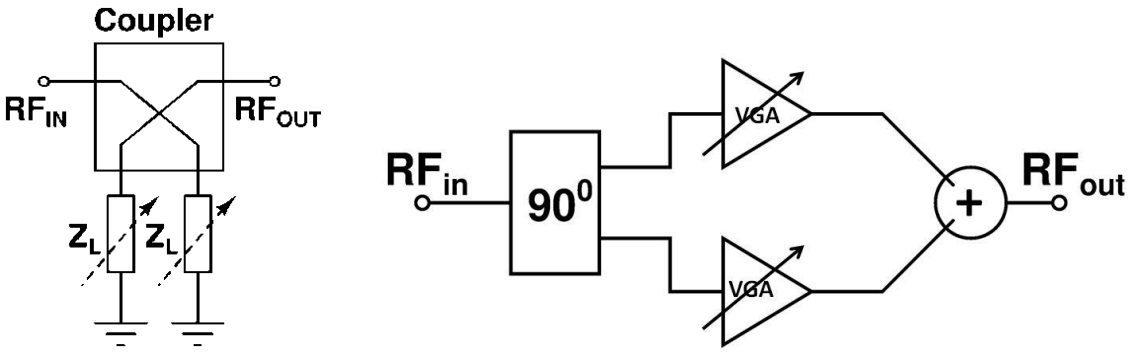
Fig. 31. Representations of a) HP-LP and b) BP-LP phase shifters

capacitors; as a result constructed phase shifter introduces loss to the system. BP-LP type phase shifter can be seen as an alternative of HP-LP type, due to including only a single path, which is used to bypass the filter Fig.31 (b). With BP-LP type, loss that is introduced by one filter is canceled out. In other meaning, BP-LP type phase shifter can be seen as an alternative to HP-LP design that has a better gain performance, while it sacrifices the possible wideband operation of the phase shifter, due to not having HP and LP filters together.

As in the switched line case, a signal line should be selected for filter type phase shifter. Due to adding an additional control mechanism to the phase shifter, the design may have more loss. Thus additional to the phase shifter, low loss switches should also be constructed.

3.3.4. Reflection Type Phase Shifter

Even if reflection type phase shifter (RTPS) and load line type phase shifter seem to be similar to each other, there exist fundamental differences. A typical representation of RTPS can be seen Fig.32 (a). As mentioned, load line type phase shifter is a digital phase shifter, due to switching through different phase states. RTPS is using variable components to continuously vary the phase, which means that RTPS is an analog type phase shifter. Due to varying load impedances of the mechanism, the phase steps are limited with the amount of the variation of the loads.



(a) (b)

Fig. 32. Representations of a) RTPS and b) Vector Modulator type phase shifter

One of the drawbacks of the load line phase shifter is surpassed in RTPS mechanism with using hybrid coupler; two ports of the coupler is used for signal input and output, while the remaining two ports are used for the loads. Therefore, ports are isolated through the coupler, which concludes with less varying return loss performance between different phase states. On the other hand, couplers will introduce loss and noise to the system.

3.3.5. Vector Modulator

The common part of the previously mentioned phase shifter types, is being majorly designed with passive components. Phase shifters designed with vector modulator technique, are active device dominated, instead of passive components; vector modulator utilize Variable Gain Amplifier (VGA), to vary the phase with the help of amplitude. A block level representation of vector modulator can be seen Fig.32 (b).

The working principle of vector modulator technique depends on adding separate output signals that are obtained from different VGAs. As a first step, incoming signal splits into two signals that have equal amplitudes; first one is the In-phase signal, while the second one is the Quadrature of the input signal.

If the input signal is $V_{in} = M\angle 0^0$, then

$$V_I = \frac{M}{\sqrt{2}}\angle 0^0 \quad \text{, and} \quad V_Q = \frac{M}{\sqrt{2}}\angle(-90^0) \tag{18}$$

are outputs of I/Q generator that are in-phase and quadrature phase compared with input signal. If inphase and quadrature phase are introduced to VGAs as described, output signal will be vector summation of VGA outputs, which are multiplication of VGA gain with I/Q generator output. Total output signal is represented in equation (19);

$$V_{out} = (G_1 \angle(-k_1 180^0)(V_1) + (G_2 \angle(-k_2 180^0)(V_Q) \tag{19}$$

where $G_{1,2}$ represent gain for certain path of VGA. As mentioned, VGA gains can be converted to loss to introduce 180^o of phase difference, which will be used to cover all defined degrees; as a result $k_{1,2}$ represent the condition of negative gain, where

$$k_{1,2} = \begin{cases} 0, & if \quad G_{1,2} \geq 0 \\ 1, & if \quad G_{1,2} < 0 \end{cases} \tag{20}$$

Magnitude of output vector signal can be found with simple vector summation with combining (18) and (19);

$$|V_{out}| = \left[\begin{array}{l} \left(|G_1| \sin \angle(-k_1 180^0) + |G_2| \sin \angle(-90^0 - k_2 180^0) \right)^2 \\ + \left(|G_1| \cos \angle(-k_2 180^0) + |G_2| \cos \angle(-90^0 - k_2 180^0) \right)^2 \end{array} \right] \frac{M}{\sqrt{2}} \tag{21}$$

Due to $\sin(180^0) = \cos(90^0) = 0$, equation (21) can be simplified to

$$|V_{out}| = \frac{M}{\sqrt{2}} \left[\left(|G_2| \sin \angle(-90^0 - k_2 180^0) \right)^2 + \left(|G_1| \cos \angle(-k_2 180^0) \right)^2 \right]^{1/2} \tag{22}$$

As a result magnitude of output vector can be calculated as

$$|V_{out}| = \frac{M}{\sqrt{2}} \left(|G_2|^2 + |G_1|^2 \right)^{1/2} \tag{23}$$

where $\sin(90^0) = \cos(180^0) = 1$. Similarly**,** *phase* of output vector can be calculated as

$$\phi = \tan^{-1} \left(\frac{|G_1| \sin \angle(-k_1 180^0) + |G_2| \sin \angle(-90^0 - k_2 180^0)}{|G_1| \cos \angle(-k_1 180^0) + |G_2| \cos \angle(-90^0 - k_2 180^0)} \right) \tag{24}$$

which can be simplified to

$$\phi = \tan^{-1} \left(\frac{|G_2| \sin \angle(-90^0 - k_2 180^0)}{|G_1| \cos \angle(-k_1 180^0)} \right) \tag{25}$$

As can be seen from (25), phase of the output vector is varying with gain and phase of VGA. To understand output phase more clearly, $k_{1,2}$ values should be added to equation (25), with regarding VGA gain;

$$\phi = \begin{cases} \tan^{-1}\left(\frac{|G_2|}{|G_1|}\right) & if \quad G_{1,2} \geq 0 \\ -\tan^{-1}\left(\frac{|G_2|}{|G_1|}\right) & if \quad G_1 \geq 0, G_2 < 0 \\ 180 - \tan^{-1}\left(\frac{|G_2|}{|G_1|}\right) & if \quad G_1 < 0, G_2 \geq 0 \\ 180 + \tan^{-1}\left(\frac{|G_2|}{|G_1|}\right) & if \quad G_{1,2} < 0 \end{cases} \tag{26}$$

Additional 180^0 are for covering all phase conditions that are between 0^0 to 360^0 [34].

As can be understood from the equation (23), one of the most significant benefits of vector modulator technique is introducing certain level of gain to the system, instead of loss, which was the case for other phase shifter types [34].

For the VGA structure, current-steering technique can be seen as a good option, which can be seen from Fig.33. With increasing the number of current-steering transistors, sensitivity of the phase shifter can increase. As a drawback, VGAs should introduce negative gain to cover 0^0 to 360^0 of different phases; as a result RMS gain error can increase due to sharp decay at the gain curve. Moreover, it can also affect the phase performance, because difference between each control voltage state might be small enough, to cause some problems to the Digital-to-Analog Converter (DAC), which controls the current steering mechanism.

Preferring differential input pair can solve this difficulty; with that way there will be two signals which directly have a phase difference of 180^0. An additional block that creates 180^0 of phase difference between two terminals can be used, such as a Balanced-Unbalanced (balun), for applying this solution to single ended systems. Active balun structures can be a good approach to end up with small and compact area, but lacks from linearity performance. Also, passive balun design might be an alternative, which can improve the linearity performance of the vector modulator, with the expense of the increased area.

For the I/Q generation different types of mechanisms exist, such as HP-LP Filters, and All-Pass Filters. The mentioned structures can be constructed with using different types of lumped components. RLC networks can be seen as an option for I/Q generator, but it increases the total area, and it can cause a narrow band operation. RC networks

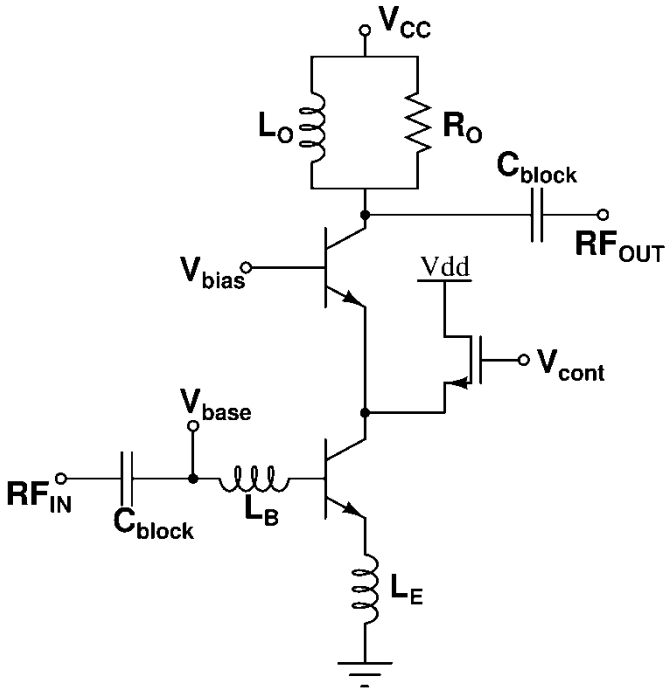


Fig. 33. Representations of VGA with current-steering technique

can also be preferred for I/Q generator, which consumes much smaller area. Selecting high value resistances will achieve wider bandwidth. The drawback of the RC network is introducing more loss than other networks. Also when the resistor value is increased to end up with wide bandwidth, more loss is introduced, which concludes with bandwidth-loss trade-off [34].

Excluding I/Q generator, the whole phase difference mechanism of vector modulator depends on active area; as a result, consumed area is much smaller than the previously mentioned phase shifting techniques. RMS gain error of the vector modulator technique is also lower in compared with the other designs; as can be seen from the equation (23), there is not much deviation in the total gain of the phase shifter. However, vector modulator technique consumes power, due to being an active design, which can be seen as a disadvantage.

Actually, one most significant problem about the vector modulator technique is its linearity performance. Due to being constructed with active devices, and giving priority to the phase performance of the design, dynamic range of the vector modulator is fairly poor in compared with the passive phase shifters. As a result of this, using vector modulator in the system may degrade whole T/R Module's linearity performance. In

other meaning, even its performance metrics are superior to other phase shifting mechanisms, passive structures can be preferred due to not limiting the linearity performance of the system.

3.4. Hybrid Phase Shifter Design

For a phase shifter, most significant performance parameter is RMS phase error; as a result the topology of the phase shifter should be selected with regarding phase performance, but if selected architecture limits the T/R Module performance, then chosen design should be reconsidered. For a phase shifter design that aims wideband operation, and high phase resolution, topology should be selected very carefully. Before starting the selection of architecture, it would be beneficial to emphasize on performance metrics according to their priority.

Different than other examples, first priority of the designed phase shifter is linearity; the proposed T/R Module includes a LNA that can supply at least 15dBm of output power. Then the input-P1dB of phase shifter should be at least 15dBm to operate the incoming signal without any distortion, if the SPDT switch has at most 2dB of loss. It would be very hard to configure a vector modulator type phase shifter that achieves 15dBm input-P1dB, without any degradation in the phase performance. For that reason, passive structures are most appropriate option, due to high linearity requirement.

Even if passive phase shifters satisfy linearity specifications of the system, it may not achieve wideband high phase resolution. Actually it is really hard to achieve a low phase error with passive phase shifters, even in narrowband operation. When similar works are analyzed, it is observed that most of the phase errors are a result of bad phase formation of MSBs [35]. Even if LSBs are designed well enough, 90^0 and 180^0 of phase differences are giving high phase errors. Thus, different solutions have to be found for the mentioned MSBs, to end up with low RMS phase error.

Another concern is the loss of the phase shifter; aiming at least 2.8^0 RMS phase error means the phase shifter can supply at least 6-bit of operation. As a result the loss of the design might reach at least 30dB; 6dB from the passive lumped components, while 24dB from the SPDT switches, with assuming 2dB loss per SPDT switch. High loss is not only affecting the gain of the T/R Module, but also the NF of the system; due

to having at least 30dB of loss, all gain of the LNA will be suppressed. As a result, NF of following blocks will directly add to system NF. To prevent that, loss of the phase shifter should be at least 10dB lower than LNA gain.

Using passive structures to design 6-bit phase shifter ends up with many inductors exist in the total layout. As a result, if a significant improvement is not applied to the passive phase shifters, total area might even exceed $10mm^2$, which is too large in comparison with the other blocks of T/R Module, and also very hard to design.

When all of the mentioned designing concerns are considered, combination of different phase shifter types can be a good approach, to include all advantages in a single design. Phase shifter design, which depends on mentioned approach, is named as hybrid phase shifter.

3.5. Block Level Description of Hybrid Phase Shifter

In this section, the blocks of the selected hybrid phase shifter design will be analyzed in detail. The hybrid phase shifter design depends on combination of passive structures with I/Q generator block of vector modulator technique. With that methodology disadvantage of each technique is surpassed.

At first switching mechanism for hybrid phase shifter will be described, which continues with the topology that is selected for each bit. After that, controlling mechanism for bits will be mentioned, and explanation of wideband operation. Finally the bit ordering, layout of the design, correction states and 7-bit performance of the phase shifter will be explained.

3.5.1. DPDT and SPDT Switches

When passive structures are decided to be used for phase shifter, a switching mechanism should be chosen to cause a phase difference between states. For that purpose, SPDT switches are usually preferred to be used in phase shifter design. Bits will not be dramatically affected by the loading affect, due to having a certain level of isolation.

There exist different types of SPDT switches, but generally the topology that is

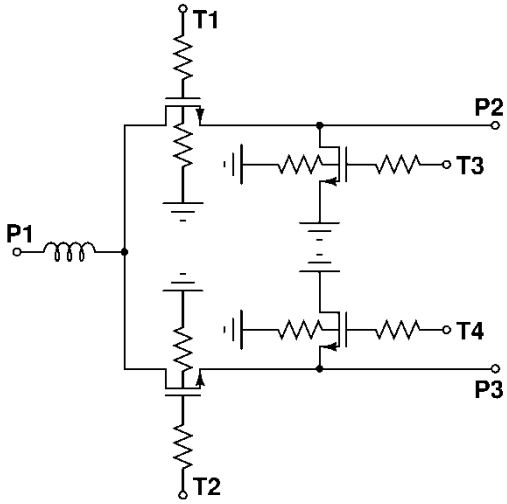
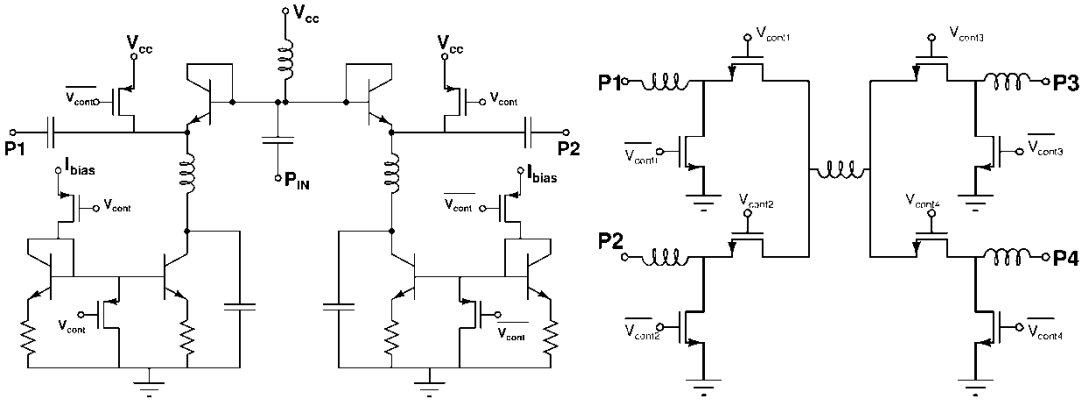


Fig. 34. Basic representation of SPDT switch

shown in Fig.34 is used, due to occupying small area, providing high isolation and operating wideband of frequency. In Fig.34, devices T3 and T4 are used as shunt transistors, while T1 and T2 is used for the series ones; the series transistors are used for blocking the incoming signal from input ports P1 and P2, while the shunt transistors are used for shorting leaking signal to ground. With that way, certain way of isolation can be achieved. Signal is transferred to the expected path with the help of the series transistor. As a result the loss is mainly determined by the "ON" resistance of the used NMOS transistor.

To decrease the loss of SPDT switch, some modifications in design can be done as in Fig.35 (a) [36]. In this design, shunt PMOS transistors are used for isolation purpose. Different than the previous design the series transistors are replaced with the Common-Collector amplifiers. Using emitter follower enables to end up with low loss, due to having approximately equal output and input signals. The switching-off mechanism for the emitter follower based on interrupting the current bias network of the amplifier. The amplifier type of switching mechanism can be seen as a good alternative due to low level of loss, if power consumption is not a concern. On the other hand, switch is amplifier oriented; as a result the dynamic range of switch can limit the linearity performance of the phase shifter.



(a) (b)

Fig. 35. Basic representation of a) Active-SPDT and b) Cascaded-SPDT switch

For specified phase shifter, a switch with low loss and high linearity should be used; as a result two different switches are preferred, which are Fig.35 (b), and Fig.36. Those switches include two input terminals and two output terminals, so they are called Double-Pole-Double-Throw (DPDT) switches. Actually, the design in Fig.35 (b) can be seen as a cascaded version of two SPDT switches, while the design at Fig.36 is working with the same principle with the SPDT switches. DPDT design in Fig.36 uses only a single series transistor, which are G_1, G_2, G_3 and G_4, in a certain signal path to minimize the loss, with shunt transistors (G_5, G_6, G_7 and G_8) connected to all terminals to increase the isolation [37]. As a result the DPDT switch in Fig.36 selected to be utilized for connecting the bits to each other, while simple SPDT switches in Fig.34 are preferred to be used for connecting the input and output of the bits to the following stages.

For the design of both SPDT and DPDT switches, isolated NMOS devices are used, which have thick gate-oxide; as a result higher voltage levels can be applied, which is essential to achieve high linearity switch design. For both designs, medium sized series NMOS transistors are used to decrease the "ON" resistance of the transistor; if the transistor size is selected too large, then internal capacitance of transistor will increase, which will a parallel load capacitance to incoming stage. Increased parasitic effects cause high phase variation across the band; hence transistor sizes are chosen with regarding trade-off between phase variation, insertion loss and isolation.

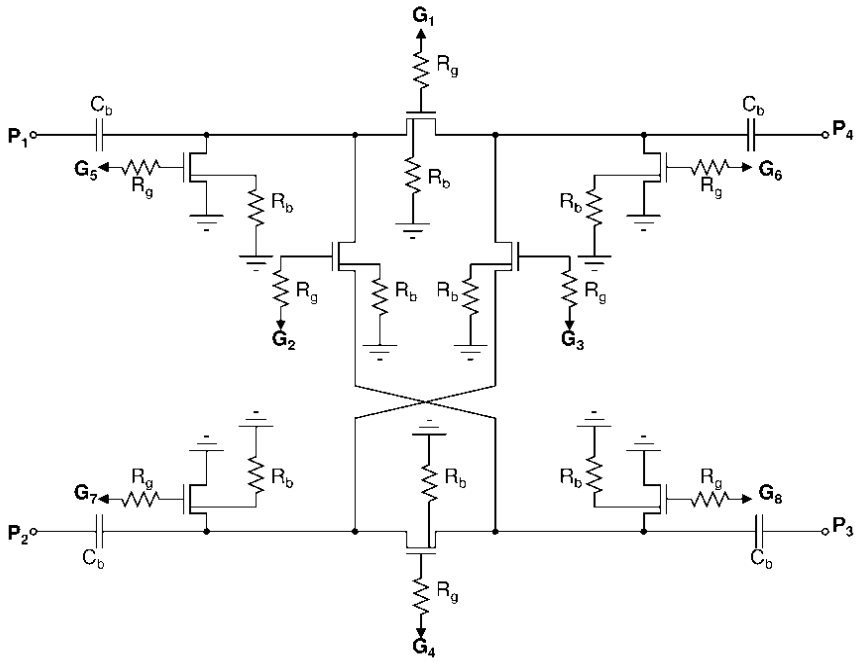


Fig. 36. Basic representation of DPDT switch

3.5.2. Filter Type Phase Shifter

Passive phase shifter design is used for LSB bits of hybrid phase shifter. One of the reasons of this selection is their linearity performance. In passive phase shifter designs, dynamic range performance is depending on the linearity of the switching mechanisms; as a result high linearity can be achieved with using passive phase shifters.

HP-LP filter type phase shifter is the preferred passive phase shifter design, due to its low phase variation across the defined bands. MSBs, such as 90^0 and 180^0, can cause problems for passive phase shifters due to their high phase variation and high phase error, so those bits are decided to be designed with using other architectures. One of the concerns about the passive structures is their area consumption. Filter type of designs are constructed with using π-network and T-network; as a result there exist many lumped components which increase the total area. In Fig.37, All-π and T network can be seen. When π-network or T-network is used for each bit, three inductors exist, which dramatically increase the total area. Instead of using π-network and T-network separately, the covered area can be approximately halved with using both networks together [35]. When T-network for HP and π-network for LP is chosen, only two

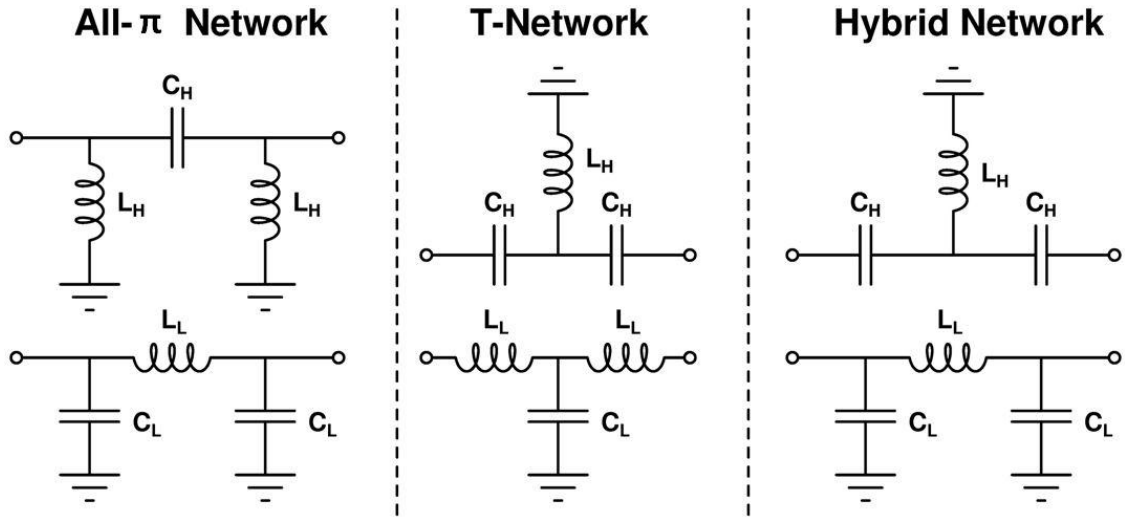


Fig. 37. Different filter type phase shifters architectures

inductors are enough to construct expected HP-LP mechanism, as demonstrated in Fig.37.

In HP-LP topology, HP constructs +ϕ, while LP constructs -ϕ of phase difference. Before going into detail about the selection of architecture for each bit, it would be beneficial to introduce the working principle of HP-LP filter. Fig.38 demonstrates half-circuit model of HP filter for π-network. Input impedance of half-circuit, Z_{in}, can be calculated as;

$$Z_{in} = \frac{1}{jw2C_S} + (Z_L \,//\, jwL_P) \tag{27}$$

where

$$Z_L \,//\, jwLp = \frac{(w^2 L_P^2 Z_L + jwL_P Z_L^2)}{(Z_L{}^2 + w^2 L_P{}^2)} \tag{28}$$

For matching purposes, Z_{in} should be 50Ω, which means that imaginary part should be zero. Therefore,

$$imag(Z_{in}) = \frac{-j}{w2C_S} + \frac{jwL_P Z_L{}^2}{(Z_L{}^2 + w^2 L_P{}^2)} = 0 \tag{29}$$

which enables to calculate series capacitance of half circuit as,

$$2C_S = \frac{(Z_L{}^2 + w^2 L_P{}^2)}{(w^2 L_P{}^2 Z_L{}^2)} \tag{30}$$

Next step is calculating parallel inductance, L_P, which will be used to extract $2C_s$. For

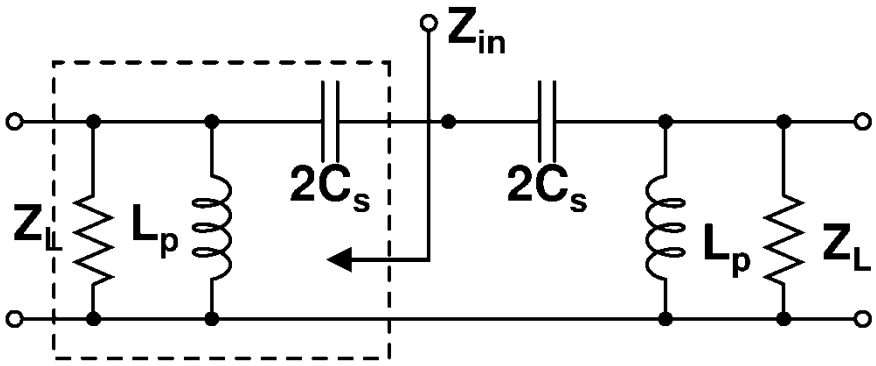


Fig. 38. Half-circuit analyze of HP filter for π-network

that purpose transfer function of half circuit, H(w), can be calculated;

$$H(w) = \frac{(Z_L \,//\, jwL_p)}{(Z_L \,//\, jwL_p) + \left(\frac{1}{jw2C_S}\right)} \tag{31}$$

When simplifications are done, transfer function is obtained as

$$H(w) = 1 - \frac{jZ_L}{wL_P} \tag{32}$$

As a result, phase of the transfer function can be founded;

$$\angle H(w) = \phi/2 = \tan^{-1}\left(\frac{Z_L}{wL_P}\right) \tag{33}$$

With using equation (33), L_p can be extracted as

$$L_P = \frac{Z_L}{w\tan\left(\frac{\phi}{2}\right)} \tag{34}$$

Equation (34) gives the chance of calculating specific inductance of π-network for preferred phase value. For calculating series capacitance value as L_p, (34) should be inserted (30), which results with

$$2C_S = \left(\frac{Z_L{}^2 + \frac{w^2 Z_L{}^2}{w^2 \tan^2\left(\phi/2\right)}}{w^2\left(\frac{Z_L}{w\tan\left(\phi/2\right)}\right)Z_L{}^2} \right) \tag{35}$$

When appropriate cancellation and trigonometric simplifications are done, series capacitance of π-network can be calculated as

$$C_S = \frac{1}{wZ_L \sin\phi} \tag{36}$$

Similar calculations can be done for the LP design, which will end up with;

$$C = \frac{\tan\left(\phi/2\right)}{wZ_0} \quad \text{, and} \quad L = \frac{Z_0 \sin(\phi)}{w} \tag{37}$$

Calculated results are applicable for All-π network, but they can be easily transformed to T-network values, by basic impedance transformation [35].

HP-LP filter type phase shifter is only used for 3rd and 4th bit of the design. The reason is basically the lumped components that are used in the filter; as phase difference gets lower, component values start to be more unfeasible. Due to requiring undesirable capacitance and inductor values, remaining LSBs are not constructed with using HP-LP topology, but designed with LP-LP topology. The reason for selecting LP-LP design instead of HP-HP design is basically the total area; HP-HP design includes parallel inductors which increase the area when other blocks are considered.

1st bit, so called LSB, is also designed with LP-LP topology, as can be seen from Fig.39 (a). As in previous case, forming LSB with HP-LP filters is not feasible. Also, LSB is one of the most significant bits of phase shifter, due to having smallest phase which can cause high phase error; as a result it should be formed separately from the remaining bits, due to being very influential on total RMS phase error. After constructing 2nd, 3rd, and 4th bit with using DPDT switches, 1st bit is connected to them with the help of SPDT switches. As a result, 1st bit is much isolated from the remaining bits, which causes 1st bit less affected from the connected bits.

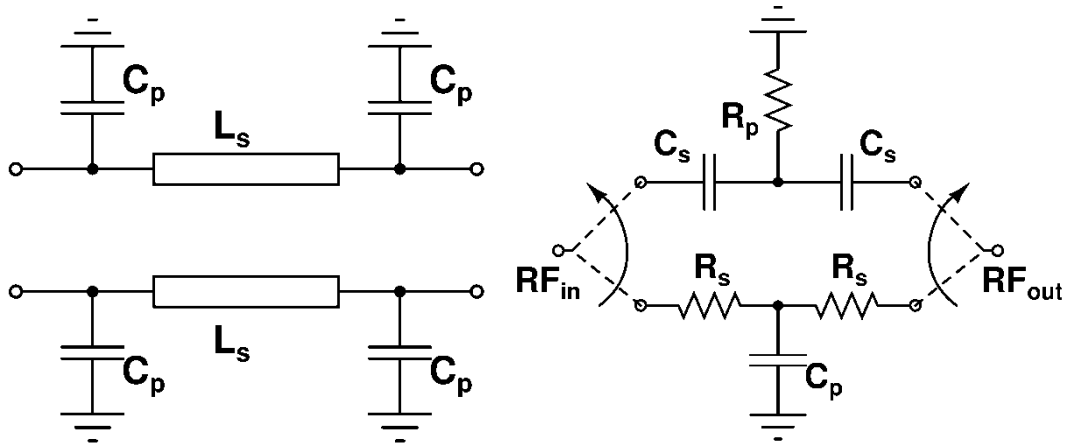


Fig. 39. a) LSB and b) 5th bit of hybrid phase shifter

3.5.3. T-network for I/Q Generator

For the remaining 5th and 6th bit, a different mechanism should be used, to come up with low RMS phase error, and less area. Vector modulator technique is an active phase shifter design, but it still uses mostly passive structures for 90^0 and 180^0. Designing those bits with using HP-LP structures causes high phase variation, as mentioned before. Instead of those topologies, using I/Q generator of vector modulator is one of the best alternatives. I/Q generators with RC network can generate almost flat phase response, while consuming very low area in compared with HP-LP topology, due to using only resistance, and capacitance. The used RC network for I/Q generator can be seen in Fig.39 (b). RC network are usually designed with L-network, but T-network is preferred for I/Q generator, due to its reciprocal behavior, which improves return loss performance of network. Constructing I/Q network with resistance is an proper choice to enhance wideband phase performance of phase shifter. The disadvantage of designed I/Q network is having high loss and high RMS gain error, which increase the RMS gain error of the total Phase shifter design.

3.5.4. Common Emitter-Common Base Amplifier Design

Active circuitry is decided to be utilized for 6th bit. As mentioned in the vector modulator section, constructing 180^0 of phase shift with VGA can cause performance degradation, so additional architectures can be used to form 180^0. Passive balun

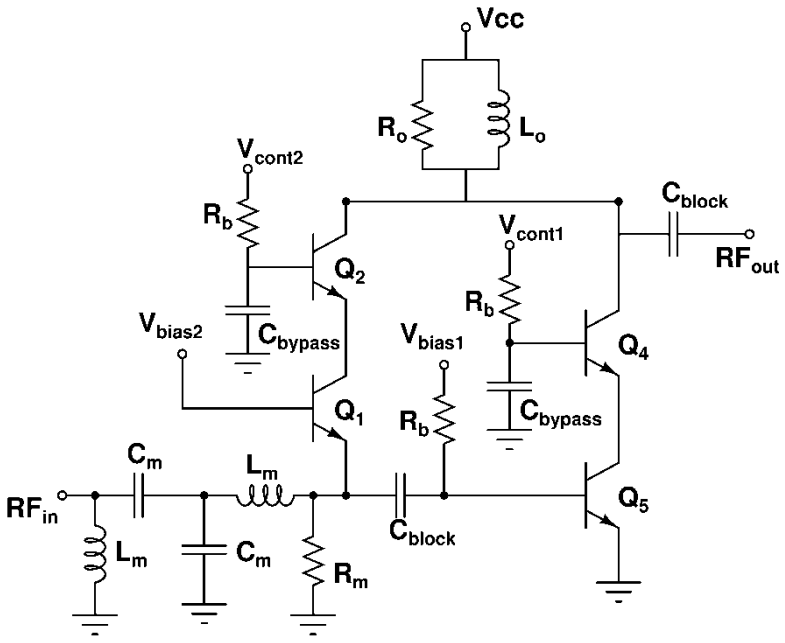


Fig. 40. Common Base – Common Emitter architecture for 6th bit

structures achieves good linearity performance but lacks from compactness, as a result active balun structures are better option even they have problems from the aspect of linearity. Due to introducing loss to system while forming LSBs, input power will be low enough to not to saturate 6th bit.

Common Emitter – Common Base (CE-CB) design, which can seen in Fig.40, is a good alternative to construct 180^0 of phase difference. The design is based on combining the output of CE cascade amplifier and CB amplifier, with the help of control voltages. CE amplifier is an inverting amplifier, while CB amplifier is a non-inverting amplifier; as a result both amplifiers have about 180^0 of phase difference from their amplifying nature. Basically, it would be enough to turn one of the amplifiers off, to achieve expected level of phase shift. One of the advantages of this design is its gain performance. There exist two different phase states for the CE-CB design, and both of these phase states include an amplifier that has a certain level of gain. If both amplifiers are managed to have about same gain level, RMS gain error of the structure becomes very small. One of the disadvantages is its input return loss performance, which varies with switching on-and-off different amplifiers. The mentioned disadvantage can be solved with increasing the order of the input matching network.

Mainly, phase difference performance is determined with the amplifier performance and their bias voltages, but also other components can be used for phase

adjustment, in addition to their original functionality. The capacitance "C_{block}" is used as a DC blocking capacitance between the amplifiers, but phase can also be adjusted with using this capacitance. For the output matching network, RL-network is used. Both amplifiers are connected to the same output node and both CE and CB amplifiers have a CB amplifier as a load transistor; as a result their output return loss performance does not vary much, differently from input return loss.

In terms of constructing a certain level of phase shift and their switching mechanism, all blocks are described. When the total gain performance is calculated briefly, it can be observed that loss of the whole phase shifter design is close to 30dB, even with using DPDT switches, and active balun structure. The reason of this is, using SPDT switches for 1^{st} and 5^{th} bit, and utilizing T-Type RC network for the 5^{th} bit. SPDT switches introduced about 4dB of additional loss to the system. RC structure with T-network is used to improve the return loss and phase performance of the bit, but gain performance and RMS gain error is sacrificed for a certain level of phase flatness. 50Ω of series and parallel resistances are used in the total design, which improved the bandwidth of the design, while it increased the loss dramatically. As a result, the total loss and RMS gain performance worsened, even with using active balun design.

3.6. Wideband Operation for Hybrid Phase Shifter

Designing a wideband phase shifter that is dominated with passive structures, should not be done with selecting a single center frequency. A common property of passive phase shifters is, having sharp upswings in RMS phase error curve, after passing selected center frequency.

To solve this problem in hybrid phase shifter design, two different center frequencies are selected; so 3 bits are designed with regarding one center frequency, while other bits are constructed with focusing on second center frequency. With that methodology, RMS phase error curve will not be a "V" type, but be like a flat and sinusoidal type result.

For a phase shifter the highest RMS phase error is the limiting factor. So instead of having a very low RMS phase error in a single center frequency, forming a higher

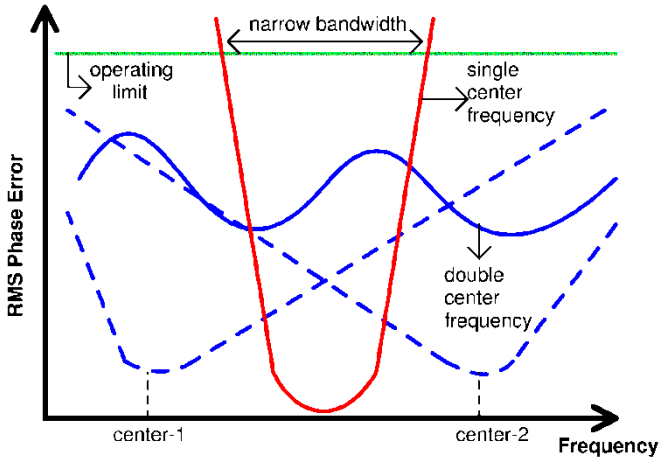


Fig. 41. Description for RMS phase error with double center frequency

error rate in the center frequency, and obtaining a wider bandwidth is more essential, as depicted in Fig.41.

3.7. Additional Low Noise Amplifier Design

Total loss is a significant problem that has to be solved. As mentioned briefly, a 30dB of loss will end up with very low gain and very high NF in system level performance, when LNA about 20dB of gain is used. This problem can be solved, with using an additional block of 2-stage LNA; with that way total size of the design will increase, but the gain performance will be superior without sacrificing the linearity of the design. With regarding mentioned concerns, a two-stage cascode LNA is designed, which is depicted in Fig.42. The important concern of the LNA design is its bandwidth of operation; its return loss and gain flatness should be at a level that is not affecting the designed phase shifter. As a result, LNA is designed with regarding performance specifications of other blocks that will be connected.

3.8. Digital Circuitry for Controlling Mechanism

There exist several DPDT and SPDT switches in the hybrid phase shifter design, and they should be controlled with a digital controlling mechanism. Especially, each DPDT switch requires eight different control inputs, which will cause trouble without a digital controlling mechanism. On the other hand, there exist two separate DPDT designs, which mean that there should be sixteen different DC pads, without counting

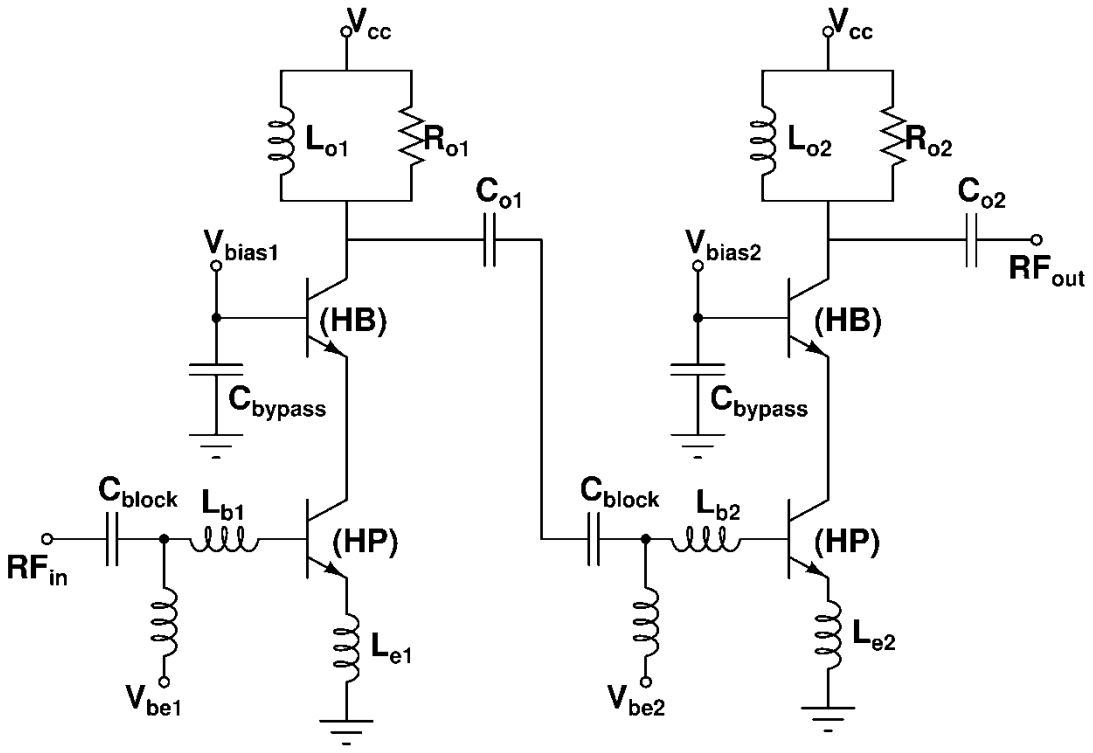
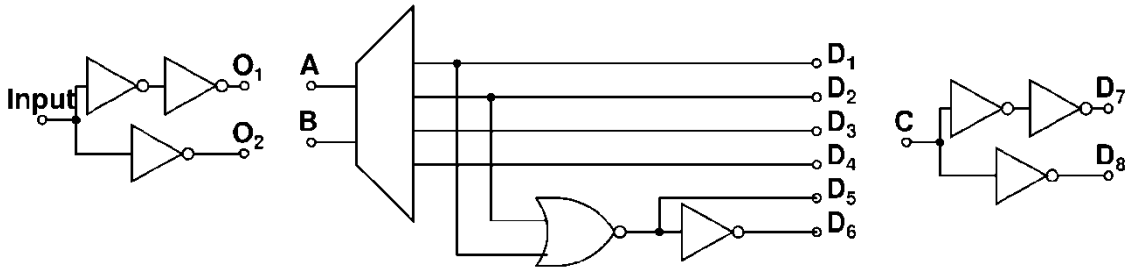


Fig. 42. Low Noise Amplifier for hybrid phase shifter

the supply voltages for n-well terminal, source, and drain of the NMOS transistors. If a digital circuitry is not used in the total structure, the number of pads would surely increase total area of design; for that purpose full-custom digital circuitries are designed.

Steady state performance is expected from digital circuitries; as a result they do not include any clock in the total structure. Controlling SPDT switches is straight-forward, due to requiring only a buffer and an inverter. The total digital circuitry that is used for SPDT switches can be seen from Fig.43 (a). For DPDT switches, the digital circuitry is more complex than SPDT switches, due to having independent eight different DPDT inputs. As a result, a digital circuitry is designed with regarding the Look-Up Table (LUT) of the DPDT switch. The digital circuitry for DPDT switch includes 2-to-4 decoder, Buffer, NOR gate, NAND gate, and inverter. Total structure can be seen from Fig.43 (b) and Fig.43 (c).

Devices of digital circuitries have a significant difference in compared with the NMOS transistors that are used in the RF circuitry; they have different bias conditions. In switches, RF-NMOS devices are biased in a way that the gate voltage can reach up to



(a) (b) (c)

Fig. 43. Control circuitries for SPDT and DPDT switches

4.6V, while the source and drain voltages are 2V. The reason of choosing described biasing conditions is basically improving linearity of the switch. Even if same NMOS transistors are used in digital circuitries, logical output "1" level means 2.5V, due to using 2.5V of supply voltage. To convert the 2.5V of digital output voltage level, to 4.6V, which is required for the switch inputs, a level shifter circuitry is designed, as can be seen from Fig.44. Actually, the designed level shifter is not full satisfying the expectation; it can reach up to 4.57V, while logical "0" is equal to about 0.14V. The voltage difference causes* a change for the "ON" and "OFF" resistance of the switches, but due to not observing any major change in the total phase, the selected topology is used for level shifter purpose.

3.9. Bit Ordering

Bit ordering is very significant to improve the performance of phase shifter design. For instance, if the first block has poor input-P1dB performance, whole system performance would be affected, even remaining blocks have adequate input-P1dB. Moreover, area consumption is one of the most significant concerns about bit ordering; for total layout, an "S" type layout template is decided to be used. Otherwise, the layout would be inefficiently horizontally long.

Return loss of each block is very significant, because each block is designed with regarding 50Ω load impedance, but unfortunately it is not possible to construct all bits with wideband matching. As a result, bits that have best return loss performance is tried to be placed in the center of the whole system. 2^{nd}, 3^{rd}, and 4^{th} bit is designed together with using DPDT switches, so 1^{st}, 5^{th}, and 6^{th} bit can be placed after the mentioned 3-bit group. 5^{th} bit has the worst return loss performance among all of the bits, while 6^{th} bit

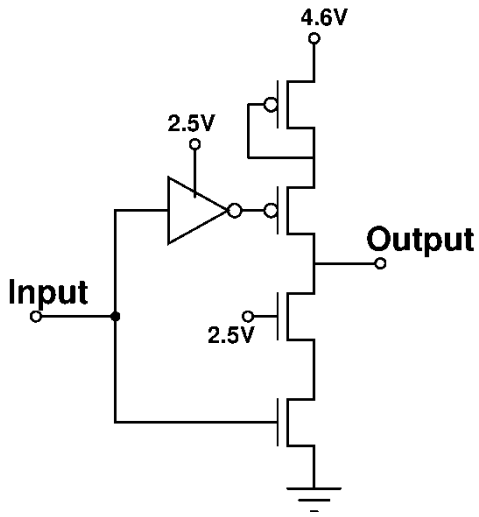


Fig. 44. Level shifter for digital circuitries

has low input-referred compression point. So, 1st bit is the only option that is appropriate after 3-bit group without performance degradation.

Other benefit of using 1st bit after 3-bit group is, lowering the output power; 6th bit comes right after first 4 bits, to increase the gain level, but if a high output power is served, 6th bit will compress the signal. To prevent that, 1st bit is beneficial to introduce loss and lower output signal power.

After 6th bit, lately designed LNA is placed, to improve the gain performance. 6th bit requires good output return loss performance, while 5th bit requires wideband input matching; as a result LNA is not only functional for improving gain and NF performance of the total structure, but also acts like a transition block between last two MSBs, with the cost of increased area and power consumption.

So-called 3-bit group is constructed with regarding total area; 3rd and 4th bit are designed with HP-LP filters, while 2nd bit designed with LP-LP filters. LP-LP filters include series inductors, while other two bits include parallel inductors. If 3rd, and 4th bit are cascaded, total are would increased due to existence of other parallel inductors. Total bit ordering figure can be seen Fig.45.

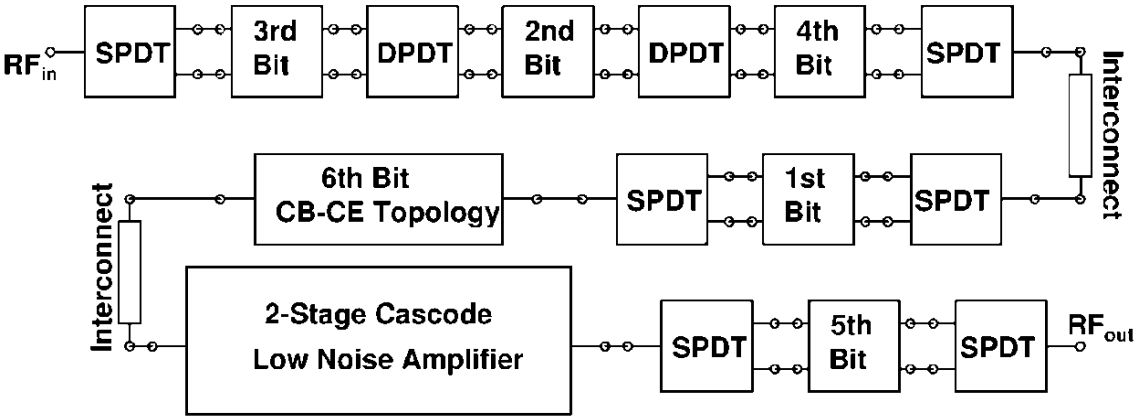


Fig. 45 Order of stages for hybrid phase shifter

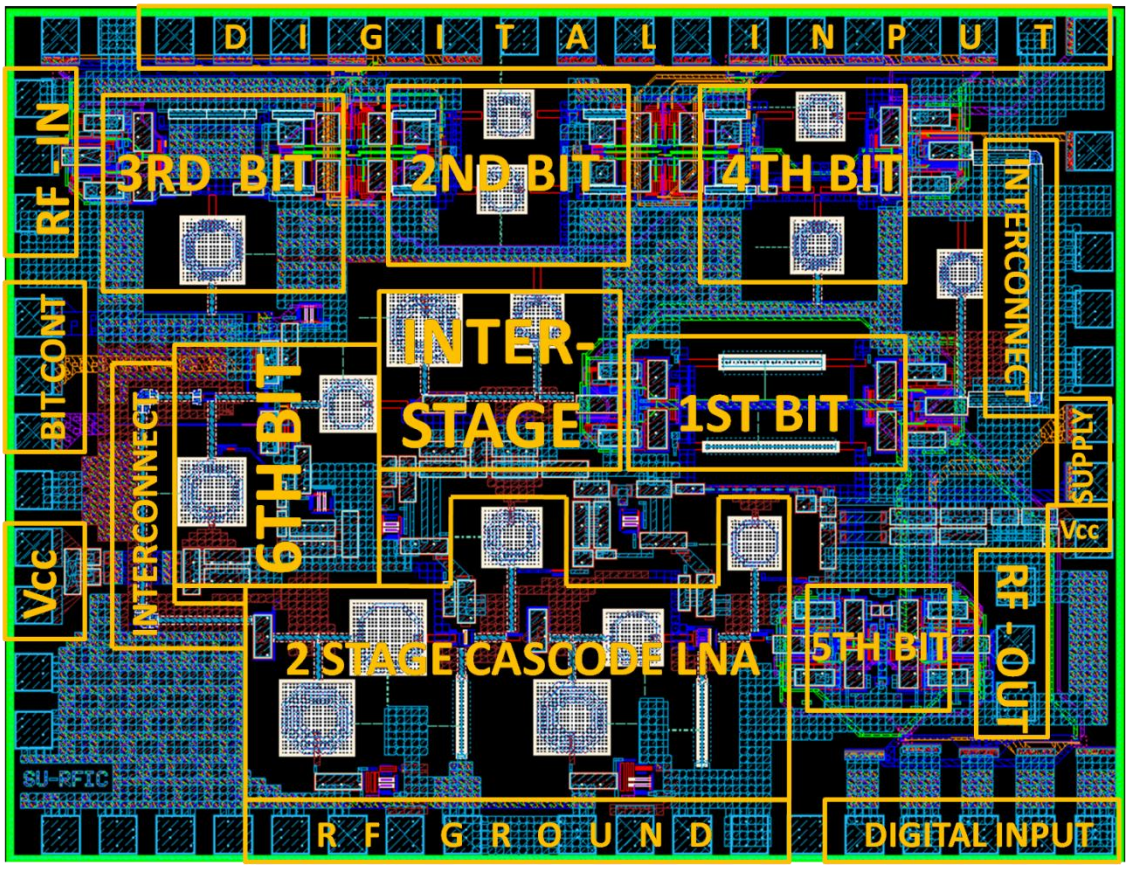


Fig. 46. Layout of hybrid phase shifter

3.10. Layout of Phase Shifter

Ordering the bits of hybrid phase shifter is done with considering the total area of the layout. Total area is 6.27 mm^2, from pad to pad; additionally added LNA consumes about 1.32mm^2 area, without pads. As a result, pure effective phase shifting area can be told as 4.96 mm^2. Constructed layout can be seen from Fig.46.

Some areas in the layout are left blank intentionally, such as spaces around spiral inductors. If inductors are placed too close to each other, their magnetic fields start to affect each other, which will cause a deviation from model parameter. Also placing inductors at least 80μm away from nearest substrate contact increased total area, which is significant for preventing substrate loss. It is essential to ground substrate, due to preventing parasitic affect that occur due to substrate, but adding substrate contact close to inductor will decrease the substrate resistance, which will affect the performance of the inductor.

Even if a clock does not exist in the digital circuitry, coupling between RF and Digital circuitry is a serious case to be solved. At least 80μm of separation is left between RF-Analog circuitries, and Digital circuitries, to improve isolation. Also, no substrate contacts are used in the described separation area, to increase the substrate resistance between circuitries. On the other hand, Deep Trench Isolation (DTI) mask layers are used around the digital circuitries, to isolate digital circuitry more; DTI layer gives a chance of increasing the resistance between circuitries.

3.11. Simulation Results

RMS phase error is one the most significant metric of the phase shifter design, which determines overall phase performance of the design. As mentioned, two different center frequencies are selected, as a result multiple deviations in RMS phase error are observed, as can be seen in Fig.47. Designed hybrid phase shifter is expected to have at most 2.8^0 of phase error at X-band, which is achieved for 4.5GHz. When 6-bit operation is considered, bandwidth of hybrid phase shifter is 6.75GHz, while it is 4.5GHz for 7-bit operation.

Gain performance varies between different phase states; lowest loss is -11.25dB, while highest -17.5dB at 10GHz, as in Fig.48. Main reason of high loss is 5^{th} bit, which

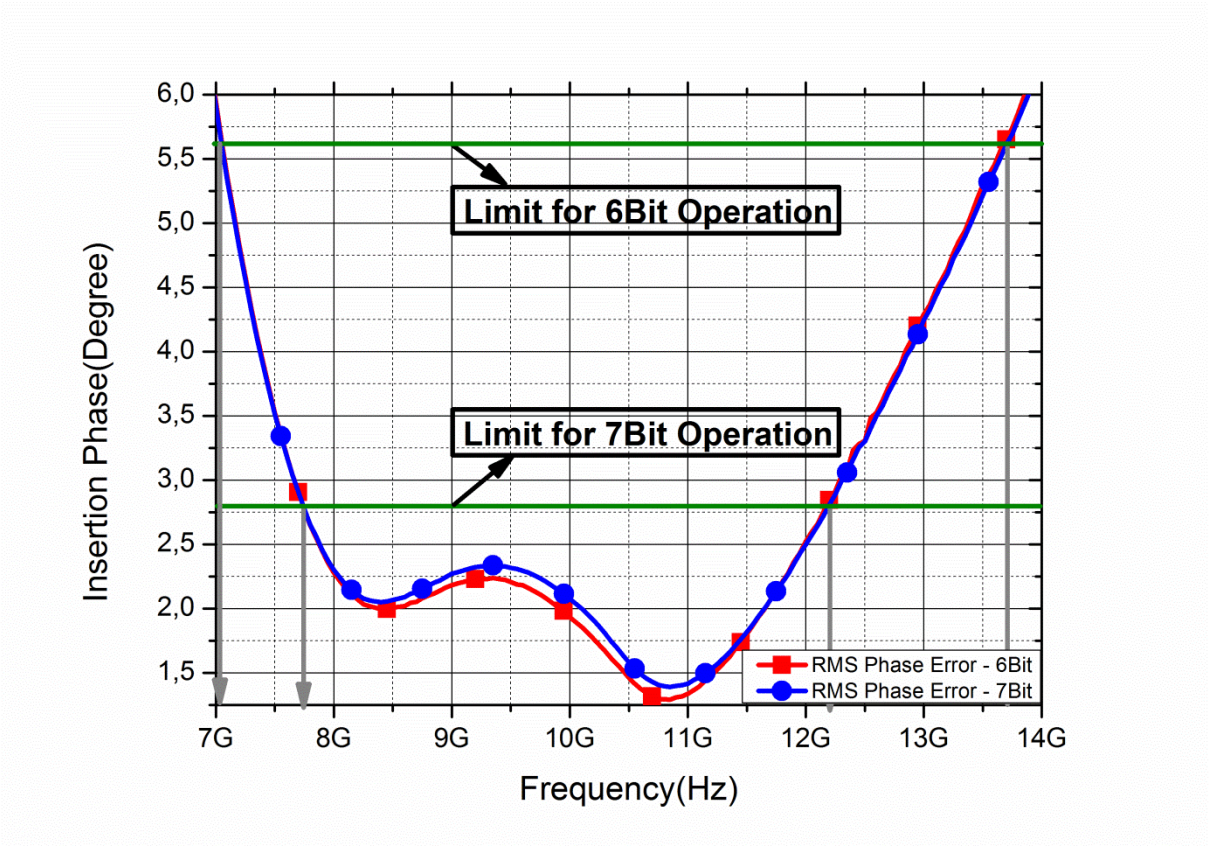


Fig. 47. RMS phase error for 6-bit and 7-bit operation of hybrid phase shifter

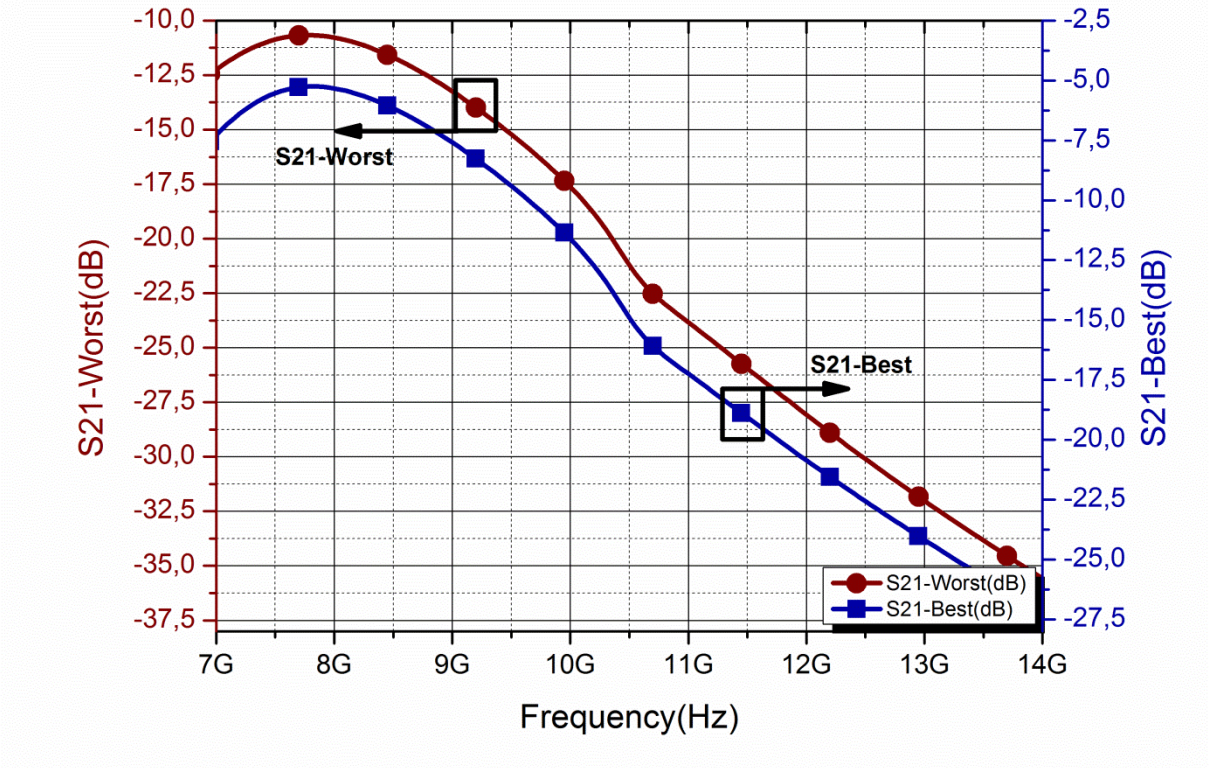


Fig. 48. Best and worst gain performance of 6-bit hybrid phase shifter

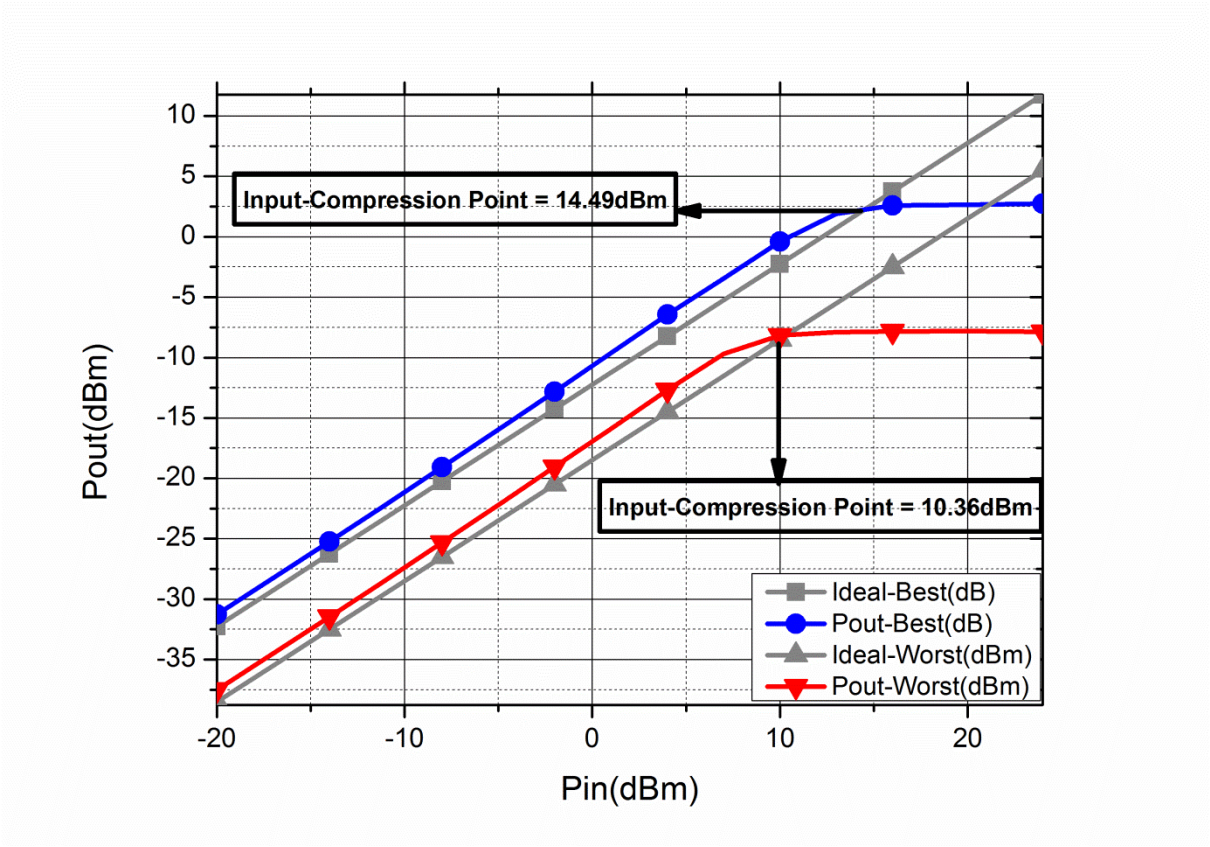


Fig. 49. Best and worst input-P1dB performance 6-bit hybrid phase shifter

is composed of RC-network. On the other hand, loss of RC-network varied unexpectedly high across X-Band. SPDT loss that is close to 2dB can be told as another major reason of high loss of hybrid phase shifter. RMS Gain error of hybrid phase shifter is about 6dB.

Input-referred compression point performance is one of the main goals of hybrid phase shifter, because if constructed phase shifter has poor linearity performance, then designed high linearity LNA for T/R module will be useless, due to not reflecting its high output power to the following stages. As represented in Fig.49, hybrid phase shifter achieves the high linearity specification, with reaching 14.49dBm of input-P1dB, at its last phase state. As phase states vary, input-P1dBm also changes as expected, due to varying loss and impedance. Minimum input-P1dB is 10.36dBm at first state, which is still acceptable, due to still achieving expected linearity performance for T/R Module.

Return loss performance is represented in Fig.50. Input and output impedances are matched to optimum impedance value to end up loss phase variation across X-Band, instead of being matched for maximum power transfer, which degraded return loss

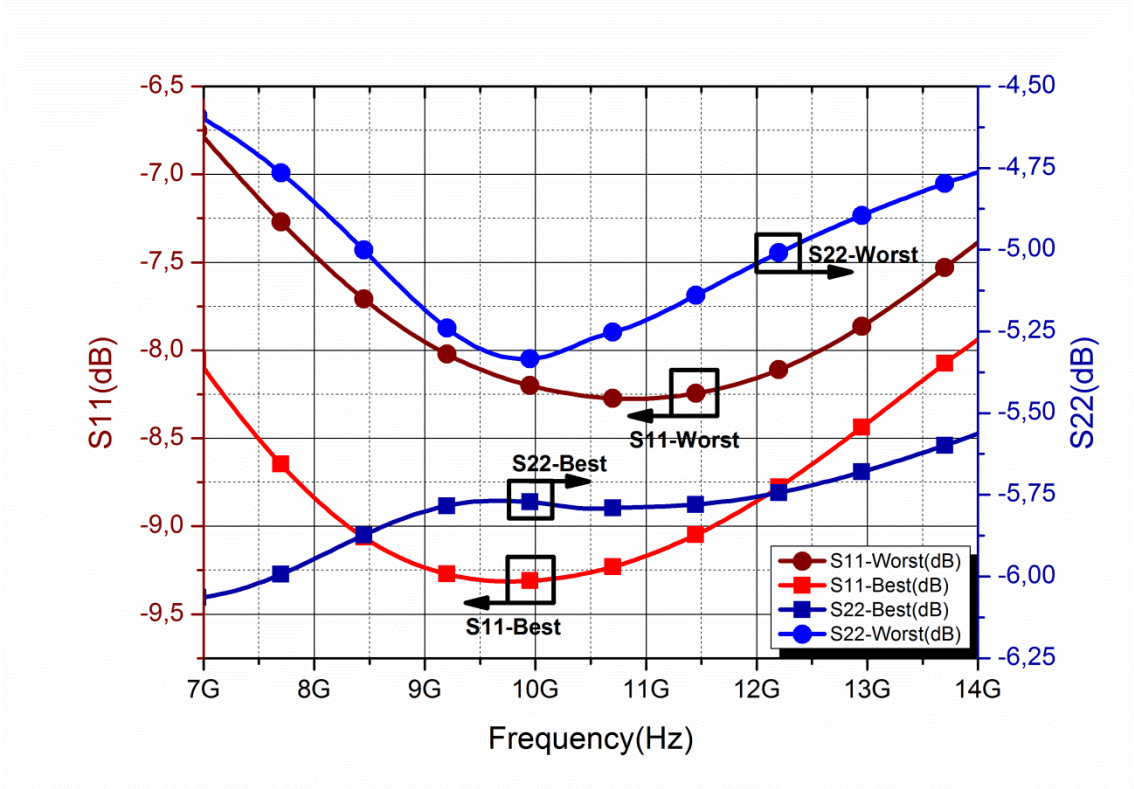


Fig. 50. Best and worst input and output matching performances of hybrid phase shifter

performance. Actually, much better input matching could be achieved with adding a series inductance at input port, which increase about 0.6mm^2; even if preferred inductance value is small enough, it widens layout dramatically. In other meaning input return loss is sacrificed for smaller area. Output return loss is related with 5th bit itself; poor input and return loss are expected from RC-network, which is not possible to be corrected with introducing new components. It should be noted that, hybrid phase shifter designed with regarding 50Ω loads; if dissimilar load impedance values are introduced, design can suffer from RMS phase error and phase variation. Moreover, hybrid phase shifter consumes power, due to including active devices. Highest power consumption is 141.5mW, while lowest value is 116mW.

3.12. Correction States and 7th bit of Phase Shifter

Designed phase shifter aims very low RMS phase error in a wideband region, as a result practical solutions for the failure mechanisms should be found. The hybrid phase shifter design includes several digital control voltages, and 4 different analog control voltages; two of the analog voltages are for controlling 6th bit, while remaining two are

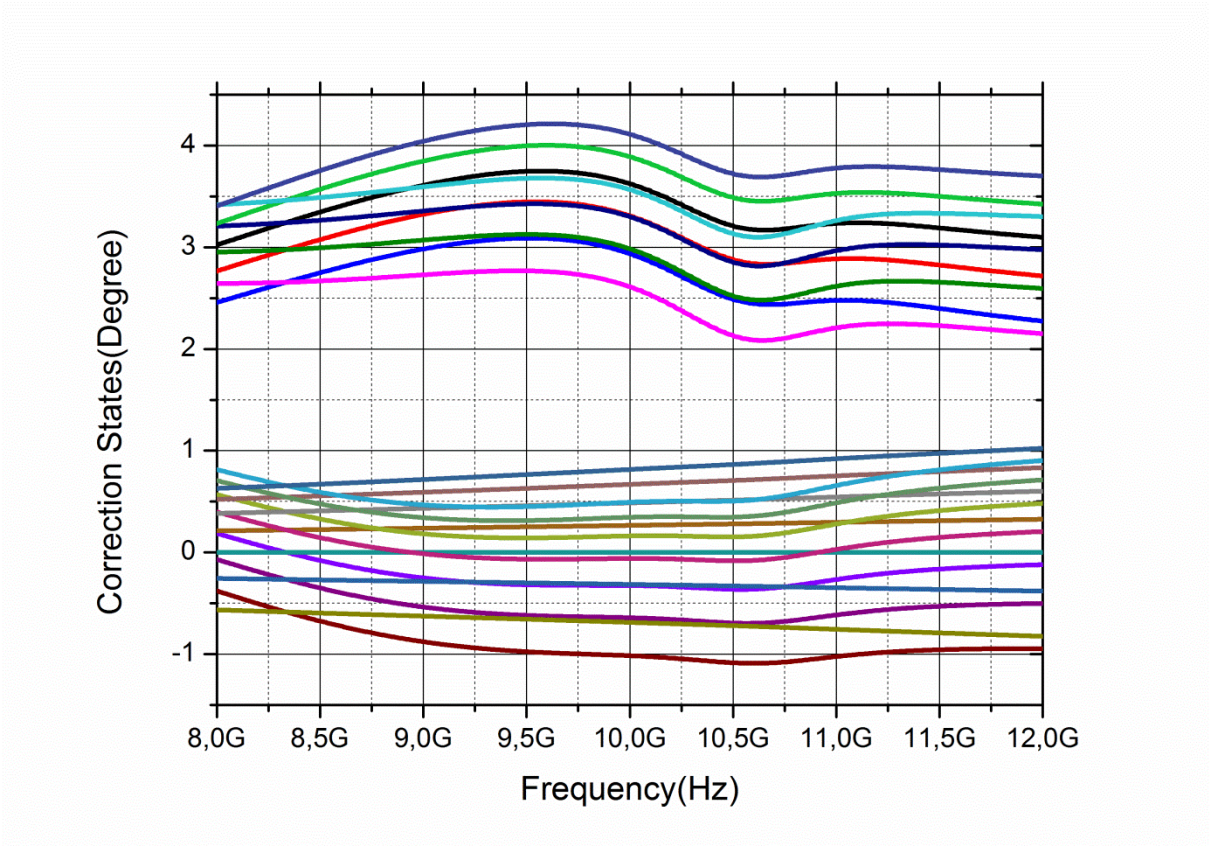


Fig. 51. Correction states of hybrid phase shifter

for bias networks of LNA. For minor changes or improvements, small variations at those analog control voltages can improve the phase resolution performance of the design, without any degradation in the gain performance. The mentioned method gives the chance of addition or subtraction of phase states that has high errors. The correction states can be seen from Fig.51.

With the "correction method" a new question can pop-up; what if the circuitry, does not require any correction? As in simulation results, there is no need for correction due to constructing all states of the 6-bit phase shifter, but this result does not mean that the control voltages are ineffective. They can be rearranged to form a new LSB; 7^{th} bit. Without any additional block, design can construct some states of 7-bit phase shifter, which means that hybrid phase shifter can switch between 6-bit and 7-bit performance, with regarding the expected performance. RMS phase error result of 7-bit phase shifter can be seen from Fig.46, with 6-bit performance. Due to constructing new LSB almost flat, new RMS phase error does not differ much from the 6-bit RMS phase error.

3.13. Performance Comparison

Table II represents the comparison of designed hybrid phase shifter design with similar phase shifter examples in literature. If LNA is excluded from the phase shifter layout, the area reduces to 4.96mm^2. When only phase shifting mechanisms are collated, the design consumes low area in compared with the other passive structures. Due to including active elements, loss performance is enhanced, in comparison with passive phase shifter examples, but due to including passive architectures, active phase shifters have higher gain, which is expected. Even if hybrid phase shifter includes active devices, it satisfies linearity specifications. When RMS phase error and wideband operation is compared, design achieved one of the best results; it has 6.75GHz of bandwidth for 6-bit operation, while it is 4.5GHz for 7-bit. On the other hand it consumes smaller area than passive phase shifter architectures, with achieving high dynamic range that is much better in compared with active phase shifter designs.

TABLE 2. Performance Comparison with Similar Works in the Literature

	This Work (6-Bit)	**This Work (7-Bit)**	**[36]**	**[35]**	**[37]**	**[38]**	**[39]**
Architecture	Hybrid	Hybrid	Passive	Passive	Passive	Active	Active
Number of bits	6-Bit	7Bit	5-Bit	5-Bit	6-Bit	6-Bit	5-Bit
Frequency	8-12GHz	8.12GHz	8.5-10.5GHz	8-12GHz	8.5-10.5GHz	8-12GHz	6-18GHz
RMS Phase Error	5.625^0	2.8125^0	8^0	13^0	4.1^0	5.6^0	5.6^0
Bandwidth	6.75GHz	4.5GHz	2GHz	4GHz	2GHz	4GHz	12GHz
Gain	-11.25dB	-11.25dB	-17dB	-25dB	-13.2dB	-10dB	16.5dB
Input-P1dB	14.49dBm	14.49dBm	4.4dBm	-	3dBm	2dBm	-17dBm
Power Cons.	141.5mW	141.5mW	248mW	1mW	1mW	16.6mW	61.7mW
Chip Area	6.27mm^2	6.27mm^2	9.84mm^2	4.87mm^2	-	0.45mm^2	0.9mm^2

4. CONCLUSION AND FUTURE WORK

4.1. Summary of Work

Previous generation phased array structures were using mechanical equipments for beam shifting mechanism. New phased array systems are shifting beam electronically, with the help of T/R module structures. Thousands of T/R module structures are used in a phased array system. T/R module is responsible for electronically beam shifting mechanism, receiving and transmitting of signals; therefore its features are very influential on system level performance. Due to targeting high performance metrics, III-V semiconductor technologies are suggested for T/R module systems. III-V devices can satisfy the requirements of whole structure with disadvantages, such as high cost, large size, and weight. As a result, T/R module based markets are majorly dominated with military applications. Recent enhancement in SiGe HBT BiCMOS technology enables Si-based devices used in T/R Module structures, thanks to bandgap engineering. With using SiGe devices similar performance metrics can be achieved in smaller area with lower cost, in compared with III-V devices, which extends market to commercial applications. This thesis presents two major blocks of SiGe HBT BiCMOS based X-Band T/R Module; high dynamic range LNA and wideband hybrid phase shifter.

Three different LNA structures are presented in this thesis, with aiming high dynamic range metric. Single-stage LNA design is designed with using IHP Microelectronic's 0.13µm SiGe BiCMOS technology. Selected Cascode LNA structure achieved about 16.4dB of gain, with lower than 1.2dB of NF in simulations. For improving linearity, load transistor of cascode topology is biased with regarding full voltage swing; thus input-referred P1dB is obtained as -3.87dBm, with 20mW of power consumption. When measurements are done for single-stage cascode LNA, significant deviation for collector current level is observed, which results with degradation in return

loss performance, gain, and NF; gain is measured about 10dB, while NF is 1.9dB at 9GHz. Having a low β_{DC} value is a consequence of unexpected emitter resistance, which concludes with a certain deviation in design metrics. Input-P1dB is measured as -0.25dBm, due to having a lower gain than expected.

Telescopic LNA topology is preferred for targeting high linearity with high gain. As in previous LNA design, IHP Microelectronic's 0.13μm SiGe BiCMOS technology is used for telescopic LNA. Using two-stage can be another option to result with high gain, but selected technology support only HP devices which have low breakdown voltage. As a result a new approach is applied to end up with high gain with high dynamic range; addition of another load transistor, enhances linearity and gain performance of the design, with same HP transistors. Drawback of telescopic design is consuming high power to achieve linearity. Telescopic structure achieved about 20dB of gain, with lower than 1.6dB of NF between 9-to-11GHz. Input-referred P1dB is -3.55dBm in simulations. As in single-stage LNA, DC collector current is low in compared with the simulations; as a result return loss performance is degraded and shifted to lower frequencies. On the other hand, reverse isolation has a sharp decay, which causes design to work at the edge of oscillation. For a center frequency of 7.5GHz, designs has acceptable level of return loss performance with mean 16.5dB gain, and NF with lower than 2dB. Input compression point is measured about 2.5dBm, which matches with simulation results.

Two-stage amplifier is designed with using IBM's 0.13μm SiGe BiCMOS technology. One of the main reasons of selecting two-stage structure is to obtain high input dynamic range, with higher gain and lower power consumption, as in previous two LNAs. Other than HP transistors, HB transistors are also supported for mentioned technology; second stage of LNA requires higher linearity performance, which can only be achieved with HB transistors. Additional stage increased NF, which is sacrificed to have better linearity with lower power consumption. Transistor scale is affecting the breakdown voltage limitations of CB transistor, and described scaling technique is used to enhance output voltage swing, which improves linearity. Two-stage LNA design achieves about 20.5dB of gain, with 2dB of NF between 9-to-11GHz. Input-P1dB is -3.72dBm, with consuming 115.8mW of power. In compared with similar works, designed LNA has best input dynamic range, which is achieved with low power consumption and high gain.

Wideband hybrid phase shifter is designed for specified phase shifter block of T/R module. Due to having high output power from LNA, SPDT and phase shifter blocks also require high dynamic range for transferring output signal of LNA to incoming blocks. For designed phase shifter, one of the targets is having high phase resolution in a wide bandwidth. Vector modulator topology can achieve wideband results with low RMS phase error, while passive designs have best linearity performances. Hybrid phase shifter aims to combine advantages of different phase shifter designs in a single structure. For this purpose, HP-LP and LP-LP filters, active balun design, and I/Q generator are preferred, while DPDT and SPDT switches are used to combine bits. For control voltages of switches, full-custom digital circuits are designed, instead of using pads. Also an additional level shifter is designed for converting 2.5V to 4.6V; digital circuits can supply maximum 2.5V, while switches require 4.6V of gate voltage. So, level shifter is working as a buffer, which converts the voltage level of digital circuits.

One methodology that is used for having wideband operation, is selecting two center frequencies, to achieve wider RMS phase error response. To improve gain performance, two-stage LNA is added to design. Different than other phase shifter examples, hybrid design includes its own correction states, which are generated with certain control voltages; if RMS phase error is high for 6-bit operation, correction states can be used to lower phase error. If no error correction is required due to concluding with required level of phase resolution, mentioned states can be used for 7^{th} bit of phase shifter. Constructed phase shifter has 6.75GHz bandwidth for 6-bit of operation, while it is 4.5GHz for 7-bit operation. Minimum loss is -10.5dB at 10GHz, while consuming at most 141.5mW of power. Designed hybrid phase shifter consumes 6.27mm^2 area, including pads; when additional LNA is excluded total area decreases to 4.96mm^2, which is low in compared with passive phase shifter approaches.

4.2. Future Work

There exists a significant deviation between simulation and measurement results, which results with a major degradation in design performance for LNA. One of the main reasons for mentioned degradation can be low collector current; which results with failure in first steps of the design. Actually, there is no such DC variation in designs, when dies with other technologies are measured with using same measurement setup. If

this phenomenon is occurring as a result of the process itself, then its parasitic model should be added to simulator; with that manner, much correlated results can be obtained. Two-stage cascode LNA is designed with using a different foundry's technology; as a result such a variation is not expected.

Described methodologies that is used for high dynamic range LNA, can be fitted to Power Amplifier (PA). Due to being limited with breakdown voltage levels, achieving high output power is a significant concern for 0.13μm SiGe technology. Scaling devices with regarding breakdown voltage limitations, and raising voltage swing of CB amplifier up, without concerning the CE breakdown voltage can result with high output power, which is a requirement of overall T/R module.

Hybrid phase shifter approach is selected to end up with high dynamic range and high phase resolution in wideband frequency range. Total T/R Module structure requires about -10dBm of input-P1dB, as a result a phase shifter with high input-P1dB would be sufficient for achieving expected linearity for T/R Module. In other meaning, forming different hybrid structures can perform lower dynamic range, but higher bandwidth or lower phase error. Described hybrid phase shifter has two concerns that can be improved; high loss, and large area. 5^{th} bit is the block that causes high gain error and high loss. Better loss and gain error performances can be achieved with using RC polyphase filters. On the other hand, forming LSB with active circuitries can decrease area consumption, with sacrificing linearity.

When performances between III-V and SiGe devices are compared, there exists a major gap, especially in terms of output power. As in hybrid approach of phase shifter, both technologies can be used together to form a superior T/R module. III-V devices have better performance in terms of NF and output power, whereas other performances can also be achieved with SiGe technology also. Instead of constructing all blocks in III-V technology, only LNA and PA would satisfy the requirements, while SiGe-based LNA and PA blocks can still be in use to improve performance. With that way cheaper, compact and light T/R module designs can be obtained, without sacrificing the performance. Recent studies demonstrate that III-V and SiGe HBT technologies can be integrated together, without any degradation in technologies [63].

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