Low-power LVDS for digital readout circuits

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ABSTRACT

This paper presents a mixed-signal LVDS driver in 90 nm CMOS technology. The designed LVDS core is to be used as a data link between Infrared Focal Plane Array (IRFPA) detector end and microprocessor input. Parallel data from 220 pixels of IRFPA is serialized by LVDS driver and read out to microprocessor. It also offers a reduced power consumption rate, high data transmission speed and utilizes dense placement of devices for area efficiency. The entire output driver circuit including input buffer draws 5mA while the output swing is 500mV at power supply of 1.2V for data rate of 6.4Gbps.Total LVDS chip area is 0.79 mm^2. Due to these features, the designed LVDS driver is suitable for purposes such as portable, high-speed imaging.

Keywords: High performance data serialization, low-power integrated circuit, low-voltage differential signalling (LVDS), input/output drivers

1. INTRODUCTION

The scaling down silicon technology enables a variety of devices such as microprocessors to operate faster. However off-chip data transmission technologies cannot be simultaneously improved since greater data transmission rates cause an increase in cost of IC packaging and thermal performance of the circuitry [1]. In addition to this, power consumption of the data transmission structure is vital for the battery life of portable systems.

Low-voltage differential signalling (LVDS) is a differential transmission and termination method which provides power saving with wide bandwidth of data transmission when compared to regular methods. Additionally, differential operation mode of LVDS offers multiple benefits such as; robustness of link to supply and oscillation of common-mode, reduction of electromagnetic interference and coupling. Since LVDS drivers can provide data serialization with the aforementioned features, they are utilized in a wide range of application fields such as: image processing, computation, telecommunications etc.

IEEE 1596.3-1996 standard LVDS driver output signal swing is expected to be centred at 1.25 V and the accepted swing range is from 250 mV to 400 mV. Receiver side has differential load and the source end has a termination resistor to minimize reflection of waveforms especially at higher speeds of data transmission.

In the literature, there are multiple LVDS core topologies which offer different benefits and, therefore, a spectrum of applications. Bridged-switched current sources (BSCS), double current source (DCS), switchable current source and open-drain architectures are commonly used topologies of LVDS drivers. BSCS and DCS topologies utilize two current sources implemented on the core of LVDS driver. In BSCS topology, the polarity of the input pulse and the complimentary of the input pulse turn switches on and off, creating a current flow in varying directions.

In DCS, the input pulse determines which NMOS switch to turn on and off and the current flows from the two current sources with varying direction. In both architecture, the variation of the current direction creates an output voltage swing on the common-mode voltage level.Open-drain (OD) and switchable current source (SCS) topologies similarly utilize a single source. Although it has a single current source, OD is noted to be the highest current consuming topology in literature [2]. On the other hand, SCS utilizes two PMOS current sources switching depending on the input pulse. Therefore, SCS architecture offers a high output voltage swing and a low power consumption compared to other topologies.

There are various studies in the literature about implementation of LVDS in different technologies. In 0.35 micron technology with 1.8 V supply usage, Chen et al [3]. switchable current source LVDS driver provides 340 mV peak to peak swing with a static power consumption of 23 mW. The maximum data serialization rate available to this system is

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1.4 Gbps. In 0.18 micron, LVDS driver designed by Lu et al.[4] consumes 4.4 mW at the data rate of 1.25 Gbps with a single-end output swing of 203-288 mV. This driver possesses a 1.8 V supply voltage and can go up to 4.25 Gbps and it is an all-digital LVDS driver. Another work in the literature in 0.18 micron technology is [5] work which use a source coupled logic topology and no internal termination resistance to avoid extreme power consumption. This work is optimized for 250 MS/s operation and it consumes 7.2 mW with a peak to peak swing of 400 mV.

This paper presents design overview of a mixed-signal LVDS driver in 90 nm CMOS technology. The designed LVDS core is to be used as a data link between Infrared Focal Plane Array (IRFPA) detector end and microprocessor input. Parallel data from 2^{20} pixels of IRFPA is serialized by LVDS driver and read out to microprocessor. It also offers a reduced power consumption rate, high data transmission speed and utilizes dense placement of devices for area efficiency. Due to those features, the designed LVDS driver is suitable for purposes such as portable, high-speed imaging. Additionally, the design offers a wide range of temperature of operation. It can provide fast data transmission at room temperature and within cryogenic temperature range.

2. DESIGN FUNDAMENTALS

2.1 Switchable Current Source LVDS Core

Switchable current source LVDS core consists of two PMOS current sources turning on and off with respect to input pulse. Changing polarity of the current flowing on the differential load creates voltage swing. Differential load resistor is symmetrically divided into two 50 Ohm resistors and the common mode voltage is set to 600 mV via a feedback loop. To generate a 500 mV peak to peak swing, 2.5 mA current must flow through the differential load resistor and the 100 Ohm termination resistor as well. Therefore, PMOS transistors must be able to drive high amount of current and possess large device sizes. Following the PMOS drivers and differential load resistors, NMOS transistors are used as switches to prevent or permit the current flow through the legs by turning off and on with respect to input pulse. At the bottom of the circuit, an NMOS transistor S_3functions as a current sink which needs to flow 5 mA of current to ground. The input voltage of current sink is a function of the common-mode node and set by common-mode feedback loop.

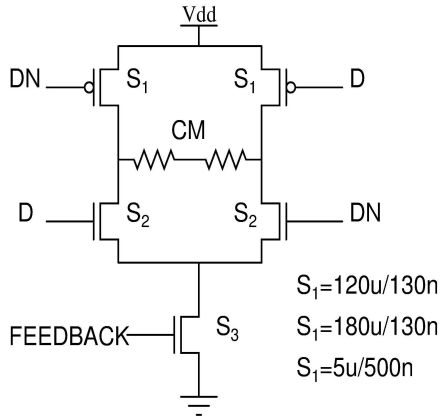

Figure1. The switchable current source LVDS core

2.2 Common-mode Feedback

Common-mode feedback loop consists of a 30 dB gain and 57.5 MHz bandwidth single stage operational amplifier. Op-amp generates output voltage of 489 mV when common-mode node reaches 600 mV. This op-amp takes the open common-mode node and the 600 mV reference voltage as inputs and compares them. Output of the op-amp drives the gate of NMOS current sink connected to LVDS core [6].

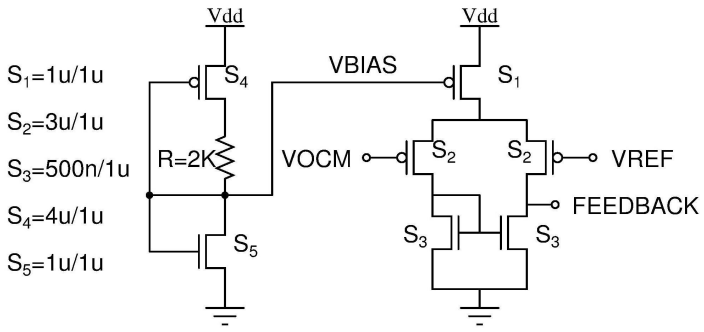

Figure 2. Single stage common-mode feedback amplifier

2.3 Passive Pull Up/Down Circuitry

Passive pull up and down circuitry is utilized to provide wider bandwidth of operation to LVDS core. Since the device sizes are large, it is hard to charge and discharge each and every node by a swing of 0-1.2 V in the gates of PMOS current sources. It is therefore required to use a pull up and down circuitry to narrow down the gate swing of PMOS drivers. Since the power efficiency is another crucial performance specification, a passive pull up and down circuitry is more preferable compared to an active one.

Passive pull up and down circuitry consists of a capacitor and an op-amp connected in buffer fashion to determine the minimum value of the swing and drive the gate to this value.

In the case of HIGH input to the gate, driver works as a basic voltage divider and distributes this voltage level in accordance with gate capacitance and passive capacitor value. In the case of LOW input to the gate, negative feedback connection of op-amp drives the gate to 600 mV and prevents this node from going below this level. The op-amp has a wide bandwidth requirement since it is required to drive the gate to its minimum value depending on the pulse input to the system.

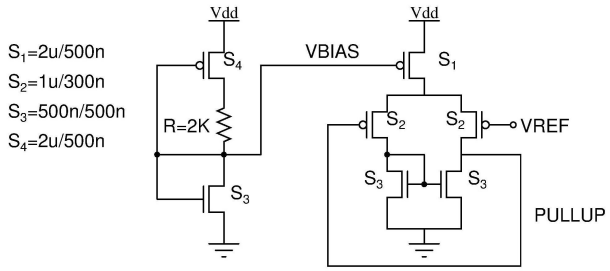

Figure 3. Op-amp connected in buffer fashion. The op-amp drives the transmission gates.

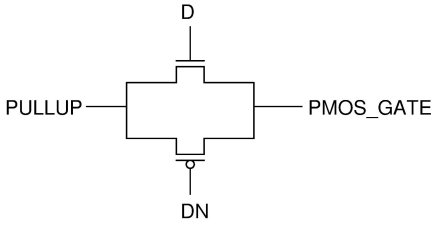

Figure 4. Transmission gates used in the system are driven by the input pulse and its complimentary signal.

2.4 Low Power and Operating Temperature Design

The study has two prior aims for sake of novelty; low power consumption and operation at cryogenic temperatures. LVDS core consumes the highest amount of current within the overall system. Therefore the switchable current source topology and a low-voltage supply are used in the system to reduce the power consumption. The switchable current source, as explained in former sections, utilizes one PMOS current source and an NMOS sink which are controlled by the digital input pulse and the common-mode feedback respectively. The challenge is to operate PMOS transistors in saturation mode of operation since their drains are already driven by a low-voltage supply. Additionally, the PMOS gate swing is limited and a buffer drives the gate to 600 mV, the reference voltage of overall system, in the case of digital LOW input. TSMC regular P MOS transistors offers -379.9 mV of threshold voltage, the ultra-low threshold voltage devices has a threshold voltage of -292.4 mV which is approximately 90 mV higher. Therefore, ultra-low threshold voltage PMOS is preferred to acquire fast switching speed in addition to low power consumption. The sizing of PMOS devices and the sink is particularly crucial in order to provide the system the required driving strength. PMOS current sources must have high aspect ratio in order to drive 5 mA due to narrowed down gate swing. To minimize the area of the core, the largest sub-block, the channel length of the PMOS current sources and the NMOS switches are selected to be the shortest possible. However, channel length of the NMOS sink is chosen to be 500 nm to avoid possible current leakage and process related deviations in order to guarantee a robust flow of 5 mA of current in the core.

Low operation temperature design mainly utilizes a voltage reference which can operate within cryogenic temperature range. Ability to perform a robust operation within cryogenic temperature ranges, from -196 ºC to -146 ºC, is a novel feature of the proposed LVDS driver. The voltage reference circuit for LVDS designed separately consist of CMOS devices only.

3. SIMULATION RESULTS

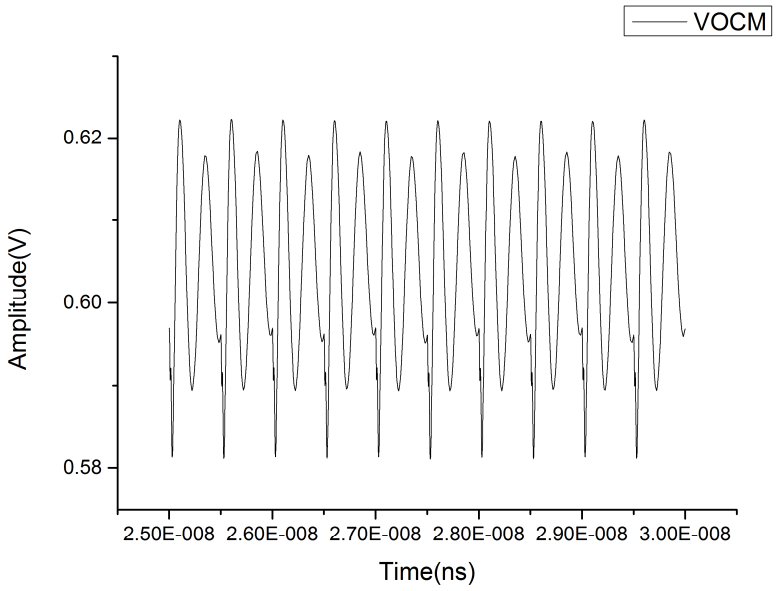

Figure 5. Transient response of common-mode signal at room temperature for a 1 GHz input clock

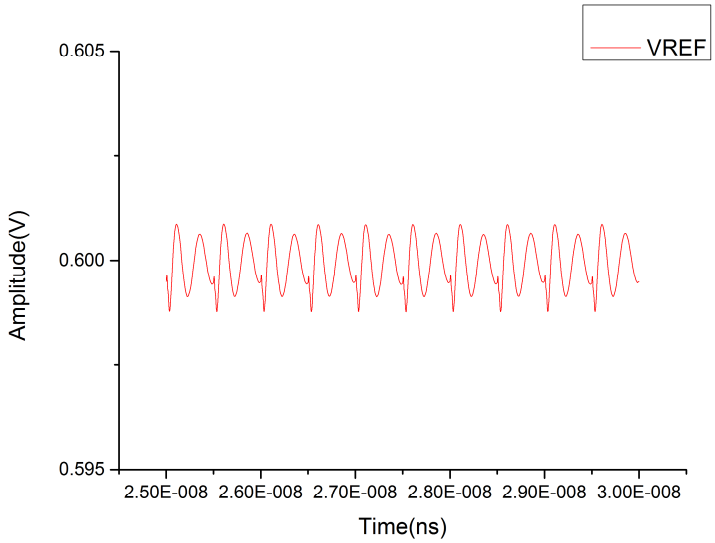

Figure 6. Transient response of voltage reference signal at room temperature for a 1 GHz input clock

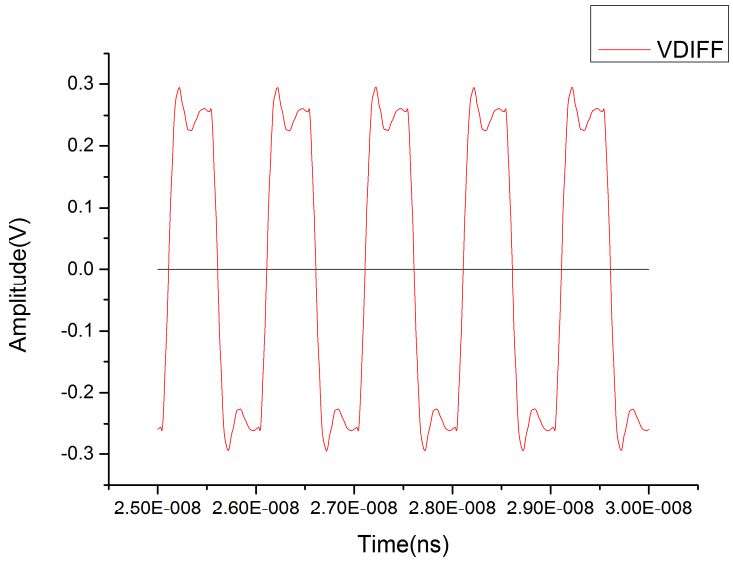

Figure 7. For 1GHz input clock output voltage swing at room temperature. Receiver end and transceiver end resistors are matched using the built-in MTline models of Cadence**.**

Slew rate of the differential output signal measured at room temperature for a gigabit-per-second rate of data input is 6.4E+9 V/ns which is approximately twenty times above the IEEE standard. Differential output signal has a 500 mV peak to peak swing and it swings around 600 mV the common mode voltage level of the system.

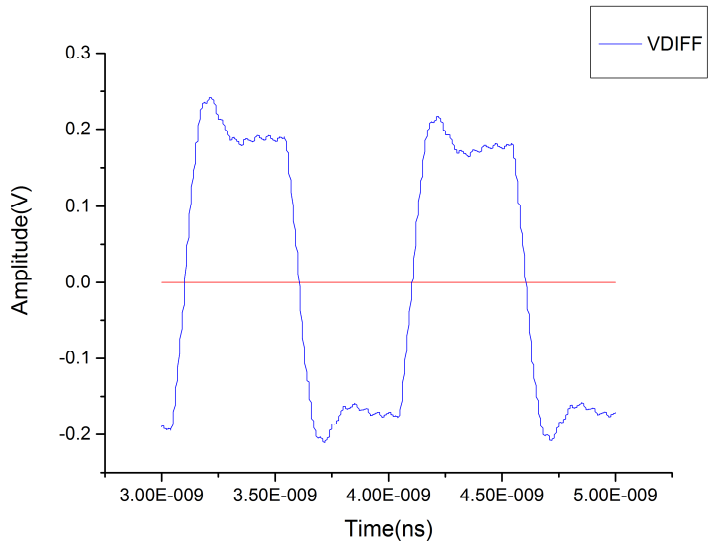

Figure 8. For 1 GHz input clock output voltage swing at -196 °C . Peak to peak voltage swing is approximately 450 mV.

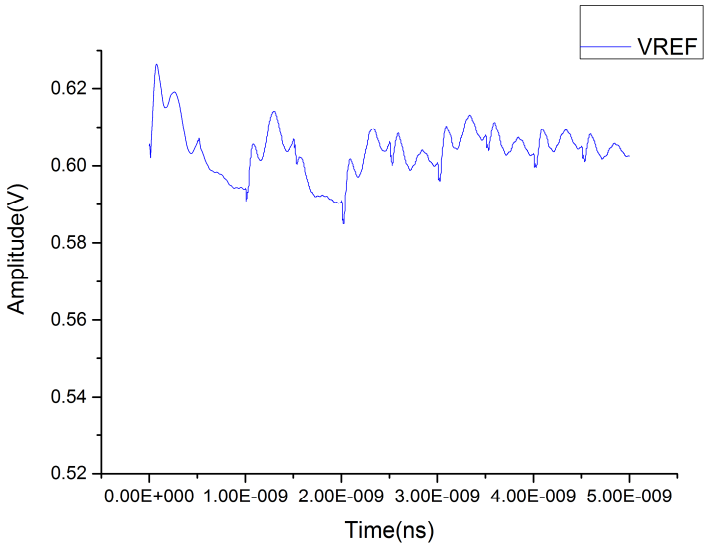

Figure 9. Transient response of voltage reference signal at -196 °C for a 1 GHz input clock

4. CONCLUSION

Slew rate of the differential output signal measured at room temperature for a gigabit-per-second rate of data input is 6.4E+9 V/ns which is approximately twenty times above the IEEE standard. Differential output signal has a 500 mV peak to peak swing and it swings around 600 mV the common mode voltage level of the system. In this paper, a low-power LVDS circuit for serial link applications has been presented. The proposed circuit includes switchable current source LVDS core along with passive pull up/down circuitry and hence reducing the power consumption of over-all LVDS. The output driver circuit along input buffer draws only 5mA current at 1.2V power supply. The output has swing of 500mV at 6.4Gbps which is approximately twenty times above the IEEE standard.

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