

4-Bit SiGe Phase Shifter using Distributed Active Switches and Variable Gain Amplifier For X-Band Phased Array Applications

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Abstract—This paper presents a 4-bit digitally controlled phase shifter for X-band (8-12.5 GHz) phased-arrays, implemented in 0.25- μm SiGe BiCMOS process. Distributed active switches are utilized in first three bits. On-chip inductances are used to provide 22.5° phase shift steps. The placement and the geometry of these inductances are optimized for minimum phase error and insertion loss. In order to compensate the gain variations of this stage, a single stage variable gain amplifier is used. The fourth bit which provides 0/180° phase shift is obtained in third amplification stage, with switching between common base - common emitter configuration. With utilization of this technique overall phase error is significantly decreased and overall gain is increased. The phase shifter achieves 7dB gain with 3 dB of gain error. 360° phase shift is achieved in 4 bit resolution with a phase error of 0.5° at center frequency of 10GHz, and maximum 22° phase error in 4.5 GHz bandwidth. The chip size is 2150 μm x 1040 μm including the bondpads. These performance parameters are comparable with the state of the art using similar technology.

Keywords — Phase shifters, BiCMOS, Radar, phased arrays, Transceivers, Distributed amplifiers.

I. INTRODUCTION

Transmit/receive modules are essential parts of modern phased arrays to achieve fast beam scanning and electronic beam control functions. These modules determine overall performance of phased arrays. A simple block diagram of a T/R module is shown in Fig.1, which consists of a power amplifier, a low noise amplifier, two single-pole double-throw (SPDT) switches, a T/R switch and a phase shifter which is one of the key components of a T/R module with determining the phase resolution of the system, [1]. III-V technologies are chosen for implementation of phase shifters due to its high performance requirements. However, recent developments in silicon process technologies enabled design of Si-based highly compact and low cost phase shifters, [2].

In this paper a 4 bit digitally controlled phase shifter using distributed active switches is presented. The circuit is designed in 0.25 μm SiGe BiCMOS. Distributed amplifier technique is applied in design of the first three bits, [3]. As a novelty in this work, fourth bit is a 180° phase shifter based on switching between common base (CB) and common emitter (CE) amplifiers, rather than switching between high pass (HP) and low pass (LP) filters. Secondly, due to their high f_t/f_{max} values, set of npn-HBTs are used in order to decrease the

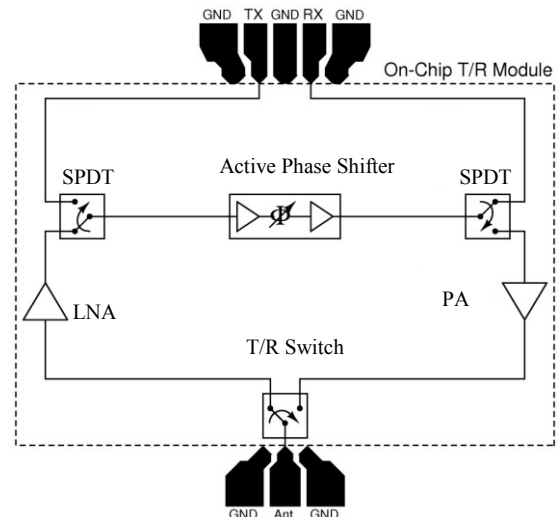


Figure 1: Simple block diagram of a SiGe BiCMOS On chip T/R module

number of cascaded amplifier stages and power consumption. Thirdly, variable gain amplifier is utilized to compensate gain variations in phase shifter. All of the inductors and interconnections are simulated using Sonnet®. Proposed 4 bit phase shifter is designed for high gain, low power consumption and relatively low phase error.

II. CIRCUIT DESIGN

Fig. 2 a. shows the proposed phase shifter topology, which consists of eight stage of cascaded ladder network with series inductors and shunt capacitances. The phase shift per section can be derived as $\Delta\phi \approx \omega\sqrt{LC}$, [3]. L and C values are optimized in order to provide 22.5° phase shift for each step. This equation also shows that the phase shift is valid for single frequency but there will be phase error for wide bandwidths. Therefore, this topology can be utilized for a limited bandwidth, which is 4.5 GHz for this work. The number of LC stage (NoS) is selected as eight because lower NoS increases rms phase error [2] and higher NoS increases parasitics and area. To determine phase shift, the base voltage of selected HBT ($V_{p1}-V_{p8}$) is set to VDD while the rest is set to GND. LD1- LD2 and C1-CD2 values are optimized for interstage matching.

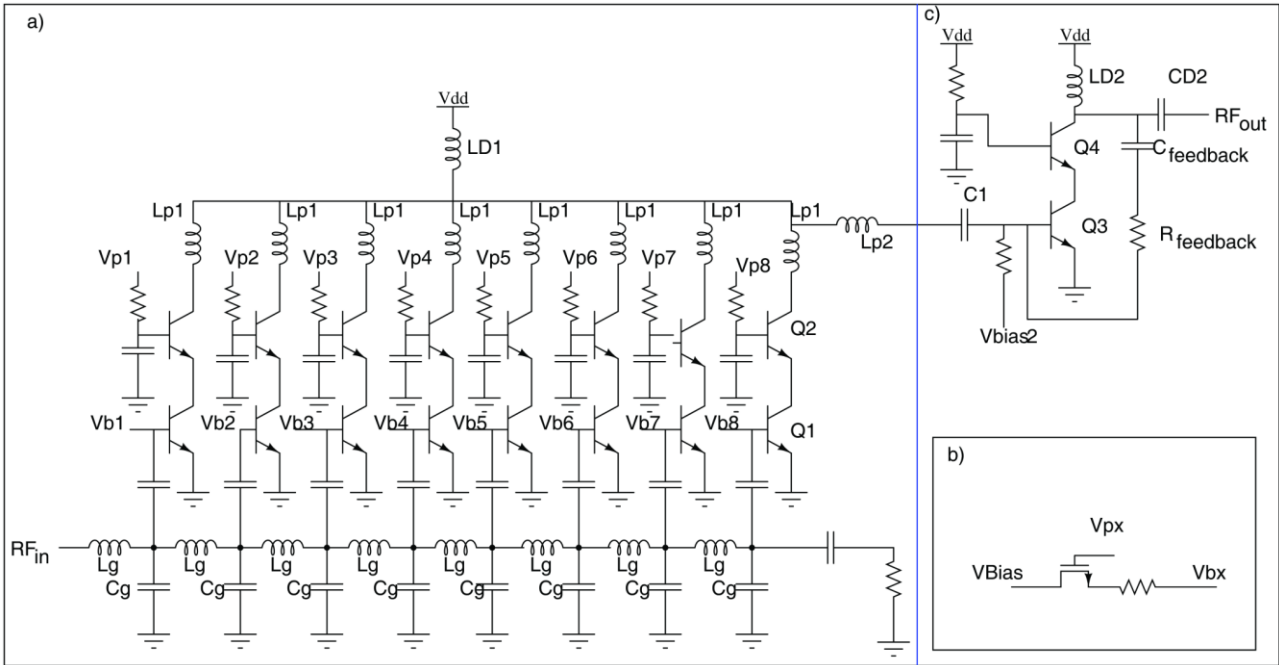


Figure 2: a) Schematic of BiCMOS phase shifter using distributed active switches b) Schematic of VGA c) bias circuit to minimize base current for off state.

Fig 2.b shows the biasing circuitry which is used to minimize the base current of driver HBTs (Q1) when the pair is not selected. Fig 2.c shows variable gain amplifier which is designed to compensate the gain variations in first stage. Here an R-C feedback is used in order to increase the bandwidth of the amplifier for matching. However, gain is reduced.

The fourth bit, 0/180° phase shifter is based on selection between CE and CB stages which is represented in Fig. 3. In order to obtain 180° phase shift, vc and vcb are set to GND and VDD respectively. In this state, CE circuit is biased while no current flows on CB. Similarly, for 0° phase shift vc and vcb are set to VDD and GND, respectively, to provide required bias conditions of CB state and cut the current of CE. For this circuit, for two phase states, two different input impedances are obtained. The input matching circuits which is formed by C₁, C₂, C₃, L₁, R₁, R₂ and are optimized to achieve more than 10dB return loss. Similarly, output matching circuit is constructed with L_{load}, R_{load} and C_{load}. Gain variation for two different configurations is also minimized. In this 180° phase shifter stage, 1° phase error is achieved in 4 GHz bandwidth and 2dB Gain with 0.2 dB gain variation is obtained in post layout simulations.

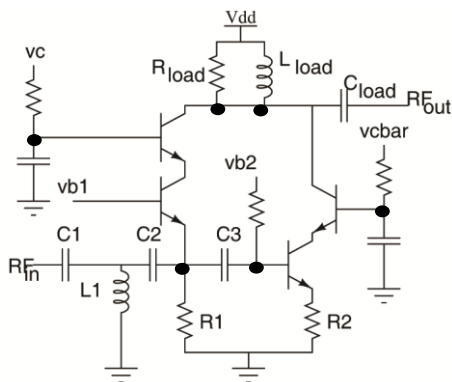


Figure 3: Schematic of active 0°/180° phase shifter

The die photo of complete circuit can be seen in Fig.4. To reduce inductance variation, interconnection loss and enhance quality factor; on chip inductors and high-Q MIM capacitors are utilized. Their values are also optimized to provide differential phase shift. Placement and geometry of these passive components are optimized to minimize loss and area. Furthermore, variations in values of parasitic inductances which are resulted from the interconnection are minimized. These inductances are represented as Lp1 in Fig 2.a. The inductance values, coupling between passive components are simulated and optimized.

III. MEASUREMENT RESULTS AND COMPARISON

Difference between insertion phases of each state at 8-12.5 GHz bandwidth is shown in Fig. 5. The phase shift at 10 GHz is incremented in 22.5° steps. RMS phase error is shown in Fig. 6. The relative phase difference varies with frequency, therefore, the circuit is optimized to provide minimum phase error (0.5°) at center frequency (10 GHz), however, maximum rms phase error (22°) is observed at edge of the frequency band (8.5-12.5 GHz). The electromagnetic model inaccuracies and high coupling between the inductances which are very close to each other due to compact layout caused the difference between post layout simulation and measurement results. In addition, phase difference of VGA varies with bias voltage,

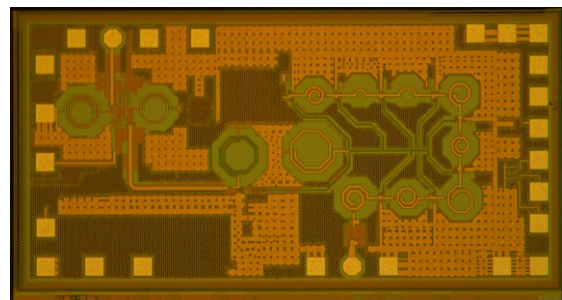


Figure 4: Die photo of the Phase Shifter 2050x1040 μm

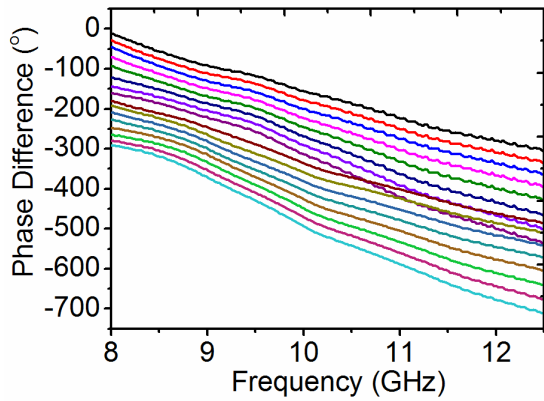


Figure 5: Measured relative phase shift for all 16 states

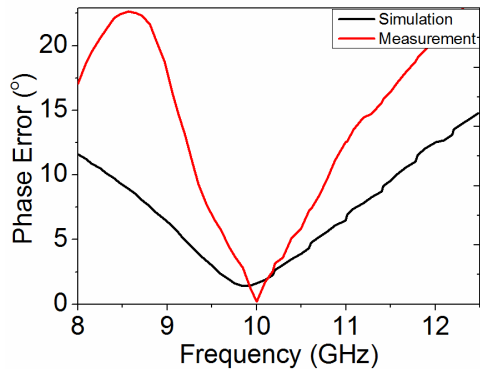


Figure 6: Simulation and measurement Results for rms phase error

and this variation is utilized to minimize this phase error at the cost of gain error. It is shown in Fig 7 that input and output return losses are more than 10dB. As shown in fig. 8, 7 dB average gain 0.3dB gain variation is observed in 10GHz. 3 dB gain error is measured in 16 different phase states in 4.5 GHz bandwidth.

Recently reported phase shifters in silicon process and post layout simulation results of this work are compared in Table 1. HP/LP filter switching based phase shifters utilizes passive switches with their high insertion loss (IL) [4, 6]. These passive phase shifters do not consume power, however, cascaded power hungry amplifiers are needed to compensate this IL. Active quadrature generator based phase shifters exhibit low rms phase error with wide operating frequency range however the power consumption is significantly high due to additional circuits which are required to control VGA [5]. These additional circuits also increase the design complexity. [2] is a very similar work, however its configuration based on NMOS transistors consume significant amount of power to provide lower gain. As a result, the work presented in this paper achieves comparable rms phase error (for 9.5-10.5 GHz), higher gain, lower gain variation (compensated with a VGA), reasonable power consumption with its 4 bit digital control, in comparison with similar works in literature. RMS phase error at 8-12.5 GHz is lower than least significant bit therefore this phase shifter can be used in this bandwidth.

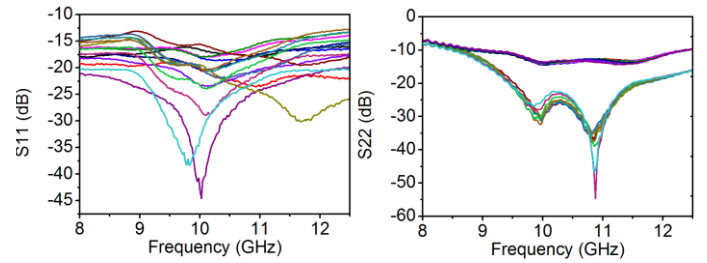


Figure 7: Measurement results for input and output return loss

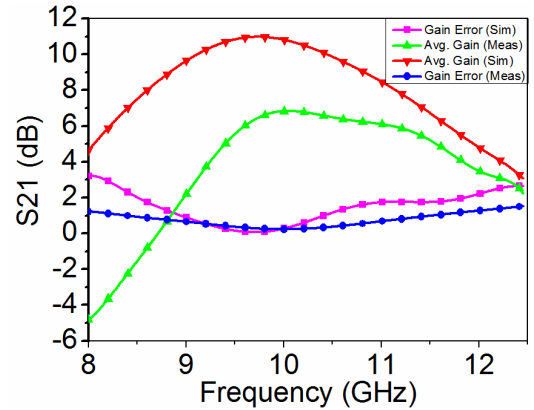


Figure 8: Simulation and measurement results comparison for average gain and gain Error

IV. CONCLUSION

In this paper a 4 bit phase shifter in 0.25- μm SiGe BiCMOS process technology is presented. 3 bit distributed phase shifter is cascaded to a VGA which is connected to CB-CE amplifier selection based active 0/180° phase shifter. Small chip area and high gain is achieved while gain and phase variation is compensated with a single stage VGA. Measurement results show that overall gain is at 7 dB at 10GHz with a DC power consumption of 28mW. RMS phase error is less than 22° over 4.5 GHz bandwidth, and lower than 5.8° at 1GHz bandwidth. The phase shifter is appropriate for on-chip phased array systems.

TABLE I. COMPARISON OF SILICON PHASE SHIFTERS

Process	Freq GHz	Ph. Error (°)	Gain dB	Phase range	Area mm ²	DC pow. mW	Ref
180 nm CMOS	11.6-12.6	5.5	3.5 ±1.2	360° (4-bit)	1.7	26.6	[2]
SiGe HBT	8-12	2	-12 ±2	360° (4-bit)	0.9	-	[4]
180 nm SiGe HBT	6-18	5.6	18 ±1.5	360°	0.18	62	[5]
45 nm CMOS	60-67	3	-6	360° (3-bit)	0.6	-	[6]
SiGe HBT	8-12.5	22	4± 3	360° (4-bit)	2.2	28.2	This Work
SiGe HBT	9.5-10.5	5.8	7± 0.3	360° (4-bit)	2.2	28.2	

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