A VERILOG HDL DIGITAL ARCHITECTURE FOR DELAY CALCULATION

A. CHACÓN-RODRÍGUEZ†, F. N. MARTÍN-PIRCHIO‡, P. JULIÁN‡§ and P. S. MANDOLESI‡

† *Laboratorio de Componentes Electrónicos, Universidad Nacional de Mar del Plata, Mar del Plata, Argentina, on leave from Instituto Tecnológico de Costa Rica.*
achacon@fi.mdp.edu.ar
‡ *Departamento de Ingeniería Eléctrica y Computadores, Universidad Nacional del Sur, Bahía Blanca, Argentina*
§ *Consejo Nacional de Investigaciones Científicas y Técnicas-*(*CONICET*)
fmartinpirchio@uns.edu.ar, pjulian@uns.edu.ar, pmandolesi@uns.edu.ar

***Abstract*— A method for the calculation of the delay between two digital signals with central frequencies in the range [20, 300] Hz is presented. The method performs a delay calculation in order to determine the bearing angle of a sound source. Computing accuracy is tested against a previous implementation of the Cross Correlation Derivative method. A Verilog RTL model of the method has been tested on a Xilinx® FPGA in order to evaluate the real performance of the method. Simulations of an ASIC design on a standard CMOS technology predict a power saving of about 25 times per delay stage over previous implementations.**

***Keywords*— Verilog, FPGA, low power, digital CMOS VLSI.**

I. INTRODUCTION

Methods for the detection of sound sources have been widely studied, including the use of complex techniques such as Independent Component Analysis, Cross-correlation analysis (Carter, 1987; Knapp and Carter, 1976; Riddle, 2004), Gradient Flow techniques (Stanacevic and Cauwenberghs (2005), and the emulation of the human hearing cochlea (Shamma *et al.,* 1986; Lazzaro and Mead, 1989; Horiuchi, 1995), some of which have been successfully implemented in analog and digital VLSI circuits (Lazzaro and Mead, 1989; Horiuchi, 1995; Harris *et al.,* 1999; Grech *et al.*, 1999; van Schaik and Shamma, 2004). There are only a few cases in the literature where low power integrated circuits have been implemented for this task. Van Schaik and Shamma (2004) implemented an integrated circuit (IC) based on an analog cochlea using a 0.5μm process in an area of 5 mm^2. In this case, the power dissipation depends strongly on the input signals. With no activity, the cochlear channels dissipate 400 μW; for a time delay of 100 μs (corresponding to a 77 ° angle incoming signal), the power dissipated is 1.85 mW. Stanacevic and Cauwenberghs (2005) implemented a 3 mm by 3 mm, 0.5μm CMOS technology IC with a method based on analog processing at a sampling rate of 16 kHz, which discriminates 2 μs with a power consumption of 32 μW. A third implementation, proposed in Julián *et al.* (2004) and successfully implemented in Julián *et al.* (2006), is based on a cross-correlation derivative algorithm. This method features an accuracy of one degree for angles in the range = [0,50] U [+130,+180] for signals between [20 Hz, 200 Hz], using two detectors (i.e. four microphones) to cover the whole 360 degrees without accuracy loss. The integrated circuit (IC) designed by Julián *et al.* (2006), allows for this with less than 600μW of power dissipation (for a full quadrant bearing estimation) on a 0.35μm technology with measures of 2 mm by 2.4 mm.

An alternative method for the estimation of such angle is proposed in this paper in order to reduce power dissipation still further, while keeping calculation performance. The problem is to determine the direction of a sound source picked by an array of microphones such as the one in Fig. 1. The digital signals are provided from this array after being conveniently conditioned. The cross-correlation derivative (CCD) approach is a variation of the standard time-domain cross-correlation between two signals. The CCD algorithm works with a one bit discrete quantization of the input signals, and therefore, reduces drastically the complexity of the resulting digital circuitry. Another feature is that the spatial derivative of the cross-correlation is calculated instead of the cross-correlation itself. Calculation of the CCD results in an activity reduction of a thousand times in the digital circuitry. In the case of the standard cross-correlation approach, once the partial correlations are calculated, the maximum needs to be evaluated which requires a dedicated stage. In the CCD, it is only necessary to locate a change in the output value of the partial correlations (which are either 1 or 0), making this task trivial: one only needs to detect transitions of the input signals.

The strategy proposed in this paper is to use a single counter for delay measurement together with an adaptive closed loop system. The closed loop guarantees stability, and also a convergence of the counter count to the delay under measurement. The reduction of power consumption is a consequence of the reduction in size of the circuitry. In fact, just one counter is needed as opposed to the 104 10-bit counters used in the implementation proposed by Julián *et al.* (2006).

The paper is organized as follows. Section II describes the Verilog HDL front-end implementation of the proposed structure for the detection of transitions