REDUCTION OF TOTAL HARMONIC DISTORTION IN POWER INVERTERS

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***Abstract*— The output voltage of PWM power inverters shows harmonic distortion due to several causes; the main ones are the modulation algorithm, nonlinearities in the output filter, dead times, voltage drops across the switches and modulation of the dc bus voltage. The distortion is more evident when using low dc bus voltages. As a result, motors driven by these inverters have important torque pulsations. This work proposes to reduce the distortion produced by dead times and voltage drops across the switches using a simple algorithm that recalculates the width of each PWM pulse, while preserving the ideal area. By simulation, the THD was reduced from 18% to 0.29% in a single-phase inverter. The proposed algorithm only needs products and sums, so it is suitable for being implemented on a DSP with a very low processing load.**

***Keywords* — Power inverter, distortion, blanking time, THD.**

I. INTRODUCTION

A single-phase PWM power inverter is shown in Figure 1. By turning on exclusively one switch in each leg (M1 and M4, or M2 and M3) a voltage difference is produced across points A and B. Simultaneous turning on of the two switches of either leg must be avoided to prevent a short circuit to ground on the dc-link. The natural turn-on and turn-off delays of the switches increase the possibility of producing the short circuit. A *delay time*, also called dead time (DT), is added before applying the turn-on pulse on any switch to minimize this risk; such that the previous conducting switch of the same leg has effectively turned off. Arbitrary waveforms can be synthesized between points A and B by adequate modulation of the turn-on pulse widths. The low-frequency spectrum of the synthesized waveform is similar to the desired one.

The most important sources of distortion in power inverters are: the kind of modulation used, nonlinearities in the output filter, dead times, the direct Voltage Drop across the Switches (VDS) and modifications of the voltage of the dc-link. The standard measure used to characterize distortion is the total harmonic distortion (THD).

Distortion due to DTs: The DTs are normally introduced at the beginning of each pulse, delaying the turning

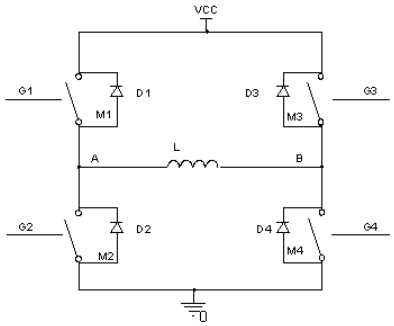

Figure 1. Full bridge inverter with inductive load.

on of the respective switch, to allow the other switch to effectively turn off (Mohan *et al.*, 1989). Distortion caused by the DTs has already been studied. In Mohan *et al.* (1989) and Mosely *et al.* (1999) a basic description of the problem and its influence over the THD of the output waveform can be found. Since during the DT both switches of the same leg are off, the sign of the output current dictates which of the freewheeling diodes conducts. In consequence, when the current is negative (positive current flows from point A to point B in Fig. 1 by convention) the average output voltage is higher than desired. On the contrary, when the current is positive the average output voltage is lower than desired. Then the output waveform is distorted, with low-order harmonic components that are difficult (or relatively expensive) to filter out.

According to Mosely *et al.* (1999), the ratio (Period/DT) must be > 15 or the DT < 6.7% of the period to keep the THD below 1%.

The problem has been extensively investigated (Ueda *et al.*, 1982; Chin, 1985 and Ueda *et al.*, 1989) with respect to the torque pulsations produced on the electric motors by the distorted waveforms. Several correction methods have been proposed to correct the distortion produced by the DTs; Murai *et al.*, 1987; Jeong & Park, 1991; Colby *et al.*, 1990, Choi *et al.*, 1994; Mohan *et al.*, 1989; Mutoh *et al.*, 1990 and Sukegawa *et al.*, 1991). Most of them are based on the mean value theory. The lost voltage is averaged along one switching interval and used to compensate the command voltage (Murai *et al.*,

1987, Jeong and Park, 1991; Colby *et al.*, 1990; Choi *et al.*, 1994). One technique uses a PI Controller to adjust the compensation time (Choi *et al.*, 1994), while another one corrects the pulse widths by detecting the direction of the power flow (Mutoh *et al.*, 1990). Other technique (Sukegawa *et al.*, 1991) uses a feedforward method applied in high performance current-mode variable speed drives, while another (Leggate and Kerkman, 1997) proposes a pulse-by-pulse compensation that adjusts the PWM symmetric pulses to correct the voltage distortion due to the DTs.

Our proposed DT compensator performs pulse-by-pulse compensation by adding a compensating pulse at the end of each original pulse to yield the ideal pulse area. The polarity of the load current has to be known. The correction is independent of the carrier and modulator frequencies.

As shown in Choi *et al.* (1999), when unidirectional switches are used, not all DTs are necessary. The DTs are only necessary when producing command pulses near the zero-crossing of the load current. An analysis of the different operating modes of the inverter reveals that a switch is not always switched on when it receives a switch-on command. The switch turns on only when the load current changes polarity; in all other cases, the corresponding diode will conduct the current and the inverter can be driven without DTs. The DTs are necessary only when the output current is near zero. A limit ΔI can be established such that if $|I| > \Delta I$, no DTs are generated. When a sinusoidal waveform is synthesized (e.g., in variable speed drives) the zero crossing of the current can be predicted, minimizing ΔI. When $|I| < \Delta I$, the DTs and all signals must be generated, since the current can switch polarity at any time. Elimination of the unnecessary DTs improves the global efficiency of the inverter, since a great amount of gate pulses is eliminated. Additionally, the THD of the output voltage is reduced noticeably.

Distortion due to VDS: The ideal PWM modulator calculates the pulse widths based on three possible amplitudes for a two-level inverter: $\{V_{cc}, 0, -V_{cc}\}$. These voltage values are never attained in practice.

When the sign of the current is positive (SI = 1) and the sign of the voltage is positive (SV = 1), current flows through M1 and M4. Considering that the voltage drop V_{on} on the MOSFETS are equal and constant, then the resulting voltage on the load is $V_{cc}-2V_{on}$. When SI = –1 and SV = –1, current flows through M2 and M3. In this case, the voltage on the load is $-V_{cc}+2V_{on}$. When SI = 1 and SV = 1 there are two possible ways for generating the DTs: one is to turn off M1 leaving M4 on, which makes the current to flow through D2. The other is to turn off M4 leaving M1 on, and the current flows through M1 and D3. In both cases the load voltage is $-V_d-V_{on}$. Finally, the zeros generated by M1 and M3, or M2 and M4 have amplitude $\pm(V_d+V_{on})$, being positive for SI=–1 and negative for SI=1.

Table 1 shows the inverter operation considering the effects of the DTs and the VDSs, simultaneously (for VDS equal to V_{on} under unipolar PWM). For unipolar PWM, there are four pulse sequences that are repeated while the polarities of voltage and current do not change. Table 1 shows the corresponding repetitive uncompensated waveforms of each sequence. Each pulse is identified by the triggering signal of the switches that should conduct (e.g., G2G4), and also the amplitude is identified (e.g., $-V_d-V_{on}$).

The output voltage can adopt four different values, corresponding to positive (HI), zero (0), negative (LO) and the value adopted during the DT, that can be HI, 0 or LO, depending on the signs of the voltage and current.

For the sequence {SV = –1, SI = 1} the ideal output should switch between 0 and $-V_{cc}$.

However, the real voltage level corresponding to 0 is $-V_d-V_{on}$. Similarly, the real voltage level corresponding to LO is $-V_{cc}-2V_d$. During the DT the output goes to the LO state. The DT is always inserted at the beginning of the state, reducing its effective duration. When the voltage during DT is different than the desired value, then the DT produces an error. For example, in the sequence {SV = –1, SI = 1}, the output voltage during DT is LO. When the transition is from 0 to LO, the voltage during the DT(LO) is the same as desired, and no error is produced. On the contrary, when there is a transition between LO to 0, the output voltage remains LO during the DT, shorting the duration of the state 0. A similar effect can be described for the other three sequences.

It is important to note that in the table the corresponding values for the three possible states are: HI = $\{V_{cc}-2V_{on}, V_{cc}+2V_d\}$; LO = $\{-V_{cc}-2V_d, -V_{cc}+2V_{on}\}$ and 0=$\{-V_d-V_{on}, V_d+V_{on}\}$. This affects the synthesized waveform since, for example, a pulse of width *pw* and height *h* = 0 should have a null area, but as the height is $-V_d-V_{on}$, the area is finite. Distortion will be more evident when the output voltage level is similar to that of VDS.

II. PROPOSED CORRECTION METHOD

The proposed method is an extension of Leggate and Kerkman, (1997) combined with the method of Choi *et al.* (1999), and it is useful to compensate not only the DTs but also the VDS. The proposed DT compensator compensates the area of each pulse by adding a compensating pulse at the end, without distorting the original pulse width, to preserve the ideal area.

Then, the pulses are distorted to compensate for the errors produced by the power stage (DT and VDS). The results of simulations show that the THD of a single-phase full-bridge converter can be reduced from 18% to 0.29% using this algorithm.

Figure 2 shows the case where the PWM algorithm has determined that pulse PA must have a width *pw* and height *h* (noted PA (*pw*, *h*)). The original (uncompensated) pulse has width pw_1 and height h_1, distorted by the DT (shaded areas). It is possible to compensate the pulses using a post-modulator that adds a new pulse, PC (pw_2, h_2), satisfying:

$$pw = pw_1 + 2\,DT + pw_2\,, \qquad (1)$$

$$pw\ h = (pw_1 + 2\ DT)\ h_1 + pw_2\ h_2\ , \quad (2)$$

where the voltage during DT is h_1. Equation (1) establishes the necessary condition to keep the width unaltered and Eq. (2) preserves the desired area. The solution is:

$$pw_1 + 2\ DT = pw\ k_1\ ,\ pw_2 = pw\ k_2\ , \quad (3)$$

where

$$k_1 = (h_2 - h)/(h_2 - h_1),\ k_2 = (h - h_1)/(h_2 - h_1). \quad (4)$$

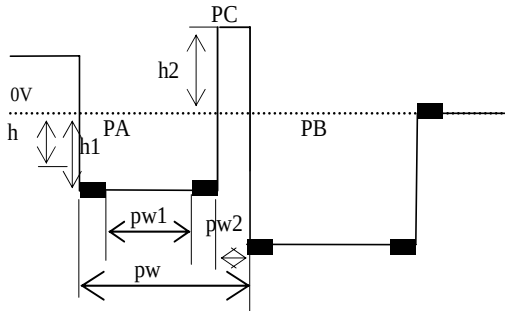

Figure 2 General compensation method.

For each original pulse, there are two DTs in the compensated PWM, one at the beginning of pulse PA and the other at the beginning of the compensation pulse.

Table 1 shows also the compensated waveforms for all possible combinations of the four sequences determined by the voltage and current signs (SV and SI). It can be shown that the solutions of Eqs. (1)-(4), in all cases shown in Table 1, provide unique values for k_1 and k_2:

$$k_1 = (V_{cc} - 2\ V_{on})/(V_{cc} + V_d - V_{on}), \quad (5)$$

$$k_2 = (V_d + V_{on})/(V_{cc} + V_d - V_{on}). \quad (6)$$

The compensation can be applied when the pulses are wide enough. Near the zero crossing of the voltage signal, the pulses become narrow and finally become distorted (to a triangular shape) due to the *slew rate* of the switches. Then the proposed compensation is not useful any more. If the modulating waveform is symmetrical, an analysis of the PWM in the interval $\{-\Delta I, +\Delta I\}$ shows that the amplitude of the positive and negative "zeros" in average becomes compensated. The average of the HI and LO pulses are partially compensated to $\{V_{cc}$ *and* $-V_{cc}\}$. A practical compensation algorithm should not take any action when the pulse widths become very narrow.

Figure 2 summarizes the different compensation regions along one period of the synthesized waveform.

III. ANALYSIS OF THE DISTORTION

The analysis of the distortion presented in the output waveform was simulated to evaluate the distortion produced by DTs and VDS. An unipolar PWM waveform corresponding to a 1 kHz sine wave, modulated by a 500 kHz[1] triangular carrier, was analyzed under different circumstances for a modulation index MA = 0.8 and a dc-link voltage of V_{cc} = 16 V. The THD was evaluated using the first 20 spectral components obtained from a FFT of the PWM waveform.

THD without DT and with ideal switches: The THD of the PWM waveform produced without introducing DTs and with ideal switches was evaluated as a baseline for simulations. Due to numerical errors, the simulated THD for the baseline case was 0.0115% instead of zero; at a sampling time of 1 ns.

Distortion due to VDS: When the voltage drops across diodes and switches are taken into account, the THD increased to 5.9%.

Distortion due to the DTs and VDS: Finally, the distortion due to both the DTs and the VDS was simulated. The THD in these circumstances was 18.6% for a 16-V dc-link (for a fixed DT of 100 ns). Very fast switches were used in the simulations (1 ns switching time).

IV. PROPOSED ALGORITHM

Table 1 shows the compensated waveforms. Note that for SV = –1 and SI = +1, the "zero" determined by G2G4 in fact has a negative value ($-V_d - V_{on}$). If a positive pulse is applied to cancel the area, (G1G4), then the new area will be zero. Note that at the beginning of the compensating pulse, a DT (G4) must be included to keep the original voltage value. The flow diagram of the compensation algorithm is shown in Fig. 3, Fig. 4 and Fig. 5. The gates to be triggered are loaded in "xx", and the pulse width in "pw". Each pulse generated by the PWM is taken by the compensator together with a sample of the output current. Once the sequence is identified, it is determined if the pulse must be compensated. If so, the adequate compensating pulse is selected, and then the algorithm calculates the DTs and the corresponding pulse widths. For current values $>\Delta I$, nor DTs neither unnecessary gate signals are generated. Figure 4 and Fig. 5 show the flow diagrams of the subroutines "Cmp" and "Inhibit gate", respectively.

V. CONCLUSIONS

A method for compensation of the THD produced by DTs and VDS was presented. It is an extension of that of by Leggate and Kerkman, (1997) combined with the one presented Choi *et al.* (1999). The original PWM pulses are pre-distorted to compensate deficiencies of the power stage. Extremely fast switches were used in simulations (1ns switching time) with the DTs in a range of 4 to 100 ns. The THD was reduced in simulations from 18.6% to 0.27% using the algorithm. The addition of the compensating pulse doubles the switching frequency. However, unipolar PWM requires half the switching frequency than required by bipolar PWM; therefore, the compensated PWM waveform would have the same switching frequency than an uncompensated waveform modulated using bipolar PWM. The proposed algorithm only needs

[1] A high enough switching frequency was selected to eliminate aliasing and separate its effect from the distortion produced by DT and VDS.

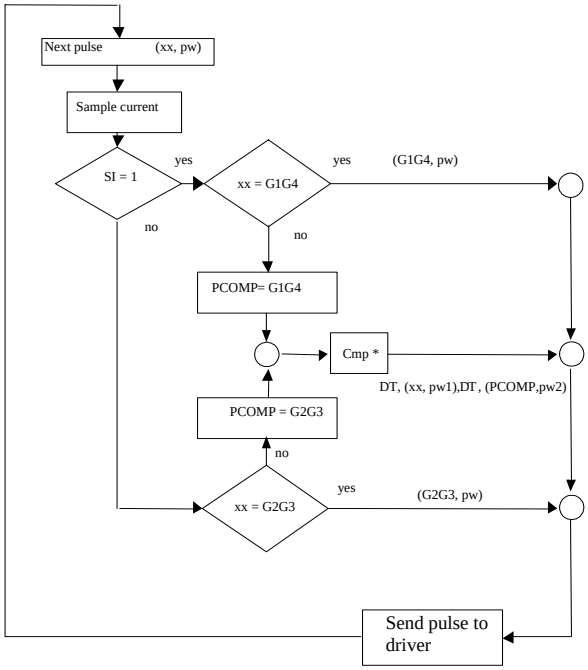

Figure 3: Proposed compensation algorithm.

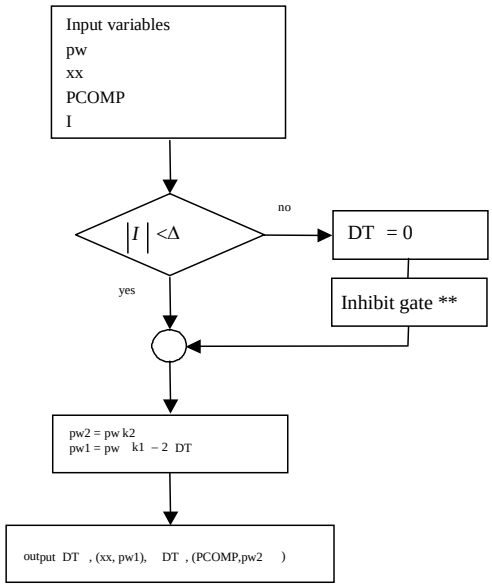

Figure 4 Subroutine Cmp*.

products and sums so it is suitable for being implemented on a DSP. Actually a prototype is being built. Preliminary experimental results show a reduction of the THD from 17.9% to 0.59%.

AKNOWLEDGEMENT

This work was partially supported by grants PGI UNS 24/K021 and PICT'98 3963 of ANPCYT

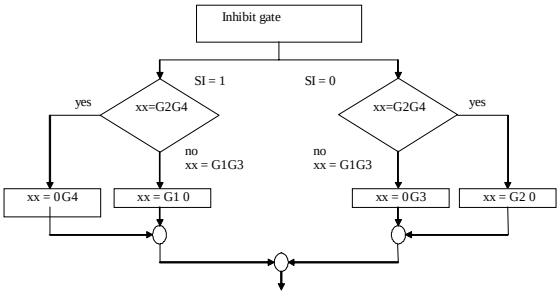

Figure 5: Inhibit gate algorithm.

REFERENCES

Chin, T. H., "Instability of Variable Frequency Induction Motor Drives Fed from Voltage Source Inverter", *IEEE Annual Conference Record*, 704-709 (1985).

Choi, J., S. Yong and S. Sul, "Inverter Output Voltage Synthesis Using Novel Dead Time Compensation", *IEEE APEC Conference Record*, 100-106 (1994).

Choi, J.S., J.Y. Yoo, S.W., S.W. Lim and Y.S. Kim, "A novel dead time minimization algorithm of the PWM inverter," *Industry Applications Conference*, 1999. Conference Record of the Thirty-Fourth IEEE IAS Annual Meeting, **4**, 2188-2193 (1999).

Colby, R. S., A. K. Simlot and M.A. Halloude, "Simplified Model and Corrective Measures for Induction Motor Instabilities Caused by PWM Inverter Blanking Time", *21st IEEE Power Electronics Specialists Conference*, PESC '90, 678-683 (1990).

Jeong, S. and M. Park, "The Analysis and Compensation of Dead-Time Effects in PWM Inverters", *IEEE Trans. On Industrial Electronics*, **38,** 108-114 (1991).

Leggate, D. and R.J. Kerkman, "Pulse Based Dead Time Compensator for PWM Voltage Inverters." *IEEE Transactions on Industrial Electronics*, **44**, 191-197 (1997).

Mohan, N., T. Undeland and W. Robbins, *Power Electronics: Converters, Applications, and Design*, John Wiley and Sons, New York (1989).

Mosely I. D., P. H. Mellor and C.M. Bingham, "Effect of dead time on harmonic distortion in Class-D audio power amplifiers." *Electronics letters*, **35**, 950-952 (1999).

Murai, Y., T. Watanabe and H. Iwasaki, "Waveform Distortion and Correction Circuit for PWM Inverters with Switching Lag-Times", *IEEE Trans. on Industry Applications*, **23**, 881-886 (1987).

Mutoh, N., A. Ueda, K. Sakai, M. Hattori and K. Nandoh, "Stabilizing Control Method for Suppressing Oscillations of Induction Motors Driven by PWM Inverters", *IEEE Trans. on Industrial Electronics*, **37**, 48-56 (1990).

Sukegawa, T., K. Kamiyama, K. Mizuno, T. Matsui and T. Okuyama, "Fully Digital, Vector-Controlled PWM VSI-Fed ac Drives with an Inverter Dead-

Time Compensation Strategy," *IEEE Trans. on Industry Applications*, **27**, 552-559 (1991).

Ueda, R., T. Sonoda, Y. Inoue and T. Umezu, "Instable Oscillating Motor in PWM Variable Speed Drive of Induction Mode and its Stabilization", *IEEE IAS Annual Conf. Rec*., 686-691 (1982).

Ueda, R., T. Sonoda and S. Takata, "Experimental Results and their Simplified Analysis on Instability Problems in PWM Inverter Induction Motor Drives", *IEEE Trans. on Industry Applications*, **25**, 86-95 (1989).

Table 1 Output Voltage and waveforms with non-ideal switches.

Seq.		Output Voltage V_{AB}				Waveforms
SV	SV	HI	0	LO	DT	
–1	1	X	$-V_d-V_{on}$	$-V_{cc}-2V_d$	LO	Uncompensated / Compensated
–1	–1	X	V_d+V_{on}	$-V_{cc}+2V_{on}$	0	Uncompensated / Compensated
+1	+1	$V_{cc}-2V_{on}$	$-V_d-V_{on}$	X	0	Uncompensated / Compensated
+1	–1	$V_{cc}+2V_d$	V_d+V_{on}	X	HI	Uncompensated / Compensated

Received: October 8, 2003.
Accepted: October 27, 2004.
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