

# Distributed Circuit Analysis and Design for Ultra-wideband Communication and sub-mm Wave Applications

**Temitope Oluseun Odedeyi**

A thesis submitted for the degree of Doctor of Philosophy  
of  
**University College London**



Communications and Information Systems Research Group  
Department of Electronic and Electrical Engineering  
University College London

January 29, 2020

# Declaration

I, Temitope O. Odedeyi confirm that the work presented in this thesis is my own. Where information has been derived from other sources, I confirm that this has been indicated in the thesis.

Temitope O. Odedeyi

# Acknowledgement

Praise to the Lord, the Almighty, the King of creation and to Jesus Christ, His Son and humanity's Saviour! I am most thankful to God for the grace He has given me, to start and to complete this research, and for all His help along the way.

I most sincerely appreciate my PhD supervisor, Professor Izzat Darwazeh, for his immense support through the course of this research. I am really grateful for the quality mentorship, the consistent effort towards my development as a proper researcher, and for showing, in ways too numerous to mention, that a supervisor can also be a friend. My sincere gratitude also goes to Dr Clive Poole who has served as my secondary supervisor through the course of this research. Indeed, Clive has been a great help from my days as an MSc student and he introduced me to high-speed circuit analysis and design.

I would like to thank Professor Herbert Zirath of the Department of Microtechnology and Nanoscience (MC2), Chalmers University of Technology, Göteborg Sweden for the opportunity to work in his lab and access provided to state-of-the-art microwave process design libraries. Many thanks to Mr Stavros Giannakopoulos at MC2 for his help with laying out the circuits for integrated circuit fabrication as well as in doing the measurement. I appreciate Dr Zhixin Liu and Mr Zichuan Zhou of the optical networks group at UCL, and Dr Brian Kelly, Dr John O'Carroll and Dr Richard Phelan of Eblana Photonics for their research collaboration, which has lead to a Photonics Journal publication.

The research reported in this thesis was conducted in the Communications and Information Systems research labs of the Electronic and Electrical Engineering department, and I owe some measure of appreciation to a long list of people in the group, all to whom I am immensely grateful. I must mention Mr Waseem Ozan, Ms Amany Kassem, Ms Xinyue Liu, Dr Hedaia Ghannam and Dr Tongyang Xu - who were PhD candidates under Professor Darwazeh during the period of my

---

research - for being sounding-boards, editors and audience at various points in the research process, and more importantly for the precious gift of community. My very special thanks to Dr Paul Haigh, who was a postdoctoral research fellow with Professor Darwazeh, and is now a lecturer at Newcastle University, for his collaboration, invaluable friendship and support, and for the much needed distraction that our mutual interest in boxing provided at crucial times.

My dear wife, Mobolaji, words cannot adequately convey the depth of my gratitude to you for been God's great blessing to me. I really cannot thank you enough for most graciously bearing all the inconveniences of living with me through this period. Your words of encouragement, the constant prayers, the many sacrifices, the regular meals and meticulously packed lunches (and treats) have played major roles in making this achievement possible. To our daughter, Oluwaseun Sarah, thanks for the joy and laughter you bring to us by your little adventures and for being the most effective stress relief ever! My parents, Ven (Professor) Olatunji and Mrs Olufunmilola Odedeyi, I am deeply grateful for all that you have been to me. Dad and Mum, Archbishop David and Mrs Oluremi Fabusoro, I am grateful for all your support, encouragement and constant prayers. Dr Oladapo and Dr Abisayo, Dr Akinola and Dr Comfort, Ms Omotunde, Ms Oreofe, Ms Success, all my siblings, family, mentors, friends and everyone who has encouraged me on this journey with a prayer, a kind word, a smile, I say a sincere thank you.

Finally, many thanks to the Nigerian government for funding my postgraduate studies under the Presidential Scholarship Scheme for Innovation and Development (PRESSID) and through the Petroleum Technology Development Fund (PTDF), with particular gratitude to the administration of Dr Goodluck Ebele Jonathan for inaugurating the PRESSID scheme



# Abstract

This thesis explores research into new distributed circuit design techniques and topologies, developed to extend the bandwidth of amplifiers operating in the mm and sub-mm wave regimes, and in optical and visible light communication systems. Theoretical, mathematical modelling and simulation-based studies are presented, with detailed designs of new circuits based on distributed amplifier (DA) principles, and constructed using a double heterojunction bipolar transistor (DHBT) indium phosphide (InP) process with  $f_T/f_{max}$  of 350/600 GHz. A single stage DA (SSDA) with bandwidth of 345 GHz and 8 dB gain, based on novel techniques developed in this work, shows 140% bandwidth improvement over the conventional DA design. Furthermore, the matrix-single stage DA (M-SSDA) is proposed for higher gain than both the conventional DA and matrix amplifier. A two-tier M-SSDA with 14 dB gain at 300 GHz bandwidth, and a three-tier M-SSDA with a gain of 20 dB at 324 GHz bandwidth, based on a cascode gain cell and optimized for bandwidth and gain flatness, are presented based on full foundry simulation tests. Analytical and simulation-based studies of the noise performance peculiarities of the SSDA and its multiplicative derivatives are also presented. The newly proposed circuits are fabricated as monolithic microwave integrated circuits (MMICs), with measurements showing 7.1 dB gain and 200 GHz bandwidth for the SSDA and 12 dB gain at 170 GHz bandwidth for the three-tier M-SSDA. Details of layout, fabrication and testing; and discussion of performance limiting factors and layout optimization considerations are presented. Drawing on the concept of artificial transmission line synthesis in distributed amplification, a new technique to achieve up to three-fold improvement in the modulation bandwidth of light emitting diodes (LEDs) for visible light communication (VLC) is introduced. The thesis also describes the design and application of analogue pre-emphasis to improve signal-to-noise ratio in bandwidth limited optical transceivers.

# Impact Statement

This thesis presents and validates new circuit design and bandwidth performance improvement techniques in the field of high speed communication. This theme is particularly relevant given the exponentially increasing demand for high speed data communication to meet the global need for high definition multimedia content streaming; higher resolution imaging systems; optoelectronic and instrumentations systems etc, such that it is expected that  $>30$  Exabyte/month will be required to satisfy end users by 2020.

The analysis, techniques and topology introduced in this thesis provide insight for design optimisation of mm and sub-mm wave amplifiers, which are essential components of high speed communication systems. It is envisaged that this will provide benefit in the realisation of next generation analogue and digital communication systems. The thesis also explores low cost and low complexity techniques for performance improvement in optical and visible light communication (VLC). In optical communication, the thesis describes the application of analogue pre-emphasis to increase the signal-to-noise ratio of bandwidth limited transceivers, with potential application in high capacity, short-reach communication links, typical of data centres. Nascent VLC is one of the more promising candidates for high-speed communications service provisioning, due to its wide, license-free spectrum, low capital expenditure and ability to provide simultaneous room illumination as well as data communications capabilities, with the technique introduced in this thesis providing an approach to improving data rate by bandwidth optimisation.

Most of the concepts presented in this thesis have been peer-reviewed and presented at six top conferences in the field of circuit and systems design and microwave theory and techniques, with one journal article published. All the conference papers have also been published as conference proceedings on the IEEE *Xplore* digital library, the online research repository of the Institute of Electri-

---

cal and Electronics Engineers (IEEE), the world's largest technical professional organization for the advancement of technology. Open access pre-print versions of these publications are also available on UCL Discovery (the online archive for UCL's Research Publication Service), with over a thousand full-text views and downloads from around the world.

# Contents

<b>List of Figures</b>	<b>12</b>
<b>List of Tables</b>	<b>18</b>
<b>List of Abbreviations and Symbols</b>	<b>19</b>
<b>1 Introduction</b>	<b>24</b>
1.1 Thesis Structure . . . . .	29
1.2 Key Contributions to Research Field and Publications . . . . .	31
<b>2 Distributed Amplification: Concept, Components &amp; Techniques</b>	<b>34</b>
2.1 Introduction . . . . .	34
2.2 The Concept of Distributed Amplification . . . . .	35
2.3 Gain and Bandwidth Mechanism of the DA . . . . .	38
2.4 Elements of the Conventional DA . . . . .	42
2.4.1 The Gain Cell . . . . .	42
2.4.2 The Artificial Transmission Line (ATL) . . . . .	44
2.4.3 The Transmission Line Termination . . . . .	46
2.5 DA Active Device Technologies . . . . .	46
2.5.1 DAs based on Bipolar Devices . . . . .	46
2.5.2 DAs based on Field-Effect Devices . . . . .	50
2.5.3 CMOS DAs . . . . .	54
2.5.4 BiCMOS DAs . . . . .	55
2.6 Modifications to the Conventional DA . . . . .	56
2.6.1 Gain Cell Modifications . . . . .	56
2.6.1.1 Phase Synchronisation . . . . .	56
2.6.1.2 Cascode Configuration . . . . .	59

2.6.1.3	Inductive-Peaked Cascode Loss Compensation . . .	61
2.6.2	Transmission Line Modifications . . . . .	63
2.6.2.1	$m$ -Derived Sections . . . . .	63
2.6.2.2	$L$ -Section Buffers . . . . .	63
2.6.2.3	DC Matching Termination with Damping Resistors or $RC$ Network . . . . .	64
2.6.2.4	Active Idle Port Termination . . . . .	64
2.6.3	Multi-tier DAs . . . . .	65
2.7	Conclusions . . . . .	67
<b>3</b>	<b>HBT Based DAs</b>	<b>69</b>
3.1	Introduction . . . . .	69
3.2	Historical Review of HBT based DAs . . . . .	70
3.2.1	Analytical studies of the HBT DA . . . . .	79
3.3	Discussion . . . . .	82
3.3.1	Merits of HBT in SSDA Design . . . . .	85
3.4	The TSC250 InP DHBT Process . . . . .	87
3.5	Derivation and Verification of Equivalent Circuit Model . . . . .	91
3.6	Conclusions . . . . .	93
<b>4</b>	<b>ATL Modifications for Bandwidth Enhancement in SSDAs</b>	<b>95</b>
4.1	Introduction . . . . .	95
4.2	Design Concept . . . . .	96
4.2.1	Input Line Modification . . . . .	97
4.2.2	Gain Cell and Output Line Modification . . . . .	103
4.3	Performance Assessment and Verification . . . . .	107
4.3.1	Simulations based on Ideal Transmission Lines . . . . .	107
4.3.2	Full Foundry Simulations based on Lossy Transmission Lines	111
4.4	MMIC Layout . . . . .	114
4.5	SSDA MMIC Measurement . . . . .	116

4.6	Discussion . . . . .	122
4.7	Conclusions . . . . .	125
<b>5</b>	<b>The M-SSDA: Design and Analysis</b>	<b>126</b>
5.1	Introduction . . . . .	126
5.2	Design Concept . . . . .	129
5.3	Performance Prediction and Comparison . . . . .	131
5.4	Bandwidth Optimized M-SSDA . . . . .	134
5.4.1	$2 \times 1$ M-SSDA . . . . .	135
5.4.2	$3 \times 1$ M-SSDA . . . . .	142
5.5	M-SSDA MMIC Measurement . . . . .	146
5.6	Discussion . . . . .	149
5.7	Conclusions . . . . .	151
<b>6</b>	<b>Noise Performance of the SSDA and its Derivative Topologies</b>	<b>152</b>
6.1	Introduction . . . . .	152
6.2	Noise Figure Modelling in Multiplicative DAs . . . . .	155
6.2.1	Evaluating Single-Stage Noise Figure . . . . .	155
6.2.2	Modelling of Noise Factor in Multiplicative DAs . . . . .	161
6.3	EINCSD of Single-Stage and Multiplicative DAs . . . . .	168
6.3.1	Evaluating Single-Stage EINCSD . . . . .	168
6.3.2	EINCSD for Multiplicative DAs . . . . .	172
6.3.3	Design guide for optimising EINCSD in multiplicative DAs .	182
6.4	Discussion: Noise Performance Optimisation for Multiplicative DAs	184
6.5	Summary and Conclusions . . . . .	185
<b>7</b>	<b>Application of ATL Synthesis in Optical Comms. and VLC</b>	<b>187</b>
7.1	Pre-emphasis equalizer based on $T$ -half filter section for sensitivity improvement in bandwidth limited transceivers . . . . .	188
7.1.1	Pre-emphasis Equalizer Design . . . . .	188
7.1.2	Principle of SNR enhancement . . . . .	191

7.1.2.1	Experimental setup . . . . .	192
7.1.3	Results and Discussion . . . . .	194
7.2	Application of Transmission Line Synthesis	
	Techniques in Visible Light Communication	
	Systems . . . . .	198
7.2.1	Design Concept . . . . .	200
7.2.2	Performance Assessment . . . . .	204
7.3	Conclusions . . . . .	207
<b>8</b>	<b>Concluding remarks</b>	<b>208</b>
8.1	Summary and Discussion . . . . .	208
8.2	Future Work . . . . .	212
<b>A</b>	<b>Alternative Approach to EINCSD Derivation</b>	<b>216</b>
A.1	EINCSD for SSDA . . . . .	216

# List of Figures

2.1	A simple bandpass amplifier. . . . .	35
2.2	Conventional bipolar DA. . . . .	37
2.3	Basic filter sections: simplified unit cells of the DA ATL. . . . .	39
2.4	Simplified equivalent circuits of the input and output ATLs of the HBT SSDA. . . . .	41
2.5	Structure of the conventional DA. . . . .	43
2.6	A vacuum tube DA . . . . .	43
2.7	HBT hybrid- $\pi$ model equivalent circuit with extrinsic device parasitics	47
2.8	MESFET/HEMT hybrid $\pi$ model equivalent circuit with package parasitics . . . . .	51
2.9	The first MMIC DA implemented on a 1 $\mu\text{m}$ GaAs MESFET tech- nology . . . . .	54
2.10	Capacitive and inductive phase synchronisation. . . . .	60
2.11	Gain cell modifications: conventional cascode and cascode with at- tenuation compensation. . . . .	62
2.12	Schematic circuit of a cascaded DA. . . . .	66
2.13	Schematic circuit of a matrix DA. . . . .	67
3.1	MMIC layout of the first HBT DA. . . . .	71
3.2	HBT process structures: conventional, base-undercut and trans- ferred substrate structures . . . . .	72
3.3	Circuit schematics of HBT SSDA and 2-C-SSDA . . . . .	79
3.4	Microphotographs of two state-of-the-art HBT DAs . . . . .	84
3.5	Simplified schematic of the TSC250 InP DHBT device. . . . .	88
3.6	IC interconnect cross-section showing low loss THz microstrip lines and high density thin-film interconnects . . . . .	89



3.7	Representative cross-section of TSC250 IC technology . . . . .	90
3.8	3D view of MMIC section showing passive circuit elements: TFML, TFR, MIM capacitor and via . . . . .	91
3.9	Simulated emitter current density, $J_E$ , as a function of the collector-to-emitter voltage, VCE, for different base currents, $I_B$ , of TSC250. .	92
3.10	S-parameter comparison: foundry process model vs extracted small-signal model. . . . .	93
4.1	Simplified equivalent circuits of the input and output ATLs of a conventional HBT SSDA. . . . .	97
4.2	Bandwidth improvement from transmission line scaling. . . . .	100
4.3	Effect of shunt capacitance on frequency response of 50% scaled transmission line. . . . .	101
4.4	Line losses for a conventional transmission line; 50% scaled transmission line; and a 50% scaled transmission line with peaking. . . .	102
4.5	Line losses for a conventional; Butterworth; Chebyshev and the proposed transmission line. . . . .	103
4.6	SSDA schematic circuits: inductive peaked cascode vs new bandwidth extension configuration . . . . .	106
4.7	Structure of DA featuring transmission line scaling and a peaking (shunt) capacitance on the input ATL, with inductive peaking for attenuation compensation. . . . .	107
4.8	Forward Gain $S_{21}$ (dB) with corresponding simulated eye diagrams at 500 Gbps (inset): conventional - 132 GHz bandwidth with 7 dB gain; SSDA with inductive-peaked cascode - 253 GHz bandwidth with 7 dB gain; and SSDA with new bandwidth enhancement technique - 328 GHz bandwidth with 7 dB gain. . . . .	108
4.9	Input line reflection $S_{11}$ (dB) comparison. . . . .	109
4.10	Output line reflection $S_{22}$ (dB) comparison. . . . .	110

4.11	Forward gain $S_{21}$ (dB): conventional - 140GHz bandwidth with 8 dB gain; SSDA with inductive-peaked cascode - 275GHz bandwidth with 8 dB gain; and SSDA with new bandwidth enhancement technique - 345 GHz bandwidth with 8 dB gain. . . . .	112
4.12	Input line reflection $S_{11}$ (dB) comparison. . . . .	113
4.13	Output line reflection $S_{22}$ (dB) comparison. . . . .	113
4.14	Chip planar layout: SSDA with input line scaling and capacitive peaking (chip area: $615 \mu\text{m} \times 475 \mu\text{m}$ ). . . . .	115
4.15	Chip layout: SSDA with inductive-peaked cascode (Chip area: $615 \mu\text{m} \times 540 \mu\text{m}$ ). . . . .	116
4.16	Microphotograph of the SSDA. MMIC size: $620 \mu\text{m} \times 460 \mu\text{m}$ . . . .	117
4.17	Measured vs simulated S-parameters of the amplifier. . . . .	118
4.18	Effects of ground inductance on output reflection coefficient. . . . .	119
4.19	Setup for 100 MHz – 120 GHz S-parameter measurement. . . . .	120
4.20	Setup for 140 GHz – 220 GHz S-parameter measurement. . . . .	121
4.21	High frequency S-parameter response for SSDA under different bias conditions. . . . .	122
5.1	The DA family tree: <i>Major DA configurations with the originating publication.</i> . . . .	128
5.2	Structure of the M-SSDA. . . . .	129
5.3	$2 \times 1$ CE HBT M-SSDA (a); with simplified equivalent circuits of: the output transmission line (b), the intermediate transmission line (c), and the input transmission line (d). . . . .	130
5.4	S-parameter comparison of a $2 \times 1$ M-SSDA with a 2-C-SSDA . . .	133
5.5	Two-tier M-SSDA schematic with scaled input and intermediate transmission lines. Inset shows the modified gain cell. . . . .	137

5.6	S-parameter comparison of a two-tier CE M-SSDA, a two-tier M-SSDA with bandwidth extension; and a two-tier M-SSDA with bandwidth extension and EF input buffer: forward gain $S_{21}$ (dB) comparison. . . . .	138
5.7	S-parameter comparison of a two-tier CE M-SSDA, a two-tier M-SSDA with bandwidth extension; and a two-tier M-SSDA with bandwidth extension and EF input buffer: input line $S_{11}$ (dB) and output line reflection $S_{22}$ (dB) comparison. . . . .	139
5.8	Two-tier M-SSDA with bandwidth extension: lossless transmission lines and ideal passive element (dashed lines); lossy transmission lines, passive elements with vias and transitions (solid lines). . . .	140
5.9	MMIC planar layout: two-tier M-SSDA with bandwidth extension (footprint: $565\text{ }\mu\text{m} \times 600\text{ }\mu\text{m}$ ). . . . .	141
5.10	Three-tier M-SSDA schematic with scaled input and intermediate transmission lines. Inset shows the modified gain cell. . . . .	143
5.11	Three-tiered M-SSDA with bandwidth extension: lossless transmission lines and ideal passive element (dashed lines); lossy transmission lines, passive elements with vias and transitions (solid lines). . .	144
5.12	MMIC planar layout: three-tier M-SSDA with bandwidth extension (footprint: $766\text{ }\mu\text{m} \times 800\text{ }\mu\text{m}$ ). . . . .	145
5.13	Microphotograph of the M-SSDA. MMIC size: $770\text{ }\mu\text{m} \times 800\text{ }\mu\text{m}$ . . .	147
5.14	Setup for 100 MHz – 67 GHz S-parameter measurement. . . . .	148
5.15	Comparison of simulated and measured responses for the three-tier M-SSDA: simulated - dashed lines; measured result - solid lines. . .	149
6.1	Comparison of forward gain $S_{21}$ (dB) and noise figure (dB) for the SSDA, two-stage and three-stage DA. Analysis based on TSC250 common-emitter gain cell with transmission lines optimised for bandwidth and gain flatness. All circuits operate at same bias. . . . .	153

6.2	Simplified intrinsic equivalent circuit of a MESFET/HEMT with its associated gate and drain noise sources. . . . .	156
6.3	Simplified intrinsic equivalent circuit of a bipolar transistor with its associated base and collector noise sources. . . . .	160
6.4	Comparison of gain and noise figure for the SSDA, two-tier and three-tier M-SSDA. Analysis based on TSC250 common-emitter gain cell with transmission lines optimised for bandwidth and gain flatness. All circuits operate at same bias. . . . .	166
6.5	Verification of (6.22): comparison based on a common-emitter gain cell using foundry model of TSC250 as active device, with transmission lines optimised for bandwidth and gain flatness. . . . .	167
6.6	Noise voltage sources in a SSDA. . . . .	169
6.7	Components of the total EINCSD of the SSDA. . . . .	173
6.8	Noise voltage sources in a matrix multiplicative FET DA. . . . .	178
6.9	The scaling of transimpedance, noise voltage and noise current spectral densities in multiplicative amplifiers using a simplified equivalent HEMT model. . . . .	179
6.10	The effect of different values of input termination on transimpedance, noise voltage and noise current spectral densities for a five-tier M-SSDA using simplified equivalent HEMT model. . . . .	180
6.11	The effect of different values of output termination on noise current spectral density on a five-tier M-SSDA using a simplified equivalent HEMT model. . . . .	181
7.1	(a) Circuit diagram of RF pre-emphasis filter; and (b) Frequency response of the 3 dB and 6 dB RF pre-emphasis filter. Red curve: 3 dB; Blue curve: 6 dB; Dotted line: Simulation result; Solid line: Measured result (with 0.1 GHz). . . . .	190
7.2	Signal chain model comparing digital pre-emphasis and analogue pre-emphasis. . . . .	191

7.3	Experimental set-up for DML. RRC: root-raise-cosine, DAC: digital-to-analogue converter, ADC: analogue-to-digital converter, PD: photodiode, VOA: variable optical attenuator, DSP: digital signal processing, SMF-28: standard single-mode fiber. . . . .	193
7.4	Frequency response of the 32-GBd PAM4 using RF pre-emphasis filters with different pre-emphasis levels. . . . .	195
7.5	Receiver sensitivity measurements for back-to-back transmission. . .	196
7.6	Receiver sensitivity measurements after 1-km SMF-28. . . . .	197
7.7	Performance improvement of using RF pre-emphasis filter using different DAC resolutions. . . . .	198
7.8	A simplified LED equivalent circuit. . . . .	201
7.9	HBT hybrid- $\pi$ model equivalent circuit with dashed lines around the input in common emitter configuration. . . . .	201
7.10	Simplified LED equivalent circuit $C_d$ incorporated into a $p$ -ATL cell. Dashed lines surround the equivalent LED circuit. . . . .	202
7.11	Comparison of input impedance magnitude with the 3 dB bandwidth annotated. . . . .	205
7.12	Comparison of normalised current $i_d$ through the LED (dashed lines for inductance at $L_d/2$ to reduce peaking). . . . .	206

# List of Tables

2.1	Description of bipolar transistor hybrid- $\pi$ model element values. . .	47
2.2	Performance summary of state-of-the-art HBT-based DAs. . . . .	50
2.3	Description of a MESFET/HEMT hybrid- $\pi$ model element values. .	51
2.4	Comparison of electrical parameters of bipolar and field effect transistors . . . . .	53
2.5	Performance summary of state-of-the-art MESFET/HEMT-based DAs. . . . .	54
2.6	Performance summary of state-of-the-art CMOS-based DAs. . . . .	55
2.7	Performance summary of state-of-the-art BiCMOS-based DAs. . . .	56
3.1	Historical review of HBT DAs: <i>a summary</i> . . . . .	80
3.2	Employing HBTs in DA design: <i>merits and demerits</i> . . . . .	87
4.1	Comparison of the performance of new SSDA with state-of-the-art SSDAs and C-SSDAs. . . . .	121
5.1	Comparison of the performance of new M-SSDA with state-of-the-art matrix DAs. . . . .	149
6.1	Design guide for optimising EINCSD: <i>Key equations with numbering</i> . . . . .	183
7.1	Parameters for RF pre-emphasis filter. . . . .	190
7.2	LED parameters at various drive currents . . . . .	204

# List of Abbreviations and Symbols

$\alpha$	Attenuation factor
$\gamma$	Propagation factor
$\omega_c$	Angular cut-off frequency
$\phi$	Phase Constant
$A_V$	Amplifier voltage gain
$C_\mu$	Base-collector junction depletion region capacitance
$C_\pi$	Base-emitter depletion region plus base-charging diffusion capacitance
$C_{BC}$	Base-collector junction capacitance
$C_{BE}$	Base-emitter junction capacitance
$C_{CE}$	Collector-emitter junction capacitance
$C_{DS}$	Extrinsic drain-source substrate region capacitance
$C_{ds}$	Intrinsic drain-source substrate region capacitance
$C_{GD}$	Extrinsic gate-drain junction resistance
$C_{gd}$	Intrinsic gate-drain junction resistance
$C_{GS}$	Extrinsic gate-source junction capacitance
$C_{gs}$	Intrinsic gate-source junction region charging capacitance
$f_{3dB}$	Upper -3dB amplifier cut-off frequency
$f_{max}$	Maximum frequency of oscillation

---

*LIST OF ABBREVIATIONS AND SYMBOLS*

---

$g_m$	Transistor transconductance
$GSa/s$	GigaSamples/second
$L_b$	Base contact inductance
$L_c$	Collector contact inductance
$L_d$	Drain contact inductance
$L_e$	Emitter contact inductance
$L_g$	Gate contact inductance
$L_s$	Source contact inductance
$N_{opt}$	Optimum number of gain stages in a distributed amplifier
$r_\pi$	Base-emitter junction dynamic resistance
$r_{bb}$	Intrinsic base region spreading resistance
$R_b$	Base contact resistance
$R_c$	Collector plus sub-collector contact resistance
$R_{ds}$	Drain-source output resistance
$R_d$	Drain contact resistance
$R_e$	Emitter contact resistance
$R_g$	Gate terminal series resistance
$R_i$	Channel region gate-charging resistance
$R_s$	Source contact resistance
$Z_o$	Image impedance
$Z_{int}$	Intermediate line impedance (matrix amplifier)



$Z_{in}$	Input line impedance
$Z_{o-int}$	Image impedance of the input artificial transmission line
$Z_{o-out}$	Image impedance of the output artificial transmission line
$Z_{out}$	Output line impedance
$f_{max}$	Unilateral gain cut-off frequency
$f_T$	Transition frequency
ATL	Artificial transmission line
BiCMOS	Bipolar complementary metal-oxide-semiconductor
BJT	Bipolar junction transistor
c	Speed of light in free space
C-SSDA	Cascaded single stage distributed amplifier
CE	Common emitter
CMOS	Complementary metal-oxide-semiconductor
CPM	Coplanar waveguides
DA	Distributed amplifier
DHBT	Double heterojunction bipolar transistor
DMT	Discrete-multitone
DPSK	Differential Phase Shift Keying
EF	Emitter follower
EINCS	Equivalent noise current spectral density
FET	Field effect transistor

GBP	Gain-bandwidth product
HBT	Heterojunction bipolar transistor
HEMT	High electron mobility transistor
IC	Integrated circuit
InP	Indium Phosphide
JFET	Junction field-effect transistor
M-SSDA	Matrix single stage distributed amplifier
MBE	Molecular beam epitaxy
MESFET	Metal-semiconductor field-effect transistor
MIM	Metal-insulator-metal
MMIC	Monolithic microwave integrated circuit
NRZ	Non-return to zero
PAM	Pulse amplitude modulation
PAM	Pulse-amplitude modulation
PAM-4	4-level pulse-amplitude modulation
PSK	Phase Shift Keying
RFE	Receiver front-end
RZ	Return to zero
SSDA	Single-stage distributed amplifier
TDM	Time division multiplexing
TIA	Transimpedance amplifier

## *LIST OF ABBREVIATIONS AND SYMBOLS*

---

TMICs Terahertz monolithic integrated circuits

VCSEL Vertical cavity surface emitting laser

VNA Vector network analyser

# Chapter 1

## Introduction

The rapid growth of the telecommunications industry has brought about an exponentially increasing demand for higher speed, larger capacity and more precise communication systems. An area where this growth can be most prominently observed is in the rapidly increasing demand in multimedia communication requiring transmission systems with higher data rates and bandwidths. This and other areas such as high speed data communications, high resolution imaging systems, optoelectronic and instrumentation systems rely on a family of high performance electronic systems which includes amplifiers, and continue to drive demand for ultra-wideband integrated circuitry extending into the 0.3 - 3 THz frequency bands [1]. Amplifiers in such systems are often required - among many other requirements - to cover a wide frequency range at appreciable gain. The wide bandwidth requirement is particularly necessary as it defines the capability of the system for transferring high-data-rate information, transmitting/receiving short pulses or processing wideband signals.

The distributed amplifier (DA) topology has been the most prominent approach to designing ultra-wideband amplifiers. Distributed amplification is a fairly mature concept, having been initially proposed by Percival in 1936 [2]. In the topology, the bandwidth-limiting intrinsic capacitance of the active device is absorbed into a transmission-line-like structure through a system of series inductances. This way, the capacitance from individual gain cells are isolated while the output currents combine additively. Since its introduction, the wide bandwidth offered by DAs has led to its application in fibre optic and satellite communication systems, phased array radar and broadband instrumentation.

The structure of the original DA has seen lots of modifications over the years, to suit varying applications and to improve figures of merit. A major driver for the development in the design of DAs is the evolution of the primary component of the DA, the active device. Considering that the concept and application of distributed amplification pre-dates solid state electronics, the earliest DAs were based on thermionic devices. However, with the advent of transistor technology, focus rapidly shifted to transistor-based DAs. As is common knowledge, there are two major families of transistors; bipolar and field effect transistors. Both families have been widely adopted in DA design. Limitations on the high frequency performance of bipolar junction transistors (BJTs) due to process constraints originally limited their application in DAs. However, with the advent and development of the heterojunction bipolar transistor (HBT) which offered significant improvements in high frequency performance over their conventional homojunction counterparts [3], these devices began to find increasing application in DA design.

Despite the remarkable progress in the development of complementary metal-oxide-semiconductor (CMOS) and high electron mobility transistor (HEMT) process design, attributes such as the ability to deliver higher gains, better linearity and higher bandwidth/feature-size make HBTs attractive for high frequency and wideband circuits such as DAs [4–6]. HBTs also offer better threshold voltage uniformity and low phase jitter properties, important requirements for high speed optical communication receiver applications [7–9]. As transistor technology continue to move further into the terahertz bandwidth range primarily driven by indium phosphide (InP)-based heterojunction devices, some key advantages of the HBT over the field effect-based high electron mobility transistor (HEMT) have also being identified as making them more suitable in terahertz monolithic integrated circuits (TMICs) [10–12]. One of such properties is that InP HBTs attain much higher breakdown voltage than HEMTs at a given transition frequency  $f_T$  due to the wide bandgap InP collector making them better suited for the design of ultra-wideband power amplifiers. Other properties such as higher speed and low

noise performance make it possible to have an InP-HBT-based single IC platform on which all receiver and transmit components can be integrated [3, 11, 13, 14].

However, with these advantages come some notable limitations, which make the application of HBTs in DAs more complicated. A major drawback is attributable to the fact that HBTs have resistive/capacitive inputs resulting a complex characteristic impedance that makes the design of the distributed network and line termination more challenging [15]. The resistive input nature of HBTs also results in losses and power dissipation on their input artificial transmission line. This introduces higher attenuation with each additional stage of the HBT-based DA, resulting in fewer realisable stages compared to a FET-based DA [15, 16]. Such considerations has resulted in the high electron mobility transistor (HEMT) - a field effect device - being the dominant active circuit solid state technology in DA circuits.

To overcome these limitations, significant research effort has gone into the analysis and design of high performing HBT DAs. As is usually the case in designs based on solid state devices, performance improvement is driven in two streams: the continual evolution in process technology yielding better performing circuit elements; and the development of novel circuit techniques which optimises the performance of available devices. A clear evidence of the significant progress already achieved in both facets is that the DA with the current record bandwidth and gain-bandwidth product (GBP) performance of any process technology is an InP HBT based cascaded single stage DA (C-SSDA) with 16 dB gain and 235 GHz bandwidth [17]. However, as the device was based on a process with  $f_T$  of 350 GHz, only about two-thirds of the available current gain bandwidth was utilised.

As advancements in integrated circuit (IC) fabrication technology continue to deliver device processes with greater IC bandwidth [6], there is need for circuit design topologies and techniques that optimise these new generation devices and enable them to deliver maximum benefits in performance [1, 18, 19]. Electronic devices operating at these frequencies are exclusively monolithic ICs. Hence, from

the transistor-side, achieving bandwidths closer to the  $f_T$  is - in theory - realisable, as the extrinsic parasitics from the transistor that could impose frequency limitation are quite minimal. However, passive circuit elements required for matching and signal transmission impose restrictions on overall performance. The degree of scaling required to achieve such low-terahertz bandwidth performance imposes extra-design constraints both in device fabrication and circuit design. For instance, an InP HBT process with 130 nm emitter width developed by Teledyne Scientific Company (TSC) has an extrapolated  $f_T$  of 521 GHz and  $f_{max}$  - which is the frequency at which the unilateral gain of the transistor becomes unity - of 1.15 THz at bias condition of  $V_{CE} = 1.6$  V and  $I_C = 6.9$  mA. At 600 GHz, a single 130 nm HBT is expected to have approximately 6 dB of gain [14]. However, restrictions imposed by the wavelength of the signal at this frequency and high-frequency attenuative losses from transmission lines would make it practically impossible to achieve wideband performance using the conventional DA design techniques [14]. Modifications such as the ones adopted in [17] give strong indications as to the possibility of lower terahertz-bandwidth (0.3-3 THz) amplification, forming a basis for further research.

This thesis explores the application of new circuit design techniques and topologies to improve the gain and bandwidth performance of the HBT DA. Particular focus is given to the single-stage distributed amplifier (SSDA), due to its proven potential to optimising the gain and bandwidth performance of HBT devices coupled with a relative design and implementation simplicity. For higher gain performance than the single cell of the SSDA can provide, the matrix-SSDA (M-SSDA) is introduced as an alternative to the already existing cascaded-SSDA (C-SSDA). While both amplifiers are functionally similar in that they operate on the same gain mechanism, the M-SSDA has the advantage of a wider range of tunability arising from the nature of its architecture. This higher degree of design flexibility allows for more freedom in optimisation and significant potential for improved performance.

A common application of the DA is as a preamplifier, in conjunction with the photodetector forming the optical receiver front-end (RFE) [20]. The optical signal that arrives at the photodetector is usually weak, requiring that the RFE, which converts the light to an electric signal is significantly low noise so as to avoid poor bit error rate performance. Hence, a study of the noise performance of the RFE is crucial, as it determines the utility of the DA as preamplifiers in this application. This thesis presents an analytical study, backed up by extensive full foundry simulations, of the noise figure and the equivalent input noise current spectral density (EINCS) of the SSDA and its derivative topologies. Moreover, as the resistive matching required to achieve wideband matching in DAs generally results in poorer noise performance, techniques to optimise noise performance are discussed.

Based on concepts in artificial transmission line synthesis that have been applied in achieving bandwidth extension in DA, the thesis introduces a new technique to achieve up to three-fold improvement in the modulation-bandwidth of light emitting diodes (LEDs) for visible light communication (VLC). By incorporating the bandwidth-limiting diffusion capacitance of the LED into an artificial transmission line, the technique enables the modification of the frequency response of the LEDs, and achieves bandwidth improvement. The thesis also describes the application of similar concepts in designing analogue pre-emphasis equalizers to improve signal-to-noise ratio (SNR) in bandwidth limited optical transceivers.

The theoretical and analytical work described in this thesis are validated by extensive simulations based on a full foundry model of an InP DHBT process supplied by Teledyne (TSC250). All circuit schematic modelling, chip layout and optimisation, and performance simulations reported in this thesis were performed using Advanced Design System (ADS), an electronic design automation software supplied by Keysight Technologies. Two of the monolithic microwave integrated circuit (MMIC) devices described in this thesis - an SSDA with bandwidth extension modifications and a three-tier M-SSDA - have also been fabricated and mea-



sured, with details of the device layout, optimisation and measurement presented. Due to limitations of the accuracy the transistor models beyond 100 GHz, coupled with yield challenges with the TSC250 fabrication process [14], which are beyond the scope of this work, the devices exhibited frequency responses that significantly deviated from that predicted pre-fabrication, with bandwidth performance being up to 40% less.

## 1.1 Thesis Structure

The structure of the thesis is outlined as follows.

- This introductory chapter is followed by a general introduction to the theory of distributed amplification. The chapter also includes description of the main elements of the DA and commonly adopted circuit modifications to improve performance. A comparison of the properties of bipolar and field effect transistors is presented, to highlight the merits and demerits of these devices particularly as it relates to DA design. Performance summaries of the state-of-the-art DAs based on MESFETs/HEMTs, HBTs, CMOS and Bipolar CMOS (BiCMOS) processes are also presented.
- Chapter 3 contains a comprehensive review of reported HBT DAs circuits. The chapter highlights the effects that improved process fabrication techniques and circuit synthesis techniques have on improving figures of merit of the HBT DA. The chapter also covers analytical reports on the subject area. Based on inference drawn the literature review, the justification for the apparent suitability of HBTs for SSDA implementation is discussed. This chapter also describes the HBT process with which the ideas generated from this research are demonstrated in circuit - Teledyne's TSC250. The process of extracting small signal parameters from the foundry model supplied by the device manufacturer, which informed the designs that are later on presented, is described. The accuracy of the extracted small signal equiva-

lent model was assessed based on a comparison of S-parameter performance of both the foundry model and the extracted equivalent model in a basic common-emitter amplifier mode.

- In Chapter 4, a new approach to improving the bandwidth performance of the SSDA based on transmission line modifications is described. The three-step technique described involves scaling down the inductance on the input artificial transmission line (ATL); creating a high frequency resonance peak by the addition of shunt capacitance on the input ATL; and compensating for the resulting increased reflection with adapted negative resistance attenuation compensation techniques. Also presented is a comparative assessment of the S-parameter performance of an SSDA based on the new modifications with a conventional SSDA and one designed featuring the inductively-peaked cascode method applied in the DA with the highest gain-bandwidth product currently recorded.
- Chapter 5 discusses a new amplifier topology, the M-SSDA. As proof of concept, a two-tier common-emitter (CE) M-SSDA based on a full foundry double heterojunction bipolar transistor (DHBT) model is presented, demonstrating the viability of the proposed design. The S-parameter performance of the proposed circuit is compared with that of a C-SSDA with two gain cells to show the similarity in their gain and bandwidth performance. To demonstrate the utility of the proposed design, a practical  $3 \times 1$  M-SSDA circuit is also presented based on the bandwidth extension techniques described in the previous chapter.
- In Chapter 6, analyses the noise performance of the SSDA and its multiplicative derivatives, i.e. the M-SSDA and C-SSDA. By contrasting the noise mechanism of the multistage DA with the multiplicative DA vis-à-vis their gain, a case is made for the latter despite the established poorer noise attribute. In this chapter, a model is derived and verified for estimating the

noise performance of a C-SSDA or M-SSDA with  $m$ -tiers based on Friis' noise factor formula. The equivalent noise current spectral density (EINCSD) for a SSDA was also derived from existing models for multi-stage DAs, which forms the basis for estimating EINCSD for a  $m$ -tier multiplicative DA based on the adapted Friis noise factor formula.

- The application of transmission line synthesis techniques to extending the bandwidth of LEDs in the context of VLC is explored in Chapter 7. The proposed technique is demonstrated in a simulation study based on a previously reported LED small-signal equivalent circuit model.
- The final chapter, concludes the thesis and presents an outline for future work.

## 1.2 Key Contributions to Research Field and Publications

The research work presented in this thesis contains a number of original theoretical and design contributions to the general field of ultra-wideband circuit design. A summary of the main contributions is as follows:

- Development and verification of artificial transmission line scaling and capacitive peaking as techniques for improving SSDA bandwidth performance. The analytical bases of these techniques are presented and verified based on full foundry MMIC simulation.
- Development of a new amplifier topology, the M-SSDA, which employs multiplicative gain, similar to the C-SSDA. The M-SSDA has advantages in smaller circuit footprint, a potential for lower transmission line losses and better noise performance.

- Derivation of analytical models that describe the line impedances of the input ( $Z_{in}$ ), intermediate ( $Z_{int}$ ) and output ( $Z_{out}$ ) transmission lines, respectively, for a M-SSDA with a common emitter gain cell.
- Design, optimisation and fabrication of a SSDA based on TSC250 - an InP DHBT supplied by Teledyne with  $f_t/f_{max}$  values of 350/600 GHz. The MMIC measured 7.1 dB gain at 200 GHz bandwidth; the highest bandwidth reported for a SSDA.
- Design, optimisation and fabrication of the first matrix-SSDA, also based on TSC250. The three-tier device measured 12.5 dB gain at 170 GHz bandwidth, with good input and output matching.
- Derivation and validation of new equations that describe the scaling of noise figure, noise voltage spectral density (NVSD) and the EINCSD in multiplicative DAs (i.e. M-SSDA and C-SSDA).
- Description of gain-bandwidth-noise performance optimisation considerations for multiplicative DAs.
- Development and analytical validation of the application of transmission line synthesis techniques to improving the bandwidth light emitting diodes (LEDs) in the context of visible light communication (VLC).

This research project has resulted in seven publications, to date, comprising of six conference proceedings and one journal article. These are publications are listed chronologically, as follows:

1. **T. Odedeyi** and I. Darwazeh, "Bandwidth enhancement technique for bipolar single stage distributed amplifier design", *IEEE Asia Pacific Microwave Conference (APMC)*, Kuala Lumpur, Malaysia Nov 2017.
2. **T. Odedeyi** and I. Darwazeh, "Matrix single stage distributed amplifier design for ultra wideband application", *24th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Batumi, Georgia, Dec 2017.

3. **T. Odedeyi**, P. A. Haigh, and I. Darwazeh, "Transmission line synthesis approach to extending the bandwidth of LEDs for visible light communication", *11th International Symposium on Communication Systems, Networks, and Digital Signal Processing (CSNDSP)*, Budapest, Hungary, Jul 2018.
4. **T. Odedeyi**, C. Poole, and I. Darwazeh, "Noise analysis of multiplicative distributed amplifiers", *IEEE International Symposium on Circuits and Systems (ISCAS)*, Sapporo, Japan, May 2019.
5. **T. Odedeyi**, S. Giannakopolous, H. Zirath, and I. Darwazeh, "Single-stage and multiplicative distributed amplifiers for 200 GHz+ amplification", *2019 IEEE Asia Pacific Microwave Conference (APMC)*, Singapore Dec 2019.
6. Z. Zhou, **T. Odedeyi**, B. Kelly, J. O'Carroll, R. Phelan, I. Darwazeh, and Z. Liu, "Impact of analog and digital pre-emphasis on the signal-to-noise ratio of bandwidth-limited optical transceivers", DOI: 10.1109/JPHOT.2020.2966617 *IEEE Photonics Journal*, pp.1-1, 2020.
7. **T. Odedeyi**, and I. Darwazeh, "Derivation of the Equivalent Input Noise of Multiplicative Distributed Amplifiers for Wideband Optical Receiver Applications", *accepted for presentation at the IEEE International Symposium on Circuits and Systems (ISCAS)*, Seville, Spain, May 2020.

# Chapter 2

## Distributed Amplification: *Concept, Components and Circuit Techniques*

### 2.1 Introduction

As a concept, distributed amplification was initially proposed by Percival in a patent filed in 1937, as a means of improving the robustness of thermionic valve circuits in terms of bandwidth and bias voltage. The concept involved the separation of the inter-electrode capacitances of individual vacuum tubes, while adding their transconductances [2]. In what qualifies as the seminal work on the subject, Ginzton *et al.* (1948) expanded extensively on the concept, providing theoretical proof and analyses fundamental to understanding the DA [21]. In their paper, it was demonstrated that by an appropriate distribution of ordinary electron tubes along artificial transmission lines, amplification over much greater bandwidths could be achieved. This circuit configuration overcame the GBP limitation that is characteristic of conventional amplifier circuits. Also discussed were the frequency response of the DA, dissipation effects, noise characteristics and techniques for performance optimisation. It was in this paper that the terms *distributed amplification* and *distributed amplifier* were first used. The term *travelling wave amplifier* is also often used to describe the DA [22–27], reflecting the manner in which the input signal, under ideal conditions, is propagated as a forward travelling wave

along the input ATL, exciting the active devices in the amplifier, and inducing an amplified forward travelling wave on the output ATL.

This chapter discusses the concept of distributed amplification, describing how the setup breaks the gain-bandwidth limit. The main elements of the DA and commonly adopted circuit modifications for performance improvement are also described. Furthermore, a comparison of bipolar and field effect based DAs is presented in this chapter, to highlight the merits and demerits of each process in DA design. Performance summaries of the state-of-the-art DAs based on MES-FET/HEMTs, HBTs, CMOS and BiCMOS processes are also presented.

## 2.2 The Concept of Distributed Amplification

Parameters intrinsic to the active device used in amplifiers sets a limit on the bandwidth that is achievable at a given gain level if conventional amplifier topologies are employed. This essentially creates a trade-off between the gain and bandwidth such that the product of voltage gain and bandwidth is fixed. It has been shown that regardless of the complexity of the inter-stage coupling and matching networks utilised, the GBP of a conventional cascade of active devices cannot exceed this set limit. This point was illustrated in [28] by considering the voltage transfer function  $A_v(\omega)$  of a simple bandpass amplifier consisting of an active device and a resonant coupling circuit, as shown in Figure 2.1.

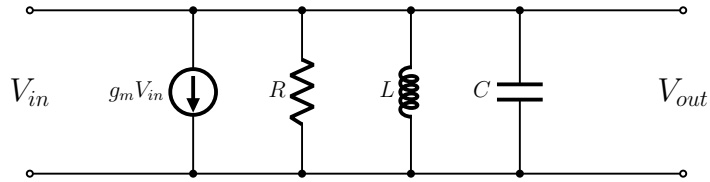


Figure 2.1: A simple bandpass amplifier.

$$A_V(\omega) = \frac{-g_m R}{1 + j\omega_o RC \left( \frac{\omega}{\omega_o} - \frac{\omega_o}{\omega} \right)} \quad (2.1)$$

with  $\omega_o = 1/\sqrt{LC}$ . The 3 dB bandwidth (B) of the amplifier is

$$B = \frac{1}{2\pi RC} \quad (2.2)$$

and the maximum voltage gain ( $A_{Vo}$ ) has a magnitude of  $g_m R$  (occurring when  $\omega = \omega_o$ ); thus yielding

$$GBP = A_{vo}B = g_m R \times \frac{1}{2\pi RC} = \frac{g_m}{2\pi C} \quad (2.3)$$

The absence of  $R$  - the load resistor, which influences maximum passband gain - in definition of GBP (2.3), reflects the fact that any increase achieved in gain would be offset by an equal reduction in bandwidth. As the defining parameters are intrinsic to the active device, it is not possible to surpass this limitation by an optimization of external circuit elements. Furthermore, the approach of cascading single-stage amplifiers, which have bandwidth approaching the limiting GBP of the active device amplifiers, would also be inefficient; as with such designs, the gain of each stage would be close to unity. Also, while combining the output from a number of active devices in parallel will increase the output power, it will yield no improvement in the GBP. This is because the effective capacitance of the active devices in parallel is the sum of capacitance contributions from each active device [29, 30]. Hence, we may infer that the design that would break the GBP limitation would be one that superimposes the output current from a number of devices, while keeping the shunt capacitances of these devices from being accumulated [28]. Such solution was found in distributed amplification.

In a DA, the (shunt) capacitance intrinsic to the active device is *distributed* with series inductive elements ( $L$ ), forming the familiar constant -  $k$  low pass filter structure. The combination of the input and output shunt capacitance from the transistor and corresponding series inductances required to achieve the distributed effect forms the input and output lines of the DA. These lines have a structure



and response that closely resembles transmission lines hence they are described as artificial transmission lines (ATLs).

To illustrate the operation of the DA, a schematic structure of a bipolar-based DA is shown in Figure 2.2<sup>1</sup>. The resultant capacitances at the base-emitter and collector-emitter junctions of the transistor are absorbed into ATLs formed with inductive lines, with the resultant transmission lines referred to as the *base* and *collector* lines, respectively. A signal applied at the input travels down the base line towards  $R_{TERM}$  where it is absorbed. The travelling voltage wave excites each transistor and transfers the signal to the collector line through its transconductance. In the ideal scenario that the phase velocities of both lines are equal, the amplified signal from each of the transistors are all in phase and they add in the forward direction towards the output. As the waves travelling in the reverse direction are out of phase, they tend to cancel out; any uncanceled signal is absorbed by  $R_{TERM}$  on the collector line. DAs based on field effect devices operate in a similar fashion, with the base and collector lines replaced by *gate* and *drain* lines, respectively.

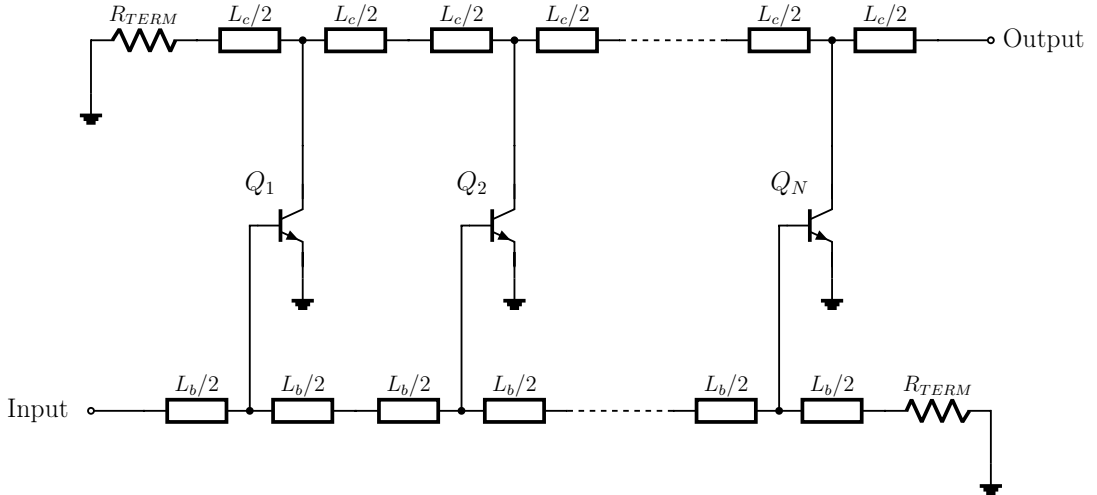


Figure 2.2: Conventional bipolar DA.

<sup>1</sup>In this thesis, the distributed inductances that are part of the transmission lines of the DA are represented with rectangular symbols, rather than the curly inductor (European) symbol, to reflect their distributed nature. Lumped inductors and inductances that are components of equivalent circuits are represented with the curly inductor symbol.

## 2.3 Gain and Bandwidth Mechanism of the DA

The active device gain of the DA is accumulated in an additive manner. A signal applied to the input port travels down the input transmission line towards the idle port termination. As the signal travels, it excites the individual gain cells, which amplify the signal and feed to the output line. On the output line, the signal splits in two directions: towards the output port or towards the idle port termination on the output line. As the signal travelling towards the output port add in phase, a large signal is incident on the output terminating load. Waves travelling in the reverse direction (towards the idle port termination) tend to diminish due to destructive interference from phase mismatch; what is left is absorbed by the terminating resistor.

Assuming a lossless transmission line and ignoring resistive losses due to the active device, the gain of a DA is given by

$$Gain = Ng_m \frac{\sqrt{Z_{o-in}Z_{o-out}}}{2} \quad (2.4)$$

where  $N$  is the number of gain stages,  $g_m$  is the transistor transconductance, and  $Z_{o-in}$  and  $Z_{o-out}$  are the image impedances of the input and output ATLs [21]. The image impedance of an ATL is analogous to the characteristic impedance of a real transmission line, and is defined as the impedance seen looking into one end of the transmission line when the other end is terminated with its own image impedance [31].

Conventionally, the ATL for DAs are designed using the image parameter filter design method. This involves the specification of passband and stop-band characteristics for a cascade of simple two-port networks, closely related to terminated periodic structures [32]. The ATL of a unit cell could be formed either of a T-section (Figure 2.3(a)) or a  $\pi$ -section (Figure 2.3(b)) filter; with the T-section implementation being more commonly adopted. Fundamental characteristics of the ATL can be observed by studying the basic T-section or  $\pi$ -section filter network.

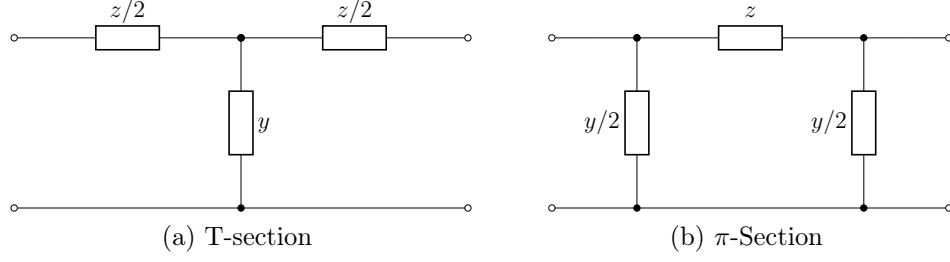


Figure 2.3: Basic filter sections: simplified unit cells of the DA ATL.

The image impedances of the T-section and  $\pi$ -section,  $Z_{oT}$  and  $Z_{o\pi}$ , respectively, are given by [29, 32]

$$Z_{oT} = \sqrt{\frac{z}{y} \left( 1 + \frac{zy}{4} \right)} \quad (2.5)$$

$$Z_{o\pi} = \sqrt{\frac{z}{y} \left( 1 + \frac{zy}{4} \right)^{-1}} \quad (2.6)$$

where  $z$  is the total series arm impedance and  $y$  is the shunt arm admittance of the filter. In the particular case of a DA transmission line where  $z$  is inductive and  $y$  is capacitive, the image impedance is given by (2.7)

$$Z_{oT} = \sqrt{\frac{L}{C} \left( 1 - \frac{\omega^2 LC}{4} \right)} \quad (2.7)$$

and

$$Z_{o\pi} = \sqrt{\frac{L}{C} \left( 1 - \frac{\omega^2 LC}{4} \right)^{-1}} \quad (2.8)$$

for the T-section and  $\pi$ -section, respectively. The low-pass characteristics may be inferred from the filter structure as the combination of series inductors and shunt capacitors tend to block high frequency signals while passing low frequency signals. At DC (i.e.  $\omega = 0$ ), it also satisfies the condition for a constant- $k$  filter. A purely reactive symmetrical two-port network is considered a constant- $k$  filter if its series arm impedance and shunt arm admittance satisfy the relation:

$$\frac{z}{y} = k^2 \quad (2.9)$$

where  $k$  is a fixed real number known as the constant of inversion. It can be observed that  $k = Z_{oT}$  when  $\omega = 0$ ; this value of  $Z_{oT}$  is the characteristic impedance of the transmission line, denoted by  $Z_o$  [29, 32].

From (2.7), it can be shown that beyond a certain angular frequency, the value of  $Z_o$  changes from being purely real to being purely imaginary. This frequency is called the Bragg frequency, and represents the upper cut-off frequency  $\omega_c$  of the T- and  $\pi$ -section filters; given by

$$\omega_c = 2\pi f_c = \frac{2}{\sqrt{LC}} \quad (2.10)$$

The image impedance (2.7) can, therefore, be expressed as

$$Z_{oT} = \sqrt{\frac{L}{C} \left(1 - \frac{\omega^2}{\omega_c^2}\right)} \quad (2.11)$$

and

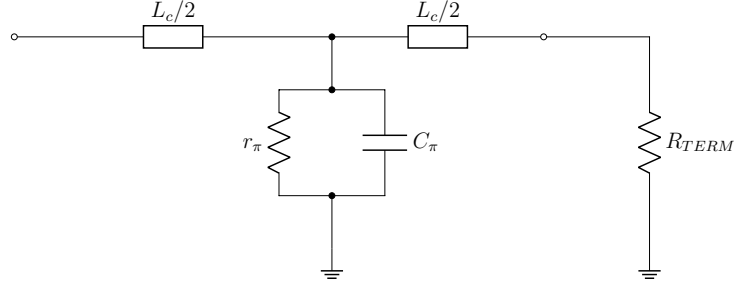
$$Z_{o\pi} = \sqrt{\frac{L}{C} \left(1 - \frac{\omega^2}{\omega_c^2}\right)^{-1}} \quad (2.12)$$

Comparing (2.2) and (2.10), it may be observed that the constant- $k$  ATL may be designed for significantly higher cut-off frequency than the basic  $RC$  combination of the conventional common emitter amplifier.

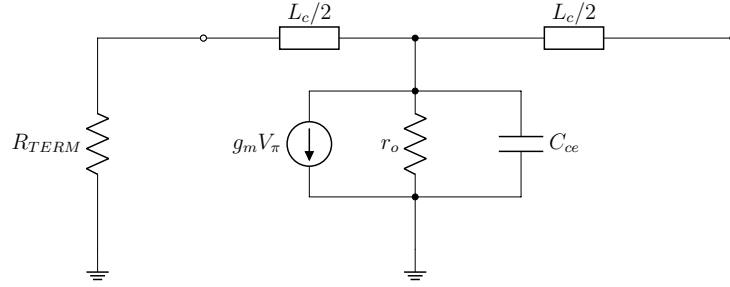
Figure 2.4 shows simplified equivalent circuits of the input and output ATLs of the single cell of an HBT DA. The lines are made up of intrinsic capacitance  $C_\pi$  and  $C_{ce}$  and inductive lines  $L_B$  and  $L_C$ ; with both lines coupled by the transistor transconductance  $g_m$ .  $r_\pi$  and  $r_o$  are the transistor base-emitter junction resistance and output resistance, respectively, and  $R_{TERM}$  is the terminating resistance.

If it is assumed that  $R_{TERM}$  is the image impedance of the lines, the current delivered to the load is given by

$$I_{out} = \frac{1}{2}g_m e^{\gamma_n/2} \left( \sum_{n=1}^N V_{in-n} e^{-(N-n)\gamma_n} \right) \quad (2.13)$$



(a) Input ATL of a conventional HBT SSDA.



(b) Output ATL of a conventional HBT SSDA.

Figure 2.4: Simplified equivalent circuits of the input and output ATLs of the HBT SSDA.

where  $V_{in-n}$  is the voltage at the input of the  $n^{th}$  transistor and  $\gamma_n$  is the propagation factor/section of the collector line.

$$\gamma_n = \alpha_n + j\phi_n \quad (2.14)$$

with  $\alpha_n$  and  $\phi_n$  representing the attenuation and phase shift per section on the collector line.

As set out in Wong (1995), the transfer function of the two-port network, formed by individual constant- $k$  elements, is described by the ABCD matrix

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \prod_{n=1}^N \begin{bmatrix} A & B \\ C & D \end{bmatrix}_n \begin{bmatrix} V_{n+1} \\ I_{n+1} \end{bmatrix} \quad (2.15)$$

If the two ports are matched on the image basis, so that  $Z_{i2}^{(n)} = Z_{i1}^{(n+1)}$ , (2.15) can be expressed as

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{Z_{i1}^{(1)}}{Z_{i2}^{(n)}}} \cosh \gamma & \sqrt{Z_{i1}^{(1)} Z_{i2}^{(n)}} \sinh \gamma \\ \frac{1}{\left(\sqrt{Z_{i1}^{(1)} Z_{i2}^{(n)}}\right)} \sinh \gamma & \sqrt{\frac{Z_{i2}^{(n)}}{Z_{i1}^{(1)}}} \cosh \gamma \end{bmatrix} \begin{bmatrix} V_{n+1} \\ I_{n+1} \end{bmatrix} \quad (2.16)$$

where

$$\gamma = \sum_{m=1}^n \gamma_m \quad (2.17)$$

is the propagation factor for the transmission network, and

$$\alpha = \sum_{m=1}^n \alpha_m \quad (2.18)$$

$$\beta = \sum_{m=1}^n \beta_m \quad (2.19)$$

are the attenuation and phase shift, respectively, for the transmission network. Within the passband, the ideal network has a power transfer coefficient of unity and a phase shift  $-\phi$ . Beyond cut-off, the power transfer coefficient rolls off with a slope equal to  $e^{-2\alpha}$ .

## 2.4 Elements of the Conventional DA

The basic architecture of DAs is shown in Figure 2.5. It consists of input and output artificial transmission lines coupled by the transconductance from the gain cell formed of active device(s), with suitably matched terminations. Each of these constituents and their application in DA design are subsequently discussed.

### 2.4.1 The Gain Cell

The concept of distributed amplification pre-dates the invention of the transistor. Hence, vacuum tubes were employed as the active device in the earliest DA circuits

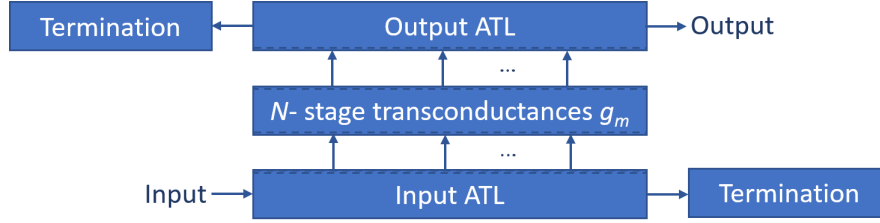


Figure 2.5: Structure of the conventional DA.

[21, 33–35]. The years 1936-1956 saw some foundational investigation into DA design and performance using such thermionic devices. Their use was rapidly phased out as solid-state technology matured. Figure 2.6 shows a vacuum tube distributed power amplifier reported in 1950 with 11 dB gain operating from 100 Hz to 300 MHz [35]. Contemporary DA circuits mostly feature bipolar (BJTs and HBTs) and field-effect (MESFETs and HEMTs) devices [36]. However, the demand for low cost, devices with small device area and low power consumption is driving the design of DAs using mainstream complementary-metal-oxide-semiconductor (CMOS) technologies [36, 37].

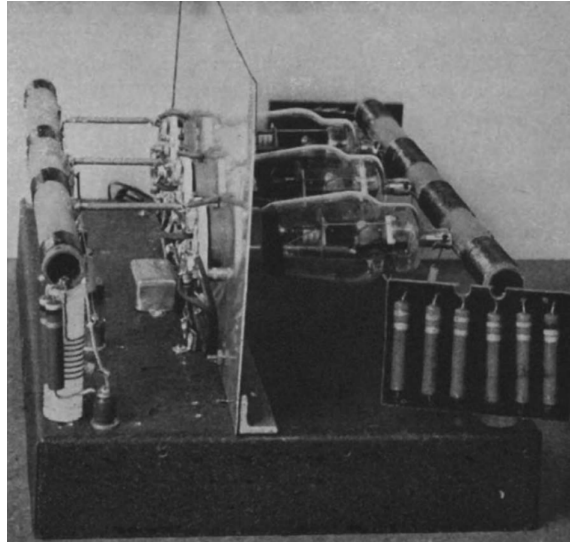


Figure 2.6: A vacuum tube DA *Copson, 1950* [35].

HBTs and HEMTs, being heterojunction devices, offer higher transistor operation speeds - defined by both the  $f_T$  and  $f_{max}$  - than their homojunction counterparts and from the gain cells of new generation ultra-wideband DAs.  $f_T$  is the

frequency at which the transistor incremental gain drops to unity while  $f_{max}$  is the frequency at which the maximum available power gain of the transistor drops to unity, and is used to estimate power gain, considering that over a wide range of frequencies, maximum available power gain follows the relation  $G_p = \left(\frac{f_{max}}{f}\right)^2$  [38].

### 2.4.2 The Artificial Transmission Line (ATL)

As mentioned earlier, the DA consists of active gain cells connected by lumped or distributed inductive elements. The combination of the inductive elements and the capacitance from the active device forms the transmission lines also described as the distributed network. Due to the similarity of this structure to ideal transmission lines, it is described as an artificial transmission line (ATL). One ATL on the input connects the gates (in the case of FETs) or the bases (in the case of bipolar transistors); while the output ATL connects the drains or the collectors in FETs and bipolar transistors, respectively. Both lines are primarily coupled via the transconductance  $g_m$  of the active device, forming an additive setup [28]. Each ATL (output or input) consists of N-filter sections, with N being the number of gain cells employed in the DA. When bipolar devices are employed, the input and output ATLs are referred to as base-line and collector-line, respectively while for field-effect devices, they are referred to as gate-line and drain-line respectively. It has been observed that the bandwidth and gain profile of an amplifier can be improved by designing more sophisticated ATLs while maintaining an appropriate impedance level [28].

The ATLs in DAs are essentially filters. This is because their action involves the modification of the frequency dependence of the given circuit to extend its bandwidth. More specifically, the distribution of a prescribed capacitance over an extended network makes it possible, through impedance transformation, to maintain a required impedance level; so as to achieve the desired gain without sacrificing bandwidth. Furthermore, many impedance transformation networks for high frequency applications are constructed from reactive elements. Their transmission



characteristics are frequency dependent [28]. Since distributed amplifiers were introduced to achieve gain and bandwidth that are unachievable with simple coupling networks, the operation of distributed amplifiers should be expected to be closely related to the action of filters. More specifically, the distribution of a prescribed capacitance over an extended network creates the possibility, through impedance transformation, of maintaining a required impedance level so as to achieve the desired gain without sacrificing bandwidth. Impedance transformation networks for high frequency applications are primarily constructed from reactive elements, hence, their transmission characteristics are frequency dependent [28].

It is worth mentioning that conventionally, these transmission lines are designed using the image parameter approach, as opposed to the more common insertion loss (also described as network synthesis) design method. The image parameter approach is more straightforward, requiring just the knowledge of the design impedance and the capacitances of the active device. However, while the image parameter method is adequate, it is by no means optimal. It has limitations, one of which is the fact that an arbitrary frequency response cannot be incorporated into the design [32], such that there is no systematic way to achieving a prescribed response. Also, as the value of the image impedance  $Z_{oT}$  is frequency dependent, its value constantly deviates from the fixed resistive source, termination and load impedances of the DA as frequency increases; this raises a challenge in achieving a perfect broadband match. This is discussed in more detail in Section 2.4.3.

While it is possible to use lumped inductors to form ATLs [39–42], the vast majority of modern ATLs utilise microstrip transmission lines [22, 43, 44] or coplanar waveguides (CPWs) [7, 45, 46]. These better support high frequency performance, due to their lower parasitics. They can also be fabricated to specific inductance values.

### 2.4.3 The Transmission Line Termination

To avoid reflections, both input and output ATLs need to be terminated with resistance equal to the image impedance of the lines. The conventional approach is to terminate with a resistor with the value of the designs characteristic impedance (typically a 50  $\Omega$  resistor). However, owing to the frequency dependence of the image impedance of the ATLs, this solution is severely limited in its functionality. Compared to the reactive matching adopted in narrowband amplifiers, the resistive match provides a broadband performance, albeit with poorer power reflection across the device bandwidth. A significant amount of study has gone into designing terminations that closely matches the frequency dependence of the transmission lines. Common examples of these are described in Section 2.6.2.

## 2.5 DA Active Device Technologies

### 2.5.1 DAs based on Bipolar Devices

The first reported transistor-based DA featured a bipolar junction transistor (BJT) [47]. The bipolar transistor technology - particularly with heterojunction bipolar transistors (HBTs) and double-heterojunction bipolar transistors (DHBTs) - typically offer higher transconductance gain ( $g_m$ ) values than their contemporary field-effect devices [48]. HBTs and DHBTs consist of heterostructures of compound semiconductors designed to have an energy band configuration that supports the rapid transit of electrons injected from the emitter through the base layer and collector depletion region to be collected in the sub-collector region. Hence, they are able to support very high frequency of operation, and processes capable of operating well into the THz-range have been reported [14, 19]. This class of transistors also exhibits better linearity [49]. Figure 2.7 shows the AC small-signal hybrid- $\pi$  equivalent circuit model of a bipolar transistor and Table 2.1 provides a descrip-

tion of the constituent elements of the model. A distinction is made between the intrinsic device parameters and package parasitics [50].

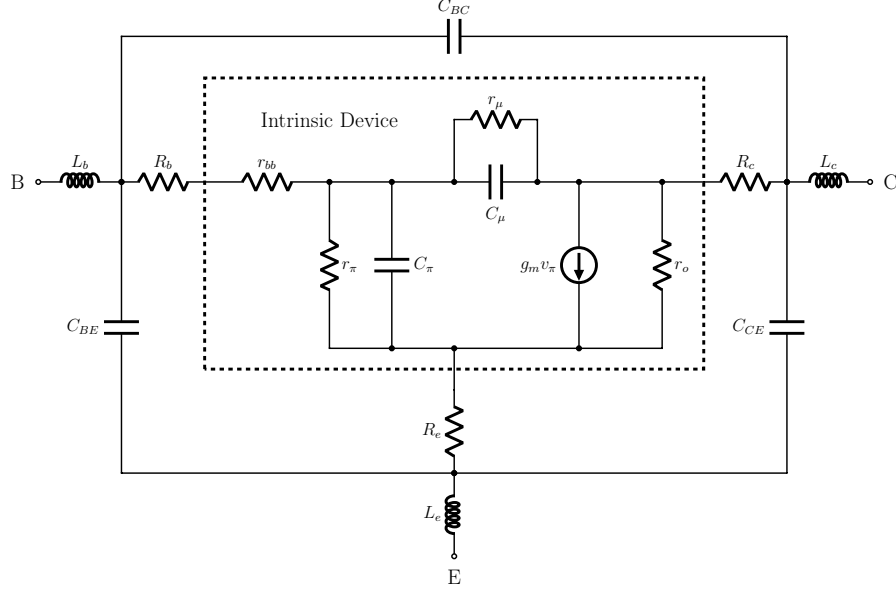


Figure 2.7: HBT hybrid- $\pi$  model equivalent circuit with package parasitics [50].

Table 2.1: Description of bipolar transistor hybrid- $\pi$  model element values.

Element	Description
$C_\pi$	Base-emitter depletion region plus base-charging diffusion capacitance
$C_{BE}$	Base-emitter junction capacitance
$C_{CE}$	Collector-emitter junction capacitance
$C_\mu$	Base-collector junction depletion region capacitance
$C_{BC}$	Base-collector junction capacitance
$r_\pi$	Base-emitter junction dynamic resistance
$r_{bb}$	Intrinsic base region spreading resistance
$R_b$	Base contact resistance
$R_c$	Collector plus sub-collector contact resistance
$R_e$	Emitter contact resistance
$L_b$	Base contact inductance
$L_c$	Collector contact inductance
$L_e$	Emitter contact inductance
$g_m$	Device transconductance

The current gain cut-off frequency  $f_T$  of HBTs given by [38]

$$f_T = \frac{1}{2\pi\tau_{EC}} = \frac{1}{2\pi(\tau_E + \tau_B + \tau_{CSCL} + \tau_C)} \quad (2.20)$$

where

- $\tau_{EC}$  is the emitter-to-collector transit time delay, a sum of all the delay components corresponding to charges stored in different regions of the transistor.

$$\tau_{EC} = \frac{dQ_B}{dI_c} \quad (2.21)$$

$dQ_B$  is the base charge associated with an increment input voltage and  $dI_C$  is the corresponding increment in output current.

- $\tau_E$  is the emitter delay, containing components associated with charges stored at the emitter-base depletion region edges, needed to establish the electrostatic fields at the junction. It is given by

$$\tau_E = \frac{C_\pi}{g_m} \quad (2.22)$$

$\tau_E$  accounts for a major fraction of the total delay,  $\tau_{EC}$ .

- $\tau_B$  is the base delay due to the hole charge stored in the quasi-neutral base to neutralize the charge associated with the electrons traversing the region and is given by

$$\tau_B = \frac{W_B^2}{2D_n} + \frac{W_B}{v_m} \quad (2.23)$$

where  $W_B$  is the base thickness,  $D_n$  is the electron diffusivity, and  $v_m$  is the velocity at which electrons cross from the base to the edge of the collector.

- $\tau_{CSCL}$  is the delay due to the hole charge stored in the base, that is required to neutralize the charge of electrons traversing the base-collector depletion region, given, for electron travel at saturated velocity  $v_{sat}$ , as

$$\tau_{CSCL} = \frac{W_c}{2v_{sat}} \quad (2.24)$$

where  $W_c$  is the width of the base-collector depletion region<sup>2</sup>.

- $\tau_C$  represents the transit time across the collector, corresponding to the  $RC$  time constant for charging the base-collector capacitance given by

$$\tau_C = C_\mu \left( R_E + R_C + \frac{kT}{qI_C} \right) \quad (2.25)$$

( $\frac{kT}{qI_C}$  is the inverse of the intrinsic transconductance of the device i.e.  $1/g_m$ )

The power gain cut-off frequency  $f_{max}$  is given by

$$f_{max} = \sqrt{\frac{f_T}{8\pi r_{bb,eff} C_{\mu,eff}}} \quad (2.26)$$

where  $r_{bb,eff} \cdot C_{\mu,eff}$  represents the effective time constant for the distributed  $RC$  network at the base-collector junction [38, 49].

However, there are some major drawbacks with the use of bipolar transistors in DA design. Firstly, with the higher transconductance comes an inherently higher input capacitance  $C_\pi$ , which depends on the base transit time  $\tau_B$ , of the device [51, 52].

$$C_\pi = C_{je} + g_m(\tau_B + \tau_C) \quad (2.27)$$

This potentially limits the bandwidth of the DA, as would be discussed in Section 2.4.2. Another challenge with bipolar based DAs is the presence of minority carriers, which results in poorer noise performance compared to FETs. Furthermore, bipolar transistors exhibits less thermal stability, due to the presence of reverse saturation (leakage) current. Table 2.2 presents a summary of the state of the art in reported HBT-based DAs, including information on the gain, bandwidth, GBP, noise figure (NF), DC power consumption ( $P_{dc}$ ), the process technology, and year of publication with reference.

---

<sup>2</sup>The factor of two in this expression arises because only half the charge needed to neutralize the travelling carriers corresponds to hole charge in the base, as the remainder is neutralized in the collector [38].

Table 2.2: Performance summary of state-of-the-art HBT-based DAs.

Gain (dB)	Bandwidth (GHz)	GBP (GHz)	NF (dB)	$P_{dc}$ (mW)	Technology	Year/Reference
12.7	27.5	119	4.0	650	2 $\mu$ m GaInP/GaAs HBT	2000/ [53]
25	50	889	-	1,700	1.2 $\mu$ m GaAs/InP HBT DHBT	2004/ [54]
30	45	1,423	-	3,000	1.2 $\mu$ m GaAs/InP HBT DHBT	2004/ [54]
17	60	425	-	2,500	1.2 $\mu$ m GaAs/InP HBT DHBT	2004/ [54]
10	102	323	-	150	1 $\mu$ m InP/InGaAs DHBT	2005/ [55]
12	94	374	-	460	1 $\mu$ m InP/InGaAs DHBT	2005/ [55]
11	80	284	-	224	1 $\mu$ m InP/InGaAs DHBT	2005/ [55]
21	120	1,346	-	610	0.7 $\mu$ m InP DHBT	2008/ [56]
12.8	70	306	-	105	InP HBT	2009/ [27]
15	90	506	-	-	0.7 $\mu$ m InP DHBT	2010/ [57]
13	110	491	-	-	0.7 $\mu$ m InP DHBT	2010/ [57]
10	182	576	-	105	0.25 $\mu$ m InP HBT	2014/ [58]
12.8	180	786	8	110	0.25 $\mu$ m InP DHBT	2015/ [17]
7.5	192	455	8.5	40	0.25 $\mu$ m InP DHBT	2015/ [17]
16	235	1,483	10	117	0.25 $\mu$ m InP DHBT	2015/ [17]
19	160	1,426	-	108	0.13 $\mu$ m SiGe HBT	2016/ [59]
13.5	207	980	-	210	0.25 $\mu$ m InP DHBT	2017/ [60]

### 2.5.2 DAs based on Field-Effect Devices

Moser (1967) reported the first FET-based DA. A combination of factors such as high gain, wide bandwidth - especially with HEMTs; better noise performance and greater thermal stability has made field effect technology the more prominent transistor technology for high performance DAs [42, 61]. Figure 2.8 shows the small-signal hybrid- $\pi$  equivalent circuit model of a MESFET/HEMT and Table 2.3 provides a description of the constituent elements of the model, with a distinction made between the intrinsic device and package parasitics [50].

Similar to the HBT, the HEMT is a heterostructure device made with semiconductors of different bandgaps. Based on this property, HEMTs can achieve exceptionally high electron mobilities compared to bulk material of the same composition, leading to higher transconductance and gain at high frequencies. The transition frequency  $f_T$ , considering small signal and linear operation, is given by [38]

$$f_T = \frac{1}{2\pi\tau_{SD}} \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (2.28)$$

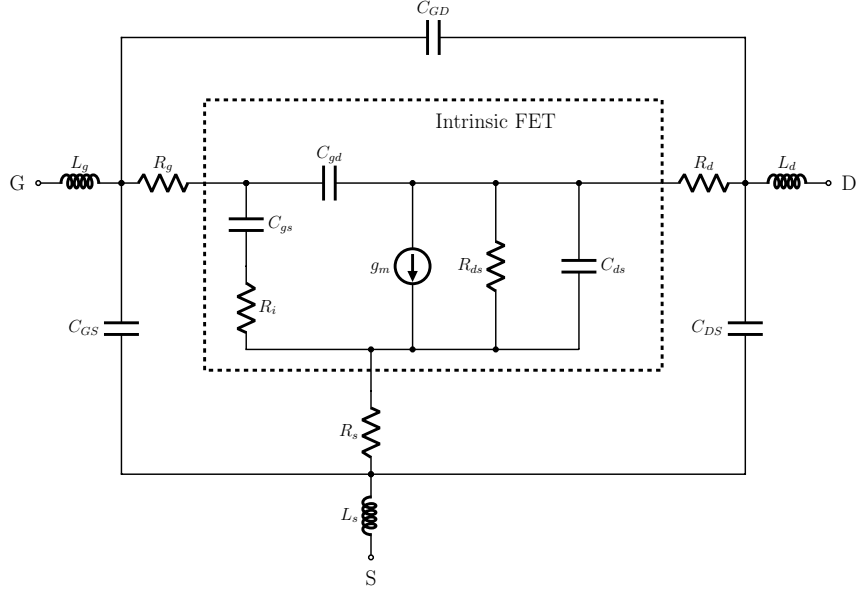


Figure 2.8: MESFET/HEMT hybrid  $\pi$  model equivalent circuit with package parasitics [50].

Table 2.3: Description of a MESFET/HEMT hybrid- $\pi$  model element values.

Element	Description
$C_{gs}$	Intrinsic gate-source junction region charging capacitance
$C_{GS}$	Extrinsic gate-source junction capacitance
$C_{ds}$	Intrinsic drain-source substrate region capacitance
$C_{DS}$	Extrinsic drain-source substrate region capacitance
$C_{gd}$	Intrinsic gate-drain junction resistance
$C_{GD}$	Extrinsic gate-drain junction resistance
$R_i$	Channel region gate-charging resistance
$R_{ds}$	Drain-source output resistance
$R_g$	Gate terminal series resistance
$R_d$	Drain contact resistance
$R_s$	Source contact resistance
$L_g$	Gate contact inductance
$L_d$	Drain contact inductance
$L_s$	Source contact inductance
$g_m$	Device transconductance
$\tau$	Time delay associated with $g_m$

$\tau_{SD}$  is the time delay of the current through the control region. The transition frequency  $f_T$  is also given by  $v_{sat}/\text{gate length}$  for the electron travel at saturated velocity  $v_{sat}$  [38, 49]. For the intrinsic field-effect device, the maximum frequency

of oscillation  $f_{max}$  (under small signal and linear operation) is given by [38]

$$f_{max} = \frac{f_T}{\sqrt{2\pi f_T C_{gd} R_g + \frac{R_g + R_s}{R_{ds}}}} \quad (2.29)$$

Ideally, the two different materials forming the heterojunction would have the same spacing between atoms (referred to as the lattice constant). However, in practice, the lattice constants are typically slightly different, such as in AlGaAs on GaAs, resulting in crystal defects. In semiconductors, these discontinuities form deep-level traps and greatly reduce device performance.

A HEMT for which this ideality is contravened, is called a pseudomorphic HEMT (pHEMT). This is achieved by using an extremely thin layer of one of the materials; so thin that the crystal lattice simply stretches to fit the other material. This technique allows the construction of transistors with larger bandgap differences than otherwise possible, resulting in even higher electron mobility [49, 62].

Another way in which materials of different lattice constants is used is to place a buffer layer between them, as in the case of metamorphic HEMTs (mHEMT). The buffer layer is made of AlInAs, with the indium concentration graded so that it can match the lattice constant of both the GaAs substrate and the GaInAs channel. This brings the advantage that practically any level of indium concentration in the channel can be realized, so the devices can be optimized for different applications. Further advantages lie in the lower manufacturing costs, better robustness and larger wafer sizes available with GaAs substrates. [49, 62, 63]. cut-off frequencies of mHEMTs are very similar to those obtained from HEMTs with similar gate lengths [49]. Table 2.4 presents a comparison between bipolar and field effect devices.



Table 2.4: Comparison of electrical parameters of bipolar and field-effect transistors. From [52] with modifications.

Parameter	BJT/HBT	FET
Input impedance $Z$	Low $Z$ owing to forward biased junction-large diffusion capacitance $C_{be}$	High $Z$ owing to reverse biased junction or insulator-small depletion layer capacitance $C_{gs}$
Turn-on voltage	Forward voltage $V_{BE}$ highly repeatable-Set by thermodynamics	Pinch-off voltage $V_p$ not very repeatable-Set by process variation
Transconductance	High $g_m$ ( $=I_c/(kT/q)$ )	Low $g_m$ ( $\cong v_{sat}C_{gs}$ )
Current gain	$\beta$ or $(h_{fe}) = 50$ -150; $\beta$ is important owing to low input impedance	Not meaningful at low frequencies and falls as $1/\omega$ at high frequencies
Unity current gain (cut-off frequency $f_T$ )	$f_T = g_m/2\pi C_{BE}$ is usually lower than for FETs	$f_T = g_m/2\pi C_{gs}$ ( $=v_{sat}/2\pi L_g$ ) higher for FETs
Maximum frequency of oscillation $f_{max}$	$f_{max} = f_T/(8\pi r_b C_{bc})^{1/2}$	$f_{max} = f_T(r_{ds}/R_{in})^{1/2}$
Feedback capacitance	$C_{bc}$ large because of large collector junction	Usually, $C_{gd}$ is much smaller than $C_{bc}$
Thermal noise [64]	Higher thermal noise due to $r_{bb}$ -resistive input	Low thermal noise due to channel ohmic resistance
Phase noise	Low phase noise, associated with low flicker $1/f$ noise in BJTs/HBTs	Very high $1/f$ noise corner frequency and phase noise
Thermal behaviour	Thermal runaway and second breakdown	No thermal runaway
Other		Backgating is a problem in semi-insulating substrates

The first MMIC DA, reported in a 1982 paper [22], was implemented in a  $1\ \mu m$  GaAs MESFET technology, and is shown in Figure 2.9. The amplifier reported 9 dB gain, from 1-13 GHz.

In Table 2.5, a performance summary of the state of the art for DAs based on MESFETs/HEMTs is presented, with information on the gain, bandwidth, GBP, NF, 1 dB compression point ( $P_{1dB}$ ) as a measure of the amplifier linearity,  $P_{dc}$ , the process technology, and year of publication with reference.

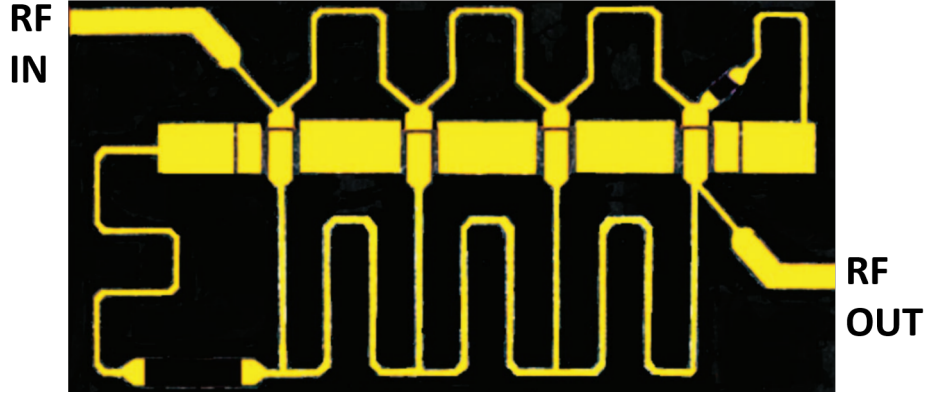


Figure 2.9: The first MMIC DA implemented on a  $1\ \mu\text{m}$  GaAs MESFET technology (size:  $2.5\ \text{mm} \times 1.65\ \text{mm}$ ) *Ayashli et al., 1982* [22].

Table 2.5: Performance summary of state-of-the-art MESFET/HEMT-based DAs.

Gain (dB)	Bandwidth (GHz)	GBP (GHz)	NF (dB)	$P_{1dB}$ (dBm)	$P_{dc}$ (mW)	Technology	Year/Reference
5.5	95	179	-	-	-	$0.1\ \mu\text{m}$ HEMT	1990/ [65]
10	89.2	282	-	-	860	$0.1\ \mu\text{m}$ HEMT	1995/ [66]
9	44	124	5.4	-	1,000	$0.2\ \mu\text{m}$ MESFET	1996/ [67]
7	111	248	-	-	-	$0.1\ \mu\text{m}$ HEMT	1998/ [68]
5	156	277	-	-	-	$0.1\ \mu\text{m}$ HEMT	1998/ [68]
5	180	320	-	-	-	$0.1\ \mu\text{m}$ HEMT	1998/ [68]
13.4	65	304	2.0	11	105	$0.15\ \mu\text{m}$ mHEMT	2002/ [69]
15	54	304	-	20	1,100	$0.15\ \mu\text{m}$ pHEMT	2002/ [70]
13	92	411	-	-	800	$0.1\ \mu\text{m}$ HEMT	2002/ [71]
22	39.9	503	-	10	484	$0.15\ \mu\text{m}$ pHEMT	2003/ [72]
12.5	50	211	2.5	-	400	$0.1\ \mu\text{m}$ mHEMT	2005/ [73]
20.1	34.5	349	-	25.1	1,300	$0.15\ \mu\text{m}$ pHEMT	2005/ [74]
13.2	41	187	-	24.6	1,860	$0.15\ \mu\text{m}$ pHEMT	2005/ [74]
19.2	37.5	342	2.3	12.6	131	$0.1\ \mu\text{m}$ pHEMT	2014/ [75]
21	80	898	-	-	-	$0.7\ \mu\text{m}$ HEMT	2015/ [76]
15.2	43.3	249	2.0	9.5	110	$0.1\ \mu\text{m}$ pHEMT	2018/ [77]

### 2.5.3 CMOS DAs

As earlier mentioned, the CMOS technology is becoming increasingly attractive for DA implementation due to the low cost and low power-consumption advantages that it offers. An additional driver of this trend is the proliferation of CMOS-based ICs, offering the possibility of integration of the DA with other baseband CMOS circuitry [36, 78]. The first CMOS DA, reported by Kleveland *et al.* in 1999, was implemented in a  $0.18\ \mu\text{m}$  process and measured 5 dB gain at 16.6 GHz band-

width [78]. Advancements in nanoscale CMOS technologies has made it possible to design CMOS DAs with significantly superior bandwidth performance, with a 110 GHz bandwidth DA based on 22 nm fully depleted Silicon-on-insulator (FD-SOI) CMOS process, representing the state of the art [79]. Table 2.6 summarizes the performance of state-of-the-art CMOS DAs.

Table 2.6: Performance summary of state-of-the-art CMOS-based DAs.

Gain (dB)	Bandwidth (GHz)	GBP (GHz)	NF (dB)	$P_{1dB}$ (dBm)	$P_{dc}$ (mW)	Technology	Year/Reference
5	87	155	-	-	90	120 nm SOI	2004/ [80]
9	81	228	505	10	130	120 nm SOI	2004/ [80]
8	59	148	302	12.5	132	90 nm SOI	2005/ [81]
7.4	80	188	-	8	120	90 nm	2005/ [82]
7	70	157	-	10	122	90 nm	2005/ [83]
19	44	392	-	-	57	90 nm	2006/ [84]
8	7	18	402	-	9	180 nm	2006/ [85]
9.8	43.9	136	-	-	103	130 nm	2007/ [86]
16.2	33.4	216	-	-	260	180 nm	2007/ [87]
20	39.4	394	-	-	250	180 nm	2007/ [87]
19	74	660	5.2	3.7	84	90 nm	2009/ [88]
15	12	67	2.3	8	26	130 nm	2009/ [89]
14	73.5	368	-	3.2	84	90 nm	2009/ [90]
24	33	523	605	7.5	238	180 nm	2011/ [91]
9	92	259	-	-	73.5	45 nm SOI	2011/ [92]
22	65	818	6.9	10	97	65 nm	2012/ [93]
7	61.3	137	-	-	60	90 nm	2013/ [94]
7	30	67	4	2	34	40 nm	2015/ [95]
8.5	110	292	-	-	80	22 nm FD-SOI	2017/ [79]
25	62	1102	-	-	107	28 nm	2018/ [96]

## 2.5.4 BiCMOS DAs

The BiCMOS process, which is a combination of the bipolar and CMOS technologies, has been used in the design of DAs with much higher bandwidth, when compared to CMOS processes. The technology combines the low power dissipation property of CMOS with the high switching and input/output speed and good noise performance of bipolar technology, resulting in devices offering improved speed over CMOS and lower power dissipation than bipolar devices. Table 2.7 summarizes the performance of state-of-the-art SiGe BiCMOS DAs.

Table 2.7: Performance summary of state-of-the-art BiCMOS-based DAs.

Gain (dB)	Bandwidth (GHz)	GBP (GHz)	NF (dB)	$P_{1dB}$ (dBm)	$P_{dc}$ (mW)	Technology	Year/ Reference
12	11	44	-	19.5	400	250 nm	2009/ [97]
13.2	29.4	134	-	-	136	130 nm	2010/ [98]
26	13	259	10.8	0	82	120 nm	2010/ [99]
10	110	348	-	16.7	119	130 nm	2011/ [100]
24	95	1,506	-	-	247.5	130 nm	2012/ [101]
10	170	538	-	7.5	108	130 nm	2015/ [102]
13	170	759	-	-	74	130 nm	2015/ [103]
18.7	180	1,550	6	-	86	130 nm	2015/ [104]
8.5	135	360	7	2	99	55 nm	2016/ [105]
12	91	362	-	14.9	297	90 nm	2016/ [106]
10	200	632	-	-	300	130 nm	2017/ [107]
16	175	1102	9.5	4.5	360	130 nm	2018/ [108]

## 2.6 Modifications to the Conventional DA

### 2.6.1 Gain Cell Modifications

A significant amount of the overall attenuation in a DA is due to the resistive elements present in the active devices employed. This is particularly more so in HBT-based DAs, where the presence of intrinsic series resistive element  $r_{bb}$  and extrinsic  $R_b$ ,  $R_c$  and  $R_e$  lead to significant power dissipation [32]. In addition, the loading effect arising from shunt resistances  $r_o$  and  $r_\pi$  also contribute to attenuation; however, as  $r_o$  is usually very large, it has minimal attenuating effect. With FET based DAs, attenuation due to series resistive elements is less of an issue as these tend to be lower when compared to HBTs.

#### 2.6.1.1 Phase Synchronisation

The velocity factor of a lossless transmission line is the ratio of the speed at which an electrical signal passes through the medium (i.e. its phase velocity,  $v_\phi$ ), to the speed of light in a vacuum, expressed by [109]

$$V_f = \frac{v_\phi}{c} = \frac{1}{c\sqrt{L'C'}} \quad (2.30)$$

where  $c$  is the speed of light in free space,  $L'$  is the distributed inductance (in henries per unit length),  $C'$  is the capacitance between the two conductors (in farads per unit length). Hence, the fact that the output capacitance, dominated by  $C_{ds}$  in FETs and  $C_{ce}$  in HBTs, is generally lower than the input capacitance, implies that the output ATL would have a higher velocity of propagation than the input ATL, resulting in phase mismatch as the signal arrives at the output terminal. This results in signal degradation from destructive interference. Phase synchronisation, also described as phase matching, refers to techniques adopted to equalise the the phase shifts on both the input and output ATLs. There are two commonly adopted approaches to achieving phase synchronisation: a series capacitance introduced at the input to match the resultant capacitance at the input to the output capacitance, also referred to as capacitive coupling [23, 110, 111]; or a series inductance introduced at the output to achieve a similar effect [43, 112]. These techniques are also described as phase matching

### Capacitive Phase Synchronisation

Capacitance phase synchronisation, also referred to as capacitive coupling was originally proposed by Ginzton *et al.* (1948), described then as *paired-plate* or *paired-grid* connection [21]. Much later, the general idea was adopted by Ayasli *et al.* in 1984, to mitigate the loading effect of the gate-source capacitance on the input line of the FET-based DA and improve power-handling capability [23]. With this technique the overall input capacitance can be made equal to the output capacitance by adding a phase-synchronising series capacitance  $C_{ps}$  at the gate/base terminal, as shown in Figure 2.10(a). An approximate value of the required capacitance value for  $C_{ps}$  can be obtained from the equivalent series capacitance relation. This is presented for bipolar transistors and FETs in (2.31) and (2.32), respectively.

$$C_{ps} = \frac{C_{\pi}C_{ce}}{C_{\pi} - C_{ce}} \quad (2.31)$$

$$C_{ps} = \frac{C_{gs}C_{ds}}{C_{gs} - C_{ds}} \quad (2.32)$$

In addition to the phase synchronisation achieved, this technique also results in bandwidth improvement, as the cut-off frequency of the input ATL is reduced. However, with this configuration, a voltage divider circuit is formed at the base/gate, such that the gain of the amplifier is reduced by the input signal voltage drop across the added series capacitance

$$V_{cps} = \frac{C_{ps}}{C_{ps} + C_{\pi/gs}} V_i \quad (2.33)$$

where  $V_{cps}$  is the voltage drop across  $C_{ps}$ ,  $V_i$  is the input voltage and  $C_{\pi/gs}$  represents the input capacitance for both bipolar transistors and FETs. In MMIC implementation, this loss can be reduced using a bigger HBT/FET and setting the value of  $C_{ps}$ , such that the higher proportion of the input voltage goes in through the base/gate of the transistor. Furthermore, the presence of a capacitor across the signal path potentially increases the low frequency cut-off. This effect is more severe with very high  $f_T$  HBTs and HEMTs, which possess relatively much lower  $C_{\pi}$  and  $C_{gs}$ , and require very low capacitance value for phase synchronisation. The combination of voltage divider setup also makes it possible to sample a desired portion of the input signal [23].

Furthermore, by varying the divider ratio along the gate line, it is possible to tailor the input excitation to individual gain cells, making it possible to increase the input power significantly. This extension to the capacitive coupling technique was initially proposed by Chen in 1967 [113], and is the origin of the non-uniform DA, which like the capacitive coupled DA is mostly adopted in the design of wideband power amplifiers [23, 114].

### Inductive Phase Synchronisation

This technique involves introducing an inductance  $L_{ps}$  between the collector terminal of the active device and the point of contact on the output ATL (as shown

in Figure 2.10(b)), to match the velocity of propagation of the signal travelling on the output ATL to that of the input ATL. A good approximation of the value of the phase synchronising inductance  $L_{ps}$  for bipolar transistors and FETs can be obtained by (2.34) and (2.35), respectively.

$$L_{ps} = Z_o^2(C_\pi - C_{ce}) \quad (2.34)$$

$$L_{ps} = Z_o^2(C_{gs} - C_{ds}) \quad (2.35)$$

This approach has been widely adopted in the design of MMIC distributed amplifiers [43, 112].  $L_{ps}$  also introduces an inductive peak that can be tuned to improve high frequency performance and gain flatness.

### 2.6.1.2 Cascode Configuration

In an inverting voltage amplifier, there is an increase in the equivalent input capacitance arising from a capacitance between the input and output of the amplifier. This phenomenon is termed the Miller Effect. This additional capacitance (which is not used in forming the ATL) is further amplified by the gain of the amplifier, giving it a significant adverse effect on high frequency performance. The cascode topology has been widely used in solving this problem [28, 67, 115–117]. It consists of a common emitter/source transistor feeding into a common base/gate transistor. This improves the input/output isolation, as there is no direct coupling between the input and the output, thus, eliminating the Miller capacitance. Also the higher output resistance of the common base/gate circuit helps to improve the gain of the amplifier [28]. The equivalent circuit for an HBT cascode is shown in Figure 2.11(a). The output impedance  $Z_{out}$  of the cascode pair for the field-effect based gain cell, is given by [67]

$$Z_{out} = \frac{Z_{ds1}}{Z_{ds1} + Z_{gs2}} \left( \frac{g_m Z_{ds2}}{j\omega C_{gs2}} + Z_{gs2} \right) + Z_{ds2} \quad (2.36)$$

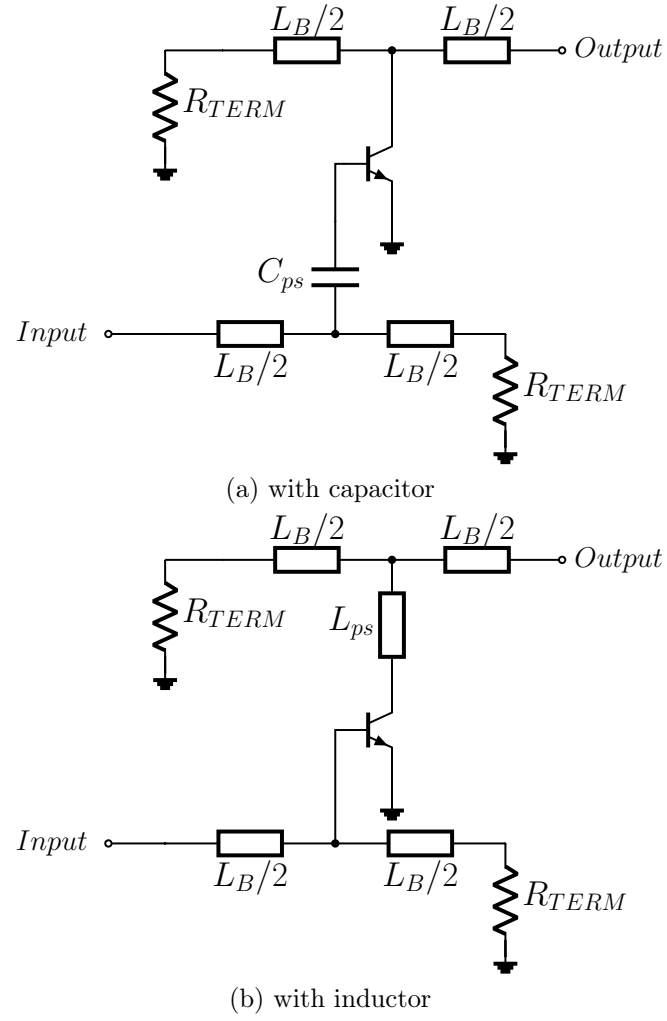


Figure 2.10: Capacitive and inductive phase synchronisation.



with an expression of the output impedance of the cascode pair for the bipolar based gain cell derived as

$$Z_{out} = \frac{Z_{ce1}}{Z_{ce1} + Z_{be2}} \left( \frac{g_m Z_{ce2}}{j\omega C_{\pi 2}} + Z_{be2} \right) + Z_{ce2} \quad (2.37)$$

### 2.6.1.3 Inductive-Peaked Cascode Loss Compensation

Inductive-peaked cascode loss compensation was introduced by Kimura *et al.* (1996) to improve the high frequency performance of the cascode configuration. The key feature of the technique is the addition of two inductors:  $L_{cg}$  (at the gate of the common gate transistor) and  $L_{sd}$  (between the common source and common gate transistors) of a cascode HEMT DA, as shown in Figure 2.11(b) [118].

The output impedance for bipolar and field effect based DA featuring this loss compensation technique is expressed by ((2.38)) and ((2.39)) [118], respectively.

$$Z_{out} = \frac{(Z_{ce1} + j\omega L_{ce})}{(Z_{ce1} + j\omega L_{ce}) + (Z_{be} + j\omega(L_{cb}))} \left( \frac{g_m Z_{ce}}{j\omega C_{\pi}} + (Z_{be} + j\omega(L_{cb})) \right) + Z_{ce} \quad (2.38)$$

$$Z_{out} = \frac{(Z_{ds1} + j\omega L_{sd})}{(Z_{ds1} + j\omega L_{sd}) + (Z_{gs2} + j\omega L_{cg})} \left( \frac{g_m Z_{ds2}}{j\omega C_{gs2}} + (Z_{gs2} + j\omega L_{cg}) \right) + Z_{ds2} \quad (2.39)$$

The addition of  $L_{cb}$  and  $L_{cg}$  reduces the value of the denominator of the first fraction in both equations (2.38) and (2.39), which increases negative resistance and consequently improves the high frequency gain. However, as the amplifier becomes unstable when the real part of the output impedance  $\text{Re}(Z_{out})$  becomes negative,  $L_{ce}$  and  $L_{sd}$  decreases  $Z_{ce}$  and  $Z_{ds1}$ , respectively, to dampen the effect of  $L_{cg}$  and maintain stability.

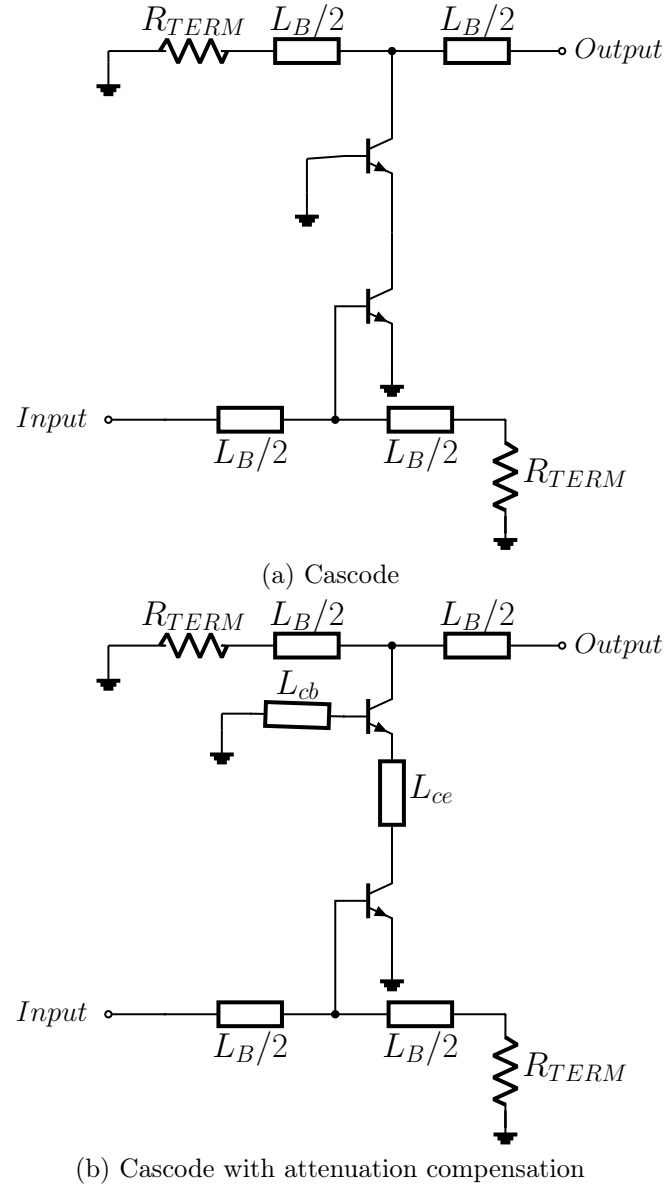


Figure 2.11: Gain cell modifications: conventional cascode and cascode with attenuation compensation.

## 2.6.2 Transmission Line Modifications

### 2.6.2.1 $m$ -Derived Sections

As pointed out in Section 2.3, the image impedance of a constant- $k$  filter has considerable frequency dependence across the passband. Hence, when it is terminated by a resistor, the mismatch would result in significant deterioration in filter passband performance. Furthermore, as attenuation does not increase rapidly as the cut-off frequency is approached, a wide transition band between the passband and stop-band [2, 28]. These drawbacks are significantly mitigated by modifying the constant- $k$ , sections to become what are commonly known as  $m$ -derived sections.

An  $m$ -derived section can be implemented using a single inductance value. This is based on the idea that for certain values of  $m$ , the series inductors and the inductor in series with the shunt capacitance can be made to be equal. For a full  $m$ -section, this value of  $m$  is found to be 0.577 and for mid-series  $m$ -sections (also called  $L$ -sections) the value is 0.707. The justification for this approach is that it reduces the number of unique inductors required to implement the DA, an important consideration in hybrid circuits featuring discrete inductors [119].

### 2.6.2.2 $L$ -Section Buffers

The  $L$ -section is a derivative of the  $m$ -section, also described as the half- $m$  derived section. It is often used as a buffer between the source, load and terminating resistances to convert these resistive elements into appropriate image impedances. This way, the terminating resistances are better matched to the transmission lines [41]. This is a widely used technique to improve matching and gain flatness at high frequencies [28, 36, 119]; with the bisected- $T$   $m$ -section being the more commonly used. In [119], it was observed that the  $\pi$ -half section results in better matching than the  $T$ -half section. With the bisected- $T$  section implementation, more passband ripples are observed as cut-off is approached, with the resultant effect of a less uniform group delay [119].

### 2.6.2.3 DC Matching Termination with Damping Resistors or $RC$ Network

The DC bias for the DA transistors is usually fed through the transmission lines. DC matching terminations are incorporated to achieve low frequency performance and also reduce power dissipation. Essentially, a shunt and a series resistance are incorporated at the idle ports - in place of the conventional series terminating resistance - to achieve flat gain from DC and reduce the effect of parasitic impedance at the bias terminal [118]. The value of the shunt resistor on the input line is typically close to the matching impedance, while the shunt resistor on the output line is higher. This is to compensate for the lower output impedance at low frequencies caused by the parallel connection of the output impedance of the cascode pair and the drain termination. An alternative approach is using an  $RC$  network in place of the shunt resistor. The purpose of the design is to have the termination impedance increase at high frequencies, to compensate for the decreasing output impedance of the conventional DA [67, 120]

### 2.6.2.4 Active Idle Port Termination

An active idle port termination has been considered to be a versatile DA design solution, as it can be used to feed the bias, achieve bias decoupling [7] and reduce noise on both the input and output ATLS [121]. To achieve amplification at very low frequencies, a large capacitor to ground is required to achieve effective bias decoupling. The input and output AC coupling capacitors in combination with the conventional  $50\ \Omega$  characteristic impedance provide a high-pass pole, at a frequency given by

$$f_{c-high} = \frac{1}{2\pi Z_o C_{coupling}} \quad (2.40)$$

where  $f_{c-high}$  is the high pass cut-off frequency and  $C_{coupling}$  is the capacitance of the decoupling capacitor. A capacitance value that is large enough to ensure

baseband performance can be difficult and often impractical to achieve with MMIC implementations, which features monolithically integrated metal-insulator-metal (MIM) capacitors with capacitance defined by area [117]. The active loads consist of an HBT in common-collector mode, which transforms a shunt load capacitance on the base to an effectively larger load capacitance when looking into the emitter. In this way an AC ground can be extended to lower frequencies using the active HBT with a relatively limited effect on chip size.

This termination method also provides advantages with regards to noise performance. The resistor terminating the input line of the DA causes a marked increase in noise figure at low frequencies [122]. An active termination, acts as an electronically-cold resistor - a low noise device that can be configured to emulate a one-port resistor [121, 123].

### 2.6.3 Multi-tier DAs

While the concept of distributed amplification would imply that the gain of a DA could be increased indefinitely, by the addition of more gain cells, without compromising bandwidth, practically, this is not the case. Losses due to resistive elements in the active devices and attenuation from the transmission lines builds up with the addition of gain sections, up to a point, after which adding another section is no longer beneficial [22, 28, 42]. The notion of an optimum number of stages had been initially suggested by Ginzton *et al.* in their seminal work published in 1948. However, the actual derivation and equation for this constraint, termed  $N_{opt}$ , was presented by Ayasli *et al.* (1982) as [22]

$$N_{opt} = \frac{\ln(\alpha_d l_d) - \ln(\alpha_g l_g)}{\alpha_d l_d - \alpha_g l_g} \quad (2.41)$$

Based on a more precise approximation of DA gain, given by

$$G = \frac{g_m^2 N^2 Z_o^d Z_o^g}{4} \left( 1 - \frac{\alpha_g l_g N}{2} + \frac{\alpha_g^2 l_g^2 N^2}{6} \right)^2 \quad (2.42)$$

a more compact approximation for  $N_{opt}$  is given by

$$N_{opt} = \frac{2}{R_{gs}\omega^2 C_{gs} Z_o^d} \quad (2.43)$$

Beyond  $N_{opt}$ , while increase may still be observed in low frequency gain, reasonably flat gain performance across the DA's bandwidth rapidly deteriorates. Higher gain may be achieved by introducing a multiplicative gain aspect to the additive gain property of the conventional distributed amplifier. There are two approaches to achieving this: cascading stages [21, 120] or forming a matrix with DA stages as tiers [117, 124]. Cascading DA stages to get more gain from DAs was initially proposed by Ginzton *et al.* in their 1948 paper and has been widely implemented [83, 120, 125]. The DAs are AC-coupled, such that the preceding tier delivers its output to the input of the next one, with the limit of the cascade stage being set by practical considerations, such as the dynamic range of the amplifier and its noise performance.

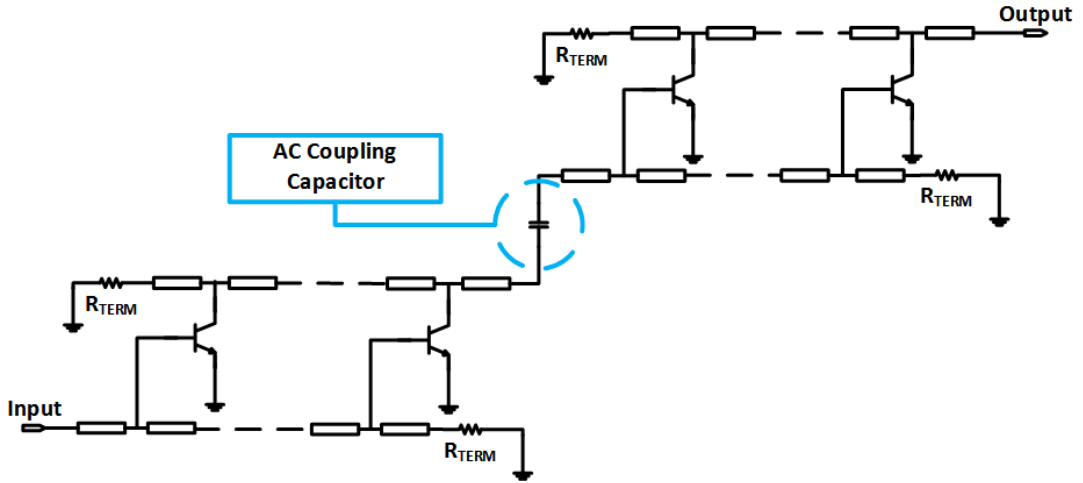


Figure 2.12: Schematic circuit of a cascaded DA.

The concept of the matrix DA is more recent, having been introduced by Niclas and Pereira in 1987. With this technique, DAs are stacked one on top of the other in a matrix structure with intermediate transmission lines serving as the connection between the layer below and the one above it. By convention, it features additive

gain in the horizontal direction and multiplicative gain in the vertical direction of the amplifier [124, 126–128].

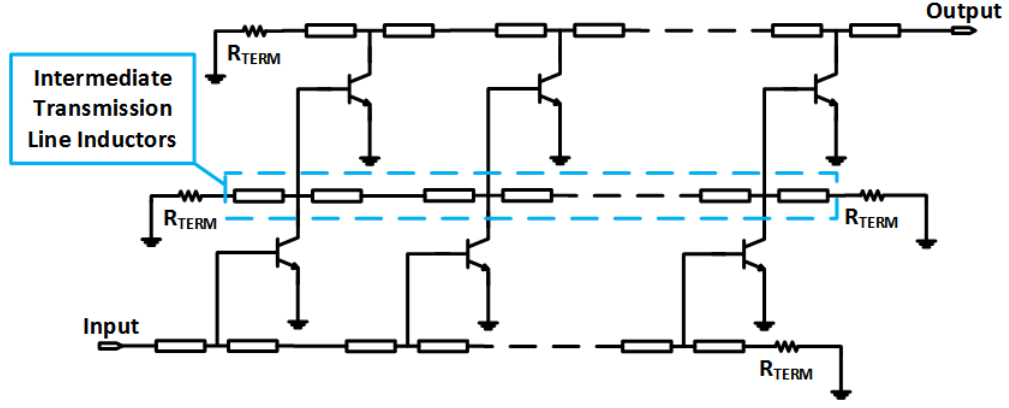


Figure 2.13: Schematic circuit of a matrix DA.

The main advantages of this structure over the cascaded DA arise from its reduced MMIC footprint, due to the shared intermediate line(s). The matrix topology is also highly suitable for monolithic integration, with a further advantage in the ease of adopting stacked biasing to lower the current consumption of the amplifier [117]. This will be further discussed in Chapter 5, where the M-SSDA - a variant of the matrix DA - is proposed. Both share a limitation imposed by the requirement of large inter-tier AC coupling capacitor, which may significantly increase the device footprint in MMICs.

## 2.7 Conclusions

As a general introduction to distributed amplification, this chapter has discussed the concept, gain and bandwidth mechanism and components of the DA. Major modifications to the conventional DA, to improve the bandwidth and gain performance have been reviewed. The cascaded and matrix amplifier topologies, which introduce a multiplicative aspect to the gain mechanism of the conventional DA, have also been described. For DAs, bandwidth and gain-bandwidth performance are usually considered as the main figures of merit. Hence, the state of the art in

DA performance for the various active device technologies has been considered. It has been observed that InP and SiGe have been particularly prominent in setting the state of the art in gain-bandwidth performance both in HBTs and BiCMOS processes.



# Chapter 3

## HBT Based DAs

### 3.1 Introduction

The concept of HBTs was first proposed and patented by William Shockley in 1951, in the original BJT patent; with the basic theory published by Kroemer in 1957 [129]. The HBT and BJT are based on similar operational principles, both being current-controlled bipolar transistors. The superior performance of HBTs over BJTs is due to improved base-emitter junction injection characteristics, arising from the presence of multiple junctions. Early HBTs were mostly AlGaAs/GaAs based. Contemporary high performance HBTs employ advanced material systems, such as the InAlAs/InGaAs/InP and InGaP/GaAs; offering improved speed, higher current gains, lower noise and better efficiency and reliability.

In this chapter, a review of HBT DAs reported to-date is presented, highlighting the effect of the evolution in process technology on performance; milestones achieved in performance based; reported applications and application-based designs; and modifications to the conventional structure. A review of analytical studies for predicting HBT DA gain, noise performance and stability is also presented.

Also presented in this chapter is a description of TSC250, the integrated circuit foundry process supplied by Teledyne Scientific Company, which is used in demonstrating the bandwidth enhancement concepts and novel DA implementation that are presented in Chapters 4 and 5. A brief description of the double heterojunction bipolar transistor (DHBT) device and presentation of the multilayer back-end process is presented in the first section. This is followed by a description of the pro-

cess of extracting small-signal parameters that closely approximates the foundry model. S-parameter comparisons of common-emitter amplifiers designed using the foundry model and the extracted small-signal model show close similarity, attesting to the effectiveness of the parameter extraction process employed.

## 3.2 Historical Review of HBT based DAs

The first HBT-based DA was reported by Nelson *et al.* in 1989 as an alternative to field-effect DAs, which were limited in their ability to simultaneously satisfy ultra low noise, low inter-modulation distortion and low DC power consumption requirements (Figure 3.1) [130]. The 4-staged amplifier covering 0.05 - 9 GHz frequency range, with 10 dB gain, exhibited remarkably improved linearity and better power performance (50 mW power consumption) over previously reported DAs based on MESFETs and HEMTs. However, the bandwidth performance of this amplifier was significantly less than the 39 GHz bandwidth reported for the state-of-the-art field-effect DA within the same time period [131]. A monolithic version of the hybrid HBT DA, originally reported, was presented in 1990, having a gain of 6-10 dB over the same 8.95 GHz bandwidth [132]. The bandwidth limitation could be partly attributed to the fact that the HBT IC process employed had an  $f_T$  of 20 GHz. Early research into HBT DAs was primarily based at the TRW Electronics and Technology Division in Redondo Beach, California, and most of the early reported circuits were by researchers at this institution.

As is to be expected, improvement in HBT process design technology continued to foster the design of faster and more efficient HBT DAs. Based on an HBT molecular beam epitaxy (MBE) profile with exponentially graded base doping, which results in reduced base transit time, lower base-emitter and collector-base capacitances ( $C_\pi$  and  $C_\mu$ , respectively), Kobayashi *et al.* [51, 133] reported a 2-24 GHz DA with 9.5 dB gain, with slightly higher power consumption. The amplifier featured a  $2 \times 3$  matrix structure, similar to the MESFET matrix amplifier reported

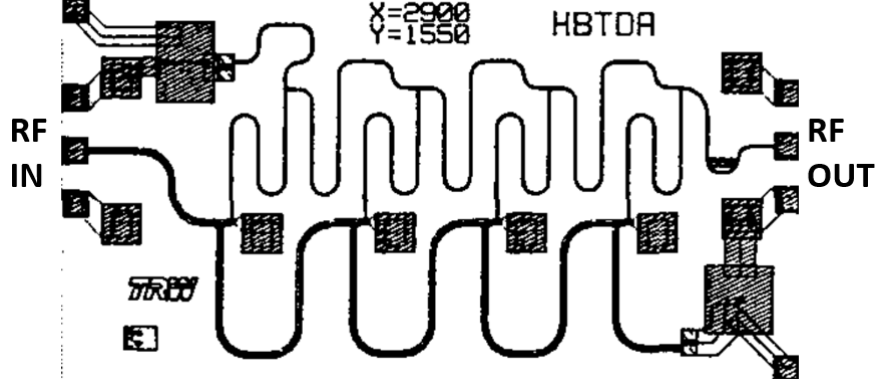


Figure 3.1: MMIC layout of the first HBT DA (*Nelson et al.*, 1989 [130]).

in [134]. In 1992, another matrix DA ( $2 \times 2$ ), with improved output  $IP_3$  and 1-dB compression point having a gain of 9.6 dB over 2-19 GHz, was reported by Chang *et al.* [135]. Using a technique described as exponentially-graded doping, as opposed to the previously reported graded composition method of producing built-in drift fields in the base of an NPN GaAs-AlGaAs HBT, Streit *et al.* (1991) [136] were able to significantly reduce the transistor base transit time  $\tau_B$  and increase  $f_T$  by 23%. However, at a gain of 9.5 dB and 24 GHz bandwidth, this was only a marginal improvement over the reported state of the art. Based on an InAlAs/InGaAs  $1 \times 4 \mu m^2$  single-emitter HBTs with a base under-cut structure (for reducing the collector-base capacitance  $C_{\mu}$ , resulting in up to 20% improvement in device  $f_{max}$ ), Kobayashi *et al.* (1996), reported a 5-section coplanar wave-guide HBT DA with 48 GHz bandwidth (2-50 GHz) - a 25% improvement over the previous state of the art [137]. This was followed by a 50 MHz - 55 GHz InP-based HBT DA [8]. The InP active device also featured the base-undercut technology and active load terminations on both the input and output transmission lines, to extend the low-frequency gain performance (similar to the design employed by Kobayashi *et al.* in [7]).

The transferred substrate HBT IC technology enabled the fabrication of HBT processes with very high  $f_T/f_{max}$  values. Agarwal *et al.* (1998) reported an 80 GHz bandwidth HBT DA based on this HBT technology with  $f_{max}$  greater than

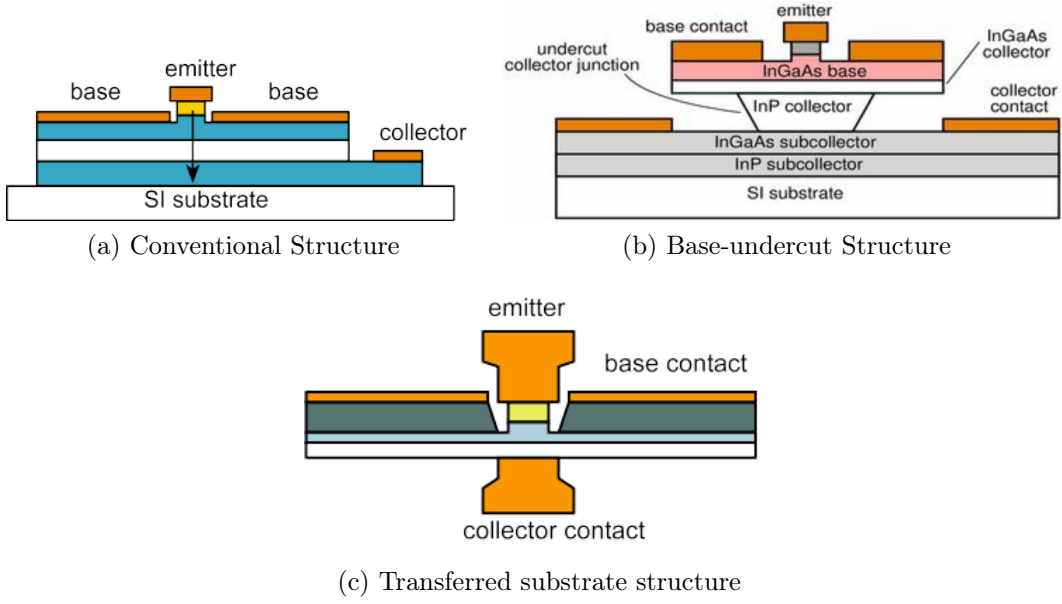


Figure 3.2: HBT process structures (Rodwell *et al.* 1999 [138], Rodwell *et al.* 2002 [133]).

400 GHz [44, 138]. Based on a transferred substrate InP process with  $f_T/f_{max}$  420/450 GHz, Kraemer *et al.* (2009) reported an HBT DA with 12.8 dB gain and a 3 dB cut-off frequency of 70 GHz [27].

While previous reports on performance improvement had been primarily driven by improvements in the active device, Kobayashi *et al.* (1994) reported the first DA circuit employing novel circuit-based modifications to improve bandwidth performance [116]. In the reported circuit, attenuation compensation was incorporated into the input line of the DA, by means of an active impedance transformation. A common-emitter device actively transforms a capacitive impedance at the emitter to generate a negative impedance at the base (input). On the output line, a cascode configuration was employed, which simultaneously increases output resistance and increases input-output isolation. A four-section HBT DA featuring this technique achieved a gain of 15 dB and a 3 dB bandwidth greater than 15 GHz from a 23 GHz  $f_T$  transistor. Based on a figure of merit that normalises GBP to  $f_T$ , this DA represented a 55% improvement over existing state-of-the-art performance. Aguirre and Plett (2003) reported a 0.1 - 50 GHz SiGe HBT employing

constant- $K$   $m$ -derived sections in the output transmission line [139]. The amplifier exhibited the a flatter-gain-with-sharper-roll-off property of  $m$ -derived filters compared the the basic constant- $k$  based DA. However, marked improvement was also reported in input line matching (evidenced by a better  $S_{11}$ ), which is unexpected considering that only the output line was reportedly modified. In [140], Meliani, Rudolph and Heinrich (2005) reported a technique to achieve DC to high frequency coverage by connecting two GaAs HBT DAs with compensatory properties. The low frequency gain of the first DA is increased by modifying the base-line terminating resistor and the collector series resistance of each cell. Each DA had 8 dB gain with 26 GHz 3 dB bandwidth. With the interconnect technique, the reported circuit achieved a total broadband gain of 14.5 dB.

Chang *et al.* (2011) [141] and Chen *et al.* (2012) [142] reported circuits, which featured cascode pairs, with two different transistor technologies. In [142], a SiGe HBT-NMOS cascode combination was adopted as the gain stage of the DA, while [141] had a GaAs HEMT-HBT cascode gain stage. However, apart from demonstrating the possibility of these implementations, the actual merit of the combinations and their effect on performance is unclear. Hoffman *et al.* [143,144] reported a MOS-HBT cascode on a 55 nm SiGe BiCMOS process. The combination takes advantage of the higher Q impedance of the MOSFET for DC coupling on the input line. Additionally, the MOS-HBT cascode exhibits higher linearity and better stability than the HBT-HBT cascode at the same bias current, with comparable maximum available gain and bandwidth. More recently, Li *et al.* (2016) reported a 10 to 170 GHz DA using three-level stacked 130 nm SiGe HBTs with 19 dB gain [59].

Wong *et al.* (1995) presented an AlGaAs/GaAs HBT high power fully-differential limiting DA operating at 10 Gb/s [29]. The amplifier was specifically designed to drive a III-V Mach-Zehnder modulator, which required up to 3 V peak-to-peak per arm at the modulating frequency for equal push-pull operation. A peculiar feature of this circuit was that the input transmission lines were driven by a front-end

amplifier on chip. The incorporation of a small input transistor at the front-end and on the same IC as the DA stage resulted in additional gain and lower input return loss. The first demonstration of power HBT DA based on a large-signal design approach was presented in [145]. The 0.5 W, 2 - 8 GHz MMIC HBT DA featured the addition of series capacitors between the CE amplifier and the input line, which while reducing gain, provides better gain compression characteristics for power operation. The amplifier design was based on a non-linear HBT model, which is more accurate for power amplifier simulations. Kobayashi *et al.* (2000) reported a capacitively coupled HBT medium power DA designed for 10 Gb/s fiber-optic transmitter applications [146]. The amplifier had a nominal 8 - 9 dB gain from 500 MHz to 16 GHz with frequency capability down to baseband, and delivered up to 19 dBm of output power, while operating at 420 mW - half the DC power of previous HBT modulator driver ICs reported in [26, 29, 145]. Fraysse *et al.* (2000) also reported a 2W, 2 - 8 GHz MMIC HBT power DA based on a non-linearly optimized HBT cascode cell. Series capacitances of increasing value were added between the common emitter of each stage and input line, to reduce the input capacitance of the cascode cell; and to compensate for the loss along the input line and equalize the input drive for each device. Krishnamurthy *et al.* (2013) reported an InP DHBT distributed power amplifier MMIC with 42 GHz bandwidth and 15 dBm output power [147]. The single chip solution employed a broadband lumped preamplifier to drive the distributed stage, achieving a mid-band gain of 34.9 dB.

The first HBT DA featuring CPW transmission lines was reported in [45] by Kobayashi *et al.* (1995). The 2 - 32 GHz DA was based on a InAlAs/InGaAs-InP process with  $f_T/f_{max}$  of 60/100 GHz and adopted the cascode gain cell topology to achieve its contemporaneously record bandwidth. However, for a DA with 5 gain cells, the gain of this amplifier - at 5 dB - was remarkably low. In an extended version of their 1995 paper, Kobayashi *et al.* presented this circuit configuration with active load terminations, to improve the DA lower frequency performance [7].

The resulting circuit had a lower bandwidth performance extended by two decades, resulting in performance below 45 MHz. As opposed to the conventional 'through-wafer' microstrip line implementation in MMICs, Schick *et al.* (2005) presented an HBT DA using highly lossy thin film microstrip lines, formed by the top- and lowest metal layers of the HBT process metal layer stack [148]. This was proposed as an option to the CPW type line, which is usually adopted in Si/SiGe based process with no backside metallisation and substrate vias.

In contrast to DAs based of field effect devices, HBT DAs are more prone to DC bias variations, with respect to variations in ambient temperature. This is primarily due to the inherent current-controlled nature of HBTs. Iqbal and Darwazeh (1997) described a novel MMIC area efficient method for DC bias stabilisation, with respect to ambient temperature variations, whilst also maintaining low frequency gain [149]. The commonly adopted technique for dealing with this is through a decoupling capacitor for emitter resistance  $R_e$ . However, due to the size limitations of MMIC devices, the capacitor size becomes a limiting factor to low frequency performance. The proposed technique involves the addition of an active bypassing circuit, which behaves like a low value resistor in parallel with  $R_e$ . This significantly reduces the effective resistance at the emitter terminal of the CE HBT, even at low frequencies, allowing gain to be maintained down to near-DC. This was practically demonstrated with a 23 GHz baseband HBT DA reported in [16].

Having established the practicability and merits of HBT DAs, a number of circuits in which the amplifier was proposed for application in transimpedance amplifiers, as drivers or mixers, were reported. The application of HBT DA approach to transimpedance amplifier (TIA) design, as opposed to direct coupled HBT-based topologies (such as the the common-base), was first demonstrated in [46]. Featuring an emitter follower (EF) input and cascode for loss compensation, the amplifier had a transimpedance-bandwidth product close to 2 times greater than previously reported conventional HBT-based direct-coupled topologies, when normalised to

$f_T$ . Based on similar circuit design techniques, Suzuki *et al.* reported a HBT DA for 40 Gbps time division multiplexing (TDM) optical transmission systems using an InP/InGaAs HBT technology [150, 151]. From a study of optimal design of high-gain HBTs, Mohammadi *et al.* described this topology (EF-cascode combination) as being most favourable high gain-bandwidth performance [9, 53]. Other fully integrated HBT DA for optoelectronics application include [152]. A 12 - 24 GHz HBT active balanced mixer based on the distributed topology was demonstrated by Kobayashi *et al.* in [153], with potential application as direct-conversion receivers. The MMIC mixer featured a distributed active balun design, which employed a HBT active intermediate-frequency center-tap combiner that both provides gain and also functions as an active load termination for the distributed local oscillator and RF baluns. Baeyans *et al.* (2003) reported a 2-stage InP DHBT differential driver featuring a lumped input and a distributed output stage. The amplifier, which recorded a differential gain of 25 dB and more than 50 GHz bandwidth, was considered capable for 40 Gbps transmission for non-return to zero (NRZ), return to zero (RZ), duobinary and differential phase shift keying (DPSK) transmission formats. Hosoya *et al.* (2003) reported an InGaP HBT IC chipset for 40 Gbps optical transmission. It included a 10.3 dB gain, 50+ GHz bandwidth; a 40 GHz analogue phase shifter and a 20 GHz/40 GHz clock amplifier. Hoffman *et al.* (2016) in [144] reported analogue electronic circuits for a possible 80 GHz bandwidth, frequency-interleaved, 4-level pulse-amplitude modulation (PAM4) or discrete-multitone (DMT) linear fibre-optic front-end implemented in a 90 nm SiGe BiCMOS technology. An 80 GHz bandwidth distributed optical modulator driver with a measured output compression point of 13 dBm per side, (corresponding to 7 Vpp output differential swing) was reported in a system which also included a vertically coupled 40 - 100 GHz bandpass filter and a 125 GHz bandwidth PIN-diode SPST switch.

Paoloni (2000) proposed a novel matrix topology that features HEMTs in the first tier and HBTs in the second [154]. Made possible by the introduction of



HEMT–HBT-selected MBE integration technology, the  $2\times 4$  matrix DA combined the electrical characteristics of the different transistor technologies to optimise performance. This circuit was however, not practically demonstrated.

While the linearity performance of HBT DAs had consistently surpassed field-effect based DAs, in terms of gain-bandwidth performance, HBT DAs lagged behind. However, in 1999, Baeyens *et al.* reported the first HBT DA with comparable gain-bandwidth product as the state of the art in HEMT DAs [155]. The 13 dB gain, 74 GHz bandwidth four-stage DA was based on InAlAs/InGaAs-InP HBT process with 160 GHz  $f_T$  and 140 GHz  $f_{max}$ . The circuit featured a coplanar layout and  $RC$  emitter degeneration network. Based on the condition that a bandwidth of at least 70% is needed to amplify NRZ signals, without significant degradation of the pulse shape, the amplifier was predicted as being capable of amplifying 100 Gbps NRZ data. As a TIA incorporating a PIN photodiode with parasitic capacitance of 50 fF, a transimpedance gain of 45 dB $\Omega$  with 70 GHz bandwidth. An added merit of the reported amplifier is that it was fabricated using optical lithography; a more cost-effective technique compared to the electron-beam written gate technology used in HEMTs.

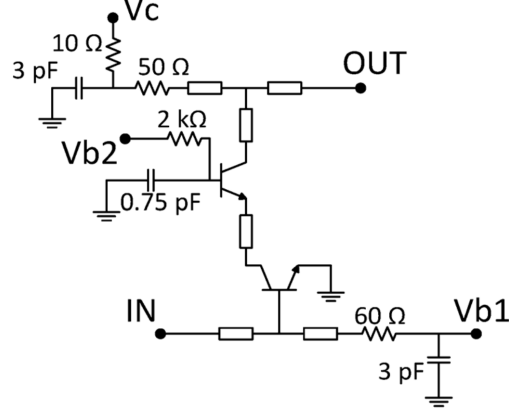
Baeyans *et al.*, in 2001, reported a seven section DA with a GBP of 495 GHz; the highest achieved with any process technology at that time [156]. In 2004, Arayashiki *et al.* reported a InGaP/GaAs HBT DA which had a GBP of 504 GHz (16 dB gain at 80 GHz bandwidth) [157]; another record holder. The amplifier featured gain cells with a novel two-block configuration, which enhanced the gain and bandwidth performance. Other HBT DAs with notably high performing GBP were reported by Wohlgemuth *et al.* in [158], which had 7 dB single ended gain (13 dB differential gain), with 81 GHz bandwidth, based on a SiGe HBT process; Cohen *et al.* in [159] and [160], with a bandwidth of 75 GHz and 14 dB gain, based on a InP HBT; and Yoon *et al.* in [58], with 10 dB gain from 40 to 222 GHz, based on a 250 nm InP HBT.

Following the remarkable performance recorded from the HBT DA reported by Baeyans *et al.* (1999) in [155], the utility of the HBT in achieving ultra-wideband amplifier performance was again demonstrated by Baeyans *et al.* (2006) in [161]. Using a 0.5  $\mu\text{m}$  InGaAs/InP DHBT with  $f_T/f_{max}$  of 337/345 GHz, they reported an five-stage DA with  $17\pm 1.5$  dB gain from 45 MHz up to 110 GHz. The unit cell consisted of a cascode stage buffered by a cascade of two emitter followers with resistor current sources for improved bias stability.

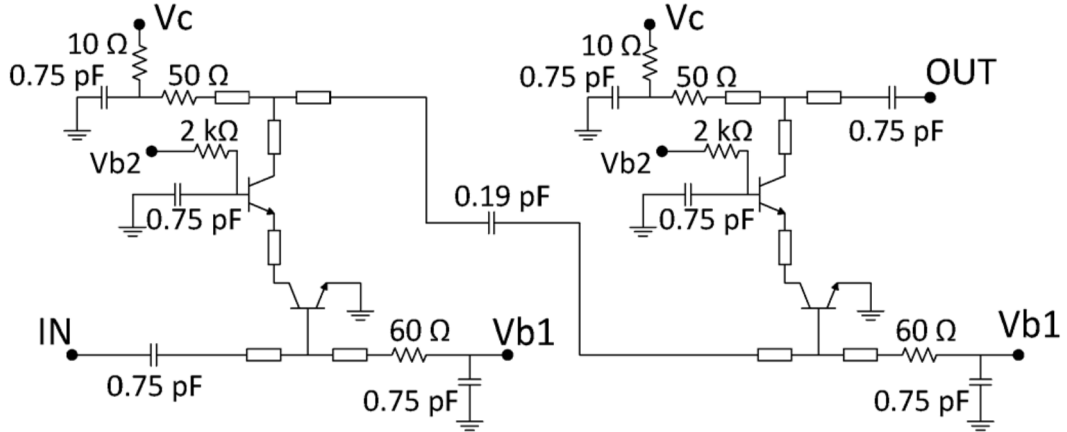
The practicability of SSDAs and C-SSDAs had been proposed by Liang and Aitchison in 1995 [162] and experimentally demonstrated in 1998, with a field-effect-based circuit reported by Benyamin *et al.* [163]. In 2003, Koon *et al.* proposed the first HBT based C-SSDA, which featured a commercially available SiGe/BiCMOS process [164]. The amplifier demonstrated a  $21\pm 0.5$  dB power gain over a frequency range of 300 kHz to 15 GHz in simulation.

In 2014, Eriksson, Darwazeh and Zirath reported two ultra-wideband InP HBT DA MMICs, one of which has remained the widest band amplifier in any technology to-date [120]. One, a single-stage DA design - with a cascode gain cell - achieved 7.5 dB gain and 192 GHz bandwidth (circuit schematic shown in Figure 3.3(a)); and the other, a 2-C-SSDA - also with a cascode gain cell - achieved an average gain of 16 dB with a bandwidth of 235 GHz (circuits schematic shown in Figure 3.3(b)). This work was extended from a conference proceeding to a journal paper, published in the IEEE transactions on Microwave Theory and Techniques in 2015, and reported a 3-staged cascode DA with more than 10 dB gain from 70 kHz to 180 GHz along with the SSDA and 2-C-SSDA [17]. These circuits are essential elements in the backdrop to the research reported in this thesis, as they reveal the potential of the relatively easy to implement SSDA in achieving ultra-fast amplifiers. It is instructive to note that all three circuits were based on the same foundry process - an InP DHBT process with 250-nm emitter width from Teledyne Scientific, with  $f_T/f_{max}$  of 350/650 GHz; and it presumed that all the circuits were optimised for the best gain-bandwidth performance. Hence, the fact that the 3-

stage DA reported in [17], and based on the same technology had less bandwidth than both SSDA based designs, points to the utility of the topology and presents grounds for further study.



(a) SSDA with cascode gain cell



(b) 2-C-SSDA with cascode gain cell

Figure 3.3: Circuit schematics of HBT SSDA and 2-C-SSDA (*Eriksson et al.* 2015 [17].)

Table 3.1 summarises the historical review of HBT DAs reported in open literature, showing notable circuits and design features.

### 3.2.1 Analytical studies of the HBT DA

A number of analytical models for HBT DA design have also been reported. In 1994, Botterill and Aitchison [166] presented an analytical expression predicting the small-signal gain of the HBT DA, assuming lossless lines and ideal termina-

Table 3.1: Historical review of HBT DAs: *a summary*.

Year, Reference	Technology	Topology	Gain (dB)	Bandwidth (GHz)	Feature/Comment
1989, [130]	3 $\mu\text{m}$ GaAs	4 stage CE	10	8.95	1st HBT DA
1990, [132]	3 $\mu\text{m}$ GaAs	4 stage CE	10	8.95	1st MMIC HBT DA
1994, [165]	GaAs	4 stage cascode	15	15	EF/Cascode with active impedance transformation
1995, [45]	1 $\mu\text{m}$ InAlAs/ InGaAs/InP	5 stage cascode	5	30	CPW transmission lines
1997, [149]	2 $\mu\text{m}$ InGaP/GaAs	4 stage cascode	15	23	Cascode with active DC bias stabilisation
1999, [155]	3 $\mu\text{m}$ InAlAs/ InGaAs/InP	4 stage cascode	13	74	1st to report GBP close to HEMT DA, Optical lithography
2002, [156]	0.5 $\mu\text{m}$ InGaAs/InP	4 stage cascode	13	74	1st to achieve comparable GBP with HEMT DAs
2003, [139]	SiGe BiCMOS	3 stage cascode	7	50	$m$ -Section output line
2003, [164]	SiGe BiCMOS	3-C-SSDA (CE)	21	15	1st HBT C-SSDA, active load, -ve impedance loss compensation
2005, [140]	GaAs	4 stage DA	14.5	26	2 interconnected DAs with complementary properties
2005, [148]	SiGe	6 stage cascode	13.6	32.2	Thin-film transmission lines, differential configuration
2011, [141]	2 $\mu\text{m}$ InGaP/GaAs	6 stage cascode	8.5	43.5	HBT-NMOS cascode
2012, [142]	0.18 $\mu\text{m}$ SiGe	10 stage cascode	8.2	31	HEMT-HBT cascode
2014, [120]	0.25 $\mu\text{m}$ InP	SSDA (cascode)	7.5	192	Record GBP SSDA
2014, [120]	0.25 $\mu\text{m}$ InP	2-C-SSDA (cascode)	16	235	Record bandwidth and GBP DA
2015, [17]	0.25 $\mu\text{m}$ InP	3 stage cascode	10	180	–
2016, [59]	0.13 $\mu\text{m}$ SiGe	5 stage cascode	8.2	31	3-level stacked structure

tions. The proposed expression demonstrated a predictive accuracy within approximately 1 dB of the simulated gain across the majority of the amplifier passband. This was followed in 1994 by a small-signal gain prediction model considering practical terminations [167]; and in 1995 by a report presenting analytical prediction for the small-signal gain of an HBT DA in dual-fed configuration [168].

Iqbal and Darwazeh (1996) introduced a new technique for modelling the HBT DAs, based on full hybrid- $\pi$  model of the HBT [15]. The reported model incorporated all feedback and parasitic elements associated with the transistor, resulting in significantly higher predictive accuracy. A unilateral HBT model for DA design oriented to a fast prediction of the performance of HBT DAs MMIC was also proposed by Paoloni and Agostino [169]. The model attempted to present the effects of HBT parasitics with a simpler and more intuitive expression than in previous models. Their paper also included a graphical design procedure based on a set of generalized charts as a simple design aid. To facilitate the design of low noise HBT DA based optical receivers, by providing an insight into how various param-

eters influence noise performance, Iqbal and Darwazeh (1999) derived expressions for the equivalent input noise current spectral density (EINCSD) of the amplifier [170]. Based on the analytical framework reported in their earlier paper [15], the derived EINCSD expression included noise from the HBTs, the photodiode and from line terminating impedances. This was followed by an analytical model for the transimpedance gain of a optical receiver, composed of a PIN photodiode and HBT DA [171]. A similar noise analysis was presented by Tian, Freundorfer and Roy (2003) for the first photoreceiver with on-chip PIN photodetector [172]; with good agreement obtained between predicted and measured noise performance.

Koon *et al.* (2001) derived what they described as optimal values for  $R_{be}$ ,  $R_{bb}$  and  $C_\pi$ , through simulation-based analysis of individual device parameter [173]. The effect of feedback base collector capacitance ( $C_\mu$ ) on GBP performance was also considered. It was suggested that extra active circuits may be added to achieve the optimal value of these parameters - such as reported in [116] if they cannot be realized for a practical device. However, the significance of the study is questionable, as no actual set of optimal values are presented. Furthermore, the technique adopted in the analysis, which involved varying a single parameter across a broad range while fixing all others, would result in parameter combinations that are nearly impossible or impractical to replicate in an actual device.

An analytical and experimental study by Melaini, Rudolph and Heinrich (2005) presented a relation between the optimal 3 dB cut-off frequency of the DA and the transistor frequency limits  $f_T$  and  $f_{max}$  [174]. Also reported was a small-signal analytical gain model, which considers small-signal parameters of the transistor equivalent circuit, the feedback resistor and the artificial transmission lines. A rather interesting conclusion was that for DA, cut-off frequency was more dependent on transistor  $f_{max}$  than  $f_T$ . Their amplifier was the only reported HBT DA in which the amplifier bandwidth exceeded the reported  $f_T$  of the process employed. The finding that  $f_{max}$  had a higher influence on cut-off frequency was again quan-

titatively demonstrated through a study of DAs based on two InP technologies with different  $f_T/f_{max}$  ratios - 190/120 GHz and 36/170 GHz.

Tian *et al.* (2003) [172] reported a noise analysis for the HBT common-collector cascode distributed preamplifier using methods similar to that adopted by Aitchison in [175], and Freundorfer and Nguyen in [176] for MESFET based designs. Hamidi *et al.* (2008) reported simpler but equally accurate expressions for the intrinsic noise figure of MMIC DAs, which is meant to be applicable to both MESFETs and HBT based designs.

### 3.3 Discussion

An obvious theme from the review of the reported HBT DA is the large part played by continually evolving process technology in the design of faster and more efficient DA circuits. This is due to the fact that the primary loss mechanisms of the ATLs are effects of parameters intrinsic to the transistor, rather than attenuation from the lines; thus, a significant portion of these performance limiting factors may and have been increasingly addressed with advancement in transistor design ([41,177]). Steady improvements in transistor technologies has lead to the realisation of HBTs with higher  $f_T$  and  $f_{max}$  values, which has in turn supported the milestone figures-of-merit achieved. Advanced MBE processes [51], exponentially-graded doping [136], base-undercutting [8] and transferred substrate technology [27,44] are some of the reported process technologies that have driven the recorded improvement in HBT DA performance.

However, the impact of improved transistor processes on performance metrics in no way lessens the importance of innovative circuit modifications and design techniques. Apart from the availability of better performing transistors, the remarkable performance recorded with HBT DAs has also being partly driven by such circuit modification as the adapted attenuation compensation cascode for improved input-output isolation and better high-frequency performance [165]; active termination for improved low frequency performance [7]; novel transmission

line synthesis for improved reflection performance [178]; optimised inductive peaking for high frequency gain compensation and improved gain flatness [17, 120, 177]. Several reports that compare results from the conventional design approach with newly proposed circuit modifications [7, 51, 131, 146, 165, 177, 179], have demonstrated that significant performance improvement can be achieved, thereby making these ideas well worth the effort that goes into conceptualising and implementing them. Indeed, it is arguable that without the advantage conferred by new circuit modifications and topologies, the utility of advanced transistor processes will be minimal.

A particular topology that has been identified from this review, for its remarkable utility in designing HBT DAs with ultra-wide bandwidth performance, is the single-stage cascode DA and its cascaded derivative. This relatively easy to implement topology was employed in the design of the first HBT DA to achieve a gain bandwidth performance that is comparable to the state of the art in HEMT-based DAs, which was dominating this aspect of performance at the time. Also, the amplifier that holds the current bandwidth record of any process technology and topology is the DHBT based C-SSDA cascode reported by Eriksson, Darwazeh and Zirath [17, 120]. Figure 3.4(a) and 3.4(b) show the MMIC chip photos of the SSDA and C-SSDA, respectively, as reported in [17].

Going by the underlying principles of distributed amplification and the synthesis of ATLs, as set out in the early studies on the subject, the idea of having a SSDA would be considered counter-intuitive. As described in Chapter 2, the ideal transmission line is of infinite length, with each section terminated in its own image impedance. Its realistic approximation, conceptually, is required to be as long as attenuative losses allow and terminated with a resistance. With these compromises, the bandwidth of the DA can, in theory, be extended to the unity gain limit of the active device; significantly reduced reflection is achieved on the resulting ATLs; and by process of additive gain, serviceable overall gain can be achieved with the amplifier. However, achieving unity gain at the widest

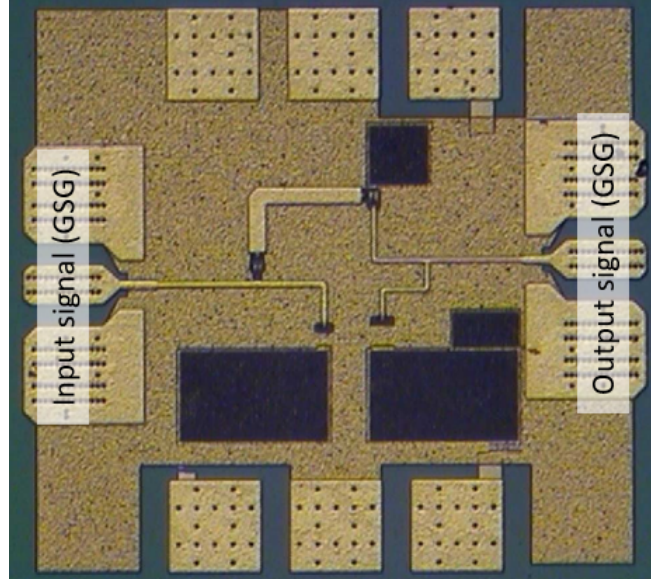
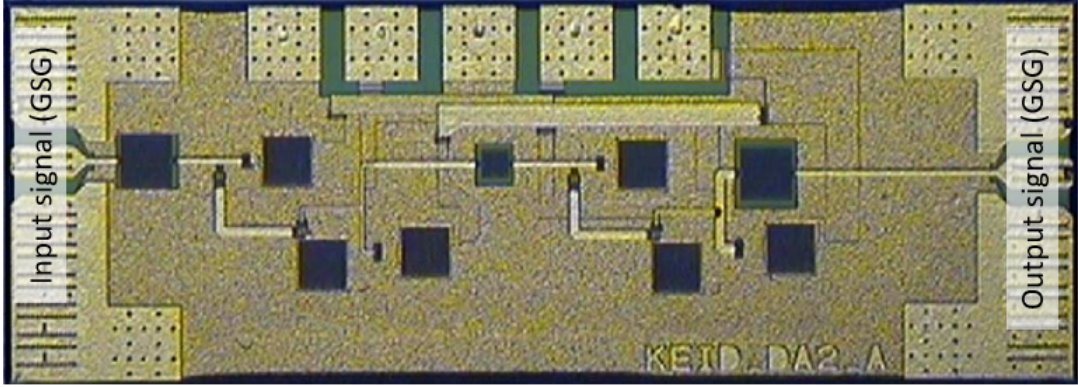
(a) Micro-photograph of SSDA ( $0.52 \text{ mm} \times 0.64 \text{ mm}$ )(b) Micro-photograph of C-SSDA ( $1.09 \text{ mm} \times 0.38 \text{ mm}$ )

Figure 3.4: [Microphotographs of two state-of-the-art HBT DAs (*Eriksson et al.* 2015 [17]).

bandwidth poses an impractical amplifier design target and it is more common that the single-stage power gain is high enough to justify C-SSDAs. Also, the addition of extra stages reduces overall bandwidth, as is observed in multi-stage filters. Furthermore, as the studies that introduced the SSDA show, the reduction in reflection with additional stages is only marginal and a significant measure of the required distributed effect can be achieved, even with a single stage. These observations from this review suggest an apparent suitability of the SSDA topology for ultra-wideband amplification and of HBTs as the active device in such designs



(this would be explored in Chapter 3.3.1). In latter chapters, efforts at circuits modifications with the intent of optimising the utility, particularly the gain and bandwidth performance of the HBT SSDA, are also presented.

### 3.3.1 Merits of HBT in SSDA Design

As described in Chapter 2 (Section 2.4.1), HBTs and HEMTs are high performance members of bipolar and field-effect transistor families, respectively. Both exploit the properties of heterojunctions to attain performance enhancements over their homojunction counterparts [52, 180]. Transistor heterojunctions are formed through the use of different semiconductor materials with different bandgaps. The material with the wider bandgap facilitates the injection of electrons into the narrower bandgap material, while also limiting the injection of holes occurring in the reverse direction. This allows a higher doping density to be used in heterojunction devices; a significant factor behind their improved performance (this is discussed with more details in the next chapter) [52].

Generally, HBTs possess some advantages over HEMTs that make them more attractive as active devices in DA design. This is primarily in the ability to deliver higher gains and better linearity than HEMTs of a similar generation [4, 5]. HBTs also offer better threshold voltage uniformity and low phase jitter properties (due to the low flicker noise property of bipolar devices), important requirements for ultra wide bandwidth optical receivers for high speed optical communication [7–9]. As transistor technology continues to move farther into the terahertz bandwidth range, driven primarily by InP-based heterojunction devices, some key advantages of the HBT over the HEMT have also been identified as making them more suitable in terahertz monolithic integrated circuits (TMICs) [10–12]. InP HBTs attain much higher breakdown voltage than HEMTs at a given  $f_T$ , due to the wide bandgap InP collector, making them well suited for ultra-wideband power amplifiers. Other properties, such as higher digital speed and low noise performance, make it possible to have an InP-HBT-based single IC platform in which all re-

ceiver and transmit components - low noise amplifier, voltage-controlled oscillator, mixer, local oscillator, phase-locked loop - can be constructed [3, 11, 13, 14].

However, with these advantages come some notable limitations. The fact that HBTs have resistive/capacitive inputs and output introduces some added complexity to its use in DAs [15]. While the input impedance of HEMTs can be closely modelled by a series  $RC$ , where the value of the resistance  $R$  is quite small, HBTs possess a more complex input structure [17, 22]. This is due to the presence of a forward-biased PN junction between the base and the emitter, resulting in a complex characteristic impedance that makes the design of line termination more challenging [15]. The resistive input characteristic also results in higher losses on the input ATL. Neglecting transmission line losses, approximate expressions of the input line attenuation per-stage for HBT ( $\alpha_{HBT}$ ) and HEMT ( $\alpha_{HEMT}$ ) DAs, are given by (3.1) [22] and (3.2) [17], respectively.

$$\alpha_{HBT} = \frac{1}{2} \sqrt{\frac{L_B}{C_\pi}} \left( \frac{1}{r_\pi} + \omega^2 r_\pi C_\pi^2 \right) \quad (3.1)$$

$$\alpha_{HEMT} = \frac{1}{2} \sqrt{\frac{L_G}{C_{gs}}} (\omega^2 R_i C_{gs}^2) \quad (3.2)$$

Additional attenuation arises due to dissipation of power in the series resistive elements  $R_b$ ,  $R_c$  and  $R_e$  (see Figure 2.7); the equivalents of which tends to be lower in FETs. This effectively introduces higher attenuation with each additional stage of the HBT-based DA, meaning that fewer stages can be realised compared to a FET-based DA before the overall gain begins to drop [15, 16]. Furthermore, while the HBT phase noise properties are superior to HEMTs, at low frequencies, HEMTs show superior noise figure because of low input shot noise. (The higher base resistance of HBTs results in poorer low frequency noise performance). Table 3.2 presents the merits and demerits of employing HBTs in DAs.

From the foregoing discussion, it can be said that HBTs have limitations that might make them less suitable - compared to HEMTs - in multi-stage DAs. How-

Table 3.2: Employing HBTs in DA design: *merits and demerits*.

<b>Merits</b>
<ol style="list-style-type: none"> <li>1. Higher gain and linearity [4, 5]</li> <li>2. Much higher breakdown voltage than in InP HBTs, compared to HEMTs with similar <math>f_T</math> [10–12]</li> <li>3. Low phase noise, associated with low flicker (<math>1/f</math>) noise [7–9, 38]</li> <li>4. Better high frequency noise performance [38]</li> <li>5. Higher switching (digital) speed [3, 11, 13, 14]</li> </ol>
<b>Demerits</b>
<ol style="list-style-type: none"> <li>1. Complex (resistive/capacitive) input nature [15, 17, 22]</li> <li>2. Higher attenuation from series resistive elements [15, 16]</li> <li>3. Higher input thermal noise generated by base spreading resistance [170]</li> </ol>

ever, this combination of properties make them particularly suitable for application in a SSDA. The higher gain and better linearity properties coupled with the stricter limitation on the number of stages due to the resistive input characteristics makes bipolar transistors better suited in SSDAs than in multi-stage DAs. Employed in SSDAs, the gain and linearity advantages of bipolar transistors can be harnessed with limited impairment from the deficiencies arising from the lossy input nature. Moreover, as there is less accumulated capacitance for a single-stage design, the transmission line length (and hence the inductance) can be reduced with little or no detrimental effect on the overall DA response. Employed in SSDAs, the gain and linearity merits of bipolar transistors can be harnessed with limited impairment to performance from the deficiencies arising from the described complexities. Furthermore, higher gain can be achieved by cascading [17, 120, 162, 163, 179, 181, 182] or - as will be described in Chapter 5, through a matrix of single-stage cascode DAs.

### 3.4 The TSC250 InP DHBT Process

TSC250 is an InP DHBT process from Teledyne Scientific, with an emitter width of 0.25  $\mu\text{m}$ . The DHBT is so-called because it uses a different material in the base, than in the collector and emitter, forming two heterojunctions in the device. Hence,

a material that can allow a higher doping concentration may be used in the base. Also, the base can be made thinner, resulting in a lower base resistance; properties that are both essential for high frequency operation. This, essentially, is how the DHBT offers higher  $f_T$  and  $f_{max}$  than is achievable with single-heterojunction bipolar transistors. Figure 3.5 shows a simplified schematic view of a DHBT process.

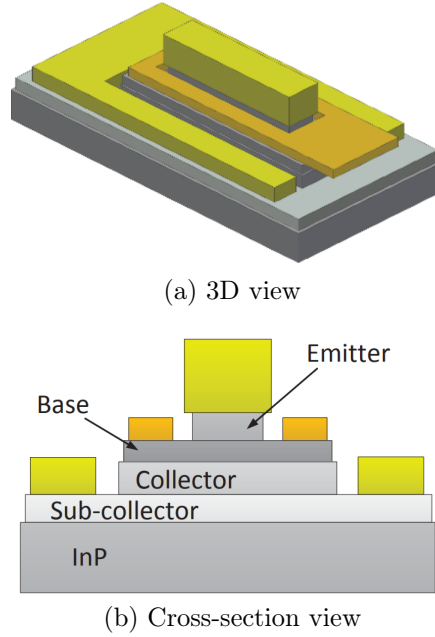


Figure 3.5: Simplified schematic of the TSC250 InP DHBT device [183].

TSC250 is fabricated on an InP substrate, a highly doped p-type InGaAs base lies between the n-type InP collector and InP emitter. It is an advanced bipolar process that relies on sub-micron transistor scaling to achieve state-of-the-art device performance. Devices in this family offer typical  $f_t/f_{max}$  values of 350/600 GHz, while maintaining a common-emitter breakdown voltage of more than 4 V [183]. This process was chosen for the designs reported in this thesis, particularly due to its high  $f_t/f_{max}$  values. An additional consideration is that the same process was employed in the design of the DAs that hold the world record bandwidth at the time this study was carried out.

The DHBT structure is grown using MBE on four-inch semi-insulating substrates. The epitaxy utilizes a 30 nm carbon-doped base layer and a 150 nm  $n$ -type InP collector region. The emitter contact is patterned using electron-beam lithography and formed using an Au-based electroplating process [11].

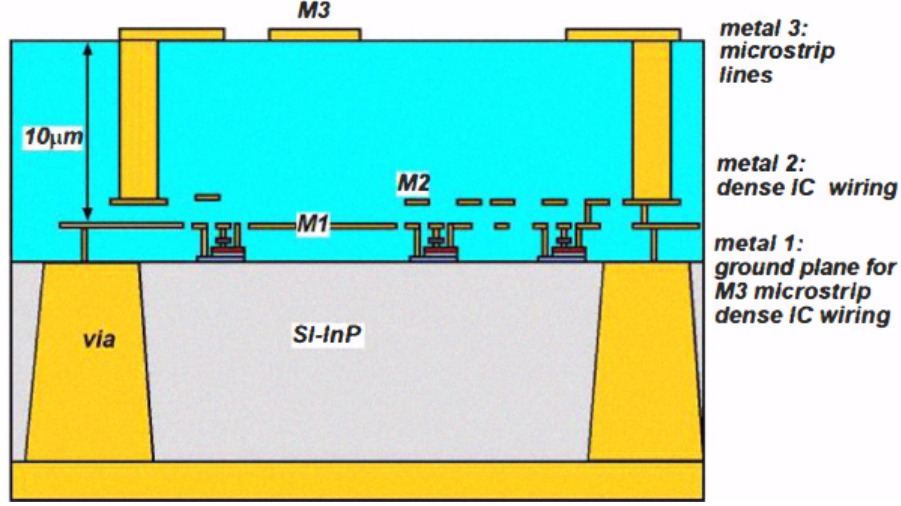


Figure 3.6: IC interconnect cross-section showing low loss THz microstrip lines and high density thin-film interconnects (*Hacker et al. 2010* [11]).

TSC250 is a 3rd-generation DHBT process, with emitter junction width of 256 nm. The device has a measured DC current gain of  $\sim 30$ . In this technology,  $0.25 \times 4 \mu\text{m}^2$  on-wafer S-parameter measurements show  $f_t/f_{max}$  of 378/808 GHz [11]. The IC process is a multi-layer interconnect back-end process with four metal layers (M1 to M4), separated by a  $1 \mu\text{m}$  benzocyclobutene (BCB) dielectric (with  $\epsilon_r = 2.6$ ). It features thin-film resistors (TFRs), with resistance at  $50 \Omega/\square$ ; MIM capacitors, and 3-levels of interconnect. A  $10 \mu\text{m}$  thick BCB layer is used between the 2nd and 3rd interconnect layers, to facilitate the formation of low-loss thin-film microstrip lines [11, 17]. The substrate thickness is  $10 \mu\text{m}$ , with the thickness of M1 - M3 being approximately  $1 \mu\text{m}$ , whereas M4 is  $3 \mu\text{m}$  thick to support higher current densities [17]. A schematic cross-section of the back-end process is shown in Figure 3.7 [183].

There are four layers of BCB (as seen in Figure 3.7) on top of the InP substrate and DHBT devices. Lying on each BCB layer is metal layers M1 - M4. These metal

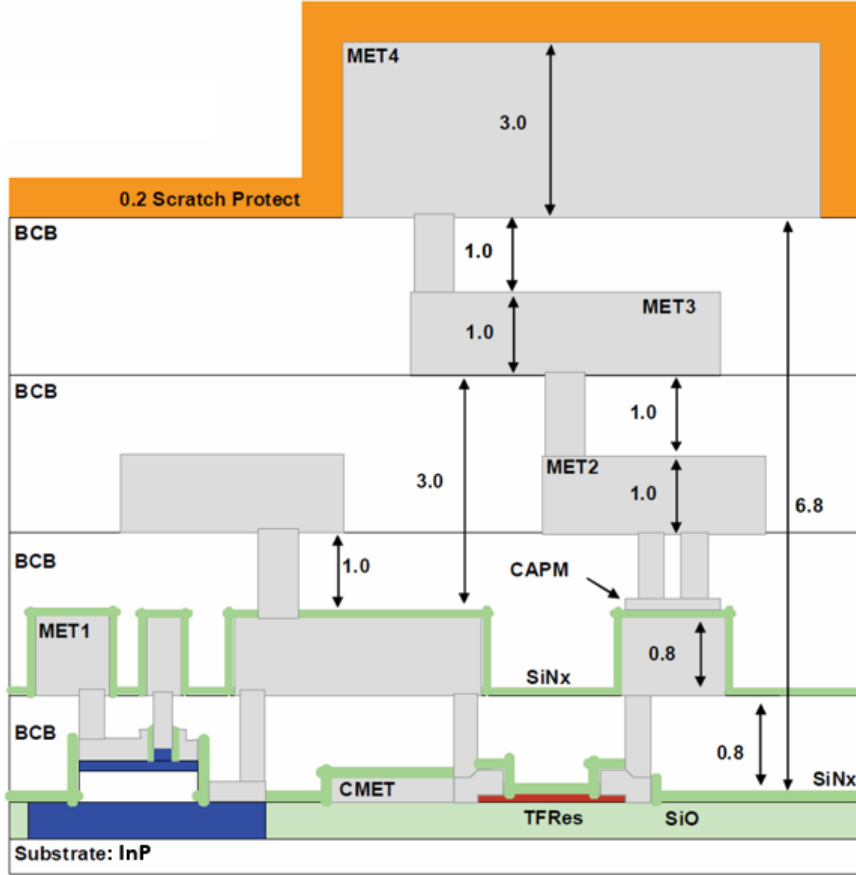


Figure 3.7: Representative cross-section of TSC250 IC technology. All dimensions in  $\mu\text{m}$  [183].

layers can be connected vertically through vias - holes etched through the wafer substrate and plated to achieve conduction. The DHBT devices, TFRs and MIM capacitors (between M1 and a dedicated metal layer CAPM, accessed through vias from M2) all exist on the same topographic level [184].

Thin-film microstrip lines (TFMLs) are preferred as interconnects at frequencies well beyond 100 GHz. They can operate at much higher frequencies than microstrip interconnects, which are limited to 100 GHz due to implementation constraints [184]. Alternatively, CPWs can be adopted, as they support higher frequency operation. They also permit low inductive connections to ground and offer minimal coupling between adjacent lines. However, CPWs, being more complex implementation, are also more difficult to accurately model [49]. The TFMLs

maybe realized using M4 as the signal layer and M2 or M1 as ground; such that the dielectric thickness adds up to 3  $\mu\text{m}$  or 5  $\mu\text{m}$ , respectively. The small thickness of the dielectric substrates allows the TFMLs to support higher frequency operation; thicker substrates will result in reduced wavelength and consequently lower frequency performance. While using M3 as ground may offer even higher frequency interconnect performance, due to the 1  $\mu\text{m}$  dielectric thickness between M4 and M1, there is the risk of unwanted coupling. Figure 3.8 is a three dimensional view of a section of a TSC250 MMIC, showing the TFML, TFR, MIM capacitor and via.

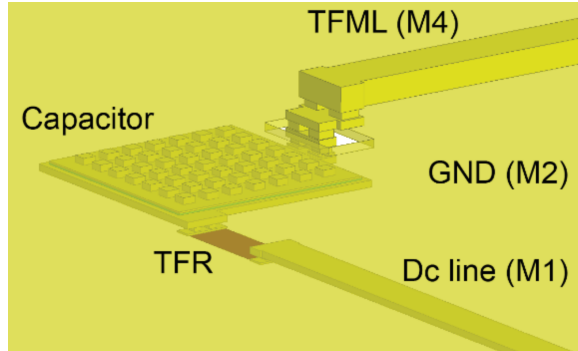


Figure 3.8: 3D view of MMIC section showing passive circuit elements: TFML, TFR, MIM capacitor and via (*Eriksson 2015* [17]).

### 3.5 Derivation and Verification of Equivalent Circuit Model

The device model used in the design and simulations of the circuits in this thesis is a large-signal model that is supplied by Teledyne Scientific. It is based on Keysight's III-V HBT model [17, 185]. The simulated DC characteristics of the DHBT device are presented in Figure 3.9.

To aid the design and optimisation of the circuits that were developed during the course of this study, parameters for a complete equivalent circuit model as described in Figure 2.7 were extracted from the full foundry large-signal model

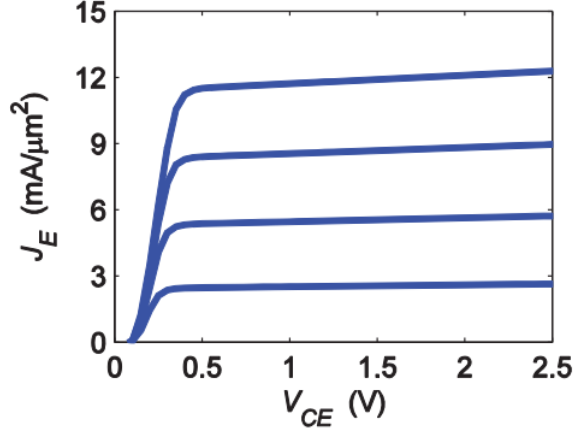


Figure 3.9: Simulated emitter current density,  $J_E$ , as a function of the collector-to-emitter voltage,  $V_{CE}$ , for different base currents,  $I_B$ , of TSC250. Emitter size:  $4\text{ }\mu\text{m} \times 0.25\text{ }\mu\text{m}$  with  $I_B$  stepped from  $100\text{ }\mu\text{A}$  to  $400\text{ }\mu\text{A}$  in  $50\text{ }\mu\text{A}$  steps (*Eriksson 2015* [17]).

of TSC250, supplied by Teledyne. The parameter extraction involved derivations from known transistor values, such as the  $f_T$  and  $f_{max}$ ; and a curve fitting process to obtain similar S-parameter performance from both models. First, after setting to the bias point that optimises the transistor  $f_T$  (described in the device datasheet), a basic single-stage common emitter amplifier was simulated to obtain the DC gain of the amplifier. From this, the current gain  $\beta$  and transconductance  $g_m$  of the amplifier at the set bias point was obtained. With  $f_T$ ,  $f_{max}$ ,  $g_m$  and  $\beta$  known, approximate values for intrinsic parameters  $C_\pi$ ,  $r_\pi$ ,  $C_\mu$  and  $r_{bb}$  were extracted using Equations (2.20) and (2.26).

As is common with bipolar transistors, a large resistance value was assumed for  $r_o$ . Having obtained good approximations for the all the intrinsic parameter, approximate values were chosen for the extrinsic parameters within the range expected, based on reported complete small signal model of an high  $f_T/f_{max}$  HBT [186]. Afterwards, using both the foundry model and the extracted equivalent model in common emitter amplifier mode, an iterative parameter-tuning process was used to obtain closely matching curves from DC to 500 GHz.

Figures 3.10(a) to 3.10(d) present S-parameter comparison of the model based on the extracted small-signal parameters, with the response of the model supplied



by the foundry for a common-emitter amplifier. For proprietary reasons, the actual values extracted for the small-signal equivalent circuit cannot be published at this time.

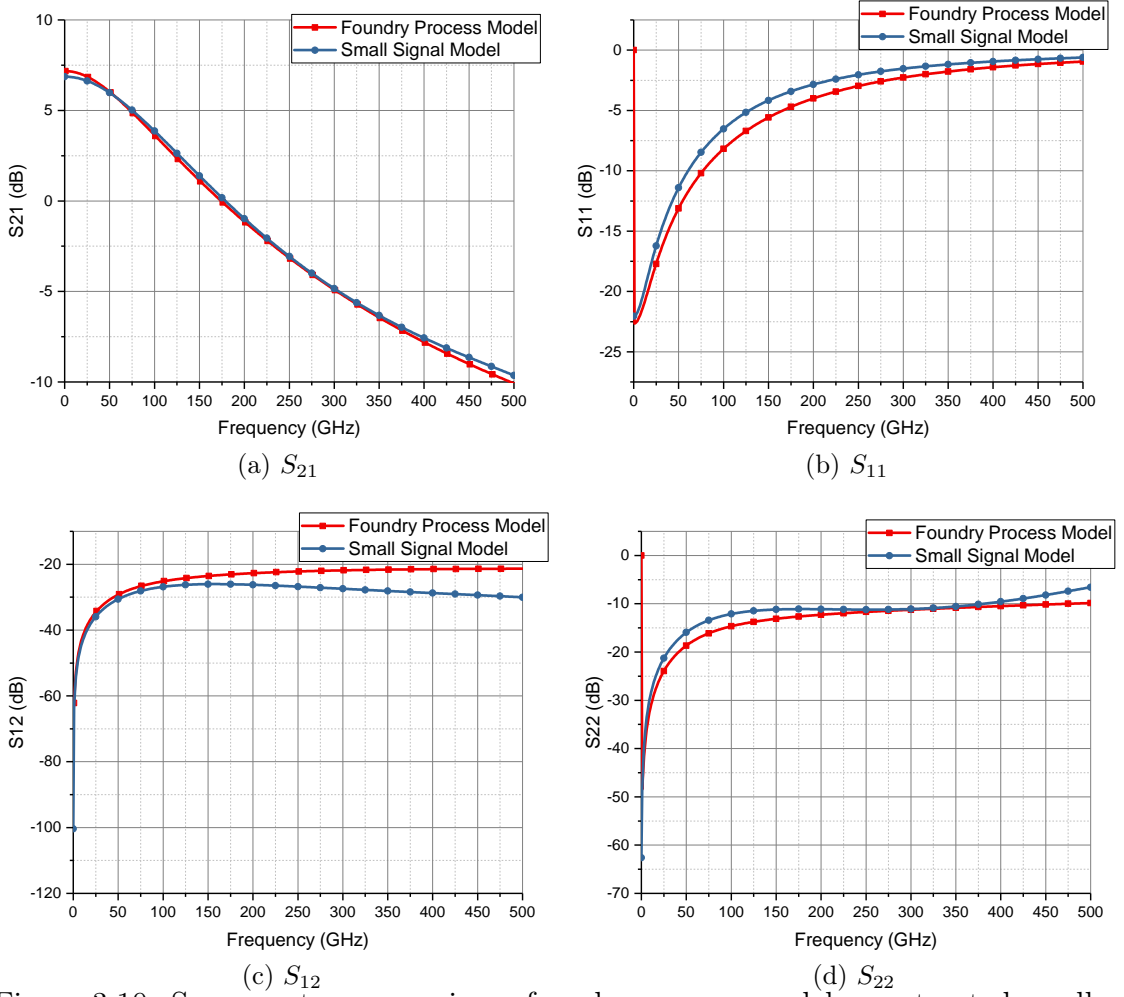


Figure 3.10: S-parameter comparison: foundry process model vs extracted small-signal model.

### 3.6 Conclusions

This chapter has presented a review of HBT DAs reported to date. The effect of improvement in transistor and integrated circuit technology; process modifications to the conventional design; application based designs; and performance milestones have been reviewed. A section of the review was also devoted to analytical studies

of the HBT DA, which has fostered a better understanding of the topic and has provided intuitive aids for the amplifier designer. A major takeaway from this review effort is the apparent suitability of HBTs for application in SSDA designs; evidenced by the contemporaneous state-of-the-art-performance achieved by DAs based on this topology and its cascade derivative. On one hand, the SSDA topology and its cascaded derivative take advantage of the higher transconductance and better linearity properties of the HBT, while on the other hand, by limiting the number of gain cells, losses due to the resistive input nature of HBTs is minimised. In Chapters 4 and 5, new bandwidth extension techniques for the SSDA, and a new SSDA derivative topology, respectively are presented. The purpose of which is to extend the performance and utility of SSDAs.

The TSC250 InP DHBT process supplied by Teledyne Scientific, which is used to validate the techniques presented in this thesis, has also being described in this chapter. The techniques and topology presented in the Chapters 4 and 5, respectively, are demonstrated in simulation using TSC250. The process of extracting an equivalent small-signal circuit model from the full foundry large-signal process model, supplied by the device manufacturer, has also been described and the resulting model verified for accuracy.

# Chapter 4

## Artificial Transmission Line

## Modifications for Bandwidth Enhancement in SSDAs

### 4.1 Introduction

The DA was originally conceived as a multi-celled additive amplifier [21], with four and five stages being more commonly reported. While the distributed effect that gives the DA its bandwidth advantage can be achieved with a single gain stage, it was expedient to have as many gain stages as possible, to minimise the reflection from the poorly matched resistive termination, particularly at the end of the input ATL. In addition to this, due to the gain/bandwidth trade-off, it is often the case that in designing DAs, the gain of a single stage is made low (close to unity gain) to maximise bandwidth; thus making the concept of additive gain more effective than the multiplicative gain possible through cascading [21, 28].

However, in 1981, Nwaogu and Aitchison demonstrated the concept and practicability of SSDAs [187]. The reported MESFET SSDA had a gain of  $5 \pm 1$  dB with 5.5 GHz bandwidth, a modest performance at the time. More importantly, the fact that a basic SSDA, as they reported, could achieve that much gain and gain flatness paved the way for the design of C-SSDAs, which retained the gain flatness and bandwidth of the conventional DA but with much higher gain from the multiplicative effect of the cascade arrangement [188]. Furthermore, advancement in transistor design has allowed the design of SSDAs with much higher GBP,

leading to even higher GBP values from cascading two or more SSDAs than with a conventional DA employing the same number of gain cells [162, 179, 188].

An additional motivation for SSDA designs is the potential for better bandwidth performance. Considering that both the input and output ATLs of a DA are essentially filters; and from foundational works on filter theory [189], it has been established that the degree of attenuation at and beyond cut-off increases with the number of filter stages, such that with an infinite number, of stages a perfect filter - one with zero insertion loss and a linear phase response in the pass-band and near-infinite attenuation in the stop-band - can be achieved. However in DA designs, where the aim is to extend the bandwidth as much as possible, there is an advantage to having minimal attenuation beyond the cut-off frequency of the input line. With lower attenuation, high frequency attenuation compensation techniques, such as inductive peaking and application of negative resistance, can be more easily applied on the output transmission line. This way, bandwidth extension can be achieved.

As highlighted in the the previous chapter, bipolar transistors possess a combination of characteristics that make them particularly suited for SSDA design. This chapter describes bandwidth extension techniques for the HBT SSDA, based on modifications to the transmission lines. These techniques allow the design of SSDAs with bandwidth closer to the active device transition frequency  $f_T$ . The described techniques may also be applied to FET-based SSDAs.

## 4.2 Design Concept

Figures 4.1(a) and 4.1(b) show simplified equivalent circuits of the input and output ATLs of an HBT SSDA, respectively. The lines are made up of intrinsic capacitance  $C_\pi$  and  $C_{ce}$  and inductive lines  $L_B$  and  $L_C$ ; with both lines coupled by the transistor transconductance  $g_m$ . Resistances  $r_\pi$  and  $r_o$  are the transistor base-emitter junction resistance and output resistance, respectively, and  $R_{\text{TERM}}$  is the terminating resistance.

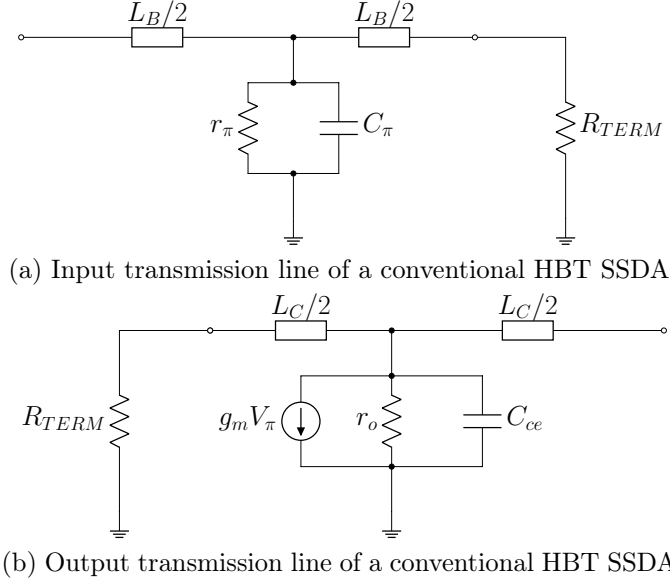


Figure 4.1: Simplified equivalent circuits of the input and output ATLs of a conventional HBT SSDA.

Equations (4.1) and (4.2) are derived to estimate the line impedances of the input ( $Z_{in}$ ), and output ( $Z_{out}$ ) transmission lines, respectively of a simplified conventional SSDA.

$$Z_{in} = \frac{j\omega L_B}{2} + \frac{r_\pi (j\omega \frac{L_B}{2} + R_o)}{r_\pi + (R_o + j\omega \frac{L_B}{2}) (1 + j\omega r_\pi C_\pi)} \quad (4.1)$$

$$Z_{out} = \frac{j\omega L_C}{2} + \frac{r_o (j\omega \frac{L_C}{2} + R_o)}{r_o + (R_o + j\omega \frac{L_C}{2}) (1 + j\omega r_o C_{ce})} \quad (4.2)$$

The design technique proposed is a three-step process, involving two modifications to the input line of the conventional SSDA and one to the output line.

#### 4.2.1 Input Line Modification

As it has been established in Chapter 2, the bandwidth performance of a DA is mainly limited by the cut-off frequency of the input line [21, 28]. This is due to the fact that the input capacitances of both bipolar and field-effect transistors is usually larger than their output capacitances. Hence, by the image impedance design approach employed in conventional DA, the input line would have a lower

cut-off frequency, which will dominate the DA bandwidth performance. Therefore, as this is the main bottleneck, increasing the 3 dB cut-off frequency of the input ATL results in an increase in bandwidth of the DA. This is achieved in two steps:

**Step 1: Increase the 3 dB cut-off frequency of input line by scaling down the line length (inductor value, if discrete components are used)**

Transmission line scaling involves the reduction of the inductance on the input ATL, effectively altering the  $L$ - $C$  ratio. The effect of the termination mismatch on the forward gain is compensated for through basic inductive peaking [58, 190] or the more effective negative resistance attenuation technique that features a cascode and inductive lines [118, 165]. The technique exploits the fact that the frequency response of an SSDA has a single gain ripple, as there is just one pole in its transfer function. This makes it relatively easy to achieve a flat gain with the output line compensation techniques.

Recall that the image impedance of the input transmission line ( $Z_{o-in}$ ) is given by

$$Z_{o-in} = \sqrt{\frac{L_B}{C_\pi} \left( 1 - \frac{4\pi^2 f^2 L_B C_\pi}{4} \right)} \quad (4.3)$$

with  $C_\pi$  being the base-emitter capacitance of the common emitter amplifier;  $L_B$  being the inductance value required to achieve the distributed effect; and  $\omega$  being the angular frequency. With the cut-off frequency of the line,  $f_c = 1/\pi\sqrt{L_B C_\pi}$  (for ideal lossless lines). At this frequency, the image impedance transitions from being purely real to being purely imaginary if the line is terminated with the DC value of  $Z_{o-in}$ , denoted by  $Z_{o-in}^*$  such that

$$Z_{o-in}^* = \sqrt{\frac{L_B}{C_\pi}} \quad (4.4)$$

The cut-off frequency may be extended by scaling  $L_B$  by a factor,  $\zeta$  (with  $\zeta < 1$ ), while keeping the terminating impedances  $R_{TERM}$  at the value of  $Z_{o-in}^*$ . This results in cut-off frequency  $f_{c'}$  that is

$$\frac{1}{\pi\sqrt{L_B C_\pi}} < f_{c'} < \frac{1}{\pi\sqrt{\zeta L_B C_\pi}} \quad (4.5)$$

For  $f_{c'} = 1/\pi\sqrt{\zeta L_B C_\pi}$ , the terminating impedance must be reduced such that  $R_{TERM} = \sqrt{\zeta L_B / C_\pi}$ . However, this would lead to a corresponding reduction in gain, as

$$Gain = N g_m \frac{\sqrt{Z_{o-in} \cdot Z_{o-out}}}{2} \quad (4.6)$$

$Z_{o-in}$  is the input line image impedance;  $Z_{o-out}$  is the output line image impedance and  $N$  is the number of gain stages. By terminating with  $Z_{o-in}^*$ , the gain is kept at the same level as will be obtained from a conventional DA.

In modelling the gain of the DA, it is often implicitly assumed - for simplicity - that the transmission lines are image-impedance terminated [21], [15], [166], [169]. However, as established in Chapter 2, this can only be achieved in the ideal scenario with an infinite length of transmission line with equal image impedance at each section, hence the need for a resistive termination. The input line modifications, considering that the line is purposely mismatched with its termination to maintain overall gain at pre-modified levels; deviates even further from the ideal matching scenario. Equation (4.8) describes the image impedance  $Z_{o-in}^*$  of the line-scaled input transmission line.

$$Z_{o-in}^* = \sqrt{\frac{\zeta L_B}{C_\pi} \left( 1 - \frac{\omega^2 \zeta L_B C_\pi}{4} \right)} \quad (4.7)$$

This is adjusted with the addition of  $Z_{adj}$ , given by

$$Z_{adj} = \left( \sqrt{\frac{L_B}{C_\pi}} - \sqrt{\frac{\zeta L_B}{C_\pi}} \right) \left( \sqrt{1 - \frac{\omega^2 L_B C_\pi}{4}} \right) \quad (4.8)$$

to approximate the effect of the mismatched termination for gain modelling. For DAs featuring the proposed scaled input-line technique,  $(Z_{o-in}^* + Z_{adj})$  replaces the input line image impedance in existing gain models, such as presented in [21], [15], [166], [169], as otherwise, such models would be rendered inaccurate for the proposed design.

From (5.4), the line impedance  $Z_{in}^*$  of the scaled input line is

$$Z_{in}^* = \frac{j\omega\zeta L_B}{2} + \frac{r_\pi \left( j\omega\frac{\zeta L_B}{2} + R_o \right)}{r_\pi + \left( R_o + j\omega\frac{\zeta L_B}{2} \right) (1 + j\omega r_\pi C_\pi)} \quad (4.9)$$

Figure 4.2 shows the gain in bandwidth with incremental scaling for a hypothetical HBT with  $C_\pi$  of 50 fF and 50  $\Omega$  termination. It is interesting to note that for negligible line losses, the bandwidth is always extended with scaling at the expense of slight degradation in the passband gain profile.

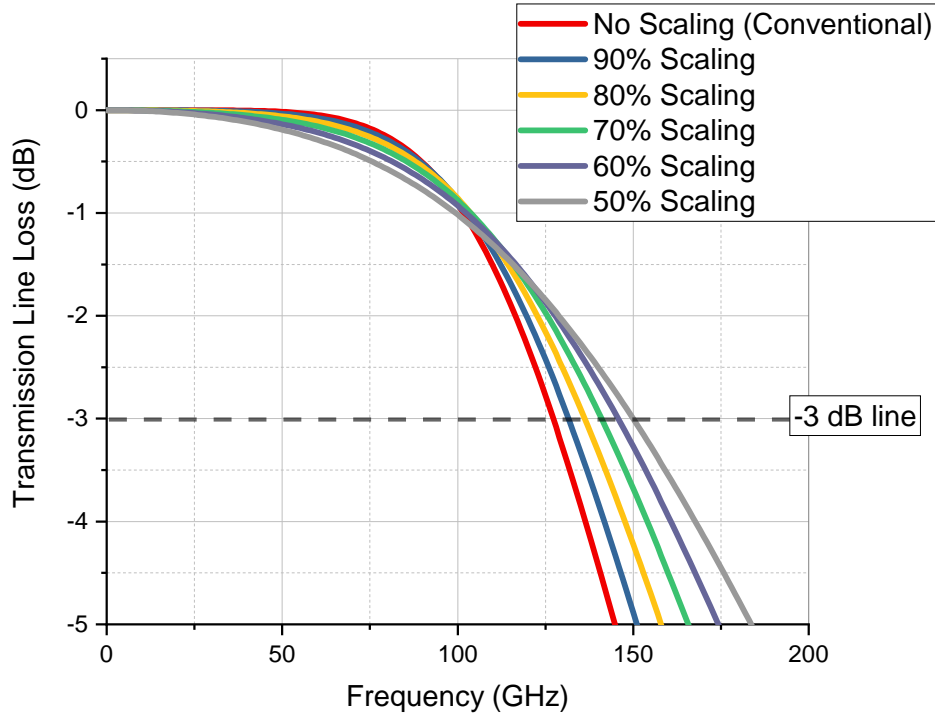


Figure 4.2: Bandwidth improvement from transmission line scaling.



**Step 2: Introduce a high frequency peak through a shunt capacitance**

To increase the bandwidth of the input line further, a shunt capacitor  $C_{peak}$  is added, resulting in a high frequency resonant peak ( $f_{peak}$ ), given to a good approximation by

$$f_{peak} = \frac{1}{2\pi\sqrt{\zeta L_{CB} C_{peak}}} \quad (4.10)$$

Significant improvement in the 3 dB bandwidth of the input line can be obtained by optimizing the values of  $C_{peak}$  and  $\zeta$ . The impedance  $Z_{in}^{**}$  of the resulting transmission line is

$$Z_{in}^{**} = \frac{Z_{in}^*}{1 + j\omega C_{peak} Z_{in}^*} \quad (4.11)$$

Figure 4.3 shows the effect of various capacitance values (normalised to  $C_\pi$ ) on the frequency response of the transmission line.

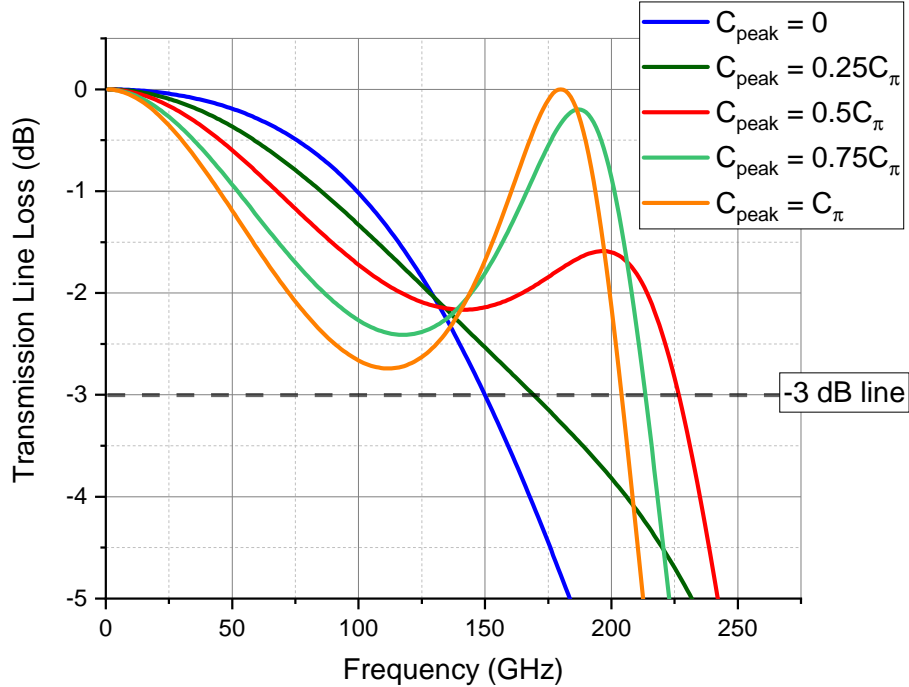


Figure 4.3: Effect of shunt capacitance on frequency response of 50% scaled transmission line.

To demonstrate the utility of the described concepts, Figure 4.4 compares the bandwidth (in terms of transmission loss) of a conventional image impedance line with a 50% scaled line, a peaked line, and a line that features both 50% scaling and peaking for a transmission line with capacitance of 50 fF and 50  $\Omega$  termination. In both cases where peaking is applied, the value of the peaking capacitor is individually optimized to yield the best bandwidth performance.

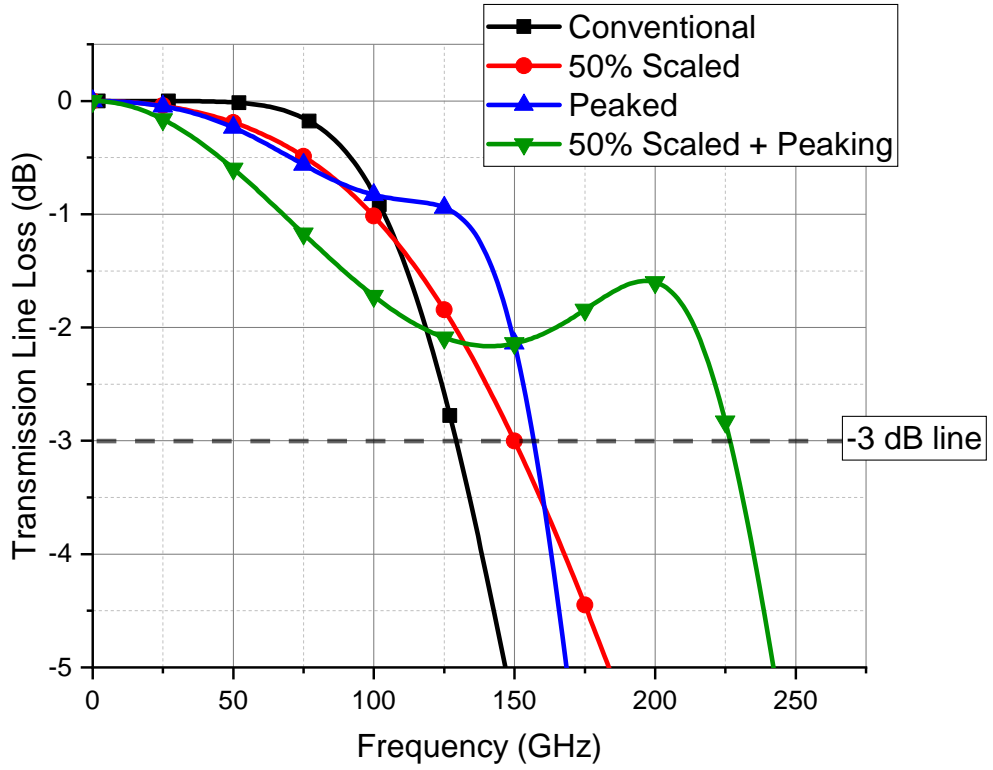


Figure 4.4: Line losses for a conventional transmission line; 50% scaled transmission line; and a 50% scaled transmission line with peaking.

As can be observed in Figure 4.4, scaling the transmission line as described only marginally increases the 3 dB cut-off frequency, however, it alters the frequency response in a manner that makes capacitive peaking more effective. Added merits of transmission line scaling is the consequent reduction in attenuation due to line losses and potential reduction in overall circuit footprint.

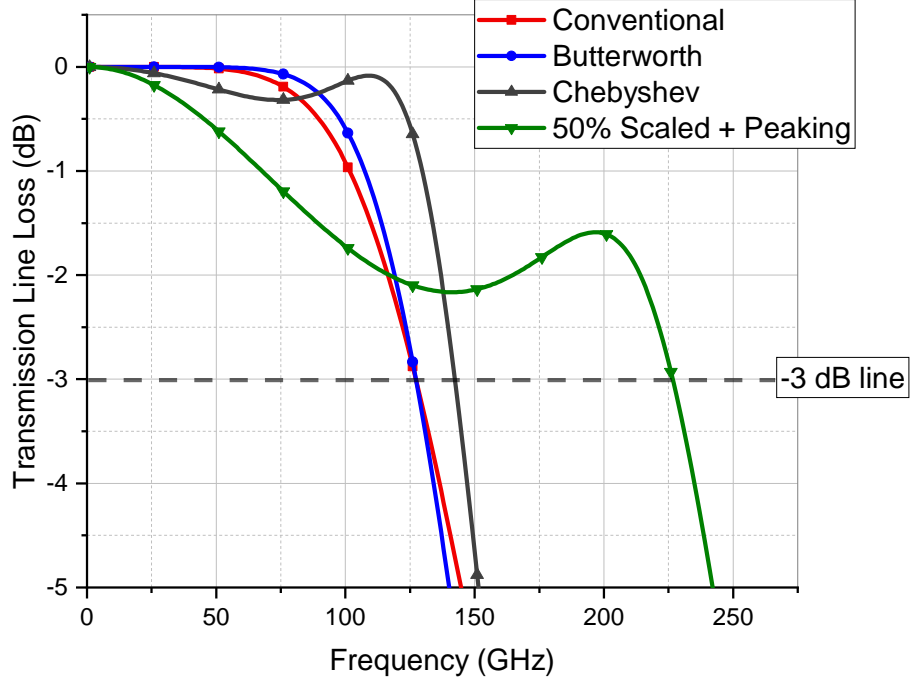


Figure 4.5: Line losses for a conventional; Butterworth; Chebyshev and the proposed transmission line.

Furthermore, from Figure 4.5, it can be observed that the 3 dB bandwidth of the proposed transmission line significantly exceeds that of transmission lines designed based on Butterworth and Chebyshev functions, proposed in [191, 192], for use in the conventional and matrix DA, respectively.

#### 4.2.2 Gain Cell and Output Line Modification

The cascode pair gain cell is considered adequate, as this provides wider bandwidth and better input-output isolation than the CE, such that the bridge capacitance  $C_\mu$  has a negligible effect.

**Step 3: Apply negative resistance attenuation compensation technique to improve the overall gain profile**

The effect of increasing the ratio of  $C_\pi$  to  $L_B$  is that the transmission line would have higher reflection, at high frequencies, leading to a dip in the gain profile.

To counteract this, the HBT version of the attenuation compensation techniques described in [118] and [165] is modified to achieve a flat gain profile.

The key feature of this technique is the introduction of two additional transmission lines,  $L_{cb}$  (at the base of the common base transistor) and  $L_{ce}$  (between the common emitter and common base transistors) to a cascode gain cell, as shown in Figure 4.6(c). For this circuit, the output impedance  $Z_{out}$  is

$$Z_{out} = \frac{(Z_{ce} + j\omega L_{ce})}{(Z_{ce} + j\omega L_{ce}) + (Z_{be} + j\omega L_{cb})} \left( \frac{g_m Z_{ce}}{j\omega C_{be}} + (Z_{be} + j\omega L_{cb}) \right) + Z_{ce} \quad (4.12)$$

where  $Z_{ce}$  is the impedance between the collector and the emitter of the common collector and  $Z_{be}$  is the impedance between the base and the emitter of the common base forming the cascode pair. The value of  $L_{ce}$  is adjusted proportional to  $\zeta$  to increase the negative resistance generated in the circuit and maintain the desired high frequency gain. The resulting inductance value, is denoted by  $L'_{ce}$  in (4.13).  $L_{cb}$  is also modified appropriately to maintain stability (the resulting value is denoted by  $L'_{cb}$  in (4.13)).

The resulting output impedance is given by

$$Z_{out} = \frac{(Z_{ce} + j\omega L'_{ce})}{(Z_{ce} + j\omega L'_{ce}) + (Z_{be} + j\omega L'_{cb})} \left( \frac{g_m Z_{ce}}{j\omega C_{be}} + (Z_{be} + j\omega L'_{cb}) \right) + Z_{ce} \quad (4.13)$$

As in [165], the value of  $L_{ce}$  is adjusted to increase the negative resistance generated in the circuit and achieve the desired high frequency gain.  $L_{cb}$  is also modified appropriately to maintain stability.

To further improve gain flatness, an inductance  $L_{cc}$  is added between the collector terminal of the common base transistor and line  $L_C$ . This creates an m-section type filter [28], for which  $m = C_{ce}/\zeta C_\pi$  for delay synchronisation; and

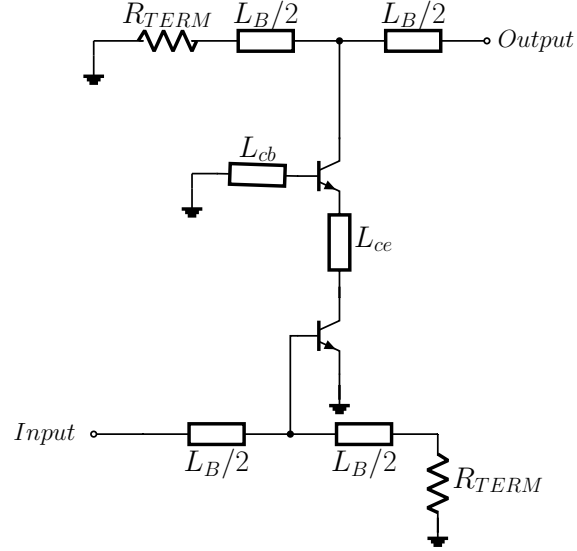
$$L_{cc} = \frac{1 - m^2}{4m} \zeta L_B \quad (4.14)$$

$L_{cc}$  also offers an extra degree of freedom that can be valuable for performance optimisation.

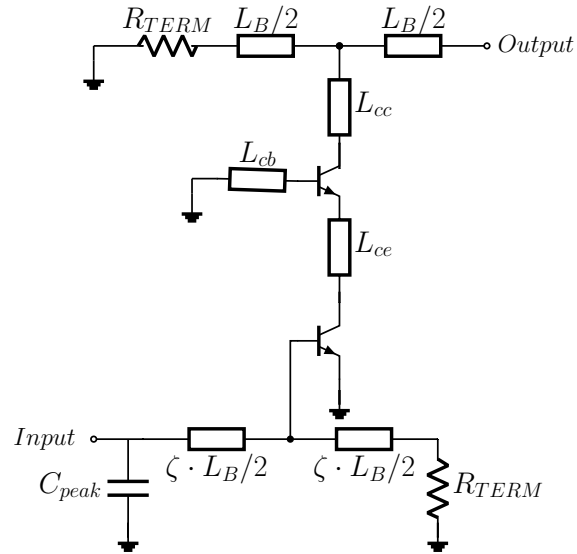
Figure 4.6(a) shows the loss compensation circuit presented in [67], while Figure 4.6(b) shows the new SSDA schematic featuring the scaled input line, the shunt capacitance for input line peaking and the adapted loss compensation for gain flatness. Figure 4.7 is a depiction of the structure of a DA featuring the proposed modifications.

Due to the complexity of the analysis involved, the optimal values for  $L'_{cb}$  and  $L'_{ce}$  may be more easily obtained through computer aided optimisation. For extra degree of tunability, an inductance  $L_{cc}$  is added between the collector terminal of the common base transistor and line  $L_C$ .

It is interesting to note that either of Steps 1 or 2 may be combined with output line attenuation compensation to achieve improved bandwidth performance. However, as is to be expected from Figure (4.4), combining the two steps yields the maximum bandwidth improvement.



(a) SSDA with inductive-peaked cascode



(b) new SSDA with scaled input line, shunt capacitance and adapted attenuation compensation

Figure 4.6: SSDA schematic circuits: inductive peaked cascode vs new bandwidth extension configuration

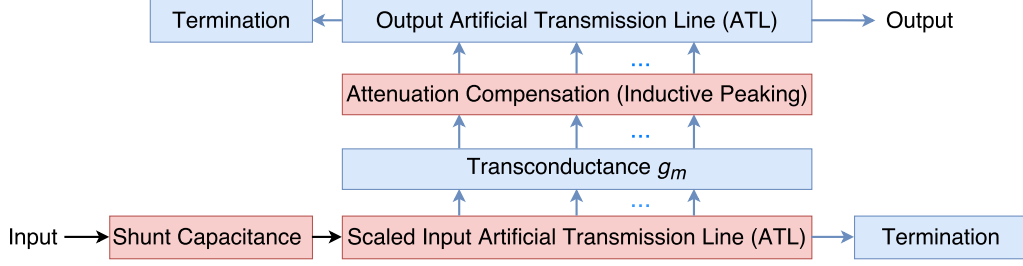


Figure 4.7: Structure of DA featuring transmission line scaling and a peaking (shunt) capacitance on the input ATL, with inductive peaking for attenuation compensation.

## 4.3 Performance Assessment and Verification

### 4.3.1 Simulations based on Ideal Transmission Lines

The aforementioned technique was initially demonstrated in simulation using the active components of the full circuit model of TSC250 [11], however, with ideal - lossless - transmission lines. The advantage of this simulation approach is that it provides the benefit of observing the intrinsic merit of the bandwidth extension technique, without the added complexities introduced by the models of lossy passive circuit components.

Figures 4.11, 4.12 and 4.13 compare the forward gain  $S_{21}$  (dB), the input line reflection  $S_{11}$  (dB) and the output line reflection  $S_{22}$  (dB) respectively, of a conventional SSDA; SSDA with the inductive-peaked cascode technique used in [120] (Figure 4.6(a)); and a SSDA that features the proposed bandwidth extension technique (Figure 4.6(b)). For a meaningful performance comparison, all three circuits are simulated using the same process model and operate at the same bias conditions. Initial simulations were based on lossless transmission lines and ideal circuit elements. Ideal DC-blocks were used to achieve AC coupling for baseband performance. The transmission lines were only minimally optimised (especially  $\zeta$  and  $C_{peak}$ ) at this stage of the simulations, to avoid getting results that would be impossible to replicate when lossy lines and real circuit element are introduced.

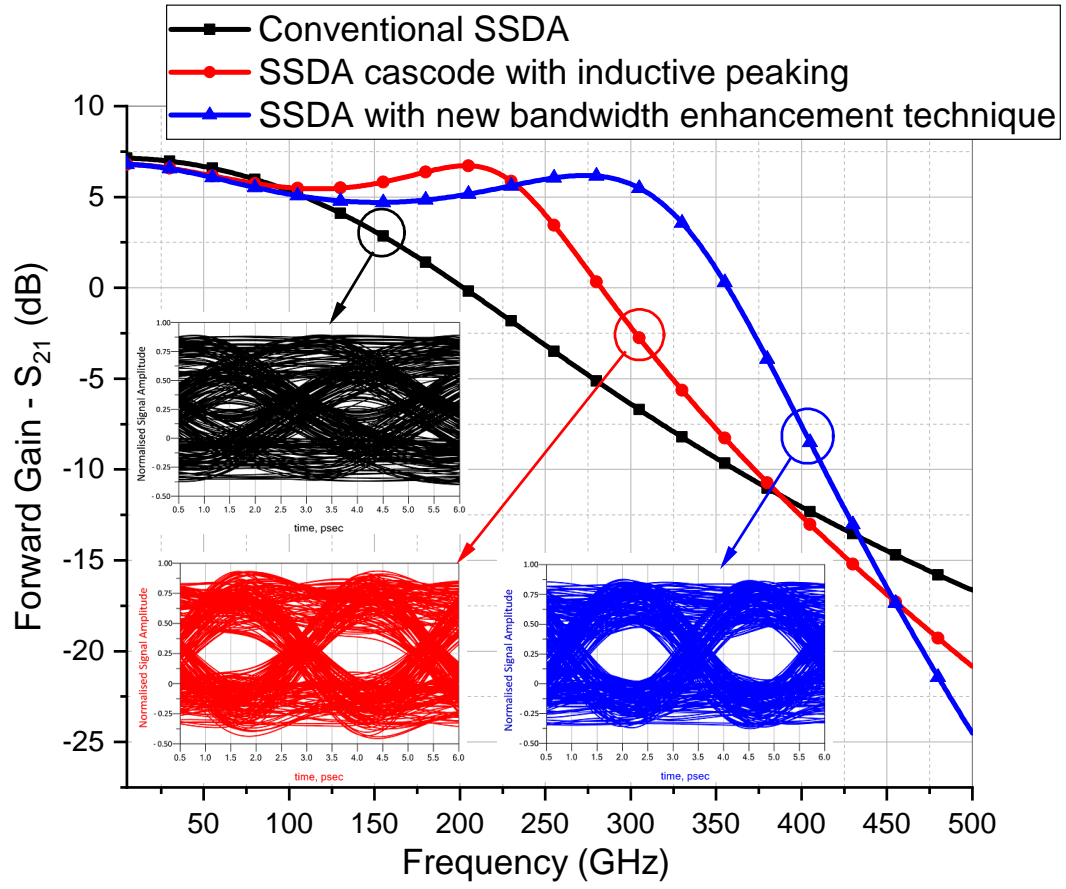


Figure 4.8: Forward Gain  $S_{21}$  (dB) with corresponding simulated eye diagrams at 500 Gbps (inset): conventional - 132 GHz bandwidth with 7 dB gain; SSDA with inductive-peaked cascode - 253 GHz bandwidth with 7 dB gain; and SSDA with new bandwidth enhancement technique - 328 GHz bandwidth with 7 dB gain.



Circuit simulations predict a 328 GHz 3 dB bandwidth for the the new technique. This is nearly two-and-a-half times the bandwidth of an otherwise equivalent SSDA designed using conventional means and 30% higher than what is achieved with the technique adopted in [120] (Figure 4.8). The input line modifications result in a gain ripple of  $\pm 1$  dB. The phase response of the new design was tested and shows linear phase up to the 3 dB gain of the amplifier, leading to good pulse response. This is indicated by an open eye shown in the inset of the figure, simulated assuming 500 Gbps data stream of  $2^{12} - 1$  pseudo random binary sequence. Also, from Figure 4.8, the open eye for the new design furthermore shows its advantage when compared to the fully closed eye diagram of the conventional design and the less open one of the design following [120].

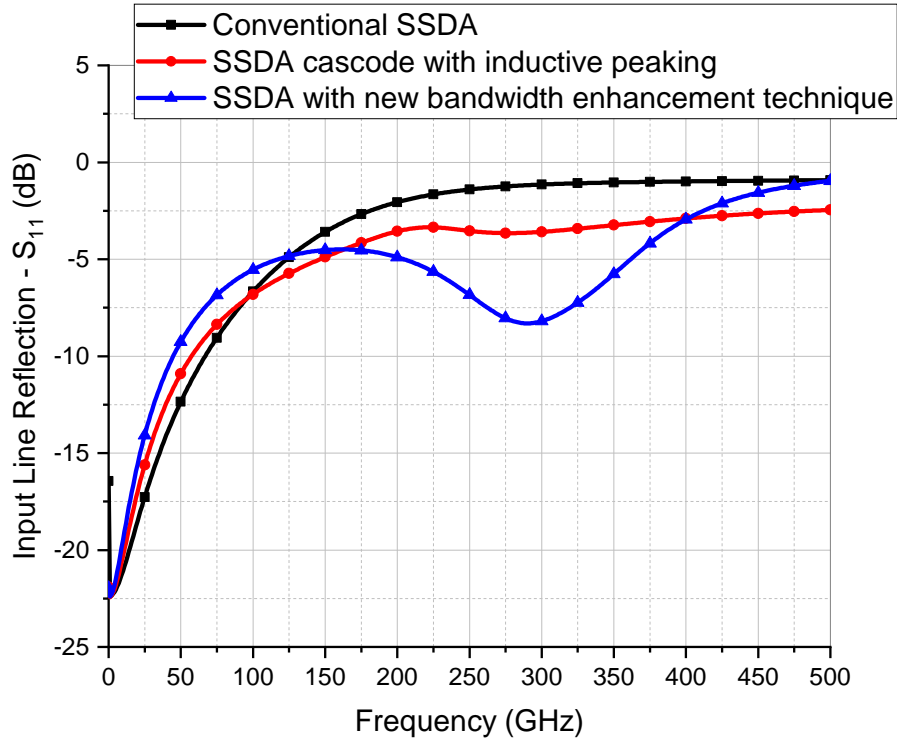


Figure 4.9: Input line reflection  $S_{11}$  (dB) comparison.

Additionally, the design improves the input and output matching behaviour, as shown respectively in Figure 4.9 and Figure 4.10. The design is unconditionally

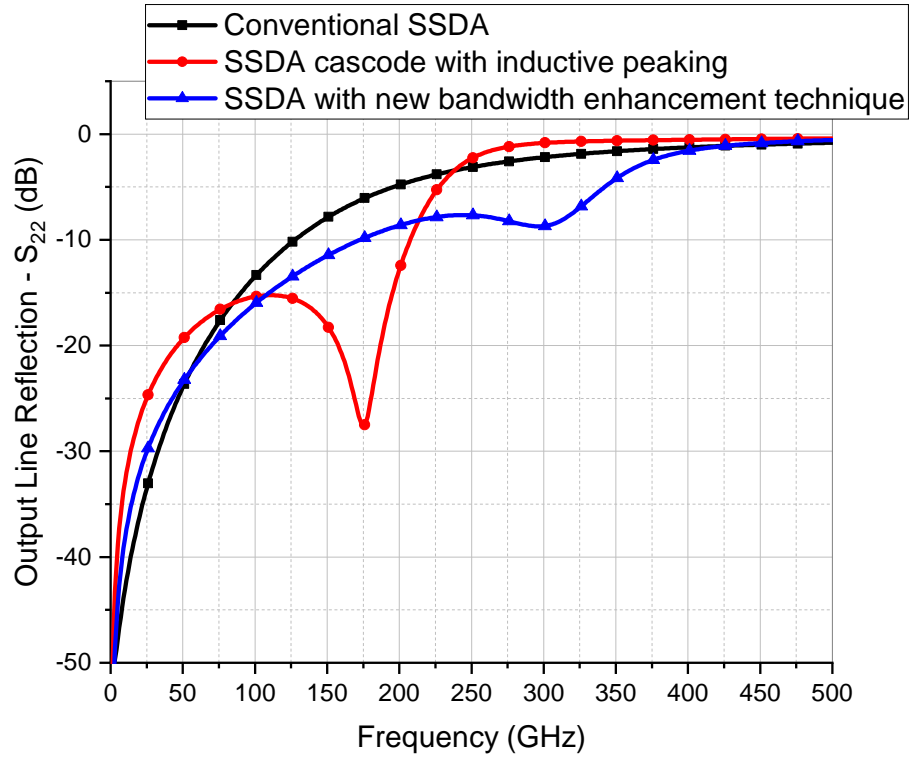


Figure 4.10: Output line reflection  $S_{22}$  (dB) comparison.

stable, as both the Edwards-Sinsky stability parameters ( $\mu_1$  and  $\mu_2$ ) and the Rollett's stability factor ( $K$ ) are greater than 1 from DC up to 500 GHz. Furthermore, the new design displays better phase linearity and smaller delay variation than the conventional design. The group delay is simulated to be approximately  $4 \pm 1$  ps from low frequencies to 500 GHz, which leads to the good pulse response observed in the eye diagram of Figure 4.8.

### 4.3.2 Full Foundry Simulations based on Lossy Transmission Lines

More detailed simulations that featured transmission line models with expected losses were performed. Vias required for inter-layer connections and interconnects between all circuit elements were also closely modelled and included in the simulation setup. Furthermore, ideal 1  $\mu$ F AC-coupling capacitors used in initial simulations were replaced with more realisable capacitance values within the range of 2.5 pF to 3.5 pF (taking up about  $50 \mu\text{m} \times 200 \mu\text{m}$  on chip) realized with MIM capacitors. With lossy lines and real passive elements in place, the transmission lines were more rigorously optimised and it was found that a higher bandwidth could be achieved than in the initial simulations.

Circuit simulations predict a 345 GHz 3 dB bandwidth for the new technique, a 17 GHz improvement over the initial simulation result. This is almost two-and-a-half times the bandwidth of an otherwise equivalent SSDA designed using conventional means and more than 25% higher than what is achieved with the inductive-peaked cascode technique adopted in [17] (Figure 4.11). The input line modifications result in a gain ripple of  $\pm 1$  dB (Figure 4.11). As expected, the lower capacitance value used for bias decoupling resulted in low frequency peaking.

The design remains unconditionally stable, with both the Edwards-Sinsky stability parameters ( $\mu_1$  and  $\mu_2$ ) and the Rollett's stability factor ( $K$ ) greater than 1 from DC up to 500 GHz. As initially observed, the design improves the input

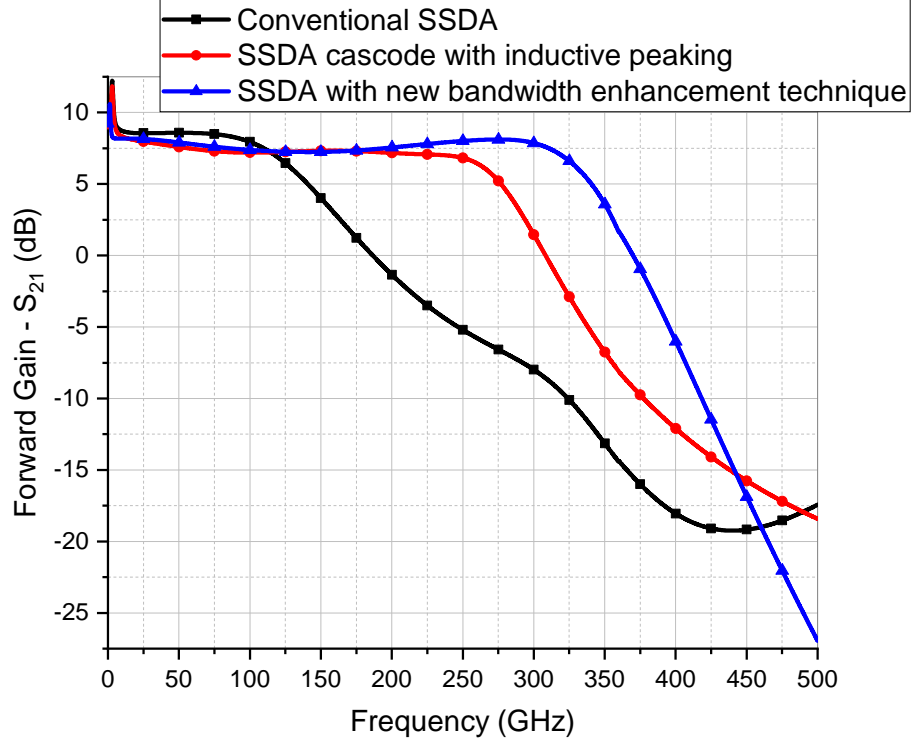


Figure 4.11: Forward gain  $S_{21}$  (dB): conventional - 140GHz bandwidth with 8 dB gain; SSDA with inductive-peaked cascode - 275GHz bandwidth with 8 dB gain; and SSDA with new bandwidth enhancement technique - 345 GHz bandwidth with 8 dB gain.

matching behaviour, as shown in Figure 4.12, though the output match is slightly worse (Figure 4.13).

In addition to the improved performance, the SSDA based on the new technique also occupies 12% less chip area compared to the inductive-peaked cascode SSDA circuit.

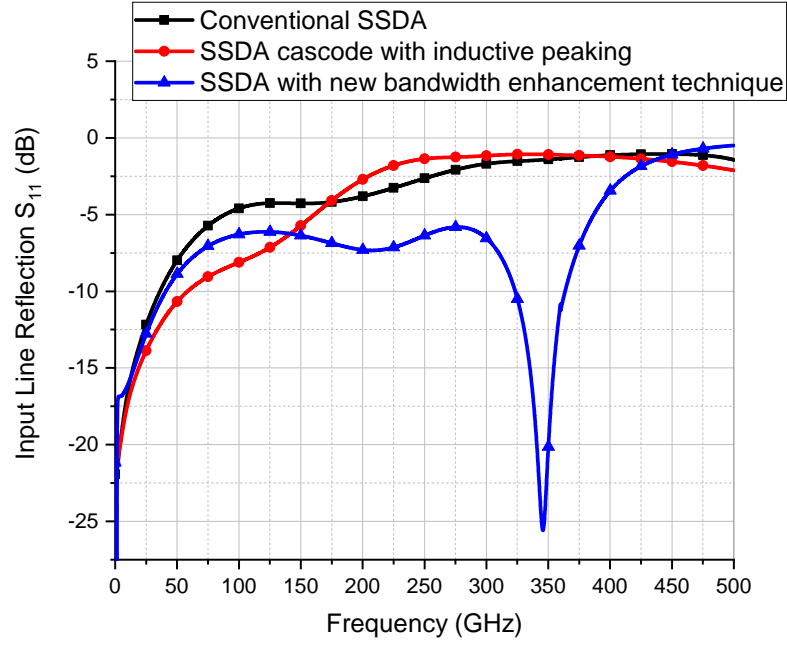


Figure 4.12: Input line reflection  $S_{11}$  (dB) comparison.

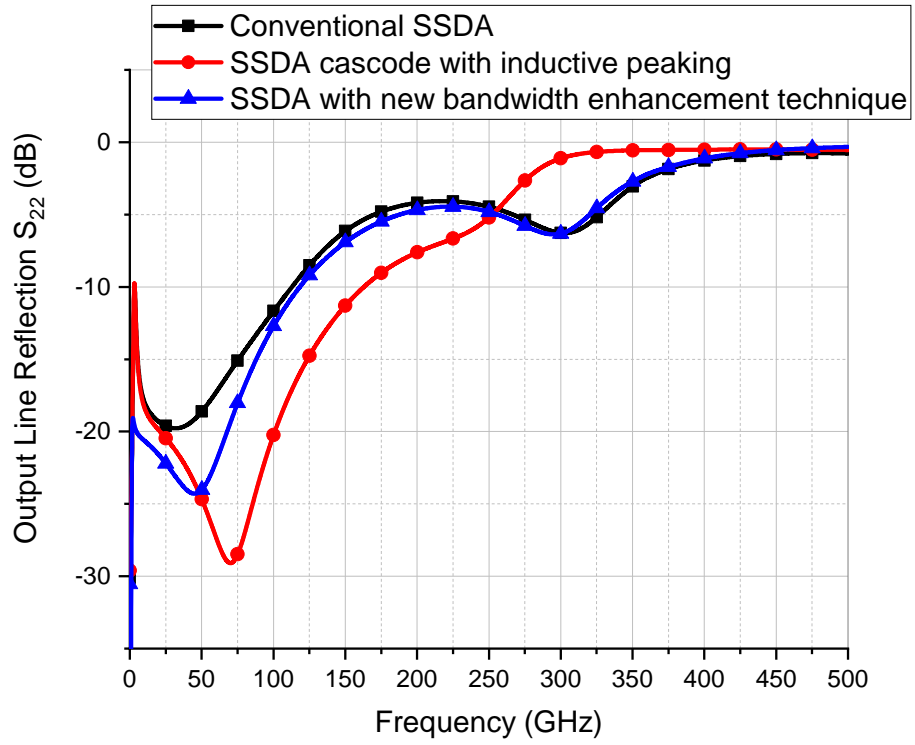


Figure 4.13: Output line reflection  $S_{22}$  (dB) comparison.

## 4.4 MMIC Layout

The laying-out process for the circuit, represented by the schematic in Figure 4.7, involved the following.

- DHBTs with emitter area of  $0.25 \mu\text{m} \times 6 \mu\text{m}$  were used in the cascode gain cell as a compromise between gain, bandwidth and power consumption.
- Artificial transmission lines for the DA were implemented using thin-film microstrip lines on the topmost layer M4.
- The second metal layer M2 was used as the ground plane allowing low inductive connection between emitter and ground, with M1 is used for dc connections. The advantage of this is that the ground plane (M2) serves as a shield, separating the signal layer (M4), which carries RF signal from the layer with DC.
- In order to have a high inductance, the width of the microstrip lines in the input and output ATLs were chosen as narrow as the process tolerances allow, which resulted in a characteristic impedance of  $75 \Omega$ . The simulated loss of the microstrip lines is 1.2 dB/mm.
- The connections from the input transmission line to the common-emitter devices were designed to be as short as possible since any inductance here reduces the gain and the bandwidth. The two devices in each gain cell are connected with a low-impedance low-loss microstrip line.
- To minimise electromagnetic couplings and losses in both MMICs, significant spacing ( $>40 \mu\text{m}$ ) was kept between adjacent transmission lines carrying RF signals and meandered lines were avoided.
- Tapered transitions were included at points where transmission lines of different dimensions connect and at corners.

Figure 4.14 shows the planar MMIC layout of the SSDA featuring the input line compensation techniques described in this chapter. A layout was also designed for the optimised inductive-peaked cascode (Figure 4.15 shows the planar MMIC layout) for performance comparison. However, this chip could not be sent in with the same tapeout batch, due to the limited wafer space available to this project at the time.

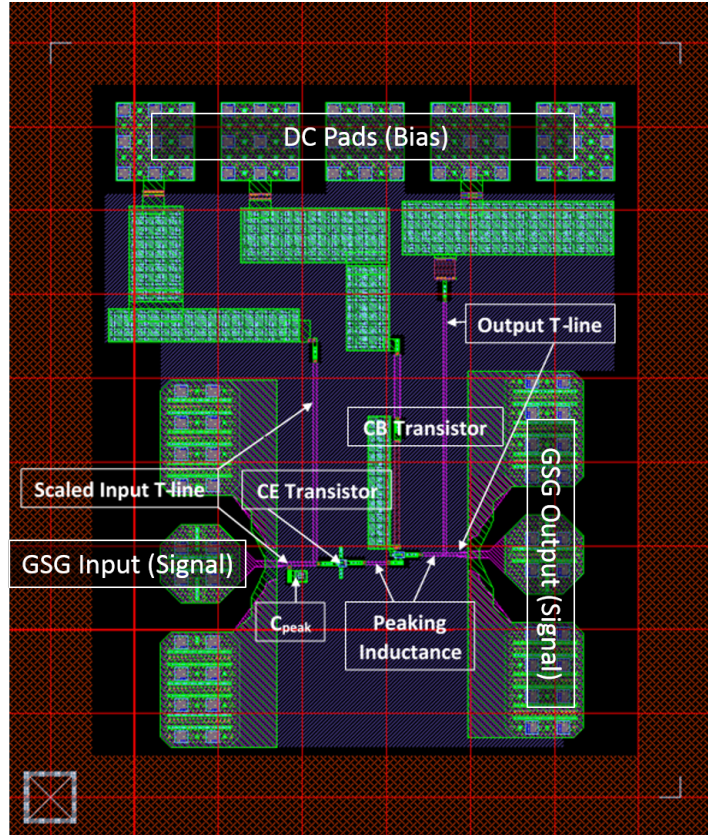


Figure 4.14: Chip planar layout: SSDA with input line scaling and capacitive peaking (chip area:  $615 \mu\text{m} \times 475 \mu\text{m}$ ).



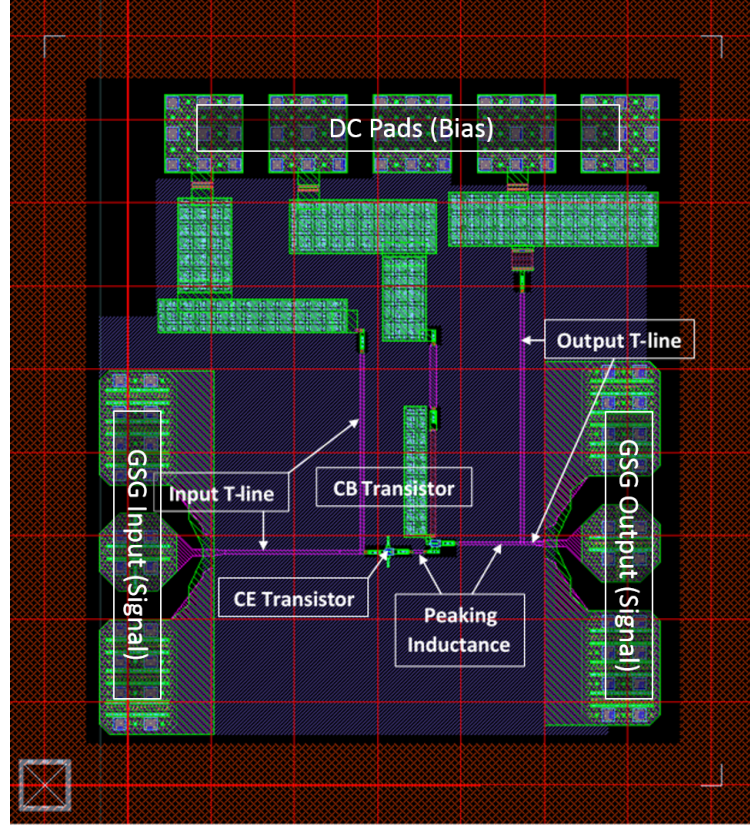


Figure 4.15: Chip layout: SSDA with inductive-peaked cascode (Chip area:  $615 \mu\text{m} \times 540 \mu\text{m}$ ).

## 4.5 SSDA MMIC Measurement

The fabricated MMIC occupies an area of  $460 \mu\text{m} \times 620 \mu\text{m}$  and can be seen in Figure 4.16. The verification of the amplifier performance was done via small-signal on-wafer probing measurements. Due to the wide bandwidth of the amplifier, two different measurement setups were required to characterize it<sup>1</sup>.

The low frequency response of the amplifier was measured from 100 MHz - 120 GHz with the VectorStar ME7838A series broadband vector network analyser (VNA) by Anritsu via  $75 \mu\text{m}$ , 145 GHz Infinity probes. The input power was set to -20 dBm to avoid saturating the amplifier. The high frequency response was measured from 140 GHz - 220 GHz with PNA-X N5247A VNA by Keysight,

<sup>1</sup>Measurements were done at the Department of Microtechnology and Nanoscience (MC2), Chalmers University of Technology Göteborg Sweden on the 1st and the 27th of November 2019.



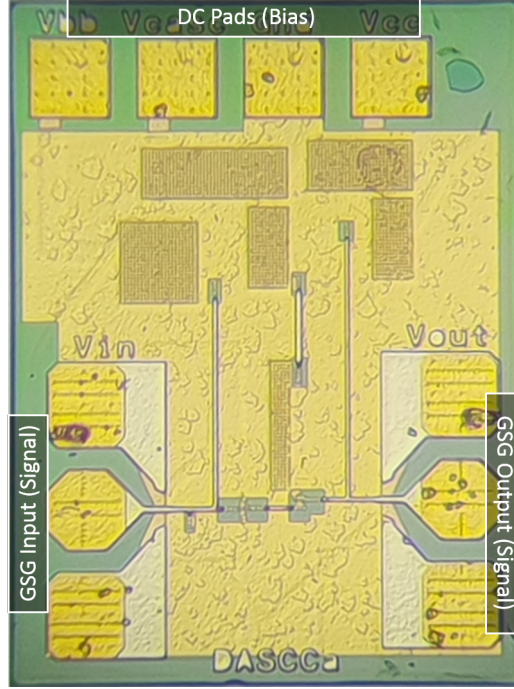


Figure 4.16: Microphotograph of the SSDA. MMIC size:  $620\ \mu\text{m} \times 460\ \mu\text{m}$ .

using VDI WR-5.1 frequency extenders and WR-5.1 waveguide probes. The input power was set and calibrated at -10 dBm to accommodate for the optimal operation of the frequency extenders. The limitations of the measurement equipment did not allow measurement in the 120 GHz - 140 GHz band. In both setups, the measurement reference plane was calibrated to the probe tips, via certified calibration substrates. The MMIC was voltage-biased using Keysight ES6312A triple output programmable DC power supply with 150  $\mu\text{m}$  pitch Picoprobe.

S-parameter measurements from the two measurement setups are presented as solid lines in Figure 4.17. A forward of gain of 7.1 dB and 200 GHz bandwidth was measured. Due to significant departure of the measured response from what was predicted from original simulations -the gain and bandwidth performance were less than predicted by 18.75% and 42%, respectively - new post-measurement simulations were conducted (results shown in dashed lines), with additional parasitics, such as bond pad parasitics, that were not included in the foundry model. Based on the post-simulation results, a good degree of agreement was observed for the

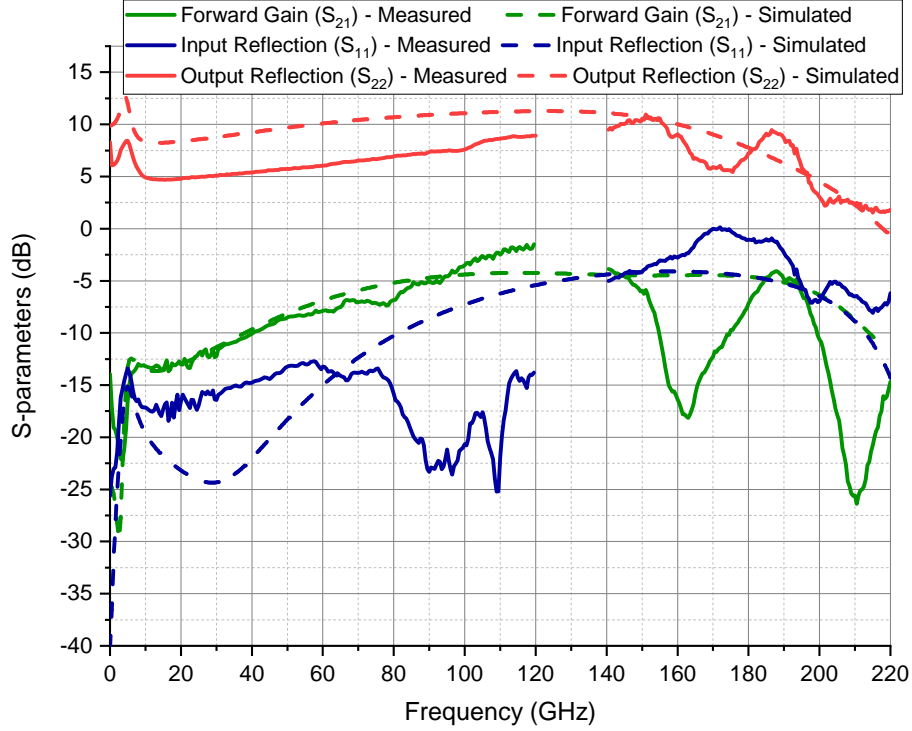


Figure 4.17: Measured vs simulated S-parameters of the amplifier.

input and output reflection ( $S_{11}$  and  $S_{22}$ , respectively) measured using the low frequency measurement setup with the performance measured from the MMIC. Furthermore, on the higher frequencies, the measured results show some unaccounted resonances on both input and output reflection curves around 150 GHz and 200 GHz. The resonances also manifest as ripples in the forward gain curve. Also, the measured bandwidth and gain profile is not as accurately predicted by the post-measurement simulation. There is good agreement between the simulated and the measured forward gain in terms of the bandwidth of 200 GHz. However, with average measured gain at 7.1 dB, there is an average shortfall in gain of 2.5 dB, when compared to the simulated response across the device bandwidth. This performance clearly suggested the presence of extrinsic/parasitic components that are yet unaccounted for even with this round of simulations.

Considering that the loss in gain was across the entire amplification bandwidth of the MMIC (rather than being limited to high frequency region), the loss in gain could be attributed to the presence of additional extrinsic emitter resistance  $R_e$

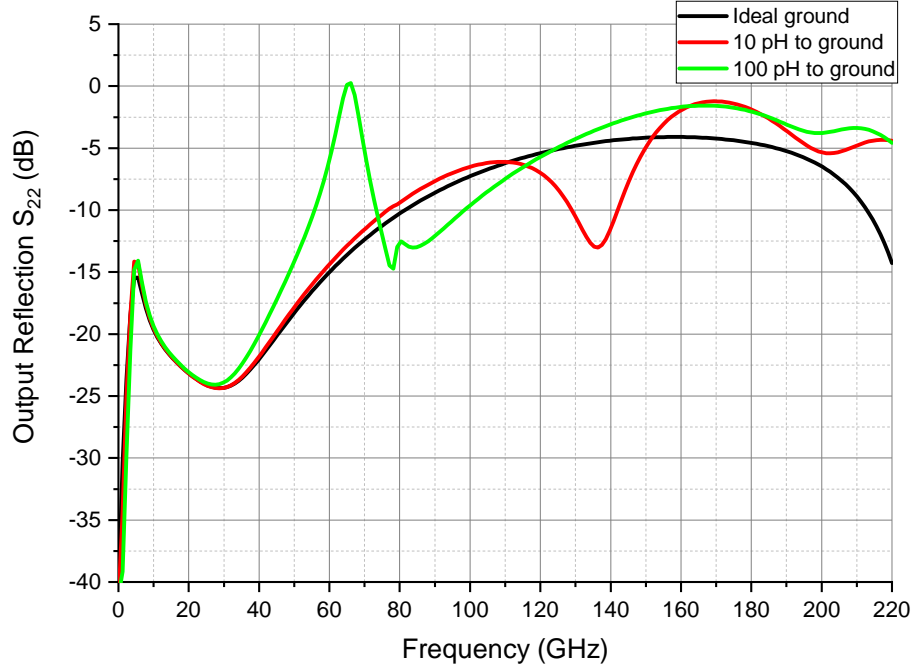


Figure 4.18: Effects of ground inductance on output reflection coefficient.

beyond what is accounted for in the foundry model, with an associated inductance  $L_e$ . Also, there is a possibility that the vias connecting the layers of the MMIC had parasitic impedances that were not fully accounted for in models. Combined, these parameters presented as an emitter degenerating impedance between the emitter and ground in the MMIC, hence reducing gain. This explanation is justified by the commensurate reduction in measured gain of the matrix MMIC, as will be seen in Section 5.5 in the next chapter.

Regarding the resonance observed in the input and output reflection curves, simulations showed that the resonant points were very sensitive to the inductance and capacitance of the DC bias probe used. Figure 4.18, shows a plot of the simulated response of the amplifier without ground inductance, with 10 pH inductance to ground and with 100 pH inductance to ground. Furthermore, a full electromagnetic simulation study of the substrate, including the through-substrate-vias used, indicated that the substrate could sustain resonant modes at frequencies close to 160 GHz and 190 GHz. These resonances would account for the output reflection coefficient approaching 0 dB. In both of these cases, their effects are expected to

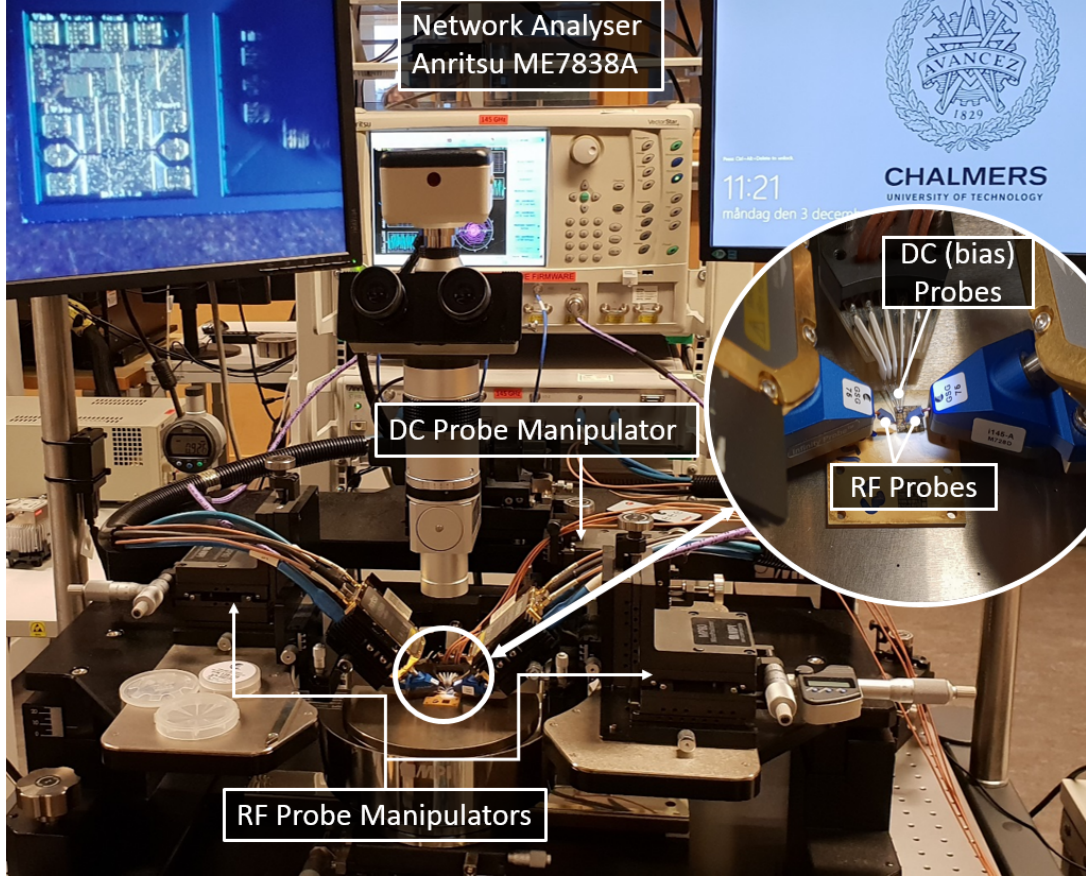


Figure 4.19: Setup for 100 MHz – 120 GHz S-parameter measurement.

be alleviated by packaging the MMIC, which would improve both the decoupling and the grounding of the amplifier.

Since the amplifier consists of a single cascode pair, it was straightforward to tune the gain of the amplifier, based on the base bias  $V_{bb}$  and the cascode bias  $V_{casc}$ , to achieve various gain profiles. The measured results for a variety of bias voltages is presented on Figure 4.21, where a gain tuning range of 5 dB up to 12 dB was demonstrated.

A comparison of the amplifier with state-of-the-art SSDAs and multiplicative DAs in literature is presented in Table 4.1. The amplifier presented in this work has the highest bandwidth among all single-stage designs and is only outperformed by the two-cascaded DA in [17]. The main limitation of the amplifier is the lower



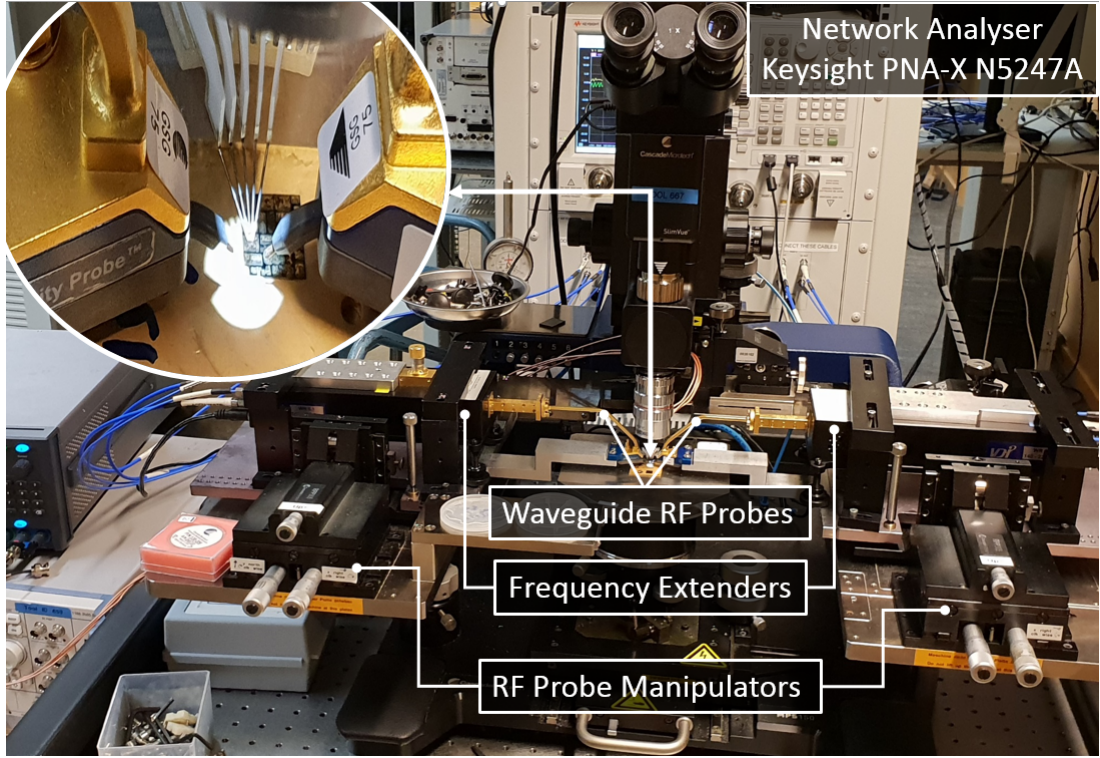


Figure 4.20: Setup for 140 GHz – 220 GHz S-parameter measurement.

Table 4.1: Comparison of the performance of new SSDA with state-of-the-art SSDAs and C-SSDAs.

Technology	Gain (dB)	Bandwidth (GHz)	GBP (GHz)	Pdc (mW)	Area (mm <sup>2</sup> )	DA Topology	Ref
250 nm InP HBT	7.5	192	455	40	0.24	SSDA	[17]
250 nm InP HBT	16	235	1480	117	0.41	2-C-SSDA	[17]
130 nm SiGe BiCMOS	13	170	759	74	0.22	4-C-SSDA	[103]
130 nm SiGe BiCMOS	16	175	1102	360	0.38	2-C-SSDA (Balanced)	[108]
<b>250 nm InP HBT</b>	<b>7.1</b>	<b>200</b>	<b>455</b>	<b>75</b>	<b>0.28</b>	<b>SSDA</b>	<b>This Work</b>

gain at the lower frequencies which is offset by the tunability range at the higher end of the frequency range.

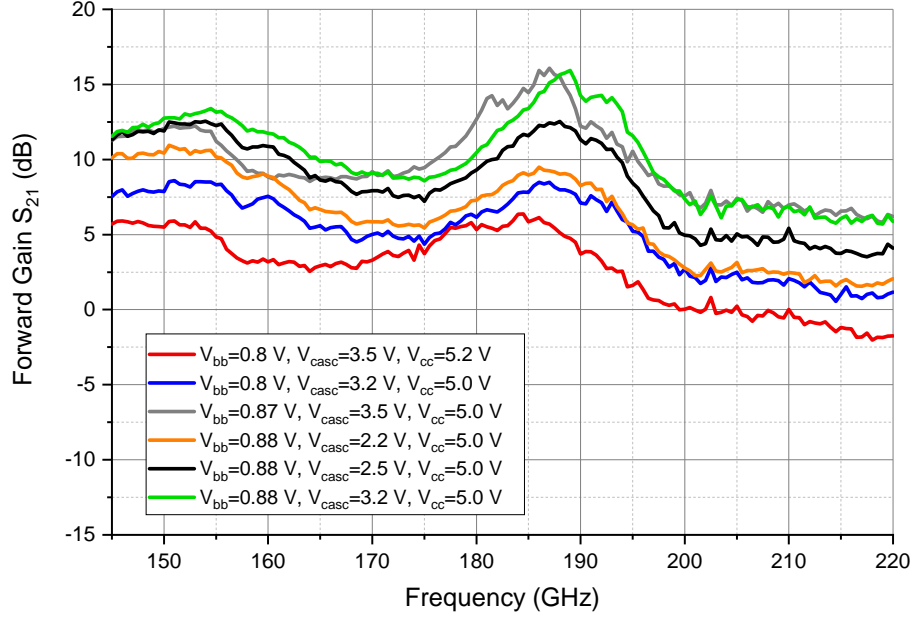


Figure 4.21: High frequency S-parameter response for SSDA under different bias conditions.

## 4.6 Discussion

This study on ATL scaling and capacitive peaking builds on the potential of SSDAs to achieve improved bandwidth performance. Essentially, with this concepts, the advantage of the SSDA in achieving distributed effects with minimal length of inductive lines is extended within the limits of acceptable wideband amplifier performance. Transmission line scaling offers merits in two respects: a wider bandwidth from the increased cut-off frequency of the ATL; and reduced attenuation associated with transmission line losses. Transmission line scaling, as described in this thesis and to the best of the author's knowledge, is entirely novel. Conceptually, the technique would be considered as divergent to classical distributed amplification theory, as its implementation would result in increased reflection from the purposive mismatch between the input ATL and termination. The viability of the approach rests on the uniqueness of the SSDA. The less stringent roll-off properties of the input ATL of the SSDA (essentially a 3rd order lowpass filter)

allows the implementation of the proposed modification, with limited impairment to performance.

The use of capacitive peaking - in some form - to achieve bandwidth enhancement has been reported for transimpedance amplifier design in [193]; as an AC-signal resistance-bypass; and in [194] based on a Butterworth-type implementation. However, its application in DA image-impedance transmission line synthesis and combination with inductive-scaling is the first application of the concept - in the manner described - to the DA. The application of the capacitance is similar in functionality to stub matching as both approaches create a similar effect. Indeed, in arriving at this approach, stubs designed based on half- $m$  sections were initially tested for matching at specific frequencies, similar to what is achieved with the capacitor. However the advantage of using plain capacitance (realized with the MIM capacitor in this case) is the reduced transmission line losses at frequencies other than the resonant frequency. Applied in isolation, it is observed that capacitive peaking on the input line offers limited bandwidth improvement with the gains arising from combining and optimising the scaling, peaking and attenuation compensation - the three aspects that comprise the new technique.

The capacitive peaking technique is not to be confused with capacitive coupling technique (also described as the capacitive division technique), which has been applied to distributed power amplifier design [23, 110, 195–197]. This technique was initially conceived by the separate teams of Kim and Tserng, and Ayasli *et al.* in 1984 to increase broadband output power and efficiency of FET based DAs, by increasing the gate width. The technique could also offer merit in bandwidth improvement as it can be used to reduce the effective input capacitance and synchronise the phase velocity of the signal propagating on the input and output lines. However, while some measure of bandwidth improvement may be achieved with the technique, this improvement is offset by the high-pass effect that arises from placing a capacitor at the input of the active device (as can be observed in the results published in [23, 110, 195–197]). The high-pass effect is even more severe

with very high  $f_T$  processes, which have comparatively low input capacitances and require series capacitance of similar order to implement the technique. Furthermore, the series capacitor forms a voltage divider circuit at the base/gate of the active device and a portion of the input signal is lost to its capacitive reactance. Hence, while the bandwidth may be improved, the gain-bandwidth product will not increase by the same factor - and might indeed drop. In [198], Kobayashi *et al.* reported a capacitively coupled DA with baseband performance, implemented by bypassing the coupling capacitor with a series resistor. However, even at higher bias current, the amplifier reported a lower gain, when compared to a conventional cascode based on the same process, due to voltage drop across the bypass resistor. Also, the bandwidth in this case was also less, which could be attributed to the significantly higher bias at which the capacitively coupled DA was driven. (The conventional cascode design achieved a nominal gain of 16 dB with a 24 GHz bandwidth, while the capacitively coupled cascode design achieved 12.5 dB gain at 20 GHz bandwidth [198]). Implementation-wise, capacitive coupling is achieved with a series capacitor at the base/gate of the active device, while in the proposed approach a shunt capacitor is added to the input line; effectively increasing the filter order by one.

However, it is important to point out that the transmission line scaling technique will find limited functionality in multi-stage DAs, as the limited distributed effect and corresponding increased reflections become more pronounced. This is even more so with HBT-based DAs, due to the complex input nature and associated mismatch losses. Hence, to meet higher gain requirements, SSDAs based on this bandwidth enhancement technique can be suitably applied as units of high-gain wideband amplifiers through cascading or in a single-stage matrix topology, as will be described in the next chapter. Finally, it is noteworthy that while in this study, the scaling and capacitive peaking techniques have been described and applied in the context of HBT based SSDAs; the techniques can be also suitably applied to field-effect based SSDAs as well. Indeed, the possibility of applying



the described techniques to multistage HEMT based DAs is envisaged, due to the better matching properties of field-effect devices.

## 4.7 Conclusions

The peculiarities of the SSDA topology make it possible to drive new generation transistor processes close to their bandwidth limit and would be instrumental in making terahertz bandwidth circuitry much more practical. A new design technique for bipolar based SSDAs is introduced, through which significant improvement in bandwidth can be achieved. It involves purposely scaling down the inductance and introducing a high frequency  $LC$  peak (through a shunt capacitance) on the amplifier's input line; and negative resistance attenuation compensation on the output line. This technique can be used to achieve DAs with significantly wider bandwidth and with improved time-domain response and input and output matching behaviour. By cascading or forming a matrix of such SSDAs, very high gains can also be achieved.

The utility of the described technique has been demonstrated in simulation tests, based on full foundry process models with expected losses factored in. Results from these tests predicted a gain of 8 dB and 345 GHz bandwidth. However, the fabricated SSDA MMIC had a gain of 5 dB and 194 GHz bandwidth, consuming 75 mW of power. While this is a remarkable performance and sets a record bandwidth for the SSDA, parasitic effects from the multilayer interconnect back-end process resulted in a loss of bandwidth of nearly 44%, when compared to full simulation. To take full advantage of the bandwidth optimisation technique, future designs will need to incorporate such parasitic resonant modes in pre-fabrication simulation studies. Furthermore, it is expected that packaging the MMIC bare die in modules would improve both the decoupling and the grounding of the amplifier.

# Chapter 5

## Matrix SSDA: Design and Analysis

### 5.1 Introduction

The concept of the matrix DA was introduced by Niclas and Pereira in 1987 [124]. Similar to the cascaded DA, it combines the processes of additive and multiplicative amplification in the same module; a step above the conventional DA, which only employs additive gain. Hence, the size of the module can be significantly reduced when compared to other amplifier topologies of similar gain-bandwidth performance.

While the matrix DA is functionally similar to the cascaded DA, in that they both combine multiplicative and additive gain properties, there is a structural distinction. The cascaded DA consists of a number of unique DAs with the output of one connected to the input of the other; while the matrix amplifier is conventionally a multi-tier single structure, due to the presence of intermediate lines connecting the output of one tier to the input of the next tier. In the design of cascaded DAs, it is essential that the individual amplifiers be designed to give a gain response as flat as possible up to the desired maximum frequency [42]. However with matrix amplifiers, the fact that the output transmission line of a lower stage would form the input line of the stage above it means that the stages cannot be individually optimised and then combined. These intermediate transmission lines must be designed to distribute the resultant capacitance of both stages that it connects.

The advantages of the matrix amplifier over the cascaded DA include: a potential for higher gain, because both the forward and reverse waves on the inter-

mediate transmission lines are amplified by the gain stage in the tier above them, whereas the reverse wave is absorbed by the drain line termination in the cascaded DA [30, 36]; an inherent reverse isolation over wide bandwidths at reduced size [30]; better input and output matching with lower noise figure [199, 200]; reduced MMIC circuit footprint and, consequently, lower production cost [200]; and significantly less phase delay and group delay variation - an important feature for applications requiring good phase tracking [200]. The matrix topology has also been used to combine both HEMT and HBT devices on different tiers, allowing for the combination of the electrical characteristics of both devices to optimise amplifier performance [154, 201].

In this chapter, the M-SSDA is introduced. A major merit of the proposed circuit is that it employs multiplicative gain only, such that with an appreciable single-stage gain, a higher overall gain will be achieved than from a multi-staged matrix DA with equal number of gain cells. While possessing a gain mechanism, similar to the C-SSDA [17, 179], the M-SSDA inherits the advantages that the matrix amplifier has over the cascaded DA. These merits are: a smaller circuit footprint and more compactness due to the sharing of intermediate transmission lines (a major advantage in monolithic circuits); potentially lower transmission line losses; and better noise performance [124] (see Figure 5.1 for the DA *family tree*).

As with the bandwidth extension technique described in the previous chapter, the M-SSDA is demonstrated using the TSC250 DHBT foundry model [11]. Employing the HBT in a matrix amplifier offers a unique advantage, which extends to the M-SSDA. The high input-output capacitance ratio of HBTs allow the synthesis of intermediate transmission lines with frequency response that is close to that of the input line. Hence, the bandwidth of the amplifier is not significantly adversely affected by the combined capacitance and resulting lower cut-off frequency on the intermediate line [52]. Other merits, as discussed in Chapter 3.3.1, arise from the suitability of HBTs for SSDA and SSDA-based designs. These include

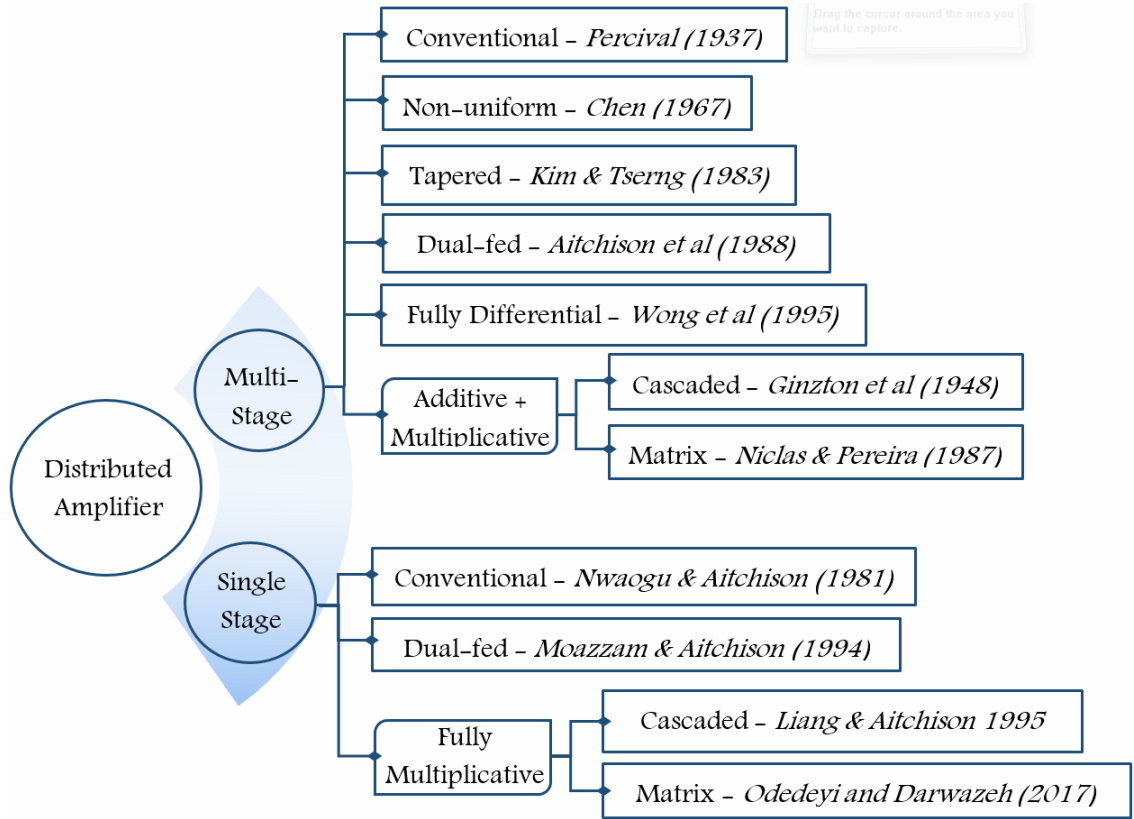


Figure 5.1: The DA family tree: Major DA configurations with the originating publication.

the higher gains and better linearity properties of the HBT [4]. The input line of the SSDAs that make up the tiers of the matrix is designed using the line scaling and capacitive peaking technique, to achieve wider bandwidth, with attenuation compensation applied on the output line to achieve overall gain flatness.

## 5.2 Design Concept

The M-SSDA is essentially two or more SSDAs connected by intermediate transmission lines, forming a  $M \times 1$  matrix structure (Figure 5.2). For a  $M \times N$  matrix amplifier, (i.e.  $M$  stacks of  $N$ -staged DAs), the overall voltage gain - assuming lossless transmission lines - is given by:

$$G_{matrix} = (Ng_m R)^M \quad (5.1)$$

with

$$R = \frac{\sqrt{Z_{Oinput} Z_{Ooutput}}}{2} \quad (5.2)$$

where  $N$  is the number of cells (columns) on each layer (row) of the amplifier and  $M$  is the number of layers.

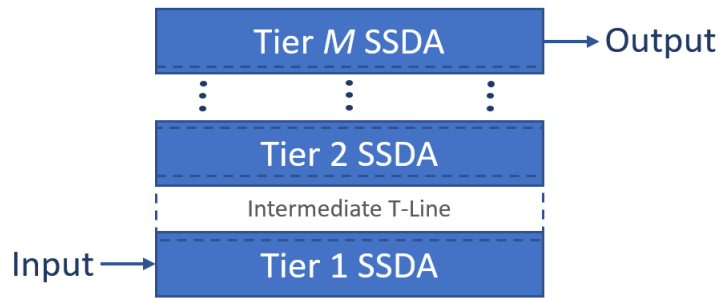


Figure 5.2: Structure of the M-SSDA.

Figure 5.3 shows the schematic and equivalent circuits of the input, intermediate and output transmission lines of a basic common-emitter (CE) M-SSDA with two tiers. The lines are made up of intrinsic capacitance  $C_\pi$  and  $C_{ce}$  and inductive lines  $L_B$ ,  $L_{CB}$  and  $L_C$ ; with the lines coupled by the transistor transconductance

$g_m$ ,  $r_\pi$  and  $r_o$  are the transistor base-emitter junction resistance and output resistance, respectively, and  $R_o$  are the terminating resistances.

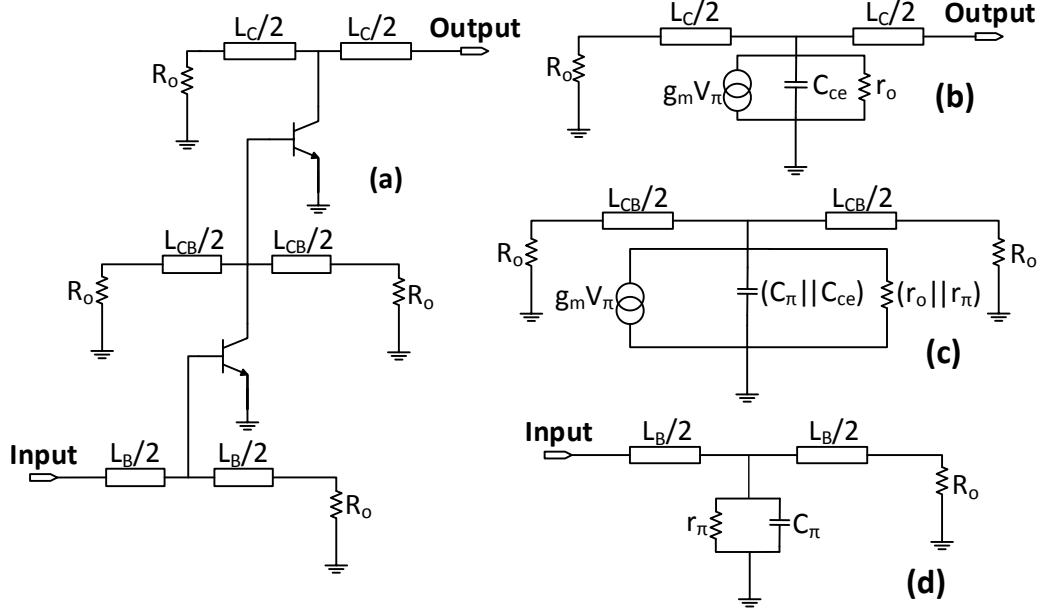


Figure 5.3:  $2 \times 1$  CE HBT M-SSDA (a); with simplified equivalent circuits of: the output transmission line (b), the intermediate transmission line (c), and the input transmission line (d).

The voltage gain of a M-SSDA with equal line impedances is given, to a good approximation, by

$$Gain = \left( \frac{g_m Z_o}{2} \right)^M \quad (5.3)$$

where  $Z_o$  is the image impedance of the transmission lines.

Equations (5.4), (5.5) and (5.6) describe the line impedances of the input ( $Z_{in}$ ), intermediate ( $Z_{int}$ ) and output ( $Z_{out}$ ) transmission lines, respectively, of the simplified CE M-SSDA:

$$Z_{in} = \frac{j\omega L_B}{2} + \frac{r_\pi (j\omega \frac{L_B}{2} + R_o)}{r_\pi + (R_o + j\omega \frac{L_B}{2}) (1 + j\omega r_\pi C_\pi)} \quad (5.4)$$

$$Z_{int} = \frac{j\omega L_{CB}}{2} + \frac{(r_\pi \parallel r_o) (j\omega \frac{L_{CB}}{2} + R_o)}{(r_\pi \parallel r_o) + (R_o + j\omega \frac{L_{CB}}{2}) (1 + j\omega (C_\pi + C_{ce}) (r_\pi \parallel r_o))} \quad (5.5)$$

$$Z_{out} = \frac{j\omega L_C}{2} + \frac{r_o \left( j\omega \frac{L_C}{2} + R_o \right)}{r_o + \left( R_o + j\omega \frac{L_C}{2} \right) (1 + j\omega r_o C_{ce})} \quad (5.6)$$

with  $L_B = Z_o^2 C_\pi$ ;  $L_{CB} = Z_o^2 (C_\pi + C_{ce})$  and  $L_C = Z_o^2 C_{ce}$  [15, 28].

As is to be expected, the bandwidth of the M-SSDA is dominated by the cut-off frequency of the intermediate transmission line ( $f_{c(int)}$ ),

$$f_{c(int)} = \frac{1}{\pi \sqrt{L_{CB} (C_\pi + C_{ce})}} \quad (5.7)$$

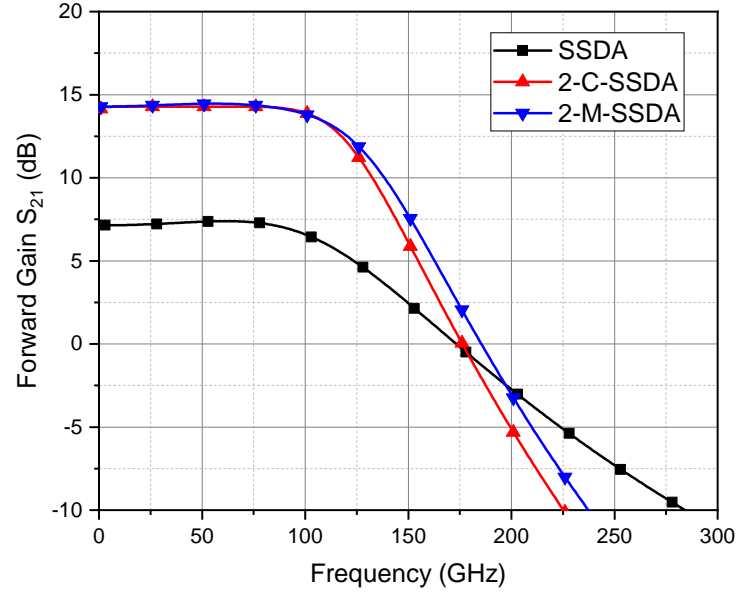
However, as under usual bias conditions,  $C_\pi$  is significantly larger than  $C_{ce}$ ; the cut-off frequencies of both the input line and intermediate transmission lines are close [28].

### 5.3 Performance Prediction and Comparison

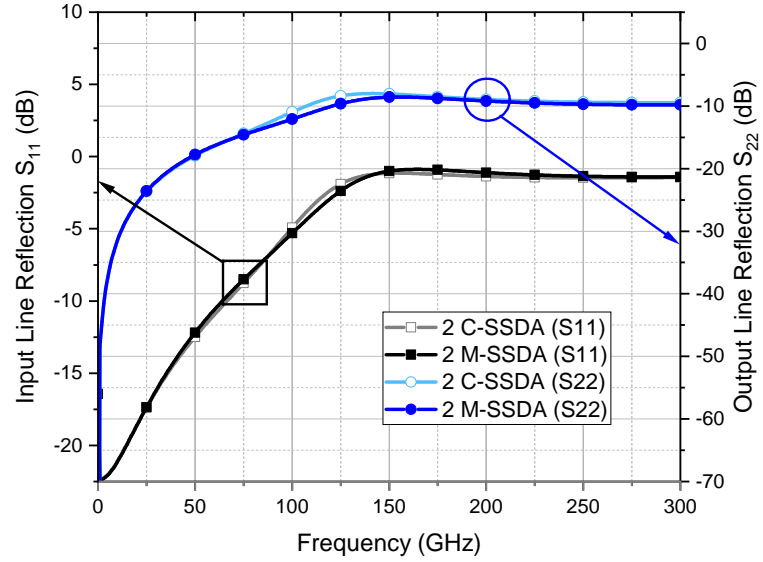
The proposed amplifier topology was initially demonstrated in a simulation study with a two-tier M-SSDA (2-M-SSDA), which featured the conventional common emitter gain cell. To show the similarity in performance of the matrix and cascaded MSSDA, Figure 5.4 compares the S-parameters of the 2-M-SSDA with a 2 cascaded SSDA (2-C-SSDA), also based on a common emitter gain cell. A plot of the SSDA forward gain is included as a reference of single-stage gain. For a meaningful performance comparison, the circuits are simulated using the same process model and the identical HBT devices are operated at the same bias conditions. All passive circuit elements of each of the identical stages are individually optimized to give the best two-stage amplifier performance. Lossless transmission lines and ideal circuit elements were used in simulations.

Figure 5.4 shows close similarity between the S-parameter performance of the 2-C-SSDA and the two-tier M-SSDA, making it a viable substitute for achieving high gain distributed amplifiers, yet with the advantage of saving circuit size.





(a) Forward gain



(b) Input and output line reflection

Figure 5.4: S-parameter comparison of a  $2 \times 1$  M-SSDA with a 2-C-SSDA

## 5.4 Bandwidth Optimized M-SSDA

From the foregoing discussion, it is clear that extending the  $f_c$  of both the intermediate and input transmission line is crucial to improving M-SSDA bandwidth performance. The technique described in Chapter 4 is applied to both lines: scaling down the input and intermediate line inductance ( $L_B$  and  $L_{CB}$ ); and creating a high frequency peak through the introduction of suitable shunt capacitance.

The intermediate line is scaled by a factor  $\zeta$  (with  $\zeta < 1$ ). The effect of the input line scaling is such that the resulting cut-off frequency  $f_c$  becomes

$$\frac{1}{\pi\sqrt{L_{CB}(C_\pi + C_{ce})}} < f_c < \frac{1}{\pi\sqrt{\zeta L_B(C_\pi + C_{ce})}} \quad (5.8)$$

(For  $f_c = 1/\pi\sqrt{\zeta L_B(C_\pi + C_{ce})}$ , the terminating impedance must be reduced from the conventional  $50 \Omega$  to a value,  $R_o = \sqrt{\zeta L_B/(C_\pi + C_{ce})}$ ; however, this would lead to a corresponding reduction in gain (5.3).

From 5.5, the impedance  $Z_{int}^*$  of the scaled intermediate line is

$$Z_{int}^* = \frac{j\omega\zeta L_{CB}}{2} + \frac{(r_\pi \parallel r_o) (j\omega\frac{\zeta L_{CB}}{2} + R_o)}{(r_\pi \parallel r_o) + (R_o + j\omega\frac{\zeta L_{CB}}{2}) (1 + j\omega (C_\pi + C_{ce}) (r_\pi \parallel r_o))} \quad (5.9)$$

As outlined in the previous chapter, to further increase the bandwidth of the intermediate line, a shunt capacitor  $C_{peak}$  is added, resulting in a high frequency resonant peak ( $f_{peak}$ ), given to a good estimation by

$$f_{peak} = \frac{1}{2\pi\sqrt{\zeta L_{CB} C_{peak}}} \quad (5.10)$$

The impedance  $Z_{in}^{**}$  of the resulting transmission line is given by

$$Z_{in}^{**} = \frac{Z_{in}^*}{1 + j\omega C_{peak} Z_{in}^*} \quad (5.11)$$

The addition of a shunt capacitance effectively increases the order of the input line filter leading to a sharper roll off. Due to the fact that the cut-off frequencies of

the input and intermediate lines ( $f_{c(in)}$  and  $f_{c(int)}$ ) are close, to achieve significant improvement in the amplifier bandwidth performance, it is essential that  $f_{c(in)}$  also be increased. Scaling the input line inductance line by a different factor  $\zeta_2$ , where

$$\zeta_2 = \zeta \left( \frac{C_\pi + C_{ce}}{C_\pi} \right) \quad (5.12)$$

would make the scaled values of  $L_{CB}$  and  $L_B$  equal, and slightly increase  $f_{c(in)}$ .  $C_{peak2}$  - the peaking capacitor on the input line may be chosen as

$$C_{peak2} = C_{peak} \left( \frac{C_\pi}{C_\pi + C_{ce}} \right) \quad (5.13)$$

to obtain a frequency response similar to the intermediate line response. To reduce reflection on the input line an emitter-follower (EF) buffer may be added.

Here, as in Chapter 4, the modified cascode gain cell is applied. Also, the value of  $L_{ce}$  is adjusted to increase the negative resistance generated in the circuit and achieve the desired high frequency gain.  $L_{cb}$  is also modified appropriately to maintain stability.

The cascode gain cell featuring the described gain cell modification is shown as inset in Figures 5.5 and 5.10.

#### 5.4.1 $2 \times 1$ M-SSDA

The proposed modifications have been applied in the design of a two-tier M-SSDA. An alternative design features an emitter follower at the input to reduce reflection on the input line arising from the applied modifications (Fig 5.5).

Figures 5.6, 5.7a and 5.7b, compare the S-parameter performance of the bandwidth optimised M-SSDA with EF input buffer and a three-tier CE M-SSDA using lossless transmission lines and ideal passive network elements. S-parameter results of the bandwidth optimised M-SSDA without an EF buffer is also included to show its effect, particularly on the input reflection  $S_{11}$  (dB) (Figure 5.7a). All three cir-

circuits were simulated using the same process model and operate at the same bias conditions.

Circuit simulations predict 13.5 dB gain and 318 GHz 3 dB bandwidth for 2-M-SSDAs, which feature the bandwidth enhancement modifications (Figures 5.6). This is more than three times the bandwidth of a conventional 2-M-SSDA - based on a common-emitter gain cell (Figure 5.6). It can also be observed in Figure 5.7a, that with the addition of a common collector input buffer, there is significant reduction in the input reflection ( $S_{11}$ ) of the modelled amplifier from a peak value of  $-3$  dB to a more desirable  $-9$  dB.

Based on these results, a more complete modelling that included foundry model passive elements and transmission line losses was performed. This study also included losses due to vias and transitions across the multilayer MMIC process. S-parameter results from this study are presented in Figure 5.8. A comparison is made between the initial study based on ideal circuit elements (represented in Figure 5.8 with dashed lines) and the full foundry based study (represented with solid lines).

A gain of 13.5 dB at 300 GHz bandwidth is predicted based on this study. Figure 5.9 shows the planar MMIC layout of the amplifier.

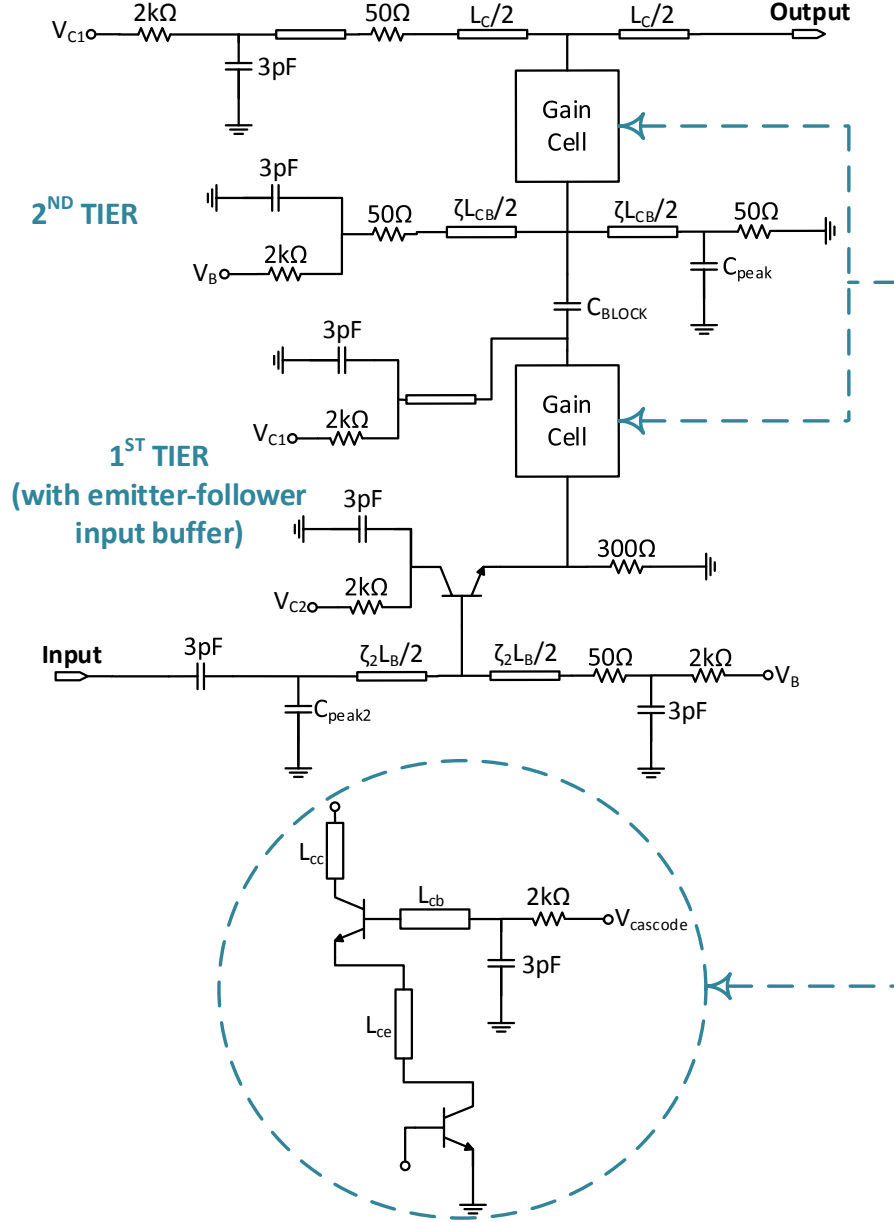


Figure 5.5: Two-tier M-SSDA schematic with scaled input and intermediate transmission lines. Inset shows the modified gain cell.

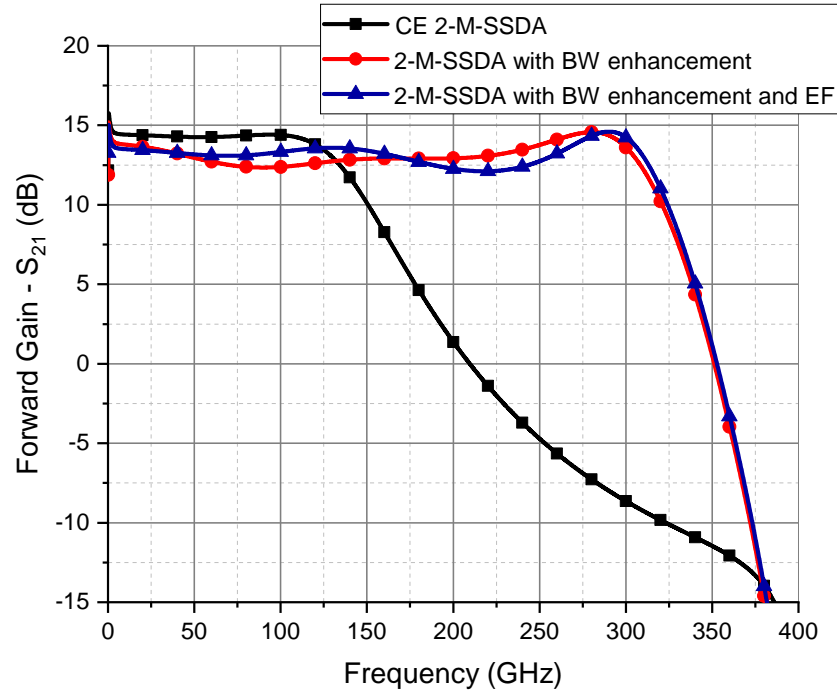
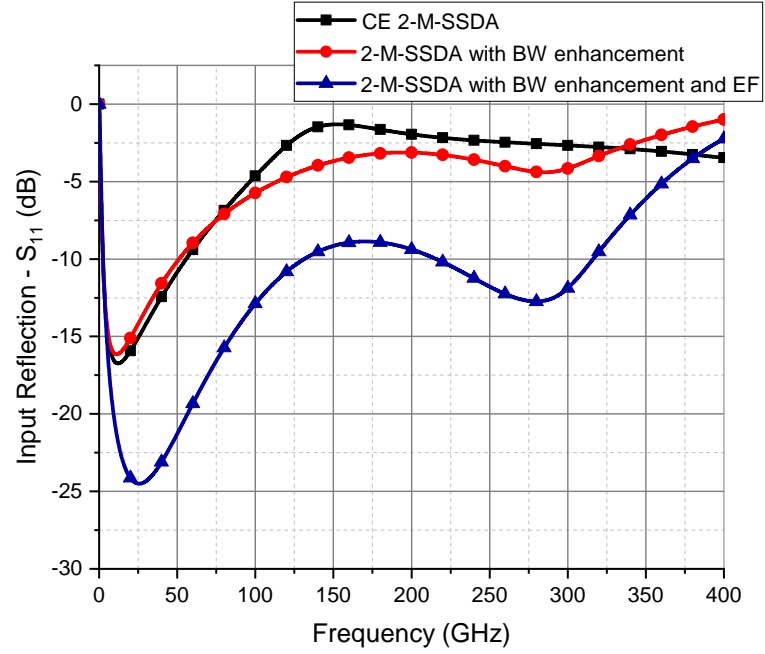
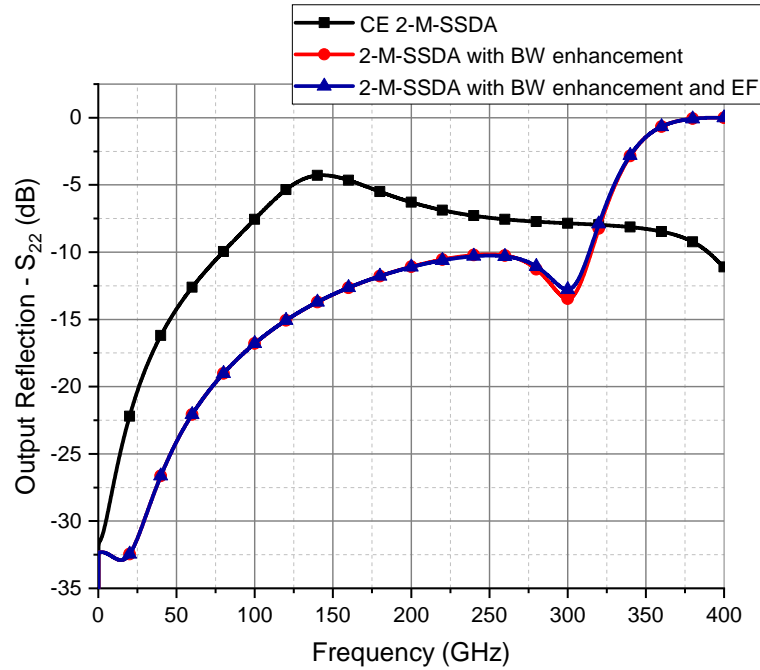


Figure 5.6: S-parameter comparison of a two-tier CE M-SSDA, a two-tier M-SSDA with bandwidth extension; and a two-tier M-SSDA with bandwidth extension and EF input buffer: forward gain  $S_{21}$  (dB) comparison.



(a)  $S_{11}$ (dB)



(b)  $S_{22}$ (dB)

Figure 5.7: S-parameter comparison of a two-tier CE M-SSDA, a two-tier M-SSDA with bandwidth extension; and a two-tier M-SSDA with bandwidth extension and EF input buffer: input line  $S_{11}$  (dB) and output line reflection  $S_{22}$  (dB) comparison.

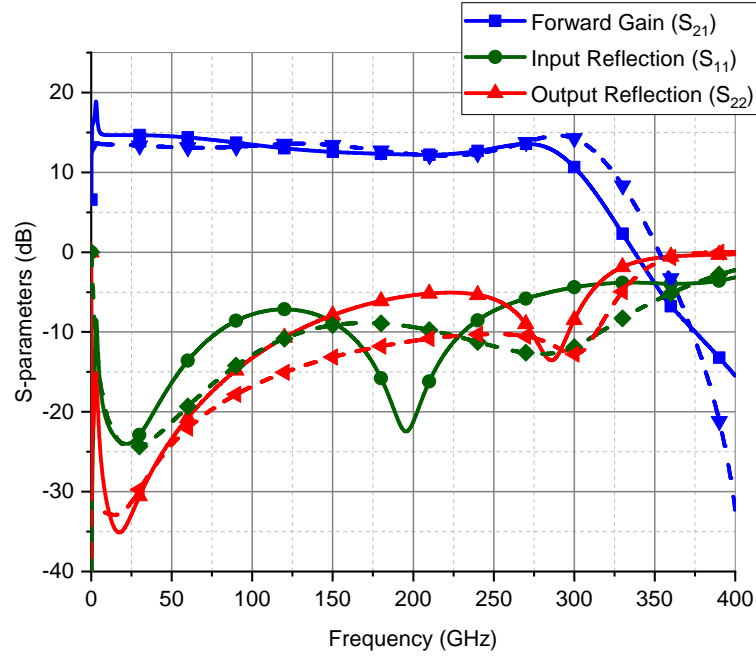


Figure 5.8: Two-tier M-SSDA with bandwidth extension: lossless transmission lines and ideal passive element (dashed lines); lossy transmission lines, passive elements with vias and transitions (solid lines).



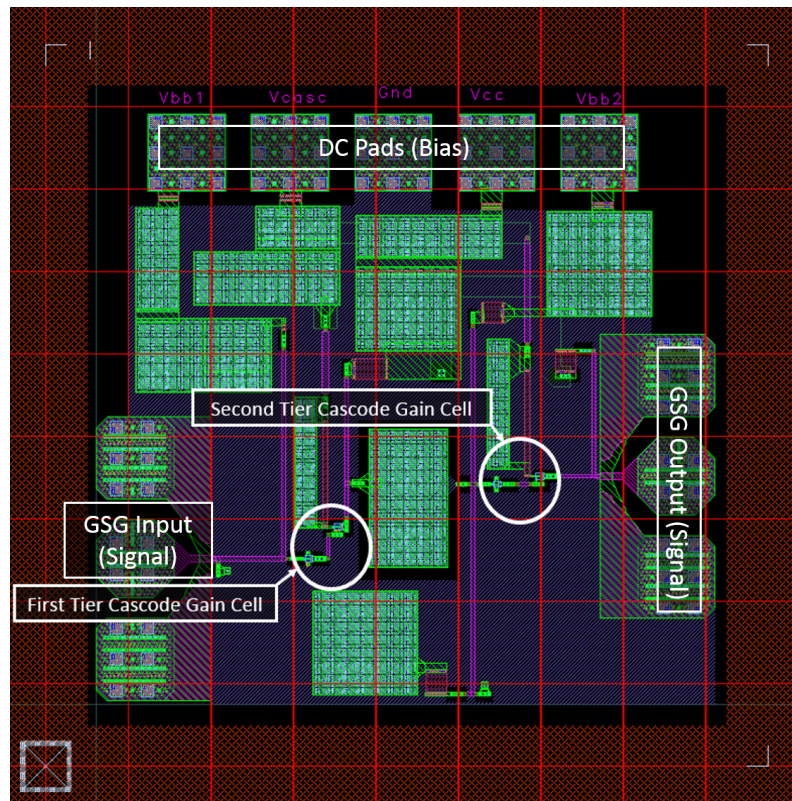


Figure 5.9: MMIC planar layout: two-tier M-SSDA with bandwidth extension (footprint:  $565 \mu\text{m} \times 600 \mu\text{m}$ ).

### 5.4.2 $3 \times 1$ M-SSDA

As an effort towards achieving significant improvement over the state of the art in GBP performance, a three-tier M-SSDA has been designed and laid out as a MMIC. This amplifier is also based on the bandwidth optimisation technique proposed in Chapter 4 and features an EF input buffer. A schematic of the 3-M-SSDA is presented in Figure 5.10. The design is also based on the TSC250 DHBT foundry process model. Circuit simulations based on a full foundry model with transmission line losses and via transitions predict a 324 GHz 3dB bandwidth for the new technique (Figure 5.11). Figure 5.12 shows the planar MMIC layout for the 3-M-SSDA with bandwidth extension modifications.

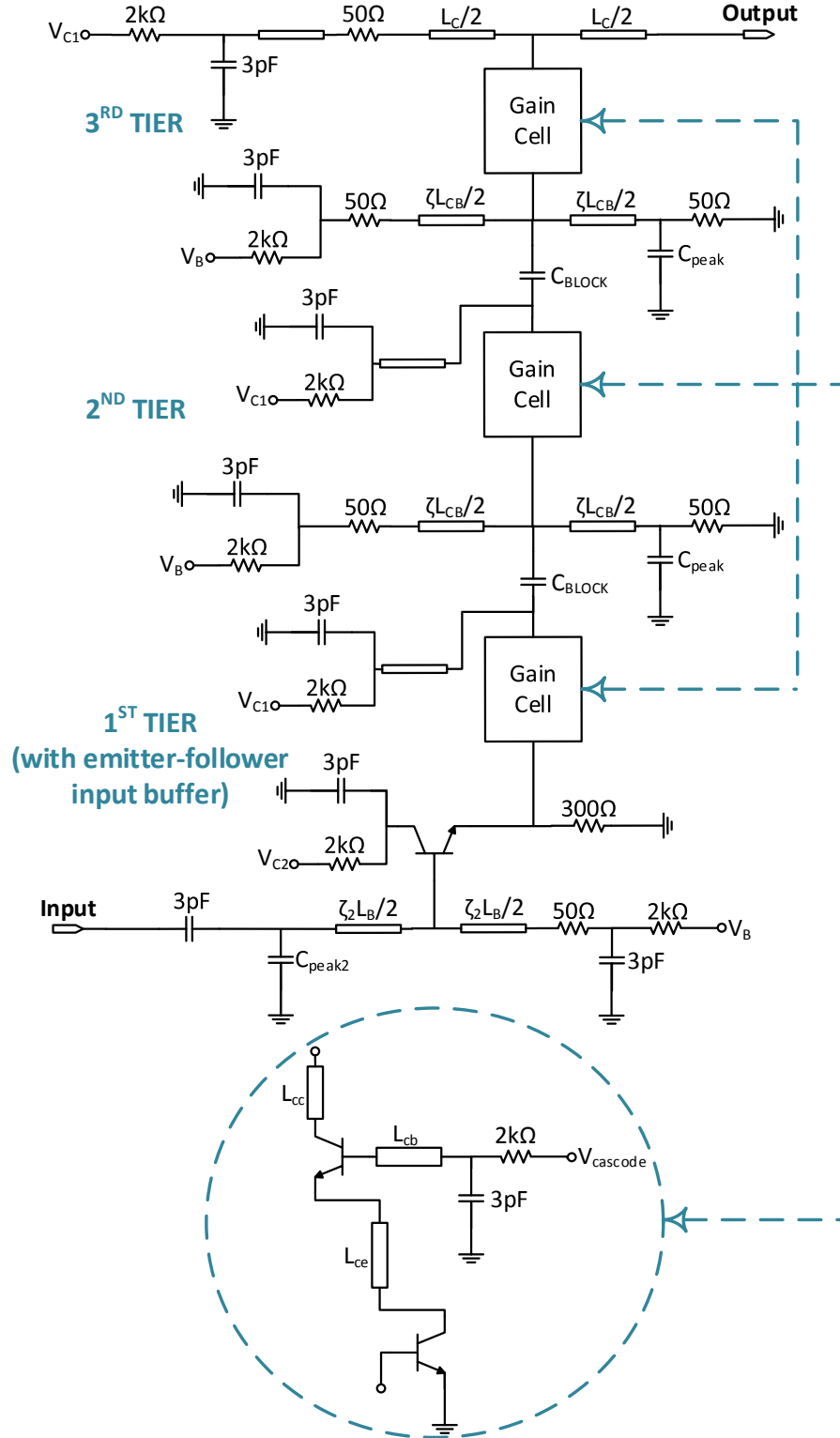


Figure 5.10: Three-tier M-SSDA schematic with scaled input and intermediate transmission lines. Inset shows the modified gain cell.

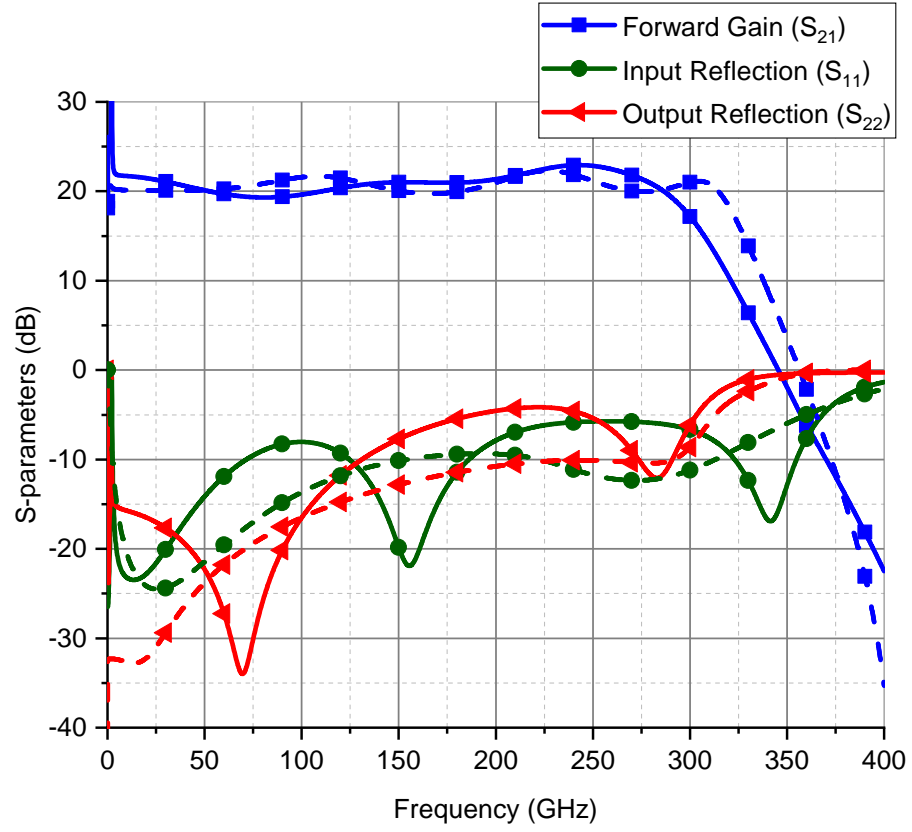


Figure 5.11: Three-tiered M-SSDA with bandwidth extension: lossless transmission lines and ideal passive element (dashed lines); lossy transmission lines, passive elements with vias and transitions (solid lines).

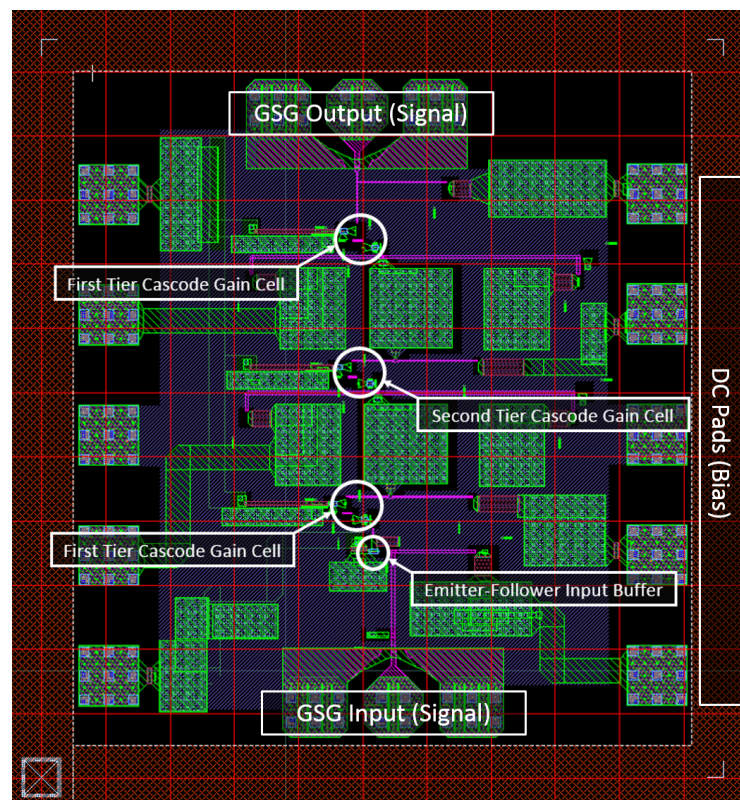


Figure 5.12: MMIC planar layout: three-tier M-SSDA with bandwidth extension (footprint:  $766 \mu\text{m} \times 800 \mu\text{m}$ ).

## 5.5 M-SSDA MMIC Measurement

Figure 5.13 shows the microphotograph of the fabricated MMIC matrix-SSDA, with actual dimension of  $1\text{ }\mu\text{m} \times 1\text{ }\mu\text{m}$ . The verification of the amplifier performance was done via small-signal on-wafer probe measurements using two measurement setups - 100 MHz – 67 GHz (shown in Figure 5.14); and 140 GHz – 220 GHz (shown in Figure 4.20)<sup>1</sup>. The low frequency response of the amplifier was measured using Keysight's N5247A PNA-X series broadband VNA, with 75  $\mu\text{m}$  145 GHz Infinity probes. The input power was set to -20 dBm to avoid saturating the amplifier. The high frequency response in the band between 140 GHz - 220 GHz was measured with PNA-X N5247A by Keysight using VDI WR-5.1 frequency extenders and WR-5.1 waveguide probes. The input power was set and calibrated at -10 dBm to accommodate for the optimal operation of the frequency extenders. The matrix MMIC amplifier required eight voltage sources to bias its three stages: three base voltage sources ( $V_{BB1}$ ,  $V_{BB2}$  and  $V_{BB3}$ ); three collector voltage sources  $V_{CC1}$ ,  $V_{CC2}$  and  $V_{CC3}$ ; one voltage source to bias the three common-base transistors forming the cascode of each gain cell (denoted by  $V_{casc}$ ); and one voltage source to bias the emitter follower (denoted by  $V_{EF}$ ). This required two additional DC power supply units compared to the measurement setup, used in characterising the SSDA, and an additional 150  $\mu\text{m}$  pitch DC probe. For ease of tunability, two Keysight ES6312A triple output programmable DC power supply units were used to supply the  $V_{BB1}$ ,  $V_{BB2}$ ,  $V_{BB3}$  and  $V_{casc}$ , while the DC supply function of an Hewlett-Packard 4145B semiconductor parameter analyzer was used for  $V_{CC1}$ ,  $V_{CC2}$ ,  $V_{CC3}$  and  $V_{EF}$ .

S-parameter measurements from the two measurement setups are presented as solid lines in Figure 5.15. A forward of gain of 12 dB and 170 GHz bandwidth was measured with good input and output matching of less than -5 dB all through the measured bandwidth. As with the measurement for the SSDA reported in the pre-

---

<sup>1</sup>Measurements were done at the Department of Microtechnology and Nanoscience (MC2), Chalmers University of Technology Göteborg Sweden on 13 - 14 March 2019.



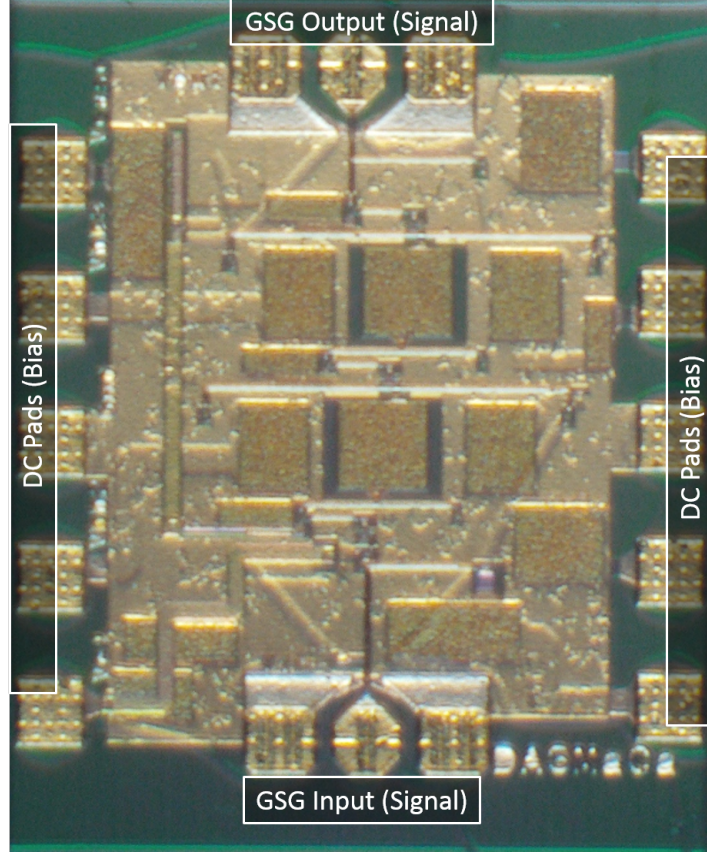


Figure 5.13: Microphotograph of the M-SSDA. MMIC size:  $770\text{ }\mu\text{m} \times 800\text{ }\mu\text{m}$ .

ceding chapter, there is also a significant departure of the measured response from what was predicted from original simulations. Hence, new post-measurement simulations were conducted (results shown in dashed lines), with additional parasitics that were not included in the foundry model.

Based on the post-measurement simulation, a good degree of agreement may be observed in the  $S_{21}$  (dB),  $S_{11}$  (dB) and  $S_{22}$  (dB) measured using the low frequency measurement setup with the performance measured from the MMIC. However, for the higher frequency measurement, while the output reflection measurement closely matches prediction, the forward gain and the input reflection do not follow the predicted profile. The amplifier also shows a sharp roll-off at 170 GHz which is peculiar, considering the relatively low input and output reflections. Comparing the simulated and measured input reflection curves, it may be observed, that at  $\sim 170$  GHz, while a sharp -40 dB dip is predicted in simulation, only a -15 dB dip is

measured, this followed by a slight peak. This, however does not fully explain the rapid gain roll-off. Considering the structure of the three-tier M-SSDA, the two intermediate transmission lines are essentially input/output transmission lines with reflections, which cannot be measured, as there are no pads connected to these lines on the M-SSDA MMIC. The cumulative effect of similar or worse reflections from these lines may well explain the overall gain response. Furthermore, as the peaking inductors required to maintain the flat gain profile are formed from transmission lines with the same properties as those used on the input, intermediate and output lines, differences in the foundry model and fabricated lines would also result in a disparity between simulated and measured responses.

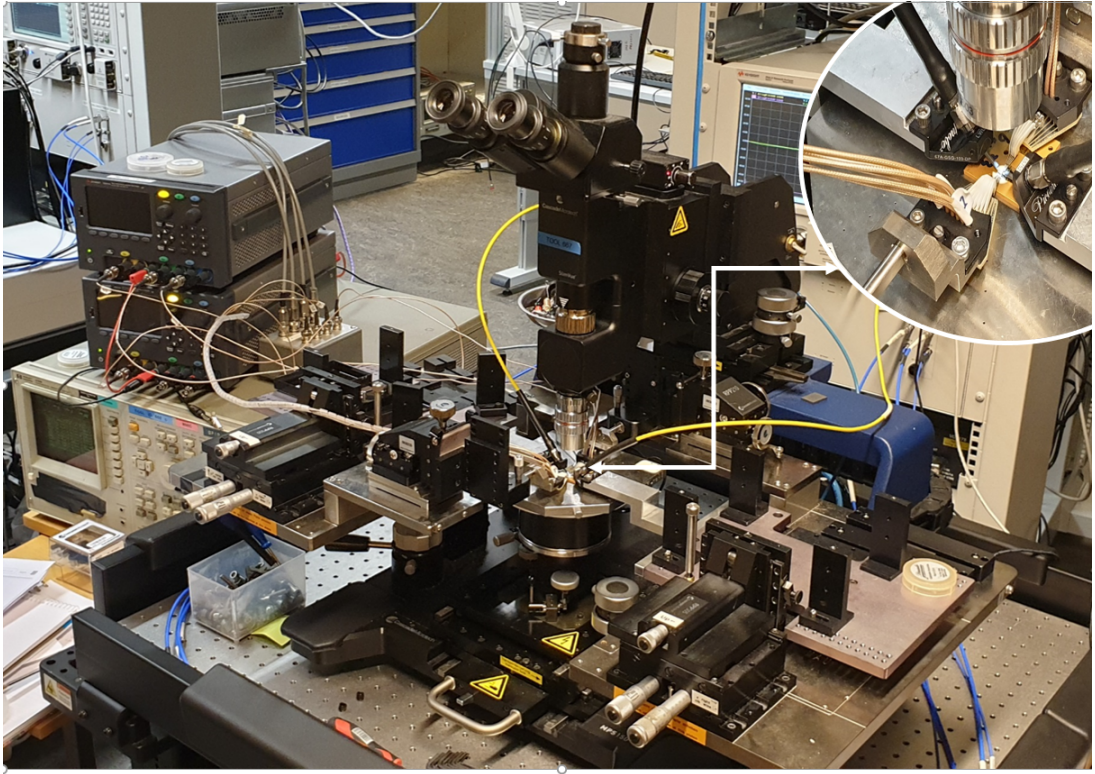


Figure 5.14: Setup for 100 MHz – 67 GHz S-parameter measurement.

Table 5.1 presents a comparison of the new M-SSDA with the state-of-the-art matrix distributed amplifiers. It is noted that the M-SSDA reported in this chapter has both the highest bandwidth and GBP of any matrix DA reported in open literature, to date.



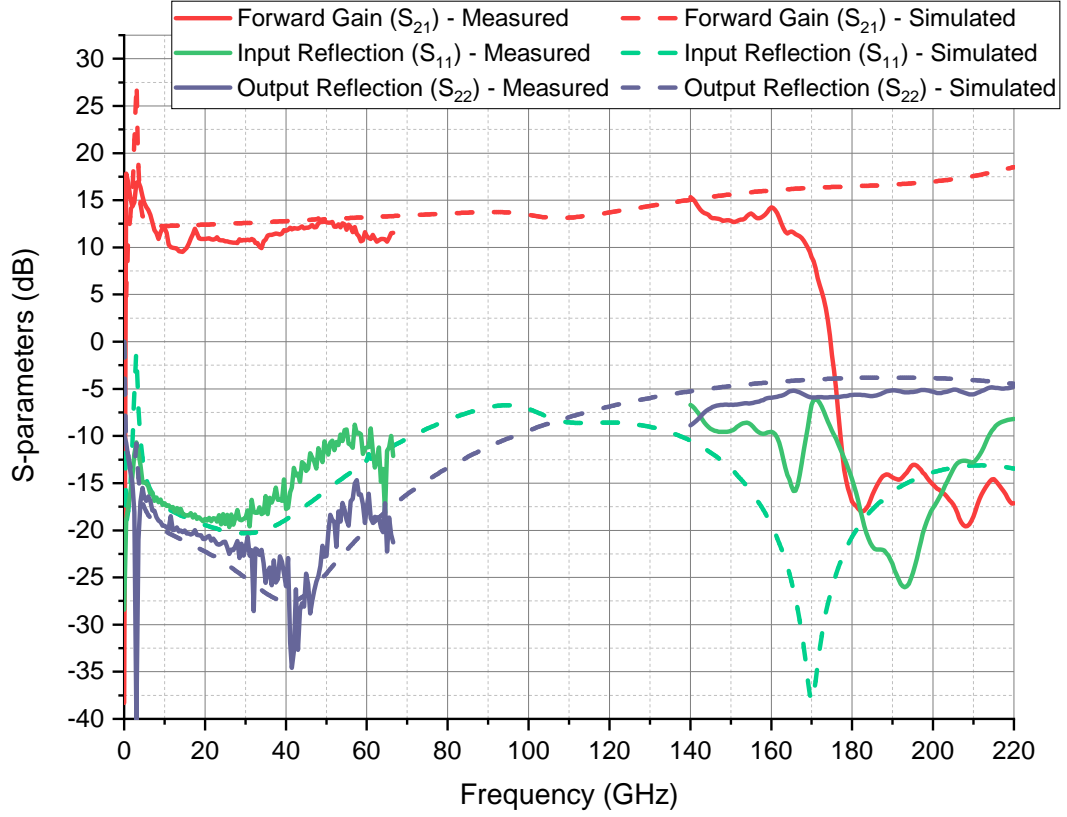


Figure 5.15: Comparison of simulated and measured responses for the three-tier M-SSDA: simulated - dashed lines; measured result - solid lines.

## 5.6 Discussion

The M-SSDA and C-SSDA topologies improve the utility of the SSDA by providing a means to achieving appreciable gain, without compromising the bandwidth. As both only feature multiplicative gain, they have been collectively termed as *multiplicative DAs*. Connected to their gain mechanism, multiplicative DAs can

Table 5.1: Comparison of the performance of new M-SSDA with state-of-the-art matrix DAs.

Technology	Gain (dB)	Bandwidth (GHz)	GBP (GHz)	Pdc (mW)	Area (mm <sup>2</sup> )	Topology	Ref
0.18 $\mu\text{m}$ CMOS	9.5	50	149	420	1.54	$2 \times 4$	[202]
0.18 $\mu\text{m}$ CMOS	6.7	45.6	99	497	1.89	$2 \times 4$	[203]
0.25 $\mu\text{m}$ GaAs PHEMT	19	19.5	174	270	7	$2 \times 4$	[204]
0.25 $\mu\text{m}$ GaAs PHEMT	20	19.5	195	500	7	$2 \times 4$	[204]
90 nm CMOS	15.4	21	124	12.5	0.41	$2 \times 4$	[205]
<b>250 nm InP HBT</b>	<b>12</b>	<b>170</b>	<b>677</b>	<b>183</b>	<b>0.28</b>	<b><math>3 \times 1</math></b>	<b>This Work</b>

offer significant advantage in power consumption, as they present the possibility of reaching a set gain target with fewer active devices than the multi-stage DA. Indeed, both multiplicative DA variants can be considered as functional equivalents, with the major advantages possessed by the M-SSDA being down to the availability of more flexibility for optimisation. With the M-SSDA, it is easier to optimise for reduced footprint by modifying the input and intermediate transmission lines without significantly compromising the matching. A similar optimisation approach can be adopted to achieve less phase delay and group delay variation. Furthermore, as M-SSDAs are more amenable to transmission lines with less inductance values than prescribed by the conventional ratio, it is possible to reduce attenuative losses and noise contributions from the ATLS.

Since the introduction of the matrix amplifier concept, there have been few reported circuits - twelve design-based publications and eight unique designs [124, 127, 200, 202–204, 206–210]. This could be attributed to a higher MMIC implementation complexity due to the intermediate transmission line and marginal comparative merits. Furthermore, while under similar conditions, the matrix and cascaded DAs would provide the same amount of gain, the matrix should, in theory, offer slightly less bandwidth as the intermediate transmission line would have a lower cut-off than the bandwidth-limiting input line of the cascaded DA (interestingly, a comparison between both topologies performed by Agostino and Paoloni (1995) reported equivalent gain and bandwidth performance under small signal conditions [210]). None of the reported matrix amplifiers is based on a SSDA, qualifying the M-SSDA as a new design, in the same order as the C-SSDA [188]. Furthermore, with the application of the bandwidth extension technique also developed as part of this PhD research, record bandwidth and gain-bandwidth product results are predicted. However, for multiplicative DAs to be considered suitable replacements for the multi-stage DA in system applications, a noise performance comparison is required. As will be explored in the next chapter, multi-stage DAs have a unique noise characteristic in that the noise figure reduces with additional stages, rather

than increase. This is not the case with multiplicative DAs, which essentially follow the Friis formula for cascaded systems, with noise increasing with additional stages. Hence, for multiplicative DAs to be useful in system applications, it is necessary to show that the gain available from this device justifies the noise it adds to system in the context of the competing multi-stage DA topology. This is the topic of the next chapter.

## 5.7 Conclusions

The M-SSDA - a multi-tier single-stage amplifier - is proposed as a more compact high gain alternative to the C-SSDA with smaller circuit footprint, potentially lower transmission line losses and better noise performance. By employing only multiplicative gain, the amplifier offers more gain-per-device than both the conventional DA and matrix amplifier. A three-tier M-SSDA circuit optimized for bandwidth and gain flatness is also presented. This design features scaled input and intermediate transmission lines and high frequency peaking is introduced through shunt capacitance. Negative resistance attenuation compensation is applied in the gain cells to achieve a flat gain profile. Simulation results based on a full foundry DHBT process predict a gain of 20 dB at 324 GHz bandwidth; this is more than a threefold bandwidth improvement compared to the basic CE M-SSDA. The three-tier M-SSDA was fabricated and measured a gain of 12 dB and 170 GHz bandwidth. While this performance falls short of pre-fabrication simulation performance, it nevertheless represents

# Chapter 6

## Noise Performance of the SSDA and its Derivative Topologies

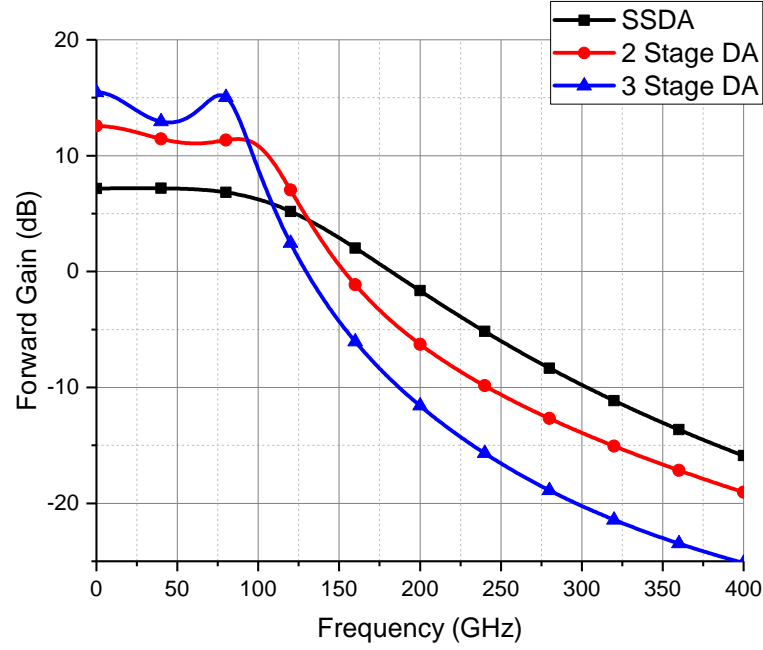
### 6.1 Introduction

Having established the potential of the single-stage and multiplicative DAs for remarkable gain-bandwidth performance, it is necessary to assess their noise performance, in order to appraise the utility of the topology in system applications. While the SSDA topology presents notable advantages in design simplicity, wide-band performance and higher average gain, it offers a poorer signal-to-noise behaviour compared to multi-stage DAs. One rather interesting merit of multi-stage DAs is that with each additional stage, the overall noise figure reduces in the amplifier passband<sup>1</sup>, improving SNR at the output - a merit that the SSDA and its derivative amplifiers do not share. Figure 6.1(a) and Figure 6.1(b) show comparisons of the forward gain and noise figure, respectively, for a single-stage, two-stage and a three-stage DA based on TSC250 common emitter gain cells, demonstrating the reduction in noise figure with additional stages. The peculiar noise performance of conventional multi-stage DAs - i.e. the possibility of reducing noise figure while simultaneously increasing gain - is a particularly valuable property.

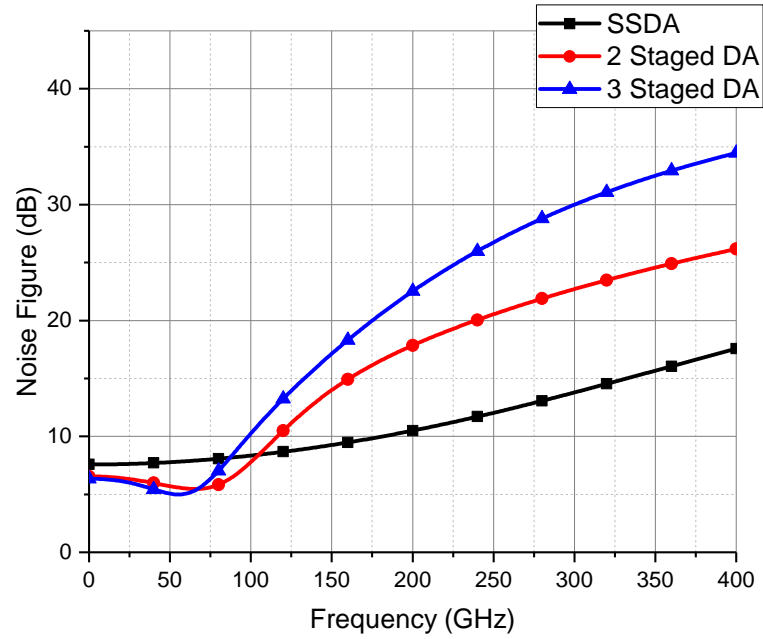
This chapter presents an analytical and simulation-based study of the noise figure of SSDA derivative topologies: the C-SSDA and M-SSDA. Studies of the

---

<sup>1</sup>This can be understood by considering an  $N$ -stage DA to which a further stage ( $N + 1$ ) is added at the output. The signal voltage contributed by the  $(N + 1)$ th stage will add linearly with the voltage contributions from the previous  $n$ -stages, while the noise contribution from the  $(N + 1)$ th stage will add quadratically [175, 199, 211].



(a) Forward gain  $S_{21}$  (dB) comparison.



(b) Noise Figure (dB) comparison.

Figure 6.1: Comparison of forward gain  $S_{21}$  (dB) and noise figure (dB) for the SSDA, two-stage and three-stage DA. Analysis based on TSC250 common-emitter gain cell with transmission lines optimised for bandwidth and gain flatness. All circuits operate at same bias.

noise figure performance of field-effect-based DAs have been reported, most definitive amongst which are the works of Niclas and others in [199, 211] and Aitchison in [175]. Noise figure analysis for cascaded and matrix DA configurations [200], with different gain cells (common emitter [175, 176, 199, 211], cascode [212] and common collector cascode [172]) and under different loading and termination conditions [213, 214] have also been reported. These studies form the bases for the extraction of models for the noise performance of the SSDA, C-SSDA and M-SSDA.

A common application of DAs is as preamplifiers, where the  $50\ \Omega$  matched source is replaced with a current input from - for instance - a photodiode. Evaluating noise performance in such cases require that the nature of the input be taken into account. Hence, expressions for the equivalent input noise current spectral density (EINCSD) for the SSDA with grounded-source (FET), common-emitter and common-collector-cascode HBT gain cells are also presented, based on models available in the open literature. These expressions are extended to multiplicative DAs with  $M$  tiers.

This chapter contains two main sections: Section 6.2 describes noise figure modelling for the SSDA, and presents new equations for the multiplicative DA, while Section 6.3 describes EINCSD modelling. In Section 6.2, following the approach advanced by Aitchison (1985) [175], the noise models for a FET SSDA based on simplified equivalent circuits are first derived, after which new equations for the multiplicative DA are derived and tested. Following a similar approach, and using a simplified equivalent HBT model, the equations derived for the FET based DA are extended to the HBT case. Considerations to adapt the Friis' formula for cascaded systems to the multiplicative DA are presented, with the adapted Friis formula, which was newly derived, and also verified. In Section 6.3, which describes EINCSD derivation, the approach advanced by Iqbal and Darwazeh (1999) [170] is adopted first in deriving the EINCSD of the FET based SSDA, after which new equations for the multiplicative DA are derived and tested.

The main focus of this chapter is to highlight the peculiarities of the SSDA topology and its multiplicative derivatives, the significance of which is to offer insight into the noise performance mechanism of the SSDA topology and present approaches to design optimisation that minimise noise and maximise gain-to-noise ratio, based on available trade-offs to match system specification. Hence, for simplicity, inductances and capacitances of the transmission line and their parasitic contributions have not been included. Also, as the noise contribution of the gain cell has already been treated exhaustively in the open literature, the outcomes of such studies have been included, rather than deriving new models.

## **6.2 Noise Figure Modelling in Multiplicative DAs**

### **6.2.1 Evaluating Single-Stage Noise Figure**

The noise sources of DAs have been identified as: noise associated with the active device(s) in each of the  $N$  gain stages; thermal noise contribution from the source impedance at the IEEE standard temperature for noise measurement ( $T_o$ ), which is 290 K (16.85° Celsius) [215]; thermal noise contribution from input and output transmission line terminations at  $T_o$ ; and noise contributions from lossy (resistive) transmission line elements [175, 211]. The noise associated with the load impedance is considered part of the network that follows the DA, and is therefore, not included as a contributor to the DA noise figure. The losses associated with the transmission line elements (which may include lossy inductors or capacitors) is also usually neglected in analysis, as these are comparatively small [175, 199, 211, 213]. This also reduces the complexity of the analysis and results in a generic model, avoiding the need for new equations to be derived for the different transmission line implementations that exist.

### For SSDAs based on FET devices

First, the case in which a field-effect transistor (FET), such as the MESFET or HEMT is used as the active device, is considered. Figure 6.2 shows a simplified equivalent circuit model for a MESFET/HEMT, featuring its associated Van der Ziel gate and drain noise sources [216].

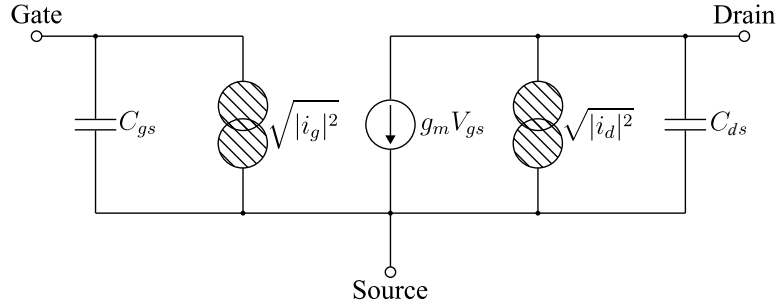


Figure 6.2: Simplified intrinsic equivalent circuit of a MESFET/HEMT with its associated gate and drain noise sources.

The noise factor ( $F$ ) of the amplifier is defined as [214]

$$F_n = 1 + \frac{\Delta \mathbf{N}}{kT_o B G_f} \quad (6.1)$$

where  $G_f$  is the DA forward gain,  $k$  is Boltzmann's constant ( $1.38 \times 10^{-23} \text{ J/K}$ ),  $B$  is the bandwidth over which noise is measured [214] and  $\Delta \mathbf{N}$  is the added noise from the amplifier to its output,

$$\Delta \mathbf{N} = \mathbf{N}(Z_{\pi d}) + \mathbf{N}(Z_{\pi g}) + \mathbf{N}_{FET} \quad (6.2)$$

where  $\mathbf{N}(Z_{\pi g}) = kT_o B$  and  $\mathbf{N}(Z_{\pi d}) = kT_o B G_r$  are the noise power contribution of the drain and gate line terminations (in a  $\pi$  transmission line configuration), respectively;  $G_r$  is the reverse gain and  $\mathbf{N}_{FET}$  is the overall noise associated with the FETs in the amplifier.  $Z_{\pi g}$  and  $Z_{\pi d}$  are  $\pi$ -image impedance of the gate (input) and drain (output) transmission lines, respectively, defined by  $Z_{\pi} = \sqrt{(L/C)/(1 - (\omega/\omega_c)^2)}$ , with  $\omega_c$  being the cut-off frequency [28, 175]. Com-



binning (6.2) and (6.1) yields

$$F_n = 1 + \frac{1}{G_f} + \frac{G_r}{G_f} + \frac{N_{FET}}{kT_o B G_f} \quad (6.3)$$

Now,

$$G_f = \frac{N^2 g_m^2 Z_{\pi g} Z_{\pi d}}{4} \quad (6.4)$$

and

$$G_r = \frac{g_m^2 Z_{\pi g} Z_{\pi d}}{4} \left( \frac{\sin n\phi}{\sin \phi} \right)^2 \quad (6.5)$$

such that

$$F = 1 + \left( \frac{\sin(N\phi)}{N \sin \phi} \right)^2 + \frac{4}{N^2 g_m^2 Z_{\pi g} Z_{\pi d}} + \frac{N_{FET}}{kT_o B G_f} \quad (6.6)$$

where  $\phi$  is the transmission line propagation delay, also referred to as the phase constant, assuming phase matched conditions.

To evaluate the noise contribution due to the active device (i.e. the fourth term of (6.6)), Aitchison (1985) introduced the two main noise contributors in the MESFET device, as originally identified by Van der Ziel [216]: the gate and drain noise contributors defined as

$$|i_g|^2 = \frac{4kT_o B C_{gs}^2 \omega^2 R}{g_m} \quad (6.7)$$

and

$$|i_d|^2 = 4kT_o B g_m P \quad (6.8)$$

respectively, where  $R$  and  $P$  are dimensionless coefficients from Van der Ziel's FET noise behaviour model that depend on bias conditions, device geometry and other technological parameters [216, 217]. This results in

$$F = 1 + \left( \frac{\sin(N\phi)}{N \sin \phi} \right)^2 + \frac{4}{N^2 g_m^2 Z_{\pi d} Z_{\pi g}} + \frac{Z_{\pi g} \omega^2 C_{gs}^2 R \sum_{r=1}^N f(r, \phi)}{N^2 g_m} + \frac{4P}{N g_m Z_{\pi g}} \quad (6.9)$$

where

$$f(r, \phi) = (N - r + 1)^2 + \left( \frac{\sin((r - 1)\phi)}{\sin\phi} \right)^2 + \frac{2(N - r + 1)\sin(r - 1)\phi \cos r\phi}{\sin\phi} \quad (6.10)$$

Equation (6.10) accounts for the phase difference between the two noise sources;  $\phi = 2\sin^{-1}(\omega/\omega_c)$ ;  $N$ , as usual, is the number of amplifier stages; and  $r$  represents individual stages.

D'Agostino *et al.* (1990) [200] have suggested that the accuracy of (6.9) may be improved by adopting a more suitable model for high frequency noise analysis for MESFETS and HEMTs, derived by Cappy (1988) in [218], which accounts for the effect of the  $C_{gd}$ .

$$\overline{i_d^2} = 4kT_o B g_m P \left[ 1 + \left( \frac{f}{f_o} \right)^2 \right] \quad (6.11)$$

where

$$f_o = \frac{g_m}{2\pi C_{gd}} \quad (6.12)$$

Hence, (6.9) becomes

$$F = 1 + \left( \frac{\sin(N\phi)}{N\sin\phi} \right)^2 + \frac{4}{N^2 g_m^2 Z_{\pi d} Z_{\pi g}} + \frac{Z_{\pi g} \omega^2 C_{gs}^2 R \sum_{r=1}^N f(r, \phi)}{N^2 g_m} + \frac{4P}{N g_m Z_{\pi g}} \left[ 1 + \left( \frac{f}{f_o} \right)^2 \right] \quad (6.13)$$

However, noting that  $C_{gd}$  is quite low in microwave transistors (making  $f_o$  very large), the  $(f/f_o)^2$  factor results in marginal differences to  $F$ , even at high frequencies<sup>2</sup>.

---

<sup>2</sup>The accuracy of (6.13) may be further improved by including the correlation between the two noise currents  $\sqrt{i_g^2}$  and  $\sqrt{i_d^2}$ , which can be evaluated by  $\Psi = i_g i_d^* / \sqrt{i_g^2 \cdot i_d^2}$  [175, 200]. However, to simplify the analyses, the convention of considering FET noise sources as uncorrelated, is followed. The approach of excluding the correlation between the two noise currents is further

The following inferences can be drawn from (6.13), all pointing to the clear noise-advantage of the multi-stage DAs over the SSDA.

1. The second term is small for large  $N$ , except for  $N\phi \approx 0$  or  $\pi$ , when the expression has a maximum value of unity; for other phase angles, the term can be minimised by increasing  $N$ .
2. The third term is the reciprocal of the forward available gain, and can also be minimised by increasing  $N$ .
3. The fourth and fifth terms, which account for noise contributions from the MESFET gate and drain noise generators, respectively, also reflect inverse proportionality to  $N$ , and can be made negligible by increasing  $N$ .

For a single-stage FET DA, the second term in (6.9) assumes its maximum value of unity, also,  $f(r, \phi) = \sum_{r=1}^N f(r, \phi) = 1$ , reducing (6.13) to

$$F = 2 + \frac{4}{g_m^2 Z_{\pi d} Z_{\pi g}} + \frac{Z_{\pi g} \omega^2 C_{gs}^2 R}{g_m} + \frac{4P}{g_m Z_{\pi g}} \quad (6.14)$$

### For SSDAs based on bipolar devices

Following the approach through which (6.14) has been derived, an equivalent expression for the noise figure of the SSDA based on an intrinsic bipolar transistor (neglecting noise contribution from  $r_{bb}$ ) as shown in Figure 6.3, may be written as

$$F = 2 + \frac{4}{g_m^2 Z_{\pi b} Z_{\pi c}} + \frac{N_{HBT}}{kT_o B G_f} \quad (6.15)$$

where forward power gain

$$G_f = \frac{g_m^2 Z_{\pi b} Z_{\pi c}}{4} \quad (6.16)$$

Similar to the FET,  $Z_{\pi b}$  and  $Z_{\pi c}$  are noise contributions from the source and load impedances (in a  $\pi$ -transmission line implementation), respectively and  $C_\pi$

---

justified when we consider the observations of D'Agostino *et al.* (1990) and Chang *et al.* (1989) that  $\bar{i}_g^2$  and  $\bar{i}_d^2$  feed purely real impedances and the correlation coefficient is purely imaginary [134, 200].

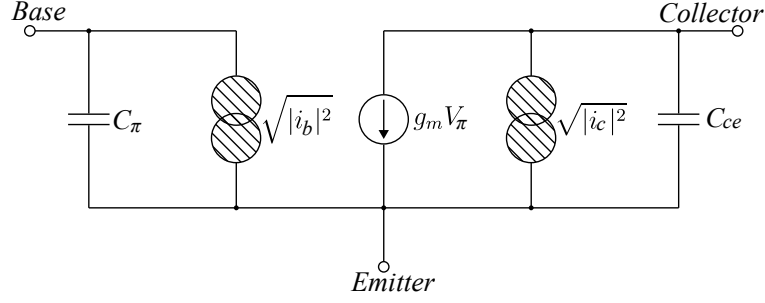


Figure 6.3: Simplified intrinsic equivalent circuit of a bipolar transistor with its associated base and collector noise sources.

and  $C_{ce}$  are intrinsic elements from the HBT equivalent circuit; and  $N_{HBT}$  comprises of the noise from the HBT noise sources  $i_b$  and  $i_c$ , given by,

$$\overline{i_b^2} = 4kT_o B R e (Y_{ebp} - Y_{ce}) + 2kT_o B g_{be} \quad (6.17)$$

and

$$\overline{i_c^2} = 2kT_o B g_m \quad (6.18)$$

where  $Y_{ebp} = gm\sqrt{2j\omega\tau_D}/\tanh\sqrt{2j\omega\tau_D}$  is the hole admittance of the emitter junction;  $Y_{ce} = gm\sqrt{2j\omega\tau_D}/\sinh\sqrt{2j\omega\tau_D}$  is the transfer admittance of the transistor;  $\tau_D$  is the diffusion time through the base region; and  $g_{be}$  is the total input conductance, as defined by Van Der Ziel and Bosman (1984) [219,220].

While it is clear that the SSDA has a disadvantage in noise performance, it is possible to improve the gain-to-noise performance ratio by considering some design trade-offs. Firstly, by inspecting (6.14) and (6.15), we can see that increasing  $Z_{\pi g}$  and  $Z_{\pi b}$ , the second and last terms can be made smaller, reducing  $F$  in both cases. However, from the equation describing the gain of the DA, it may be recalled that this would also increase the overall gain of the DA, but limits the bandwidth.

Another approach, with the potential of improving performance, can be obtained from trade-offs available in the design of the multiplicative SSDAs. To arrive at these, first, it is necessary to define how the noise figure scales with additional gain-cell tiers in cascaded and matrix SSDAs.

### 6.2.2 Modelling of Noise Factor in Multiplicative DAs

A few publications that focused on multiplicative DAs have been reported: Niclas and Chang in [199] and D'Agostino *et al.* [200] for the matrix amplifier; and Zadeh and Nikmehr in [221] covering the cascaded DA. Analysis in both [199] and [221] employ the chain matrix equations of the active devices and transmission line networks and can be readily scaled for any number of gain-cell tiers.

Niclas and Chang (1988) in [199] presented a comprehensive analysis of the matrix amplifier and provide valuable insight into the noise behaviour and tradeoffs of multiplicative DAs, by comparing the gain, noise performance and VSWR of the matrix amplifier with an equivalent cascaded DA<sup>3</sup>. Their work provides an analytical and experimental basis for the near parity in performance of the matrix amplifier and cascaded DA topologies. While, in their paper, they did report that the maximum noise figure of the matrix amplifier was some 0.6 dB lower than for the equivalent cascaded DA, it has been observed from extensive simulation-based studies that this is not an inherent advantage of the matrix topology. Rather, the observed noise performance advantage may be attributed to the lower noise contributions from the lossy transmission lines and other reactive elements - which can be made smaller in matrix amplifiers, without significant compromise to gain or bandwidth performance. This position is supported by their further observation that in including noise figure in the (transmission line) design optimization process, the difference between the maximum noise figures of equivalent gain amplifiers in both configurations increased from 0.6 dB to an excess of 2 dB in favour of the matrix amplifier. This can be proven analytically by including transmission line elements (and their accompanying losses) in the noise figure model.

Particularly relevant to this discussion is that in [199], it was demonstrated both analytically and by experimental validation that "*...the first tier of active devices contributes the largest portion of noise while the noise contribution of the*

---

<sup>3</sup>In this case, equivalence was regarded as the employment of identical types and number of devices in both the cascaded DA and matrix amplifier, however, both amplifiers were individually optimised for best gain and reflection performance [199].

second (and successive) tiers (are) only a small fraction of that of the first tier". This observation is significant, in that it ties in with much earlier observations by Friis in the study of noise figure in cascaded networks [222], setting the basis for a closed form expression for the overall noise figure of multiplicative DAs based on Friis formula for cascaded networks.

Figures 6.4(a) and 6.4(b) compare the forward gain and noise figure, respectively, of a single-stage, two-tier and three-tier MSSDA, based on TSC250 common-emitter gain cell with transmission lines optimised for bandwidth and gain flatness. It may be observed that while the gain scales in an exponential fashion, the increase in noise figure is quadratic, with the first stage contributing more than 70% to the overall noise figure of the three-tier M-SSDA.

For a FET-based DA with  $M$ -multiplicative tiers, the overall added noise a sum of noise ( $\mathbf{N}$ ) contributions, stated as

$$\Delta \mathbf{N} = \mathbf{N}(Z_{\pi d}) + \mathbf{N}(Z_{\pi g}) + \sum \mathbf{N}(Z_{\pi-int}) + \sum \mathbf{N}_{FET} \quad (6.19)$$

where the third term accounts for the sum of noise contributions from all the intermediate transmission line terminations and the last term accounts for the sum of noise contributions from the active devices on all tiers, such that the noise factor  $F_M^{mlt}$  - where the superscript  $mlt$  indicates the multiplicative DA and the subscript ( $M$ ) denotes the number of gain tiers - may be derived as

$$F_M^{mlt} = 1 + \frac{1}{G_f} + \frac{G_r}{G_f} + \sum_{i=1}^{M-1} \frac{G_r}{G_{int}(i)} + \sum_{l=1}^M \frac{\mathbf{N}_{FET}(l)}{kT_o B G_f^l} \quad (6.20)$$

$G_{int}(i)$  represents the cumulative gain, up to the  $i$ th tier, of the  $M$ -tier multiplicative DA, and the third term of the equation is multiplied by 2 to account for the presence of two equal terminating resistors on the intermediate line. With the last term of (6.20), the overall noise contribution is effectively computed, by referring noise contributions from individual stages to the input.

Forward power gain,

$$G_f = \frac{g_m^{2M} Z_{\pi int}^{2(M-1)} Z_{\pi g} Z_{\pi d}}{4^M} \quad (6.21)$$

however, as under usual bias conditions,  $C_{gs} \gg C_{ds}$ ,  $Z_{\pi int} \approx Z_{\pi g}$ , such that  $G_f \approx (N^2 g_m^2 Z_{\pi g} Z_{\pi d} / 4)^M$ , (6.20), for  $M > 1$  becomes

$$F_M^{mlt} = 2 + \left( \frac{4}{N^2 g_m^2 Z_{\pi g} Z_{\pi d}} \right)^M + 2 \sum_{l=0}^{M-1} \left( \frac{4}{N^2 g_m^2 Z_{\pi g} Z_{\pi d}} \right)^l + \left( \frac{Z_{\pi g} \omega^2 C_{gs}^2 R}{g_m} + \frac{4P}{g_m Z_{\pi g}} \right) \sum_{l=0}^{M-1} \left( \frac{4}{N^2 g_m^2 Z_{\pi g} Z_{\pi d}} \right)^l \quad (6.22)$$

where  $l$  is the gain-tier index. From (6.22), we may observe that the highest proportion of total noise is contributed by the first stage, and the noise contribution from successive stages is only a small fraction of the one preceding it. This is expected in multiplicative amplifiers and agrees with the findings in [199], which followed a chain matrix approach in deriving the overall noise figure in matrix amplifiers. It also suggests that in the case where the gain and noise figure of individual stages are known, the Friis formula for evaluating overall noise figure in cascaded systems may be applicable [222].

An equivalent expression for the intrinsic noise figure of the HBT-based multiplicative DAs may be readily derived following the approach adopted in arriving at (6.20).

$$\Delta \mathbf{N} = \mathbf{N}(Z_{\pi b}) + \mathbf{N}(Z_{\pi c}) + \sum \mathbf{N}(Z_{\pi-int}) + \sum \mathbf{N}_{HBT} \quad (6.23)$$

where  $N(Z_{\pi b})$ ,  $N(Z_{\pi c})$  are noise contributions from the input (base), output (collector) transmission line termination, respectively;  $\sum \mathbf{N}(Z_{\pi-int})$  is the sum of the noise contributions from the intermediate transmission line terminations and the last term,  $\sum \mathbf{N}_{HBT}$ , is the sum of the noise contributions from the HBT devices

on all the amplifier gain tiers. The overall noise figure is therefore given by

$$F_M^{mlt} = 2 + \frac{1}{G_f} + 2 \sum_{i=1}^{M-1} \frac{G_r}{G_{int}(i)} + \sum_{l=1}^M \frac{N_{HBT}(l)}{kT_o B G_i} \quad (6.24)$$

$G_f = G_r = (g_m^2 Z_{\pi b} Z_{\pi c} / 4)^M$  and  $G_i$  is the gain calculated from the gain-tier being considered to the output, such that for the first gain stage,  $G_i = G_f$ .

Equation (6.22) may be verified by considering the case of a multiplicative DA with identical stages such that  $F = F_1 = F_2 = \dots = F_m$ , and  $G = G_1 = G_2 = \dots = G_M$ . The noise figure of the SSDA may be re-written as

$$F = 2 + \frac{1}{G} + F_{FET} \quad (6.25)$$

where  $G$  is the single-stage gain and  $F_{FET}$  is the noise figure contribution from the FET device and covers the third and last terms of (6.14). In the same vein, (6.22) for a two tiered multiplicative DA may also be re-written as

$$\begin{aligned} F_2^{mlt} &= 2 + \frac{2}{G} + \frac{1}{G^2} + F_{FET} + \frac{F_{FET}}{G} \\ &= 2 + \frac{1}{G} + F_{FET} + \frac{1}{G} \left( 1 + \frac{1}{G} + F_{FET} \right) \\ &= F + \frac{F - 1}{G} \end{aligned} \quad (6.26)$$

Similarly, the noise factor for a multiplicative DA with three tiers  $F_3^{mlt}$  may also be written as

$$F_3^{mlt} = F + \frac{F - 1}{G} + \frac{F - 1}{G^2} \quad (6.27)$$

such that  $F_m^{mlt}$  in (6.22) may be re-written for a multiplicative DA with identical gain tiers as

$$F_M^{mlt} = F + \frac{F - 1}{G} + \frac{F - 1}{G^2} + \dots + \frac{F - 1}{G^{M-1}} \quad (6.28)$$

If we recall the Friis formula for cascaded systems [222],

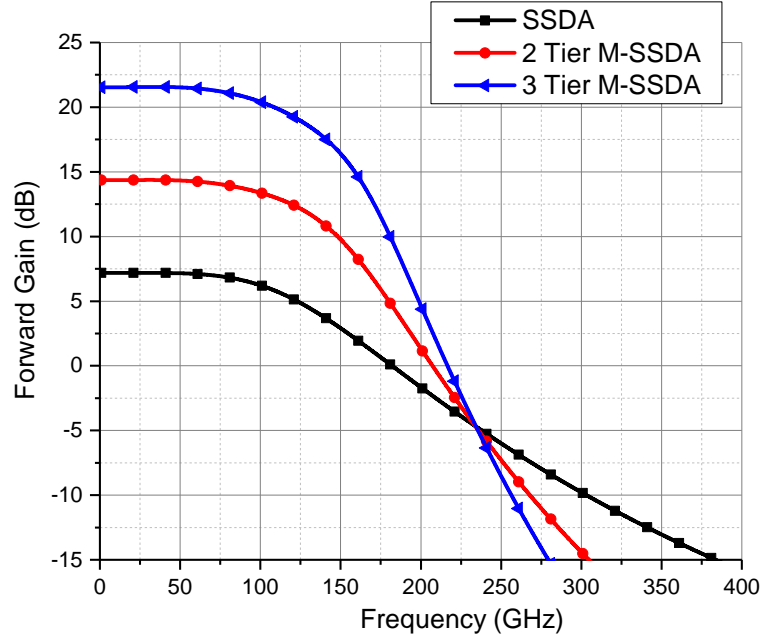
$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots + \frac{F_M - 1}{G_1 G_2 \dots G_{M-1}} \quad (6.29)$$



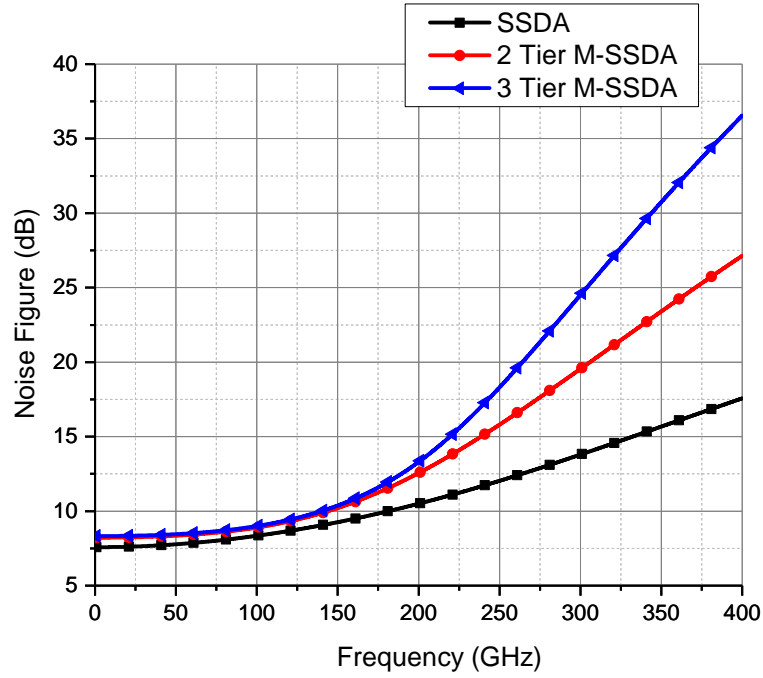
where  $F_{total}$  is the total noise factor,  $F_i$  and  $G_i$  are the noise factor and available power gain, respectively, of the  $i$ -th stage, and  $M$  is the number of cascade stages. The equivalence of the  $F_{total}$  in (6.29) and  $F_m^{mlt}$  in (6.28), under the conditions of identical gain tiers may be clearly observed. Indeed, (6.28) may be generalised to the case in which the gain tiers are non-identical, if the noise figure and gain of individual stages are known, and for  $m > 1$ ,

$$F_M^{mlt} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots + \frac{F_M - 1}{G_1 G_2 \dots G_{M-1}} \quad (6.30)$$

Figures 6.5(a) and 6.5(b) shows the result of the application of the derived models in estimating the noise figure of a two- and a three-tier M-SSDA, respectively, based on a common-emitter gain cell with a full foundry process model of Teledyne TSC250 DHBT InP device [11,13]. The close agreement between both solid and dashed lines - representing simulated and modelled results, respectively - within the 3 dB bandwidth of the amplifier ( $\sim 100$  GHz) validates the derived equation. The deviation - which increases with frequency - is attributed to contributions from the inductive reactance - which increases with frequency - from the transmission lines, which has not being subtracted from the noise contributions from the individual stages.

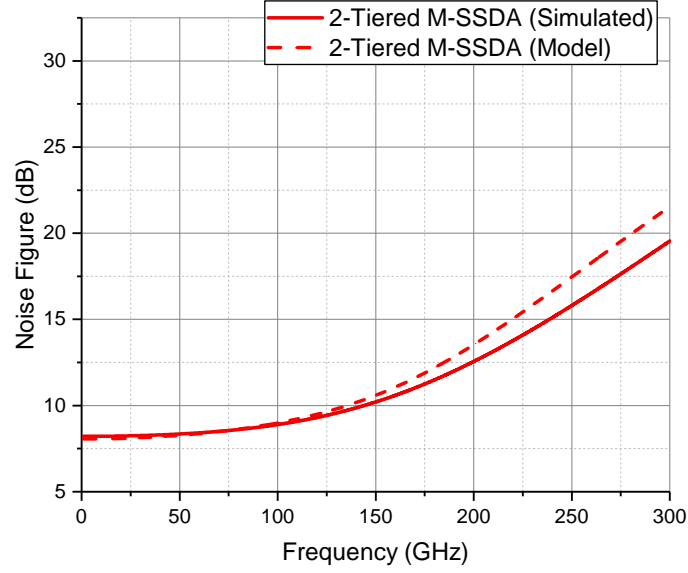


(a) Forward gain  $S_{21}$  (dB) comparison

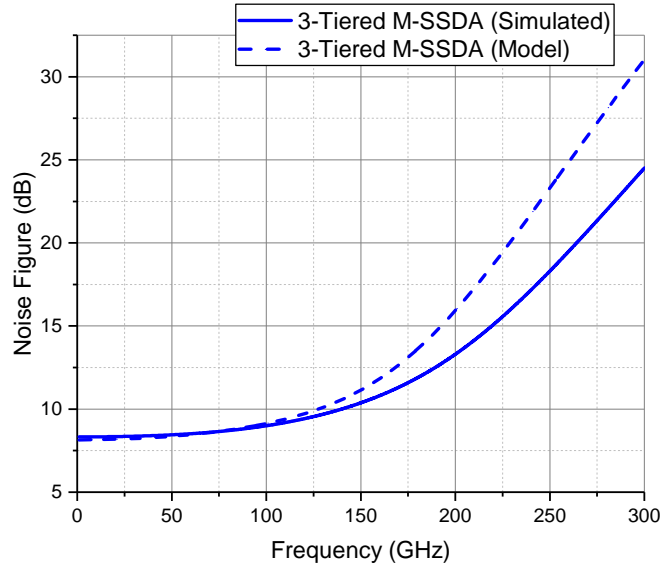


(b) Noise Figure (dB) comparison

Figure 6.4: Comparison of gain and noise figure for the SSDA, two-tier and three-tier M-SSDA. Analysis based on TSC250 common-emitter gain cell with transmission lines optimised for bandwidth and gain flatness. All circuits operate at same bias.



(a) Two-tier M-SSDA



(b) Three-tier M-SSDA

Figure 6.5: Verification of (6.22): comparison based on a common-emitter gain cell using foundry model of TSC250 as active device, with transmission lines optimised for bandwidth and gain flatness.

## 6.3 EINCSD of Single-Stage and Multiplicative DAs

It is common to analyse and report the noise properties of an amplifier in terms of its noise figure. However, by definition, the noise figure applies only to amplifiers that are excited by a purely resistive signal source, hence, it is not applicable when the signal source impedance contains a reactive component. An example of such applications is the optical front-end receiver, due to presence of a photodiode junction capacitance. For such applications, it is more useful to consider the total output port noise, referred to the input of the amplifier [223]. For the optical front-end receiver, the equivalent input noise current spectral density is of primary interest as it allows the front-end noise to be compared directly with the current signal generated by the photodiode [223].

### 6.3.1 Evaluating Single-Stage EINCSD

Two main techniques have been advanced in the evaluation of the EINCSD. One approach is to derive the noise voltage spectral density (NVSD) at the output of the amplifier, and referring this to the input (as noise current spectral density at the input - EINCSD) by dividing by the amplifier transimpedance gain [170] - this approach is adopted in this thesis. The alternative technique is to derive the noise current spectral densities of each noise contributing element, referred to the input, and taking a sum of the squares of each element [176]. For a SSDA based on a simplified equivalent FET model as shown in Figure 6.2, three noise sources may be defined - the input terminating impedance; the output terminating impedance; and the FET comprising of the gate and drain noise sources. The noise voltage due each of these current sources -  $v_{o1}$ ,  $v_{o2}$  and  $v_{o3}$ , respectively (as depicted in Figure 6.6), is subsequently defined. Thereafter, the expression is extended to define the noise voltage of the multiplicative amplifier.

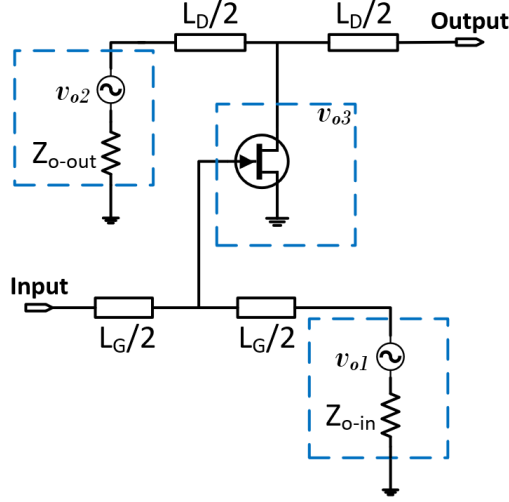


Figure 6.6: Noise voltage sources in a SSDA.

The EINCSD ( $i_{neq}$ ) is obtained by dividing  $v_{nout}$  by the amplifier transimpedance gain  $|A_{tz}|$

$$i_{neq} = \frac{v_{nout}}{|A_{tz}|} \quad (6.31)$$

The total noise voltage at the output  $v_{nout}$ , which is the noise voltage spectral density (NVSD), is the square-root of the sum of the squares of each of the uncorrelated noise voltage contributions is given by

$$v_{nout} = \sqrt{|v_{o1}|^2 + |v_{o2}|^2 + |v_{o3}|^2} \quad (6.32)$$

For a SSDA with equal terminating impedances,  $A_{tz}$  is the same in both forward i.e. at the terminating load ( $Z_f$ ) and the reverse direction i.e. at the drain termination ( $Z_r$ ), and is given by [176]

$$A_{TZ} = Z_f = Z_r = \frac{g_m Z_{\pi g} Z_{\pi d}}{2} \quad (6.33)$$

where  $Z_{\pi g}$  and  $Z_{\pi d}$  are the  $\pi$ -image impedances of the input and output transmission lines of the DA, respectively [32, 50, 176].

### Noise voltage contribution from input terminating impedance $Z_g$

The NCSD generated by  $Z_g$  is given by

$$|i_{Z_g}|^2 = \frac{4kT_0}{Z_g} \quad (6.34)$$

For a SSDA, half of the noise current  $i_{Z_{\pi g}}$  is directly absorbed by  $Z_{\pi g}$  itself, while the other half travels toward the input. As this is ideally an open circuit (current source), this signal gets totally reflected. The total voltage that appear at the output due to this source is given by

$$v_{o1} = i_{Z_g} A_{TZ} (1 + e^{-j\frac{\phi}{2}}) \quad (6.35)$$

where  $\phi = \omega\sqrt{L_g C_{gs}}$  is the transmission line propagation delay of the input transmission line.

### Noise voltage contribution from output terminating impedance $Z_d$

The NCSD generated by  $Z_d$  is given by

$$|i_{Z_d}|^2 = \frac{4kT_0}{Z_d} \quad (6.36)$$

Half of the noise current from the drain termination is dissipated in  $Z_{\pi d}$  itself while the other half travels down the drain line and gets dissipated in the output, producing a noise voltage,  $v_{o2}$ ,

$$v_{o2} = \frac{i_{Z_d}}{2} Z_d e^{-j\frac{\rho}{2}} \quad (6.37)$$

where  $\rho = \omega\sqrt{L_d C_{ds}}$  is the transmission line propagation delay of the output transmission line, and  $C_{ds}$  is the FET drain-source capacitance.

### Noise voltage contribution from the FET

The noise current sources for a FET transistor, as previously defined are the gate noise source given in (6.7) and the drain noise source given in (6.8). The gate noise contribution may be separated into two components: the first component is the forward travelling wave, which will produce an output voltage with a forward transimpedance gain. The second component is the reflected wave, due to the reverse wave reflecting off the open circuit at the input. This wave will also produce a voltage with the reverse transimpedance gain [176], such that the total output noise voltage due to  $i_g$  is given by

$$v_{out}^g = \frac{i_g}{2} Z_f + \frac{i_g}{2} Z_r = i_g A_{TZ} \quad (6.38)$$

For the drain noise, half of the drain noise current travels toward the drain termination ( $Z_d$ ) and is absorbed, while the other half travels toward the load and produces a corresponding output voltage, such that total current due to  $i_g$  can be written as

$$i_{out}^d = \frac{i_d}{2} e^{-j\frac{\rho}{2}} \quad (6.39)$$

with corresponding output voltage given by

$$v_{out}^d = i_{out}^d Z_d = \frac{i_d}{2} Z_d e^{-j\frac{\rho}{2}} \quad (6.40)$$

The square of the overall output noise voltage due to the FET noise ( $v_{o3}$ ) is, therefore, given by

$$v_{o3}^2 = |i_g A_{TZ}|^2 + \left| \frac{i_d}{2} Z_d e^{-j\frac{\rho}{2}} \right|^2 \quad (6.41)$$

Hence, substituting (6.35), (6.37) and (6.41) in (6.32),

$$v_{nout} = \sqrt{\left| i_{Z_g} A_{TZ} (1 + e^{-j\frac{\phi}{2}}) \right|^2 + \left| \frac{i_{Z_d}}{2} Z_d e^{-j\frac{\theta}{2}} \right|^2 + \left| i_g A_{TZ} \right|^2 + \left| \frac{i_d}{2} Z_d e^{-j\frac{\theta}{2}} \right|^2} \quad (6.42)$$

and the EINCSD ( $i_{neq}$ ) is obtained by dividing  $v_{nout}$  given by (6.42), by the amplifier transimpedance  $|A_{tz}|$  given by (6.33).

Figure 6.7 shows the contributions from the gate termination ( $i_{n1}$ ), the drain termination ( $i_{n2}$ ), and the FET ( $i_{n3}$ ) to total EINCSD for a single-stage FET DA with terminations  $Z_g = Z_d = 50 \Omega$ , and a simplified equivalent model based on Figure 6.2 is used as gain cell, where  $g_m$  of 50 mS;  $C_{gs}$  and  $C_{ds}$  of 50 fF and 5 fF, respectively; and FET transistor parameters R and P of 0.2 and 0.6, respectively. As seen in Figure 3, the major noise contributor in the low frequencies is the gate line termination, with minimal noise contribution from the drain (output) line termination. The noise contribution from the active device is dominated in the lower frequencies by the drain noise component ( $|i_d|$ ). However, at higher frequencies, the gate noise component ( $|i_g|$ ) dominates, due to the presence of the  $\omega^2$  factor, which also explains the continuous rise of the FET noise contribution beyond cut-off (Figure 6.7)

### 6.3.2 EINCSD for Multiplicative DAs

To extend (6.32) to multiplicative DAs, the noise voltage for the terminations  $Z_{int}$  on intermediate transmission lines - which we will denote as  $v_{o-int}$  - must be included. Figure 6.8 shows the noise sources for the matrix multiplicative DA using a FET gain cell. The last term in (6.32),  $v_{o3}$ , which represents the FET noise contribution, must also be expanded to include all the gain tiers of the preamplifier. First, the transimpedance gain of the multiplicative DA with  $M$  gain tiers ( $A_{tz}^{mlt}$ ) is defined, which for the multiplicative DA is equal in both the forward ( $Z_f^{mlt}$ ) and



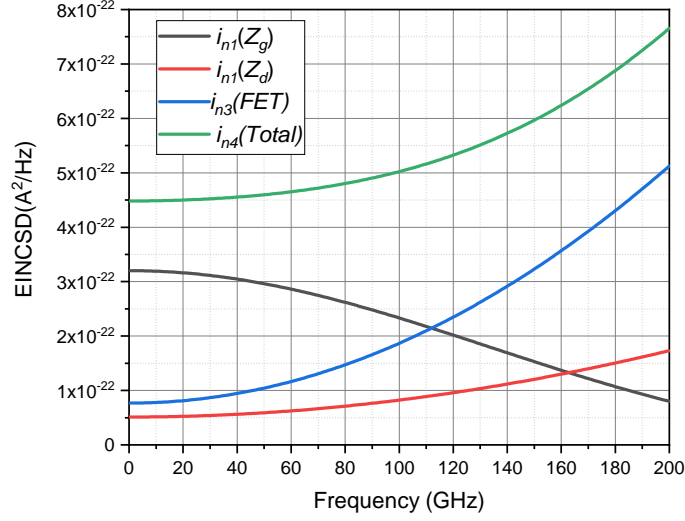


Figure 6.7: Components of the total EINCSD of the SSDA.

reverse ( $Z_r^{mlt}$ ) direction and is given by

$$A_{TZ}^{mlt} = Z_f^{mlt} = Z_r^{mlt} = \frac{g_m^m}{2^m} Z_{\pi g} Z_{\pi d} Z_{\pi-int}^{m-1} \quad (6.43)$$

where  $Z_{int}$  is the image impedance of the intermediate transmission lines, and the superscript -*mlt*- reflects that this refers to a multiplicative DA.

The total noise voltage at the output of the multiplicative DA,  $v_{nout}^{mlt}$  is given by

$$v_{nout}^{mlt} = \sqrt{|v_{o1}^{mlt}|^2 + |\sum v_{o-int}^{mlt}|^2 + |v_{o2}^{mlt}|^2 + |\sum v_{o3}^{mlt}|^2} \quad (6.44)$$

where  $v_{o1}^{mlt}$  and  $v_{o2}^{mlt}$  are the noise voltages due to the input and output line terminations, respectively; and  $\sum v_{o-int}^{mlt}$  and  $\sum v_{o3}^{mlt}$  are the sums of noise voltages from the intermediate line terminations and FET, respectively, and  $i_{neq}^{mlt}$ , which is the EINCSD, is given by

$$i_{neq}^{mlt} = \frac{v_{nout}^{mlt}}{A_{TZ}^{mlt}} \quad (6.45)$$

### Noise voltage contribution from input and output terminating impedance

The noise voltage contribution of the input terminating impedance for a multiplicative DA with  $mlt$  stages -  $v_{o1}^m$  - is the noise current multiplied by total transimpedance gain,

$$v_{o1}^{mlt} = i_{Z_g} A_{TZ}^{mlt} (1 + e^{-j\frac{\phi}{2}}) \quad (6.46)$$

The noise voltage due to the output terminating impedance, as is to be expected, remains unchanged for the multiplicative DA. However in keeping with a consistent convention, this is rewritten as  $v_{o2}^{mlt}$ , with

$$v_{o2}^{mlt} = \frac{i_{Z_d}}{2} Z_d e^{-j\frac{\phi}{2}} \quad (6.47)$$

### Noise voltage contribution from intermediate terminating impedance

The noise voltage contributions from the terminating impedances on the intermediate lines  $Z_{\pi-int}$  is derived by considering a two-tier multiplicative DA, which has only one intermediate transmission line. Assuming purely resistive terminations, the thermal noise current generated by each terminating resistor is given by

$$|i_{Z_{int}}|^2 = \frac{4kT_o}{Z_{int}} \quad (6.48)$$

with corresponding voltage  $v_{Z_{\pi-int}}$  being the product of the intermediate line current and the transimpedance gain at that point relative to the input

$$v_{Z_{int}} = \frac{i_{Z_{int}}}{4} g_m Z_{\pi d} Z_{int} \quad (6.49)$$

Unlike on the output (drain) line, where half of the termination noise current gets absorbed by the termination itself while the other half travels towards and gets dissipated in the output, the presence of two terminating resistances at opposite ends of the intermediate line results in a voltage noise source,  $v_{o-int}^{mlt}$ , which is a square root of the sum of the squares of the uncorrelated noise voltages from

each of the terminations. Considering the usual case in which both terminating impedances on the intermediate line are equal, then

$$v_{o-int}^{mlt_2} = \sqrt{2v_{Z_{\pi-int}}^2} \quad (6.50)$$

Equation (6.49) may be extended for a multiplicative DA with  $m$  gain tiers and  $(m-1)$  intermediate transmission lines, where all intermediate transmission lines are terminated with equal resistances, as

$$v_{o-int}^{mlt} = \sqrt{\sum_{p=1}^{M-1} \left| \frac{i_{Z_{int}}}{2^p} g_m^p Z_g Z_{\pi d} Z_{int}^p \right|^2} \quad (6.51)$$

### Noise voltage contribution from the FET

Equation (6.41) may be extended to the multiplicative amplifier by taking a sum of all the noise voltage excitations due to the FET noise current sources for each tier of the multiplicative DA, which essentially is the noise current multiplied by the transimpedance gain relative to the output. The overall output noise voltage from the FET in the multiplicative amplifier with  $m$  gain tiers -  $v_{o3}^{mlt}$  - is given by

$$v_{o3}^{mlt} = \sqrt{\sum_{p=1}^M \left| \frac{i_g}{2^p} g_m^p Z_{\pi g} Z_{\pi d} Z_{int}^{(p-1)} \right|^2 + \sum_{p=1}^M \left| \frac{i_d}{2^{(p-1)}} Z_{\pi d} Z_{int}^{(p-1)} \right|^2} \quad (6.52)$$

Substituting (6.46), (6.51), (6.47) and (6.52) in (6.44),

$$v_{nout}^{mlt} = \sqrt{\begin{aligned} & |i_{Z_g} A_{TZ}^{mlt} (1 + e^{-j\frac{\phi}{2}})|^2 + \left| \frac{i_{Z_d}}{2} Z_d e^{-j\frac{\phi}{2}} \right|^2 \\ & + \sum_{p=1}^{M-1} \left| \frac{i_{Z_{int}}}{2^p} g_m^p Z_g Z_{\pi d} Z_{int}^p \right|^2 \\ & + \sum_{p=1}^M \left| \frac{i_g}{2^p} g_m^p Z_{\pi g} Z_{\pi d} Z_{int}^{(p-1)} \right|^2 \\ & + \sum_{p=1}^M \left| \frac{i_d}{2^{(p-1)}} Z_{\pi d} Z_{int}^{(p-1)} \right|^2 \end{aligned}} \quad (6.53)$$

such that  $i_{neq}^{mlt}$ , which is the sought expression, is given by

$$i_{neq}^{mlt} = \frac{1}{A_{TZ}^{mlt}} \sqrt{\begin{aligned} & \left| i_{Z_g} A_{TZ}^{mlt} (1 + e^{-j\frac{\phi}{2}}) \right|^2 + \left| \frac{i_{Z_d}}{2} Z_d e^{-j\frac{\phi}{2}} \right|^2 \\ & + \sum_{p=1}^{M-1} \left| \frac{i_{Z_{int}}}{2^p} g_m^p Z_g Z_{\pi d} Z_{int}^p \right|^2 \\ & + \sum_{p=1}^M \left| \frac{i_g}{2^p} g_m^p Z_{\pi g} Z_{\pi d} Z_{int}^{(p-1)} \right|^2 \\ & + \sum_{p=1}^M \left| \frac{i_d}{2^{(p-1)}} Z_{\pi d} Z_{int}^{(p-1)} \right|^2 \end{aligned}} \quad (6.54)$$

The dominant contribution of the noise source from the input line terminating impedance ( $i_{Z_{\pi g}}$ ) to the overall NVSD and EINCSD, may be observed in the first terms of (6.53) and (6.54), as it is multiplied by the full forward transimpedance gain of the amplifier, while the intermediate transmission line terminations are multiplied by progressively less gain values. The gate noise  $i_g$  of the FET device at the first stage of the amplifier also occupies a similar position. However, due to its frequency dependence (as seen in (6.7)), its noise contribution at low frequencies is minimal, and grows as the amplifier approaches cut-off.

The derived equations are employed in plotting the graphs in Figures 6.9(a), 6.9(b) and 6.9(c), which show the transimpedance gain, total RMS NVSD at the output port and the EINCSD at each stage of a five-tier matrix-SSDA, respectively. This is to demonstrate how the EINCSD scales with additional gain tiers in multiplicative DAs. A simplified equivalent model based on Figure 6.2 is used as gain cell, with  $g_m$  of 50 mS;  $C_{gs}$  and  $C_{ds}$  of 50 fF and 5 fF, respectively; and FET transistor parameters R and P of 0.2 and 0.6, respectively. The M-SSDA features conventional 50  $\Omega$  input, output and intermediate transmission line terminations. Similar to the observation from the noise figure analysis (Figure 6.4), more than 70% of the total EINCSD for the five gain tiers of the amplifier is contributed by the first stage.

Figure 6.10 shows the effect of the input termination on transimpedance, noise voltage and noise current spectral densities for a five-tier M-SSDA, using a simplified equivalent HEMT model. In Figure 6.10(a), it may be observed that increasing the input terminating impedance, results in increased transimpedance gain. There is also an improvement in the low frequency EINCS D performance, as seen in Figure 6.10(c). In Figure 6.11, the limited effect of the output terminating resistor on performance may be observed. This is because, while the output line termination also results in an increase in transimpedance gain, there is a nearly commensurate increase in the overall noise voltage at the output; such that the EINCS D remains fairly unchanged.

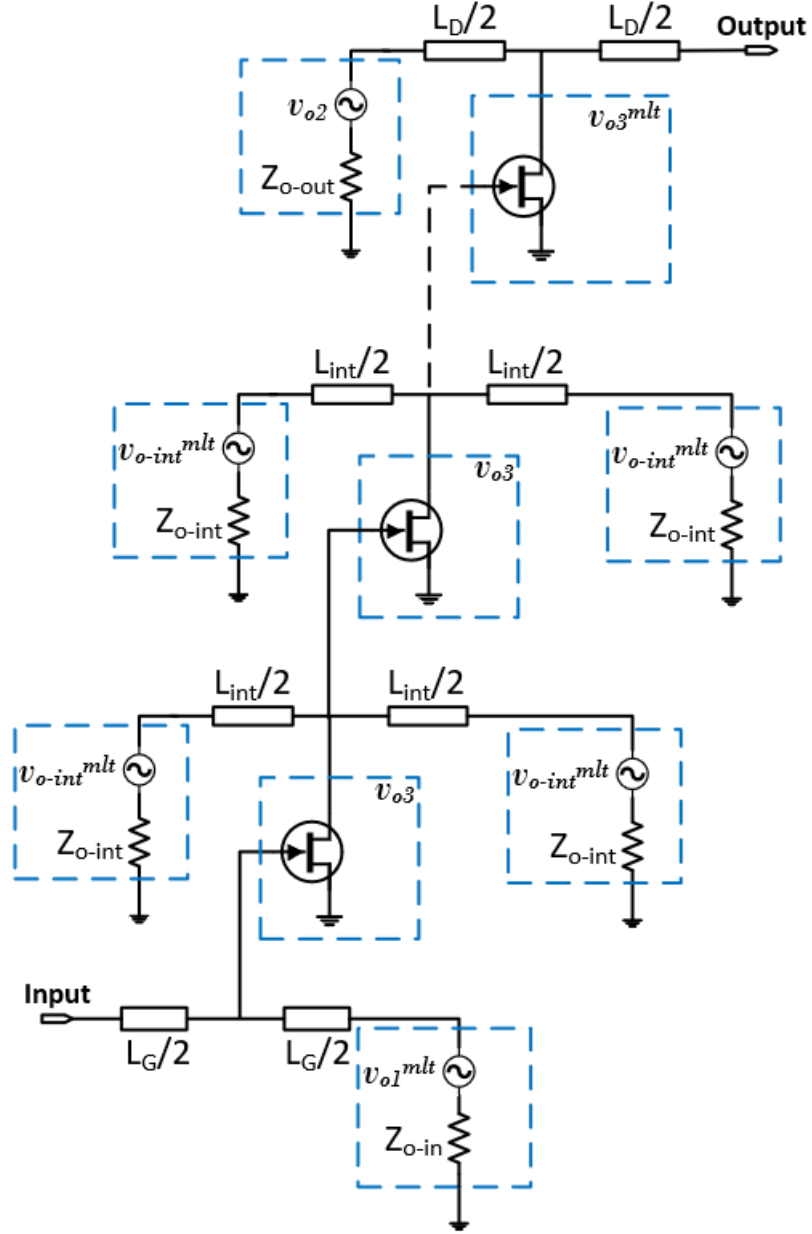
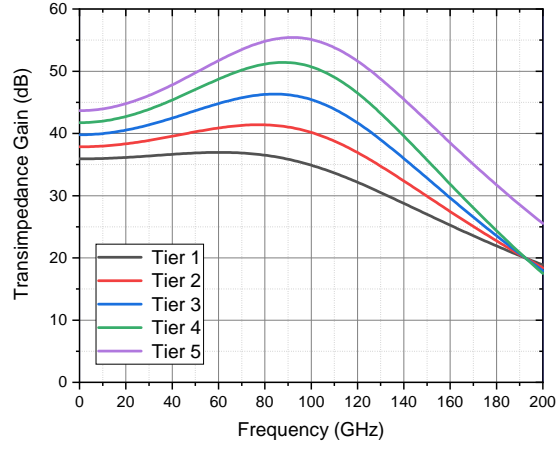
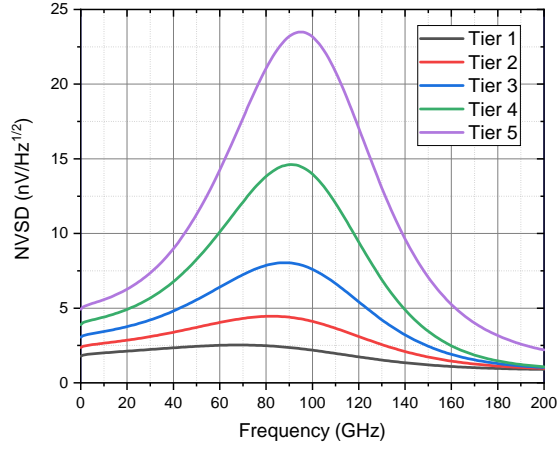


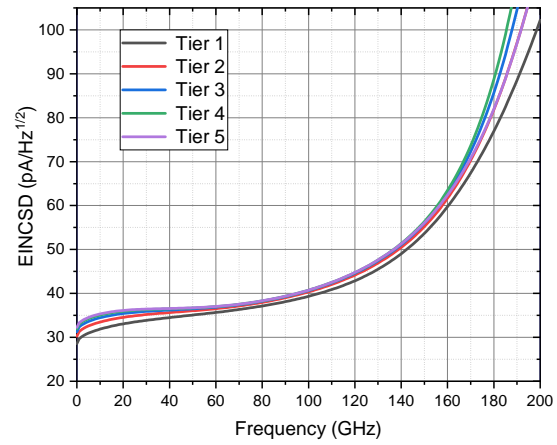
Figure 6.8: Noise voltage sources in a matrix multiplicative FET DA.



(a) Transimpedance gain

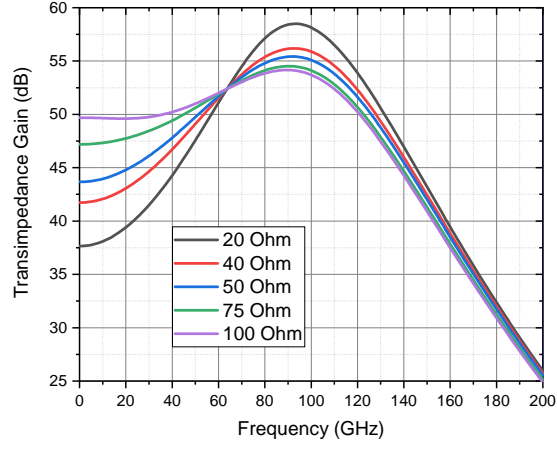


(b) Total rms noise voltage spectral density (NVSD) at output port

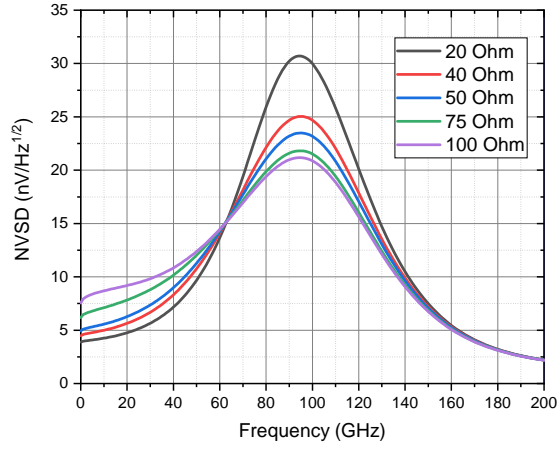


(c) Equivalent input noise current spectral density (EINCSD)

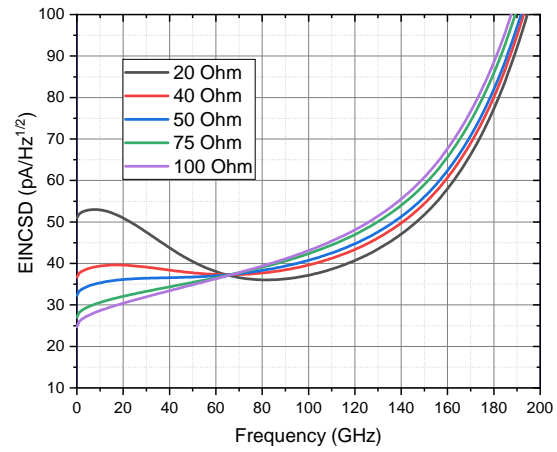
Figure 6.9: The scaling of transimpedance, noise voltage and noise current spectral densities in multiplicative amplifiers using a simplified equivalent HEMT model.



(a) Transimpedance gain



(b) Total rms noise voltage spectral density (NVSD) at output port



(c) Equivalent input noise current spectral density (EINCSD)

Figure 6.10: The effect of different values of input termination on transimpedance, noise voltage and noise current spectral densities for a five-tier M-SSDA using simplified equivalent HEMT model.



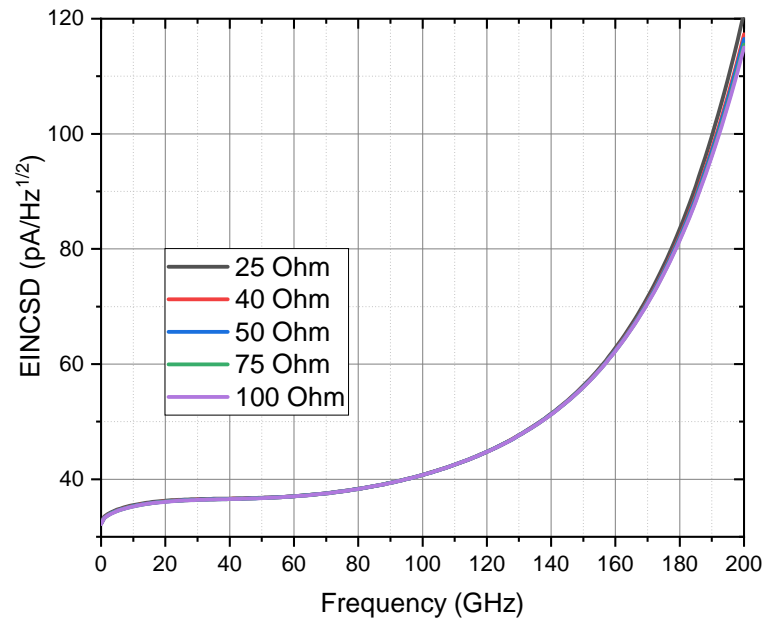


Figure 6.11: The effect of different values of output termination on noise current spectral density on a five-tier M-SSDA using a simplified equivalent HEMT model.

### 6.3.3 Design guide for optimising EINCSD in multiplicative DAs

A step-by-step guide to determine and optimise the EINCSD of a multiplicative DA is presented as follows.

- Obtain key noise parameters for the active device i.e.  $i_g$  and  $i_d$  for FETs ( $i_b$  and  $i_c$  for bipolar devices).
- Determine output NVSD contributions from the input, out and intermediate transmission line terminations using (6.46), (6.47) and (6.51), respectively; and from the active device using (6.52).
- The input noise current spectral densities due to each of the output NVSD contributors may be determined by dividing each of these NVSDs by the  $A_{TZ}$  given in (6.43).
- The EINCSD is obtained from (6.54), and is root of the sum of the squares of the individual input noise current spectral densities.
- Optimise EINCSD by maximising the value of the input line termination and minimising the noise contribution from the active device on the first stage. This may be achieved by choosing a FET with low  $C_{gs}$  and  $g_m$ , to minimise  $i_g$  and  $i_d$  for the first stage. Choosing an active device with lower  $g_m$  will reduce the transimpedance gain of the amplifier, however this loss in gain may be offset by using higher- $g_m$  devices in the other gain tiers of the amplifier.

The key equations for determining the EINCSD of a multiplicative DA are presented in Table 6.1

Table 6.1: Design guide for optimising EINCSD: *Key equations with numbering.*

Equation	No.
$A_{tz}^{mlt} = \frac{g_m^m}{2^m} Z_{\pi g} Z_{\pi d} Z_{\pi-int}^{m-1}$	6.43
$v_{o1}^{mlt} = i_{Z_g} A_{TZ}^{mlt} (1 + e^{-j\frac{\phi}{2}})$	6.46
$v_{o2}^{mlt} = \frac{i_{Z_d}}{2} Z_d e^{-j\frac{\rho}{2}}$	6.47
$v_{o-int}^{mlt} = \sqrt{\sum_{p=1}^{M-1} \left  \frac{i_{Z_{int}}}{2^{(p)}} g_m^{(p)} Z_{\pi d} Z_{int}^p \right ^2}$	6.51
$v_{o3}^{mlt} = \sqrt{\sum_{p=1}^M \left  \frac{i_g}{2^p} g_m^p Z_{\pi g} Z_{\pi d} Z_{int}^{(p-1)} \right ^2 + \sum_{p=1}^M \left  \frac{i_d}{2^{(p-1)}} g_m^{(p-1)} Z_{\pi d} Z_{\pi-int}^{(p-1)} \right ^2}$	6.52
$i_{neq}^{mlt} = \frac{1}{A_{TZ}^{mlt}} \sqrt{\left  i_{Z_g} A_{TZ}^{mlt} (1 + e^{-j\frac{\phi}{2}}) \right ^2 + \left  \frac{i_{Z_d}}{2} Z_d e^{-j\frac{\rho}{2}} \right ^2 + \sum_{p=1}^{M-1} \left  \frac{i_{Z_{int}}}{2^p} g_m^p Z_g Z_{\pi d} Z_{int}^p \right ^2 + \sum_{p=1}^M \left  \frac{i_g}{2^p} g_m^p Z_{\pi g} Z_{\pi d} Z_{int}^{(p-1)} \right ^2 + \sum_{p=1}^M \left  \frac{i_d}{2^{(p-1)}} Z_{\pi d} Z_{int}^{(p-1)} \right ^2}$	6.46

## 6.4 Discussion: Noise Performance Optimisation for Multiplicative DAs

Some inferences can be drawn from observing (6.9), in comparison to (6.14), all pointing to the clear noise-advantage of the multi-stage DAs over the SSDA. Firstly, the second term is small for large  $N$  except for  $N\phi \approx 0$  or  $\pi$ , when the expression has a maximum value of unity; for other phase angles, the term can be minimised by increasing  $N$ . It may also be observed that the third term is the reciprocal of the forward available gain, and can also be minimised by increasing  $n$ . Also, the fourth and fifth terms, accounting for noise contributions from the FET gate and drain noise generators, respectively, also reflect inverse proportionality to  $n$ , and can be made negligible by increasing  $N$ .

However, while it is clear that the SSDA has a disadvantage in noise performance, it is possible to improve gain-to-noise ratio of the multiplicative DA by considering available design trade-offs. A major insight that both (6.22) and the adapted Friis formula offer is the need to make the noise factor of the first stage of the multiplicative DA as low as possible, while keeping the gain high. Firstly, by inspecting (6.14), it may be observed that increasing the impedance of the input line  $Z_{\pi g} - Z_{\pi b}$  in the HBT-based case - the second and last terms can be made smaller, reducing  $F$  in both the first tier and the overall amplifier. This would also result in increased gain, from (6.4). However, the cut-off frequency of the input line, and as a result, the amplifier bandwidth would be reduced commensurately.

From the EINCSD analysis, it may also be noted that as  $M$  increases, the noise current contribution from successive transmission lines of the multiplicative DA reduces, with the least contribution coming from the output line. This is observed, by considering that in (6.53) and (6.54), only the noise contribution from the input termination noise source is multiplied by the full transimpedance gain of the amplifier, with the contributions from higher tiers multiplied by lower gain values based on their position relative to the output. This, again, supports

the approach of maximising the gain of the first stage and designing the input line for minimum noise contribution by making the input line impedance as large as design bandwidth specifications allows.

An alternative solution that does not sacrifice bandwidth, but slightly increases design complexity, is to use a transistor with a higher bandwidth potential in the first stage. We might recall that the main bandwidth limiting intrinsic elements of the FET and HBT active devices,  $C_{gs}$  and  $C_{\pi}$ , respectively, are both dependent on bias current and emitter/source area. This presents a trade-off: a smaller active area reduces the input capacitance, thus increasing the bandwidth, but yielding lower gain and lower output power due to lower transconductance values [17, 165]. Adopting such a device in the first stage creates an allowance to design the transmission line of the first stage at a higher characteristic impedance with reduced overall bandwidth penalty. The shortfall in gain can then be compensated for, by using transistors with higher transconductance in subsequent gain-cell tiers.

## 6.5 Summary and Conclusions

The highlights of the discussion presented in this chapter are as follows.

- Contrary to noise behaviour of the multi-stage DAs, noise figure increases with each added gain-cell tier of multiplicative DAs (i.e. both matrix amplifiers and cascaded DAs). However, the noise contribution from an additional stage is only a fraction of the contribution of the stage before it, in agreement with the principle of noise scaling in cascaded systems.
- While the SSDA and its multiplicative DA derivatives exhibits a slightly poorer noise figure and gain-to-noise ratio, when compared to the multi-stage DA, this drawback is offset by the gain advantage of the multiplicative DA.
- It is possible to improve noise performance of the SSDA by designing the input transmission line at a higher impedance level, such that  $Z_{\pi g}$  in FET-

based SSDAs and  $Z_{\pi b}$  in bipolar SSDAs can be made larger. However, from the equation describing the gain of the DA, while this would also increase gain, the bandwidth will be commensurately reduced.

- A closed-form expression for the noise figure of multiplicative DAs based on Friis' formula for cascaded networks was derived. This equation was verified for a two- and three-tier M-SSDA, based on a common-emitter gain cell, by comparison with results from simulation based on the foundry transistor model for Teledyne's TSC250.
- Expressions that describe the NVSD at the output and the EINCSD of the SSDA are derived. From these expressions, new equations that model the NVSD and EINCSD for the multiplicative DA are derived and verified.
- Based on observations from the analysis, design considerations that draw on the peculiarities of the multiplicative DA topology and may yield optimal results in noise, gain and bandwidth performance to match design requirements and specifications, were presented.

Having considered the noise performance merit of the conventional multi-stage DA, vis-à-vis its gain performance limitation, the case for multiplicative single-stage DAs becomes even more compelling. While the noise figure of the multiplicative SSDA increases quadratically with additional stages, this trend is offset by the gain, which increases exponentially, progressively increasing the margin between amplification and added noise. Furthermore, considering that the limitations of the multi-stage DA become more pronounced in ultra-high frequency designs - as process parasitics become more prominent in their effect - a stronger justification is found for adopting such single-stage based DAs.

## Chapter 7

# Application of Transmission Line Synthesis Techniques in Optical and Visible Light Communication Systems

This chapter considers the application of circuit design techniques that could be considered native to distributed amplification, in the context of optical and visible light communication systems. In the first section, the design and application of an analogue pre-emphasis filter, to compensate for the bandwidth limitation of optical transceivers, is presented. Pre-emphasis is achieved through a  $T$ -half high-pass filter section, using discrete components and PCB transmission lines. A sensitivity improvement of 1.1 dB is achieved with a direct modulated laser (DML)-based 64 Gbps PAM4, after transmission over 1 km of single mode fibre. In the second section, the concept of incorporating the bandwidth limiting capacitance of light emitting diodes (LEDs) into a *pseudo*-ATL (*p*-ATL), thus modifying the device frequency response and improving bandwidth performance, is described and tested by simulation in ADS.

## 7.1 Pre-emphasis equalizer based on $T$ -half filter section for sensitivity improvement in bandwidth limited transceivers

Digital pre-emphasis techniques are widely employed in communication systems, to compensate for the high frequency roll-off of bandwidth-limited optical transceivers. The digital pre-emphasis essentially trades off the magnitude of signal low frequency components for flat frequency response, resulting in reduced signal-to-noise ratios (SNRs) due to the partial use of the full output range of the digital-to-analogue converter (DAC). This trade-off between SNR and bandwidth becomes prominent with the growing need for high order modulation formats. To mitigate the SNR degradation, a simple and low cost analogue pre-emphasis filter based on the  $T$ -derived filter section is used to compensate for the frequency roll-off, demonstrating 1.1 dB increase in receiver sensitivity for 64 Gbps direct-detected PAM4 signals, using a DML.

### 7.1.1 Pre-emphasis Equalizer Design

Figure 7.1(a) shows the schematic diagram of the RF pre-emphasis filter. In this study, a second-order passive equalizer circuit, which is a modification of the constant- $K$   $T$ -half filter, is employed [28, 224]. Resistors  $R_1$  and  $R_2$  are added to set the pre-emphasis level, while the inductance and capacitance values were selected to achieve the desired frequency response slope. The circuits were input and output matched to 50  $\Omega$  transmission lines. The values of the components for two circuits, designed for 3 dB and 6 dB pre-emphasis levels are summarized in Table 7.1. The pre-emphasis level is defined as the power gain applied to the highest frequency component with respect to the 100 MHz frequency component.



The transfer function of the circuit is given by

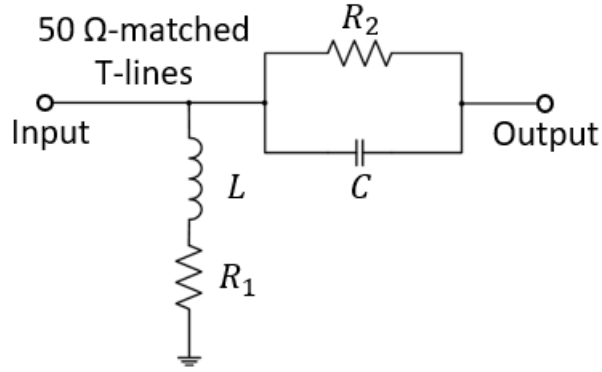
$$H(s) = \frac{R - 1 + (L + R_1 C)s + LCs^2}{R_1 + R_2 + (L + R_1 C)s + LCs^2} \quad (7.1)$$

with the pre-emphasis level set by the ratio  $R_1/(R_1 + R_2)$  and zero at  $1/R_2 C$ . The required inductance values may be realized using the self-inductance of lengths of copper, and off the shelf surface mount microwave capacitors and resistors may be adopted in implementing the design.

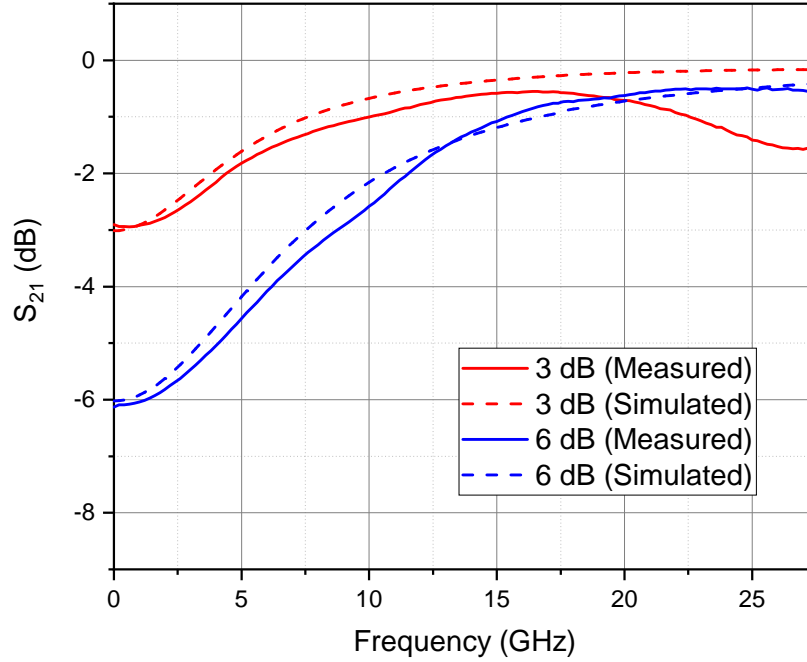
Figure 7.1(b) shows the frequency response ( $S_{21}$ ) of the two circuits. The dotted curves show the designed  $S_{21}$  in simulation and the solid curves show the measured  $S_{21}$  using a vector network analyzer (Keysight N5227A), with a resolution of 0.1 GHz. The red and blue curves represent the response of the 3 dB and 6 dB RF pre-emphasis filters, respectively. At peak amplitude, the 3 dB and 6 dB filters have insertion losses of 0.6 dB and 0.8 dB, respectively. The measured frequency roll-off of the 3 dB RF pre-emphasis filter (red solid curve) was mainly due to the frequency limitation of the standard SMA connectors used in the circuit. This imperfection was eliminated in the 6 dB RF pre-emphasis circuit by using precision SMA connectors, resulting in a flat high frequency response up to 27 GHz. The slope of the filter roll-off can be customized by careful optimization of the values of the circuit components, to compensate for different system frequency roll-off. It is worth pointing out that the filters are designed to compensate for transceivers with a smooth frequency roll-off. A more sophisticated design will be required for a transceiver that has a more complex frequency response, with fluctuations or dips in their  $S_{21}$  characterization. A frequency response similar to what is shown in 7.1(b) could be achieved by a constant-resistance bridged-T amplitude equalizer, as described in [225]. However, the adopted design, being more compact, offers the potential for wider bandwidth performance, and lower insertion loss.

Table 7.1: Parameters for RF pre-emphasis filter.

Pre-emphasis level	3 dB	6 dB
$R_1$	100 $\Omega$	100 $\Omega$
$R_2$	10 $\Omega$	50 $\Omega$
C	3 pF	0.5 pF
L	3 nH	2.5 nH



(a) Circuit diagram



(b) Frequency response

Figure 7.1: (a) Circuit diagram of RF pre-emphasis filter; and (b) Frequency response of the 3 dB and 6 dB RF pre-emphasis filter. Red curve: 3 dB; Blue curve: 6 dB; Dotted line: Simulation result; Solid line: Measured result (with 0.1 GHz).

### 7.1.2 Principle of SNR enhancement

The signal chain model in Figure 7.2 is used to illustrate the principle of SNR enhancement and to present a comparison of analogue and digital pre-emphasis. Assuming uniformly distributed quantization error and added white Gaussian noise, due to the thermal noise and sampling jitter, a DAC with  $\eta$  effective number of bits (ENOB) can achieve an SNR (dB) of [226]

$$SNR = 6.02\eta + 1.76 \quad (7.2)$$

A smooth frequency roll-off, as shown in Figure 7.2(b) is used as an example, where  $S(f)$  represents the normalized system frequency response,  $f_{max}$  is the high signal frequency at which the signal power is attenuated by  $S_{min}$  (dB).

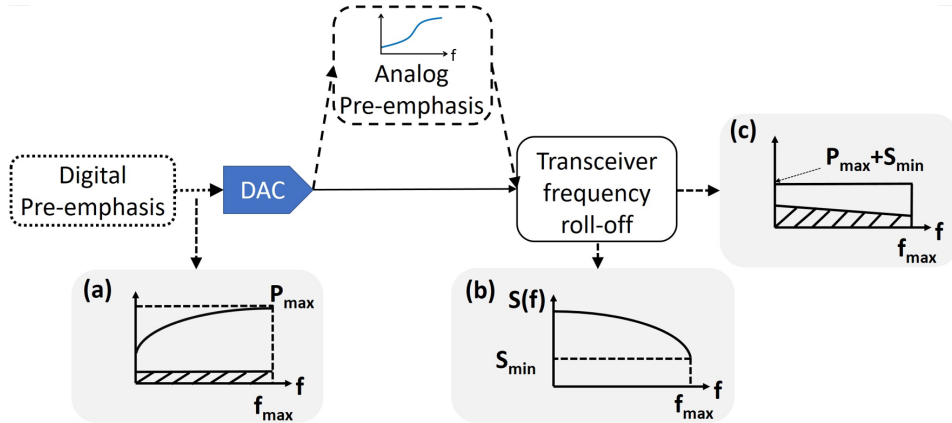


Figure 7.2: Signal chain model comparing digital pre-emphasis and analogue pre-emphasis.

When digital pre-emphasis is applied, the spectrum of the emphasized signal has higher power in its high frequency region, when compared to the low frequency region. Since the DAC has a fixed dynamic range, the low frequency components are attenuated in the digital domain, to create the emphasized signal. For example, a DAC with peak-to-peak voltage of  $V_{pp}$  can only generate a sinusoidal signal (a single frequency component) with a power of  $V_{pp}^2/R_L$ , where  $R_L$  is the load resistance. This maximal achievable power is represented as  $P_{max}$  in Figure 7.2(a). Thus, a

full equalization of the system frequency roll-off requires attenuating the power of the low frequency component by  $S_{min}$  dB, leading to an SNR degradation, as shown in Figure 7.2(c). The achievable SNR at frequency component  $f$  is

$$SNR(f) = 6.02\eta + 1.76 + S_{min} - S(f) \quad (7.3)$$

In contrast, by implementing analogue pre-emphasis, the system response becomes more uniform. This corresponds to a smaller value of  $S_{min} - S(f)$  that improves the SNR. With ideal compensation,  $S_{min} - S(f)$  becomes zero across the whole signal frequency region, (7.3) becomes (7.2), achieving the highest SNR possible using a DAC. It should be noted that smooth frequency roll-off is used to facilitate easy understanding, similar analysis can be applied for frequency response with ripples. Although the analogue pre-emphasis allows the DAC to use its full resolution across the signal frequency range, it reduces the power of the analogue output signals, due to the insertion loss of the circuit and the attenuation of the low frequency components. Hence, a higher gain amplifier is needed to drive the transmitters. In the practical signal generation, the non-flat phase response of the analogue pre-emphasis filter might introduce inter-symbol-interference that degrades the signal performance. However, in a DAC-based system, the phase response of the transceiver can be compensated without reducing the SNR.

#### 7.1.2.1 Experimental setup

The merit of the analogue pre-emphasis was investigated using an experimental setup that featured a DML, as illustrated in Figure 7.3. The DML is a low-cost discrete mode laser emitting at 1549 nm [227], with a bandwidth of 16 GHz, when biased at 95 mA, and a sharp roll-off between 16-18 GHz [228]. The DML was 50  $\Omega$  coupled to a linear RF driver (SHF100BP-ML), outputting 8 dBm driving power. The 3 dB and 6 dB RF pre-emphasis filters described in Section 7.1.1 were connected at the transmitter side to test their performance. The additional loss due to the RF pre-emphasis filters was compensated for, by increasing the output

power of the DAC. More specifically, the output peak-to-peak voltage of DAC was increased from 650 mV (without the RF filter) to 750 mV, 850 mV and 1000 mV, when the 3 dB, 6 dB and 9 dB RF filters were inserted, respectively. An RF power meter was used to ensure the same driving power to the DML.

The PAM4 symbols were generated from a pseudo-random binary sequence (PRBS) with length of 216. A root-raised-cosine (RRC) filter, with a roll-off factor of 1%, was used to generate Nyquist-shaped PAM4 digital samples. The digital samples were interpolated to 92 GigaSamples/second (GSa/s) to generate the RF signals using a DAC (33 GHz bandwidth, ENOB of about 5 bits). A linear digital pre-emphasis filter [229] was implemented to compensate for both the amplitude and phase response in the signal chain, including the frequency responses of the DAC, RF cables and amplifier, optical transmitters and the receiver. The digital pre-emphasis filter fully compensates for the frequency roll-off, from DC to the maximum DML signal bandwidth of 16 GHz. Consequently, the received signals have flat frequency spectra after detection. The impact of the DAC nominal resolution was studied by quantizing the digital samples to a limited number of levels of  $2L$ , where  $L = 5, 6$ , and  $8$  were tested.

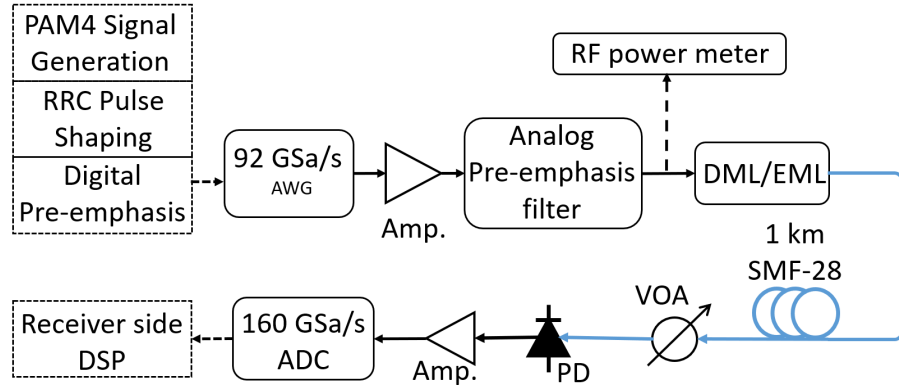


Figure 7.3: Experimental set-up for DML. RRC: root-raised-cosine, DAC: digital-to-analogue converter, ADC: analogue-to-digital converter, PD: photodiode, VOA: variable optical attenuator, DSP: digital signal processing, SMF-28: standard single-mode fiber.

At the receiver side, the optical signals were fed into a variable optical attenuator (VOA) for receiver sensitivity measurement. The signals were detected by a

40 GHz photodetector with 0.6 A/W responsivity and amplified by a 40 GHz RF power amplifier with 17 dB gain. The electrical waveforms were captured by a 63 GHz, 160 GSa/s analogue-to-digital converter (ADC). To emulate the threshold detection in a real-time PAM4 receiver, the captured samples were down-sampled to one sample per symbol for threshold detection. Post-compensation using 15-tap feedforward equalizer was also implemented to compare the performance with and without receiver-side DSP. The bit error ratio (BER) was calculated from  $1.5 \times 10^6$  bits.

The frequency responses using different analogue filters were calculated from the received samples. A 1 km SMF-28 with 0.5 dB total loss and a dispersion of 16 ps/(nm·km) was used to emulate short-reach data center interconnection. After transmission, the fiber dispersion caused frequency fading in the high frequency region (25 - 32 GHz). Due to the limited dispersion, this frequency fading acts as a low pass filtering (no dip in the spectrum). Therefore, digital pre-emphasis can be used to compensate for this effect and obtain a flat spectra.

### 7.1.3 Results and Discussion

The performance of the analogue pre-emphasis filters was tested using a DML-based transceiver. Figure 7.4 shows the comparison of the system frequency response without analogue pre-emphasis to the response observed with three different pre-emphasis levels. The red curve shows the back-to-back system frequency response without any pre-emphasis. It has a 6 dB roll-off from DC to 10 GHz and a relatively flat response up to 15 GHz before falling due to the DML's bandwidth limitation. The black, blue, and the green curves show the frequency response after connecting our 3 dB, 6 dB, and 9 dB analogue pre-emphasis filters, respectively.

It is noted that the analogue pre-emphasis filters mainly equalize the frequency roll-off at the low frequency region (DC-10 GHz, see Figure 7.1(b)). Compared to the 6 dB filter, the 3 dB filter only partially compensates for the frequency roll-off. Thus, the SNR is lower than the signal generated with the 6 dB filter. The

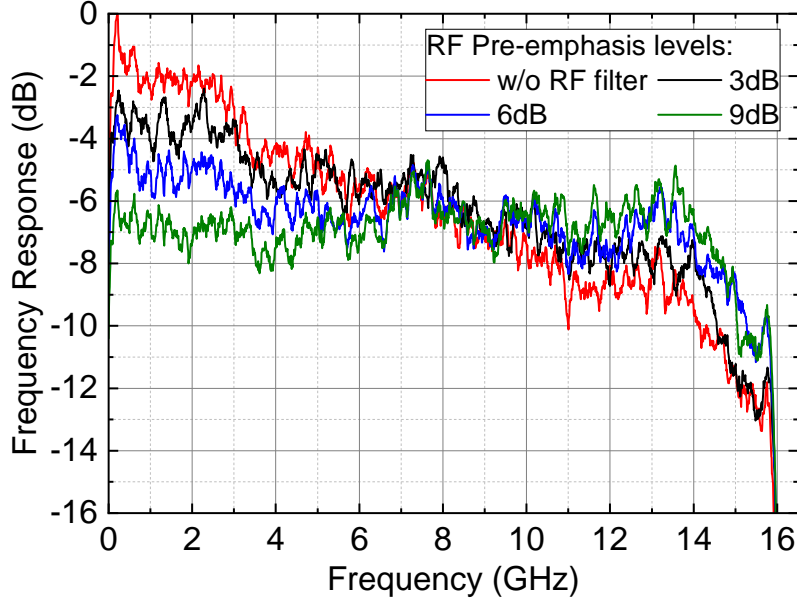


Figure 7.4: Frequency response of the 32-GBd PAM4 using RF pre-emphasis filters with different pre-emphasis levels.

9 dB pre-emphasis filter, however, over-attenuated the low frequency component and resulted in SNR degradation because the digital emphasis has to attenuate the high frequency components for a flat response. Though the 6 dB showed the best performance, it is not ideal because there still existed power fluctuation in the frequency response.

Figure 7.5 shows the measured BER of the 32 GBd (64 Gbps) PAM4 signal at different received powers at back-to-back. The red markers show BER with digital pre-emphasis only. The triangle, diamond and square markers show the BER curves using our analogue pre-emphasis filters of 3, 6, and 9 dB pre-emphasis levels, respectively. The 9 dB pre-emphasis filter was achieved by cascading the 3 dB and 6 dB filters.

Using digital pre-emphasis only, the required optical power at the HD-FEC threshold of  $3.8 \times 10^{-3}$  BER was 0.6 dBm. After implementing both the analogue and digital pre-emphasis, the receiver sensitivities were improved to -0.1, -0.6 and -0.1 dBm, with the analogue pre-emphasis levels of 3, 6 and 9 dB, respectively.

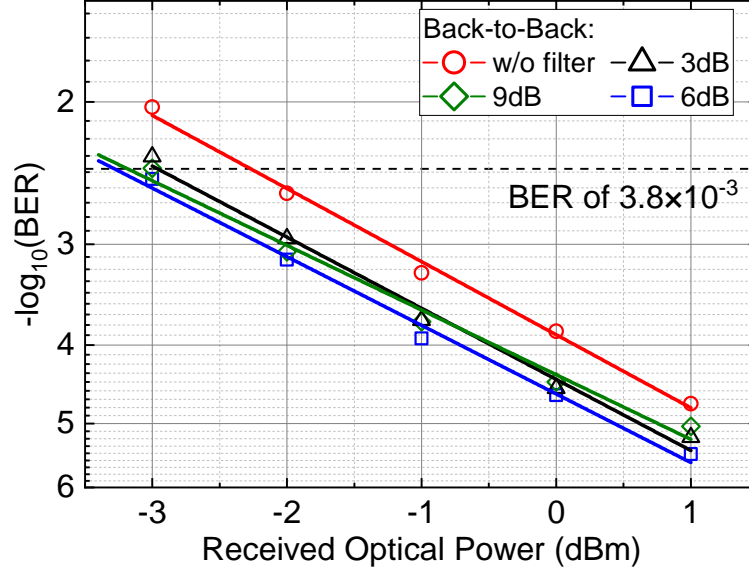


Figure 7.5: Receiver sensitivity measurements for back-to-back transmission.

The best performance was achieved using the 6 dB analogue pre-emphasis filter, which yielded 1.2 dB sensitivity improvement.

Figure 7.6 shows the receiver sensitivity after transmission over 1km SMF-28, with insets showing the eye diagrams with and without the 6 dB RF pre-emphasis filter. Due to the dispersion-induced frequency roll-off, there was a need to increase the digital pre-emphasis levels to obtain flat spectra, which consequently reduced the signal SNR; resulting in a 1.4 dB power penalty (at BER of  $3.8 \times 10^{-3}$ ), when compared to the digital pre-emphasis only results at back-to-back transmission. The receiver sensitivities were improved to 1.0 dBm, 0.4 dBm and 0.9 dBm, using the analogue pre-emphasis filters of 3 dB, 6 dB, and 9 dB, respectively. Similar to the back-to-back transmission, the 6 dB analogue pre-emphasis filter yielded the best performance, showing 1.6 dB sensitivity improvement.

The performance of the RF pre-emphasis filter at different DAC resolutions was also investigated, with the BERs measured for back-to-back transmission. As shown in Figure 7.7, a clear performance improvement is observed using the 6 dB analogue pre-emphasis filter and digital pre-emphasis, operating at the 8-bit DAC resolution, obtaining a reduced BER from  $4.6 \times 10^{-4}$  to  $1.4 \times 10^{-4}$ . Reducing the



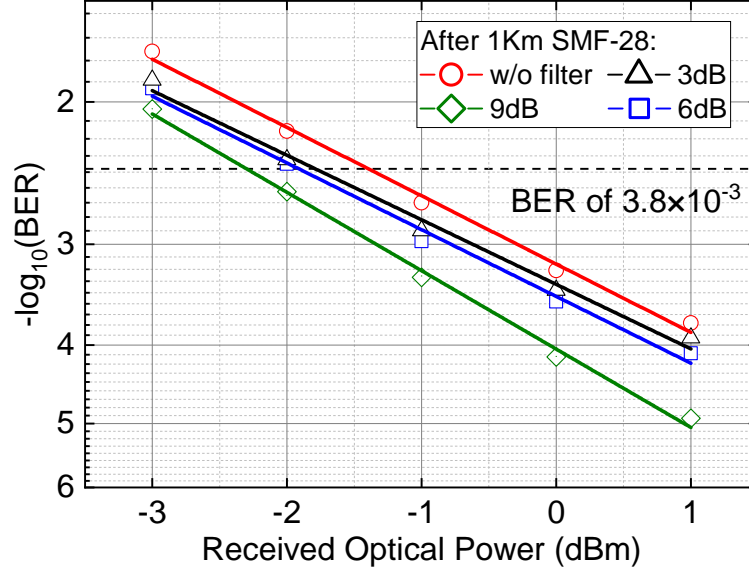


Figure 7.6: Receiver sensitivity measurements after 1-km SMF-28.

DAC resolution to 6 and 5 bits, the BERs were decreased from  $7 \times 10^{-4}$  to  $2.6 \times 10^{-4}$  and from  $1.3 \times 10^{-3}$  to  $8.5 \times 10^{-4}$ , respectively. This clearly demonstrates that the analogue pre-emphasis technique could improve the performance of transceivers using DACs of different resolutions. The transceiver performance could be further improved by using a higher order analogue pre-emphasis filter to fully compensate for the roll-off. Nevertheless, this does not undermine the conclusion that analogue pre-emphasis filter does improve the signal SNR and the receiver sensitivity.

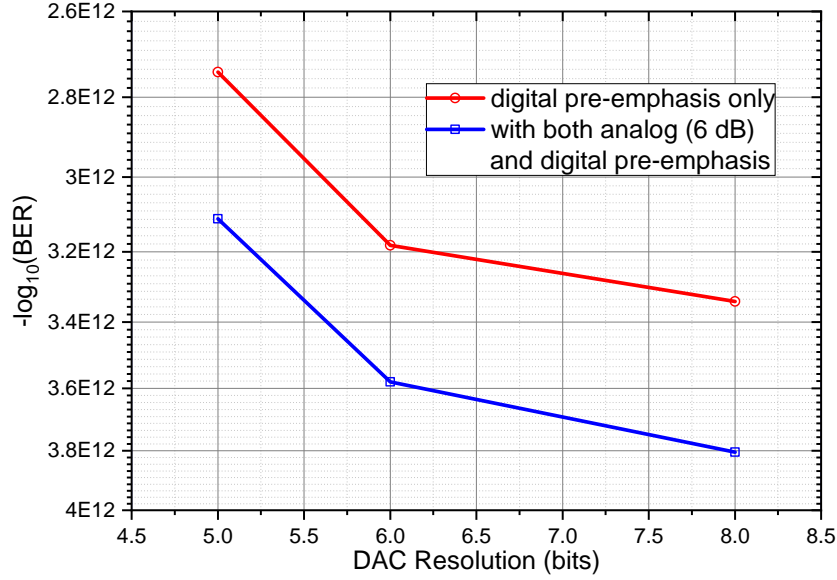


Figure 7.7: Performance improvement of using RF pre-emphasis filter using different DAC resolutions.

## 7.2 Application of Transmission Line Synthesis Techniques in Visible Light Communication Systems

Visible light communications (VLC) is an emerging technology that has become the focus of enormous attention in recent years [230–232]. VLC operates on the principle of intensity modulation and direct detection of visible wavelengths using LEDs and silicon photodetectors, respectively. VLC is one of the most promising candidates for the access network in a converged multi-technology 5G domain [233–236], where existing radio-frequency technologies such as Wi-Fi can be complemented by high-speed, low latency optical signals, due to its wide, license-free spectrum (380–780 nm), low capital expenditure and ability to provide simultaneous room illumination as well as data communications capabilities.

The main drawback to VLC, however, is the modulation bandwidth of LEDs, which is often limited to just several MHz [237]. In general, the high power LEDs used for room illumination are based on a blue-emitting GaN semiconductor with a colour converting phosphor that spreads some of the energy to yellowish wavelengths, resulting in aggregated white light illumination. There are two fundamental processes that limit the overall device bandwidths; the carrier lifetime and the  $RC$  time constant, connected to the diffusion capacitance of the diode [238]; and the slow temporal response of the colour converting phosphor [239]. Another key limitation of LEDs is their inherently non-linear electro-optic response, meaning transmitted signals must be carefully designed to avoid clipping or distortion [240].

To provide high bandwidths and subsequently, high capacity links, several methods have been proposed. These include (i) signal pre-distortion [241], (ii) post-distortion [242], (iii) amplitude equalization [225, 241], (iv) application of driver circuitry that reduces pulse decay time [243] and (v) digital equalisation [237]. Techniques (i)–(iii) aim to simply reduce the capacitance of the device, through high-pass filtering at different stages of the link. While these approaches have been demonstrated to support high transmission speeds, they are not generic and are normally designed on a trial-and-error basis. These methods are also often accompanied by a significant power penalty, as shown in Figure 5 of [244], that directly impacts gain-to-noise ratio. On the other hand, in technique (v), the residual inter-symbol interference induced by out-of-band transmission is calculated and mitigated systematically. However, high performance digital equalisers can be computationally expensive and are not always suitable for any given application.

Drawing on the concept of distributed amplification, an LED modulation-bandwidth extension technique, based on ATL synthesis, is proposed. The technique involves incorporating the LED diffusion capacitance into a  $p$ -ATL cell using series inductors and terminating with a resistor. The line has been described as a *pseudo* ATL, to reflect the origin of the concept, while also indicating the slight

difference in implementation. While the ATL was conceived to be of infinite length with each section terminated in its own image impedance, the  $p$ -ATL actually is a single-celled filter structure similar to a resistively terminated single-staged ATL. As with the ATL, the  $p$ -ATL may also be designed to exhibit significantly improved transmission and cut-off properties by applying techniques developed to enhance DA performance.

Importantly, as VLC evolves, there are numerous LED technologies emerging, such as  $\mu$ -LEDs [245], polymer LEDs (PLEDs) [246] and resonant cavity LEDs (RC-LEDs) [247], all of which have distinct characteristics. The  $p$ -ATL approach proposed in this chapter could enable bespoke driver circuits, based on the individual characteristics of the LEDs, while the combination with existing bandwidth extension schemes can lead to further improvement.

### 7.2.1 Design Concept

In Figure 7.8, a single pole simplified equivalent circuit of an LED is shown [238, 240], where  $C_d$  is the diffusion capacitance,  $R_d$  is the small signal differential resistance and  $R_s$  accounts for the series resistance from the ohmic contact and device material [248].

$$Z_{in} = R_s + \frac{R_d}{1 + j\omega R_d C_d} \quad (7.4)$$

From analysis of Figure 7.8, the input impedance  $Z_{in}$  of the LED is derived to be  $Z_{in} = R_s + \frac{R_d}{1 + j\omega R_d C_d}$ . The LED exhibits low-pass filter properties, which are reflected in its equivalent circuit. At fixed bias, a reasonable approximation of the LED bandwidth can be made from the 3 dB cut-off frequency  $f_c$  related to the  $RC$  time constant  $\tau$ , ( $\tau$  corresponds to the LED recombination time constant  $\tau_c$  [248]) as

$$f_c = \frac{1}{2\pi\tau_c} = \frac{1}{2\pi C_d R_d} \quad (7.5)$$

The similarity between the LED equivalent circuit as depicted in Figure 7.8, and the intrinsic equivalent circuit of the input of an HBT device, as shown in

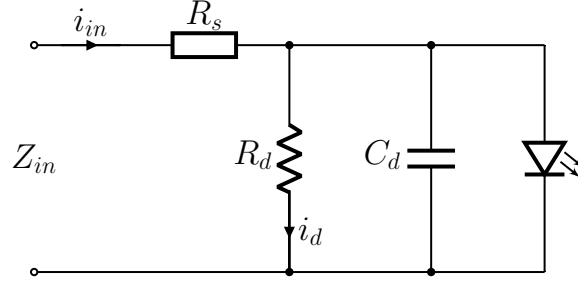
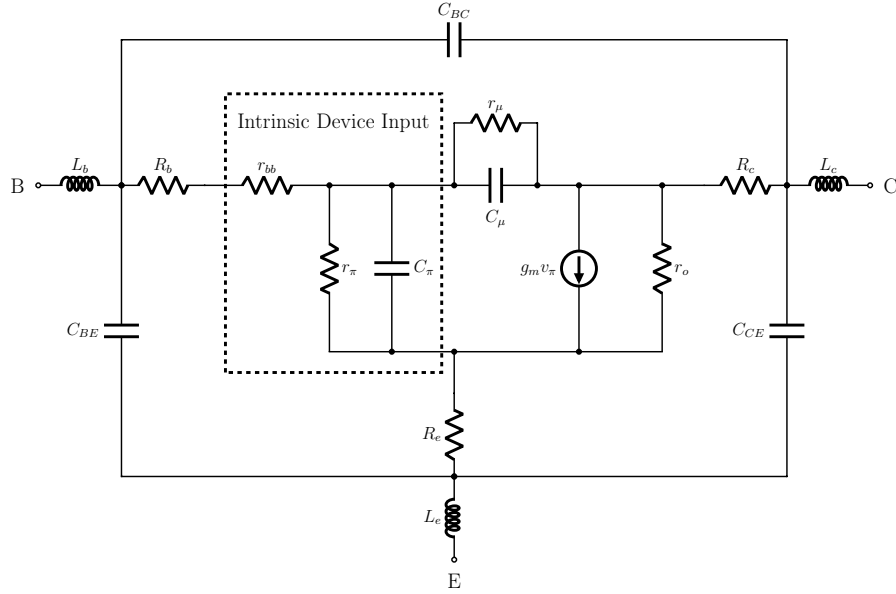


Figure 7.8: A simplified LED equivalent circuit.

Figure 7.9; may be readily observed, with  $R_s$ ,  $R_d$  and  $C_d$  of the LED corresponding to  $r_{bb}$ ,  $r_\pi$  and  $C_\pi$  of the HBT, respectively. Hence, similar to how the distributed effect on the transmission lines of SSDAs result in increased cut-off frequency and consequently bandwidth extension, it is conceivable that this same effect can be replicated for LEDs in the VLC context.


 Figure 7.9: HBT hybrid- $\pi$  model equivalent circuit with dashed lines around the input in common emitter configuration.

The shunt capacitance  $C_d$  may be incorporated into a  $p$ -ATL cell, using series inductance, with the aim of distributing the effect of the shunt capacitance more uniformly and across a wider passband. The design of the  $p$ -ATL cell follows the

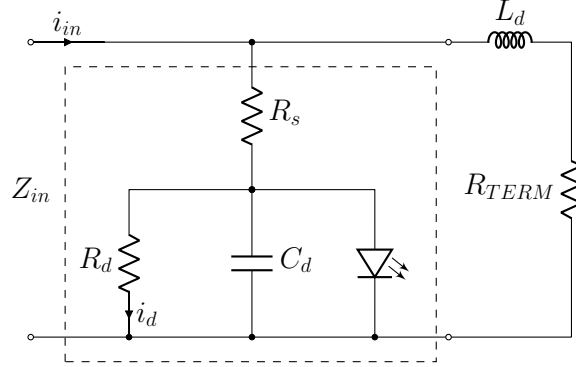


Figure 7.10: Simplified LED equivalent circuit  $C_d$  incorporated into a  $p$ -ATL cell. Dashed lines surround the equivalent LED circuit.

design of the input and output transmission lines of a SSDA [187, 249, 250], based on the image impedance filter design method [32, 189].

To achieve the desired distributed capacitance effect, an inductance  $L_d$  is introduced at the input terminal of the LED (as shown in Figure 7.10), based on the image impedance ( $Z_o$ ) relation for a lossless ATL, which is given by

$$Z_o = \sqrt{\frac{L}{C} \left( 1 - \frac{\omega^2 LC}{4} \right)} \quad (7.6)$$

with the cut-off frequency of the ATL ( $f_{c-ATL}$ ) given by:

$$f_{c-ATL} = \frac{\omega_c}{2\pi} = \frac{1}{\pi\sqrt{LC}} \quad (7.7)$$

where  $L$  represents the series inductance required to achieve a distributed effect,  $C$  is the shunt capacitance (which in this case corresponds to the LED diffusion capacitance  $C_d$ ),  $\omega$  is the angular frequency and  $\omega_c$  is the angular cut-off frequency [28, 50]. From (7.6), the value of  $L$  is conventionally chosen as the product of  $C$  and the square of the DC value of  $Z_o$  [28]. The terminating resistance  $R_{TERM}$  is conventionally chosen as the DC value of  $Z_o$  to achieve a broadband match.

It may be observed from Figure 7.10 that a current divider circuit is formed between the LED and the sum of  $R_{TERM}$  and the reactance of  $L_d$ , which reduces the effective LED drive current. Hence, as  $R_d$  and  $C_d$  are dependent on bias, the

ATL needs to be designed at the parameters corresponding to the effective LED drive current.

However, for the proposed application, the lossless assumption commonly adopted in ATL synthesis is invalid due to the presence of  $R_d$  and  $R_s$ . Furthermore, the parallel combination of  $(R_d + R_s)$  and  $R_{TERM}$  also impacts  $Z_o$ , such that  $R_{TERM}$  does not provide an image-impedance match, even at very low frequencies.

The input impedance of the LED with distributed input  $Z_{in}^*$ , as shown in Figure 7.10 is derived as

$$Z_{in}^* = \left( R_s + \frac{R_d}{1 + j\omega R_d C_d} \right) \parallel (j\omega L_d + R_{TERM}) \quad (7.8)$$

which on expansion becomes (7.9).

$$Z_{in}^* = \frac{R_{TERM}(R_s + R_d) + j\omega(R_s R_d R_{TERM} C_d + L_d(R_s + R_d)) - \omega^2 R_s R_d L_d C_d}{R_{TERM}(R_s + R_d) + j\omega(L_d + R_s R_d C_d + R_d R_{TERM} C_d) - \omega^2 R_d C_d L_d} \quad (7.9)$$

There are two main observations from (7.8): firstly, the frequency response and cut-off behaviour of the LED is no longer solely dependent on the  $RC$  time constant of the LED, such that by appropriate choice of the p-ATL impedance  $Z_o$  (with corresponding values of  $L_d$  and  $R_{TERM}$ ), significant bandwidth improvement may be achieved. The second observation is that at DC,  $Z_{in}^* = (R_s + R_d) \parallel R_{TERM}$ , which is lower than  $Z_{in}$  in (7.4); such that while there is a gain in bandwidth, there is an associated loss in impedance magnitude.

The effect of the sacrifice of impedance magnitude for wider bandwidth on a VLC system would be a reduction in the optical power and output light intensity of the LED, such that while the modulation bandwidth improves, the power-bandwidth product does not improve commensurately. However, trading optical power for bandwidth is hardly a demerit in VLC, as these systems generally have low overall power consumption and high optical power outputs [248]. Moreover, considering Shannon's capacity equation  $C = B \log_2(1 + \text{SNR})$ , it may be observed that while capacity increases linearly with increasing bandwidth, it only increases

with the logarithm of SNR [251]. Hence, the gain-bandwidth trade-off is beneficial insofar as the decrease in power output is not sufficiently large as to limit improvement in overall capacity.

### 7.2.2 Performance Assessment

To illustrate the effect of the  $p$ -ATL input technique so far described, Figure 7.11 compares the input impedance of an LED with two cases in which the proposed technique is applied:  $Z_o = Z_{in}$ , and  $Z_o = Z_{in}/2$ , assuming equal effective current drive LED parameters.

LED equivalent model parameters derived and verified in [238] are employed. These parameters are presented in Table 7.2, where  $m$  is the average ideality factor obtained from the LED low frequency impedance model

$$|Z_{in}| = R_s + R_d = R_s + \frac{mV_T}{I_b} \quad (7.10)$$

The values derived at 2 mA drive current selected for this study.

Table 7.2: LED parameters at various drive currents [238].

I <sub>b</sub> (mA)	$R_s(\Omega)$	$R_d(\Omega)$	$C_d(\text{nF})$	$\tau_c(\text{ns})$	$m$
1	1.6	28.4	0.342	9.7	1.09
2	1.6	14.4	0.59	8.5	1.11
5	1.6	6.0	1.33	8.0	1.15
10	1.6	3.0	2.67	8.0	1.15

As reported in [238], the LED equivalent circuit model on its own has a predicted and verified 3 db cut-off frequency of 18.7 MHz. In the first case, where the distributed transmission line is designed at  $Z_o = Z_{in}$ , a threefold improvement in bandwidth is predicted, while the input impedance reduces by 50%; this agrees with (7.8). In the second case (i.e.  $Z_o = Z_{in}/2$ ), there is a further improvement in bandwidth of 65%, which translates to nearly 400% overall improvement in input impedance bandwidth, compared to the LED performance, at 66.7% overall loss in impedance magnitude.



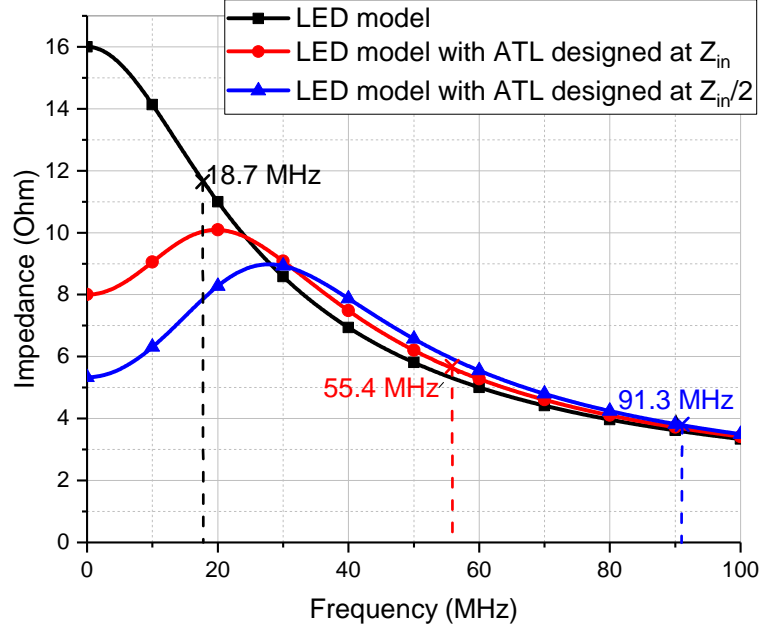


Figure 7.11: Comparison of input impedance magnitude with the 3 dB bandwidth annotated.

To further demonstrate the utility of the proposed concept, the response of the LED with the two application cases of the proposed technique as previously described (i.e.  $Z_o = Z_{in}$ , and  $Z_o = Z_{in}/2$ ) is compared to a 100 MHz modulating current. Again, the LED equivalent circuit parameters at 2 mA presented in [238] are adopted. Towards minimising the peaking effect observed in Figure 7.11, the distributing inductance is also reduced to  $L_d/2$  in both application cases. Results of this comparison is presented in Figure 7.12, where it is seen that the current  $i_d$  closely follows the profile of  $Z_{in}$  in both cases where the distributing inductance is kept at  $L_d$ . In the cases in which distributing inductance of  $L_d/2$  is used, a flatter gain profile can also be observed.

As can be inferred from the foregoing discussion, the proposed technique requires reasonably accurate equivalent circuit parameters. A popular approach to extracting these parameters is described in [238], following which approximate values for  $R_s$ ,  $R_d$  and  $C_d$  can be extracted from S-parameters measurement under bias conditions corresponding to the effective LED drive currents. Before measurement, the network analyser is calibrated with a load that is close to the impedance of the

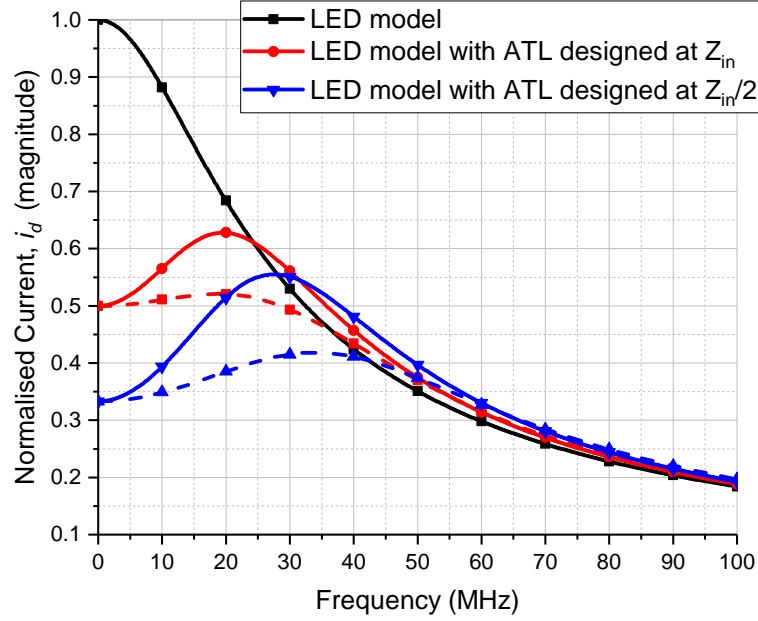


Figure 7.12: Comparison of normalised current  $i_d$  through the LED (dashed lines for inductance at  $L_d/2$  to reduce peaking).

device under test (DUT), as this tends to yield more accurate results [238]. Due to the relatively low input impedance of communication LEDs, the load resistance used for calibration would usually be a value other than the conventional  $50 \Omega$  load [238, 252]. Thereafter, an iterative curve fitting process is adopted to arrive at an even closer match between the measured and modelled frequency responses.

However, experiments show that while the LED equivalent circuit correctly represents the frequency response of the device, unlike transistor equivalent models, it does not represent the LEDs behaviour in a circuit. A model that both describes the independent behaviour of the LED and also its behaviour in circuit is required to verify the proposed technique. Ideally, this model will incorporate both linear and non-linear recombination techniques and account for the bandwidth limiting effect arising from the carrier mobility of the device.

### 7.3 Conclusions

In this chapter, the application of artificial transmission line synthesis in the contexts of optical and visible light communications has been described. In the first context, analogue pre-emphasis based on  $m$ -derived filters is used to compensate for the frequency roll-off in a bandwidth-limited transceiver. Compared to digital pre-emphasis only, we obtained clear performance improvement by combining both analogue and digital pre-emphasis techniques. The simple RF circuit design has low insertion loss and can be integrated with transceiver modules. Even with un-optimized design, a 1.1 dB sensitivity improvement was obtained for DML-based 32 GBd (64 Gbps) PAM4 after transmission over 1 km SMF-28.

In the context of VLC, an LED-bandwidth extension approach based on transmission line synthesis has been described and verified using an LED small signal equivalent circuit model. The proposed technique involves incorporating the bandwidth limiting diffusion (shunt) capacitance of the LED into a  $p$ -ATL cell with series inductance and terminating with a resistor, based on the image impedance filter design method. The  $p$ -ATL can be designed for significantly improved cut-off, with 400% improvement presented in this chapter, from studies based on a verified LED equivalent circuit model. An added merit is the potential for achieving a flatter frequency response profile, which correlates to a more uniform group delay and less signal distortion. It is expected that the proposed approach will enable bespoke driver circuits, based on the individual characteristics of LEDs, while combination with existing bandwidth extension schemes can link to further improvement. For the purpose of describing the concept, the focus has been placed on the case of a single LED, based on the conventional design. It is envisaged that the technique can be adapted for an array of LEDs, with the techniques described in Chapter 4 applied for further bandwidth extension.

# Chapter 8

## Concluding remarks

### 8.1 Summary and Discussion

The research reported in this thesis has explored the application of novel circuit synthesis techniques and topologies to the design of HBT-based DAs with a view to improving gain and bandwidth performance. Particular attention has been given to the SSDA and SSDA-based topologies, due to the record performances reported for HBT DAs based on this topology. This study has resulted in the development of bandwidth extension techniques that offer significant improvement over current methods and a new DA topology - the M-SSDA - which offers similar performance to the C-SSDA, but with reduced circuit footprint and potential for better noise performance. Reports on the design and measurement of two MMIC amplifiers, a SSDA that features the bandwidth extension techniques developed and an M-SSDA, have been presented. The application of concepts from distributed amplification to improving the bandwidth of optical and visible light communication systems has also been set out and verified in this thesis.

The first two chapters presented a general introduction to the subject of distributed amplification and gave a background to the work presented in this thesis. Chapter 1 described the motivation for the study, set an outline for the thesis and presents what has been the contribution of this study to knowledge. The concept of distributed amplification was presented in Chapter 2. The primary elements of the DA and commonly adopted circuit modifications to improve performance were also described. Also presented in this chapter is a comparison of bipolar and

field-effect based DAs, as well as performance summaries of the state-of-the-art DAs based on MESFET/HEMTs, HBTs, CMOS and BiCMOS processes.

In Chapter 3, a comprehensive review of reported HBT DAs circuits was presented. This chapter highlighted the effect that improved process fabrication techniques have had on improving figures of merit of the HBT DA. The chapter also highlighted the significance of novel transmission line synthesis techniques and circuit topologies in achieving better device performance. A section was also committed to discussing analytical reports modelling such parameters as the gain, bandwidth and noise performance of the amplifier. The apparent suitability of HBTs in SSDAs and SSDA derivatives was observed in this review, prompting further study. Justification for the apparent suitability of HBTs for SSDA implementation was considered. It was established that the SSDA topology maximises the high gain and better linearity merits of the HBT, while limiting the adverse effect arising from its resistive input nature. Also included in Chapter 3 is a description of the HBT process used in the majority of the practical implementations considered in this thesis - Teledyne's TSC250; and the process of extracting small-signal parameters from the foundry model supplied by the device manufacturer. The accuracy of the extracted small-signal model was verified by comparing S-parameter performance of both the foundry large-signal model and the extracted equivalent model in a basic common-emitter amplifier mode.

In Chapter 4, a set of modifications to improve the bandwidth performance of the HBT SSDA was presented, supported by full foundry model-based simulation results. This approach to bandwidth improvement builds on the peculiarities of the SSDA topology, which makes its transmission lines more tolerable to sub-optimal modifications with limited effect on the distributed effect necessary for wideband performance. The three-stepped technique described involves scaling down the inductance on the input ATL; creating a high frequency resonance peak, by the addition of shunt capacitance on the input ATL; and compensating for the resulting increased reflection with adapted negative resistance attenuation compensation

techniques. Based on these modifications, an SSDA with a bandwidth of 345 GHz at 8 dB gain was demonstrated in simulation. This represents close to 50% improvement in bandwidth performance over the state of the art reported in [17]. The SSDA MMIC was fabricated by Teledyne, and on measurement, showed a gain of 7.1 dB at 200 GHz bandwidth, representing a significant shortfall of 11% and 42% in gain and bandwidth, respectively, from simulation results.

A new amplifier topology, the M-SSDA, was introduced in Chapter 5. It is a functional relative of the C-SSDA, as they share a similar gain mechanism, in that they are both fully multiplicative DAs. The presence of a shared intermediate transmission line connecting the tiers of the M-SSDA makes it possible to achieve more compactness and smaller circuit footprint. The topology also affords the potential for lower attenuative losses and better noise performance from the optimisation of the intermediate transmission lines. A two-tier M-SSDA based on common-emitter gain cells was presented to demonstrate the viability of the proposed design. The S-parameter performance of the proposed circuit is compared with that of a C-SSDA with two gain cells to show the similarity in their gain and bandwidth performance. A  $3 \times 1$  M-SSDA circuit with a predicted gain of 20 dB at 324 GHz bandwidth based on full foundry process model was demonstrated in simulation. The measured result from the fabricated M-SSDA MMIC showed a gain of 12 dB at 170 GHz bandwidth.

Chapter 6 presented a study of the noise performance of the SSDA and its derivative multiplicative DA, to allow for a more complete appraisal of this family of DAs. New equations that describe the noise figure, the noise voltage spectral density (NVSD) at the output and equivalent input noise current spectral density (EINCSD) of the multiplicative DA were derived and verified. It was established that unlike in multi-stage DAs, where noise figure reduces with additional stages, the noise figure and EINCSD of multiplicative DAs increase with each added gain-cell tier. However, the noise contribution from an additional stage is only a fraction of the contribution of the stage before it, in agreement with the principle of noise

scaling in cascaded systems. Based on the analytical study, design approaches to balance the trade-off between the gain and noise performance were also discussed. A significant observation pointed out in this chapter was that while the noise figure of the multiplicative DA does indeed increase quadratically with additional stages; this trend is offset by the gain, which increases at an exponential rate, progressively increasing the margin between amplification and added noise. These considerations, in addition to the limitations of the multi-stage DAs in ultra high frequency designs, lends justification to the adoption of the SSDA and its multiplicative derivatives.

In Chapter 7, the application of transmission line synthesis techniques to improve bandwidth performance in the contexts of optical and visible light communications was described. A high-pass filter based on the  $T$ -half filter section was designed to achieve pre-emphasis equalisation and extend the bandwidth of optical transceiver systems. The strength of the technique lies in the simplicity and cost-effectiveness of the filter implementation, which makes it easy to customise the equaliser to match various transceiver frequency response profiles. Compared to the application of digital pre-emphasis only, a clear performance improvement was obtained when both analogue and digital pre-emphasis were combined. Though the experiments only investigated short-reach, intensity-modulated direct-detection transceivers, analyses indicate that the analogue pre-emphasis filter can improve SNR of any DAC-based transceiver with inherent frequency roll-off. Therefore, it is expected, that the technique will lead to performance improvement in coherent transceivers. The simple RF circuit design has low insertion loss and can be integrated with transceiver modules. A bandwidth extension technique based on the absorption of the bandwidth limiting capacitance of LEDs into a pseudo-artificial transmission line for visible light communication was also presented and verified using an LED equivalent model.

As advancement in device scaling continue to drive transistor technology towards the absolute physical limit, with the operational capability of solid state

devices now extending into the lower end of the THz frequency band, associated old and familiar circuit design challenges also evolve in their complexity and the limitations they impose. This thesis has sought to provide an answer to the question of how to achieve the widest possible bandwidth from these and the next generation of ultra-high speed process. As is often the case, solutions to complex challenges must start by an attempt at simplification, which essentially is the approach that this thesis has followed in re-examining the merit of the SSDA. In its simplicity, the SSDA provides a basic building block that can be modified and stacked to fit varying requirements. Following this, the multiplicative matrix SSDA has been introduced, which addresses the main limitation of the SSDA - gain. Furthermore, by studying the noise performance of the SSDA and its multiplicative derivative, the thesis provides a complete picture by which performance merits can be assessed and trade-offs considered.

## 8.2 Future Work

The research project that has resulted in this thesis has addressed a limited number of issues, raising new questions worthy of future investigation

- **Developing accurate transistor models beyond 100 GHz:** The discrepancy between the measured and simulated S-parameters demonstrates the challenge of modelling ultra-wideband circuits, especially towards the higher end of the frequency range; warranting further investigation. Even with the benefit of hindsight, which informed the inclusion of additional parasitic components, the response from post-measurement simulations still showed significant deviation from the measured response. It may be the case that the unexpected performance shortfalls are results of unforeseen design faults or the effects of electromagnetic coupling between the various MMIC components, despite best efforts to avoid these at the design and layout stage.



- **More fabrications and testing:** In Chapter 4, an inductive peaked cascode SSDA is presented with full foundry simulation and layout prepared for MMIC fabrication. However, due to the limited wafer space available, this as well as a two-tier M-SSDA presented in Chapter 5 could not be fabricated at the time. Fabricating both the SSDA with the bandwidth extension techniques introduced in this thesis, and the fairly standard inductive peaked cascode technique on the same wafer, would make it possible to have a proper comparison of the effectiveness of the two techniques under similar fabrication constraints. The fabrication and measurement result of the two-tier M-SSDA would also provide further insights into the design considerations of the M-SSDA, especially regarding the effect of the intermediate line reflections on overall gain performance.
- **Performance evaluation for other relevant figures of merit for SSDA and M-SSDA:** While the gain and noise performance of multiplicative DAs have been explored in this thesis, other figures of merit such as the group delay and dynamic range, which are also important performance requirements for preamplifier application, have not been addressed. Hence, it will be quite useful to investigate these, both in the particular context of HBTs, in line with the research presented in this thesis and also in the general context. Possible approaches to the evaluation of the group delay is by utilising the phase associated with the transfer function expressions presented in this thesis or by extraction from the S-parameter measurements using the Touchstone (.s2p) data holder functionality of Keysight's ADS.
- **Implementation of SSDA and M-SSDA using CMOS active device and RFE integration:** While the research reported in this thesis has focused the application of HBTs as the active device, the techniques reported are not limited to HBTs. It would be interesting to analyse and design MMICs using HEMTs and CMOS technologies that feature the bandwidth optimisation techniques described. It would be particularly valuable to ex-

plore RFE integration of photodetectors with CMOS based distributed transimpedance amplifier, due to the cost effectiveness of CMOS and recent advances that have resulted in record-high bandwidth beyond 100 GHz for high-speed photodetectors compatible CMOS fabrication standards [253–255].

- **Application of bandwidth extension technique and the M-SSDA in active equalization:** The development of active equalization using the distributed transversal filter (DTF) concept, to achieve tunable pre-emphasis magnitude and frequency response profile. Apart from providing more latitude for performance optimisation, with sufficient number of taps, a DTF will be ideal for equalising transceivers with uneven frequency response characteristics. A particularly interesting area of application would be in equalising the response of lasers, which have roll-off at both high and low frequencies, when operated at high currents for optimal speed. It will also be worth exploring the application of the matrix amplifier and the M-SSDA in transversal filtering.
- **Practical implementation of  $p$ -ATL in a VLC system:** This thesis has only described the concept of the  $p$ -ATL and predicted potential performance improvement based on simulation tests. Research towards practically implementing this technique will be of interest. It will also be of interest, to see the effect of the proposed circuit modifications on group delay and signal distortion.

The research presented in this thesis has been concerned with the analysis and design of ultra-wideband distributed circuits, exploring design considerations that would result, particularly, in bandwidth performance improvement. This has led to the development of new bandwidth extension techniques based on the SSDA, that optimise the performance of ultra-fast MMIC processes. The MMIC amplifier designed and fabricated featuring this techniques achieved a record bandwidth of 200 GHz for the SSDA, with a gain of 7.1 dB. A new multiplicative amplifier

topology, the M-SSDA, has also been developed and a three-tier amplifier fabricated based on this topology. The application of concepts that could be considered native to distributed amplification, towards performance improvement in optical communication and VLC have also been explored. A number of original contributions have also been made, with six papers published. It is hoped that the analysis and techniques presented in this thesis will find application in the design of amplifiers and communication systems suitable for next generation high-speed analogue and digital requirement.

# Appendix A

## Alternative Approach to EINCSD Derivation

The approach adopted by Freundorfer and Nguyen (1996) [176], in deriving the EINCSD for the multistage DA, had been initially followed to arrive at an expression for the multiplicative DA. While essentially accurate, this technique resulted in equations that were not as tractable as the method adopted by Iqbal and Darwazeh (1999) [170]. Hence, the approach presented in [170] has been followed for the EINCSD derivations in this thesis, and this has been included in Chapter 6. However, the derivation of the EINCSD for the SSDA based on this approach, has been included as an appendix for completeness.

### A.1 EINCSD for SSDA

Following the noise analysis method adopted by Aitchison in [175], Freundorfer and Nguyen (1996) obtained an expression for the EINCSD of the MESFET distributed preamplifier [176]; the differences being that a current source input was substituted for the  $50\ \Omega$  matched system adopted in [175] and the inclusion of correlation between the noise sources.

$$i_d * i_g = j\sqrt{|i_d|^2|i_g|^2} = j4kT_o\omega C_{gs}\sqrt{RP} \quad (\text{A.1})$$

where  $R$  and  $P$  are noise parameters of the transistor [176, 256].

To arrive at the desired expression, the overall noise contribution is broken into constituent independent noise power densities:

- equivalent input noise power density from the gate termination  $Z_{\pi g}$  given by

$$|i_{n1}|^2 = \frac{|i_{z\pi g}|^2}{4} \left| 1 + \frac{Z_r}{Z_f} e^{jN\phi} \right|^2 \quad (\text{A.2})$$

- equivalent input noise power density from the drain termination  $Z_{\pi d}$  given by

$$|i_{n2}|^2 = \frac{|i_{z\pi d}|^2}{4} \left| \frac{Z_{\pi d}}{Z_f} \right|^2 \quad (\text{A.3})$$

- and equivalent input noise power density of all FETs in the N stages, given by

$$\begin{aligned} |i_{n3}|^2 = & \frac{|i_g|^2}{4} \sum_{r=1}^n (A(r, \phi)^2 + B(r, \phi)^2) + \frac{|i_d|^2}{4} \left| \frac{Z_{\pi d}}{Z_f} \right|^2 n \\ & + \frac{1}{2} \sum_{r=1}^n \text{Re} \left[ i_g i_d^* \frac{Z_{\pi d}^*}{Z_f^*} (A(r, \phi) + jB(r, \phi)) e^{j(n-2r+1)\phi} \right] \end{aligned} \quad (\text{A.4})$$

the summation of which gives the total noise power density [176]. The equivalent current noise density at the input is derived by dividing the output voltage noise density by the transimpedance gain of the preamplifier. The total EINCSD is the sum of the contribution of the individual noise current densities

$$|i_n| = \sqrt{|i_{n1}|^2 + |i_{n2}|^2 + |i_{n3}|^2} \quad (\text{A.5})$$

$$\begin{aligned} = & \sqrt{\frac{|i_{z\pi g}|^2}{4} \left| 1 + \frac{Z_r}{Z_f} e^{jn\phi} \right|^2 + \frac{|i_{z\pi d}|^2}{4} \left| \frac{Z_{\pi d}}{Z_f} \right|^2} \\ & + \frac{|i_g|^2}{4} \sum_{r=1}^n (A(r, \phi)^2 + B(r, \phi)^2) + \frac{|i_d|^2}{4} \left| \frac{Z_{\pi d}}{Z_f} \right|^2 n \\ & + \frac{1}{2} \sum_{r=1}^n \text{Re} \left[ i_g i_d^* \frac{Z_{\pi d}^*}{Z_f^*} (A(r, \phi) + jB(r, \phi)) e^{j(n-2r+1)\phi} \right] \end{aligned} \quad (\text{A.6})$$

where

$$|i_{z\pi g}|^2 = \frac{4kT_0}{Z_{\pi g}} \quad (\text{A.7})$$

$$|i_{Z\pi d}|^2 = \frac{4kT_0}{Z_{\pi d}} \quad (\text{A.8})$$

The forward transimpedance gain,

$$Z_f = -\frac{n}{2}g_m Z_{\pi g} Z_{\pi d} e^{-jn\phi} \quad (\text{A.9})$$

The transimpedance gain at the output terminating resistance,

$$Z_r = -\frac{1}{2}g_m Z_{\pi g} Z_{\pi d} \frac{\sin(n\phi)}{\sin \phi} e^{-jn\phi} \quad (\text{A.10})$$

$$A(r, \phi) = 1 + \frac{(n-r+1)}{n} \cos(2r-1)\phi + \frac{\sin(r-1)\phi}{n \sin \phi} \cos(r-1)\phi \quad (\text{A.11})$$

$$B(r, \phi) = \frac{(n-r+1)}{n} \sin(2r-1)\phi + \frac{\sin(r-1)\phi}{n \sin \phi} \sin(r-1)\phi \quad (\text{A.12})$$

$$\phi = \omega \sqrt{L_g C_{gs}} \quad (\text{A.13})$$

For the SSDA,

$$Z_f = Z_r = -\frac{1}{2}g_m Z_{\pi g} Z_{\pi d} e^{-j\phi} \quad (\text{A.14})$$

$$A(r, \phi) = 1 + \cos \phi \quad (\text{A.15})$$

$$B(r, \phi) = \sin \phi \quad (\text{A.16})$$

which simplifies (A.6) to

$$|i_{FET}| = \sqrt{\frac{|i_{Z\pi_g}|^2}{4} |1 + e^{j\phi}|^2 + \frac{|i_{Z\pi_d}|^2}{4} \left| \frac{Z_{\pi_d}}{Z_f} \right|^2 + \frac{|i_g|^2}{2} (1 + \cos \phi) + \frac{|i_d|^2}{4} \left| \frac{Z_{\pi_d}}{Z_f} \right|^2 + \frac{1}{2} \text{Re} \left[ i_g i_d^* \frac{Z_{\pi_d}^*}{Z_f^*} (1 + \cos \phi + \sin \phi) \right]} \quad (\text{A.17})$$

Following A.17, the derivation of an equation describing the EINCSD of an HBT-based SSDA based on the intrinsic equivalent circuit in Figure 6.3 involves replacing the noise contributors with their HBT-based SSDA equivalents as thus

$$|i_{HBT}| = \sqrt{\frac{|i_{Z\pi_b}|^2}{4} |1 + e^{j\rho}|^2 + \frac{|i_{Z\pi_c}|^2}{4} \left| \frac{Z_{\pi_c}}{Z_f} \right|^2 + \frac{|i_b|^2}{2} (1 + \cos \rho) + \frac{|i_c|^2}{4} \left| \frac{Z_{\pi_c}}{Z_f} \right|^2 + \frac{1}{2} \text{Re} \left[ i_g i_c^* \frac{Z_{\pi_c}^*}{Z_f^*} (1 + \cos \rho + \sin \rho) \right]} \quad (\text{A.18})$$

with

$$\rho = \omega \sqrt{L_B C_\pi} \quad (\text{A.19})$$

Tian, Freundorfer and Roy (2003) derived an EINCSD expression based on a common-collector-cascode (CCC) DA HBT preamplifier [172], which helps to verify the validity of this position. In [172], the noise model of the HBT CCC gain cell was transformed into a noiseless two-port network with two correlated voltage and current noise generators ( $e_{nc}$  and  $i_{nc}$ , respectively) connected at its input. The derivation of noise sources  $e_{nc}$  and  $i_{nc}$  was then carried out analytically following

the Van der Ziel's noise network theory.

$$|i_n| = \sqrt{\begin{aligned} & \frac{|i_{Z\pi b}|^2}{4} \left| 1 + \frac{\sin n\rho}{n \sin \rho} e^{jn\rho} \right|^2 + \frac{|i_{Z\pi c}|^2}{4} \left| \frac{Z_{\pi c}}{Z_f} \right|^2 \\ & + \frac{|i_{nc}|^2}{4} \sum_{r=1}^n |C(r, \rho)|^2 + \frac{|e_{nc}|^2}{n} \left| \frac{1}{Z_{\pi b}} \right|^2 \\ & + \frac{1}{2} \sum_{r=1}^n \text{Re} \left[ i_{nc} e_{nc}^* \left( -\frac{2}{n Z_{\pi b}} \right)^* C(r, \rho) e^{j(-2r+1)\rho} \right] \end{aligned}} \quad (\text{A.20})$$

where

$$|i_{z\pi b}|^2 = \frac{4kt}{Z_{\pi b}} \quad (\text{A.21})$$

$$|i_{z\pi c}|^2 = \frac{4kt}{Z_{\pi c}} \quad (\text{A.22})$$

$$C(r, \rho) = 1 + \frac{n-r+1}{n} e^{j(2r-1)\rho} + \frac{\sin(r-1)\rho}{n \sin \rho} e^{j(r-1)\rho} \quad (\text{A.23})$$

$$\begin{aligned} \overline{i_{nc}^2} = A_1 & \left\{ \begin{aligned} & \overline{i_{11}^2} |g_{m1} R_{e1}|^2 + \overline{i_{12}^2} |Y_{\pi 1} R_{e1}|^2 \\ & + \overline{i_{21}^2} |(R_{e1} + r_{b2} + R_{e2}) Y_{\pi 1}|^2 \\ & + (\overline{e_{e1}^2} + \overline{e_{b2}^2} + \overline{e_{e2}^2}) |Y_{\pi 1}|^2 \end{aligned} \right\} \\ & + \left| \frac{1}{g_{m2} g_{m3} (Y_{\pi 1} + g_{m1}) R_{e1}} \right|^2 \left\{ \begin{aligned} & \overline{i_{22}^2} |(g_{m3} Y_{\pi 1}) [Y_{\pi 2} (R_{e1} + R_{e2}) \\ & + (Y_{\pi 2} r_{b2} + 1)]|^2 \\ & + \overline{i_{31}^2} |g_{m3} C_1|^2 + \overline{i_{32}^2} |Y_{\pi 3} C_1|^2 \end{aligned} \right\} \quad (\text{A.24}) \end{aligned}$$



$$\begin{aligned} \overline{e_{nc}^2} = A_1 & \left\{ \begin{aligned} & \overline{i_{11}^2} |R_{e1}(1 - r_{b1}g_{m1})|^2 + \overline{i_{12}^2} |R_{e1}(Y_{\pi1}r_{b1} + 1)|^2 \\ & + \overline{i_{21}^2} |A_0(r_{b2} + R_{e2}) + R_{e1}(Y_{\pi1}r_{b1} + 1)|^2 \\ & + \overline{e_{b1}^2} |(Y_{\pi1} + g_{m1})R_{e1}|^2 \\ & + \overline{e_{e1}^2} |Y_{\pi1}r_{b1} + 1|^2 + (\overline{e_{b2}^2} + \overline{e_{e2}^2}) |A_0|^2 \end{aligned} \right\} \\ & + \left| \frac{1}{g_{m2}g_{m3}(Y_{\pi1} + g_{m1})R_{e1}} \right|^2 \left\{ \begin{aligned} & \overline{i_{22}^2} |(g_{m3}C_0 - g_{m2}g_{m3}R_{e2}A_0|^2 \\ & + \overline{i_{31}^2} |(g_{m3}C_0|^2 + \overline{i_{32}^2} |(Y_{\pi3}C_0|^2 \end{aligned} \right\} \quad (A.25) \end{aligned}$$

$$\begin{aligned} i_{nc}e_{nc}^* = & A_1 \left\{ \begin{aligned} & \overline{i_{11}^2} (g_{m1}R_{e1}) [R_{e1}(1 - r_{b1}g_{m1})]^* - \overline{i_{12}^2} (Y_{\pi1}R_{e1}) [R_{e1}(Y_{\pi1}r_{b1} + 1)]^* \\ & - \overline{i_{21}^2} [(R_{e1} + r_{b2} + R_{e2})Y_{\pi1}] [A_0(r_{b2} + R_{e2}) + R_{e1}(Y_{\pi1}r_{b1} + 1)]^* \\ & - \overline{e_{e1}^2} Y_{\pi1} (Y_{\pi1}r_{b1} + 1)^* - \overline{e_{b2}^2} Y_{\pi1} A_0^* - \overline{e_{e2}^2} Y_{\pi1} A_0^* \end{aligned} \right\} \\ & + \left| \frac{1}{g_{m2}g_{m3}(Y_{\pi1} + g_{m1})R_{e1}} \right|^2 \\ & + \left\{ \begin{aligned} & \overline{i_{22}^2} g_{m3} Y_{\pi1} [Y_{\pi2}(R_{e1} + R_{e2}) \\ & + (Y_{\pi2}r_{b2} + 1)] [g_{m3}C_0 - g_{m2}g_{m3}R_{e2}A_0]^* \\ & + \overline{i_{31}^2} (g_{m3}C_1) (g_{m3}C_0)^* + \overline{i_{32}^2} (Y_{\pi3}C_1) (Y_{\pi3}C_0)^* \end{aligned} \right\} \quad (A.26) \end{aligned}$$

$$\begin{aligned} C_0 = & Y_{\pi2}R_{e1}(Y_{\pi1}r_{b1} + 1) + [(Y_{\pi1}r_{b1} + 1) + R_{e1}(Y_{\pi1} + g_{m1})] \\ & \cdot [(Y_{\pi2}r_{b2} + 1) + (Y_{\pi2} + g_{m2})R_{e2}] \quad (A.27) \end{aligned}$$

$$C_1 = Y_{\pi1} \cdot [Y_{\pi2}(R_{e1} + r_{b2} + R_{e2}) + 1 + g_{m2}R_{e2}] \quad (A.28)$$

$$A_0 = R_{e1}(Y_{\pi1} + g_{m1}) + Y_{\pi1}r_{b1} + 1 \quad (A.29)$$

$$A_1 = \left| \frac{1}{R_{e1}(Y_{\pi1} + g_{m1})} \right|^2 \quad (\text{A.30})$$

$$Y_{\pi i} = \frac{1}{r_{\pi i}} + j\omega C_{\pi i}, (i = 1, 2, 3) \quad (\text{A.31})$$

$Z_f$  is the forward transimpedance gain of the preamplifier in the passband, derived as

$$Z_f = \frac{v_{out}}{i_s} = -\frac{nGZ_{\pi c}Z_{\pi b}e^{-jN\rho}}{2} \quad (\text{A.32})$$

where  $G$  is the equivalent transconductance of the HBT CCC given by

$$G = \frac{g_{m2}g_{m3}}{Y_{\pi3}g_{m3}} \cdot \frac{(Y_{\pi1} + g_{m1})R_{e1}}{(Y_{\pi1}r_{b1} + 1)Y_{\pi2}R_{e1} + [(Y_{\pi1}r_{b1} + 1) + (Y_{\pi1} + g_{m1})R_{e1}][(Y_{\pi2}r_{b2} + 1) + (Y_{\pi2} + g_{m2})R_{e2}]} \quad (\text{A.33})$$

As previously defined,  $\rho$  is the per stage phase delay of the HBT DA and  $r_{\pi i}$  and  $C_{\pi i}$  are the HBT model parameters. The contribution of the base and collector terminations to the overall noise density are reflected in the first two terms of (A.20), while the remaining contributions are noise sources for the HBT gain cells.  $|i_{nc}|^2$  and  $|e_{nc}|^2$  are equivalent noise sources of the HBT gain cell which are derived from the equivalent circuit of the gain cell;  $i_{nc}e_{nc}^*$  is the correlation between these two noise sources.

The single-stage expression for A.20 simplifies to

$$|i_{HBT-CCC}| = \sqrt{\begin{aligned} & \frac{|i_{Z\pi b}|^2}{4}|1 + e^{j\rho}|^2 + \frac{|i_{Z\pi c}|^2}{4} \left| \frac{Z_{\pi c}}{Z_f} \right|^2 \\ & + \frac{|i_{nc}|^2}{4}|1 + e^{j\rho}|^2 + \frac{|e_{nc}|^2}{n} \left| \frac{1}{Z_{\pi b}} \right|^2 \\ & + \frac{1}{2} \text{Re} \left[ i_{nc}e_{nc}^* \left( -\frac{2}{Z_{\pi b}} \right)^* (1 + e^{-j\rho}) \right] \end{aligned}} \quad (\text{A.34})$$

as  $C(r, \rho) = 1 + e^{j\rho}$

As expected, the noise contribution for the the source, load and terminations are the same as in (A.18), while the noise contribution from the gain cell differs slightly. The difference observed between (A.18) and (A.34) is attributable to the higher analytical complexity involved in expressing the noise contributions and correlation of the CCC gain cell which has three active devices compared to just one in the CE gain cell.

Equation (A.17) may also be extended to an  $m$ -tier multiplicative DA based on a MESFET common source gain cell. To arrive at the desired expression, the equivalent input noise power contribution from the intermediate transmission lines - which is denoted by  $|i_{n-int}^m|^2$  -and the total equivalent input noise density of  $m$ -FETs or  $m$ -HBTs (denoted by  $|i_{n3}^m|^2$ ) in a cascade arrangement need to be derived. Hence, the total equivalent input noise density for the multiplicative DA ( $\sqrt{|i_n^m|^2}$ ) is given by

$$|i_n^m| = \sqrt{|i_{n1}^m|^2 + |i_{n-int}^m|^2 + |i_{n2}^m|^2 + |i_{n3}^m|^2} \quad (\text{A.35})$$

where the superscript  $m$  in this equation indicates that the elements relate to the multiplicative DA rather than as a factor of exponentiation.

# References

- [1] S. Kang, D. Kim, M. Urteaga, and M. Seo, “State-of-the-art THz integrated circuits in InP HBT technologies,” in *Radio-Frequency Integration Technology (RFIT), 2017 IEEE International Symposium on*. IEEE, 2017, pp. 25–27.
- [2] W. Percival, “Thermionic valve circuits,” *British patent*, vol. 460562, p. 25, 1937.
- [3] M. Urteaga, M. Seo, J. Hacker, Z. Griffith, A. Young, R. Pierson, P. Rowell, A. Skalare, V. Jain, E. Lobisser *et al.*, “InP HBTs for THz frequency integrated circuits,” in *23rd International Conference on Indium Phosphide and Related Materials*. IEEE, 2011, pp. 1–4.
- [4] M. Kim, A. Oki, G. Gorman, D. Umemoto, and J. Camou, “GaAs heterojunction bipolar transistor device and IC technology for high-performance analog and microwave applications,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 37, no. 9, pp. 1286–1303, 1989.
- [5] S. M. Taher and J. R. Scott, “A comparison of InP HBT transimpedance amplifier topologies for high dynamic range photonic links,” in *Microwave Conference, 2009. APMC 2009. Asia Pacific*. IEEE, 2009, pp. 222–225.
- [6] M. Rodwell, Z. Griffith, N. Parthasarathy, E. Lind, C. Sheldon, S. Bank, U. Singiseti, M. Urteaga, K. Shinohara, R. Pierson *et al.*, “Developing bipolar transistors for sub-mm-wave amplifiers and next-generation (300 GHz) digital circuits,” in *Device Research Conference, 2006 64th*. IEEE, 2006, pp. 5–8.
- [7] K. W. Kobayashi, L. T. Tran, J. C. Cowles, T. R. Block, A. K. Oki, and D. C. Streit, “Extending the bandwidth performance of heterojunction bipolar

- transistor-based distributed amplifiers,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 5, pp. 739–748, 1996.
- [8] K. Kobayashi, J. Cowles, L. Tran, A. Gutierrez-Aitken, T. Block, A. Oki, and D. Streit, “A 50-MHz-55-GHz multidecade InP-based HBT distributed amplifier,” *IEEE Microwave and Guided Wave Letters*, vol. 7, no. 10, pp. 353–355, 1997.
- [9] S. Mohammadi, J. Park, D. Pavlidis, J. Guyaux, and J. Garcia, “Optimal design and experimental characterization of high-gain GaInP/GaAs HBT distributed amplifiers,” in *Microwave Symposium Digest, 1999 IEEE MTT-S International*, vol. 2. IEEE, 1999, pp. 685–688.
- [10] R. Lai, W. Deal, X. Mei, W. Yoshida, J. Lee, L. Dang, J. Wang, Y. Kim, P. Liu, V. Radisic *et al.*, “Fabrication of InP HEMT devices with extremely high F<sub>max</sub>,” in *Indium Phosphide and Related Materials, 2008. IPRM 2008. 20th International Conference on.* IEEE, 2008, pp. 1–3.
- [11] J. Hacker, M. Seo, A. Young, Z. Griffith, M. Urteaga, T. Reed, and M. Rodwell, “THz MMICs based on InP HBT technology,” in *Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International*. IEEE, 2010, pp. 1126–1129.
- [12] M. Urteaga, J. Hacker, Z. Griffith, A. Young, R. Pierson, P. Rowell, M. Seo, and M. Rodwell, “A 130 nm InP HBT integrated circuit technology for THz electronics,” in *Electron Devices Meeting (IEDM), 2016 IEEE International*. IEEE, 2016, pp. 29–2.
- [13] M. Urteaga, A. Carter, Z. Griffith, R. Pierson, J. Bergman, A. Arias, P. Rowell, J. Hacker, B. Brar, and M. Rodwell, “THz bandwidth InP HBT technologies and heterogeneous integration with Si CMOS,” in *Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), 2016 IEEE*. IEEE, 2016, pp. 35–41.

- 
- [14] M. Urteaga, Z. Griffith, M. Seo, J. Hacker, and M. J. Rodwell, "InP HBT technologies for THz integrated circuits," *Proceedings of the IEEE*, vol. 105, no. 6, pp. 1051–1067, 2017.
- [15] A. Iqbal and I. Darwazeh, "Analytical modelling of the heterojunction bipolar transistor based distributed amplifier," in *High Frequency Postgraduate Student Colloquium, 1996., 2nd.* IEEE, 1996, pp. 11–16.
- [16] —, "A 23 GHz baseband HBT distributed amplifier for optical communication systems," in *Microwave Conference, 1998. 28th European*, vol. 1. IEEE, 1998, pp. 6–11.
- [17] K. Eriksson, I. Darwazeh, and H. Zirath, "InP DHBT distributed amplifiers with up to 235-GHz bandwidth," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 4, pp. 1334–1341, 2015.
- [18] M. Rodwell, E. Lobisser, M. Wistey, V. Jain, A. Baraskar, E. Lind, J. Koo, Z. Griffith, J. Hacker, M. Urteaga *et al.*, "THz bipolar transistor circuits: Technical feasibility, technology development, integrated circuit results," in *Compound Semiconductor Integrated Circuits Symposium, 2008. CSIC'08. IEEE.* IEEE, 2008, pp. 1–3.
- [19] M. Urteaga, Z. Griffith, R. Pierson, P. Rowell, A. Young, J. Hacker, B. Brar, S. Kim, R. Maurer, and M. Rodwell, "THz InP bipolar transistors-circuit integration and applications," in *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2017 IEEE.* IEEE, 2017, pp. 1–4.
- [20] C. Aitchison, "Potential of the distributed amplifier as a photo-diode detector amplifier in high bit rate optical communication systems," *Electronics Letters*, vol. 26, no. 20, pp. 1693–1695, 1990.
- [21] E. L. Ginzton, W. R. Hewlett, J. H. Jasberg, and J. D. Noe, "Distributed amplification," *Proceedings of the IRE*, vol. 36, no. 8, pp. 956–969, 1948.

- 
- [22] Y. Ayasli, R. L. Mozzi, J. L. Vorhaus, L. D. Reynolds, and R. A. Pucel, "A monolithic gaas 1-13-GHz traveling-wave amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 30, no. 7, pp. 976–981, 1982.
  - [23] Y. Ayasli, R. Mozzi, L. Hanes, and S. Miller, "Capacitively coupled traveling-wave power amplifier," *IEEE Transactions on Microwave Theory Techniques*, vol. 32, pp. 1704–1709, 1984.
  - [24] Y. Ayasli, L. Reynolds, R. Mozzi, and L. Hanes, "2-20-GHz GaAs traveling-wave power amplifier," *IEEE Transactions on Microwave Theory Techniques*, vol. 32, pp. 290–295, 1984.
  - [25] C. Paoloni and S. Kosslosky, "Graphical design method for traveling wave amplifier based on filter theory," in *Microwave Symposium Digest, 1993., IEEE MTT-S International*. IEEE, 1993, pp. 273–276.
  - [26] V. Kaman, T. Reynolds, A. Petersen, and J. E. Bowers, "A 100-kHz to 50-GHz traveling-wave amplifier IC module," *IEEE Microwave and Guided Wave Letters*, vol. 9, no. 10, pp. 416–418, Oct 1999.
  - [27] T. Kraemer, C. Meliani, F. J. Schmueckle, J. Wuerfl, and G. Traenkle, "Traveling-wave amplifiers in transferred substrate InP-HBT technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 9, pp. 2114–2121, 2009.
  - [28] T. T. Wong, *Fundamentals of distributed amplification*. Artech House, 1993.
  - [29] T. Y. Wong, A. P. Freundorfer, B. C. Beggs, and J. E. Sitch, "A 10 Gb/s Al-GaAs/GaAs HBT high power fully differential limiting distributed amplifier for III-V Mach-Zehnder modulator," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 10, pp. 1388–1393, 1995.
  - [30] N. Kumar and A. Grebennikov, *Distributed Power Amplifiers for RF and Microwave Communications*. Artech House, 2015.

- [31] G. L. Matthaei, L. Young, E. M. Jones *et al.*, *Microwave filters, impedance-matching networks, and coupling structures*. McGraw-Hill New York, 1964, vol. 5.
- [32] D. M. Pozar, *Microwave engineering*. John Wiley and Sons, 2009, pp 404 - 407.
- [33] W. Horton, J. Jasberg, and J. Noe, “Distributed amplifiers: practical considerations and experimental results,” *Proceedings of the IRE*, vol. 38, no. 7, pp. 748–753, 1950.
- [34] D. V. Payne, “Distributed amplifier theory,” *Proceedings of the IRE*, vol. 41, no. 6, pp. 759–762, June 1953.
- [35] A. Copson, “A distributed power amplifier,” *Electrical Engineering*, vol. 69, no. 10, pp. 893–898, 1950.
- [36] G. Nikandish, R. B. Staszewski, and A. Zhu, “The (r)evolution of distributed amplifiers: From vacuum tubes to modern CMOS and GaN ICs,” *IEEE Microwave Magazine*, vol. 19, no. 4, pp. 66–83, 2018.
- [37] B. Kleveland, C. Diaz, D. Vock, L. Madden, T. Lee, and S. Wong, “Monolithic CMOS distributed amplifier and oscillator,” in *Solid-State Circuits Conference, 1999. Digest of Technical Papers. ISSCC. 1999 IEEE International*. IEEE, 1999, pp. 70–71.
- [38] S. M. Sze, “High-speed semiconductor devices,” *New York, Wiley-Interscience, 1990, 653 p. No individual items are abstracted in this volume.*, 1990.
- [39] J. Schellenberg, H. Yamasaki, and P. Asher, “2 to 30 GHz monolithic distributed amplifier,” in *IEEE GaAs IC Symposium Tech. Dig., October 1984*, 1984, pp. 77–79.



- [40] E. Strid and K. R. Gleason, "A DC-12 GHz monolithic GaAs FET distributed amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 30, no. 7, pp. 969–975, 1982.
- [41] J. Beyer, S. Prasad, J. E. Nordman, R. Becker, and G. K. Hohenwarter, "Wideband monolithic microwave amplifier study." DTIC Document, Tech. Rep., 1983.
- [42] J. B. Beyer, S. Prasad, R. C. Becker, J. E. Nordman, and G. K. Hohenwarter, "Mesfet distributed amplifier design guidelines," *IEEE Transactions on Microwave Theory and Techniques*, vol. 32, no. 3, pp. 268–275, 1984.
- [43] I. Darwazeh, P. Moreira, A. Borjak, and J. O'Reilly, "A distributed optical receiver preamplifier with unequal gate/drain impedances," in *Microwave and Millimeter-Wave Monolithic Circuits Symposium, 1995. Digest of Papers., IEEE 1995*. IEEE, 1995, pp. 199–202.
- [44] B. Agarwal, Q. Lee, D. Mensa, R. Pallela, J. Guthrie, and M. J. Rodwell, "80-GHz distributed amplifiers with transferred-substrate heterojunction bipolar transistors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 12, pp. 2302–2307, 1998.
- [45] K. W. Kobayashi, J. Cowles, L. Tran, T. Block, A. Oki, and D. Streit, "A 2-32 GHz coplanar waveguide InAlAs-InGaAs-InP HBT cascode distributed amplifier," in *Microwave Symposium Digest, 1995., IEEE MTT-S International*. IEEE, 1995, pp. 215–218.
- [46] K. Kobayashi, L. Tran, M. Lammert, A. Oki, and D. Streit, "Transimpedance bandwidth performance of an HBT loss-compensated coplanar waveguide distributed amplifier," *Electronics Letters*, vol. 32, no. 24, pp. 2287–2288, 1996.

- 
- [47] L. Enloe and P. Rogers, "Wideband transistor distributed amplifiers," in *Solid-State Circuits Conference. Digest of Technical Papers. 1959 IEEE International*, vol. II, Feb 1959, pp. 44–45.
- [48] W.-K. Chen, *The VLSI handbook*. CRC press, 2006, pp 72-16 - 72-17.
- [49] L. A. Samoska, "An overview of solid-state integrated circuit amplifiers in the submillimeter-wave and THz regime," *IEEE Transactions on Terahertz Science and Technology*, vol. 1, no. 1, pp. 9–24, 2011.
- [50] C. Poole and I. Darwazeh, *Microwave Active Circuit Analysis and Design*. Academic Press, 2015.
- [51] K. W. Kobayashi, R. Esfandiari, M. E. Hafizi, D. C. Streit, A. K. Oki, L. T. Tran, D. K. Umemoto, and M. E. Kim, "GaAs HBT wideband matrix distributed and darlington feedback amplifiers to 24 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 39, no. 12, pp. 2001–2009, 1991.
- [52] W.-K. Chen, *The VLSI handbook*. CRC press, 2006.
- [53] S. Mohammadi, J.-W. Park, D. Pavlidis, J.-L. Guyaux, and J. C. Garcia, "Design optimization and characterization of high-gain GaInP/GaAs HBT distributed amplifiers for high-bit-rate telecommunication," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 6, pp. 1038–1044, 2000.
- [54] Y. Baeyens, N. Weimann, P. Roux, A. Leven, V. Houtsma, R. F. Kopf, Y. Yang, J. Frackowiak, A. Tate, J. S. Weiner *et al.*, "High gain-bandwidth differential distributed InP D-HBT driver amplifiers with large (11.3 v pp) output swing at 40 Gb/s," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 10, pp. 1697–1705, 2004.
- [55] K. Schneider, R. Driad, R. E. Makon, H. Maßler, M. Ludwig, R. Quay, M. Schlechtweg, and G. Weimann, "Comparison of InP/InGaAs DHBT distributed amplifiers as modulator drivers for 80-Gbit/s operation," *IEEE*

- 
- Transactions on Microwave Theory and Techniques*, vol. 53, no. 11, pp. 3378–3387, 2005.
- [56] V. Hurm, F. Benkhelifa, R. Driad, R. Lösch, R. Makon, H. Massler, J. Rosenzweig, M. Schlechtweg, and H. Walcher, “InP DHBT-based distributed amplifier for 100 Gbit/s modulator driver operation,” *Electronics Letters*, vol. 44, no. 12, pp. 705–706, 2008.
- [57] J.-Y. Dupuy, A. Konczykowska, F. Jorge, M. Riet, and J. Godin, “Distributed amplifiers in InP DHBT for 100-Gbit/s operation,” in *Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International*. IEEE, 2010, pp. 920–923.
- [58] S. Yoon, I. Lee, M. Urteaga, M. Kim, and S. Jeon, “A fully-integrated 40–222 GHz InP HBT distributed amplifier,” *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 7, pp. 460–462, 2014.
- [59] Y. Li, W.-L. Goh, H. Tang, H. Liu, X. Deng, and Y.-Z. Xiong, “A 10 to 170 GHz distributed amplifier using 130-nm SiGe HBTs,” in *Integrated Circuits (ISIC), 2016 International Symposium on*. IEEE, 2016, pp. 1–4.
- [60] S. Giannakopoulos, K. Eriksson, I. Darwazeh, Z. S. He, and H. Zirath, “Ultra-broadband common collector-cascode 4-cell distributed amplifier in 250nm InP HBT technology with over 200 GHz bandwidth,” in *Microwave Integrated Circuits Conference (EuMIC), 2017 12th European*. IEEE, 2017, pp. 142–145.
- [61] W. Jutzi, “A MESFET distributed amplifier with 2 GHz bandwidth,” *Proceedings of the IEEE*, vol. 57, no. 6, pp. 1195–1196, 1969.
- [62] M. Cooke, “Technology focus: Indium phosphide; transcending frequency and integration limits,” semiconductorTODAY Compounds&AdvancedSilicon, Vol. 1 Issue 3, Tech. Rep., 2006.

- 
- [63] G. I. Ng, K. Radhakrishnan, and H. Wang, "Are we there yet?-a metamorphic HEMT and HBT perspective," in *Gallium Arsenide and Other Semiconductor Application Symposium, 2005. EGAAS 2005. European.* IEEE, 2005, pp. 13–19.
- [64] L. Moura and I. Darwazeh, *Introduction to linear circuit analysis and modelling: from DC to RF.* Elsevier, 2005.
- [65] R. Majidi-Ahy, C. K. Nishimoto, M. Riazat, M. Glenn, S. Silverman, S.-L. Weng, Y.-C. Pao, G. Zdasiuk, S. Bandy, and Z. Tan, "5-100 GHz InP coplanar waveguide MMIC distributed amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 38, no. 12, pp. 1986–1993, 1990.
- [66] S. Kimura, Y. Imai, Y. Umeda, and T. Enoki, "0-90 GHz In-AlAs/InGaAs/InP HEMT distributed baseband amplifier IC," *Electronics Letters*, vol. 31, no. 17, pp. 1430–1431, 1995.
- [67] S. Kimura and Y. Imai, "0-40 GHz GaAs MESFET distributed baseband amplifier ICs for high-speed optical transmission," *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 11, pp. 2076–82, 1996.
- [68] B. Agarwal, A. E. Schmitz, J. Brown, M. Matloubian, M. G. Case, M. Le, M. Lui, and M. J. Rodwell, "112-GHz, 157-GHz, and 180-GHz InP HEMT traveling-wave amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 12, pp. 2553–2559, 1998.
- [69] M. Heins, C. Campbell, M.-Y. Kao, M. Muir, and J. Carroll, "A GaAs MHEMT distributed amplifier with 300-GHz gain-bandwidth product for 40-Gb/s optical applications," in *Microwave Symposium Digest, 2002 IEEE MTT-S International*, vol. 2. IEEE, 2002, pp. 1061–1064.
- [70] H. Shigematsu, M. Sato, T. Hirose, and Y. Watanabe, "A 54-GHz distributed amplifier with 6-v/sub PP/output for a 40-Gb/s LiNbO/sub 3/modulator

- driver,” *IEEE Journal of Solid-State Circuits*, vol. 37, no. 9, pp. 1100–1105, 2002.
- [71] C. Meliani, G. Post, G. Rondeau, J. Decobert, W. Mouzannar, E. Dutisseuil, and R. Lefevre, “DC-92 GHz ultra-broadband high gain InP HEMT amplifier with 410 GHz gain-bandwidth product,” *Electronics Letters*, vol. 38, no. 20, p. 1, 2002.
- [72] K.-L. Deng, T.-W. Huang, and H. Wang, “Design and analysis of novel high-gain and broad-band GaAs pHEMT MMIC distributed amplifiers with traveling-wave gain stages,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 11, pp. 2188–2196, 2003.
- [73] G. Wolf, H. Happy, S. Demichel, R. Leblanc, F. Blache, R. Lefevre, and G. Dambrine, “A metamorphic GaAs HEMT distributed amplifier with 50 GHz bandwidth and low noise for 40 Gbits/s,” in *Microwave Symposium Digest, 2005 IEEE MTT-S International*. IEEE, 2005, pp. 3–pp.
- [74] M. Hafele, K. Beilenhoff, and H. Schumacher, “GaAs distributed amplifiers with up to 350 GHz gain-bandwidth product for 40 Gb/s LiNbO<sub>3</sub>/modulator drivers,” in *Microwave Conference, 2005 European*, vol. 1. IEEE, 2005, pp. 4–pp.
- [75] G. Nikandish and A. Medi, “Unilateralization of MMIC distributed amplifiers,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 12, pp. 3041–3052, 2014.
- [76] Y. Li, W.-L. Goh, and Y.-Z. Xiong, “A 2 to 92 GHz distributed amplifier using 70-nm InP HEMTs,” in *Wireless Symposium (IWS), 2015 IEEE International*. IEEE, 2015, pp. 1–4.
- [77] G. Nikandish and A. Medi, “A 40-GHz bandwidth tapered distributed LNA,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 11, pp. 1614–1618, 2018.

- 
- [78] B. Kleveland, C. Diaz, D. Vock, L. Madden, T. Lee, and S. Wong, "Monolithic CMOS distributed amplifier and oscillator," in *Solid-State Circuits Conference, 1999. Digest of Technical Papers. ISSCC. 1999 IEEE International*. IEEE, 1999, pp. 70–71.
- [79] P. V. Testa, D. Fritsche, S. Schumann, W. Finger, C. Carta, and F. Ellinger, "110 GHz travelling-wave amplifier in 22 nm FD-SOI CMOS," in *Microwave Conference (APMC), 2017 IEEE Asia Pacific*. IEEE, 2017, pp. 406–409.
- [80] J.-O. Plouchart, J. Kim, N. Zamdmer, L.-H. Lu, M. Sherony, Y. Tan, R. A. Groves, R. Trzcinski, M. Talbi, A. Ray *et al.*, "A 4-91-GHz traveling-wave amplifier in a standard 0.12-/spl mu/m SOI CMOS microprocessor technology," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 9, pp. 1455–1461, 2004.
- [81] F. Ellinger, "60-GHz SOI CMOS traveling-wave amplifier with NF below 3.8 dB from 0.1 to 40 GHz," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 2, pp. 553–558, 2005.
- [82] R.-C. Liu, T.-P. Wang, L.-H. Lu, H. Wang, S.-H. Wang, and C.-P. Chao, "An 80GHz travelling-wave amplifier in a 90nm CMOS technology," in *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*. IEEE, 2005, pp. 154–590.
- [83] M.-D. Tsai, H. Wang, J.-F. Kuan, and C.-S. Chang, "A 70GHz cascaded multi-stage distributed amplifier in 90nm CMOS technology," in *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*. IEEE, 2005, pp. 402–606.
- [84] J. R. Weiss, M. A. Kossel, C. Menolfi, T. Morf, M. L. Schmatz, T. Toifl, and H. Jaeckel, "A DC-to-44-GHz 19dB gain amplifier in 90nm CMOS using capacitive bandwidth enhancement," in *Solid-State Circuits Conference, 2006*.

- ISSCC 2006. Digest of Technical Papers. IEEE International.* IEEE, 2006, pp. 2082–2091.
- [85] F. Zhang and P. R. Kinget, “Low-power programmable gain CMOS distributed LNA,” *IEEE Journal of Solid-State Circuits*, vol. 41, no. 6, pp. 1333–1343, 2006.
- [86] K. Moez and M. Elmasry, “A 10dB 44GHz loss-compensated CMOS distributed amplifier,” in *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International.* IEEE, 2007, pp. 548–621.
- [87] J.-C. Chien and L.-H. Lu, “40-Gb/s high-gain distributed amplifiers with cascaded gain stages in 0.18- $\mu$ m CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2715–2725, 2007.
- [88] C. Marcu, D. Chowdhury, C. Thakkar, J.-D. Park, L.-K. Kong, M. Tabesh, Y. Wang, B. Afshar, A. Gupta, A. Arbabian *et al.*, “A 90 nm CMOS low-power 60 GHz transceiver with integrated baseband circuitry,” *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3434–3447, 2009.
- [89] Y.-J. Wang and A. Hajimiri, “A compact low-noise weighted distributed amplifier in CMOS,” 2009.
- [90] A. Arbabian and A. M. Niknejad, “Design of a CMOS tapered cascaded multistage distributed amplifier,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 4, pp. 938–947, 2009.
- [91] P. Chen, J.-C. Kao, P.-C. Huang, and H. Wang, “A novel distributed amplifier with high gain, low noise and high output power in 0.18- $\mu$ m CMOS technology,” in *Microwave Symposium Digest (MTT), 2011 IEEE MTT-S International.* IEEE, 2011, pp. 1–4.
- [92] J. Kim and J. F. Buckwalter, “A 92 GHz bandwidth distributed amplifier in a 45 nm SOI CMOS technology,” *IEEE Microwave and Wireless Components Letters*, vol. 21, no. 6, pp. 329–331, 2011.

- [93] A. Jahanian and P. Heydari, "A CMOS distributed amplifier with distributed active input balun using GBW and linearity enhancing techniques," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 5, pp. 1331–1341, 2012.
- [94] C.-Y. Hsiao, T.-Y. Su, and S. S. Hsu, "CMOS distributed amplifiers using gate–drain transformer feedback technique," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 8, pp. 2901–2910, 2013.
- [95] V. Bhagavatula, M. Taghivand, and J. C. Rudell, "A compact 77% fractional bandwidth cmos band-pass distributed amplifier with mirror-symmetric norton transforms," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 5, pp. 1085–1093, 2015.
- [96] H. Li, G. Balamurugan, J. Jaussi, and B. Casper, "A 112 Gb/s PAM4 linear TIA with 0.96 pJ/bit energy efficiency in 28 nm CMOS," in *ESSCIRC 2018-IEEE 44th European Solid State Circuits Conference (ESSCIRC)*. IEEE, 2018, pp. 238–241.
- [97] B. Sewiolo, G. Fischer, and R. Weigel, "A 12-GHz high-efficiency tapered traveling-wave power amplifier with novel power matched cascode gain cells using SiGe HBT transistors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 10, pp. 2329–2336, 2009.
- [98] A. Ghadiri and K. Moez, "Gain-enhanced distributed amplifier using negative capacitance," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 11, pp. 2834–2843, 2010.
- [99] J. F. Buckwalter and J. Kim, "Cascaded constructive wave amplification," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 3, pp. 506–517, 2010.



- 
- [100] J. Chen and A. M. Niknejad, "Design and analysis of a stage-scaled distributed power amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 5, pp. 1274–1283, 2011.
- [101] A. Arbabian and A. M. Niknejad, "A three-stage cascaded distributed amplifier with GBW exceeding 1.5 THz," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2012 IEEE*. IEEE, 2012, pp. 211–214.
- [102] P. V. Testa, G. Belfiore, R. Paulo, C. Carta, and F. Ellinger, "170 GHz SiGe-BiCMOS loss-compensated distributed amplifier," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 10, pp. 2228–2238, 2015.
- [103] P. V. Testa, R. Paulo, C. Carta, and F. Ellinger, "250 GHz SiGe-BiCMOS cascaded single-stage distributed amplifier," in *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2015 IEEE*. IEEE, 2015, pp. 1–4.
- [104] D. Fritsche, G. Tretter, C. Carta, and F. Ellinger, "A trimmable cascaded distributed amplifier with 1.6 THz gain-bandwidth product," *IEEE Transactions on Terahertz Science and Technology*, vol. 5, no. 6, pp. 1094–1096, 2015.
- [105] J. Hoffman, S. Shopov, P. Chevalier, A. Cathelin, P. Schvan, and S. P. Voinigescu, "55-nm SiGe BiCMOS distributed amplifier topologies for time-interleaved 120-Gb/s fiber-optic receivers and transmitters," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 9, pp. 2040–2053, 2016.
- [106] K. Fang, C. S. Levy, and J. F. Buckwalter, "Supply-scaling for efficiency enhancement in distributed power amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 9, pp. 1994–2005, 2016.
- [107] P. V. Testa, C. Carta, and F. Ellinger, "200 GHz SiGe-BiCMOS loss-compensated distributed power divider," in *Microwave Conference (APMC), 2017 IEEE Asia Pacific*. IEEE, 2017, pp. 295–298.

- [108] P. V. Testa, C. Carta, U. Jörges, and F. Ellinger, “Analysis and design of a 30-to 220-GHz balanced cascaded single-stage distributed amplifier in 130-nm SiGe BiCMOS,” *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1457–1467, 2018.
- [109] P. C. Magnusson, A. Weisshaar, V. K. Tripathi, and G. C. Alexander, *Transmission lines and wave propagation*. CRC press, 2017.
- [110] B. Kim and H. Q. Tserng, “0.5 W 2-21 GHz monolithic GaAs distributed amplifier,” *Electronics Letters*, vol. 20, no. 7, pp. 288–289, March 1984.
- [111] M. Pimenta and I. Darwazeh, “Circuit design proposal for multi-GBit/s CDMA over fibre using distributed topologies,” in *Communications and Information Technology, 2009. ISCIT 2009. 9th International Symposium on*. IEEE, 2009, pp. 1000–1005.
- [112] Y. Ayasli, J. Vorhaus, R. Mozzi, and L. Reynolds, “Monolithic GaAs travelling-wave amplifier,” *Electronics Letters*, vol. 17, p. 413, 1981.
- [113] W. Chen, “Distributed amplifiers: survey of the effects of lumped-transmission-line design on performance,” *Electrical Engineers, Proceedings of the Institution of*, vol. 114, no. 8, pp. 1065–1074, 1967.
- [114] C. F. Campbell, “Evolution of the nonuniform distributed power amplifier: A distinguished microwave lecture,” *IEEE Microwave Magazine*, vol. 20, no. 1, pp. 18–27, Jan 2019.
- [115] D. Dawson, M. Salib, and L. Dickens, “Distributed cascode amplifier and noise figure modeling of an arbitrary amplifier configuration,” in *Solid-State Circuits Conference. Digest of Technical Papers. 1984 IEEE International*, vol. XXVII, Feb 1984, pp. 78–79.
- [116] K. W. Kobayashi, R. Esfandiari, and A. K. Oki, “A novel HBT distributed amplifier design topology based on attenuation compensation techniques,”

- IEEE Transactions on Microwave Theory and Techniques*, vol. 42, no. 12, pp. 2583–2589, Dec 1994.
- [117] I. D. Robertson and S. Lucyszyn, *RFIC and MMIC Design and Technology*. Iet, 2001, no. 13.
- [118] S. Kimura, Y. Imai, Y. Umeda, and T. Enoki, “Loss-compensated distributed baseband amplifier IC’s for optical transmission systems,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 44, no. 10, pp. 1688–1693, 1996.
- [119] A. Kopa and A. B. Apsel, “Alternative m-derived termination for distributed amplifiers,” in *Microwave Symposium Digest, 2009. MTT’09. IEEE MTT-S International*. IEEE, 2009, pp. 921–924.
- [120] K. Eriksson, I. Darwazeh, and H. Zirath, “InP DHBT wideband amplifiers with up to 235 GHz bandwidth,” in *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*. IEEE, 2014, pp. 1–4.
- [121] P. K. Ikalainen, “Low-noise distributed amplifier with active load,” *IEEE Microwave and Guided Wave Letters*, vol. 6, no. 1, pp. 7–9, Jan 1996.
- [122] K. Niclas and R. Pereira, “Performance of a 2-18 GHz ultra low-noise amplifier module,” in *Microwave Symposium Digest, 1989., IEEE MTT-S International*. IEEE, 1989, pp. 841–844.
- [123] R. H. Frater and D. R. Williams, “An active "cold" noise source,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 29, no. 4, pp. 344–347, Apr 1981.
- [124] K. B. Niclas and R. R. Pereira, “The matrix amplifier: a high-gain module for multioctave frequency bands,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 35, no. 3, pp. 296–306, 1987.

- [125] K.-H. Chen and C.-K. Wang, "A 3.1-10.6 GHz CMOS cascaded two-stage distributed amplifier for ultra-wideband application," in *Advanced System Integrated Circuits 2004. Proceedings of 2004 IEEE Asia-Pacific Conference on.* IEEE, 2004, pp. 296–299.
- [126] A. Chang, K. Niclas, B. Cantos, and W. Striffler, "Design and performance of a 2-18 GHz monolithic matrix amplifier," in *Digest of Papers., Microwave and Millimeter-Wave Monolithic Circuits Symposium.* IEEE, 1989, pp. 139–141.
- [127] S. Chu, Y. Tajima, J. Cole, A. Platzker, and M. Schindler, "A novel 4-18 GHz monolithic matrix distributed amplifier," in *Microwave Symposium Digest, 1989., IEEE MTT-S International.* IEEE, 1989, pp. 291–295.
- [128] K. Simon, S. Chu, R. Wolhert, M. Schindler, and J. Cole, "A millimeter-wave monolithic matrix distributed amplifier," in *IEEE 1992 Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest of Papers.* IEEE, 1992, pp. 73–75.
- [129] H. Kroemer, "Theory of a wide-gap emitter for transistors," *Proceedings of the IRE*, vol. 45, no. 11, pp. 1535–1537, 1957.
- [130] B. Nelson, C. Perry, R. Dixit, B. Allen, M. Kim, A. Oki, J. Camou, and D. Umemoto, "High-linearity, low DC power GaAs HBT broadband amplifiers to 11 GHz," in *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1989. Technical Digest 1989., 11th Annual.* IEEE, 1989, pp. 79–82.
- [131] H. Brouzes, G. Deredec, and Y. Bender, "A 1 to 40 GHz MESFET hybrid distributed amplifier," in *Microwave Symposium Digest, 1989., IEEE MTT-S International.* IEEE, 1989, pp. 849–852.
- [132] B. Nelson, D. Umemoto, C. Perry, R. Dixit, B. Allen, M. Kim, and A. Oki, "High-linearity, low DC power monolithic GaAs HBT broadband amplifiers

- to 11 GHz,” in *Microwave and Millimeter-Wave Monolithic Circuits Symposium, 1990. Digest of Papers., IEEE 1990.* IEEE, 1990, pp. 15–18.
- [133] M. Rodwell, D. Scott, M. Urteaga, M. Dahlstrom, S. Krishnan, Z. Griffith, Y. Wei, N. Parthasarathy, and Y. Kim, “Submicron InP bipolar transistors: Scaling laws, technology roadmaps, advanced fabrication processes,” *Solid State Devices and Materials*, pp. 270–271, 2002.
- [134] A. Chang, K. Niclas, B. Cantos, and W. Striffler, “Design and performance of a 2-18 GHz monolithic matrix amplifier,” in *Microwave and Millimeter-Wave Monolithic Circuit Symposium Digest, 1990., IEEE.* IEEE, 1990, pp. 139–141.
- [135] K. Chang, B. Nelson, A. Oki, and D. Umemoto, “2-19 GHz low-DC power and high-IP/sub 3/monolithic HBT matrix amplifier,” *IEEE Microwave and Guided Wave Letters*, vol. 2, no. 1, pp. 17–18, 1992.
- [136] D. C. Streit, A. K. Oki, D. K. Umemoto, L. T. Tran, and K. W. Kobayashi, “High performance HBTs with built-in base fields: exponentially-graded doping vs. graded composition,” in *[1991] Proceedings IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits*, Aug 1991, pp. 325–333.
- [137] K. Kobayashi, J. Cowles, L. Tran, T. Block, A. Oki, and D. Streit, “A 2-50 GHz InAlAs/InGaAs-InP HBT distributed amplifier,” in *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1996. Technical Digest 1996., 18th Annual.* IEEE, 1996, pp. 207–210.
- [138] M. Rodwell, Q. Lee, D. Mensa, J. Guthrie, Y. Betser, S. Martin, R. Smith, S. Jaganathan, T. Mathew, P. Krishnan *et al.*, “Transferred-substrate heterojunction bipolar transistor integrated circuit technology,” in *Indium Phosphide and Related Materials, 1999. IPRM. 1999 Eleventh International Conference on.* IEEE, 1999, pp. 169–174.

- 
- [139] J. Aguirre and C. Plett, "A 0.1-50 GHz SiGe HBT distributed amplifier employing constant-k m-derived sections," in *Microwave Symposium Digest, 2003 IEEE MTT-S International*, vol. 2. IEEE, 2003, pp. 923–926.
- [140] C. Meliani, M. Rudolph, and W. Heinrich, "On-chip GaAs-HBT broadband-coupled high-bitrate modulator driver TWAs," in *Gallium Arsenide and Other Semiconductor Application Symposium, 2005. EGAAS 2005. European*. IEEE, 2005, pp. 661–664.
- [141] H.-Y. Chang, Y.-C. Liu, S.-H. Weng, C.-H. Lin, Y.-L. Yeh, and Y.-C. Wang, "Design and analysis of a DC–43.5-GHz fully integrated distributed amplifier using gaas HEMT–HBT cascode gain stage," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 2, pp. 443–455, 2011.
- [142] S.-H. Chen, Y.-C. Liu, S.-H. Weng, H.-Y. Chang, K. Chen, and S.-H. Wu, "A monolithic DC-31 GHz distributed amplifier using cascode HBT-NMOS gain cell in 0.18  $\mu\text{m}$  SiGe technology," in *Microwave Conference Proceedings (APMC), 2012 Asia-Pacific*. IEEE, 2012, pp. 211–213.
- [143] J. Hoffman, S. P. Voinigescu, P. Chevalier, A. Cathelin, and P. Schvan, "A low noise, DC-135GHz MOS-HBT distributed amplifier for receiver applications," in *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2015 IEEE*. IEEE, 2015, pp. 1–4.
- [144] J. Hoffman, J.-R. Martin-Gosse, S. Shopov, J. J. Pekarik, R. Camillo-Castillo, V. Jain, D. Hame, and S. P. Voinigescu, "Analog circuit blocks for 80-GHz bandwidth frequency-interleaved, linear, large-swing front-ends," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 9, pp. 1985–1993, 2016.
- [145] J. Viaud, M. Lajugie, R. Quéré, and J. Obregon, "First demonstration of a 0.5 W, 2 to 8 GHz MMIC HBT distributed power amplifier based on a large signal design approach," in *Microwave Symposium Digest, 1997., IEEE MTT-S International*, vol. 2. IEEE, 1997, pp. 893–896.

- 
- [146] K. Kobayashi, A. Oki, M. Lammert, A. Gutierrez-Aitken, E. Kaneshiro, P. Grossman, K. Sato, T. Block, and D. Streit, "A 0.5-16 GHz capacitively coupled HBT medium power amplifier MMIC with active bias regulation," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2000. Digest of Papers. 2000 IEEE*. IEEE, 2000, pp. 165–168.
- [147] K. Krishnamurthy, J. Chow, M. Rodwell, and R. Pallela, "0.1-42 GHz InP DHBT distributed amplifiers with 35 dB gain and 15 dBm output," *Electronics Letters*, vol. 39, no. 22, pp. 1594–1595, 2003.
- [148] C. Schick, T. Feger, E. Soenmez, K. Schad, A. Trasser, and H. Schumacher, "Attenuation compensation techniques in distributed SiGe HBT amplifiers using highly lossy thin film microstrip lines," in *IEEE MTT-S Int. Microwave Symp., Long Beach, CA*, 2005.
- [149] A. Iqbal and I. Darwazeh, "A novel technique for designing wideband, bias stabilised HBT based distributed amplifiers for optical receiver applications," in *4th Communication Networks Symposium Digest*, 1997, pp. 71–77.
- [150] H. Suzuki, K. Watanabe, K. Ishikawa, H. Masuda, K. Ouchi, T. Tanoue, and R. Takeyari, "InP/InGaAs HBT ICs for 40 Gbit/s optical transmission systems," in *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, 1997. Technical Digest 1997., 19th Annual*. IEEE, 1997, pp. 215–218.
- [151] —, "Very-high-speed InP/InGaAs HBT ICs for optical transmission systems," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 9, pp. 1313–1320, 1998.
- [152] L. Robin, M. Regis, H. Cam, A. Perennec, D. Herve, D. Le Berre, A. Peden, S. Yaegassi, H. Yano, and S. Furudate, "Fully integrated distributed amplifier design on InP HBT technology for optoelectronics application," in *Microwave Symposium Digest, 2005 IEEE MTT-S International*. IEEE, 2005, pp. 4–pp.

- 
- [153] K. Kobayashi, L. Tran, M. Lammert, T. Block, A. Oki, and D. Streit, "A novel 12-24 GHz broadband HBT distributed active balanced mixer," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 1997., IEEE*. IEEE, 1997, pp. 75–78.
- [154] C. Paoloni, "HEMT-HBT matrix amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 8, pp. 1308–1312, 2000.
- [155] Y. Baeyens, R. Pallela, J. Mattia, H.-S. Tsai, and Y.-K. Chen, "A 74-GHz bandwidth InAlAs/InGaAs-InP HBT distributed amplifier with 13-dB gain," *IEEE Microwave and Guided Wave Letters*, vol. 9, no. 11, pp. 461–463, 1999.
- [156] Y. Baeyens, G. Georgiou, J. S. Weiner, A. Leven, V. Houtsma, P. Paschke, Q. Lee, R. F. Kopf, Y. Yang, L. Chua *et al.*, "InP D-HBT ICs for 40-Gb/s and higher bitrate lightwave transceivers," *Tech. Dig. 23rd Annu. Gallium Arsenide Integrated Circuit (GaAs IC) Symp*, vol. 37, no. 9, pp. 125–128, 2001.
- [157] Y. Arayashiki, Y. Ohkubo, Y. Amano, A. Takagi, M. Ejima, and Y. Matsuoka, "16 dB 80 GHz InGaP/GaAs HBT distributed amplifier," *Electronics Letters*, vol. 40, no. 4, pp. 244–245, 2004.
- [158] O. Wohlgemuth, P. Paschke, and Y. Baeyens, "SiGe broadband amplifiers with up to 80 GHz bandwidth for optical applications at 43 Gbit/s and beyond," in *Microwave Conference, 2003 33rd European*. IEEE, 2003, pp. 1087–1090.
- [159] E. Cohen, Y. Betser, B. Sheinman, S. Cohen, V. Sidorov, A. Gavrilov, and D. Ritter, "75 GHz InP HBT distributed amplifier with record figures of merit and low power dissipation for OEIC applications," in *Indium Phosphide and Related Materials, 2005. International Conference on*. IEEE, 2005, pp. 609–612.



- [160] E. Cohen, Y. Betser, B. Sheinman, S. Cohen, S. Sidorov, A. Gavrilov, and D. Ritter, "75 GHz InP HBT distributed amplifier with record figures of merit and low power dissipation," *IEEE Transactions on Electron Devices*, vol. 53, no. 2, pp. 392–394, 2006.
- [161] Y. Baeyens, N. Weimann, V. Houtsma, J. Weiner, Y. Yang, J. Frackoviak, P. Roux, A. Tate, and Y. Chen, "Submicron InP D-HBT single-stage distributed amplifier with 17 dB gain and over 110 GHz bandwidth," in *Microwave Symposium Digest, 2006. IEEE MTT-S International*. IEEE, 2006, pp. 818–821.
- [162] J. Y. Liang and C. S. Aitchison, "A proposal of a broadband high gain block using cascaded single-stage distributed amplifiers," in *High Performance Electron Devices for Microwave and Optoelectronic Applications, 1995. EDMO., IEEE 1995 Workshop on*. IEEE, 1995, pp. 173–178.
- [163] B. Banyamin, J. Liang, and C. Aitchison, "A new high gain-broadband amplifier using cascaded single stage distributed amplifiers," in *Asia-Pacific Microwave Conference Proceedings*, 1998, pp. 753–756.
- [164] K. Koon, Z. Hu, H. Aghvami, and A. A. Rezazadeh, "High gain and ultra wideband SiGe/BiCMOS cascaded single stage distributed amplifier for 4G RF front-end applications," in *Personal, Indoor and Mobile Radio Communications, 2003. PIMRC 2003. 14th IEEE Proceedings on*, vol. 3. IEEE, 2003, pp. 2180–2184.
- [165] K. W. Kobayashi, R. Esfandiari, and A. K. Oki, "A novel HBT distributed amplifier design topology based on attenuation compensation techniques," *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, no. 12, pp. 2583–2589, 1994.

- 
- [166] I. Botterill and C. Aitchison, "Predicted small-signal gain of the HBT distributed amplifier," in *Microwave Symposium Digest, 1994., IEEE MTT-S International*. IEEE, 1994, pp. 421–424.
- [167] —, "Predicted small-signal gain of the HBT distributed amplifier with practical terminations," in *Microwave Conference, 1994. 24th European*, vol. 2. IEEE, 1994, pp. 1882–1887.
- [168] —, "Accurate prediction of the small-signal gain of the HBT dual-fed distributed amplifier," in *Microwave Symposium Digest, 1995., IEEE MTT-S International*. IEEE, 1995, pp. 1073–1076.
- [169] C. Paoloni and S. D'Agostino, "An HBT unilateral model to design distributed amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 6, pp. 795–798, 1999.
- [170] A. Iqbal and I. Z. Darwazeh, "Analytical expression for the equivalent input noise current spectral density of HBT distributed amplifier based optical receivers," in *IEE Colloquium on Opto-Electronic Interfacing at Microwave Frequencies*. IET, 1999, p. 2.
- [171] I. Darwazeh and A. Iqbal, "Transimpedance gain modelling of optical receivers employing a PIN photodiode and HBT distributed amplifier combination," in *IEE Colloquium on Opto-Electronic Interfacing at Microwave Frequencies*. IET, 1999, p. 3.
- [172] X. Tian, A. Freundorfer, and L. Roy, "Noise analysis of a photoreceiver using a PIN and GaAs HBT distributed amplifier combination," *IEEE Microwave and Wireless Components Letters*, vol. 13, no. 6, pp. 208–210, 2003.
- [173] K. Koon, Z. Hu, A. Rezazadeh, and S. Marsh, "Design optimisation of HBT broadband distributed amplifiers," in *Electron Devices for Microwave and Optoelectronic Applications, 2001 International Symposium on*. IEEE, 2001, pp. 285–290.

- [174] C. Meliani, M. Rudolph, and W. Heinrich, "A 40 Gbps GaAs-HBT distributed amplifier with an over- $f_T$  cut-off frequency: Analytical and experimental study," in *IEEE MTT-S International Microwave Symposium digest*, vol. 4. Institute of Electrical and Electronics Engineers, 2005, pp. 1857–1860.
- [175] C. S. Aitchison, "The intrinsic noise figure of the MESFET distributed amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 33, no. 6, pp. 460–466, 1985.
- [176] A. P. Freundorfer and T. Nguyen, "Noise in distributed MESFET preamplifiers," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 8, pp. 1100–1111, 1996.
- [177] S. Deibele and J. B. Beyer, "Attenuation compensation in distributed amplifier design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 37, no. 9, pp. 1425–1433, Sep 1989.
- [178] A. Zólomy, "Synthesis method for distributed amplifiers," in *Microwaves, Radar and Wireless Communications, 2002. MIKON-2002. 14th International Conference on*, vol. 2. IEEE, 2002, pp. 512–515.
- [179] B. Y. Banyamin and M. Berwick, "Analysis of the performance of four-cascaded single-stage distributed amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 12, pp. 2657–2663, 2000.
- [180] M. Henini, "Heterojunction devices proving their worth," *III-Vs Review*, vol. 11, no. 2, pp. 40–46, 1998.
- [181] A. Virdee and B. Virdee, "Experimental performance of ultra-broadband amplifier design concept employing cascaded reactively terminated single-stage distributed amplifier configuration," *Electronics Letters*, vol. 36, no. 18, pp. 1554–1556, 2000.

- [182] B. Banyamin and M. Berwick, "The gain advantages of four cascaded single stage distributed amplifier configurations," in *2000 IEEE MTT-S International Microwave Symposium Digest (Cat. No.00CH37017)*, vol. 3, June 2000, pp. 1325–1328 vol.3.
- [183] T. Scientific, *TSC250v1.0 Design Manual*. Teledyne Scientific Company, 20xx.
- [184] K. Eriksson, "InP DHBT amplifiers and circuit packaging up to submillimeter-wave frequencies - PhD thesis," Chalmers University of Technology, Tech. Rep., 2015.
- [185] M. Seo, M. Urteaga, J. Hacker, A. Young, Z. Griffith, V. Jain, R. Pierson, P. Rowell, A. Skalare, A. Peralta *et al.*, "InP HBT IC technology for terahertz frequencies: Fundamental oscillators up to 0.57 THz," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 10, pp. 2203–2214, 2011.
- [186] A. Oudir, M. Mahdouani, and R. Bourguiga, "Direct extraction method of HBT equivalent-circuit elements relying exclusively on S-parameters measured at normal bias conditions," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 8, pp. 1973–1982, Aug 2011.
- [187] G. Nwaogu and C. Aitchison, "A very broadband microwave distributed amplifier using FETs," in *1981 11th European Microwave Conference*, 1981, pp. 609–613.
- [188] J. Y. Liang and C. S. Aitchison, "Gain performance of cascade of single stage distributed amplifiers [microwave circuits]," *Electronics Letters*, vol. 31, no. 15, pp. 1260–1261, Jul 1995.
- [189] G. L. Matthaei, L. Young, and E. M. Jones, "Design of microwave filters, impedance-matching networks, and coupling structures. volume 2," DTIC Document, Tech. Rep., 1963, pp 85 - 86.

- [190] B. Analui and A. Hajimiri, "Bandwidth enhancement for transimpedance amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 8, pp. 1263–1270, 2004.
- [191] C. Paoloni and S. Kossowski, "New approach on the design of travelling wave amplifier," in *Circuits and Systems, 1991., Proceedings of the 34th Midwest Symposium on*. IEEE, 1991, pp. 414–417.
- [192] E. Hamidi and M. M. Taheri, "Using filter theory for the design of matrix distributed amplifiers," in *Applied Electromagnetics and Communications, 2005. ICECom 2005. 18th International Conference on*, 2005, pp. 1–3.
- [193] H. Kikuchi, Y. Miyagawa, and T. Kimura, "Broad-band GaAs monolithic equalizing amplifiers for multigigabit-per-second optical receivers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 38, no. 12, pp. 1916–1923, 1990.
- [194] F.-T. Chien and Y.-J. Chan, "Bandwidth enhancement of transimpedance amplifier by a capacitive-peaking design," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 8, pp. 1167–1170, 1999.
- [195] M. J. Schindler, J. P. Wendler, M. P. Zaitlin, M. E. Miller, and J. R. Dormail, "A K/Ka-band distributed power amplifier with capacitive drain coupling," *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 12, pp. 1902–1907, 1988.
- [196] W. Ciccognani, G. Giolo, E. Limiti, and P. E. Longhi, "Split gate line distributed power amplifier using tapered drain line approach and active broadband input power divider," in *Microwave Conference, 2009. EuMC 2009. European*. IEEE, 2009, pp. 1425–1428.
- [197] N. Camilleri, P. Chye, A. Lee, and P. Gregory, "Monolithic 9 to 70 GHz distributed amplifier," in *Microwave and Millimeter-Wave Monolithic Circuits Symposium, 1990. Digest of Papers., IEEE 1990*. IEEE, 1990, pp. 27–30.

- 
- [198] K. W. Kobayashi, Y. Chen, I. Smorchkova, B. Heying, W.-B. Luo, W. Sutton, M. Wojtowicz, and A. Oki, "Multi-decade GaN HEMT cascode-distributed power amplifier with baseband performance," in *Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE*. IEEE, 2009, pp. 369–372.
- [199] K. B. Niclas and A. P. Chang, "Noise in two-tier matrix amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 1, pp. 11–20, 1988.
- [200] S. D'agostino, G. D'inzeo, P. Marietti, and G. Panariello, "A method for computing the noise figure in matrix distributed amplifier," in *Microwave Symposium Digest, 1990., IEEE MTT-S International*. IEEE, 1990, pp. 351–354.
- [201] M. Keshavarzi, A. Abdipour, A. Mohammadi, and G. Moradi, "Investigation of the transmission line loss on the performance of the HBT\_HEMT matrix amplifier," in *Applied Electromagnetics and Communications, 2005. ICECom 2005. 18th International Conference on*. IEEE, 2005, pp. 1–4.
- [202] J.-C. Chien, T.-Y. Chen, and L.-H. Lu, "A 9.5-dB 50-GHz matrix distributed amplifier in 0.18- $\mu\text{m}$  CMOS," in *VLSI Circuits, 2006. Digest of Technical Papers. 2006 Symposium on*. IEEE, 2006, pp. 146–147.
- [203] T.-Y. Chen, J.-C. Chien, and L.-H. Lu, "A 45.6-GHz matrix distributed amplifier in 0.18-nm CMOS," in *Custom Integrated Circuits Conference, 2005. Proceedings of the IEEE 2005*. IEEE, 2005, pp. 119–122.
- [204] A. Lamesa, G. Giolo, and E. Limiti, "Design procedure and performance of two 0.5-20 GHz GaAs PHEMT MMIC matrix distributed amplifier for EW applications," in *Microwave Conference, 2004. 34th European*, vol. 1. IEEE, 2004, pp. 9–12.

- 
- [205] B. Machiels, P. Reynaert, and M. Steyaert, "Power efficient distributed low-noise amplifier in 90 nm cmos," in *2010 IEEE Radio Frequency Integrated Circuits Symposium*. IEEE, 2010, pp. 131–134.
- [206] K. Niclas, R. Pereira, A. Graven, and A. Chang, "Design and performance of a new multi-octave high-gain amplifier," in *Microwave Symposium Digest, 1987 IEEE MTT-S International*, vol. 2. IEEE, 1975, pp. 829–832.
- [207] K. W. Kobayashi, R. Esfandiari, M. E. Hafizi, D. C. Streit, A. K. Oki, L. T. Tran, D. K. Umemoto, and M. E. Kim, "GaAs HBT wideband matrix distributed and darlington feedback amplifiers to 24 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 39, no. 12, pp. 2001–2009, 1991.
- [208] S. D'Agostino, G. D'Inzeo, G. Grifoni, P. Marietti, and G. Panariello, "A 0.5-12 GHz hybrid matrix distributed amplifier using commercially available FETs," in *Microwave Symposium Digest, 1991., IEEE MTT-S International*. IEEE, 1991, pp. 289–292.
- [209] R. Heilig, D. Hollmann, and G. Baumann, "A monolithic 2-52 GHz HEMT matrix distributed amplifier in coplanar waveguide technology," in *Microwave and Millimeter-Wave Monolithic Circuits Symposium, 1994. Digest of Papers., IEEE 1994*. IEEE, 1994, pp. 191–194.
- [210] S. D'Agostino and C. Paoloni, "Comparison between MMIC matrix and distributed amplifiers," *IEE Proceedings-Microwaves, Antennas and Propagation*, vol. 142, no. 1, pp. 75–77, 1995.
- [211] K. Niclas and B. Tucker, "On noise in distributed amplifiers at microwave frequencies," *IEEE Transactions on Microwave Theory and Techniques*, vol. 31, no. 8, pp. 661–668, 1983.
- [212] W. Ko and Y. Kwon, "Improved noise analysis of distributed preamplifier with cascode FET cells," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 1, pp. 361–371, 2005.

- [213] C. S. Aitchison, "The predicted signal to noise performance of a photodiode-distributed amplifier optical detector," in *Microwave Symposium Digest, 1992., IEEE MTT-S International*. IEEE, 1992, pp. 769–772.
- [214] J. V. Terán, M. L. de la Fuente, E. Limiti, B. Aja, and E. Artal, "Noise analysis in distributed amplifiers with feedback-active load," *IET Microwaves, Antennas & Propagation*, vol. 10, no. 15, pp. 1692–1700, 2016.
- [215] IEEE Group on Electron Devices, "IEEE Standard definitions on electron tubes," *American National Standards Institute*, vol. –, no. 02, pp. 10–11, 1971.
- [216] A. Van der Ziel, "Thermal noise in field-effect transistors," *Proceedings of the IRE*, vol. 50, no. 8, pp. 1808–1812, 1962.
- [217] A. Van Der Ziel, "Gate noise in field effect transistors at moderately high frequencies," *Proceedings of the IEEE*, vol. 51, no. 3, pp. 461–467, 1963.
- [218] A. Cappy, "Noise modeling and measurement techniques HEMTs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 1, pp. 1–10, 1988.
- [219] A. Van der Ziel and G. Bosman, "Accurate expression for the noise temperature of common emitter microwave transistors," *IEEE Transactions on Electron Devices*, vol. 31, no. 9, pp. 1280–1283, 1984.
- [220] A. Der Ziel, "Theory of shot noise in junction diodes and junction transistors," *Proceedings of the IRE*, vol. 43, no. 11, pp. 1639–1646, 1955.
- [221] A. R. Zadeh and S. Nikmehr, "Noise considerations in cascaded single-stage distributed amplifiers," in *Electrical and Computer Engineering, 2006. ICECE'06. International Conference on*. IEEE, 2006, pp. 92–95.
- [222] H. T. Friis, "Noise figures of radio receivers," *Proceedings of the IRE*, vol. 32, no. 7, pp. 419–422, 1944.



- [223] A. Iqbal, “Heterojunction bipolar transistor based distributed amplifiers for fibre optic receiver front-end applications - PhD thesis,” University of Manchester, Tech. Rep., 1999.
- [224] P. K. Hanumolu, G.-Y. Wei, and U.-K. Moon, “Equalizers for high-speed serial links,” *International Journal of High Speed Electronics and Systems*, vol. 15, no. 02, pp. 429–458, 2005.
- [225] X. Huang, J. Shi, J. Li, Y. Wang, Y. Wang, and N. Chi, “750Mbit/s visible light communications employing 64QAM-OFDM based on amplitude equalization circuit,” in *Optical Fiber Communication Conference*. Optical Society of America, 2015, pp. Tu2G–1.
- [226] W. R. Bennett, “Spectra of quantized signals,” *The Bell System Technical Journal*, vol. 27, no. 3, pp. 446–472, 1948.
- [227] J. O’Carroll, R. Phelan, B. Kelly, D. Byrne, L. P. Barry, and J. O’Gorman, “Wide temperature range  $0 < t < 85^{\circ}$  C narrow linewidth discrete mode laser diodes for coherent communications applications,” *Optics Express*, vol. 19, no. 26, pp. B90–B95, 2011.
- [228] Z. Liu, B. Kelly, J. O’Carroll, R. Phelan, D. J. Richardson, and R. Slavík, “Discrete multitone format for repeater-less direct-modulation direct-detection over 150 km,” *Journal of Lightwave Technology*, vol. 34, no. 13, pp. 3223–3229, 2016.
- [229] Z. Liu, T. Xu, G. Saavedra, and P. Bayvel, “448-Gb/s PAM4 transmission over 300-km SMF-28 without dispersion compensation fiber,” in *Optical Fiber Communication Conference*. Optical Society of America, 2018, pp. W1J–6.
- [230] P. H. Pathak, X. Feng, P. Hu, and P. Mohapatra, “Visible light communication, networking, and sensing: A survey, potential and challenges,”

- IEEE Communications Surveys Tutorials*, vol. 17, no. 4, pp. 2047–2077, Fourthquarter 2015.
- [231] S. Wu, H. Wang, and C.-H. Youn, “Visible light communications for 5G wireless networking systems: from fixed to mobile communications,” *IEEE Network*, vol. 28, no. 6, pp. 41–45, 2014.
- [232] D. Karunatilaka, F. Zafar, V. Kalavally, and R. Parthiban, “LED based indoor visible light communications: State of the art,” *IEEE communications surveys and tutorials*, vol. 17, no. 3, pp. 1649–1678, 2015.
- [233] M. Ayyash, H. Elgala, A. Khreishah, V. Jungnickel, T. Little, S. Shao, M. Rahaim, D. Schulz, J. Hilt, and R. Freund, “Coexistence of WiFi and LiFi toward 5G: concepts, opportunities, and challenges,” *IEEE Communications Magazine*, vol. 54, no. 2, pp. 64–71, 2016.
- [234] C.-X. Wang, F. Haider, X. Gao, X.-H. You, Y. Yang, D. Yuan, H. Aggoune, H. Haas, S. Fletcher, and E. Hepsaydir, “Cellular architecture and key technologies for 5G wireless communication networks,” *IEEE Communications Magazine*, vol. 52, no. 2, pp. 122–130, 2014.
- [235] M. B. Rahaim and T. D. Little, “Toward practical integration of dual-use VLC within 5G networks,” *IEEE Wireless Communications*, vol. 22, no. 4, pp. 97–103, 2015.
- [236] L. Feng, R. Q. Hu, J. Wang, P. Xu, and Y. Qian, “Applying VLC in 5G networks: Architectures and key technologies,” *IEEE Network*, vol. 30, no. 6, pp. 77–83, 2016.
- [237] P. A. Haigh, Z. Ghassemlooy, S. Rajbhandari, I. Papakonstantinou, and W. Popoola, “Visible light communications: 170 Mb/s using an artificial neural network equalizer in a low bandwidth white light configuration,” *Journal of Lightwave Technology*, vol. 32, no. 9, pp. 1807–1813, 2014.

- 
- [238] W. Cheung, P. Edwards, and G. French, "Determination of LED equivalent circuits using network analyser measurements," in *Optoelectronic and Microelectronic Materials Devices, 1998. Proceedings. 1998 Conference on.* IEEE, 1999, pp. 232–235.
- [239] S. Miyahara, S. Aono, and Y. Matsumoto, "Preproduction of LED driver for visible light communications and evaluation of response performance of visible LED," *Technical Report of IEICE, ICD2005-44*, pp. 25–30, 2005.
- [240] P. Deng, M. Kavehrad, and M. A. Kashani, "Nonlinear modulation characteristics of white LEDs in visible light communications," in *Optical Fiber Communication Conference.* Optical Society of America, 2015, pp. W2A–64.
- [241] Y.-F. Liu, Y. C. Chang, C.-W. Chow, and C.-H. Yeh, "Equalization and pre-distorted schemes for increasing data rate in in-door visible light communication system," in *Optical Fiber Communication Conference and Exposition (OFC/NFOEC), 2011 and the National Fiber Optic Engineers Conference.* IEEE, 2011, pp. 1–3.
- [242] H. L. Minh, D. O'Brien, G. Faulkner, L. Zeng, K. Lee, D. Jung, Y. Oh, and E. T. Won, "100-Mb/s NRZ visible light communications using a postequalized white LED," *IEEE Photonics Technology Letters*, vol. 21, no. 15, pp. 1063–1065, Aug 2009.
- [243] H. Tanaka, Y. Umeda, and O. Takyu, "High-speed LED driver for visible light communications with drawing-out of remaining carrier," in *Radio and Wireless Symposium (RWS), 2011 IEEE.* IEEE, 2011, pp. 295–298.
- [244] P. A. Haigh, Z. Ghassemloooy, H. Le Minh, S. Rajbhandari, F. Arca, S. F. Tedde, O. Hayden, and I. Papakonstantinou, "Exploiting equalization techniques for improving data rates in organic optoelectronic devices for visible

- light communications,” *Journal of Lightwave Technology*, vol. 30, no. 19, pp. 3081–3088, 2012.
- [245] D. Tsonev, H. Chun, S. Rajbhandari, J. J. McKendry, S. Videv, E. Gu, M. Haji, S. Watson, A. E. Kelly, G. Faulkner *et al.*, “A 3-Gb/s single-LED OFDM-based wireless VLC link using a Gallium Nitride  $\mu$ led,” *IEEE Photon. Technol. Lett.*, vol. 26, no. 7, pp. 637–640, 2014.
- [246] P. A. Haigh, F. Bausi, H. Le Minh, I. Papakonstantinou, W. O. Popoola, A. Burton, and F. Cacialli, “Wavelength-multiplexed polymer LEDs: Towards 55 Mb/s organic visible light communications,” *IEEE Journal on Selected Areas in Communications*, vol. 33, no. 9, pp. 1819–1828, 2015.
- [247] C. L. Tsai and Z. F. Xu, “Line-of-sight visible light communications with InGaN-based resonant cavity LEDs,” *IEEE Photonics Technology Letters*, vol. 25, no. 18, pp. 1793–1796, Sept 2013.
- [248] E. F. Schubert, *Light emitting diodes*. Wiley Online Library, 2003 pp.60-61, 297-299.
- [249] T. Odedeyi and I. Darwazeh, “Bandwidth enhancement technique for bipolar single stage distributed amplifier design,” in *2017 IEEE Asia Pacific Microwave Conference (APMC)*. IEEE, Nov 2017, pp. 833–836.
- [250] —, “Matrix single stage distributed amplifier design for ultra wideband application,” in *24th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Batumi, Georgia, 2017*. IEEE, 2017.
- [251] C. E. Shannon, “A mathematical theory of communication,” *Bell System Technical Journal*, 1948.
- [252] E. F. Schubert, T. Gessmann, and J. K. Kim, *Light emitting diodes*. Wiley Online Library, 2005.

- [253] Y. Salamin, P. Ma, B. Baeuerle, A. Emboras, Y. Fedoryshyn, W. Heni, B. Cheng, A. Josten, and J. Leuthold, “100 GHz plasmonic photodetector,” *ACS Photonics*, vol. 5, no. 8, pp. 3291–3297, 2018.
- [254] S. Assefa, F. Xia, and Y. A. Vlasov, “Reinventing germanium avalanche photodetector for nanophotonic on-chip optical interconnects,” *Nature*, vol. 464, no. 7285, p. 80, 2010.
- [255] J. Michel, J. Liu, and L. C. Kimerling, “High-performance Ge-on-Si photodetectors,” *Nature Photonics*, vol. 4, no. 8, p. 527, 2010.
- [256] K. Ogawa, “Noise caused by GaAs MESFETs in optical receivers,” *Bell System Technical Journal*, vol. 60, no. 6, pp. 923–928, 1981.