Performance and reliability degradation of CMOS Image Sensors in Back-Side Illuminated configuration

Andrea Vici, Felice Russo, Nicola Lovisi, Aldo Marchioni, Antonio Casella, Fernanda Irrera

We present a systematic characterization of wafer-level reliability dedicated test structures in Back-Side-Illuminated CMOS Image Sensors. Noise and electrical measurements performed at different steps of the fabrication process flow, definitely demonstrate that the wafer flipping/bonding/thinning and VIA opening proper of the Back-Side-Illuminated configuration cause the creation of oxide donor-like border traps. Respect to conventional Front-Side-Illuminated CMOS Image Sensors, the presence of these traps causes degradation of the transistors electrical performance, altering the oxide electric field and shifting the flat-band voltage, and strongly degrades also reliability. Results from Time-Dependent Dielectric Breakdown and Negative Bias Temperature Instability measurements outline the impact of those border traps on the lifetime prediction.

***Index Terms*—Backside CMOS Image Sensors, gate oxide traps, performance and reliability degradation, noise and charge pumping measurements, lifetime prediction.**

I. Introduction

CMOS Image Sensor (CIS) is an array of light-sensitive pixels. Each pixel consists of a photodiode (PD) and several control MOSFETs. The two configurations today on the market are sketched in Fig. 1. In the Front-Side Illuminated (FSI) configuration (Fig. 1a) light first couples with the front layers, the metal lines and the intermetal dielectrics. This causes a reduction of the quantum efficiency, especially in the blue and UV region [1–4]. In the Back-Side Illuminated (BSI) configuration (Fig. 1b) the metallizations and dielectric layers lay beyond the PD with respect to the impinging light [5–7]. BSI technology is necessary for high performance at pixels sizes of 1.1 μm and smaller [8].

The manufacturing process of image sensors in BSI technology is highly complicated, since it requires processing steps from both sides of the wafer. The process flows of the FSI-CIS and BSI-CIS are schematically compared in Fig. 1c, where the FSI flow includes only Step 1 while the BSI flow includes three additional steps. As one can see, they share the metal layer deposition (M1-M4), the pads realization with ONO passivation and the first anneal (Step 1). After the end of Step 1, BSI wafers go through the so called BSI loop consisting in: wafer flipping, bonding to a handling wafer, mechanical thinning and the Through-Silicon-Via (TSV) opening (Step 2). Then, pads, ONO passivation (Step 3) and a final ^{2}H annealing (Step 4) are realized. TSV technology for the vertical electrical connection of metal pads is required in order to have optical elements and the bond pads on the same side of the wafer.

Complexity and high manufacturing process cost represent main challenges for an outright use of the BSI technology. In addition, the BSI sensors suffer from long term performance degradation when compared to the FSI. In the last few years, some practical tricks have been proposed to overcome the problem of the BSI reliability degradation. As an example, a backside process engineering was proposed, which allows effective repassivation during the final hydrogen anneal covering the backside of the wafer with a SiN layer acting as hydrogen diffusion barrier [9]. Another approach consists in opening in the back-side of the wafer a suitable pattern of deep-trenches that, passing through the passivation layers and the silicon substrate, land on the inter-level metal dielectrics. These trenches favor the flow of passivating specie (H, ^{2}H) directly to the silicon active area [10]. These empirical solutions aim to achieve acceptable device reliability, but do not shed light on the origin of the reliability degradation.

In this work, we get a deeper insight into the underlying physics of performance and reliability issues of BSI-CIS wafer-level reliability structures performing in-line parameter tests. The paper is organized as follows. Section II reports the results of systematic charge pumping and noise measurements, showing that a density of donor-like border traps is present in the gate oxides of BSI configuration [11], while it is absent in FSI. The oxide trap profile is extracted from experiments. In Section III we perform in-line electrical measurements during the BSI manufacturing process and we demonstrate that those traps are generated during the BSI loop. In the same Section we characterize their impact on MOSFETs electrical performance and successfully simulate current curves by using the extracted oxide trap profile in Sentaurus TCAD. In Section IV we report on the influence of those traps on the lifetime prediction obtained using Time-Dependent-Dielectric-Breakdown (TDDB) and Negative-Bias-Temperature-Instability (NBTI) tests.

II. Charge Pumping and Noise Measurements

The wafer test structures are arranged in the scribe line regions between the individual dies on the wafer. Each scribe line has a width of 100 μm. All the studied transistors (Tx) of the wafer test structures featured a 6.8 nm SiO_2 gate oxide thickness. A schematic cross-section of the devices under test and their location along a scribe line is sketched in Fig. 2.

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A TSV for the vertical electrical connection of metal pads is etched and then filled with aluminium. The TSV passes through the passivation layers and the silicon substrate and finally lands on the first metal line. The TSV opening is realized during the BSI-loop (Step 2 in Fig. 1c).

A. Charge Pumping

Charge Pumping (CP) is a powerful and well known technique for characterizing the Si/SiO_2 interface of MOS systems, measuring the density of interface states. We performed Spectroscopic-CP (S-CP) measurements on n-channel Tx (Area=212.52 μm^2), which allows deriving information on the energy distribution of surface states in a large part of the silicon energy gap [12]. The gate bias was increased from -3.5 V up to 0.5 V, superimposing a train of trapezoidal pulses with amplitude ΔV_G=2.5 V and rise/fall times in the range 8 ns÷10 ms. S-CP consists in monitoring the two values of bulk charge pumping current I_{cp} obtained with two different rise times ($t_{r1}<t_{r2}$) keeping the fall time t_f constant, and vice versa. The difference between the two I_{cp} values is proportional to the energy band gap scanned by the gate signal. Calling spectroscopic signal (S_r) the energy window defined by t_{r1} and t_{r2}, it can be demonstrated that:

$$S_r(t_{r1},t_{r2}) = I_{cp}(t_{r2},t_f) - I_{cp}(t_{r1},t_f) = qfA_{eff}D_{it}(E_{or})k_BT\cdot ln\left(\frac{t_{r2}}{t_{r1}}\right), \quad (1)$$

where q is the electronic charge, f the gate signal frequency, A_{eff} is the effective area and $D_{it}(E_{or})$ the interface density associated to the mean energy level E_{or}, which is the energy window defined by t_{r1} and t_{r2}:

$$E_{or} = E_i + k_BTln\left[\sigma_p v_{th} n_i \frac{|V_T - V_{FB}|}{\Delta V_G}\frac{(t_{r1}+t_{r2})}{2}\right], \quad (2)$$

where σ_p is the capture cross section of holes, v_{th} the thermal velocity of carriers and n_i the intrinsic carrier concentration.

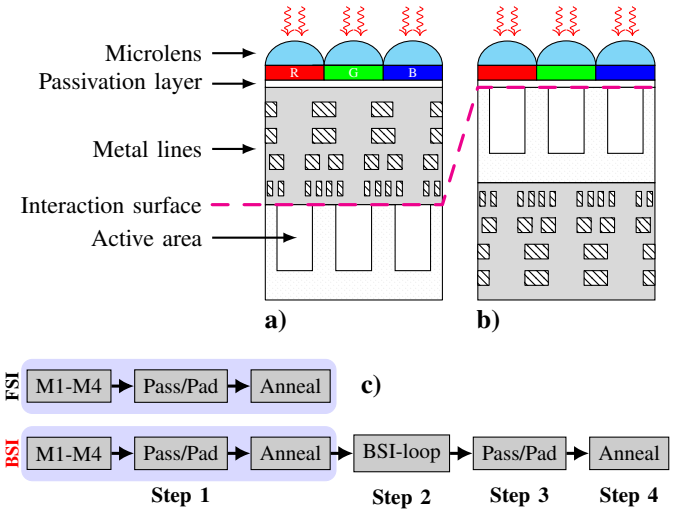

Fig. 1. Sketch of a) Front-Side and b) Back-Side Illuminated Sensors. In c) the process flows of FSI-CIS and BSI-CIS are shown.

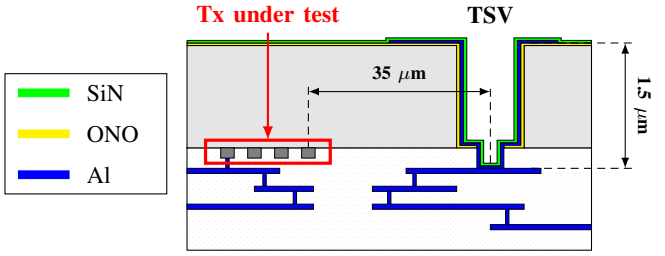

Fig. 2. Cross section of a BSI scribe line where the transistors under test are located. Sketch of the TSV landing onto the M1.

Keeping the rise time t_r constant and changing the fall times between t_{f1} and t_{f2}, one obtains in a similar way:

$$S_f(t_{f1},t_{f2}) = I_{cp}(t_r,t_{f1}) - I_{cp}(t_r,t_{f2}) = qfA_{eff}D_{it}(E_{of})k_BT\cdot ln\left(\frac{t_{f2}}{t_{f1}}\right) \quad (3)$$

and

$$E_{of} = E_i + k_BTln\left[\sigma_n v_{th} n_i \frac{|V_T - V_{FB}|}{\Delta V_G}\frac{(t_{f1}+t_{f2})}{2}\right], \quad (4)$$

where S_f is spectroscopic signal associated to the energy window t_{f1} and t_{f2} , $D_{it}(E_{of})$ the interface density associated to the mean energy level E_{of}, corresponding to the same window and σ_n is the electron capture cross section.
Using $\sigma_n = \sigma_p = \sigma$ =10^{-15} cm^2, in the BSI we found a density of interface states around mid-gap of 10^{10}-10^{11} $cm^{-2}eV^{-1}$, progressively increasing toward the band edges. This is shown in Fig. 3.

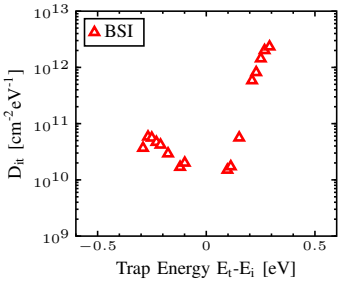

Fig. 3. Interface state density of the BSI configuration extracted from S-CP.

Then, we performed frequency resolved charge pumping (f-CP), which is the extension of the CP technique to low frequency. f-CP can characterize traps located close to the Si/SiO_2 interface [13]. It consists in performing multiple CP measurements at various frequencies and monitoring I_{cp}. If only fast interface traps are present, the recombined charge per cycle $Q_{cp} = I_{cp}/f$ is frequency-independent because all the states in the pumping window can exchange carriers and thus take a part in the charge pumping cycle. If border traps are present, Q_{cp} increases with decreasing frequency, because carriers tunneling from/to silicon can be captured/emitted. In Fig. 4a, the measured I_{cp} values in BSI are drawn as a function of signal frequency, while in Fig. 4b the calculated recombined charge for the two CIS configurations is displayed. In the BSI configuration the charge exhibits an increase below

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the cut-off frequency $f_0 \sim 3$ KHz, while in FSI it remains approximatively flat in the whole frequency range. The trap distribution can be extracted from f-CP data as a function of the maximum tunneling distance x_m by using literature models based on elastic tunnel approximation [14]:

$$D_{bt}(x_m) = -\frac{1}{q\lambda_n A\Delta E}\frac{dQ_{cp}}{dln(f)} \quad (5)$$

and

$$x_m = \lambda_n \cdot ln\left(\frac{\sigma_n n v_{th}}{2f}\right) \quad (6)$$

where A is the gate area, ΔE is the energy swept at the interface and λ_n is the attenuation coefficient predicted by the Wentzel-Kramers-Brillouin (WKB) theory. So, λ_n can be expressed as:

$$\lambda_n = \frac{\hbar}{\sqrt{2m_n\Phi_n}}, \quad (7)$$

being $\hbar$ the reduced Planck's constant, Φ_n the tunneling barrier and m_n the effective electron mass. Calculations using eq. 7 for the Si/SiO_2 system yield λ_n=10 nm. Fig. 5a shows the maximum tunneling distance x_m calculated in our case according to eq. 6 as a function of the measurement frequency, reaching a value $x_m \approx$1.8 nm at f=100 Hz. In Fig. 5b the exponential trap density profile calculated by using eq. 5 and 6 after uniform energy integration along the energy gap is reported. The densities of oxide traps in FSI and BSI are comparable going towards the interface (where the BSI density is 10^{10}-10^{11} $cm^{-2}eV^{-1}$, as shown in Fig. 3), while they differ consistently going inside over a tunneling distance from the interface. The exponential interpolating equation is indicated in the legend of Fig 5b for the BSI. It reaches the value of 2x10^{17} cm^{-3} at 1.8 nm, three orders of magnitude greater than in the FSI configuration. In conclusion, we can state that in BSI a relevant density of border traps is present within a tunneling distance, not found in FSI.

B. Noise Measurements

Noise characterization, especially at low-frequency, represents a real powerful diagnostic tool in MOS devices to investigate the quality of Si/SiO_2 interfaces and defectiveness of gate oxides [15–17]. We performed low frequency noise (LFN) measurements on the drain current in n-channel Tx (Area= 3.6 μm^2), increasing the gate voltage from the threshold condition. As shown in Fig. 6, the normalized Power Spectral Density (PSD) of the drain current S_{I_D}/I_D^2 in BSI shows the typical

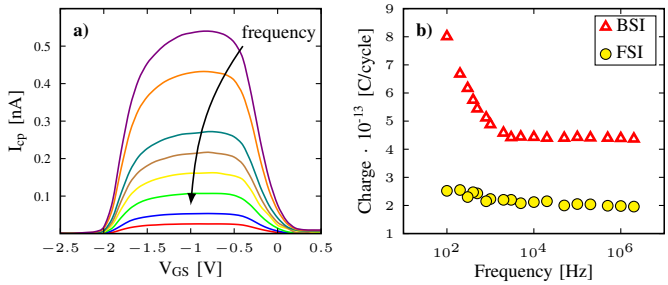

Fig. 4. a) Charge pumping current in BSI. b) Charge per cycle vs. frequency obtained with f-CP.

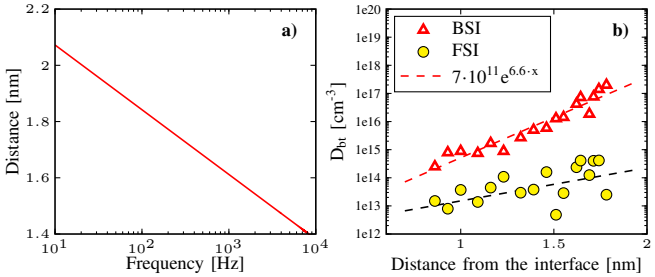

Fig. 5. a) Maximum tunneling distance calculated using eq. 6 assuming σ=1·10^{-15} cm^{-2} and v_{th}=2.2·10^7 cm·s^{-1}. b) Border trap density extracted from f-CP measurements (symbols) as function of the calculated distance from the interface for BSI (red triangles) and FSI (yellow circles).

$1/f^\gamma$ flicker noise trend, with γ ranging between 0.7 and 1.4. According to literature, two different physical models explain

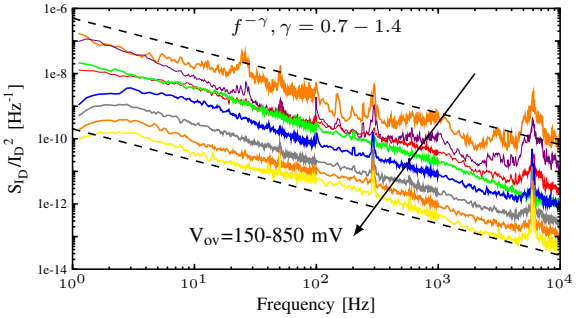

Fig. 6. Normalized spectral density of the drain current noise in BSI configuration as a function of frequency varying the overdrive.

the origin of the $1/f$ noise in the conductance of MOSFETs. The number fluctuation model assumes that the fluctuations originate from the random trapping and detrapping processes of channel carriers in oxide traps located close to the interface [18]. The normalized drain current noise can be thus written as:

$$\frac{S_{I_D}}{I_D^2} = \frac{q^2 k_B T N_t}{f^\gamma W L C_{ox}^2}\frac{g_m^2}{I_D^2}, \quad (8)$$

where $g_m = I_D/(V_G - V_T)$ is the transconductance calculated in linear region, N_t is density of traps in the gate dielectrics within x_m and C_{ox} the gate capacitance per unit area. The frequency exponent γ deviates from 1 if the oxide trap density is not uniform in depth from the interface.

The mobility fluctuations model assumes that the noise is due to fluctuations of the carrier mobility in the channel through the variation of the cross section entering the collision probability, likely due to phonon scattering [19]. By using this approach, the PSD of the drain current can be written as:

$$\frac{S_{I_D}}{I_D^2} = \frac{q\alpha_H \mu_{eff} V_{DS}}{fWL^2 I_D} \quad (9)$$

where α_H is the so called Hooge parameter and μ_{eff} the effective mobility. In our case, the model of carrier number fluctuations holds, as outlined in Fig. 7a where the S_{I_D}/I_D^2 values measured in BSI are displayed against I_D with red symbols, while the solid line represents the $(g_m/I_D)^2$ dependence and the dashed line the $1/I_D$ dependence. The results indicate a prevalence of the mechanism of carrier number fluctuations due to trapping/detrapping, rather than fluctuations of carrier

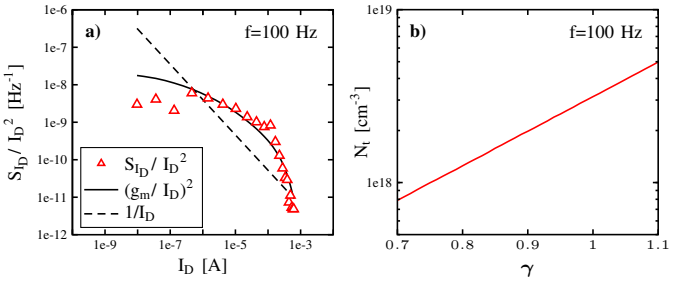

Fig. 7. a) Variation of the normalized drain-current noise versus drain current for the BSI configuration. The solid line indicates a dependence on $(g_m/I_D)^2$, the dashed line the linear dependence on 1/I_D. b) N_t extracted at the same frequency with eq. 8 against the γ coefficient.

mobility. In the carrier number fluctuations (eq. 8) there is one completely free parameter, i.e. the total density of oxide traps within x_m=1.8 nm (N_t), while the other parameter (γ) varies between 0.7 and 1.4 in our case. Plotting the N_t values calculated at 100 Hz against the γ coefficient in that range, one obtains the curve drawn in Fig. 7b for the BSI configuration, where the average density of oxide traps within 1.8 nm is around 10^{18} cm^{-3}. Comparing this result obtained from LFN measurements with the trap distribution obtained with f-CP technique (Fig. 5b) the agreement is very satisfactory, since the density of traps obtained with LFN measurements includes all the contributions, from the interface to 1.8 nm, while the distribution drawn in Fig. 4b increases from the interface to 1.8 nm, where it reaches the value 2x10^{17} cm^{-3}.

Random Telegraph Noise (RTN) in small area transistors is commonly attributed to random capture and release of carriers, which cause a fluctuation between two or more levels in the drain current. We performed RTN measurements on small area n-channel Tx (A=0.064 μm^2) measuring the I_D current in the bias condition V_{DS}=200 mV for different values of V_{ov}=V_G-V_T in the interval 100-300 mV. The experiment lasted 5 seconds. In FSI configuration the RTN could not be detected. In the BSI configuration a switch between two main current levels, namely $I_{D\text{-}high}$=4.625 μA and $I_{D\text{-}low}$=4.575 μA (ΔI_D= 50 nA) was clearly seen. A zoom of the traces are displayed in Fig 8. The stay times in the high and low current levels are indicated, respectively, with τ_h and τ_l.

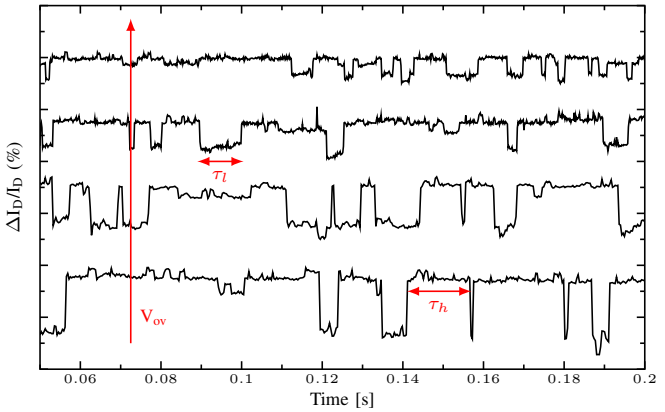

Fig. 8. Zoom of the RTN traces recorded on a BSI sample with V_{DS}=200 mV, varying V_{ov} from 100 to 300 mV.

Drawing the counts of τ_h and τ_l for each value of V_{ov} as a function of time, one finds an exponential distribution, as predicted by theory [20]. This is shown in Fig 9 for V_{ov}=100mV. We define $\overline{\tau}_h$ and $\overline{\tau}_l$ the characteristic times extracted by the exponential fits of the type $\exp(-t/\overline{\tau}_h)$ and $\exp(-t/\overline{\tau}_l)$, drawn in the same figures. Fig. 10a and 10b report the τ_h and τ_l distributions for all the V_{ov} values (symbols) and the relative exponential fits (dashed lines), and in Fig. 10c the ratio between the extracted values of $\overline{\tau}_h$ and $\overline{\tau}_l$ is displayed as a function of the overdrive. Results indicate that τ_h increases with V_{ov} while τ_l decreases, so that the ratio $\overline{\tau}_h/\overline{\tau}_l$ increases as well.

In other words, widening the channel and increasing the number of carriers, I_D stabilizes at the high value. We can conclude that, at each bias conditions, $I_{D\text{-}high}$ is the stable current level, while $I_{D\text{-}low}$ is an unstable level. We are in the presence of a noise source which is appreciable only when the channel carrier number is low and is negligible when the channel carrier number is high, and carriers interact with donor-like traps (positively charged when empty and neutral when an electron is captured).

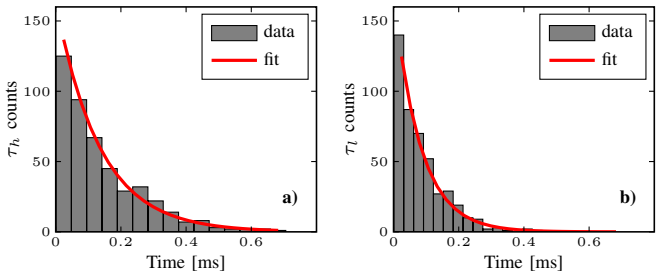

Fig. 9. Distributions of a) high and b) low times for the RTN measured at V_{OV}= 100 mV and their exponential fits.

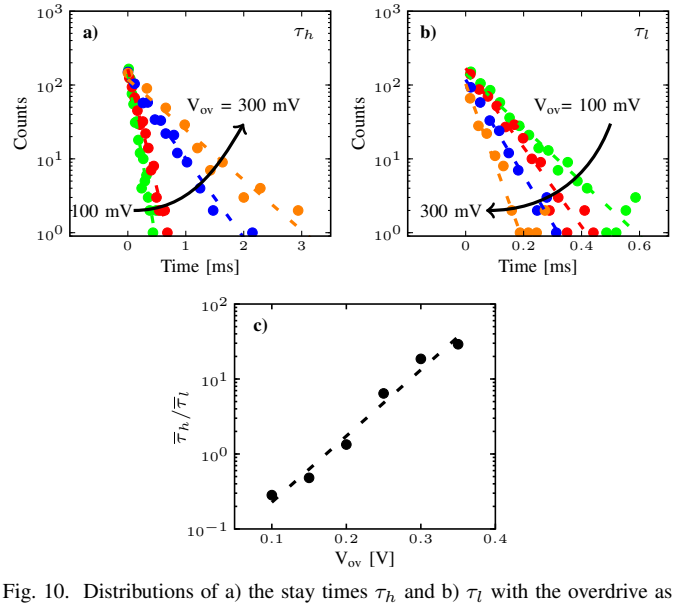

Fig. 10. Distributions of a) the stay times τ_h and b) τ_l with the overdrive as a parameter. c) Ratio between the extracted charachteristic high and low stay times as a function of the overdrive.

III. Characterization before/after the BSI-loop

In this Section, we demonstrate that the additional border traps found in the BSI configuration are created during the

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BSI-loop. To this aim, we stopped the BSI fabrication process before the BSI-loop and, on the same sample, after the BSI loop, performing I_D-V_G and I_G-V_G measurements on the n-channel Tx (Area=3.6 μm^2). It is worth noticing that the BSI process flow interrupted before the BSI-loop coincides with the FSI process flow.

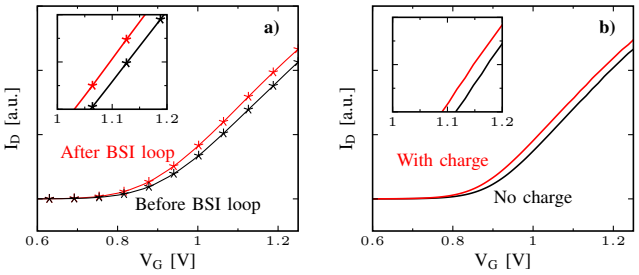

Fig. 11. a) I_D-V_G curves measured during the BSI process flow, after (red line) and before (black line) the BSI-loop. b) I_D-V_G curves simulated with Sentaurus TCAD when the distribution of positive charge drawn in Fig. 5b is present in the oxide (red line) and when no charge is present (black line).

In Fig. 11a the two I_D-V_G curves measured at V_{DS}= 50 mV are reported. As one can see, after the BSI-loop, a leftward translation of the curves takes places indicating the presence of positive charge in the oxide, with a measured shift of the threshold voltage ΔV_T=23 mV. The capacitance per unit area being C_{ox}=5.08x10^{-7} F/cm^2, the additional oxide charge density (ΔQ) after the BSI-loop is ΔQ = 1.6x10^{-8} C/cm^2. To confirm that this result is coherent with the border traps distribution found with f-CP, we performed Sentaurus TCAD simulations, using the structure depicted in Fig. 12. In one case the oxide was ideal with no charge inside, in

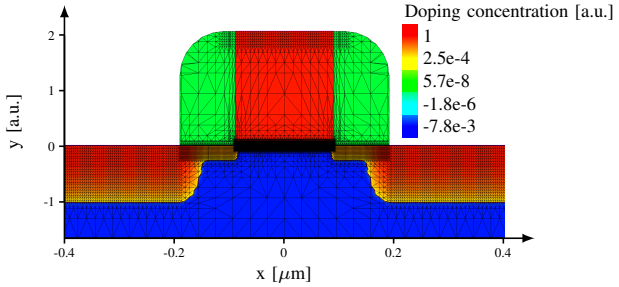

Fig. 12. 2D cross-section of the device and the mesh used in Sentaurus TCAD simulations.

the other case we introduced the exponential distribution of positive charge drawn in Fig.5b up to a distance x_m =1.8 nm from the interface. The simulated I_D-V_G curves are drawn in Fig. 11b. As a result, simulations yielded a shift $\Delta V_{T,sim}$= 25 mV, in agreement with the measured shift. Thus, we can definitely affirm that during the loop of wafer flipping/bonding/thinning/VIA opening an exponential distribution of positively charged border traps is created. The same I_D-V_G curve shift corresponds to a charge centroid of 1.6·10^{-8} C/cm^2 at 1.7 nm from the Si/SiO$_2$ interface.

The I_G-V_G curves are drawn in Fig. 13a. As one can see, after the BSI-loop the low field conduction is lower than before. For example, defining the quantity R as the ratio $I_{G,before}$/ $I_{G,after}$ between the measured current values, at V_G=+1 we find R=6.76. Assuming that the low-field conduction is

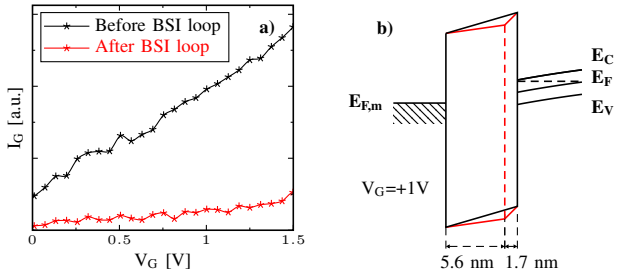

Fig. 13. a) I_G-V_G curves measured during the BSI process flow, before and after the BSI-loop. b) Band diagram of the gate stack at V_G= +1 V when a charge centroid is located at 1.7 nm from the Si/SiO$_2$ interface (red line) and when no charge is present (black).

due to trap-assisted-tunnel (TAT) and having demonstrated that trap density is higher after the BSI-loop than before, we can explain this behavior of the gate current with a reduction of the electric field after the BSI-loop. We made electrostatic simulations of the gate stack before and after the BSI-loop. In the first case, we assumed no charge inside the oxide. In the second case, we introduced a positive charge centroid of 1.6x10^{-8} C/cm^2 at 1.7 nm from the Si/SiO$_2$ interface. Then, we biased the capacitor with V_G= +1 V. The two band diagrams are depicted in Fig. 13b: the black line refers to the oxide bending before the BSI-loop and the red line refers to the oxide bending after the BSI-loop. The trap centroid is outlined with the dashed red line. The potential distortion due to traps has been emphasized for the sake of clarity. The calculated profiles of the electric field in the same bias conditions are reported in Fig. 14a and Fig. 14b versus the distance from the Si/SiO$_2$ interface. In the case of no charge in the oxide (before the BSI loop), the electric field is E_0=1.55 MV/cm. After the BSI-loop, the electric field modifies: electrons injected from the channel first tunnel a barrier of 1.7 nm in an electric field which is 1.8% higher than E_0, but then they have to pass through a much thicker barrier (5.1 nm) with an electric field which is 1.2% lower than E_0. Then, those field profiles have been used for simulating tunnelling at V_G= +1 V, before and after the BSI-loop. The 1.7 nm thick barrier after the BSI loop is tunneled directly, while in the remaining 5.1 nm barrier and in the 6.8 nm thick barrier before the BSI loop we assumed TAT mechanisms. TCAD simulations indicated that adding the charge centroid at 1.7 nm from the Si/SiO$_2$ interface reduces the conduction. Simulations at V_G=+1 V yielded a value of the ratio R_{sim}= 6.56, in excellent agreement with the experiment (R=6.76).

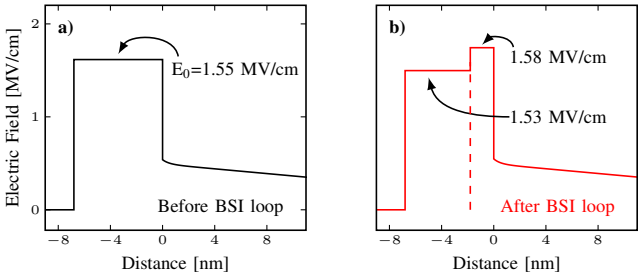

Fig. 14. Electric field profiles calculated in the case: a) no charge in the oxide and b) 1.6·10^{-8} C/cm^2 at 1.7 nm from the Si/SiO$_2$ interface.

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IV. Lifetime prediction using TDDB and NBTI

In this Section, we discuss the prediction of lifetime made after standard reliability tests of TDDB and NBTI on FSI and BSI configurations.

TDDB measurements were performed on n-channel Tx at 125°C, applying a gate stress voltage V_{stress} in the range +7 ÷ +7.6 V.

For each V_{stress} several samples were tested and the time-to-breakdown was measured adopting the three criteria defined in the JEDEC standard JESD92 [21]. For each stress condition, the fit of the Weibull distribution of the time-to-breakdown values gave the corresponding Time-to Failure (TTF). Then, the TTFs were plotted vs. V_{stress} in a log-log scale and the lifetime at the operating gate voltage was extrapolated with a power law (E-model [22]).

NBTI measurements were performed on p-channel Tx at 125°C, applying V_{stress} in the range -3 ÷ -4 V. Again, several Tx were tested. Following the JEDEC standard JESD90 [23], in this case, lifetime is defined as the stress time required to have a 10% shift of the nominal V_T. The V_T shift has a power law dependence on the stress time and the lifetime value at the operating gate voltage could be extrapolated.

Values of lifetime prediction averaged over 20 wafers are shown in Tab. I.

TABLE I
Lifetime predictions for BSI configuration respect to FSI.

	TDDB lifetime (average over 20 wafers)	**NBTI lifetime** (average over 20 wafers)
FSI (a.u)	1	1
BSI/FSI	10^{-3}	0.067

The FSI configuration is our reference and its lifetime is reported in arbitrary units. The BSI lifetime predicted after TDDB test is 0.001 times that of FSI while after NBTI test it is 0.067. To understand the reason of this apparent incongruence, we sketched the band diagram of the BSI gate stack during the TDDB test (V_G=+7 V) in Fig. 15a. The substrate is under strong inversion and the oxide barrier is only 3 nm thick. Therefore, in this case, the additional border traps consistently enhance trap-assisted-tunnel through the barrier respect to the case without traps. In consequence, the oxide degradation is faster in BSI than in FSI. This is the reason why the lifetime prediction based on TDDB is strongly sensitive to the presence of border traps.

Regarding the NBTI on p-channel Tx, the n-doped substrate is under inversion (see Fig. 15b, V_G =-3 V). Surface holes interact with the interface, breaking Si-H bonds and releasing H^+ ions, which tend to migrate into the oxide creating new traps. Here, the hydrogen ions, and not the surface carriers, are mainly responsible for the oxide degradation. So, we expect that Si-H bond breaking has the same rate in FSI and BSI. Border traps can play a minor role in weakening the surrounding bonds and thus favouring both the H^+ driven bond rupture and the creation of new traps around them. This is the reason why the lifetime prediction based on NBTI is less sensitive to the presence of border traps.

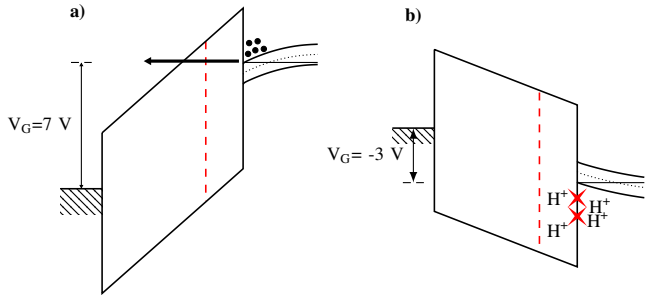

Fig. 15. Band diagram of the BSI gate stack during (a) TDDB test (V_G=7 V), (b) NBTI test (V_G=-3 V).

V. Conclusions

We presented a systematic characterization of wafer-level reliability dedicated test transistors in Back-Side-Illuminated CMOS Image Sensors. Noise and charge pumping measurements denoted the presence of donor-like border traps in the gate oxide, which were absent in the Front-Side Illuminated configuration. The trap density follows an exponential dependence on the distance from the interface and reaches the value $2x10^{17}$ cm^{-3} at 1.8 nm. Electrical measurements performed at different steps during the manufacturing process demonstrated that those border traps are created during the process loop of the Back-Side configuration, consisting of wafer upside flipping, bonding, thinning and VIA opening. Traps warp the oxide electric field and shift the flat-band voltage with respect to the Front-Side configuration, as if a positive charge centroid of $1.6x10^{-8}$ C/cm^2 at 1.7 nm was present in Back-Side configuration, altering the drain and gate current curves. Experimental results were successfully simulated using commercial TCAD once that trap distribution was introduced in the oxide.

We found that the donor-like border traps affect also the Back-Side device long term performance. Time Dependent Dielectric Breakdown and Negative Bias Temperature Instability measurements were performed to evaluate lifetime. As expected, the role of border traps in the lifetime prediction is different in the two cases, but the reliability degradation of Back-Side with respect to Front-Side-Illuminated CMOS Image Sensors is evident in any case.

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