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On Border Traps in Back-Side-Illuminated CMOS Image Sensor Oxides

Andrea Vici, Felice Russo, Nicola Lovisi, and Fernanda Irrera

***Abstract*— CMOS image sensors (CISs) in back-side-illuminated configuration consist of photodiode arrays having metal lines and drive electronics beneath the active region with respect to the device/air interface so that the light reaches the photodiode active region directly. This enhances sensor quantum efficiency but reduces the electrical performance and reliability. The back-side configuration is realized by flipping the wafer upside down, bonding it to a handling wafer, mechanically thinning it, and opening a through-silicon via with a long plasma etch. As a result, gate oxides in back-side CISs show an increased density of donor-like border traps with respect to the conventional front-side-illuminated sensors. In this article, we try to add some information toward the comprehension of the origin and the electrical nature of those traps in back-side gate oxides. To this aim, we performed negative bias temperature instability stress on p-channel MOSFETs during which the traps were filled by holes tunneling from the substrate and then studied the relaxation transients of the drain current after the stress was removed. The characteristic emission times of a few specific levels were obtained at different temperatures. This allowed us to extract values of the trap activation energies, which resulted coherent with hole-capturing E' donor-like centers (trivalent silicon dangling bonds) commonly attributed to ionizing radiation.**

***Index Terms*— Back-side illuminated (BSI) CMOS image sensors (CISs), gate oxide border traps, TDDS.**

I. Introduction

A CMOS image sensor (CIS) is an array of light-sensitive pixels. Each pixel consists of a photo-diode (PD) and several control MOSFETs. In the front-side-illuminated (FSI) configuration [Fig. 1(a)], the light reaches the PD active region through the microlenses, the filters, the passivation layers, the metal lines, and the interdielectric layers [1], [2]. So, the active region containing the PDs typically lies a few micrometers below the device/air interface. Unfortunately, the coupling of light with the front layers exhibits severe drawbacks, which cause a reduction of the maximum available photons and then a quantum efficiency degradation, especially in the blue and UV regions [3]–[6].

Manuscript received November 26, 2019; revised February 4, 2020 and March 2, 2020; accepted March 21, 2020. The review of this article was arranged by Editor L. Pancheri. *(Corresponding author: Andrea Vici.)*

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Digital Object Identifier 10.1109/TED.2020.2983039

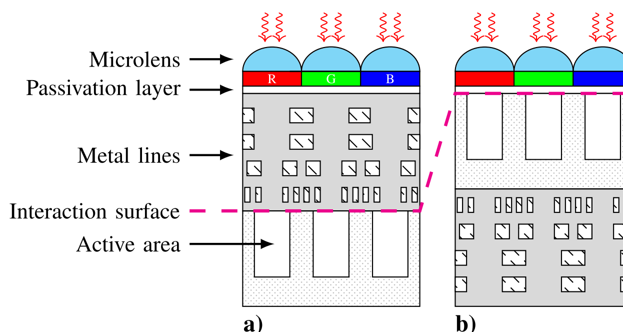

Fig. 1. Cross sections of (a) front-side and (b) BSI CISs.

A few decades ago, to enhance the sensor performances, the back-side-illuminated (BSI) configuration was proposed [7]–[10]. However, due to its prohibitive production cost, the BSI configuration was set aside from the mass production for a long time, however today it is becoming popular with pixel size shrinking. The BSI configuration consists of a device having metal wiring and transistors beneath the active region with respect to the device/air interface [Fig. 1(b)] [1], [8], [11] so that the light reaches the PD active region directly, reducing loss mechanisms and crosstalk. This is achieved adding several steps with respect to FSI manufacturing process. In particular, after the deposition of metal layers, the realization of pads with oxide-nitride-oxide (ONO) passivation, and the first ^{2}H low-temperature annealing, the BSI wafers go through a sequence consisting of flipping upside down, bonding to a handling wafer, mechanical thinning, and a long plasma etch for the through-silicon-vias (TSVs) opening. TSV opening is one of the proven technique to realize the 3-D vertical electrical connection of metal pads [12]. This sequence is here called "BSI loop." After the BSI loop, deposition of pads, ONO passivation, and a final low-temperature ^{2}H annealing are performed.

Unfortunately, despite the optical improvement, the BSI configuration exhibits several drawbacks from electrical and reliability points of view [1], [13], [14]. Some studies have been carried out to understand the reason for this

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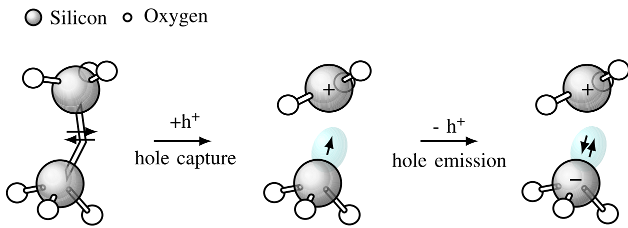

Fig. 2. Schematic representation of the switching mechanism of an E' center in SiO_2, when its interaction with channel holes is probable.

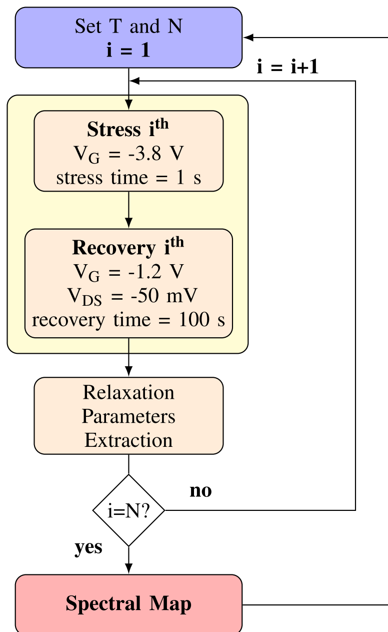

Fig. 3. Process flow of the S/R loop used in the TDDS experiment.

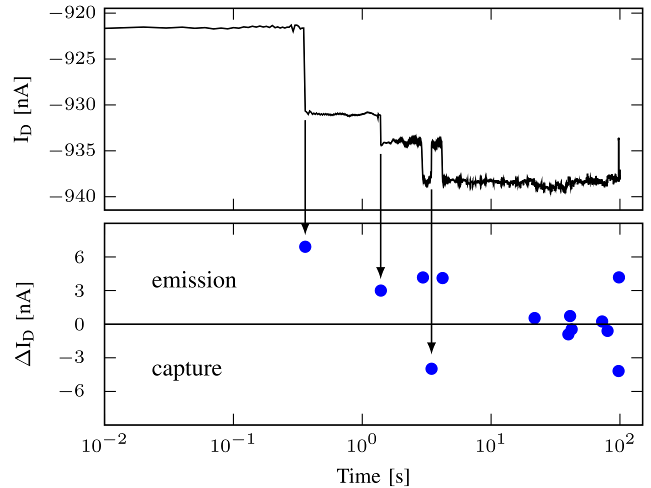

Fig. 4. Typical I_D relaxation trace after the end of an NBTI stress and corresponding ΔI_D versus recovery time plot.

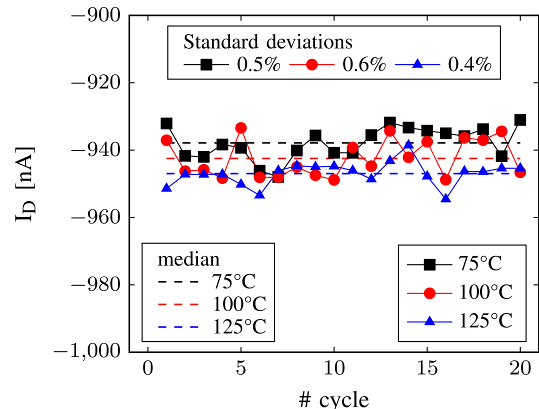

Fig. 5. I_D measured on pMOSFET ($A = 0.045\ \mu m^2$, $t_{ox} = 6.8$ nm) during S/R cycling for three temperatures at $V_{GS} = -1.2$ V and $V_{DS} = -50$ mV.

degradation [15]–[17], but the debate is still going on and further research must be done. In recent studies, we demonstrated that, with respect to FSI, BSI-CIS gate oxides contain an additional distribution of donor-like traps [18], [19]. These traps were located within a tunneling distance from the interface (border/slow traps), reaching a density around 10^{17} cm^{-3} at 1.8 nm.

II. On the Origin of Border Traps in BSI

The nature of traps in amorphous SiO_2 is still not definitely established, however the family of defects linked to an oxygen vacancy is probably the most widely studied. Microscopically, border states are associated with E' centers (trivalent silicon dangling bonds) [20]–[22] which are defects originated on asymmetrically relaxed oxygen vacancies after hole trapping [23], [24]. A schematic representation of the mechanism by which an E' center behaves is depicted in Fig. 2. The precursors of this family of defects are two tetrahedra whose bonding oxygen is missing (left side). This structure can be modified if a hole is captured: one of the silicon atoms holds an unpaired electron on an sp^3 dangling orbital and maintains a tetrahedral configuration, whereas the other holds the trapped hole and relaxes in the plane of its three-remaining oxygen neighbors (in the middle). In this situation, the E' center is positively charged. Now, in the case of hole emission, the E' center switches into its neutral state (right side). So, the E' defect behaves as a donor-like trap. The fact of being positioned close to the Si/SiO_2 interface makes its electrical switch more probable, being the interaction with channel carriers favored by the minimal distance. The origin of this kind of donor traps is commonly attributed to ionizing radiation [25]–[31]. Unfortunately, radiation is quite common in CMOS fabrication flows especially during plasma processes, such as reactive ion etching (RIE), ashing, or plasma-enhanced chemical vapor deposition (PECVD). In our previous articles, we reported that the border traps present in BSI oxides were not found in FSI [18], [19]. This indicates that they are created during those process steps of the BSI manufacturing which are not common to the FSI configuration. As we already mentioned, in the BSI loop, there is a long and aggressive step of plasma etch for the TSV opening, and therefore, we could attribute the creation of donor-like border traps to it. Once the process step responsible for the plasma damage is identified, strategies could be proposed to reduce its effects, by, for example, acting on the recipe parameters (plasma uniformity, wafer, and plasma temperature, etch time) or using circuit solutions (protection diodes and antenna design rules) [32]–[34]. However, this will

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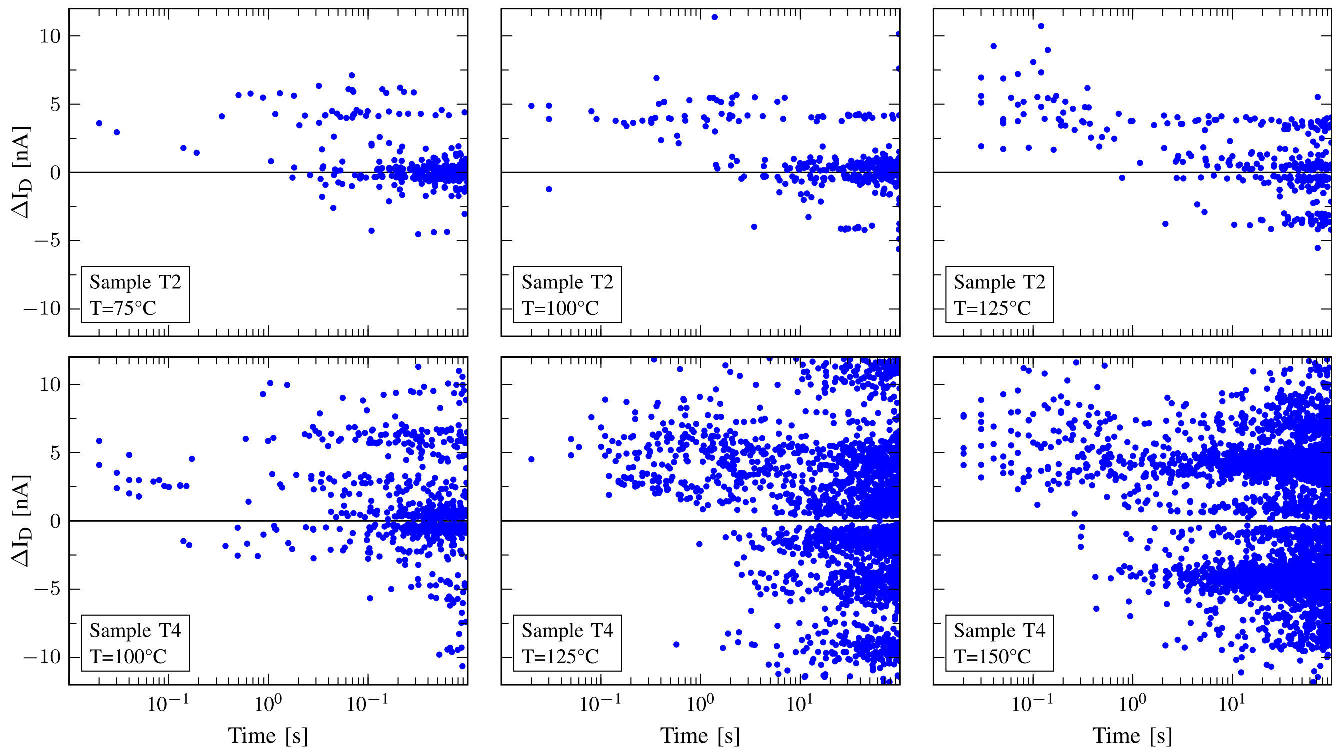

Fig. 6. Spectral maps in a 100 s window of the current steps at $T = 75$ °C, 100 °C, 125 °C, for samples T2 and T4 after N SR cycles, where $N = 25$ for T2 and $N = 40$ for T4.

be demonstrated only through a systematic set of experiments before and after the TSV opening in BSI wafers, which is beyond the target of this article.

III. Time-Dependent Defect Spectroscopy

In this section, we add some information toward the comprehension of the electrical nature of traps created in the BSI manufacturing process, measuring their emission times and activation energies. To this aim, we show the results of a systematic study of time-dependent defect spectroscopy (TDDS) [22]–[24], [32] after negative bias temperature instability (NBTI) stresses performed at different temperatures. NBTI implies stressing p-channel MOSFETs with negative gate voltages at high temperature. This gives rise to absolute sc on-current and transconductance decrease and to absolute threshold voltage (V_T) and subthreshold conduction increase.

A peculiar characteristic of the NBTI is its (partial) recoverability on a sufficiently long time-scale after the stress is removed [23], [24], [35].

Constant gate voltages were applied for 1 s and then the relaxation transients of the drain current (I_D) were monitored for 100 s. In large-area transistors, the I_D relaxation transient is typically referred to follow a sort of logarithmic behavior limited to the experimental time window, although it is not mathematically correct in absolute [24]. This behavior can be modeled as the envelope of the discharge traces of many defects with widely distributed time scales. On the contrary, in small-area transistors, the recovery proceeds with discrete steps occurring at stochastic times due to the discharging of a few oxide traps. The characteristic relaxation times and step heights depend on the trap features [22], [24], [36], [37].

The analysis in this article was carried out on four pMOS transistors coming from a single production quality BSI wafer in 100-nm process technology. Four different sites were chosen in order to monitor within-wafer variability. The selected devices were wafer-level reliability (WLR) test structure, all showing $W = 250$ nm, $L = 180$ nm, and 6.8 nm thermally grown SiO_2 oxide. The 3-D vertical electrical connection of metal pads was realized by using TSV technology. The devices were expected to be small enough to observe the step-like relaxation. Measurements were performed by using a Keithley 2612B Low Current SourceMeter, with a current resolution of 100 fA.

We obtained TDDS of each sample performing several stress/recovery (SR) cycles at different temperatures in the range 75 °C–150 °C, in order to have a good statistics of the stochastic emission/capture processes. The SR loop is described in Fig. 3. First, the temperature and the number of cycles (N) were set. Then, the $i = 1$ SR cycle started. The experimental conditions for stress and recovery are indicated in Fig. 3. At the end of each cycle, the relaxation parameters (emission time τ_e and the current step $\Delta I_D = I_{D,\text{in}} - I_{D,\text{fin}}$) were extracted. Once the N cycles at the set temperature were completed, we could graph the cumulative plots of the step height versus time (the so-called spectral map [22], [35]). Then, the temperature was changed and the SR loop repeated. During the stress, the substrate is in strong inversion ($V_G = -3.8$ V) and the holes capture from the substrate into the border traps is favored. When the stress is

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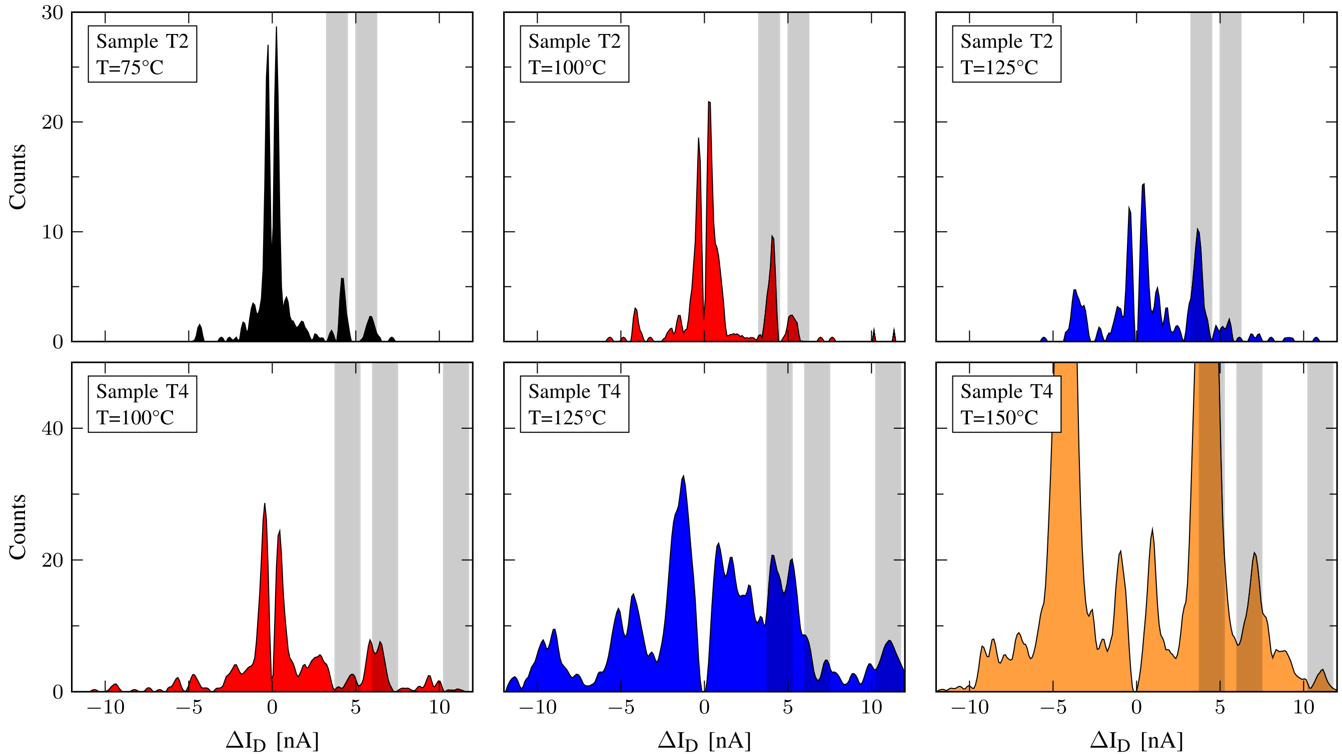

Fig. 7. ΔI_D distributions at different temperatures for samples T2 and T4 after N SR cycles, where $N = 25$ for T2 and $N = 40$ for T4. The preferred ΔI_D levels are outlined with shadowed intervals.

removed, border traps emit holes and the I_D current flowing when the MOSFET is slightly switched on ($V_G = -1.2$ V) is influenced. In the top of Fig. 4, a typical I_D relaxation trace recorded after the ith SR cycle is displayed. The ΔI_D current steps can be clearly observed. In this specific example, after a 400-ms long interval during which I_D keeps constant, several steps down and very few steps up take place. A step down ($\Delta I_D > 0$) corresponds to the emission of a hole from a trap, while a step up ($\Delta I_D < 0$) corresponds to a capture. In the bottom plot of Fig. 4, the ΔI_D and the relative emission/capture time (τ_e/τ_c) corresponding to each current step are displayed. ΔI_D values are representative of the traps involved in the emission/capture processes, since they depend on their position in the channel potential fluctuation induced by randomly located dopants [22]–[24], [35], [36], [38]. So, the fact that more than a unique ΔI_D value is present indicates that more than a unique level is involved. We verified that the 1-s long stress did not damage permanently the oxide. To this aim, we evaluated the I_D measured at the end of each SR cycle as a function of the cycling. Results for a single sample are shown in Fig. 5, all samples behaving similarly. As one can see, the three curves are essentially constant, slightly deviating from their median values. Standard deviations are reported inside the plot. Thus, no trap creation occurs during the stress but only trap filling. Fig. 6 shows the spectral maps of two representative samples named T2 and T4, at three different temperatures. Sample T4 showed a particularly pronounced sensitivity to temperature and for this reason we report the maps up to 150 °C. Apart from fluctuations around 0, several ΔI_D peaks corresponding to capture and emission processes

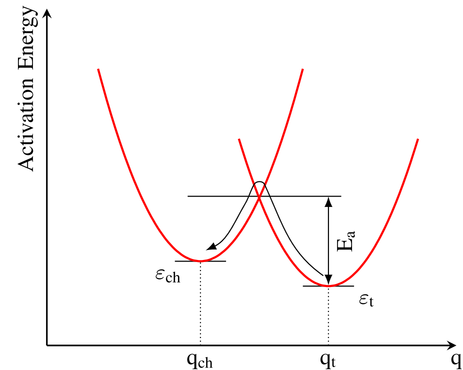

Fig. 8. Configuration coordinate diagram for hole emission from state q_t to q_{ch} (after [39]).

can be clearly recognized. Other typical features are that at shorter times (up to 1 s approximately), many more emission events than capture occur and that the tendency to react with the same level is kept in time. The effect of temperature is better outlined in the ΔI_D distributions at the end of the SR cycling, displayed in Fig. 7: increasing temperature, the overall number of emission, and capture events increases and the first is always higher. In the same figure, the preferred ΔI_D levels are outlined with shadowed intervals, for each sample and temperature. They keep approximately constant with temperature.

Studying the behavior of τ_e of a trap with temperature, it is possible to extract its activation energy (E_a). The activation energy for emission can be defined as the energy barrier that the trapped carrier must overcome to be emitted. Following the

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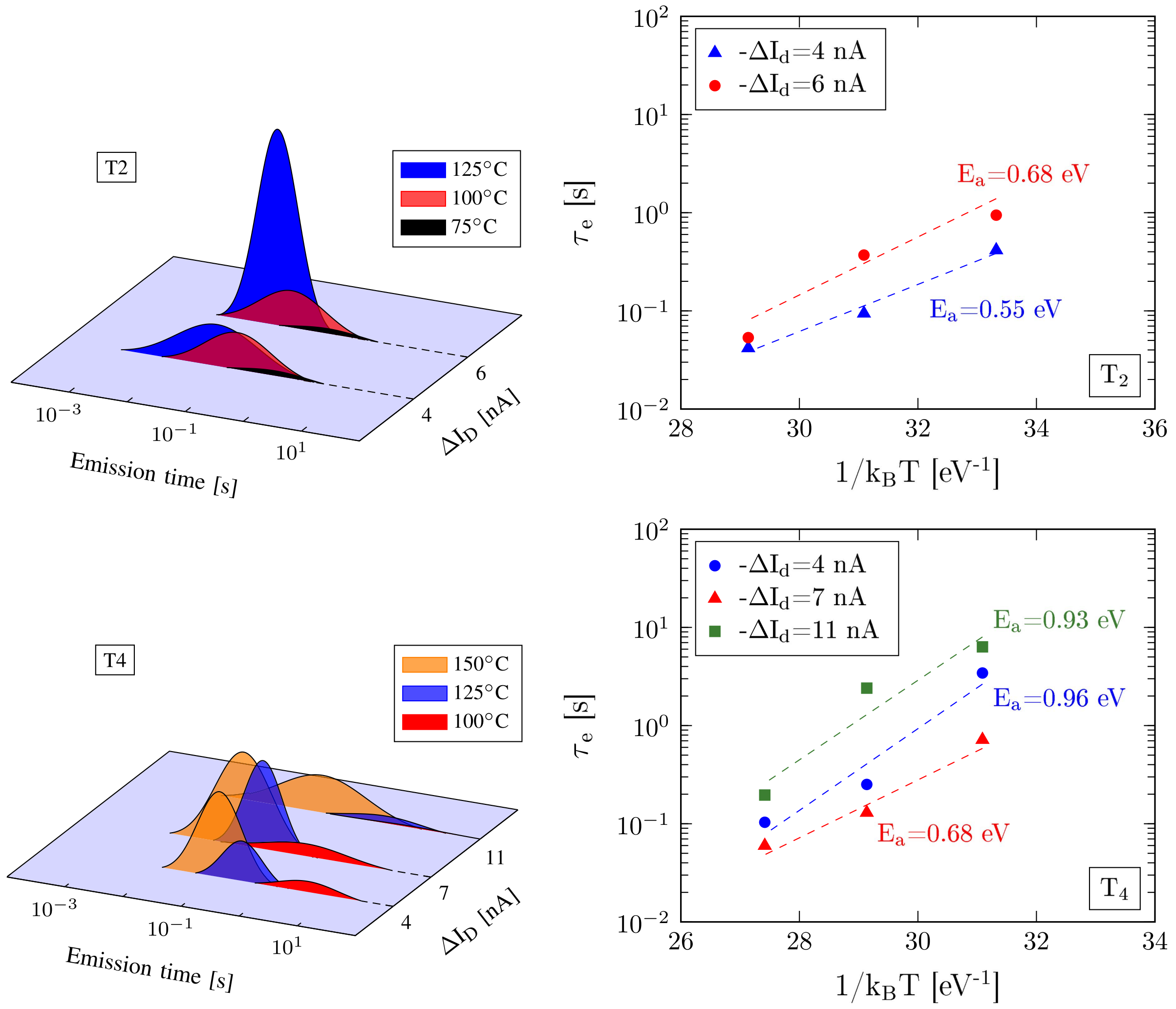

Fig. 9. Left: log-normal distributions of ΔI_D at different temperatures, for example, T2 and T4. Right: extraction of the activation energy of the traps involved in the SR experiment for the same samples, obtained using (1).

literature models based on nonradiative multiphonon (NMP) model [23], [24], [39], E_a can be explained using the configuration coordinate diagram depicted in Fig. 8, where the two parabolas represent the state coordinate of the valence band in the channel (q_{ch}) and of a defect in the gate oxide (q_t). In order to get a transition from state q_t (with energy ε_t) to state q_{ch} (with an energy ε_{ch}), the trapped hole must overcome the energy barrier E_a. The average emission time $\langle\tau_e\rangle$ is the inverse of the transition rate $k_{t\to\text{ch}}$ from state q_t toward q_{ch} and can be written as

$$k_{t\to\text{ch}} = p v_{\text{th}} \sigma \cdot e^{-E_a/k_{\text{BT}}} = \frac{1}{\langle\tau_e\rangle} \tag{1}$$

where p is the hole density, v_{th} the electron thermal velocity, and σ the trap cross section. Starting from our experiments, we derived $\langle\tau_e\rangle$ of each level as that time corresponding to the average value of the log-normal distribution of ΔI_D, at each temperature. In order to distinguish and identify the most prominent peaks, we developed a reliable algorithm in MATLAB. For each sample, those peaks which recurred in the same range ($\pm$0.5 nA) at all the investigated temperatures were identified as preferred. The algorithm results indicated as preferred levels $\Delta I_D = 4$ and 6 nA for sample T2 and 4, 7, 11 nA for T4.

The 3-D plots of the log-normal distributions are shown on the left of Fig. 9, for samples T2 and T4. Then, the calculated emission times of each level can be drawn as a function of the temperature in Arrhenius-like plots, as shown on the right of Fig. 9. Now, using (1), it is possible to extract the activation energies of the traps involved in the SR experiment. As a result, the activation energies of the two main traps in T2 are $E_a = 0.55$ eV and $E_a = 0.68$ eV, while in T4 the three traps feature $E_a = 0.68$, 0.93, and 0.96 eV. Activation energies of border traps in the range 0.5–1 eV were already reported by other authors [36]–[38], [40] and attributed hole capturing to hydrogen bridges and E' centers. Indeed, even if numerous paramagnetic centers have been observed in SiO_2, the results of several density functional theory calculations indicate these defects to be very likely candidates for hole trapping in SiO_2 [37], [41].

IV. Conclusion

Gate oxides in BSI CISs showed an increased density of donor-like border traps with respect to FSI sensors. TDDS has

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been performed on WLR dedicated test p-channel MOSFETs of a production quality BSI CIS wafer, monitoring relaxation of the drain current after NBTI stress performed at different temperatures. The step-like relaxation behavior typical of small size samples was found. Some features were common to all the devices studied. In particular, the interaction of holes with a few specific levels was clear and did not change with time and temperature, the emission events (ΔI_D steps down) occurred always before capture events (ΔI_D steps up), temperature increased the trap activity. The average emission times of each reacting level were calculated as a function of temperature to extract the corresponding activation energy, according to nonradiative multiphonon model. As a result, the activation energies of the reacting traps lay in the range 0.5–1 eV, coherently with hole capturing E' donor-like centers (trivalent silicon dangling bonds in the oxide). The origin of this kind of centers is commonly attributed to ionizing radiation during plasma processes of CMOS fabrication. We can, therefore, conclude that those donor-like BSI border traps are probably E' centers created during the etch step for the TSV opening.

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