A two-stage switched-capacitor integrator for high gain inverter-like architectures

P. Bruschi, A. Catania, S. Del Cesta, and M. Piotto

***Abstract*—A discrete-time, switched capacitor integrator is presented. The integrator is based on a two-stage architecture where the first stage converts the input voltage into a charge that is accumulated into the second stage. The main strength of the proposed circuit is a higher dc gain with respect to previous solutions, making it optimal for low-voltage inverter-like integrators. A further advantage is the fact that, in contrast with existing solutions, the output voltage is valid across the whole clock cycle. Theoretical analysis of the circuit is performed to calculate the dependence of the integrator dc gain and input-referred offset voltage on the corresponding parameters of the constituting amplifiers. Discrete-time simulations are performed to estimate the gain and phase error with respect to an ideal integrator. The results of electrical simulations performed on an inverter-like prototype, designed with the UMC 0.18 μm CMOS process, are presented to show the impact of non-idealities from the amplifiers and switches.**

***Index Terms*—Switched capacitors, discrete-time integrator, finite gain effects, inverter-like, high dc gain, low voltage.**

I. Introduction

The discrete-time integrator (DTI) is the foundation of most switched capacitor (SC) circuits, including filters [1], control loops and delta sigma (Δ–Σ) analog-to-digital converters (ADCs) [2]. Following the trend for low supply voltages and compact architectures, several examples of inverter-like DTIs have been recently proposed. Inverter-like circuits [3] are marked by (i) virtually rail-to-rail output swing; (ii) extreme compact area; (iii) optimum transconductance over supply current ratio (g_m/I_{supply}), allowing for optimal tradeoff between power consumption and speed or input thermal noise characteristics; (iv) absence of internal nodes affecting the frequency response.

A major limitation of an inverter-like DTI is the reduced gain of the amplifier, which results in reduced dc gain of the integrator. This effect is particularly detrimental in Δ–Σ ADCs where low dc gains cause resolution loss, onset of dead-zones and accuracy degradation (e.g. gain error) [2,4,5].

In the traditional parasitic insensitive SC-DTI [1], the integrator dc gain coincides with the amplifier gain (A_0). Several alternative DTI topologies that implement correlated double sampling (CDS) to reject offset and low frequency noise while providing a dc gain of the order of $(A_0)^2$ have been proposed [6,7]. However, the DTI dc gain achievable with the approaches in [6,7] might not be sufficient for high accuracy ADCs, when sub-micron channel lengths are used. It is worth noting that the absence of a non-inverting terminal prevents trivial cascading of inverters to obtain larger gains. Nevertheless, these topologies have been used in all the examples of inverter-like Δ–Σ ADCs that, in our knowledge, have been proposed over the last years [8-11].

In this work, we propose a novel two-stage integrator that reaches a dc gain close to $(A_0)^3$, performs CDS and, differently from solutions in [6,7] maintains also a valid output voltage across the whole clock cycle. These characteristics, together with low power consumption, make the proposed approach particularly interesting for Δ-Σ-based sensor interfaces [12]. The principle of operation of the integrator was already embedded into the fully differential feedback network of a recently proposed band-gap voltage reference [13]. In this paper, we apply this concept to the design of a single-ended SC-DTI, showing the strength and limitations of the approach by means of discrete-time simulations and electrical simulations, performed on an inverter-like prototype designed with the UMC 0.18 μm CMOS process.

II. Architecture of the Proposed Integrator

A. Circuit topology and operating principle

The proposed integrator is shown in Fig.1. Differently from previous solutions, the circuit uses two amplifiers, indicated with A_1 and A_2. This is not a significant complexity increase in the case that A_1 and A_2 are simple CMOS inverters.

The integrator output is V_{o2}, while V_1 and V_2 are its inverting and non-inverting inputs. Labels "1" and "2" in Fig.1 indicate the switch state in the two corresponding operating phases. In single supply implementations, the reference node (indicated with a small downward triangle) is generally a floating rail distinct from either V_{dd} or the power supply ground (*gnd*).

Submitted on July 17, 2018

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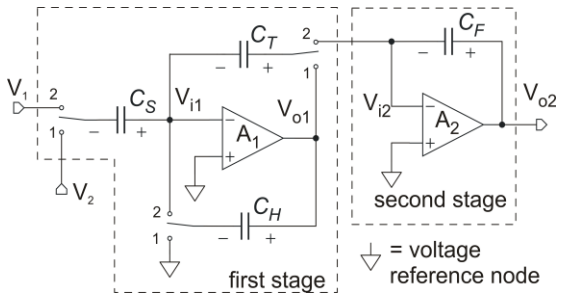

Fig. 1. Schematic view of the proposed integrator. V_{o2} is the integrator output. Other relevant voltages are indicated.

The circuit consists of two stages, indicated in Fig. 1. In phase 1, the first stage stores a charge proportional to V_2-V_1 into C_T. In phase 2, this charge is transferred to the second stage (i.e. into capacitor C_F) producing a proportional increment of the output voltage V_{o2}. The first stage uses the topology of [14] to perform the mentioned voltage-to-charge conversion with reduced sensitivity to A_1 gain and offset voltage.

B. Detailed circuit analysis

The analysis described in this section does not take into account the effects of parasitic input capacitances, amplifier non-linearity, finite bandwidth and switch non-idealities. Finite gain effects and input offset voltages are intrinsically included by the presence of non-zero amplifier input voltages, V_{i1},V_{i2}. (imperfect virtual ground). Fig.2 shows the convention used in the following part of this document to indicate the clock phases. All phases have a duration of $T/2$, where T is the clock period (f_{ck}=1/T is the clock frequency). Voltage polarities are specified in Fig.1 by +/– symbols. With $V_X^{(i)}$ we indicate generic voltage V_X sampled at the end of phase "i".

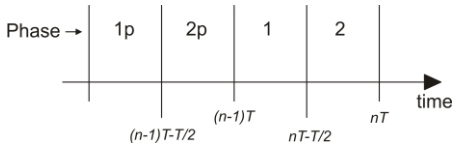

Fig. 2. Conventions used to indicate the phase sequence across two clock periods.

Let us start by considering the transition from phase 2p to phase 1. By standard analysis based on charge conservation, voltage V_{01} can be expressed by:

$$V_{o1}^{(1)} = V_{i1}^{(1)} + V_{i2}^{(2p)} - V_{i1}^{(2p)} + \frac{C_S}{C_T}\left(V_1^{(2p)} - V_2^{(1)}\right) + \\ + \frac{C_S}{C_T}\left(V_{i1}^{(1)} - V_{i1}^{(2p)}\right) \tag{1}$$

In the following 1→2 transition, voltage V_{02} becomes:

$$V_{o2}^{(2)} = V_{i2}^{(2)} + V_{CF}^{(1)} + \frac{C_T}{C_F}\left(V_{CT}^{(2)} - V_{CT}^{(1)}\right) \tag{2}$$

where V_{CF} and V_{CT} are voltages across capacitors C_F and C_T, respectively. Considering that no charge flows across C_F in the 2p→1 transition, then it can be simply found that:

$$V_{o2}^{(2)} = V_{i2}^{(2)} + V_{o2}^{(2p)} - V_{i2}^{(2p)} + \\ + \frac{C_T}{C_F}\left[\left(V_{i2}^{(2)} - V_{i1}^{(2)}\right) - \left(V_{o1}^{(1)} - V_{i1}^{(1)}\right)\right] \tag{3}$$

Using (1), the following expression for the integrator output in phase 2 can be finally found:

$$V_{o2}^{(2)} = V_{o2}^{(2p)} + \frac{C_S}{C_F}\left(V_2^{(1)} - V_1^{(2p)}\right) + \left(1 + \frac{C_T}{C_F}\right)\left(V_{i2}^{(2)} - V_{i2}^{(2p)}\right) - \\ - \frac{C_T}{C_F}\left(V_{i1}^{(2)} - V_{i1}^{(2p)}\right) - \frac{C_S}{C_F}\left(V_{i1}^{(1)} - V_{i1}^{(2p)}\right) \tag{4}$$

Notice that V_{i1} and V_{i2} are present only as difference of samples taken at different instances. As a result, flicker noise and offset contributions that contaminate V_{i1} and V_{i2} are reduced by a CDS mechanism. Voltage V_{o2} is maintained across the following phase 1.

Voltage V_{o1} in phase 2 can also be easily found:

$$V_{o1}^{(2)} = V_{i1}^{(2)} + V_{o1}^{(1)} + \frac{C_S}{C_H}\left(V_{i1}^{(2)} - V_{i1}^{(1)}\right) + \frac{C_S}{C_H}\left(V_2^{(1)} - V_1^{(2)}\right) + \\ + \frac{C_T}{C_H}\left(V_{i1}^{(2)} - V_{i1}^{(1)}\right) + \frac{C_T}{C_H}\left(V_{o1}^{(1)} - V_{i2}^{(2)}\right) \tag{5}$$

C. Ideal behavior

In the ideal case, the amplifiers have (i) infinite gain, (ii) zero offset voltage and (iii) zero input noise voltage. In these conditions, V_{i1} and V_{i2} are zero in all phases and (4) becomes:

$$V_{o2}(nT) = V_{o2}(nT - T) + \frac{C_S}{C_F}\left[V_2\left(nT - \frac{T}{2}\right) - V_1\ (nT - T)\right] \tag{6}$$

where we have considered that the output voltage is sampled at the end of phase 2. In the z-domain, (6) becomes:

$$V_{o2}(z) = H_I(z)\left[V_2(z)z^{+1/2} - V_1(z)\right] \tag{7}$$

where

$$H_I(z) = \frac{C_S}{C_F}\frac{z^{-1}}{1 - z^{-1}} \tag{8}$$

is the ideal integrator function.

Differently from the circuits in [6,7], the transfer function referred to the inverting input includes a one-cycle delay. This means that the proposed circuit performs forward Euler integration instead of backward one. Conversely, a half-cycle delay is present in the non-inverting transfer function, in conformity with traditional DTIs [6,7].

D. Finite dc gain and offset voltage.

Exact calculation of the transfer function taking into account the finite gain of the amplifiers is very complicated, and is beyond the scope of this paper. We will limit our analysis to the case where V_1 and V_2 are dc voltages and the output voltage V_{o2} has reached the final asymptotic value. In these conditions, voltages do not vary from a clock cycle to the next one. As a result, (4) becomes:

$$V_{i1}^{(1)} - V_{i1}^{(2)} = V_2 - V_1 \tag{9}$$

Indicating the input offset voltages of A_1 and A_2,with V_{io1} and V_{io2}, respectively, the following expressions follow:

$$V_{o1} = -A_1\left(V_{i1} + V_{io1}\right);\ V_{o2} = -A_2\left(V_{i2} + V_{io2}\right) \qquad (10)$$

By means of elementary but tedious calculations it is possible to solve the equation set formed by (1), (5), (9) and (10), finding the dc output voltage:

$$V_{o2}^{(2)} = A_2\left(A_1^2 + A_1 + 1\right)\left(V_2 - V_1\right) + V_{io1}A_1A_2 - V_{io2}A_2 \qquad (11)$$

Equation (11) proves that the dc gain exceeds $(A_1)^2A_2$. For $A_1=A_2=A_0$, we get a dc gain of the order of $(A_0)^3$.

The effective input referred offset voltage of the integrator ($V_{io\text{-}rti}$) can be easily derived from (11):

$$V_{io-rti} = -\frac{V_{io1}A_1 - V_{io2}}{A_1^2 + A_1 + 1} \cong -\frac{V_{io1}}{A_1} + \frac{V_{io2}}{A_1^2} \qquad (12)$$

Therefore, the integrator input offset is dominated by the input offset of the first amplifier, attenuated by A_1 gain.

III. Discrete-time simulations

Equations (1),(3) and (5) have been used to setup an *ad hoc* iterative discrete-time simulator, written using the Scipy scientific modules of the Python language. The simulator has been used to calculate the impulse response, from which the discrete-time frequency response of the integrator has been estimated by means of the Fast Fourier Transform (FFT). The only non-ideality taken into account is the finite gain of the amplifiers, set to 28 (29 dB) for both A_1 and A_2, in conformity with the actual gain of the amplifiers used in the prototype described in next section. Other simulator parameters are C_S/C_F, C_T/C_S and C_H/C_S ratios. The first ratio (C_S/C_F) acts as a multiplier factor in the ideal integrator response given by (8), hence the ideal unity gain frequency f_0 is:

$$f_0 = \frac{1}{\pi T}\arcsin\left(\frac{C_S}{2C_F}\right) \cong \frac{1}{2\pi T}\frac{C_S}{C_F} \qquad (13)$$

The other two-capacitance ratios affect the transfer function only in the case of finite gain.

Fig. 3 shows the simulated magnitude and phase response of the integrator for different C_S/C_F ratios. In order to achieve a sufficient frequency resolution the impulse response was simulated over an interval of 4×10^6 cycles. Notice that the dc gain practically coincides with the ideal value (87.14 dB), given by (11). The phase response is close to 90° over two or three decades, depending on the C_S/C_F ratio. The phase decrease at high frequencies is due to the delay term (z^{-1}) which is present in the ideal response (8), whereas the phase increase at low frequencies is the effect of finite gain.

Magnitude and phase errors with respect to (8) are highlighted in Fig. 4. The magnitude error exhibited at high frequencies is mainly due to the finite gain of A_2, which prevents the charge in C_T from being completely transferred to C_F in the 1→2 phase transition. Due to this error, the unity gain frequencies of the DTI are slightly smaller than predicted by (13), as shown in Table I, where the phase error at f_0, calculated with respect to (8) is also reported. The effect of the C_T/C_S ratio is shown in Fig. 5 where the phase and magnitude error at f_0 are shown for the case C_S/C_F=1/4.

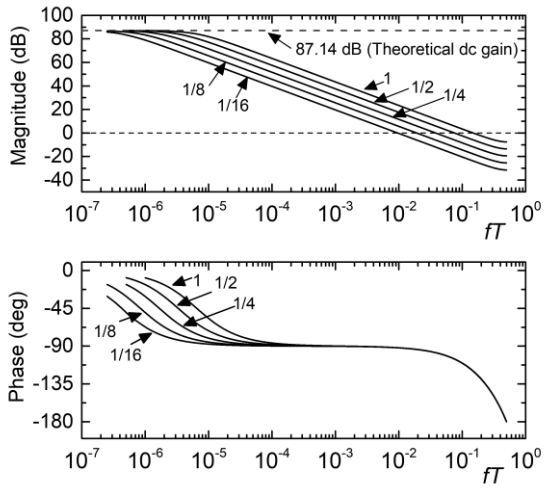

Fig. 3. Discrete-time simulation of the magnitude (top) and phase (bottom) response of the proposed DTI for different C_S/C_F ratios, indicated in the figure. Other settings are: $A_1=A_2=28$, $C_T/C_S=C_H/C_S=1$.

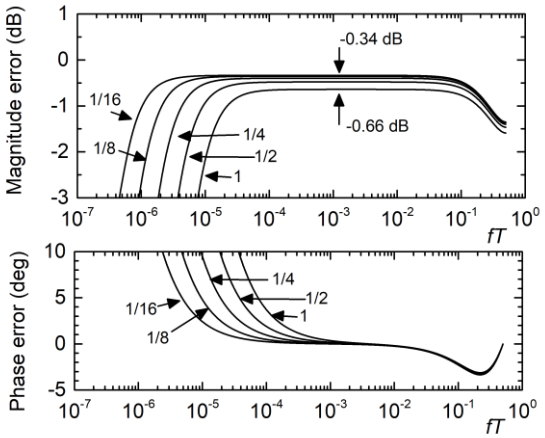

Fig. 4. Magnitude and phase error with respect of the ideal forward Euler discrete-time integrator described by equation (8) for the same parameters of Fig.3. Labels indicate different C_S/C_F ratios.

TABLE I. Unity gain and phase errors for different Cs/Cf ratios

C_S/C_F	1/16	1/8	1/4	1/2	1
f_0 error (%)	-3.8	-4.1	-4.6	-6.4	-11
Phase error at f_0	-0.24°	-0.48°	-0.94°	-1.74°	-2.78°

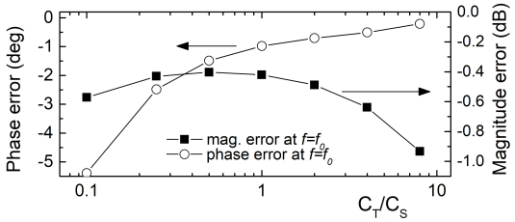

Fig. 5. Magnitude and gain errors with respect to the C_T/C_S ratio for C_S/C_F=1/4 and C_H/C_S=1.

Notice that increasing the C_T/C_S ratios reduces the phase error. Finally, simulations performed by varying the C_H/C_S ratio

showed that C_H has negligible effects for $f \leq f_0$.

IV. Simulation of an Inverter-Like Prototype

The inverter-like prototype is shown in Fig.6. INV-1,2,3 are identical CMOS inverters. All the switches are implemented with complementary p-n transmission gates ($TG_{1\text{-}6}$). Device aspect ratios are reported in Fig.6 caption. Dummy switches are placed on critical nodes to compensate for charge injection.

INV-1,2 play the role of A_1 and A_2, while INV-3 is used to create a floating rail at potential V_{ref}, which coincides with the inverter inversion voltage (V_{inv}). The analysis of previous sections is applicable to the circuit in Fig.6 if all voltages are referred to V_{ref} and V_{o1}, V_{o2} remain within the linearity range of the inverter output characteristic.

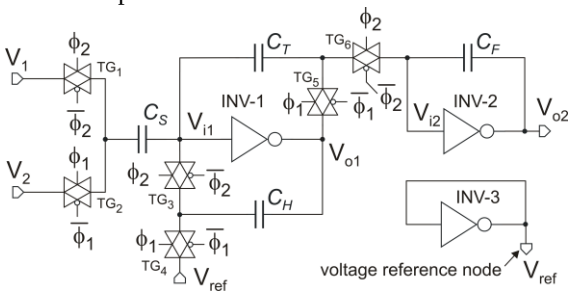

Fig. 6. Schematic view of the proposed integrator, implemented with inverter-like amplifiers. MOSFET aspect ratios (width/length, in microns) are as follows: 1.8/0.18 (nmos), 7.2/0.18 (pmos) for the inverter and 0.72/0.18 (nmos) and 2.88/0.18 (pmos) for the transmission gate.

The circuit has been designed with the 0.18 μm CMOS process of UMC. Capacitors C_S, C_T and C_H have been set to 1 pF whereas C_F is varied from 1 pF to 16 pF to produce the same C_S/C_F ratios as in previous section.

The inverter has been designed to allow operation up to clock frequencies of 1 MHz with the mentioned capacitance values and a supply voltage of 0.9 V. Aspect ratios are tuned to obtain $V_{ref} \cong V_{dd}/2$. The dc gain of the inverters, estimated for $V_{in}=V_{ref}=V_{inv}$, is 28 (~29 dB).

The circuit in Fig. 6 has been simulated using the Spectre™ (Cadence) electrical simulator. Periodic state AC simulations (PAC) have been performed since it is not feasible to simulate the impulse response over a time interval long enough to collect the same number of samples as in the discrete-time simulations of previous section. Notice that the high dc gain of the DTI, combined with residual charge injection contribution, hinders the achievement of a periodical stationary state. To overcome this difficulty, the closed loop test-bench of Fig. 7 has been used. An ideal feedback network with gain β is implemented with the voltage-controlled voltage source E_1. The output voltage is sampled at the end of phase 2 and held by the ideal switch S_H and capacitor C_M. E_2 prevents C_M from loading the integrator. The relevant waveforms are represented in the bottom right corner of Fig.7. Neglecting the duration of phase 3 pulses (=0.01 T), the time-continuous frequency response $H_{CL}(\omega) = V_{out}/V_{in}$ of the test-bench is tied to the discrete-time frequency response of the DTI, $H_I(e^{j\omega T})$, by:

$$H_{CL}(\omega) = \frac{e^{j\frac{\omega T}{2}} H_I\left(e^{j\omega T}\right)}{1+\beta H_I\left(e^{j\omega T}\right)}\left[e^{-j\frac{\omega T}{2}}\,\mathrm{sinc}\left(\frac{\omega T}{2}\right)\right] \qquad (14)$$

where $\mathrm{sinc}(x)=\sin(x)/x$ and $\omega=2\pi f$ with $f<f_{ck}/2$.

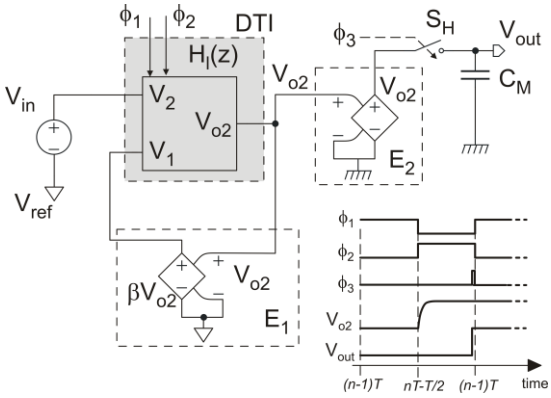

Fig. 7 Test bench used to simulate the integrator frequency response with sketch of the main waveforms (bottom-right).

Inverting (14), $H_I(e^{j\omega T})$ was estimated from $H_{CL}(\omega)$, obtained with the PAC simulations. The feedback factor β was set to 10^{-3} to reduce the sensitivity to the simulator accuracy. Fig.8 shows the discrete-time frequency response (magnitude and phase) of the integrator in Fig.6, obtained with a clock frequency of 1 MHz, V_{dd}=0.9 V and three different C_S/C_F ratios. The dc gain is around 85 dB, which is slightly lower than the theoretical limit. Preliminary investigation showed that this discrepancy is due to parasitic charge transfer caused by the drain-body and source-body capacitances of the transmission gates.

The curves in Fig.9 represent the magnitude and phase difference between the electrical simulations performed on the prototype of Fig.6 and the discrete-time simulations of previous section (Fig.3), for the particular case C_S/C_F=1/4, and different combinations of supply voltage, clock frequency and C_S value. Starting from the case f_{ck}=1 MHz and V_{dd}=0.9 V, the gain discrepancy varies between -1 dB and -2 dB across the whole input frequency range. A noticeable discrepancy between the phase responses progressively develops at high frequencies. Both phenomena can be ascribed to incomplete charge transfers between capacitors due to the transmission gate on-resistance and/or limited bandwidth of the inverter-like amplifiers. This is confirmed by the curve obtained by keeping the same supply voltage and slowing down the clock to 100 kHz. In this case, both the gain and phase differences are strongly reduced. Errors at high frequencies can be reduced also by keeping the same clock frequency (1 MHz) and scaling down all capacitors by a fixed factor. The result for a scaling factor of 0.5 is shown in Fig.9 (dotted curve). However, this operation degrades the dc gain, due to the higher sensitivity to the mentioned stray charge paths caused by parasitic capacitances. The possibility of operation at reduced supply voltage is proven by the curve at V_{dd}=0.6 V. In this case, the clock frequency was reduced to 50 kHz to maintain acceptable performance.

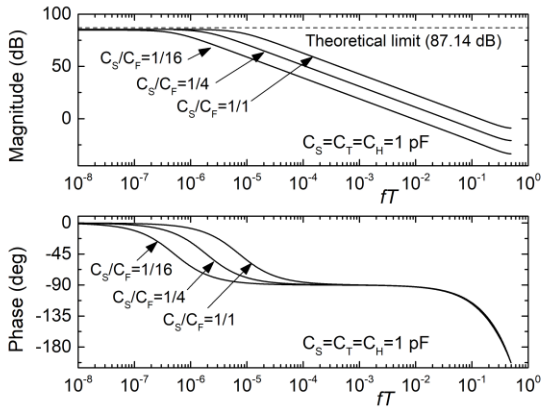

Fig. 8. Magnitude and phase response extracted from electrical simulations performed on the circuit of Fig.6, for V_{dd}=0.9 V, f_{ck}=1 MHz, and three different C_S/C_F ratios indicated with labels.

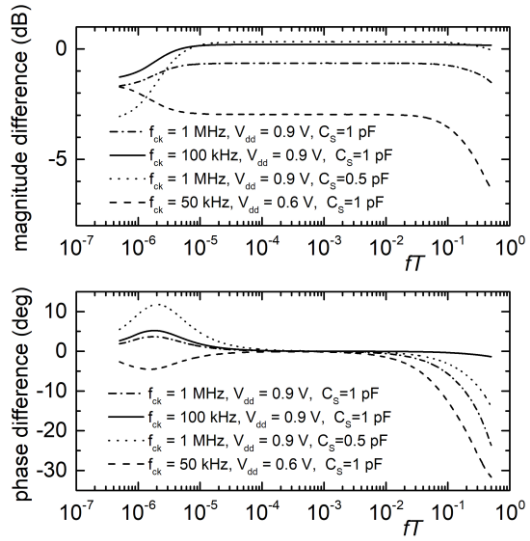

Fig. 9. Magnitude and phase difference between the discrete-time and electrical simulations for C_S/C_F =1/4 and different clock, supply voltage and capacitance C_S combinations, indicated in the figure.

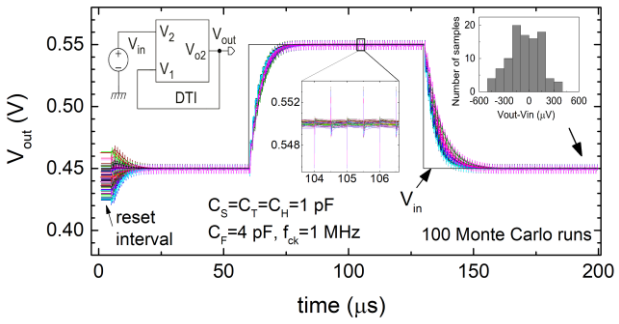

Fig. 10. Results of 100 Monte Carlo runs performed on the test bench shown in the left inset (unity gain, low pass filter), stimulated with a 70 μs pulse of 100 mV magnitude. The histogram on the right shows the dc error distribution estimated over 100 Monte Carlo runs.

In particular, the dc gain loss at V_{dd} =0.6 V is only 2 dB. The supply current is 5.6 μA at V_{dd}=0.9 V and drops to 140 nA at V_{dd}=0.6 V. Fig.10 shows the result of 100 Monte Carlo transient simulations, including both global and local variations, performed on the integrator mounted in unity-gain, closed-loop configuration, implementing a first-order, low-pass filter (cut-off frequency =40 kHz). In the first 5 μs, C_F is shorted by means of an auxiliary switch (not shown in Fig.6), so that V_{OUT} coincides with V_{INV}. of INV-2. The high initial dispersion is recovered by the mentioned CDS mechanism, and the final dispersion is shown by the histogram. Finally, the impact of the inverter non-linearity was characterized by stimulating the same first-order filter as in Fig.10 with a 1 kHz sinusoidal waveform of 0.7 V peak-to-peak magnitude (78% of V_{dd}), obtaining a THD of -56 dB (15 harmonics) that drops to -65 dB if f_{ck} is reduced from 1 MHz to 500 kHz.

V. Conclusion

Discrete-time and electrical simulations confirmed that the proposed DTI presents a dc gain close to $(A_0)^3$. The occurrence of significant gain and phase errors in the upper region of the discrete-time frequency domain reduces suitability to high-Q SC filters. Nevertheless, the proposed DTI can be considered as a valid alternative to existing inverter-like topologies for low-pass, moderate resolution, Δ–Σ converters, where the signal bandwidth is squeezed in the lower part of the frequency range.

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