Approaches to Building a Quantum Computer Based on Semiconductors

by

Sebastian Pauka

at

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Throughout this Ph.D., the quest to build a quantum computer has accelerated, driven by ever-improving fidelities of conventional qubits and the development of new technologies that promise topologically protected qubits with the potential for lifetimes that exceed those of comparable conventional qubits. As such, there has been an explosion of interest in the design of an architecture for a quantum computer. This design would have to include high-quality qubits at the bottom of the stack, be extensible, and allow the layout of many qubits with scalable methods for readout and control of the entire device. Furthermore, the whole experimental infrastructure must handle the requirements for parallel operation of many qubits in the system. Hence the crux of this thesis: to design an architecture for a semiconductor-based quantum computer that encompasses all the elements that would be required to build a large scale quantum machine, and investigate the individual these elements at each layer of this stack, from qubit to readout to control.

Each chapter of this thesis investigates a different layer of the stack from the top down. In Chapter 2, I explore the key elements of the architecture of a quantum computer. I first define a common structure by which we can compare the control and readout hardware for any given design, following which I present two potential architectures for a quantum computer: one that multiplexes both readout and control from room-temperature to 4 K in Sec. 2.2, followed by one which uses CryoCMOS to generate control pulses near the qubits in Sec. 2.3.

In Chapter 3, I move up the stack and present a set of experiments concerning the design and implementation of circulators based on the quantum Hall effect (Sec. 3.1) and the anomalous quantum Hall effect (Sec. 3.2). Circulators are vital components in qubit experiments, used to route signals and isolate qubits from thermal photons, however, are currently bulky, centimeter-scale devices. By capacitively coupling to the edge magnetoplasmon modes of micron-scale Hall droplets, I demonstrate non-reciprocal transmission with isolation similar to that of off-the-shelf components.

In Chapter 4, I explore the design of the spin qubit and examine the dispersive gate sensing technique, which holds promise as a scalable method of readout for large arrays of quantum dots. First, in Sec. 4.1, the scalable design for a singlet-triplet qubit is proposed, which allows for the layout of larger arrays of qubits while presenting a method for two-qubit coupling over intermediate length scales via an intermediate quantum state. Then, in Sec. 4.2, I inspect anomalous signals present in dispersive gate sensors, propos-

ing that they are caused by localized pockets of charge that form in the 2-dimensional electron gas (2DEG). These pockets of charge may contribute to the charge-noise that plagues semiconductor based qubits.

Finally, in Chapter 5, I study the formation of Majorana zero modes in InAs nanowires and 2DEGs and the experimental challenges of realizing a qubit based on topological qubits. In Sec. 5.1, I propose techniques for improving the quality of shallow InAs 2DEG's after processing, which remains a limiting factor in the design of qubits based on Majorana zero modes in InAs. In Sec. 5.2, I investigate techniques for finding and reading out Majorana zero modes and present benchmarks on the current generation of charge sensors in nanowires.

Thesis Supervisor: Professor David Reilly

Declaration

I herewith declare that the intellectual content of this thesis is the product of my own work, and that I have produced this work without the prohibited assistance of third parties and without making use of aids other than those specified. Notions taken directly or indirectly from other sources have been identified as such. For all published work, permission to include data in this thesis has been granted from the corresponding author, and author lists and affiliations are listed.

The thesis work was conducted from 03 Mar 2014 to 26 Aug 2019 under the supervision of Professor David Reilly and Professor Andrew Doherty at the University of Sydney.

Signed:_____

Sebastian Pauka
Date: 26 Aug 2019

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It was more than six years ago now that I found myself choosing between a research career in physics and one in computer science. At the time, it was a difficult choice, but with the benefit of hindsight, I have no doubts that I made the right call. That is to a considerable degree due to amazing people I've had the opportunity to work with.

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Chapter 0

Introduction

The invention of quantum mechanics early in the twentieth century created the most complete and accurate theory of reality that has been discovered so far. It was Richard Feynman who theorized in his seminal 1981 keynote [1] that with quantum physics we could build a quantum simulator — a machine that would be able to solve a class of problem that we couldn't solve with a classical computer (an idea we will expand on in Section 1.1). Since he delivered this keynote, the field of quantum computing has exploded. First came theoretical descriptions of algorithms with a quantum speedup: Deutsch's Algorithm in 1992 [2] and Shor's Algorithm in 1994 [3]. Despite these advances, many suspected that it was only a matter of time before a "no-go" result would be found; a result that would say that quantum computers could not scale, or that errors in a quantum system would be uncorrectable. However, with the formulation of the quantum fault-tolerance theorem [4, 5], which showed that for a sufficiently small error rate it is possible to correct errors faster than they occur, the last reasonable objection to quantum computing was overcome (my favorite reference as to why this seems true is in Chapter 14 of Scott Aaronson's book [6]). Since then, a plethora of physical systems have emerged that seem like contenders for building a quantum computer, such as trapped ions [7], nuclear spins [8], electron spins in semiconductors [9], excitations in superconductors [10], single photons [11], or a large number of other systems that are too numerous to list here. Each of them aims to realize a qubit, the quantum equivalent of a bit, which rather than being described as a single number taking the value of 0 or 1, is represented by a two-dimensional vector that evolves under the rules of quantum physics, an idea I expand upon in Section 1.1.1. Today, many of these qubits are being realized in larger and larger numbers with error rates that are butting up against the fault-tolerance threshold, raising the specter of large quantum computers in the near future.

With such a large number of physical systems to choose from, and with significant

differences in the experimental apparatus necessary to form and control them, I make the choice to limit the discussion in my thesis to semiconductor and superconductor based qubit systems. This class of qubit still encompasses a significant portion of the above systems, however, these systems have the advantage of sharing a number of features which will allow us to reason about the design of a large-scale quantum machine, despite the fact that a truly scalable quantum chip is not yet a reality. Namely, these each have all electrical control and readout with bandwidths up to a few GHz, and must all be cooled to temperatures of a few mK in order to protect the delicate quantum information stored within them from thermal excitation, and for superconducting and topological variants, to form a superconducting state. In particular, the requirement to cool these systems introduces limitations in the power that may be dissipated proximally to the quantum device, with only a few micro-Watt's of cooling power available when cooling devices to mK in a cryostat. With this in mind, the design of a quantum computer must balance power, interconnection and latency between the different stages to fit within the noise, space and power constraints of the system.

The rapid progress made in the field, while no doubt exciting, also highlights the difficulty I have in preparing this thesis. Between when I started my Ph.D. in 2014 and now, the community underwent a seismic shift in ambition, moving from trying to work on one or few-qubit systems [12] to trying to implement useful machines with hundreds of qubits [13], with a concomitant increase in funding. Industrial players have also entered the ring trying to build viable commercial quantum machines, including IBM, Intel, Google, Rigetti, DWave and Microsoft. Over the same period, our lab grew from one with a single dilution refrigerator (DR) and four other Ph.D. students to one with 7 DRs, 2 cryostats, close to 50 people and substantial backing from industry (Microsoft). It is in that context that this thesis is written. All the topics presented have the same aim: to build a useful quantum computer; but experiments span from exploring low-level materials challenges, to designing individual qubits, to scalable instrumentation design, and finally to architecture designs for building large scale quantum machines.

I have grouped results into five broad chapters, each of which presents several papers dealing with these results, intending to create a coherent story-line around my work, starting from the top level architecture in Chapter 2 and working my way down to materials science in Chapter 5. A brief description of the structure of this thesis is as follows.

In order to discuss how different architecture designs for a quantum computer vary, the topic of Chapter 2, we must first devise a system for comparing them based on common features of their design. Existing techniques for comparing designs, based on those used in classical computing such as Rent's rule [14], have recently been adapted for their quantum

counterparts [15], however are not sufficiently descriptive for describing or contrasting the different architectures that have been proposed. I will therefore begin, in Section 2.1, by defining a new quantum-specific framework for discussing architectures used for quantum computers, using the three criteria (power, interconnection and latency) highlighted above. Following this, I present two new architectures, the prime lines architecture in Section 2.2 which routes signals generated at room temperature between many qubits, and a Cryo-CMOS architecture which is able to generate pulses at mK. Each of these significantly reduces the number of interconnects necessary between room temperature and mK, allowing the number of qubits controlled by finite resources to be increased dramatically. Such approaches, while previously proposed in various theoretical forms [16, 17], are realized for the first time in Section 2.3.

To enable the architectures proposed in this thesis, it is crucial to, in parallel, develop low- or no-power technologies that form the building blocks of the routing and interconnection in this thesis, which may be tightly integrated with the qubit chip at the bottom of the fridge (see Section 2.1 for the argument as to why this must be done at mK). This idea is explored in Chapters 2 and 3. The goal of tighter integration is achieved by three methods. First, utilizing the technologies used to make qubits for routing and control, as is done with the reflective switches that enable the prime-lines architecture in Section 2.2. Second is miniaturization of existing components to allow tight integration and further scaling of existing designs, as is presented in the work miniaturizing circulators in Chapter 3. Finally, the utilization of existing technologies, in this case CMOS, for qubit control, is described in Section 2.3.

All the above discussion hinges on the demonstration of high-fidelity qubits, without which quantum computing will remain just a hypothetical idea. With that in mind, the final two chapters of this thesis deal with the development of scalable designs for high-fidelity qubits. Two ideas are explored. Chapter 4 studies a well-established qubit platform: the spin qubit. Although this platform has been studied extensively in the past [18, 9], scaling them to useful sizes requires numerous further improvements in design, control and read-out. For example, existing designs require complex protocols for initialization [19] or the placement of many large proximal charge sensors [20]. In this thesis, I tackle these two issues, presenting an tileable design of a spin-qubit device in GaAs that allows simple initialization of qubits in long chains in Section 4.1, and investigate sources of noise that limits the performance of dispersive gate sensing, a technique that allows the use of gate electrodes rather than bulky proximal charge sensors for readout of qubits, in Section 4.2. Although the experiments in this thesis focus on devices in a GaAs/(Al, Ga)As heterostructure, many

of the issues and solutions raised have applicability to any dispersive readout or quantum dot system.

Finally, in Chapter 5, we survey the nascent field of forming Majorana zero modes to use as topologically protected qubits. While such a topologically protected qubit has not yet been demonstrated, if they are realized they may have lifetimes that far exceed those of any other qubit technology [21]. While promising, the prerequisites for forming Majorana zero modes in semiconductor/superconductor hybrid structures: a large spin-orbit interaction, large Landé g-factor, high mobility, and a close, transparent interface to a superconductor, means that extensive materials and process development must be performed before they are realized. Furthermore, existing techniques for readout and control of semiconductor qubits must be adapted to this new architecture. In Section 5.1, we investigate methods for repairing the damage done to the surface of shallow 2DEGs in InAs after processing, either using TMA to remove the dirty native oxide or an ArH plasma to passivate charged surface states, and characterize the quality of these materials after treatment. Then, in Section 5.2, we evaluate techniques for charge sensing of Majorana zero modes formed in proximitized InAs nanowires.

Before delving into new results, let's start off with a brief review of the key concepts in quantum computing and materials science necessary to understand the results that follow and the context in which this research is performed.

Chapter 1

The Quest for a Quantum Computer

Before delving into the question of how we might build a quantum computer, it is worth taking a step back and exploring the question of what brought us as a scientific community to the point where it is seen as a priority to build one. The answer to that requires us to dive briefly into the world of computational complexity theory, and to examine what it means to solve problems "efficiently".

Machines we might recognize as computers were first constructed in the early 1900's, although the genesis of computation can be traced back to pioneering works by people such as Charles Babbage and Ada Lovelace in the early 1800's [22]. Based on delicate vacuum tubes and mechanical relays, and often taking up giant rooms, their inherent fragility and bugginess posed formidable obstacles to scaling. It was not until the mid-1900's that the field took off with two pivotal discoveries. The first was the construction of the first transistor in 1947, credited to Bardeen, Brattain and Shockley and for which they were awarded the Nobel Prize in 1956 [23]. This was followed by the creation of integrated circuits by Jack Kilby in 1959, for which he was awarded the Nobel Prize in the year 2000 [24]. With these two inventions, a remarkable surge in computational power occurred. This surge is embodied in Moore's law, which described an annual doubling in the number of transistors that it would be possible to fit on a single integrated circuit [25]. With this doubling came an exponential growth in the computational power that we had available to us.

Along with this growth came an obvious question. What exactly can these computers do? What sorts of problems will we be able to solve with our ever-growing bundle of transistors? To answer this question, we define the concept of an **algorithm**, a sequence of steps we run to solve a given problem. To figure out what problems we can solve, we need to calculate the number of steps we need to run to solve that problem, which tells us whether the problem can be feasibly solved. Take, for example, the question of looking for a single item

x_T, in a list $L = \{x_0, x_1, \ldots, x_n\}$ with n items in it. Assuming the list is in an unknown order, to find the location of the item x_T, we need to look at each item in the list in turn. If the length of the list were doubled to $2n$ items, it would take twice as many steps to look through the list. Tripled would be three times. The number of steps, and hence the amount of time, it takes to find an item in the list is *linear* in the length of the list. We can write the scaling of the number of steps mathematically using big-$\mathcal{O}$ notation: searching for an item in a list is $\mathcal{O}(n)$.

What about a slightly more complicated problem? What if we want to check whether any item x_i appears in the list twice? To solve this problem, we can run the above algorithm for each item in the list in turn, setting the target to $x_T = x_0$, then $x_T = x_1$ and so forth, and checking whether we find each item two or more times. So for n items in the list, we run through the list n times, so the number of steps to run the algorithm scales as $\mathcal{O}(n^2)$. That is, if the length of the list is doubled, it takes four times as long, so the scaling is *quadratic*.

In this way, we can classify algorithms into various complexity classes. For example, sorting a list of n items is, in the best case, $\mathcal{O}(n \log(n))$. Solving the traveling salesman problem (TSP) is $\mathcal{O}(n^2 2^n)$. Ideally, we would like to group problems into various complexity classes. For example, we can group problems that have at worst a polynomial complexity, i.e. $\mathcal{O}\left(f(n)\right)$ where $f(n)$ is a polynomial into the complexity class P (for polynomial). We will call these problems **efficiently computable**. Other problems may grow at worst exponentially in the size of the problem. We can group all of those problems into the complexity class EXP. These problems, and indeed any problem that has a difficulty that grows faster than a polynomial in the size of the problem, are said to be inefficient to compute.

Of course, you might say, well what sort of operations do we allow our computers to do in a single step? If I say that my computer can solve the TSP in a single step, then the complexity of that problem reduces trivially to $\mathcal{O}(1)$. The answer to the question of what a computer may do in a single step is not so trivial — it is limited by the laws of physics. What sorts of computation do they allow? To answer this question, Alan Turing and Alonzo Church came up with the notion of the Turing Machine, a universal model for a physical computational device, which defines the operations that a computer may perform in a single step according to the laws of physics, and with it stated the Church-Turing hypothesis:

> "a function is effectively calculable if its values can be found by some purely mechanical process". We may take this literally, understanding that by a purely mechanical process one which could be carried out by a machine.[26]

To paraphrase, this stated that anything a Turing machine could do, a computer could do too, and anything it *can't* do, no computer can. It wasn't long before this was extended

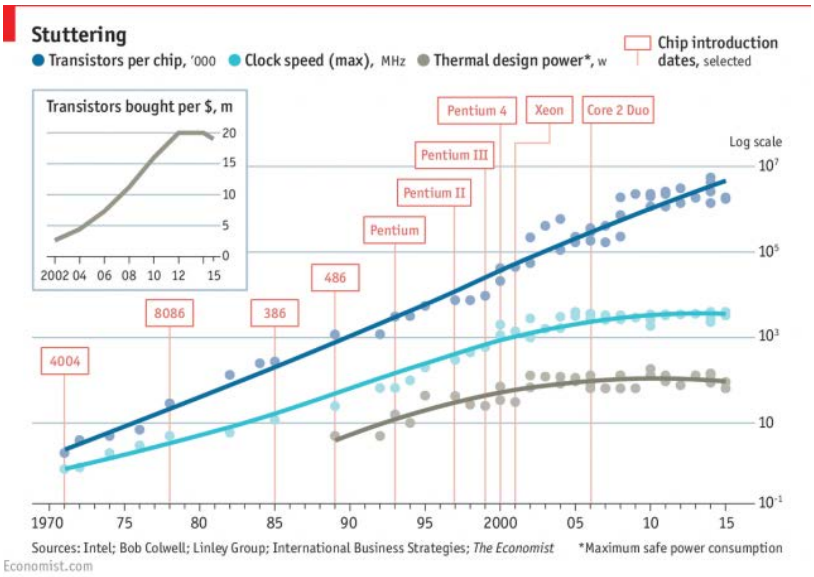

Figure 1.1: Graph of the number of transistors per chip, their clock speed, and their thermal design power plotted on a log scale against time. Although the number of transistors per chip continues to grow exponentially, the clock speed and power per chip have plateaued in the early 2000s. Reproduced with permission from [28].

to the strong Church-Turing hypothesis, which states "A probabilistic Turing machine can efficiently simulate any realistic model of computation"[27][1]. Note the addition of the term *efficiently*. This prescribes that for any operation we could add to any physical computer, we can get at most a polynomial speedup. Since a polynomial $P(n)$ divided by another polynomial $Q(n)$ is still a polynomial, and anything that grows faster than a polynomial $E(n)$ divided by a polynomial $Q(n)$ still grows faster than a polynomial, we have a universal definition for problems that are efficient to solve and those that aren't. [2]

So, we've established what sorts of problems a computer can solve efficiently, and we've also noted the exponential growth in the number of transistors on a chip. As long as both of these facts remain true, we should only have to wait a few years before our computers become twice as powerful and problems that were previously intractable fall within our grasp. Unfortunately, any exponential scaling must eventually fail, and so it was for ICs for two key reasons: power and transistor size. As we made our transistors smaller, we stopped

[1]Note we had to add the word "probabilistic" to the statement of the strong Church-Turing hypothesis. This was due to the discovery of a new complexity class, bounded-error probabilistic polynomial (BPP), which includes problems we can solve with $> 2/3$ chance in polynomial time. By running these algorithms repeatedly, we can solve problems to within a small error ϵ in polynomial time.

[2]Of course, since we're continually coming up with better algorithms to solve hard problems, the set of problems that are efficient to solve seems to keep growing!

seeing a concomitant efficiency increase, and all of a sudden, the power density of our ICs became a limiting factor. To halt this increase, we had to reduce power dissipation, and the only way we saw how was by capping the clock speed of our computers, which, as we can see in Fig. 1.1 has plateaued since the early 2000s. Moreover, the smaller our transistors became, the more costly they were to make. Even Moore's law, which has stubbornly held past the expectations of most scientists, must eventually end as we bump up against the sizes of atoms. It seems unlikely that there is much room below Samsung's recently announced 3 nm node, so if we want to bring more problems into the fold of the possible, it seems like the strong Church-Turing hypothesis must give.

It was in this context that Feynman gave his seminal address, noting that as far as we can tell, simulating quantum systems falls outside of the set of problems that are efficiently solvable on classical computers [1]. However, as long as we can manipulate quantum systems, we should also be able to set up a "quantum simulator" to see how a quantum system behaves. If this turned out to be the case, then the strong Church-Turing hypothesis would be violated[3]! Here was nature efficiently simulating a system that a Turing machine can't. It was David Deutsch who in 1985 formalized the idea of a quantum Turing machine [29], and laid out the Deutsch-Church-Turing hypothesis, which holds to this day:

> A quantum Turing machine can efficiently simulate any realistic model of computation.

With that, we finally define the class of problems that we might be able to solve efficiently if we can build a quantum computer — Bounded-Error Quantum Polynomial-Time or BQP. As far as we know, this class includes interesting problems that a classical computer could not efficiently solve. Problems such as Shor's algorithm for prime factorization [3] or estimating the ground state of molecules with the Variational Quantum Eigensolver algorithm [30] have no known efficient classical algorithm but could profoundly impact society. It is the promise of solutions to these problems that drive the search for a quantum computer; however, the challenges of realizing one remain formidable. To close out our discussion of complexity classes, I've summarized the relationship between complexity classes in Fig. 1.2. A point worth emphasizing is that although BQP is larger than P or BPP, it certainly does not enclose all problems, especially those in EXP. Although a quantum computer may offer an exponential speedup on a subset of algorithms, it will not give us an exponential speedup in the general case.

[3]Despite this violation, as far as we know the original Church-Turing hypothesis still holds. No previously uncomputable function became computable with the addition of quantum physics.

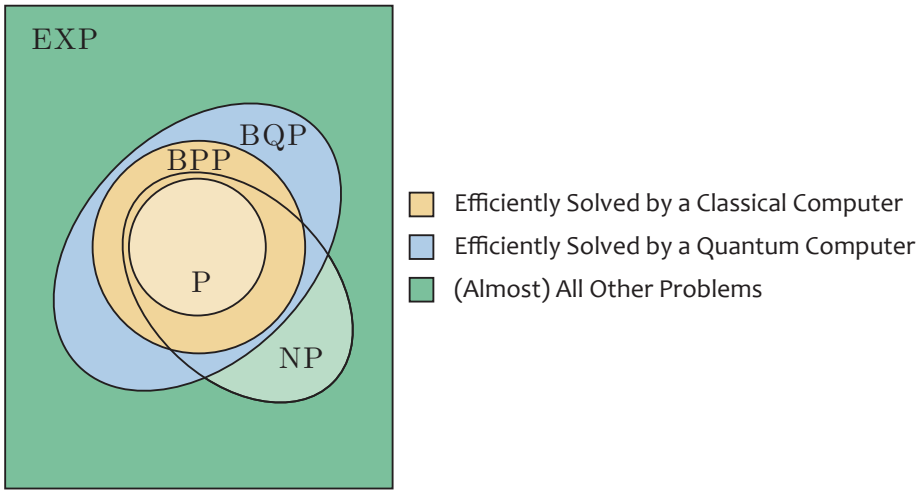

Figure 1.2: Relationship between the various complexity classes that we've discussed. The class BPP includes all problems that a classical computer can solve efficiently (including everything that can be calculated in polynomial time). BQP are all problems a quantum computer can solve efficiently (which includes everything a classical computer can do). Finally, problems that scale exponentially with input size, labeled EXP, are (almost) all other problems that are computable. The class NP is also included on this figure as it is one that often comes up in the context of complexity, if for no other reason than to emphasize that a quantum computer *cannot* solve all problems in this class.

The remainder of this chapter aims to lay out the fundamentals of quantum computing and how we might realize them in a semiconductor system. In Section 1.1, I go through a quick introduction to the concepts underlying quantum computation. In Section 1.2, I will detail several methods by which we might realize a qubit in a semiconductor. Finally, in Section 1.3, I will outline the characterization of a 2DEG, the system in which we make qubits.

1.1 A Quick Introduction to Quantum Computing

To build a quantum computer, we start by defining the notion of a quantum bit (qubit), which serves as the quantum analog to the classical bit. To review, a classical **bit** is a "piece" of information that can either take the value 0 or 1. It represents the fundamental unit of computation in digital computers. We can take individual bits, and combine them to form a **register**, whose state is defined as the state of each bit in the register. For example, two bits can take up to 4 different values: 00, 01, 10, 11. Three bits can take up to 8 values, and N bits can take up to 2^N values, however to give the state of a register all we have to do is list the state of each bit in that register, a total of N states. By choosing various encodings of values, we can map numbers, letters, and other symbols onto these registers and perform

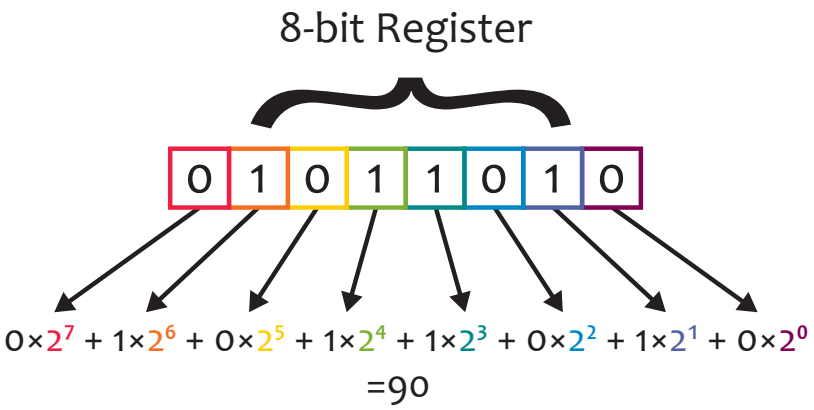

Figure 1.3: We can encode information in a register in many ways. One encoding for positive numbers is to use a base-2 positional system, like above, where the binary register 01011010 is mapped to the number 90.

computations on them. For example, we can map positive integers onto registers using a base-2 number system, as in Fig. 1.3, or letters using a mapping such as ASCII, which assigns letters to 8-bit registers. Other mappings exist for negative numbers (such as a mapping called two's complement), numbers with decimal points (such as IEEE floating point), complex numbers and so forth.

1.1.1 The Qubit

A **qubit** is similar to a bit in that it has two states, $|0\rangle$ and $|1\rangle$, except unlike a bit, it is specified by a 2-dimensional vector, and evolves according to the rules of quantum mechanics. Due to the uniquely quantum mechanical property of **superposition**, we can no longer write the state of a single qubit (which we will denote ψ) as either $|0\rangle$ or $|1\rangle$. Instead, we must write down the vector sum of the two states, which we define as follows:

$$|0\rangle = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \qquad |1\rangle = \begin{bmatrix} 0 \\ 1 \end{bmatrix} \tag{1.1}$$

$$|\psi\rangle = \alpha\,|0\rangle + \beta\,|1\rangle = \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \tag{1.2}$$

where α and β are complex numbers. If we were to take a measurement of this quantum state, rather than getting back the value of this vector sum, we would measure the $|0\rangle$ state with probability $|\alpha|^2$ and the $|1\rangle$ state with probability $|\beta|^2$. Since probabilities must sum

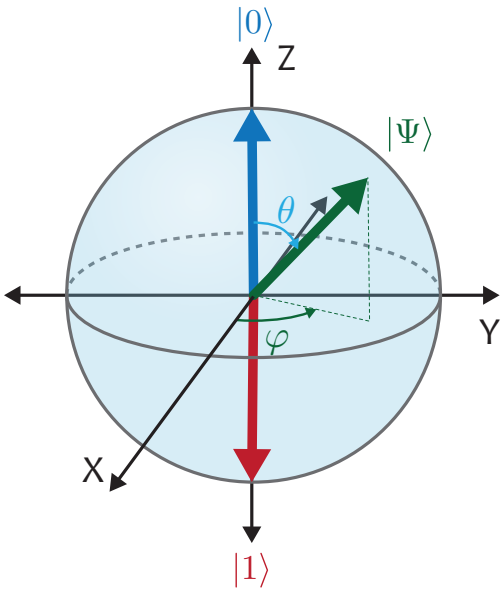

Figure 1.4: The state of a qubit can be represented as vector on the surface of a unit sphere. In this description, the state is described by two angles: θ and ψ.

to one, we also get a normalization condition: $|\alpha|^2 + |\beta|^2 = 1$. The quantities α and β are called probability amplitudes, and they can take both positive and negative complex values[4] as long as the sum of their squared magnitudes is one. This gives us the first hint as to why quantum computing might give us more power than a classical computer: their states can interact in a manner which mirrors interference!

To see how this is true, it's helpful to rewrite the above state in spherical coordinates. First, let's write $\alpha = r_0 e^{-i\varphi_1}$ and $\beta = r_1 e^{-i\varphi_2}$. The normalization condition is now $r_0^2 + r_1^2 = 1$, from which we can make the replacement $r_0 = \cos(\theta/2)$ and $r_1 = \sin(\theta/2)$. We can also factor out the phase φ_1 to give:

$$|\psi\rangle = e^{-i\varphi_1}\left(\cos\left(\frac{\theta}{2}\right)|0\rangle + e^{-i(\varphi_2-\varphi_1)}\sin\left(\frac{\theta}{2}\right)|1\rangle\right) \tag{1.3}$$

The term $e^{-i\varphi_1}$ is called a global phase factor, and is equivalent to a multiplication by a unit vector, which it's easy to see makes no difference to the probabilities of any measurement (a fact that will continue to be true even when we add more qubits). Another way of saying this is that the important information is encoded in the relative phase between states. So,

[4]Interestingly, the "complex" part of that state is unnecessary to get the extra computing power of a quantum computer [31]. There's a good reason that quantum mechanics uses complex probability amplitudes [32], but if they were real, it turns out we can still do computations in BQP efficiently.

let's make the replacement $\phi = \varphi_2 - \varphi_1$ and ignore the global phase factor, which gives us the state:

$$|\psi\rangle = \cos\left(\frac{\theta}{2}\right)|0\rangle + e^{-i\phi}\sin\left(\frac{\theta}{2}\right)|1\rangle \tag{1.4}$$

This representation is shown visually in Fig. 1.4 and is called the Bloch sphere representation of a qubit[5].

Given this description, we can now start to think about what operations on a single qubit might look like. While on a single bit, the only non-trivial operation we can perform is a flip ($0 \to 1$ and $1 \to 0$), on a qubit we have a whole host of operations that we can perform. The only limits we put on ourselves is that these operations must leave us on the surface of the Bloch sphere. In other words, after applying an operation, we must still have a normalized state. From the Bloch representation, you may have already guessed that this means we can only perform rotations.

Switching back to the 2D vector representation of a qubit, then it is also clear that these operations must correspond to 2×2 matrices. The act of performing an operation corresponds to multiplying the qubit state by one of these matrices. To ensure that the length of the qubit vector $|\psi\rangle$ remains one at all times, the matrices we can use on our qubit must be unitary. That is, given the matrix M, its complex conjugate transpose $M^\dagger = (M^*)^{\mathrm{T}}$ times itself must be equal to the identity matrix: $M^\dagger M = I$.

Let's define three unit rotation matrices as π rotations around the X, Y, Z axes. These have the symbols $\sigma_X, \sigma_Y, \sigma_Z$ respectively, and are called the Pauli matrices. They have the values:

$$\sigma_X = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \qquad \sigma_Y = \begin{bmatrix} 0 & -i \\ i & 0 \end{bmatrix} \qquad \sigma_Z = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix} \tag{1.5}$$

We can build up arbitrary rotations from these unit vectors by taking various powers of these vectors and multiplying them together. For example to apply a $\pi/2$ rotation around the y-axis applied to the state $|\psi\rangle$ we would perform $\sqrt{\sigma_Y}|\psi\rangle$[6]. A 2π rotation around the x-axis would be $\sigma_X\sigma_X|\psi\rangle$. It is possible to generalize this to arbitrary rotations, giving us the rotation operators [33]:

$$R_X(\theta) = e^{-i\theta X/2} = \cos\left(\frac{\theta}{2}\right) I - i\sin\left(\frac{\theta}{2}\right)\sigma_X \tag{1.6}$$

[5]For mathematicians, this is a description of the qubit in Complex Projective Space

[6]For those familiar with the rotation operators, this is more commonly written with a phase factor to make the solution purely real: $R_Y(\frac{\theta}{2}) = \exp(-i\pi/4)\sqrt{\sigma_Y}$

$$R_Y(\theta) = e^{-i\theta Y/2} = \cos\left(\frac{\theta}{2}\right) I - i \sin\left(\frac{\theta}{2}\right) \sigma_Y \tag{1.7}$$

$$R_Z(\theta) = e^{-i\theta Z/2} = \cos\left(\frac{\theta}{2}\right) I - i \sin\left(\frac{\theta}{2}\right) \sigma_Z \tag{1.8}$$

These three rotations (and often a global phase factor to simplify our result) are sufficient to express any single qubit operation. For completeness, we can also define some other gates that often come up in the context of quantum computation:

$$H = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} = e^{\frac{i\pi}{2}} R_Y\left(\frac{\pi}{2}\right) R_Z(\pi) = \frac{\sigma_X + \sigma_Z}{\sqrt{2}} \tag{1.9}$$

$$T = \begin{bmatrix} 1 & 0 \\ 0 & e^{\frac{i\pi}{4}} \end{bmatrix} = e^{\frac{i\pi}{8}} R_Z\left(\frac{\pi}{4}\right) = \sqrt[4]{\sigma_Z} \tag{1.10}$$

$$S = \begin{bmatrix} 1 & 0 \\ 0 & i \end{bmatrix} = e^{\frac{i\pi}{4}} R_Z\left(\frac{\pi}{2}\right) = \sqrt{\sigma_Z} \tag{1.11}$$

These are the Hadamard gate, the T gate (or $\pi/8$ gate)[7] and the phase gate respectively. As is typical, phase factors are usually dropped (something I did not do in the above), hence it is common to see variations of these equations in the literature.

As a final example, let's take a detailed look at where interfering probabilities lead to a thoroughly non-classical result. To start with, let's define two additional states:

$$|+\rangle = \frac{|0\rangle + |1\rangle}{\sqrt{2}} \qquad\qquad |-\rangle = \frac{|0\rangle - |1\rangle}{\sqrt{2}} \tag{1.12}$$

We can get these states by starting from $|0\rangle$ and rotating $\pi/2$ or $-\pi/2$ around the Y-axis. You can confirm that they are properly normalized, and that if we were to measure each state, the probabilities of measuring a $|0\rangle$ or a $|1\rangle$ are equal for both states: $\mathrm{P}(|0\rangle) = \mathrm{P}(|1\rangle) = 0.5$. So a direct measurement would be unable to distinguish these two states. However, if we were to apply the Hadamard gate to each of those two states, we surprisingly end up with two different outputs:

$$H|+\rangle = |0\rangle \qquad\qquad H|-\rangle = |1\rangle \tag{1.13}$$

In this case, the complex probability amplitudes can interfere with each other causing the

[7] The *T*-gate is often referred to as the $\pi/8$ gate, even though it represents a $\pi/4$ rotation, a name that is derived from the phase factor for historical reasons.

two states to become distinguishable, something that a classical bit could not replicate. In a similar way, a single measurement is not able to give us all the information contained within a quantum state. While with a bit, what you see is what you get, a qubit is a more complicated beast.

1.1.2 Multi-Qubit States (Qubit Registers)

The next additional computational resource that quantum physics gives us is **entanglement**. This resource rears its head when we try to combine multiple qubits into a register. Formally, we can define entanglement as a correlation between the states of qubits after they have interacted with each other. Due to this correlation, the state of a qubit that has been entangled with its partner can no longer be described independently, the states of the two qubits become linked. Perhaps the easiest way to intuitively understand the consequences of this is to give an example of how this correlation might play out.

Let's start with two qubits, one of which starts in the $|+\rangle$ state, and the other which starts in the $|0\rangle$ state. If we were to apply a gate that flips the state of the second qubit if the state of the first qubit is $|1\rangle$, then we might expect to end up with something like $|+\rangle$ in the second qubit. If we measure the first qubit and get the result $|0\rangle$, the state of the second qubit must also be zero, so the state of the second qubit can't have been described by $|+\rangle$. The state of the two qubits is correlated and depend on each other. The operation we described above is called the controlled-NOT ($CNOT$) gate, and creates a state that looks like:

$$|\psi\rangle = \frac{|00\rangle + |11\rangle}{\sqrt{2}} \tag{1.14}$$

To describe a generalized two-qubit state, we must give coefficients to each possible state the qubits can take:

$$|\psi\rangle = \alpha\,|00\rangle + \beta\,|01\rangle + \gamma\,|10\rangle + \delta\,|11\rangle = \begin{bmatrix} \alpha \\ \beta \\ \gamma \\ \delta \end{bmatrix} \tag{1.15}$$

So to combine two qubits together, we cannot just list the states of the two qubits one after another. They are described by the tensor product of the two individual states: $|\psi\rangle = |\psi_1\rangle \otimes |\psi_2\rangle$. For a three-qubit register, the total number of states we must give coefficients to is 8. For a N qubit register, the total number of coefficients is 2^N. Note the distinction between a classical register and a quantum register, to describe a classical register, we can

list the states of the individual bits one after another, whereas the quantum register requires 2^N complex numbers to express fully.

Much like a single qubit, we require new matrices that can operate on quantum registers. As one might expect, the size of these matrices is exponential in the number of qubits that we must operate on. For example, on a two-qubit register, we require a 4×4 matrix to describe operations. The $CNOT$-gate that we used above is defined as:

$$CNOT = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix} \tag{1.16}$$

Unfortunately, the potential presence of entanglement means applying single or two-qubit gates to a subset of qubits in the register is no longer a matter of applying a 2×2 or 4×4 matrix, we must construct a $2^N \times 2^N$ matrix and apply that to the full quantum register. This construction is achieved by taking the Kronecker product of identity matrices and the matrix we want to apply. For example, to apply a σ_X gate to the 2nd qubit in a three-qubit register, we construct the operator as follows:

$$\sigma_{X,2} = I \otimes \sigma_X \otimes I \tag{1.17}$$

The consequences of the twin effects of superposition and entanglement lead to the extra computational power of a quantum computer, while also hinting at the difficulty of writing quantum algorithms. As we can prepare arbitrary superposition states, we can encode an exponentially large state into a quantum register, for example representing every state between 0 and $2^N - 1$ in a N qubit register, and operate on all of these states in parallel. However, once we measure the register, we end up with only one of the possible states in the register (i.e. the state collapses), and the quantum information that was prepared in the state is lost. Quantum algorithms must, therefore, have three properties to be useful:

1. An efficient way of preparing a state. If we want to perform computations on a quantum register storing 2^N values, we lose any exponential speedup if we need to load each of these values one-by-one. For example, Shor's algorithm relies on being able to prepare an equal superposition of all states in the register with N single qubit gates [34].

2. Creation of a large entangled state. Without entanglement, a quantum algorithm can be efficiently simulated on a classical computer. We don't know quite how to quantify

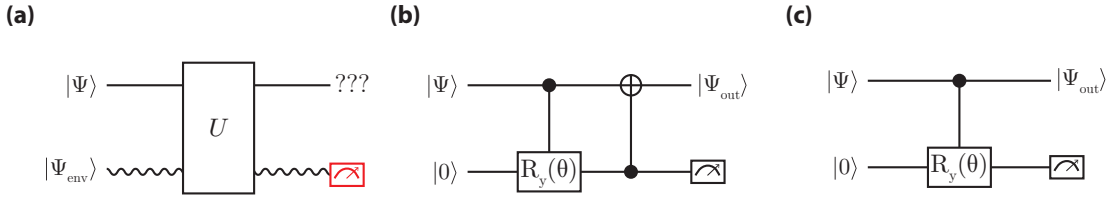

Figure 1.5: (a) We can think of noise as uncontrolled interactions with an environment. However since we can't measure information that is transferred into the environment, we end up with an incomplete representation of our qubit. In order to represent this state, with some of its information lost, we must describe the state with a density matrix representation. (b) A simple model for relaxation, where we represent the probability of a decay γ in the rotation angle $\sin^2(\theta/2) = \gamma$. Each time this gate is applied, we end up more likely to be in the $|1\rangle$ state. (c) A simple model for dephasing, where the phase θ is a random variable. This type of quantum noise has no classical analog, but causes a loss of information about the relative phase between $|0\rangle$ and $|1\rangle$.

the role that entanglement plays in computation, however, without using it, we know that quantum computers lose their advantage [35].

3. A way of whittling down the quantum state to make the "answer" the likely outcome of any readout. Since coefficients in a quantum register represent probability amplitudes that measurement will yield a given outcome, we can get at most N bits of data per measurement [36], as our register immediately collapses into one state upon measurement. To get another value out of the register, we must repeat the whole computation, including loading the state.

1.1.3 Noise

Up to this point we have assumed that there are no noise sources or sources of information loss in our qubit implementations. Unfortunately, reality is not so kind, and as has been discussed before, it is the fragility of a quantum state that remains the main challenge of implementing a large scale quantum computing, an effect called **decoherence**. Equivalently, we can describe this effect as uncontrolled coupling to the environment, either through energy loss or uncontrolled rotations, which leads to loss of information from our quantum computer, as shown schematically in Fig. 1.5 (a), where we see a qubit $|\Psi\rangle$ interact with the environment $|\Psi_{\text{env}}\rangle$. As we are unable to make a good projective measurement of the environment, the output state after the unitary interaction U with the environment cannot be well described in the vector notation we have been using this far, and some information about the state is irrevocably lost. The challenge of including these sources of noise

into our view of quantum computing is to figure out how to model the uncontrolled environment[8]. The primary way to describe such an interaction is to switch to a density matrix representation of our state, which allows us to describe a subsystem of a composite quantum system, i.e. to ignore the portion of the state lost to the environment. Indeed, this is the most complete way to describe noise processes and information loss of our state, however rather than introduce a more powerful and complex, but otherwise equivalent, description of quantum mechanics, we can instead model noise processes as interactions with a controlled and known environment, such as another qubit, as in Figs. 1.5 (b) and (c). We can categorize interactions of our qubits into two general classes: relaxation (sometimes called amplitude damping), and dephasing (sometimes called phase damping), which collectively lead to decoherence.

The first class of error, **relaxation**, causes our population to decay towards the ground state $|0\rangle$ each time it is applied with probability γ. We can think about this sort of process as a loss of energy from the qubit system, and in a way is analogous to classical relaxation, for example of an pendulum which gradually loses energy to the environment or an atom in an excited state that decays. An equivalent circuit for such a process into a controlled environment (a second qubit) is shown in Fig 1.5 (b), where the portion of the state in $|1\rangle$ undergoes a gradual rotation $R_y(\theta)$ towards the $|0\rangle$ state, where the phase θ is chosen to represent the probability of a relaxation event: $\sin^2(\theta/2) = \gamma$. We represent the permanent loss of the information as a projective measurement made on the second qubit. This error is commonly quoted in literature as a T_1 time, where T_1 is a time constant that gives us the rate at which a state will decay towards the ground state. Thus the probability of a relaxation event occurring after time t is given by:

$$P(|1\rangle \rightarrow |0\rangle, t) = 1 - e^{-t/T_1} \tag{1.18}$$

The second form of error, **dephasing**, is one that does NOT have a classical analog, and represents randomization of the phase between states in the qubit or qubit register. Understanding the effect of this sort of noise is harder than for relaxation since there is no classical analog, however if we permit ourselves a Bloch sphere representation of a qubit, we can visualize it as a randomization of the φ angle. An equivalent circuit, again using a second qubit to simulate the environment is shown in fig. 1.5 (c). We represent an irretrievable loss of information to the environment as a projective measurement on the second qubit.

[8]Or, we could replace the environment with something we CAN control and measure, an approach attempted in [37].

This error rate is commonly quoted as the T_2 time, the rate that phase information is lost to the environment. In the case of a single qubit evolving under completely uncorrelated (Markovian) noise, this would be the end of the story, however in most systems, we also define a T_2^*, an ensemble dephasing time. In the case of single qubits that evolve under quasi-static noise [9] or multi-qubit systems that operate under an inhomogeneous background, we can use correlations in the noise or the static nature of the inhomogeneous background to "rephase" our qubits [38, 39]. We can think of this effect as coming from the fact that the phase evolves at a predictable rate over the timescale of operations, such that by applying an appropriate sequence of gates, we can unroll whatever phase was accumulated. In this case, the T_2 time becomes the dephasing time after application of rephasing gates, while T_2^* is the ensemble dephasing time, assuming measurement over a longer timescale than the correlation time and without correcting for inhomogeneities.

1.2 Making Qubits in Semiconductors

Having described the basic ideas of quantum computing, our next challenge is to find a physical system that can implement the operations that we discussed above. This problem can be distilled to that of finding a quantum two-level system conforming to a set of criteria that were first laid out by David DiVincenzo, criteria that are widely considered to be the standard checklist for any qubit system [40]. They are:

1. A scalable physical system with well-characterized qubits.
2. The ability to initialize a fiducial qubit state, such that the state of the system is known prior to any quantum operations.
3. Decoherence times in the qubit subspace that greatly exceed the gate operation time.
4. A universal set of quantum gates.
5. The ability to perform measurements on individual qubits.

Although these criteria set out some requirements for useful qubits, they are certainly not so prescriptive that there is a dearth of systems that could fulfill them. It is in this context that ion-trap qubits, photonic qubits, NMR based qubits, superconducting qubits and

[9] Quasi-static noise is noise that is approximately constant over the timescale of qubit operations. More formally, we can define it as non-Markovian noise, that is there is some correlation in the noise that we can learn and correct by appropriate application of dynamical decoupling.

semiconductor-based qubits are being investigated as the base of a quantum computer, each satisfying the criteria to varying degrees. I will focus on semiconductor-based qubits for the remainder of this thesis. This type of qubit has the potential to utilize the extraordinary processing capabilities of modern semiconductor manufacturing. Despite narrowing the focus to semiconductor systems, there are still many choices of two-level subspace we could use. I will not attempt to cover all the variations of qubit that exist; rather I will focus specifically on two general designs, quantum dots and Majorana zero modes, which in many ways share similar control and readout. As such the discussion of physics in this section will largely be confined to III-V materials, although I will point out that as my thesis is aimed at the general problem of architecting a quantum computer, many of the results presented may are extensible to quantum systems beyond spins and Majoranas. Before we begin a detailed discussion of qubits in semiconductors, let's first take a look at the physics that underlie most of these implementations; the 2-dimensional electron gas (2DEG).

1.2.1 The 2-Dimensional Electron Gas

The 2-dimensional electron gas (2DEG) is the foundation for many of the experiments and qubit-realizations to follow and is a confinement of electrons in a semiconductor to a single plane. To fully appreciate what this means, we first have to discuss what it means to confine an electron in one of the three dimensions. How do we make a confining potential that can create a sheet of electrons a single electron thick? How narrow would such a potential have to be? To answer this question, we must look at the solutions to Schrödinger's equation in a semiconductor. These solutions will give us the distribution of the electron wavefunction, and an idea of its "size". The following introduction is based on material taken from [41, 42, 43].

In a crystalline material, such as a metal or a semiconductor lattice, we can think about electrons as traveling through a periodic potential, caused by the periodic spacing of nuclei in the lattice, as is shown in Fig. 1.6 (a) for a 1D lattice. There will be two sets of solutions; one for electrons that are bound around nuclei which will form the valence band and one for free electrons which will form the conduction band. The gap between these two solutions forms a band gap of size (E_G), a range of energies for which there are no available states. As we are looking at the 2DEG, let's focus on free electron solutions for now. These solutions will take the form of Bloch waves, expressed as a function of lattice position r and wave-vector k:

$$\psi_{\vec{k}}(\vec{r}) = e^{i\vec{k}\cdot\vec{r}} u_k(\vec{r}) \tag{1.19}$$

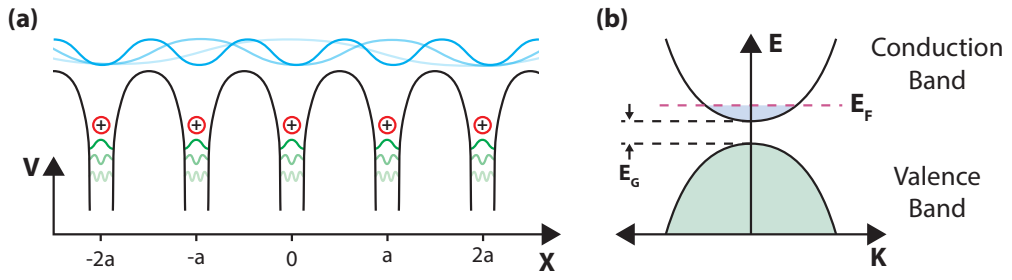

Figure 1.6: (a) Given a periodic lattice that creates a set of potential wells, the valid solutions for unbound electrons (conduction band) are plane waves with a wave vector proportional to the lattice spacing a, while solutions for bound electrons (valence band) are proportional to the strength of the potential created by the constituent elements of the lattice. (b) Assuming there are no electron-electron interactions, and the lattice may be treated as a small perturbation to plane wave solutions (the nearly-free electron model), the band structure will be parabolic, with a band gap E_G between the valence and conduction bands, where there are available states. Electron states are filled to the Fermi energy (E_F).

where u_k is a periodic function with the same periodicity as the crystal lattice and $e^{i\vec{k}\cdot\vec{r}}$ are the general form of plane waves. What this equation effectively means is that if we are able to solve around boundary conditions for a single unit cell, we can extract a band structure for the entire lattice.

Electrons in this system begin to fill the available states from the lowest energy up, obeying the Pauli exclusion principle which limits each available state to two electrons with opposite spins. For conduction band electrons in uniform crystals, we can make two additional assumptions that aid in the interpretation of the solutions to the Bloch equation. First, let's assume that there are no electron-electron interactions. Although this assumption may at first be unintuitive, it appears to be sufficient to describe much of the physics that follows. Second, we assume that the potential due to the lattice is screened by valence band electrons, and can be treated as a small perturbation to a free electron. Solving this model leads to bands which are similar to free electron plane waves up to the edge of the Brillouin zone, i.e. up to the top of the band. In the conduction band of a semiconductor, we deal with largely empty bands. As such, the dispersion relation, i.e. the energy of electrons as a function of the wave-vector, can be approximated as that of free electrons:

$$E(\vec{k}) = \frac{\hbar^2|\vec{k}|^2}{2m^*} \tag{1.20}$$

where $\vec{k}$ is the electron wave-vector and m^* is the effective electron mass that derives from the perturbation of the lattice. The effective electron mass in this instance is a scaling factor on the increase in energy as wave-vector changes and is defined as the curvature of the

Crystal	Lattice Constant (Å)	Electron Effective Mass(m^*/m_e)
Si	5.43	-
Ge	5.658	-
GaAs	5.65	0.066
InAs	6.06	0.026
InSb	6.48	0.015

Table 1.1: Lattice constants and effective electron masses for some common semiconductors. For Si and Ge semiconductors, which are indirect band gap semiconductors, the effective mass for electrons is not trivial and will vary based on direction and valley state, hence values are not given above. Values are taken from [44, 45].

conduction or valence band of the semiconductor:

$$m^* = \hbar^2 \left(\frac{\mathrm{d}^2 E}{\mathrm{d}k^2} \right)^{-1} \tag{1.21}$$

Intuitively, we can think of it as describing a change in momentum for a given energy "kick". For a parabolic and isotropic band, such as for the bottom of the conduction band in a III-V semiconductor, its value is constant, however the form of the effective mass will be more complex for materials that have directional dependencies (such as Si), or more complex band structures such as graphene. From Eqn. 1.20, we can also give the formal definition for the Fermi energy. The **Fermi energy** (E_F) is the energy of the highest filled electron state at zero temperature. This situation is represented schematically in Fig. 1.6 (b) for a single dimension. In 3D, the Fermi energy forms the surface of a sphere in momentum space delineating the region where electron states are filled, which we call the Fermi surface. Finally, we can define the **Fermi wavelength** λ_F of an electron at the Fermi surface, effectively the size of an electron in our semiconductor. Using $k = 2\pi/\lambda$ we find:

$$\lambda_F = \frac{h}{\sqrt{2m^* E_F}} \tag{1.22}$$

If we wish to confine electrons in a given dimension, the Fermi wavelength gives us the length-scale on which we must form our confining potential. For metals, the large number of free electrons means the Fermi energy is large, and as such we end up with a Fermi wavelength on the order of a few Ångström (where 1 Å $= 1 \times 10^{-10}$ m). In semiconductors, as the number of free electrons, and hence the Fermi energy, is set by the doping and is generally small, the Fermi wavelength can be on the order of a few 10s of nanometers. Parameters for some common semiconductors are given in Table 1.1. Given these values, if

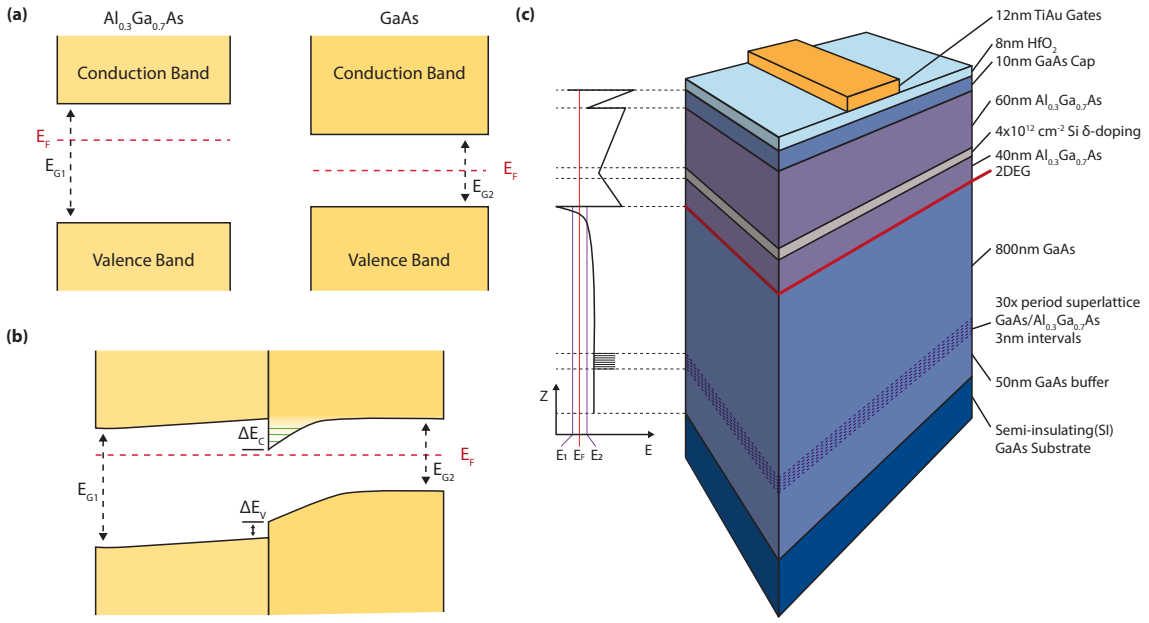

Figure 1.7: (a) Shows a straddling type heterojunction between $Al_{0.3}Ga_{0.7}As$ and GaAs with two differing bandgaps E_{G1} and E_{G2}, where the smaller gap (E_{G2}) is fully enclosed in the larger gap E_{G1}. (b) When the two semiconductors are equalized, their bands bend near the heterojunction to ensure a continuous Fermi energy. Far from the junction, the unmodified band structure is restored. (c) The layer stack of a GaAs/(Al,Ga)As heterostructure, with TiAu surface gates that can locally modify the density of the 2DEG.

we can make a potential well with a width W that's on the order of the Fermi wavelength, we can confine electrons to a few subbands. The next question is: how do we create a narrow quantum well?

The answer is to create a heterojunction; an interface between two dissimilar semiconductors with different band-gaps. The simplest type of heterojunction we can form is a straddling (type I) junction, where one semiconductor has a smaller band-gap that is contained within the band gap of the other, a situation that is represented schematically in Fig. 1.7 (a). In the case that the Fermi levels of the two semiconductors are unequal, electrons tunnel through the junction to align their levels, leading to band bending at the interface. Careful choice of semiconductors can cause a well to appear at the interface, where the width of the well can be designed to be on the order of the Fermi wavelength in the semiconductor. GaAs and (Al,Ga)As are an ideal choice for this type of heterojunction as they are almost perfectly lattice matched (their lattice constants differ by 0.14%), while also forming a straddling-gap heterojunction. The gap in GaAs is $E_{G1} = 1.424\,\text{eV}$ and the gap in $Al_xGa_{1-x}As$ can be continuously varied by changing the ratio of Al and Ga in the semiconductor, taking the value $E_{G2} = 1.424 + 1.225x$ eV. Furthermore, between $x = 0$ and $x = 0.44$, the bandgap

is direct and ratio of the step in the conductance band (ΔE_C) to the step in valence band (ΔE_V) is a constant: $\Delta E_C/\Delta E_V = 1.5$[46] [see steps in Fig. 1.7 (b)], allowing the depth of the well to be easily varied. Finally, by doping the semiconductor with Si, we can move the Fermi energy up to populate a single subband, leading to a 2-dimensional plane of electrons, where there is only a single wave-vector in the Z direction (k_z) that electrons can take. As long as the electron temperature is far below the energy gap of the subbands, only this subband will be populated.

The structure of a typical GaAs/$Al_{0.3}Ga_{0.7}$As heterostructure is shown in Fig. 1.7 (c). Such structures are normally grown by molecular-beam epitaxy (MBE) which allows atomically smooth layers to be grown a single monolayer at a time. We start with a semi-insulating GaAs substrate, over which a large buffer is grown. Repeated thin layers of GaAs/$Al_{0.3}Ga_{0.7}$As are grown to reduce the dislocation density and create a continuous, smooth single crystal at the heterojunction, and to trap impurities which may percolate upwards during the annealing stage of the growth. The red line represents the 2DEG itself on the schematic, followed by a region of Si δ-doping, used to pin the Fermi level in the substrate, and a 10 nm GaAs cap to protect against oxidation. During processing, a protective oxide barrier (either HfO_2 or Al_2O_3) is grown, followed by surface gates which allow the density of states to be locally modified, or even depleted, to define structures in the 2DEG. The oxide layer, apart from serving as a passivation barrier, is also necessary to prevent tunneling of electrons from the surface gates into the donor layer, where the movement of electrons is known to be a significant source of charge noise [47, 48].

Having confined electrons into 2-dimensions, we can now redefine several of the parameters that we had above. First, our dispersion relation becomes that of free electrons in two-dimensions:

$$E(\vec{k}) = \frac{\hbar^2|\vec{k}|^2}{2m^*} \qquad\qquad |\vec{k}|^2 = k_x^2 + k_y^2 \tag{1.23}$$

We can also define the density of states (DOS) in 2-dimensions as the number of states $n(E)$ per unit energy (E):

$$\rho_{2D} = \frac{\mathrm{d}n(E)}{\mathrm{d}E} \tag{1.24}$$

For free electrons in 2D, the states fill an area in momentum-space up to k-vector k:

$$A = \pi k^2 = \frac{2\pi m^* E}{\hbar^2} \tag{1.25}$$

where we've substituted equation 1.23 for k. The spacing of states in a crystal of size $L \times L$

is given by $\pi^2/4L^2$, so for a unit area, the area of a single state is $A_{\text{single}} = \pi^2/4$. Putting this together, the number of states up to energy E is therefore:

$$n(E) = g_s g_v \frac{A}{A_{\text{single}}} = g_s g_v \frac{m^* E}{2\pi\hbar^2} \tag{1.26}$$

and giving a density of states:

$$\rho_{2D} = g_s g_v \frac{m}{2\pi\hbar^2} \tag{1.27}$$

where g_s is the **spin degeneracy** (almost always 2), and g_v is the **valley degeneracy** (1 for III-V semiconductors, 3 for Si). Importantly we note that the density of states is independent of energy, a situation which is unique to 2-dimensions. Finally, we redefine the Fermi energy, wave-vector and wavelength in terms of the total electron density (n_s), which give the following equations:

$$E_F = \frac{n_s}{\rho_{2D}} = \frac{2\pi\hbar^2 n_s}{m^* g_s g_v} \qquad k_F = \sqrt{\frac{4\pi n_s}{g_v g_s}} \qquad \lambda_F = \sqrt{\frac{\pi g_s g_v}{n_s}} \tag{1.28}$$

Having detailed the formation of 2DEGs, we must now consider the factors that will affect their quality for experimental purposes. Broadly, the two most important effects that will affect the quality of the 2DEG are temperature and scattering. First, the main effect of temperature will be to create a distribution of filled states around the Fermi energy, rather than a sharp cut-off as we had previously assumed. This distribution is called the Fermi-Dirac distribution and takes the form:

$$f(E - E_F) = \left[1 + \exp\left(\frac{E - E_F}{k_B T}\right)\right]^{-1} \tag{1.29}$$

This thermal population places an additional constraint on 2DEG formation, namely that the thermal energy $k_B T$ should be much less than the 2D subband spacing, a requirement that is easily met for most heterostructures below a few Kelvin. Second, we account for the effect of scattering, which we capture in the form of a length that an electron can travel before scattering. Depending on the scattering mechanism this can either be inelastic, normally due to scattering off phonons (thermal scattering), or elastic, normally due to scattering off lattice defects or impurities. Therefore we define two length scales, l_ψ being the inelastic scattering length, which gives us the length scale over which total kinetic energy and momentum are conserved, and l_e being the elastic scattering length, which gives the length of time an electron will travel before any collision. From this, we can also define

the momentum relaxation time, the amount of time between electron collisions, given by $\tau = l_e/v_F$.

In general, we are more interested in the effect of scattering on conductivity, an easily measured bulk property of the semiconductor. We can reframe the scattering time into a conductivity by considering the motion of an electron through a lattice. Let's define a quantity called the drift velocity v_d as the average speed an electron moves through the lattice under an accelerating field E. Then, by Newton's second law:

$$eE = \frac{m^* v_d}{\tau} \tag{1.30}$$

If we rearrange for v_d we find:

$$v_d = \mu E \qquad \left(\text{where } \mu = \frac{e\tau}{m^*}\right) \tag{1.31}$$

where μ is a quantity called mobility, with units $\text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$. To find the conductivity, we remember the definition for current density, which will be given by the number of electrons that pass an area per second:

$$J = n_s e v_d \tag{1.32}$$

This is combined with the definition of conductivity, which is simply the current density per electric field, $\sigma = J/E$. From here, we find the equation for conductivity in terms of electron density and mobility to be:

$$\sigma = n_s e \mu \tag{1.33}$$

We will revisit these equations, adding quantum corrections where necessary, and expand on scattering mechanisms within a 2DEG in Section 1.3.

At this point, our discussion splits into two streams. The first deals with the formation of quantum dots, structures with tight confinement in all three dimensions, and is covered in Section 1.2.2. The second deals with the characterization of 2DEGs, extracting the mobility, density, strength of the spin-orbit interaction, via weak (anti-)localization measurements and the quantum Hall effect, and is covered in Section 1.3. Both of these are crucially important for building a variety of qubits in semiconductors, and many of the advances in both spin qubits and topological qubits stem from improvements in materials science that have led to higher quality 2DEGs and the availability of exotic material systems.

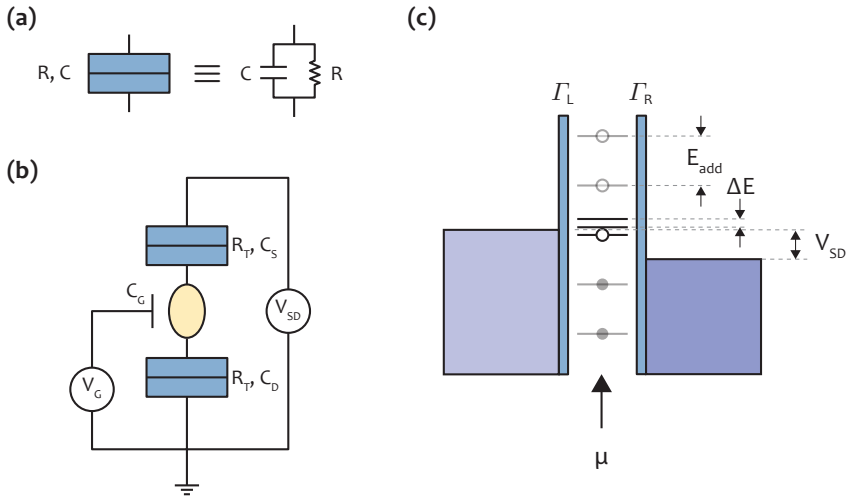

Figure 1.8: (a) We define a tunnel junction as a combination of a resistor and a capacitor in parallel since for a quantum dot the geometric capacitance of the junction is significant. (b) Equivalent circuit model of a quantum dot. The dot is connected to reservoirs by a source and drain tunnel junction, where we define the drain as ground. A voltage $V_S D$ may be applied across the quantum dot, which may cause current to flow. The levels of the quantum dot can be tuned by a gate voltage V_G that is capacitively coupled to the quantum dot. (c) Schematic of a quantum dot showing a "ladder" of states, and orbital energy level. When a level falls within the source-drain bias window current may flow across the dot, otherwise current is blocked, an effect termed Coulomb blockade.

1.2.2 Quantum Dots

Let's now consider the question of how we might use the 2DEG to form a qubit. This can occur in many different ways, for example through the creation of superconducting Josephson junctions with a 2DEG to tune the Josephson energy [49] or in Majorana zero modes [50], formed using a 2DEG as a starting point, a topic we shall explore in Section 1.2.4. By far the most well studied 2DEG based qubit is the zero-dimensional quantum dot, used to confine electrons using surface gates to define zero-dimensional "puddles" of electrons [9, 18]. These puddles of electrons, which in a semiconductor have dimensions on the order of the Fermi wavelength λ_F, creates a discrete spectrum of available states, a situation akin to having an atom with a set of orbital modes defined in the middle of your 2DEG [51]. Before considering a quantum dot in a semiconductor, let's start by looking at a small metal island, which will not have well resolved orbital modes but can still contain a discrete, well defined, number of electrons.

To understand how this is possible, we begin with the formula for the energy on a capacitor, the same one that we initially give for a classical capacitor. This is given by: $E =$

$Q^2/2C$. The energy to add a single extra electron to this island is the **charging energy**:

$$E_C = \frac{e^2}{2C_\Sigma} \tag{1.34}$$

where C_Σ is the total capacitance to the dot. We then couple this island to two reservoirs, say a source and a drain, both with resistance R_t. Realistically, these coupling resistances each add a capacitance term, which we must consider in our C_Σ term, as shown in Fig. 1.8 (a). We can also add a gate nearby that we can use to pull electrons on and off the island. This situation is represented schematically in Fig. 1.8 (b). You might ask what differentiates this system from a circuit I could make on my bench with three capacitors and two resistors. In other words, what are the conditions for the number of electrons on the dot to be well defined? Firstly, we want the thermal energy in the system to be much smaller than the charging energy; otherwise, we won't have a well-defined ground state:

$$k_B T \ll E_C \tag{1.35}$$

Next, we want to ensure that tunneling occurs at a slow rate relative to the Heisenberg uncertainty relation $\Delta E_C \Delta t \geq h/2$. If this condition is not met, dots can hop on and off the dot faster than we could resolve them. The tunneling time is given by $\tau = R_t C$, the time constant of the system. Combining τ and E_C, we derive our second restriction:

$$R_t \gg h/e^2 \tag{1.36}$$

This quantity h/e^2 is called the vonKlitzing constant, or the quantum or resistance, and will show up throughout this thesis in several contexts; as the resistance of a 1D channel, the resistance of an edge state in the quantum Hall and spin quantum Hall effect and the tunneling rate through coupled Majorana zero modes, and has the value $R_K = 25\,812.807\,\Omega$.

From here, we can define the total energy of the quantum dot with N electrons. To do this, we will use a semi-classical model called the constant-interaction model. This model defines the energy in terms of the background charge N_0, and [10], the voltage and the capacitance of the source, drain, and gate. At this point we can work in the limit of a small-sized dot relative to the Fermi wavelength, and reintroduce the orbital energy levels $E_n(B)$. Here $E_n(B)$ is defined as the energy of the n-th orbital under a magnetic field B. This gives the

[10] We can think of the background charge N_0 as the quantized equivalent of the Fermi energy. It is equivalent to $E_F = N_0^2 E_C$, and tells us how many electrons are in the dot at zero gate voltage.

equation for total energy of the quantum dot as:

$$U(N) = \frac{[-|e|(N - N_0) + C_S V_S + C_D V_D + C_G V_G]^2}{C_\Sigma} + \sum_{n=1}^{\lfloor \frac{N}{g_s g_v} \rfloor} E_n(B) \tag{1.37}$$

Note that we've included the spin and valley degeneracies in the filling of the orbital states of the quantum dot in the summation of $E_n(B)$. We can also define the electrochemical potential $\mu(N)$ of the dot:

$$\begin{aligned} \mu(N) &\equiv U(N) - U(N-1) \\ &= \left(N - N_0 - \tfrac{1}{2}\right) E_C - \frac{E_C}{|e|} \left(C_S V_S + C_D V_D + C_G V_G\right) + E_n(B) \end{aligned} \tag{1.38}$$

Note that we've assumed that we are tunneling into the lowest unoccupied orbital energy level E_n. It is a reasonably simple modification to Equation 1.38 to calculate the chemical potential of tunneling into an excited orbital state. The most important difference between the chemical potential μ and the energy E is the linear dependence on gate voltage, which allows us to draw a "ladder" of states where the gap between each state is a fixed value:

$$E_{\text{add}}(N) = \mu(N+1) - \mu(N) = E_C + \Delta E_n \tag{1.39}$$

This is depicted schematically in Fig. 1.8 (c). This equation also shows us that the electrochemical potential of the dot can be swept linearly by varying the gate voltage.

The next question we might ask is: how can we flow current through the dot. Current can only flow via the addition of an electron from the source ($N \rightarrow N+1$) and the removal of an electron to the drain ($N+1 \rightarrow N$), which only occurs when the electrochemical potential $\mu(N)$ falls within the source-drain window of the reservoirs for some N:

$$E_F - \frac{|eV_{SD}|}{2} \leq \mu(N) \leq E_F + \frac{|eV_{SD}|}{2} \tag{1.40}$$

This leads to a peaked conductance spectrum at low source-drain bias as a gate voltage is swept (as in Fig 1.9 (a)), or diamond-like regions of blocked conductance as source-drain bias is swept as a function of gate voltage (as in Fig 1.9 (b)), an effect termed Coulomb blockade. The spacing of Coulomb diamonds allows the extraction of charging energies and addition energies, as well as the lever arm α. This is the ratio of gate capacitance to total capacitance for each gate that is swept. The width of Coulomb peaks reveals information about the temperature of the electrons, as high electron temperatures smear the population

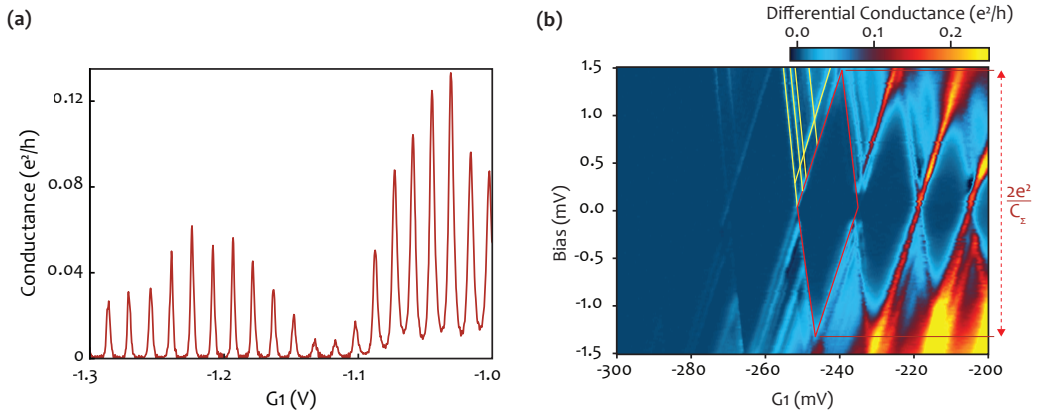

Figure 1.9: (a) Coulomb blockade through a single quantum dot. Current can only flow at points where the energy levels in the dot are in alignment with the reservoirs, which occurs as the gate voltage is swept. (b) Sweeping bias as well as the gate, we get diamond-like features as the levels move into and out of the bias window. The charging energy can be extracted by looking at the width of a diamond, as shown in red, and increases as the size of the dot is reduced by a more negative confining potential. We can also see excited states within each diamond, highlighted in yellow on a single diamond. These correspond to orbital modes within the quantum dot.

in the source and drain reservoirs. I do not give a derivation of this effect here; however, we point the curious reader to [52], and note that this is the method by which we extract electron temperatures in Section 2.3.

Double Quantum Dots

Before we move onto a discussion of how we might use these to form qubits, I will introduce the double quantum dot, where we couple two single dots together. Much like we can consider a single quantum dot an artificial atom, so too we can consider two quantum dots that allow tunneling of electrons between each side as an artificial molecule. The extension of the single quantum dot picture to a double quantum dot picture occurs by adding a tunnel junction between the left and right dots, and adding a gate to control the electrochemical potential of the second quantum dot, as shown in Fig. 1.10 (a). To completely model the effect of a double quantum dot, we must account for two additional sources of capacitance, first a cross-capacitance between the left (right) gate and the right (left) quantum dot, and second the capacitance between the left and right dot. Intuitively, we can understand the capacitance between dots as a new electron on the left dot shifting the energy and chemical potential of the right dot or vice-versa, leading to a shift in the locations of charge transitions as electrons are pulled on and off each quantum dot. To characterize the effect of the two gates on a double quantum dot, we can plot the ground state occupancy of the quantum dots as each of the gate voltages is swept, in a plot called a charge stability diagram. A mock-

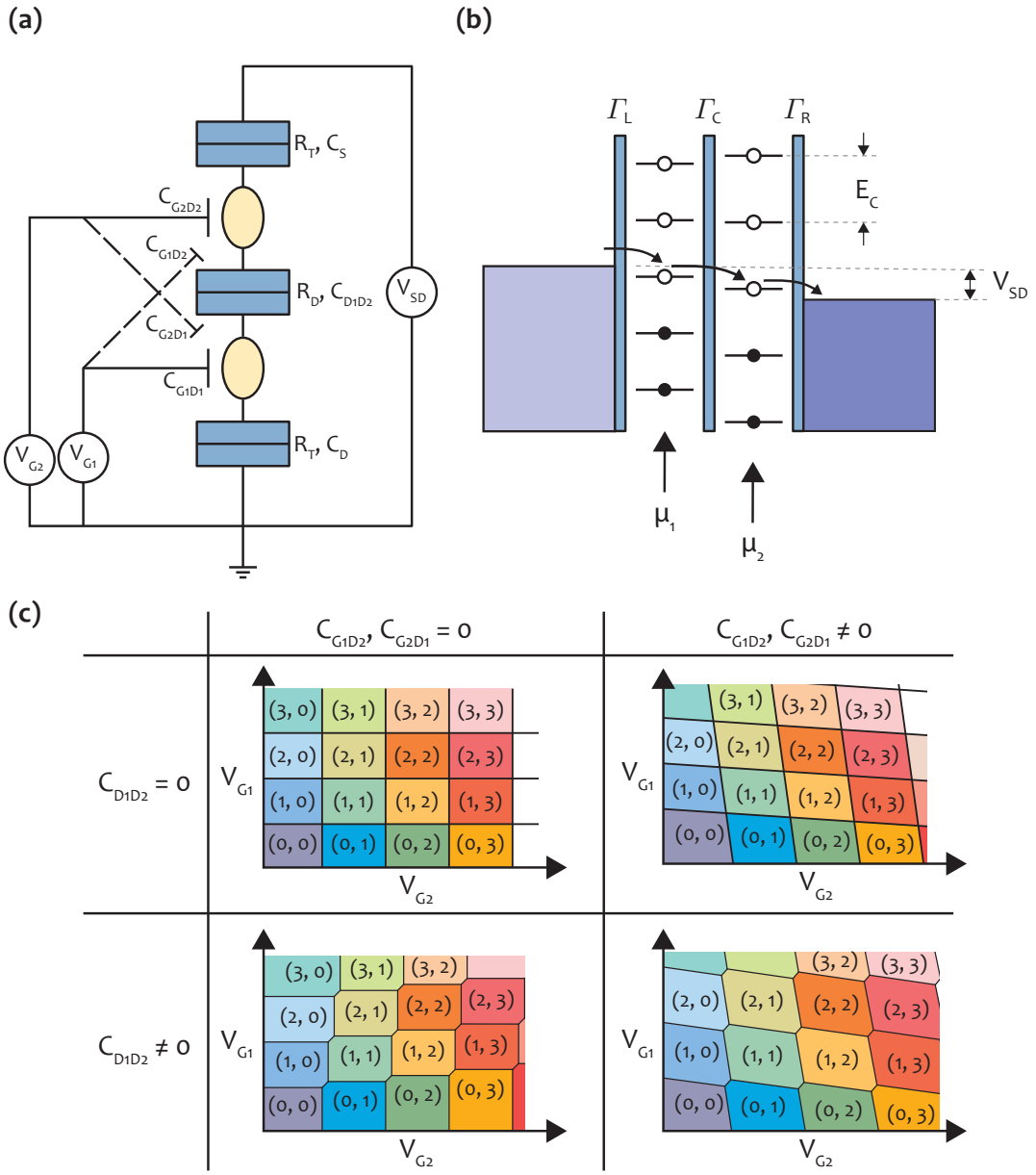

Figure 1.10: (a) Equivalent circuit model for a double quantum dot. The circuit is very similar to that of two single quantum dots in series, except that we must also account for cross capacitances between adjacent gates (the terms C_{G1D2} and C_{G2D1}), as well as the contribution of the tunnel junction between the left and right dots (the term R_D and C_{D1D2}). (b) Energy levels in a double quantum dot system. For current to flow through this circuit, there must be an available level in both the left and right quantum dots. (c) Here we map out the effect of cross capacitance and inter-dot capacitance on the charge stability diagrams of a double quantum dot system as V_{G1} and V_{G2} are varied. As each V_{G1} (V_{G2}) becomes more positive, more dots are pulled onto the left (right) quantum dot. If gate capacitance is non-zero, the lines take on a slope. If inter-dot capacitance is non-zero, each stable configuration splits into a hexagonal cell. Note that these drawings do not include the effects of tunneling between dots.

up of charge stability diagrams are shown in Fig. 1.10 (c) as both interdot capacitance and gate cross-capacitance are turned on and off. The occupancy of the double quantum dots is labeled (N, M) where N represents the occupancy of the left double quantum dot and M represents the occupancy of the right double quantum dot.

As with a single quantum dot, we can define the energy of the double quantum dot system using the constant interaction model:

$$U(N,M) = \frac{[-|e|(N-N_0) + C_S V_S + C_{G1D1}V_{G1} + C_{G2D1}V_{G2} - |e|MC_{D1D2}]^2}{C_{\Sigma,1}} + \frac{[-|e|(M-M_0) + C_D V_D + C_{G1D2}V_{G1} + C_{G2D2}V_{G2} - |e|NC_{D1D2}]^2}{C_{\Sigma,2}} + \sum_{n=1}^{\lfloor \frac{N}{g_s g_v} \rfloor} E_{n,1}(B) + \sum_{m=1}^{\lfloor \frac{M}{g_s g_v} \rfloor} E_{m,2}(B) \quad (1.41)$$

where we have added terms C_{G1D2} and C_{G2D1} to represent the cross capacitance between opposite gates and dots, and C_{D1D2} is the capacitance between dots. The electrochemical potential for each dot can also be defined in a similar way:

$$\mu_1(N,M) \equiv U(N,M) - U(N-1,M) \quad (1.42)$$

$$\mu_2(N,M) \equiv U(N,M) - U(N,M-1) \quad (1.43)$$

The constant interaction model, however, has limited power to describe the effects of tunneling between two dots, as it assumes that the occupancy of each dot is a good quantum number, a situation which will not hold near charge degeneracy points, specifically when tunneling rates between the two dots is significant. If we wish to include a finite tunnel rate, we must move to a Hubbard model that includes the effects of quantum fluctuations, spin and orbital states on each dot [53]. In this model, and indeed in most descriptions of double quantum dots, we describe the strength of tunneling between the two quantum dots as a **tunnel coupling**. This model allows us to draw a schematic of the continuous evolution from a single quantum dot to a double quantum dot as the strength of the inter-dot tunnel coupling is increased. For example, in Fig. 1.11 (a) we see the evolution from the case with large tunnel coupling (zero tunnel resistance), i.e. a single quantum dot in i., to a region of intermediate tunnel coupling in ii., and finally small tunnel coupling, i.e. a wholly separated quantum dot, in iii. In the limit of smaller tunnel couplings (larger tunnel resistance), the bending of charge transitions will continue to be visible at each charge transition as in Fig 1.11 (b), where the transitions of the constant interaction model (grey)

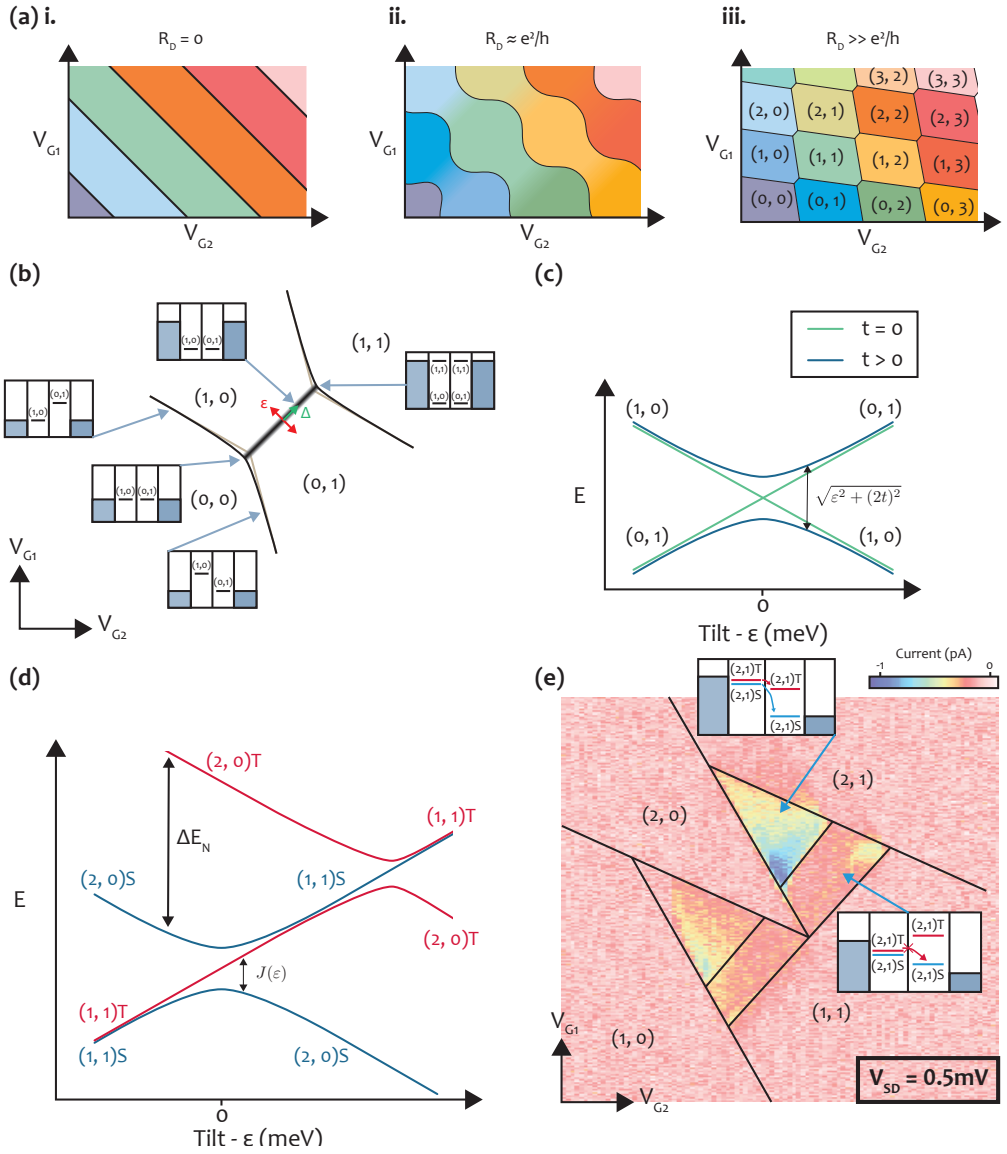

Figure 1.11: (a) Effect of varying R_D, the tunneling rate between the two dots. At low resistance, the dot effectively reverts to a single quantum dot. As the resistance is increased towards e^2/h, two separated dots begin to form, although the transition between them is tunnel broadened. Finally, if the resistance is much larger than e^2/h, there are well defined transitions between left and right dot. (b) Zoom up of a single honeycomb cell around the $(0,0)$, $(1,0)$, $(0,1)$ and $(1,1)$ charge transitions. Insets show energy levels $\mu_1(N,M)$ of the left quantum dot and $\mu_2(N,M)$ of the right quantum dot where bracketed numbers indicate the charge occupancies of both dots. We define the tilt (offset) axes perpendicular (parallel) to the inter-dot transition in red (green). (c) Calculated energy levels along the $(0,1) \rightarrow (1,0)$ charge transition according to a full quantum model. For finite tunnel coupling, an avoided crossing is formed. (d) Calculated energies of singlet and triplet spin configurations for a two-electron double quantum dot. Due to the Pauli exclusion principle, the $(2,0)T$ state is not accessible until we reach the first excited orbital state, such that the $(2,0)T$ level is energetically inaccessible at zero tilt. We define the exchange energy $J(\varepsilon)$ as the energy between the $(1,1)S$ and $(1,1)T$ states. (e) Current through a double quantum dot at $V_{SD} = 0.5\,\mathrm{mV}$. Charge transitions split into finite bias triangles which reveal the presence of excited orbital states in the dot, as well as the effects of spin, which blocks transport through the orbital ground state of the dot.

are compared to a full Hubbard model (black).

We can examine in further detail a single honeycomb cell in the charge stability diagram of a dot that includes both a cross-capacitance and an inter-dot capacitance. In the insets of Fig 1.11 (b) we map out the energy levels of a quantum dot at various points according to the constant interaction model. In this case, looking at the $(0,0),(0,1),(1,0),(1,1)$ transition, we find two points where three charge transitions meet, so-called triple points, where energy levels within both the left and right dot are aligned with the reservoirs. If we were to try and pass a current through such a system, it would only be at these points that a current would flow. In between these triple points we find a new inter-dot transition, which comes from the fact that $\mu_{(1 \text{ and } 2)}$ is now a function of gate voltage *and* the occupancy of dot $(2$ and $1)$. This dependence on the occupancy is a result of the inter-dot capacitance and leads to an additional penalty that must be overcome to load an electron on both left and right dots. Hence, the point where we move to the $(1,1)$ charge configuration is pushed up in both V_{G1} and V_{G2}, and a $(0,1) \rightarrow (1,0)$ interdot transition appears. To further analyze this charge transition, we rotate ourselves to align with the inter-dot transition and define two new perpendicular axes. Tilt (ε) is defined as movement perpendicular to the interdot charge transition and is shown in red. It measures the relative charge configuration of the dots ($\varepsilon = \mu_1 - \mu_2$) while keeping the overall charge of the two dots constant. Offset (Δ) is defined as movement parallel to the interdot charge transition and is shown in green. It measures the total charge offset $\Delta = \mu_1 + \mu_2$ without modifying the relative distance between levels in the left and right dot. In this way, we can move through the charge stability diagram in a way that ignores the effects of cross capacitances [54].

Having defined the tilt axis, we can analyze in detail the inter-dot charge transition, which for moderate tunnel couplings will show charge hybridization near the interdot charge transition. At these points, the charge becomes a bad quantum number and electrons become delocalized across the two quantum dots, leading to a blurred charge transition [as sketched in Fig 1.11 (a) ii.]. If we calculate the energy of the two charge states along the tilt axis, plotted in Fig. 1.11 (c), we find that a finite tunnel coupling leads to the formation of an avoided crossing (blue), compared to no tunnel coupling (green), which at the center will have a gap of $2t$. As a function of tilt, we find the difference in the gap between the two states is:

$$\Omega(\epsilon) = \sqrt{\varepsilon^2 + (2t)^2} \tag{1.44}$$

The charge hybridization also allows the measurement of tunnel coupling by measurement of the charge state near zero tilt, which for intermediate tunnel couplings will vary smoothly between $(0,1)$ and $(1,0)$[55].

Spin

The final effect we must include to describe the relevant physics is spin. Electrons are fermions, meaning they have half-integer spin and obey the Pauli exclusion principle, an effect we've run into before when we considered the filling of bands in a semiconductor. As a quick reminder, the spin of a system is described by the spin angular momentum operator $S = [S_x, S_y, S_z]$ and a spin magnitude (principal spin) operator $S^2 \equiv S_x^2 + S_y^2 + S_z^2$. The three orthogonal projections of the spin angular momentum are non-commuting, such that in general as long as we can choose a principal direction, we can describe the state of a system with two quantum numbers: S^2 and S_z, where we have chosen S_z by convention. The values of these operators are:

$$S^2 \left|s, m_s\right\rangle = \hbar^2 s(s+1) \left|s, m_s\right\rangle \tag{1.45}$$

$$S_z \left|s, m_s\right\rangle = \hbar m_s \left|s, m_s\right\rangle \tag{1.46}$$

where you might see that the spin state is defined by two quantum numbers s, the **principle spin quantum number** that gives us the total spin magnitude and m_s, the **azimuthal spin quantum number**, which gives us projections of the spin in different directions. As with angular momentum, the value of m_s varies in integer steps from $\{-s, -s+1, \dots, s-1, s\}$. Therefore, for a single spin, we have two eigenstates (again picking S_z as our basis):

$$\left|\uparrow\right\rangle = \left|s = \tfrac{1}{2}, m_s = +\tfrac{1}{2}\right\rangle \tag{1.47}$$

$$\left|\downarrow\right\rangle = \left|s = \tfrac{1}{2}, m_s = -\tfrac{1}{2}\right\rangle \tag{1.48}$$

At zero magnetic field in GaAs these two spin states are degenerate, however by application of a magnetic field we are able to break the degeneracy of the states such that we can address the two spin states individually, causing a spin splitting $\Delta E = g^* \mu_B B$ where g^* is the Landé g-factor, μ_B is the Bohr magnetron and B is an externally applied magnetic field.

For systems with more than one spin, to find the states the system may occupy, we must take the tensor product of the two individual spins:

$$\left|s_1, m_{s1}, s_2, m_{s2}\right\rangle = \left|s_1, m_{s1}\right\rangle \otimes \left|s_2, m_{s2}\right\rangle \tag{1.49}$$

Thus the spin states of the system are $\left|\uparrow_1\uparrow_2\right\rangle, \left|\uparrow_1\downarrow_2\right\rangle, \left|\downarrow_1\uparrow_2\right\rangle, \left|\downarrow_1\downarrow_2\right\rangle$ However, this representation gives us states in the basis of the two individual spins, which is less useful when the two states are not easily separable, for example near a charge degeneracy point or when two electrons occupy a single dot. It is often more useful to work in terms of total spin and

azimuthal spin for the joint system, which we define in the following way:

$$S^2 = (S_1 + S_2)^2 \tag{1.50}$$

$$S_z = S_{z1} + S_{z2} \tag{1.51}$$

Combining the spins, we find these four states are:

$$|S\rangle = \ |s = 0, m_s = 0\rangle = \frac{|\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle}{\sqrt{2}} \tag{1.52}$$

$$|T_-\rangle = |s = 1, m_s = -1\rangle = |\downarrow\downarrow\rangle \tag{1.53}$$

$$|T_0\rangle = \ |s = 1, m_s = 0\rangle = \frac{|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle}{\sqrt{2}} \tag{1.54}$$

$$|T_+\rangle = |s = 1, m_s = +1\rangle = |\uparrow\uparrow\rangle \tag{1.55}$$

In other words, we have a single state (the **singlet** state), where the two spins are opposite and hence the total spin is zero ($s = 0$), and three states (the **triplet** states), where the two spins are equal ($s = 1$) and have spin angular momenta that take the values $\{-1, 0, +1\}$. In the case that the two electrons occupy a single dot, the Pauli exclusion principle which tells us that two equal spins cannot occupy the same orbital state (position) leads to the $(2,0)T$ state having a higher energy than the $(2,0)S$ state with a gap set by the orbital states of the quantum dot ΔE_N. This is represented schematically in Fig. 1.11 (d), which shows the energy levels of a quantum dot around the $(1,1) \rightarrow (2,0)$ charge transition as a function of tilt. Note that although the singlet state can freely change state around zero tilt, a qubit in the triplet state will not transition into the $(2,0)$ charge configuration until we can populate an excited orbital mode off to the right. This effect is visible in the current through a double quantum dot, which will undergo a rectification due to this spin blockade, as shown in Fig 1.11 (e). Here, we find two finite bias triangles, which are the double quantum dot equivalent of Coulomb diamonds [56]. Charge transport through the quantum dots proceeds via a sequence of electron tunneling events. In the forward direction these would be: $(2,1) \rightarrow (2,0) \rightarrow (1,1) \rightarrow (2,1)$, a sequence that transfers a single electron from the left to the right reservoir. Note that near zero tilt, only a singlet state may be loaded into the left dot in the $(1,1) \rightarrow (2,1)$ transition; however, since we have an effectively infinite source of electrons in the reservoir, this can be easily accomplished. In the reverse direction, the situation depicted in the figure, electrons flow from the right to the left reservoir via the path $(2,1) \rightarrow (1,1) \rightarrow (2,0) \rightarrow (2,1)$. In this direction, the charge transition $(1,1) \rightarrow (2,0)$ will be blocked depending on the spin of the right electron, until

Parameter	Symbol	Value
Lattice Constant (Å)	a	5.65
Dielectric Constant	$\epsilon_r = \frac{\epsilon}{\epsilon_0}$	12.9
Landé g-factor	g^*	-0.44
Electron Effective Mass	(m^*/m_e)	0.066
2DEG Depth (nm)	d	91
Density (cm^{-2})	n_s	1.30×10^{11}
Mobility ($cm^2\ V^{-1}\ s^{-1}$)	μ	4.8×10^6
Fermi Wavelength (nm)	$\lambda_F = \sqrt{\frac{2\pi}{n_s}}$	70

Table 1.2: Representative properties of a GaAs 2DEG used for forming quantum dots, based on material grown by the group of Mike Manfra at Purdue University.

the second orbital energy level is accessible, a situation depicted in the insets of Fig. 1.11 (e). The prevented transition leads to a region of blocked current near the base of the triangle and a reemergence of current once the second orbital becomes accessible or spin relaxation occurs.

As with single spins, away from any charge degeneracy points, these four states are all degenerate. Near zero tilt we get an energy difference that opens between the singlet and triplet states called the exchange energy $J(\varepsilon)$. At this point, the triplet state is doubly degenerate between the T_-, T_0 and T_+ states. Application of a magnetic field creates a splitting between these three levels given by $\Delta E = g^*\mu_B B S_z$, which causes no change to the S and T_0 state, and causes the T_+ and T_- states to split off around the T_0 state. This will useful for defining our two-level subsystem in our discussion of singlet-triplet qubits later on.

Defining Double Quantum Dots on GaAs

Having covered the theoretical description of a quantum dot as well as the physics behind the 2DEG, we can describe the formation of a quantum dot in GaAs. Typical parameters for a 2DEG in GaAs are given in able 1.2, however, the key properties we require are the Fermi wavelength, which will set the approximate size of the dot we wish to form, and the depth, which will set the sharpness of the potential that the gates provide at the 2DEG. For samples that are doped and have an intrinsic density of electrons, we can form quantum dots by evaporating surface gates on top of an insulating dielectric [usually TiAu on top of $\sim$ 10 nm HfO_2 or Al_2O_3, as shown in Fig. 1.7 (c)], and applying negative voltages to deplete electrons below the gate in the 2DEG. Initially, we expect the gate to change the

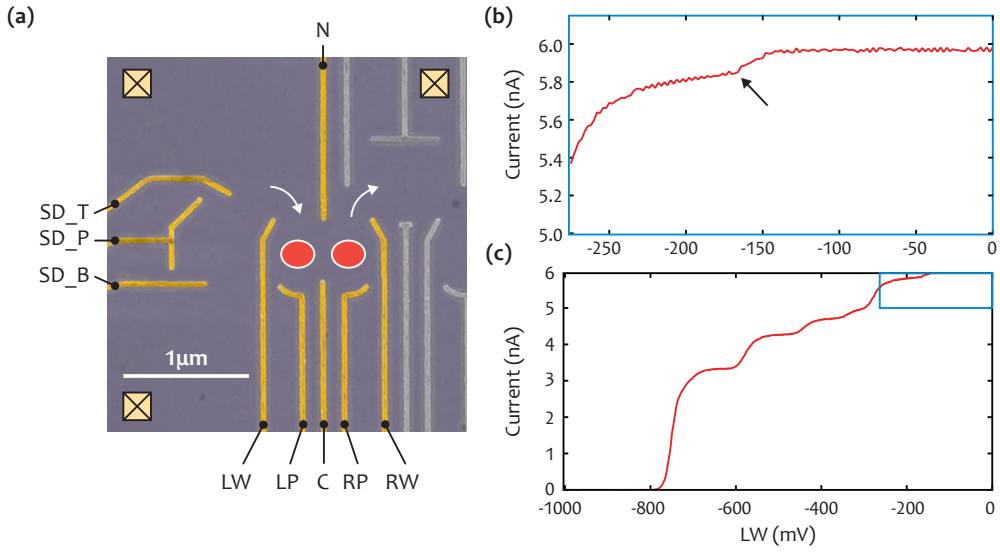

Figure 1.12: (a) False color SEM of a double quantum dot design on GaAs. Surface gates (highlighted in gold) are 12nm TiAu onto which negative voltages are applied to deplete the 2DEG 101nm underneath. The locations of the quantum dots are highlighted with red circles and the ohmic contacts to the 2DEG in yellow boxes. Descriptions of the gates are given in the main text. The width of the double quantum dot at the surface is 970nm. (b) The left wall passing through depletion while pinching off with the nose (set to -800mV), at the location marked with the arrow. All other gates are at zero. (c) A full pinch-off curve of the left wall against the nose. As the undepleted region of the 2DEG shrinks towards the Fermi wavelength, a 1D channel is formed, causing the appearance of quantized conductance plateaus.

density at the 2DEG as per that of a parallel plate capacitor:

$$\Delta n_s = \frac{\epsilon_r \epsilon_0 \Delta V_g}{ed} \tag{1.56}$$

For a gate at depth $d = 101\,\text{nm}$ from a 2DEG with density $n_s = 1.3 \times 10^{11}\,\text{cm}^{-2}$ we expect depletion at around $V_g = -180\,\text{mV}$. After this, increasingly negative gate voltages deplete the 2DEG in a halo around the gate.

Contact is made to the 2DEG via metallic ohmic contacts formed using a eutectic alloy of AuGe, which after evaporation is annealed at approximately 450 °C. A full description of the fabrication process which gives ratios and thicknesses is given in Appendix A, for now, all we need to know is this n-dopes the semiconductor directly under the contact with Germanium causing a contact to be formed to the 2DEG with a resistance of between 20 Ω and a few kΩ depending on the size and quality of the ohmic contact.

The design of gate structures that can confine electrons into quantum dots is an area of continued and fruitful research (see for example Section 4.1 of this thesis), however a common and well-tested pattern for a double quantum dot is shown in Fig. 1.12 (a). Gates

are designed to correspond to the various parameters we described in Section 1.2.2; with the gates labeled LW (left wall) and RW (right wall) controlling the tunnel rates from the reservoirs to the dots, the gate labeled C (center) controlling the tunnel coupling t_c, and LP (left plunger) and RP (right plunger) controlling the chemical potential of the left dot (μ_1) and right dot (μ_2) respectively. The N (nose) gate acts as a global control, and a charge sensor (discussed in Section 2.1.2) which in this case is a third quantum dot formed against the left wall is placed to the left of the device. The location of ohmic contacts is marked by crosses and allows us to measure current both through the device and through the sensor.

The left wall of the quantum dot passing through depletion is shown in Fig. 1.12 (b) at the location marked by the arrow. A full pinch-off trace for the gate is given in Fig. 1.12 (c), showing the appearance of quantized conductance steps as the undepleted region of 2DEG shrinks to towards the Fermi wavelength. These steps appear in units of the spin-degenerate conductance quantum, $R = 2ne^2/h$ for integer n, the physics of which we discuss in more detail in Section 1.3. Several gates on the device are wired up to allow the application of radio frequency tones or fast pulses to drive qubit rotations. Further details of how this is accomplished are given in B.

1.2.3 Qubits from Quantum Dots

As we discussed at the beginning of this section, one of the challenges of quantum computing is finding physical systems suitable to be used as qubits. They must be expressible as a two-level system, isolated enough that the quantum state is preserved during operations, and easily read-out and controlled. The last of these requirements is effectively the same as finding a system whose Hamiltonian (H) can express the operations that we defined in Section 1.1. We use Schrödinger's equation to describe this evolution:

$$i\hbar \frac{\mathrm{d}\,|\psi(t)\rangle}{\mathrm{d}t} = H\,|\psi(t)\rangle \tag{1.57}$$

For this reason, Hamiltonians describing two level systems used in quantum computers are often explicitly defined in terms of the Pauli matrices we defined in equation 1.5. For example, a model qubit Hamiltonian may be given by:

$$H = A\sigma_X + B\sigma_Z = \begin{bmatrix} B & A \\ A & -B \end{bmatrix} \tag{1.58}$$

which describes rotations around an axis of the Bloch sphere at angle $\theta = \tan^{-1}\left(\frac{A}{B}\right)$ and with a rate $\omega_r = \frac{\sqrt{A^2+B^2}}{\hbar}$. By varying the values of A and B, we are able to construct arbitrary rotations around the Bloch sphere. Alternatively, the application of photons at the frequency $\omega_e = 2\sqrt{A^2 + B^2}$ is able to drive transitions between the eigenstates of this Hamiltonian.

The Charge Qubit

Perhaps the simplest form of qubit we can form with a double quantum dot system is a charge qubit. Here we define the logical subspace of the qubit as spanned by two charge states, typically the $(0, 1)$ and $(1, 0)$ charge states, with the basis $|0\rangle = (0, 1)$ and $|1\rangle = (1, 0)$. The single qubit Hamiltonian is given by:

$$H_{\text{charge}} = \frac{1}{2}\varepsilon\sigma_Z + t_c\sigma_X \tag{1.59}$$

which is represented by the energy level diagram in Fig. 1.11. The qubit is typically operated by the application of microwave pulses with frequency $\Omega = \sqrt{\varepsilon^2 + (2t_c)^2}$ in order to drive transitions between the ground and excited charge configurations, and the state is read out via a proximal charge sensor (discussed in Section 2.1.2).

Such a qubit, while conceptually simple is highly sensitive to charge noise in the semiconductor, such that the qubit lifetime T_1 and coherence times T_2 are both on the order of 10 ns[57]. As such, the usefulness of such a qubit is limited.

The Loss-DiVincenzo (Single Spin) Qubit

The next idea for the implementation of a qubit would be to use the spin of a single electron as our two-level subsystem. In many ways, spin is an ideal phenomenon to use. It is naturally two levels, and as such has no leakage states that our qubit may accidentally end up in and can easily be implemented using quantum dots [58]. We can represent the $|0\rangle$ and $|1\rangle$ states by the spin down and up states ($|\downarrow\rangle$ and $|\uparrow\rangle$) respectively. The splitting between the two states is controlled by the application of an external magnetic field that causes a Zeeman splitting $\Delta E_Z = g^*\mu_B B$. Since the spin of an electron does not couple to electric fields (to first order), this gives the single-spin qubit some resistance to charge noise in the semiconductor. Of course, this also makes the control of the qubit more challenging, as we now require an oscillating magnetic field to control the qubit. As such, the Hamiltonian, and the control of such a qubit will vary depending on how we achieve our qubit control. There are four common methods described in the literature for controlling single spin qubits:

1. **Electron Spin Resonance (ESR)** An alternating magnetic field is generated by an alternating current run through a proximal ESR gate, with a frequency matching the Zeeman splitting [59]. However, this method of driving rotations is relatively slow (on the order of a few μs) and requires large microwave powers.

2. **Electron-Dipole Induced Spin Resonance (EDSR)** In materials with strong spin-orbit interaction, we can use the effective magnetic field felt by an electron in motion in a confining potential. Such techniques utilize an AC electric field to "wobble" the electron wave function to drive rotations within a single dot [60, 61]. This technique achieves spin rotations in ≈ 100 ns in GaAs, down to ≈ 10 ns in InAs with a stronger spin-orbit coupling.

3. **Electrically-Driven ESR in a Slanted Magnetic Field** In materials without strong spin-orbit interaction, we can generate an effective oscillating magnetic field by generating a strong magnetic field gradient across a quantum dot with the use of a micromagnet. Again, the "wobble" of the electron wave function drives rotations of single spins in a single dot [62] or between two quantum dots [63]. This technique allows rotations on the order of ≈ 10 ns.

4. **Electrically-Driven ESR in the Exchange Field of an Auxiliary Spin** The use of an auxiliary spin against which we can drive rotations via the exchange interaction again allows electric field control of spin with sub-nanosecond operation times [64]. In many ways, this method of control is similar to that of the singlet-triplet qubit, described below, with the exception that we still use a single spin as our logical subspace. However, such control has not yet been realized.

As mentioned above, although we have first-order insensitivity to electric fields, the slow speed of ESR leads us to reintroduce an electric field coupling, either via intrinsic material properties via the spin-orbit interaction, or through the creation of gradient magnetic fields, to allow for fast control of these qubits. Even then the effect of charge noise is far lower than for a charge qubit, with coherence times of hundreds of microseconds possible. Additional sources of noise originate from the coupling between electron spins and the nuclear spins of nearby spinful nuclei. This effect is termed the hyperfine interaction, and leads to a fluctuating field, termed the Overhauser field, with magnitude:

$$B_{\text{nuc}} = \frac{1}{g^* \mu_B} \sum_n^N A_n I_n \tag{1.60}$$

where I_n is the nuclear spin operator for the n-th nucleus, and A_k is the coupling strength of that nucleus with the electron spin. We can treat the Overhauser field as a classical random variable with a Gaussian distribution around zero net polarization. The RMS fluctuation of B_{nuc} is $\sigma_B = \frac{4.0\,\text{T}}{\sqrt{N}}$ where N is the number of nuclei that an electron in a quantum dot overlaps [65]. For GaAs this is typically on the order of $N \approx 10^6$. This effect is minimized by the use of isotopically purified silicon [66], which contains a reduced density of spinful nuclei.

The Singlet-Triplet Qubit

The use of a single spin, while having a convenient mapping to qubit states, requires either the application of an AC magnetic field or an AC electric field coupled with some form of gradient magnetic field or spin-orbit interaction. By creating ensembles of spin, we can trade off a more straightforward system for one with more flexible control or greater immunity to certain types of noise. The use of two electrons across two quantum dots allows us to use purely pulsed dc control to achieve full control over the qubit. For this type of qubit, we define our computational subspace as spin states of two coupled electrons, choosing $|S\rangle$ and $|T_0\rangle$ as our $|0\rangle$ and $|1\rangle$ state respectively, with a Hamiltonian described by:

$$H = J(\varepsilon)\sigma_Z + g^*\mu_B\Delta B_X\sigma_X \tag{1.61}$$

The fixed gradient field ΔB_X is achieved either through the use of a micromagnet or via the polarization of the nuclear field [67], where ΔB_X describes the difference in the field seen by an electron in the left and right quantum dots. An external magnetic field is required to break the degeneracy of the three triplet states, such that we only operate in the $S - T_0$ states. Any leakage into the T_- or T_+ states is undesirable.

The energy levels of such a qubit are shown in Fig. 1.13 (a). The qubit may be easily initialized in the $(2,0)S$ state via the exchange of electrons with the reservoirs, as the $(2,0)T$ states are energetically inaccessible for small tilt and offset [as we saw in 1.11 (d)]. In general, $S{-}T_0$ qubit rotations are driven around an axis set by the relative magnitudes of J and ΔB_X, as is shown in Fig. 1.13 (b), however, by pulsing tilt, we are able to drive rotations around the Z axis when $J(\varepsilon) \gg g^*\mu_B\Delta B_X$, or around the X-axis when $g^*\mu_B\Delta B_X \gg J(\varepsilon)$. An equivalent way of expressing this is to speak in terms of energy eigenstates: for large $J(\varepsilon)$, the two eigenstates of the qubit are $|S\rangle$ and $|T_0\rangle$, while for $J(\varepsilon) \approx 0$, the energy eigenstates of the qubit are set by the gradient field ΔB_X, with the ground state given by spins anti-aligned with the gradient magnetic field (since $g^* < 0$ in GaAs), and the excited

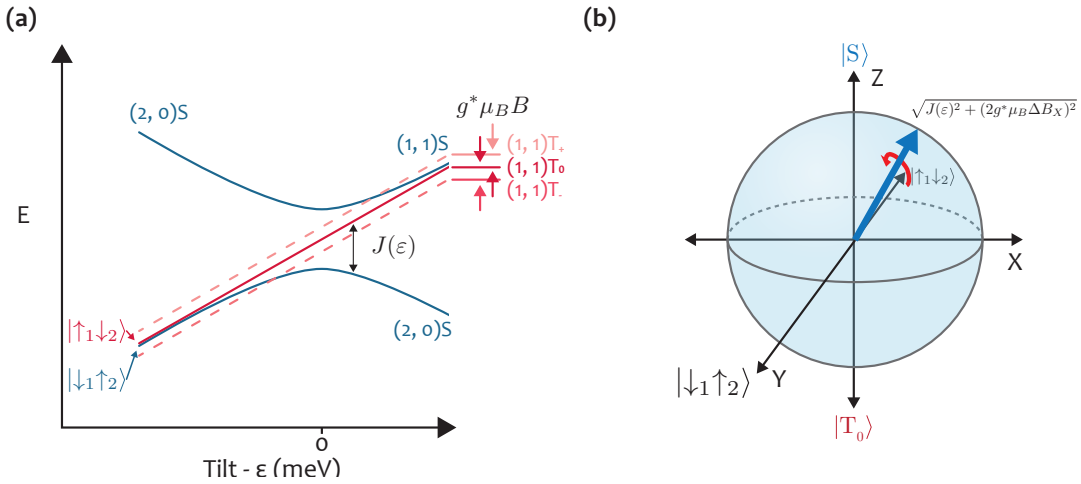

Figure 1.13: (a) The energy levels of a Singlet-Triplet Qubit. The three triplet states are split by the application of a uniform magnetic field B. At a large negative tilt, i.e. $J(\epsilon) \approx 0$, the gradient magnetic field ΔB_X leads to a change in basis, such that the energy eigenstates are described by $|\uparrow_1\downarrow_2\rangle$ and $|\downarrow_1\uparrow_2\rangle$, where here we've arbitrarily chosen $\Delta B_X > 0$. (b) Bloch sphere representation of a single Singlet-Triplet qubit. Qubit rotation proceeds around the axis in blue, which may be varied by pulsing tilt (ε). The gradient field ΔB_X is usually constant, set either by nuclear fields or a fixed micromagnet.

state by spins aligned with the gradient magnetic field. Lifetimes for singlet-triplet qubits are primarily limited by coupling to nuclear spins via the hyperfine interaction [68], which causes fluctuations in the coefficient of σ_X, as well as charge noise that is ever present in semiconductor-based systems [69]. Despite this, coherence times have been extended in GaAs spin qubits to over 200 µs via the use of dynamical decoupling sequences [70].

It is also worth mentioning that there is active research in optimizing the control schemes for singlet-triplet qubits, again with the intention of gaining resistance to certain forms of noise. For example, recent results suggest that variation of $J(\varepsilon)$ by modulation of tunnel coupling t_C, leading to symmetric pulses on the left and right quantum dot [71, 72, 73, 74], or the use of magnetic field gradient estimation and active control [75, 76] may lead to higher fidelity control and reduced dephasing. Further reduction in charge noise is expected with improved materials growth, which is expected to further extend qubit coherence times [48].

The Exchange-Only Qubit

While the singlet-triplet qubit described in the above section allows us to control our qubits with only fast pulses, they still require a spatially varying magnetic field for full two-axis control. The use of three electrons distributed through three quantum dots allows for fully electrical control of a spin qubit using only exchange interactions between the left and center,

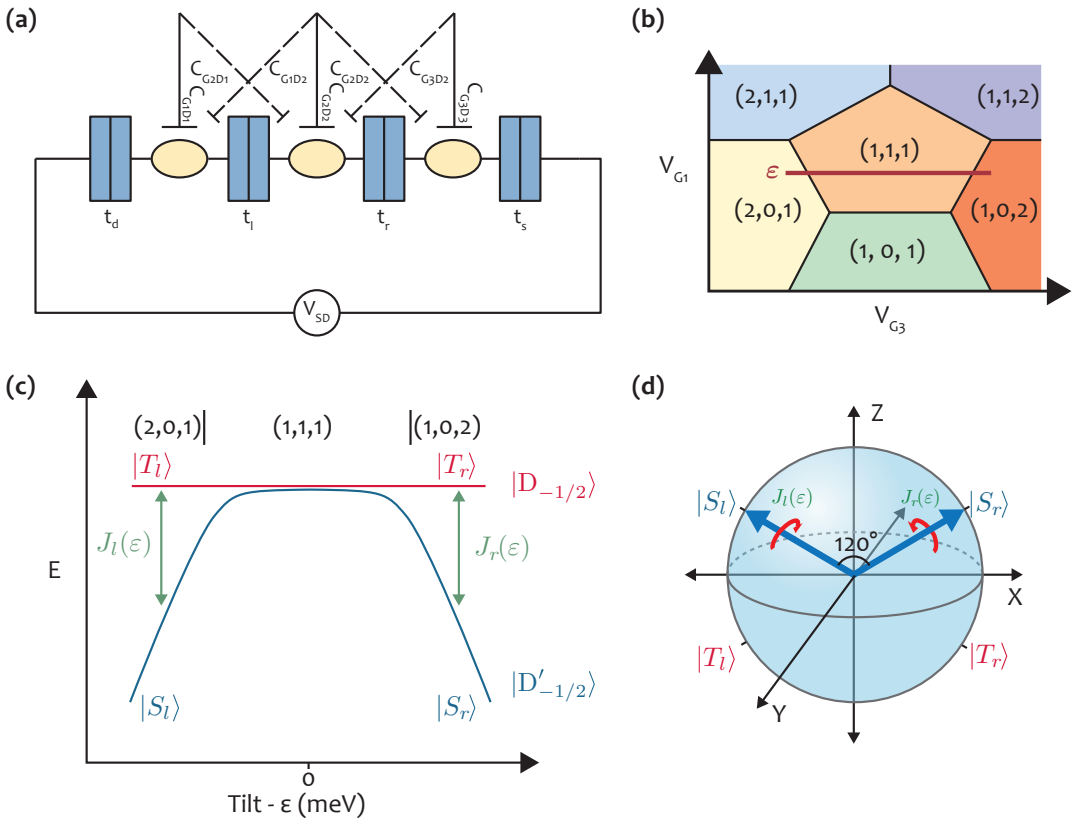

Figure 1.14: (a) Schematic of a triple quantum dot, with tunable tunnel couplings between the left and center quantum dots, and the right and center quantum dots. (b) Charge stability diagram for a triple quantum dot when sweeping the V_{G1} and V_{G3} around the $(1,1,1)$ charge configuration. The tilt axis is marked in red and sweeps from the $(2,0,1) \rightarrow (1,1,1) \rightarrow (1,0,2)$ charge configurations. (c) Energy levels of the exchange-only qubit. Quadruplet states or excited doublet states are not shown. The Exchange energies between the left (right) and center dots are swept as a function of tilt. The energy eigenstates change between $|S/T_l\rangle$ and $ketS/T_r$ at the extremes of tilt. (d) Bloch state representation of the exchange-only qubit. The exchange interaction drives rotation around two axes of the Bloch sphere separated by 120°.

and right and center quantum dots [77], as shown in Fig 1.14 (a) and (b). In this case, the system has a total of eight possible spin states. These are one set of quadruplet states with total spin $S^2 = 3/2$ and spin projections $S_Z = \{-3/2, -1/2, +1/2, +3/2\}$, and two sets of doublet states corresponding to a singlet or triplet in the left (right) dot, and a third spin on the right (left) dot. The choice of placing the singlet/triplet state on the left or right dot is set by the tilt, with the energy eigenstates of the system given by the singlet/triplet state on the left for $\varepsilon \ll 0$, and on the right for $\varepsilon \gg 0$. We can, therefore, write out the four doublet states as [11]:

$$\begin{aligned}
|\mathrm{D}_{-1/2}\rangle &= |\uparrow T_R\rangle \,(\text{for } \varepsilon \gg 0) = |T_L \uparrow\rangle \,(\text{for } \varepsilon \ll 0) \\
|\mathrm{D}_{+1/2}\rangle &= |\downarrow T_R\rangle \,(\text{for } \varepsilon \gg 0) = |T_L \downarrow\rangle \,(\text{for } \varepsilon \ll 0) \\
|\mathrm{D}'_{-1/2}\rangle &= |\uparrow S_R\rangle \,(\text{for } \varepsilon \gg 0) = |S_L \uparrow\rangle \,(\text{for } \varepsilon \ll 0) \\
|\mathrm{D}'_{+1/2}\rangle &= |\downarrow S_R\rangle \,(\text{for } \varepsilon \gg 0) = |S_L \downarrow\rangle \,(\text{for } \varepsilon \ll 0)
\end{aligned} \tag{1.62}$$

In order to break the degeneracy of the third spin, a global magnetic field is applied, such that we are left with our computational basis states, which I arbitrarily choose to be the $-1/2$ states here:

$$|0\rangle = |\mathrm{D}'_{-1/2}\rangle = |S_{l,r}\rangle \tag{1.63}$$

$$|1\rangle = |\mathrm{D}_{-1/2}\rangle = |T_{l,r}\rangle \tag{1.64}$$

Focusing on this subspace, the energy level diagram of the exchange-only qubit is given in Fig. 1.14 (c). We are able to change the exchange energy between the left (right) and center dots by sweeping tilt (ε). We can largely ignore leakage states as the set of four quadruplet states have different principal spin, and the two remaining doublet states are rendered inaccessible by the applied Zeeman field. The exchange-only qubit was first experimentally realized in [78]. In GaAs systems, rotations at rates of up to 47.4 GHz have been measured, with a lower bound of $T_2 = 100$ ns, limited by nuclear spins in GaAs [79].

The fast rotation rate also leads to increased sensitivity to exchange (charge) noise, however improved schemes building on the ideas of the exchange-only qubit [80], such as the Resonant Exchange Qubit [81], the Always-On Exchange-Only (AEON) qubit [82] or the Quadrupolar Exchange-Only Qubit [83, 84], which trade off the number of electrons or requirements to continuously drive the system for insensitivity to certain forms of noise. Additional work with double quantum dots with higher electron occupancies and hence

[11] The full set of eigenstates at different values of J_l, J_r, ε can be found in [78]

higher principal spin quantum numbers are also predicted to have desirable noise rejection, while still allowing fully electrical control, such as the hybrid spin/charge-qubit [85], which has recently shown an ensemble dephasing time of $T_2^* = 8.1\,\text{ns}$ with rotation rate $f_{\text{rabi}} = 2.43\,\text{GHz}$ in GaAs [86] or $T_2^* = 2\,\text{ns}$ with rotation rate $f_{\text{rabi}} = 5.2\,\text{GHz}$ in Si/SiGe [87], which is presently limited by charge noise [88].

1.2.4 Majorana Zero Modes

While the above section details several techniques for building qubits using semiconductor heterostructures, each of them suffers from a significant amount of noise that must be corrected for in order for these qubits to be useful in a quantum computer. For an error rate of 1×10^{-5}, it is estimated that roughly 3,000 physical qubits are required to construct one logical qubit using the surface code, and close to 10,000 gates must be performed per computational gate, to correct errors as they occur [89]. Although single qubit gate fidelities in spin qubits routinely exceed 99%[90], two-qubit gate fidelities of 98% are the highest values the author is aware of at the time of writing [91]. The primary sources of error is uncontrolled coupling to the environment, causing the loss of information stored in the qubits, as well as imprecise control and readout. An alternative approach to building qubits, one that uses the topology of exotic quasiparticles called non-abelian anyons, was proposed by Kitaev as a method of performing quantum computation in a way that is protected from local perturbations in the environment[92].

A system of non-abelian anyons uses as its computational subspace a set of degenerate ground states with a fixed number of quasiparticles, separated by a physical distance, where information is stored over multiple pairs of anyons. A result of this distributed storage is that any local perturbation to a quasiparticle does not lead to decoherence. To quote: "the only way the system can undergo a non-trivial unitary evolution — that is an evolution that takes it from one ground state to another — is by having its quasiparticles braided"[93]. A physical movement or interaction of pairs of anyons is required to change the state of the qubit. In such a way, error rates far below those achievable in other qubit systems may be possible. Rather than requiring many noisy qubits to form one logical qubit, we would be able to use a few, or even a single clean qubit instead. I will not go into further details of how such a computation is achieved via braiding, but will point the interested reader to [93], which gives a far more thorough introduction to the physics than I can in the limited space I have available. I will, however, give a quick introduction into the physical origins of the Majorana zero mode, based on the material from [94].

The challenge, then, is to find a system which contains these emergent quasiparticles.

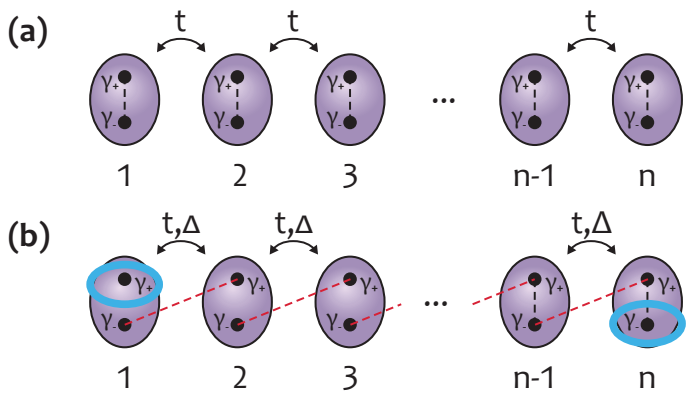

Figure 1.15: (a) Schematic of a 1D chain of fermions under conventional pairing. Although each fermion is broken into two Majorana operators, each pair of operators are tied to a single real particle, and we cannot manipulate them in isolation. (b) A chain where $\mu = 0$ and $\Delta = t \neq 0$. In this configuration the pairing occurs between neighbouring Majorana operators, leaving two unpaired Majorana zero modes (blue) at either end of our chain. We can use four of these unbound states as a topologically protected qubit.

Again, it was Kitaev who proposed that a one-dimensional chain of fermions, with a specific Hamiltonian, may cause the emergence of precisely the quasiparticles we require [95]. The Hamiltonian he proposed was [96]:

$$H = -\mu \sum_j \hat{c}_j^\dagger \hat{c}_j - \frac{t}{2} \sum_j \left(\hat{c}_j^\dagger \hat{c}_{j+1} + \hat{c}_{j+1}^\dagger \hat{c}_j \right) - \frac{\Delta}{2} \sum_j \left(e^{i\phi} \hat{c}_j \hat{c}_{j+1} + e^{-i\phi} \hat{c}_{j+1}^\dagger \hat{c}_j^\dagger \right) \quad (1.65)$$

Here we have a set of sites, indexed by j, with an onsite energy (chemical potential) μ, a hopping term t, and a superconducting coupling term Δ with phase ϕ. The terms $\hat{c}_i$ and $\hat{c}_i^\dagger$ are the fermion annihilation and creation operators respectively. Let's look at a few limits of this Hamiltonian. For $\mu < 0$, and $\Delta, t = 0$, this Hamiltonian describes a wire with a single ground state containing a fixed number of fermions. If we wish to add an extra electron, we must pay an energy cost μ, as in Fig. 1.15 (a). The next case we consider is where $\mu = 0$ and $\Delta = t \neq 0$. We can achieve the first condition, $\mu = 0$, by coupling the wire strongly to a large reservoir of fermions, such that the number of fermions on the wire is not a good quantum number (exactly the opposite of a quantum dot). To understand the effect of the next condition, $\Delta = t \neq 0$, it is helpful to decompose the fermion annihilation and creation operators into Majorana operators:

$$\gamma_+ = \hat{c} + \hat{c}^\dagger \qquad \gamma_- = -i(\hat{c} - \hat{c}^\dagger) \quad (1.66)$$

These are real operators ($\gamma_\pm = \gamma_\pm^\dagger$), they square to 1 ($\gamma_\pm^2 = 1$), and they anticommute

($\{\gamma_+, \gamma_-\} = 0$). Indeed there is nothing special about these operators; I could easily define them for a single fermion state, which would yield:

$$\hat{c} = \frac{1}{2}(\gamma_+ + i\gamma_-) \qquad \hat{c}^\dagger = \frac{1}{2}(\gamma_+ - \gamma-) \tag{1.67}$$

however since both operators are associated with a single wave function, they are inseparable. It does not make sense to operate on a single Majorana operator when they are both associated with a single particle. In fact, I have even drawn my fermions in Fig. 1.15 (a) as a pair of Majorana operators. There is really only one state described by the two operators. The question we need to answer is how do we separate our Majoranas. Let's write down the Kitaev Hamiltonian from Equation 1.65 substituting in our Majorana operators. After some rearrangement (and the removal of a global phase) we find:

$$H = -\frac{\mu}{2}\sum_j (1 + i\gamma_{j,+}\gamma_{j,-}) - \frac{t+\Delta}{4}\sum_j i\gamma_{j,-}\gamma_{j+1,-} - \frac{\Delta - t}{4}\sum_j i\gamma_{j,+}\gamma_{j+1,-} \tag{1.68}$$

Note a number of features: $P_i = (1 + i\gamma_{j,+}\gamma_{j,-})$ gives us the parity of the site i, and the second and third terms give inter-site Majorana couplings. For $\mu < 0$ and $\Delta, t = 0$ we recover the original description of a wire with a set of occupied or unoccupied sites. In the case that $\mu = 0$ and $\Delta = t \neq 0$, we end up with a vacuum state, gapped from the next state by $\frac{\Delta+t}{4}$, but with two unpaired Majorana zero modes $\gamma_{0,+}$ and $\gamma_{N,-}$, which form a zero-energy two-level system. They are protected from local perturbations by their non-local nature, a situation depicted in Fig. 1.15. In fact this "topological" domain extends around the region of $\Delta = t \neq 0$ allowing us to construct topologically protected qubits out of 2 pairs of Majorana zero modes [93].

The experimental challenge is to find a physical system that is similar to that described by the Hamiltonian in Equation 1.65. We can make a 1D chain using the principles we've covered up to this point, with an electron pairing that is similar to that of a superconductor, the complication is that the Hamiltonian describes a set of spinless fermions. The spin of electrons would, unfortunately, prevent the pairing described above. We will cover one such method for forming a spinless 1D superconductor in Sec. 1.3.6, which combines a superconducting 1D system with strong spin-orbit coupling and a parallel magnetic field to create an effective spinless system [97, 98]. At this point, such systems have been experimentally realized, and evidence for the existence of Majorana zero modes is mounting [99, 21]. However, at the time of writing a topologically protected qubit has not yet been observed.

1.3 Characterizing 2DEGs

In the previous sections, we went through how a 2DEG is constructed and wrote down some equations for scattering and conductivity in a 2DEG. These equations have all assumed that the 2DEG is purely classical; however at the temperatures and scales that many of our devices operate, this assumption begins to break down. To explore why this is the case, we must revisit the scattering mechanisms and equations for conductance that we previously wrote down in Equation 1.33 and add some quantum corrections to these equations. As we do this, we can define several regimes for transport where various quantum corrections to transport become apparent.

Before we get started, let's quickly review the scattering lengths that were originally defined in Section 1.2.1. We can classify scattering into two forms, elastic scattering, which occurs when the electron changes direction but not its energy or wavevector, or inelastic scattering, which occurs when the scattering event changes the energy of the electron. Elastic scattering occurs at impurities, or along dislocations and walls, i.e. on scattering sites with a mass much larger than the electron itself. The distance between successive elastic scattering events is called the elastic scattering length l_e[12]. Inelastic scattering occurs via time-dependent mechanisms such as phonons or electron-electron scattering that change and move between each scattering event. As the scatterers have energy and mass on the order of the electron energy and mass, the electron and the scatterer transfer energy readily. In 2DEGs, our assumption that electrons do not interact continues to hold for the effects we wish to explore, and hence, the primary inelastic scattering mechanism is electron-phonon scattering. As phonons are largely thermally generated, inelastic scattering occurs on a length-scale l_i set by the temperature of the sample. Since these scattering events are each unique and time-dependent, the events effectively randomize the phase of the electron, and so the inelastic scattering length l_i is often used interchangeably with l_ϕ, the phase coherence length.

We now have the ingredients necessary to classify transport into several distinct regimes, based on the relationship between the size of the system being measured L, and the various length scales in our system l_ϕ, l_e and λ_F.

- **Classical Diffusive** ($\lambda_F < l_e, l_\phi \ll L$): This is the classical limit of transport, true for large pieces of metal or semiconductor. The system is much larger than any relevant scattering length; hence, electrons travel diffusively through the system, with no coherent effects. This is the regime in which the previously derived equations are cor-

[12] This is sometimes also called the momentum relaxation length, l_m or l_{imp}.

rect, where we have implicitly assumed that each scattering event destroys all phase information.

- **Quantum Diffusive** ($\lambda_F < l_e \ll L, l_\phi$): At this length scale, the electron will still travel diffusively through the system, as $l_e \ll L$, however, phase coherent effects begin to appear, since correlations between the phases of different paths exist for path lengths up to l_ϕ. Weak localization is a quantum correction we must add to Equation 1.33, and appears in 2DEGs at low temperature.

- **Classical Ballistic** ($\lambda_F \ll L < l_e, l_\phi$): At this length scale, electrons travel without collisions, except at the boundaries of the system. As such the energy of an electron may not be dissipated within a system. Dissipation can, therefore, be treated separately from such systems. This also implies that processes are non-local, i.e. they can be described at any point within the system. For example, the boundary of the region describes the current at all points in the system. Effects such as electron focusing occur at this length scale.

- **Quantum Ballistic** ($\lambda_F \approx L \ll l_e, l_\phi$): At this point, discrete orbital energies occur in the confining directions. In 2D, this leads to the emergence of a 2DEG, in 1D a quantum point contact and in 0D a quantum dot.

For this thesis, we will primarily focus on the Quantum Diffusive and the Quantum Ballistic regimes, as they describe the physics of the 2DEG and the quantum dot, respectively. Having already described the physics of the quantum dot, let's look at the quantum corrections that occur in the Quantum Diffusive regime, as they will allow us to extract both the scattering length and the strength of the spin-orbit interaction. As these must be well controlled to form both quantum dots and Majorana zero modes, our understanding of the origins of scattering and the spin-orbit effect will be vital to our journey towards building a large-scale quantum computer. Characterization in this section will be performed in a hall bar, similar to the ones depicted in Fig. 1.16. A current I is applied along the length of the Hall bar. Two quantities are extracted relative to that current, the Hall resistivity $\rho_{XY} = V_{XY}/I$ gives the voltage formed orthogonal to the direction of current flow, and the transverse resistivity $\rho_{XX} = V_{XX}/I$. This second quantity gives us an expression for the conductivity of our sample:

$$\sigma = \rho_{XX}\frac{W}{L} \tag{1.69}$$

where W is the width of the sample and L is the length between contacts. Samples of Hall bars on several samples are given in Fig. 1.16 (b), (c) and (d). Device (b), fabricated on a

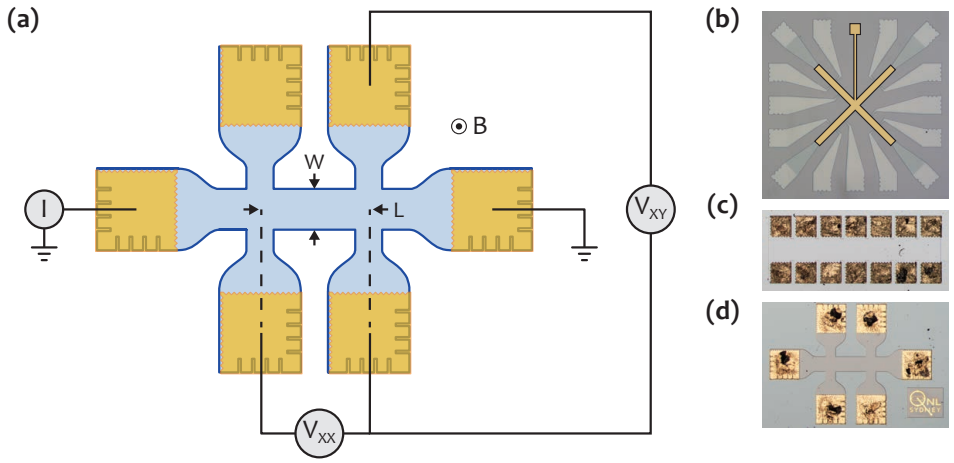

Figure 1.16: (a) Schematic of a Hall bar showing the location of contacts, and relevant dimensions. Care should be taken to ensure that current cannot flow at voltage contacts. (b) A Hall bar on InAs, with Al contacts. Several locations are defined where Hall conductivity and transverse conductivity may be measured, and a global top-gate allows continuous tuning of the electron density. (c) A Hall bar on GaAs, with multiple contacts, allowing measurement of parameters at multiple locations. (d) A Hall bar integrated on a qubit device. Fewer contacts are defined, with a focus on a small footprint, however it allows for characterization of the 2DEG before measurement. Note that for each contact, notches are defined in the mesa and the ohmic contact extends over the edge of the mesa to ensure good contact to edges at high field along multiple crystallographic axes.

shallow InAs quantum well, includes a global top gate that allows the density of electrons in the 2DEG to be tuned continuously. (d) shows a device that is embedded on a GaAs quantum dot device and is optimized for a small footprint. Details on the optimization of ohmic contacts are given in the appendix, Sec. A.2.10.

1.3.1 Weak Localization

To include the effects of phase coherence on conductivity, we will use the so-called Feynman path method to calculate a corrected conductivity. The basic idea of such an approach is to consider what conductivity refers to when considering a small number of scattering sites, in a regime where $\lambda_F < l_e \ll L, l_\phi$. Given a small sample, with a small number of elastic scattering sites within the lattice, we can define the conductivity as the probability that an electron reaches the end point, where it leaves the system, from a given starting point. A schematic of this case is shown in Fig. 1.17 (a). The wavefunction will give this probability at the final point, which is given by the sum of the wavefunctions corresponding to each path through the lattice. For example, the paths may be {start, 1, 2, 7, end} or {start, 8, 7,

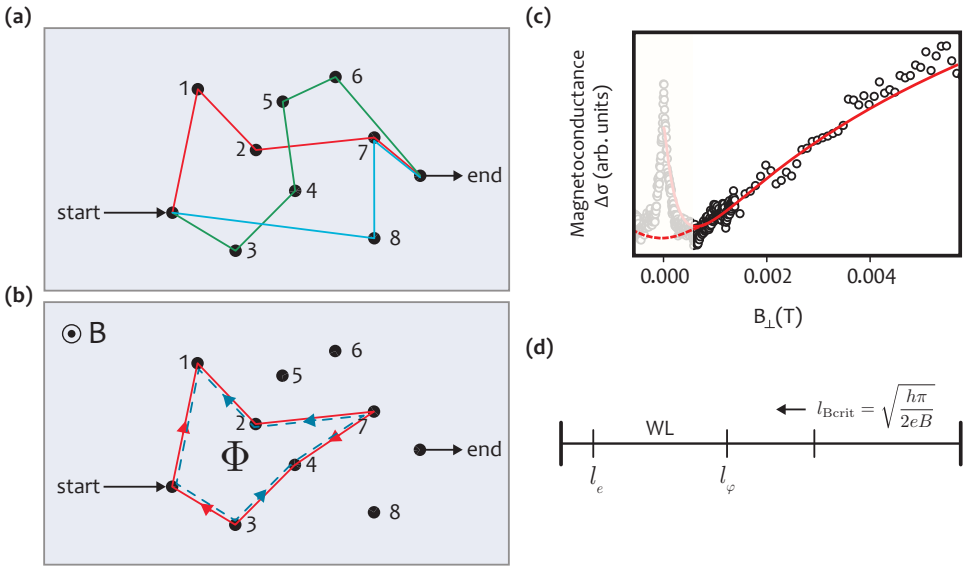

Figure 1.17: (a) To calculate the probability of transmission, we must sum together the wavefunctions for each path through the 2DEG. Scattering sites are represented by numbered dots, and several example paths are highlighted. (b) We can also calculate the probability that an electron will return to its starting location in the same way. Since an electron can travel in both a clockwise and counter-clockwise direction along the loop, there is an increased probability of reflection relative to transmission. (c) Weak localization in an InAs Hall bar. A weak anti-localization peak is seen at zero magnetic field, however, at small magnetic fields, weak localization begins to dominate, and we see a drop in conductance and a gradual recovery with the field as expected. (d) The relevant length scales in the weak localization problem. Weak localization is suppressed as the magnetic length is reduced (the field is increased).

end} etc. The total wavefunction at the end is:

$$\Psi_{\text{start}\to\text{end}} = \sum_j \psi_j = \sum_j t_j e^{i\varphi_j} \tag{1.70}$$

Here t_j is the transmission probability along the path j, and φ_j is the phase accumulated along the path j. The probability of finding the election at the endpoint is, therefore:

$$P(\text{end}) = |\Psi_{\text{start}\to\text{end}}|^2 = \sum_j t_j^2 + \sum_{j\neq k} t_j t_k \cos(\varphi_j - \varphi_k) \tag{1.71}$$

where the first term gives the probability of the electron traveling along a given path j, and the second term gives the interference between each pair of paths through the lattice. Since the phases accumulated along each path are effectively random, this second term will average to zero, and the total forward probability is given by:

$$P(\text{end}) \approx \sum_j t_j^2 \tag{1.72}$$

Next, let's consider paths that return to the starting point. In this case, we have both a clockwise and a counter-clockwise propagating path (which we can label j_+ and j_-), around which, due to the symmetry of elastic scattering, we have the same transmission probability $t_{j_+} = t_{j_-} = t_j$, and the same acquired phase $\varphi_{j_+} = \varphi_{j_-} = \varphi_j$. This situation is represented schematically in Fig. 1.17 (b). The return probability is therefore:

$$P(\text{start}) = \sum_j \left(t_{j_+}^2 + t_{j_-}^2 + t_{j_+} t_{j_-} \cos(\varphi_{j_+} - \varphi_{j_-}) + t_{j_-} t_{j_+} \cos(\varphi_{j_-} - \varphi_{j_+}) \right) = 4 \sum_j t_j^2 \tag{1.73}$$

In other words, "phase-coherent summation of time-reversed trajectories in a diffusive medium leads to an increased probability for electrons to return to their initial position"[41]. To find an expression for conductance, we must find an expression for the probabilities of different paths, and take into account the ratio of elastic and inelastic scattering length (the longer the path, the higher the chance that its phase will be randomized). A full derivation is not given here, I will simply quote the final result, however I point the interested reader towards [41, 100]. The correction to conductance is given by:

$$\Delta\sigma_{2D} = -\frac{1}{4\pi} \frac{2e^2}{h} \ln\left(\frac{l_\phi}{l_e}\right) \tag{1.74}$$

As expected this gives us an reduced conductivity due to the increased probability of coherent back-scattering.

To extract a useful parameter from this, we need some way of differentiating the contribution of weak-localization from the bare conductivity. To do this, we may apply a magnetic field perpendicular to the plane of the 2DEG, to break the time-reversal symmetry of the paths. For a magnetic field $B_\perp$, the phase difference along clockwise and counter-clockwise paths is given by:

$$\Delta\phi(B_\perp) = 4\pi \frac{\Phi}{\Phi_0} = 4\pi \frac{B_\perp A}{\Psi_0} \tag{1.75}$$

At the point where the magnetic field induces a $\pi/2$ phase shift around a loop, the destructive interference will be suppressed, thus the effect of longer loops will be suppressed as a magnetic field is applied. A measurement of weak localization on an InAs Hall bar is shown in Fig. 1.17. Near zero field, there is a weak-antilocalization peak, a topic we cover in Sec. 1.3.4, however for fields slightly above zero we see the reduction in conductivity and gradual increase towards the bulk value we expect. Assuming paths are roughly circular we can approximate the length scale that a $\pi/2$ phase change between forwards and backwards

propagating paths corresponds to as:

$$l_{\text{Bcrit}} = \sqrt{\frac{h\pi}{2eB}} \tag{1.76}$$

We therefore expect weak-localization to start getting suppressed when $l_{\text{Bcrit}} \approx l_\phi$, and the conductivity to return to the bare value when $l_{\text{Bcrit}} \approx l_e$. This is shown in Fig. 1.17 (d). The exact form for the correction for weak localization unfortunately does not have a simple form [101], however for a diffusive approximation, where $l_e \ll l_\phi$, we can use the reasonably simple form given by [102]:

$$\Delta\sigma_{2D}(B_\perp) = -\frac{2e^2}{\pi h}\left[\digamma\left(\frac{1}{2}+\frac{B_0}{B_\perp}\right) - \digamma\left(\frac{1}{2}+\frac{l_e}{l_\phi}\frac{B_0}{B_\perp}\right)\right] \tag{1.77}$$

where $\digamma$ is the digamma function and

$$B_0 = \frac{v_F m^{*2}}{2hel_e n_s} \tag{1.78}$$

Note that the diffusive approximation may not hold for high mobility GaAs samples, where the elastic scattering length is large. Alternate forms are available in [101] which may be required for such samples.

1.3.2 The Quantum Hall Effect

As the field perpendicular to the sample is applied, which for brevity we refer to as B, apart from a modification to conductivity we can also ask what occurs to the Hall (perpendicular) voltage and conductivity. As we saw in the Equation 1.31, the application of an electric field leads to a drift velocity in the sample set by the scattering time τ and the effective mass of electrons m^*. In combination with the magnetic field B, this leads to a Lorentz force $F = e\vec{v} \times \vec{B}$, causing a charge build-up along one edge of the Hall bar. The charge build-up is balanced out by an opposing electric field that is formed:

$$E_y = -e\vec{v} \times \vec{B} \tag{1.79}$$

To find the Hall resistivity, we can combine the electric field with the equation for current density, given in Equation 1.32, to find

$$\rho_{XY} = \frac{E_y}{J_x} = \frac{B}{n_s e} \tag{1.80}$$

Hence, we find a linear relationship between magnetic field and Hall resistivity with a gradient proportional to the electron density, as seen in Fig. 1.16.

As the magnitude of the magnetic field is increased, electrons are curved into roughly circular paths, with a radius:

$$R_c = \frac{m^* v_F}{eB} \tag{1.81}$$

and an angular frequency of:

$$\omega_c = \frac{v_F}{R_c} = \frac{eB}{m^*} \tag{1.82}$$

Once we are in the limit that $R_c \ll l_e$, we can write down a Hamiltonian for the system:

$$H = \frac{(P + eA)^2}{2m^*} + U(x, y) \tag{1.83}$$

where P is the momentum operator, $U(x, y)$ gives the confining potential (boundaries) of the sample, and A is the magnetic vector potential. We can choose the gauge of the vector potential such that:

$$\vec{A} = (0, Bx, 0) \tag{1.84}$$

and expand the Hamiltonian, ignoring the Z component as we only have a single mode:

$$H = \frac{p_x^2}{2m^*} + \frac{(p_y + eBx)^2}{2m^*} \tag{1.85}$$

We note that the Hamiltonian is translationally invariant in the y-direction and can be rewritten as:

$$H = \frac{p_y^2}{2m^*} + \frac{1}{2} m^* \omega_c^2 (x - x_0)^2 \tag{1.86}$$

where we've substituted ω_c from Equation 1.82 and $x_0 = \frac{p_x}{eB}$.

This Hamiltonian corresponds to that of a harmonic oscillator centered at x_0 with energy levels

$$E_n = \hbar \omega_c \left(n + \frac{1}{2} \right) \tag{1.87}$$

This implies that at high field, and neglecting the effects of scattering, our density of states evolves to a series of discrete delta functions, where each state is highly degenerate, filled up to the state $E_n < E_F$. Each of these states is called a **Landau level**. This situation is described by the schematic in Fig. 1.16. Up to this point, we've ignored the effects of scattering, however we can give a brief phenomenological description of its effect. For the case that the quantum Hall effect is beginning to appear, and $R_c \sim l_e, l_\phi$, the Landau levels become broadened, although the exact mechanism by which this occurs is not yet resolved

[103, 104]. An additional effect we have thus far ignored is spin. We can, however, trivially add it to our energies:

$$E_n = \hbar\omega_c \left(n + \frac{1}{2}\right) \pm \frac{1}{2} g^* \mu_b B \tag{1.88}$$

Finally, we introduce a parameter to describe the number of electrons per magnetic flux quantum, which corresponds to the number of Landau levels below the Fermi energy:

$$\nu = \frac{n_s}{B/\Phi_0} = \frac{n_s h}{eB} \tag{1.89}$$

As we've moved to the Landau level description of states inside the 2DEG, you might expect that the conductivity of the sample should also be modified, as we now no longer have free states at the Fermi level. This intuition is indeed correct, and the bulk of a Hall bar in the quantum Hall regime will be insulating. Current is carried at the edges of the sample, where the confining potential curves upwards, and Landau levels intersect with the Fermi level [105] as shown in Fig. 1.16. This gives rise to a series of chiral, 1D channels that carry current around the edges of the Hall bar. Since these edge states are directional, and edges flowing in the opposite direction are physically separated by the width of the Hall bar, backscattering is strongly suppressed, and edges provide dissipationless transport, i.e. $\rho_{XX} \to 0$.

What about the Hall resistance, ρ_{XY}? The number of edges that will cut through the Fermi level is given by $N_{\text{max}} = \lfloor \nu \rfloor$, each of which will contribute to the total conductivity. The total conductivity is the sum of the conductances of each of the channels. Let's assume a difference in the chemical potential of both sides of $\delta\mu = \mu_2 - \mu_1$. The total current across the sample is given by the product of the velocity $v_n(E)$ and the density of states $\rho_{\text{1D},n}$.

$$J = e \sum_n^{N_{\text{max}}} \int_{\mu_1}^{\mu_2} v_n(E) \rho_{\text{1D},n}(E) \mathrm{d}E \tag{1.90}$$

By a similar line of reasoning to Equation 1.24, we calculate the 1D DOS to be:

$$\rho_{\text{1D},n} = \frac{1}{2\pi} \left(\frac{\mathrm{d}E_n(k)}{\mathrm{d}k} \right)^{-1} \tag{1.91}$$

And the velocity from quantum mechanics is simply:

$$v_n(E) = \frac{1}{\hbar} \frac{\mathrm{d}E_n(k)}{\mathrm{d}k} \tag{1.92}$$

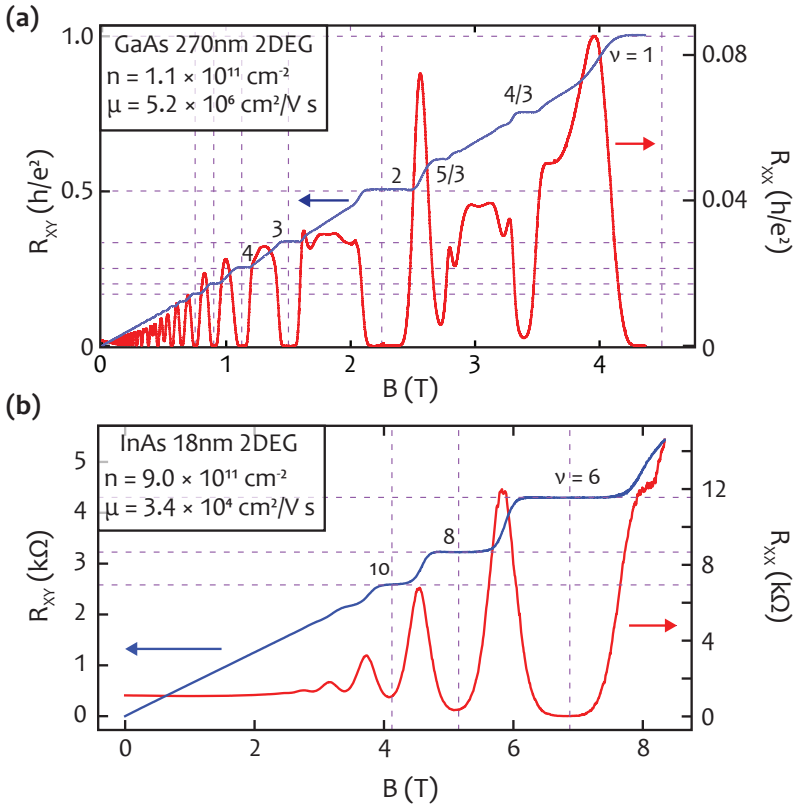

Figure 1.18: (a) The integer quantum Hall effect in a high mobility GaAs 2DEG. The locations of filling factors are calculated using Eq. 1.89 and overlaid as dotted purple lines, while expected conductances are calculated using Eq. 1.94. (b) The same data except on an shallow InAs 2DEG. The higher density results in filling factors being shifted to higher magnetic fields. The lower mobility of the sample means plateaus are not visible up to high fields.

Hence, the total current is:

$$J = e\sum_{n}^{N_{\max}} \int_{\mu_1}^{\mu_2} \frac{1}{h} \mathrm{d}E = \frac{eN_{\max}\delta\mu}{h} \tag{1.93}$$

This remarkable cancellation between the DOS and velocity is unique to 1D channels and leads to the emergence of the conductance quantum that we alluded to in section 1.2.2. The difference in chemical potential is related to the voltage by $\delta\mu = eV$, and the conductivity is therefore:

$$\sigma = \frac{J}{V} = \frac{N_{\max}e^2}{h} \tag{1.94}$$

Therefore, we find the conductance of the edge will be quantized in units of the conductance quantum, with a value determined by the filling factor, which gives us the number of conducting 1D channels parallel to the edge in the samples. As an example of this, ρ_{XX} and

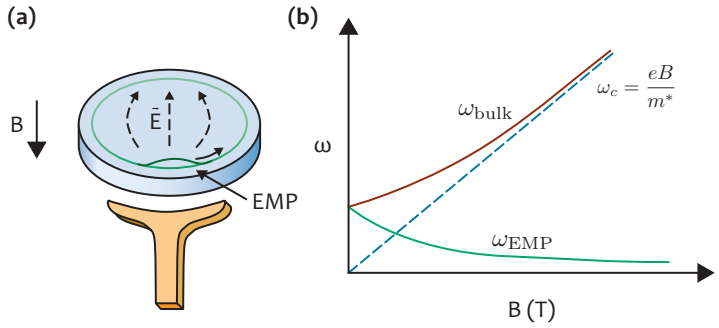

Figure 1.19: (a) Schematic of edge magnetoplasmon propagation. An external magnetic field is applied pointing into the Hall droplet. (b) Frequency of the EMP ω_{EMP} mode and bulk plasmon ω_{bulk} mode in a circular quantum Hall droplet with increasing magnetic field. At a high magnetic field, the bulk mode approaches the cyclotron frequency, while the edge mode has an approximately $1/B$ dependence on the field.

ρ_{XY} are both plotted on the same axes in Fig. 1.18, for two samples with distinct mobilities.

1.3.3 Edge Magnetoplasmons (EMPs)

The edge states of the Hall effect support charge density excitations, that we term **edge magnetoplasmons** (EMPs). Such edge excitations are distinct from bulk plasmon (drum) modes and propagate with a distinct frequency and dispersion that is set purely by the properties of the edge. Classical descriptions for such excitations were first given in the 1980s, on 2DEGs formed on the surface of liquid Helium [106, 107, 108]. We can understand the existence of such modes in a semi-classical picture. Consider a 2DEG running along the x direction, placed in a magnetic field, where the confining potential E_y causes the appearance of edge states. A local perturbation, such as a gate voltage, can cause a dipole to form across the plane of the sample, leading to an electric field that induces a propagating current $J = \sigma_{XY}E$ around the edge. As electrons are confined to travel at an angle $\theta_H = 90°$ to the edge of the sample in a single direction; this creates a charge density wave (and hence electric current) to propagate around the edge, which causes procession of the field around the disc, and hence a self sustaining oscillation. This situation is sketched in Fig. 1.19 (a). Substituting Equation 1.94 and Equation 1.89 into our expression for current density we find:

$$J = n_s e \frac{E}{B} \tag{1.95}$$

The resultant oscillatory modes are confined to the perimeter of the Hall sample and travel with a phase velocity v_D approximated by the ratio of electric and magnetic fields at the edge. To find the frequency of the EMPs, the details of the confining potential and edge

must be calculated. From [109], the excitations are found to have a fundamental angular frequency of:

$$\omega_{\text{EMP}} = \frac{\sigma_{XY}}{P\epsilon_0\epsilon^*}\left(\ln\left(\frac{P}{\pi w}\right) + C\right) \tag{1.96}$$

where P is the length of the edge, ϵ^* is the effective dielectric constant of the edge and C is a constant related to the geometry of the edge, which goes to 1 for a sharply defined edge with a step-like potential. The logarithmic correction arises due to electron correlations (which in this case does cause a measurable modification to frequency), and w represents the damping and physical width of the EMP from the edge:

$$w = i\frac{\sigma_{XX}(\omega)}{2\omega\epsilon_0\epsilon^*} \tag{1.97}$$

Note that this quantity does not necessarily go to zero on plateaus. In the limit of low transverse resistivity, ignoring electron-electron interactions ($\omega\tau \ll 1$), and taking the limit that $\omega_{\text{EMP}} \ll \omega_c$, we can approximate this term as:

$$w \approx \frac{n_s m^*}{2\epsilon_0\epsilon_r B^2} \tag{1.98}$$

These equations collectively show that the EMP travels at a significantly reduced frequency, which decreases with field, roughly proportionally to $\frac{1}{B}$. Comparing the EMP frequency to that of a bulk plasmon in Fig. 1.19 (b), one sees that while the fundamental bulk plasmon frequency ω_{bulk} approaches the cyclotron frequency ω_c, the EMP frequency ω_{EMP} decreases towards zero. This slow and directional propagation is exploited in Section 3.1 and Section 3.2 to construct compact circulators using the integer quantum Hall effect and the quantum anomalous Hall effect.

1.3.4 The Spin-Orbit Interaction

Within a solid, we've thus far assumed that the spin or an electron is independent of its motion through that semiconductor, apart from a tangential mention in Sec. 1.2.3, where we discussed its usefulness in controlling spins in semiconductors. Up to this point, we've captured the effects of the band structure of a semiconductor in the effective electron mass m^*. In reality, the band structure of a semiconductor is shaped in a complex way by the motion of electrons through the electric field created by atoms in the lattice of a crystal. This can cause both directional and spin-dependent modulation of the band structure. For this thesis, I will not aim to give a general description of the the spin-orbit interaction,

which contributes to a whole host of effects such as the fine structure of Hydrogen and the heavy/light hole structure of GaAs, but rather give an intuitive understanding of its origins in the conduction band of a semiconductor. Hence, the terms that I introduce here should not be considered to apply generally, but rather is specific to conduction band electrons in direct band-gap semiconductors. This treatment is partly derived from [110, 111].

Firstly, as we are dealing with conduction band electrons, which have a net spin angular momentum of zero ($\vec{S} = 0$), we do not have any band splitting from the atomic orbitals. Instead, the spin-orbit effect (SOI) in conduction band electrons comes from effective potential seen by an electron. Consider an electron moving through an asymmetric potential within a semiconductor. The asymmetric potential leads the electron to feel an effective electric field, which in the rest frame of the electron is equivalent to an effective magnetic field, which causes an energy difference between different spin species at a given k-vector. The origins of the asymmetric potential seen by the electron is manifested in two distinct ways. The first is called structural inversion asymmetry and is caused by an asymmetry in the confining potential of the electron (for example the triangle well that confines the 2DEG). The second is called bulk inversion asymmetry and comes from the lack of crystal inversion symmetry in III-V and II-VI semiconductors. These two terms lead to the Rashba and Dresselhaus terms, respectively.

We can write down the Hamiltonian for an electron in the system, including terms for the Rashba and Dresselhaus SOI:

$$\mathbf{H} = \frac{p_x^2 + p_y^2}{2m^*} + \frac{\alpha}{\hbar}(\sigma_x p_y - \sigma_y p_x) + \frac{\beta}{\hbar}(\sigma_x p_x - \sigma_y p_y) + \frac{\gamma}{\hbar^3}\left(\frac{d}{\pi}\right)^2 p_x p_y (p_y \sigma_x - p_x \sigma_y) \quad (1.99)$$

where σ_x and σ_y are the Pauli operators on the spin of the electron. The first term in this equation is the free-electron Hamiltonian and gives the motion of the electron through the semiconductor as we've seen in Equation 1.23. The second term is the Rashba SOI term, characterized by a strength α and linear in momentum, creating an effective magnetic field perpendicular to the momentum of the electron. The third and fourth terms are the Dresselhaus terms, with strength characterized by β for the term linear in momentum and γ for the term cubic in momentum. The cubic term is generally small relative to the two linear terms in both InAs and GaAs quantum wells and is normally ignored. For the linear Dresselhaus case, the effective magnetic field twists as the momentum of the electron changes [112]. The effects of these terms are to shift the energies of the two spin species at each point of the dispersion relation, a situation illustrated schematically in Fig. 1.20 (a) and Fig. 1.20 (b). As the Rashba term is set by the shape of the confining potential of the electrons in the

2DEG, it is also strongly tunable by the gate voltage, which can induce greater asymmetry in the confining potential. We should also note that although we call the effect of SOI an effective magnetic field, it is not a true magnetic field as it does NOT break time-reversal symmetry or introduce an asymmetry in the population of different spin species. This can be seen in Fig. 1.20 (a) and Fig. 1.20 (b), as states at each energy come in the form of Kramers pairs, such that:

$$E_{\uparrow}(\vec{k}) = E_{\downarrow}(-\vec{k}) \tag{1.100}$$

As the origins of this effect lie in the potentials formed by the constituent atoms of the semiconductors, we find that heavy-element semiconductors will have a stronger SOI. For applications that require a strong spin-orbit interaction, the use of heavy-element III-V or II-VI semiconductors, such as InAs, InSb or CdTe is common.

Collectively, these effects allow us to engineer the Hamiltonians of our systems to generate topological phases of matter as we shall see in our discussion below, where we use these effects to form anomalous quantum Hall states and Majorana zero modes. However, before we move onto those topics, we can close out our discussion of SOI with a striking modification that SOI causes to weak localization as described in Sec. 1.3.1. The fact that the rotation of spins occurs in opposite directions for opposite momenta leads to destructive interference around self-intersecting paths. This leads to an increase in conductivity, or **weak anti-localization**, in materials with strong SOI [102]. However, as the electron scatters around a closed loop, the coupling of momentum and spin leads to the randomization of the spin over several scattering events. In a semiconductor, this is described by the Dyakonov-Perel spin relaxation mechanism [113]. We can, therefore, introduce a new length scale, l_{so}, the length over which a spin relaxes in a material with SOI. This parameter is inversely proportional to the strength of the SOI, with a larger strength causing faster spin relaxation. As the destructive interference relies on the differing energies between the two distinct spin species, the length scale over which spin relaxes in the semiconductor sets a bound on the size of the loops where weak anti-localization can occur. As such, we are also able to measure this effect via low-field Hall measurements in the same way we measure weak-localization, as seen in Fig. 1.20 (c). Here the competition between weak-antilocalization (peak) and weak-localization (dip) is visible as the field is swept on a sample of InAs with strong SOI. In this regime we have $l_e < l_\phi < l_{\text{so}}$ hence all three effects are visible. As the strength of the SOI interaction is increased by increasing gate voltage, the spin-orbit length becomes comparable to the elastic scattering length $l_e \approx l_{\text{so}} < l_\phi$, thereby masking the effect of weak-localization, as seen in Fig. 1.20 (d). For materials with only Rashba SOI, the strength of the SOI may be extracted via fits given in [102]. For materials

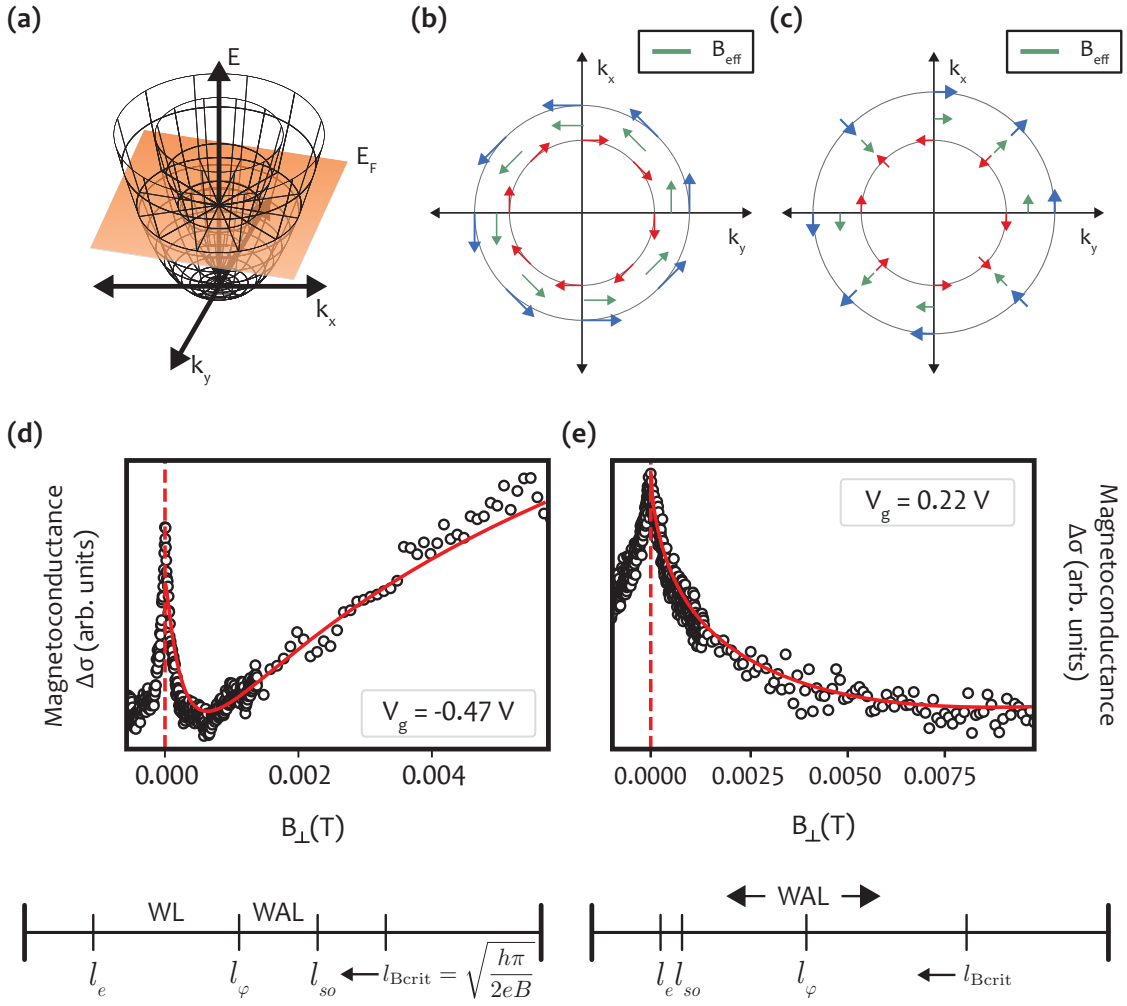

Figure 1.20: (a) The dispersion relation for a 2DEG under the influence of either Rashba or Dresselhaus SOI. Two offset parabolic dispersions are visible, a low energy and high energy spin branch. The Fermi energy E_F is shown in orange cutting through the parabolas. (b) The dispersion relation at the Fermi surface under the influence of only the Rashba spin-orbit interaction. The effective magnetic field is shown in green. (c) The dispersion relation at the Fermi surface under the influence of only the Dresselhaus spin-orbit interaction. The effective magnetic field is shown in green. (d) Weak anti-localization and weak localization in an InAs Gall bar. In this case, $l_e < l_\phi < l_{so}$. A conductance peak is seen at zero field, which is rapidly suppressed by an applied perpendicular field. At intermediate fields, weak localization begins to dominate, leading to a dip and gradual rise in conductance. (e) Weak anti-localization in the same sample, for the case that $l_e \approx l_{so} < l_\phi$. The strength of the Rashba spin-orbit interaction is increased by the application of a higher gate voltage, leading to a tilted confining potential and a reduced spin relaxation length l_{so}.

where both Rashba and SOI terms exist, a comprehensive treatment of the correction to conductivity is given in [114].

1.3.5 Quantum Anomalous Hall Effect

One fundamental question we might ask is whether we can form edge states with quantized conductance that are protected from scattering without an external magnetic field. It was several years before the question was answered in the affirmative by Thouless [115] and later Haldane [116], their insight being the relationship between the quantum Hall and related effects, and topology. For this insight, they were, along with Kosterlitz, awarded the Nobel Prize in 2016 [117]. Briefly, we can try and get an intuitive understanding of topology by considering the genus of an object. This is a global property of a surface that is related to the number of holes in it. A ball, for example, has a genus of zero, and by continuous deformation, we can turn it into other objects with the same genus, for example, a cube, a sheet of paper or even a pan have a genus of zero. A doughnut, on the other hand, has a genus of one; it has a single hole. We can stretch and shape it into objects such as a mug, where the hole is its handle, but it can never become a ball. This genus is captured by the Gauss-Bonnet theorem which states that the integral over the surface S of a shape, with local curvature K will yield the genus g of the object:

$$\frac{1}{2\pi}\int_S K\mathrm{d}A = 2(1-g) \tag{1.101}$$

We use a generalization of this theorem, called the Chern-Simons theorem, which allows us to map this theorem onto a band structure. We can define an equivalent to "curvature" along the surface of bands in a solid, termed the Berry's phase. This is the phase that a particle traveling around a path on the surface of a band acquires. The integral of the Berry's phase over momentum space leads to an integral quantity known as the Chern number n, which is an integer and characterizes the topology of the material [118]. In the integer quantum Hall effect, the number n is the same as the filling factor ν, and gives us a topological explanation for the emergence of quantized edge states. As we transition from within the material, with Chern number n, to free space, with Chern number 0, there must be a twisting of the band structure near the edge that leads to the emergence of conductive edges. However, for the quantum Hall state, a large magnetic field is required to define the Berry's phase and hence the Chern number of the material.

In materials with a strong spin-orbit coupling, it is possible to find configurations with a non-zero Chern number, a topologically non-trivial band structure. At the boundaries of

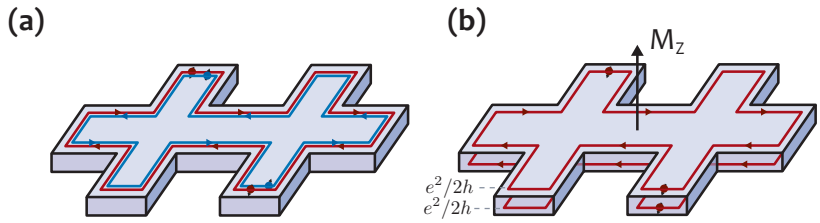

Figure 1.21: (a) The spin quantum Hall effect. Two counter-propagating spin currents flow around the edge of the sample. Spin scattering can occur between the two edges such that robust protection is not generally seen. (b) The quantum anomalous Hall effect.With the addition of a ferromagnetic dopant, and when the sample is magnetized, only a single spin polarization remains, leading to a spin-polarized chiral edge state, protected from backscattering.

such a material, a conductive state must appear [119, 120], and indeed for heterostructures of HgCdTe the **spin quantum Hall effect** has been observed [121], where two counter-propagating, spin-polarized, 1D channels lead to quantized conductance. This is shown in Fig. 1.21 (a). Unfortunately, this effect is sensitive to spin-scattering and thus is not a robust, dissipation free, effect. The addition of a ferromagnetic dopant, such as chromium or vanadium lifts the time reversal symmetry and generates leads to the formation of a spin-polarized chiral edge state, once the material has been taken past the coercive field of the Cr or V dopants. This is termed the **quantum anomalous Hall effect**. The total conductance is given by the sum of the top and bottom edge states, each contributing $e^2/2h$ of conductance, for a total Hall conductance of $\sigma = e^2/h$, as shown in Fig. 1.21 (b). We will use a sample that shows the quantum anomalous Hall effect in Sec. 3.2 to demonstrate a circulator that can operate without an external magnetic field.

1.3.6 Forming Majoranas

In section 1.2.4 we went over a brief introduction to the physics that underpins quantum computation with Majorana zero modes and left ourselves with the problem of finding a materials system that fits the model Hamiltonian given in equation 1.65. I will stress again that while this Hamiltonian represents one proposed method of forming an emergent Majorana quasiparticle, there are many techniques described in the literature involving a variety of materials systems, including in several excellent reviews [122, 123, 124, 125, 126, 127]. The technique of using a proximitized superconductor/semiconductor hybrid with strong SOI was reviewed recently in [21] and goes into far greater detail than I attempt to here. To briefly recap, our Hamiltonian required a 1-dimensional chain of spinless fermions and a superconducting pairing gap. Section 1.2.1 covered the method by which we can

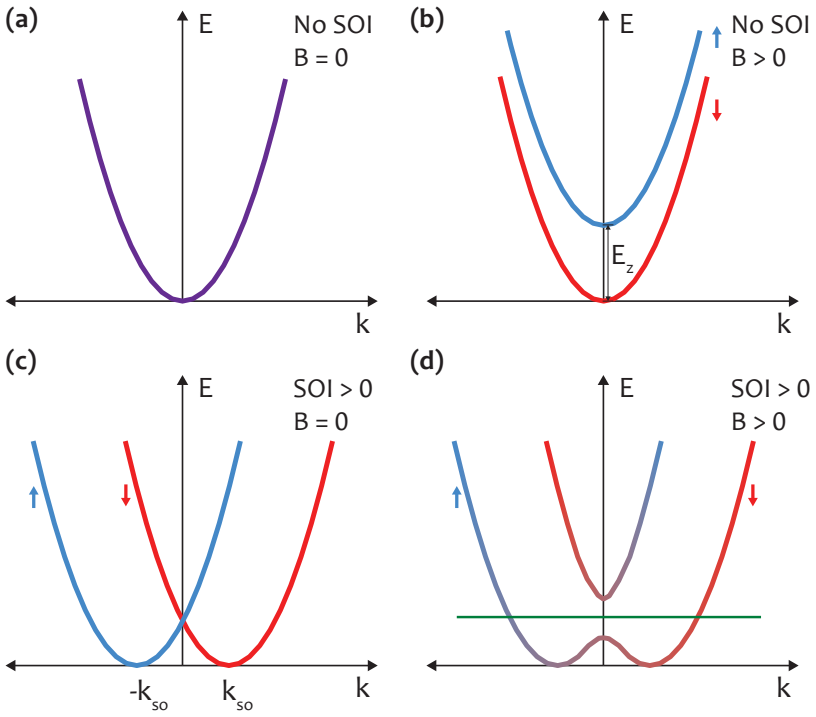

Figure 1.22: (a) The dispersion relation for a 1-dimensional chain of electrons (nanowire), assuming the nearly-free electron model. We obtain a parabolic band with two degenerate spin states. (b) The dispersion relation under the influence of an external magnetic field. A Zeeman splitting E_Z occurs between $\uparrow$ and $\downarrow$ spins. (c) The dispersion relation in a material with either a Rashba or Dresselhaus spin-orbit interaction. The two spin species are shifted relative to each other by an amount $\pm k_{\mathrm{SO}}$. Note that unlike a Zeeman field, this does not lead to any spin polarization in the material. (d) The dispersion relation in a material with spin-orbit interaction and an external magnetic field. The magnetic field creates a coupling between the split bands and opens a gap in the dispersion relation. If the chemical potential is tuned in the gap (green line) only a single band of the dispersion relation is accessible, equivalent to a system of spinless fermions.

form systems with reduced dimensions in semiconductors; the remaining challenges are to create spinless fermions and induce a superconducting pairing gap in a semiconductor. The combination of superconductivity and spinless fermions is termed superconducting p-wave pairing [95]. We can tackle each challenge one at a time.

First, let's attempt to form a system of spinless fermions. We can accomplish this using the spin-orbit interaction as described in Sec. 1.3.4. In a 1D chain, assuming a single dominant source of spin-orbit interaction (either Rashba or Dresselhaus), the coupling between momentum and spin induces a shift in the momentum parabolas compared to the case of no spin-orbit coupling. This is depicted in Fig. 1.22 (a) in the case of a bare dispersion relation, and Fig. 1.22 (b) in the case of a shifted dispersion under the influence of Rashba or Dresselhaus SOI. In this case, there is no coupling between the high and low energy branches of the dispersion relation. The application of a magnetic field parallel to the 1D channel opens a Zeeman energy gap between the two spin species with magnitude $E_z = g^* \mu_B B_\parallel$, as shown in Fig. 1.22 (c), for a case with no SOI. In the case that the SOI is present in the sample alongside an external magnetic field, there is a coupling between the two branches of the dispersion relation, which opens a gap in the spectrum, seen in Fig. 1.22 (d). If the chemical potential is tuned inside the gap (green line), there is only a single band crossing the Fermi energy, effectively describing a system with a spinless degree of freedom. The strength of the SOI in the material sets the field required to open a pairing gap in the material, hence the requirement for a material with a large SOI, without which the strength of the required magnetic field would be prohibitive, particularly when considering our second requirement: superconducting pairing.

The pairing term can be accomplished using the proximity effect of a superconductor, which is the hybridization of superconducting and metallic states between a superconducting metal and a semiconductor when a transparent interface joins the two. The hybridization is caused by the differing band structures between the two materials; there must be a gradual change between the gapless band structure of the semiconductor and the gapped structure of the superconductor. While Cooper pairs may penetrate the semiconductor for many microns, with a distance set by the elastic scattering length which destroys the coherence of pairs, for a hard-gapped band structure at the 2DEG it is necessary for the heterojunction to be grown close to the 2DEG, generally within the superconducting coherence length. Without a hard gap, quasiparticles are able to destroy the information stored in our Majorana fermions. Even with such a close spacing, the material must have also have high mobility, as disorder scattering suppresses p-wave superconductivity and destroys the topological phase [128]. To ensure there are few subgap states, the most recent experiments have

also required in-situ epitaxially grown aluminium interfaces, as any impurities at the superconductor semiconductor interface have been found to contribute to significant sub-gap conductance [129].

The choice of materials used for the formation of a Majorana zero mode in a superconductor/semiconductor hybrid system must, therefore, meet each of these, sometimes conflicting, requirements. A large SOI and Landé g-factor calls for a heavy element III-V or II-VI semiconductor; however, the majority of high-quality growth has occurred in GaAs. InAs and InSb have recently shown high mobilities for buried 2DEGs [130, 131], however the requirement for a hard-gap necessitates the growth of a 2DEG close to the surface of the semiconductor where it is difficult to shield from the effects of scattering off surface impurities, an issue we tackle in Sec. 5.1. Nonetheless, recent experiments have demonstrated ever higher quality materials and more definitive evidence of zero bias peaks, close to the expected value of $2e^2/h$[50, 132], leading to a great deal of optimism for future applications using such devices.

Chapter 2

Architecture of a Quantum Computer

Although the challenges of building a fault-tolerant qubit have by no means been overcome, the field is rapidly reaching the point where it is possible to start running algorithms on quantum computers. While algorithms such as Shor's algorithm for prime factorization requires a large number of qubits with arbitrarily long lifetimes [133, 89], other algorithms may be able to achieve a quantum speedup with a limited number of noisy qubits. Algorithms and systems operating in this regime are said to be in the Noisy Intermediate-Scale Quantum (NISQ) regime [134], a term coined by John Preskill to distinguish between a full-scale quantum computer with a large number of error corrected qubits, and a machine containing as few as 10s of noisy, imperfect qubits that we may realize in the coming decade. In the near term, the race is on to achieve **quantum supremacy**, a calculation on a quantum computer whose simulation on a classical computer is intractable. The expectation is that this milestone will be beaten in the coming years, with a system of approximately 50 noisy qubits [135]. Based on the current state of the field this will likely occur using superconducting transmon-like qubits solving a model problem such as Boson sampling [136]. While such a result would certainly be groundbreaking, the more interesting result would be a demonstration of **quantum advantage**, an algorithm whose simulation on a classical computer is intractable, but one which also solves a useful problem. While Boson sampling certainly seems to be a classically hard problem, the solution it provides does not seem to be one that has many practical implications. In the near term, our best bet for achieving a useful result seems to be using the Variational Quantum Eigensolver algorithm [30], which, as we alluded to in the introduction of Chapter 1, would allow us to model molecules that we could not on a classical computer, with a small number (100s) of imperfect qubits [137]. To date, several experimental realizations of this algorithm have been published [138, 139, 140], although none have yet simulated a molecule that is classically intractable [141].

2.1 Designing an Architecture

Given the rapid progression of the field, the questions surrounding architecting a quantum computer have been gaining increasing attention, particularly as the number of qubits grows beyond the limits that we might control with an ad-hoc architecture that a single graduate student might construct. The challenge for experimentalists continues to come down to building scalable building blocks, which balance the need for experimental flexibility surrounding qubits whose designs and control requirements remain in flux, but whose footprint does not explode for larger numbers of physical qubits. Thankfully, there is substantial overlap in the requirements for control and readout between qubit implementations (at least within the realm of superconductor and semiconductor based qubits), which allows us to design architectures for hypothetical quantum machines. Let's therefore enumerate a few of the key requirements for a control and readout architecture for solid-state qubits:

- **Cryogenic operation**: Solid-state qubits must be operated in cryogenic environments, stemming from the requirement that the thermal energy should be well below the level spacing of energy levels in the qubit, as well as the need for superconducting elements in some designs. Any control and readout architecture must, therefore, be low power, and avoid carrying thermal energy or noise down to the qubit device.

- **Control fidelity**: In order to reach the fault-tolerance threshold, fidelities of individual qubits must exceed 99%, and should ideally be well above the $(1 - 10^{-5})$ level to avoid prohibitive error correction requirements [89]. Depending on the rotation rate and decoherence rates of individual qubits, control lines must have bandwidths of several 10's of GHz, as well as being high density while maintaining low crosstalk.

- **Readout fidelity**: Readout of qubits brings unique challenges, requiring low probe powers in order to avoid disturbing the state while it is being measured, and limited measurement time due to decoherence. In addition, QEC in general requires the continued measurement of ancilla qubits while nearby qubits are operational, leading to stringent crosstalk requirements. In order to obtain sufficient signal-to-noise ratio, cryogenic amplification is generally required, which in turn limits scalable designs to a small number of parallel readout lines. As such, some form of multiplexing, either frequency-domain or time-domain, is necessary for readout.

- **Space**: This requirement is particularly difficult to accomplish as it occurs over three orders of magnitude over the scale of the chip, the cryostat and at room temperature. Each of these are discussed in detail below, but we state the problem briefly here.

> On a chip scale, dense control lines must be fit into an area set by the distance over which we can achieve coupling between qubits, setting micron-scale limits on on-chip structures. On a cryostat level, the need to operate at mK places centimeter-scale limits on cryogenic components. Finally at room temperature, phase matching of control pulses and the need for active feedback places limits on the size of the instrumentation used to control individual qubits.

In general, qubit architectures for solid-state qubits can be classified into two categories (control and readout) at three different temperature stages (room temperature (RT), four Kelvin (4 K) and milli-Kelvin (mK)), as shown in Fig. 2.1. An architecture is characterized by the number of rf and dc lines that run between temperature stages L, and a power consumption at each stage P, divided between the control and readout block. Two architectures are presented in this thesis, which trade off complexity and reduced experimental flexibility for reduced wiring and power consumption at different stages of the cryostat. The CryoCMOS architecture, presented in Sec. 2.3 utilizes a CMOS based switching matrix at millikelvin temperatures that is bonded directly to the qubit chip in order to minimize the power dissipated in parasitic capacitance. The Prime-Lines architecture, presented in Sec. 2.2 utilizes a cryogenic switching matrix near the qubit to minimize the number of high-frequency coaxial lines required to control qubits. Order of magnitude estimates for the number of control lines and the power consumption for each architecture is given in Table 2.1, characterized by a number of qubits N, and in the case of the prime-lines architecture, the number of control pulse-shapes M, where in general $M \ll N$. The sources of power dissipated for each of these architectures will be elucidated over the course of the remainder of the section. I will however draw the readers attention to the fact that even for passive, high-bandwidth wiring, there is a power cost associated with bringing these lines down [142], a topic I will explore in detail in Sec. 2.1.1.

In the remainder of this section, I will quickly review the challenges for control and readout for a large-scale quantum computer, which very much remains an open question in the field. As we move through the following sections, the sources of many of the numbers in Table 2.1 should become clear as well as our vision for solving some of these problems. In general, I will progress from the qubit plane up to room temperature control, however this structure is by no means strict.

2.1.1 Control Plane

A popular refrain for proponents of semiconductor-based qubits is to point to the maturity and flexibility of modern semiconductor processing as an argument for the scalability of

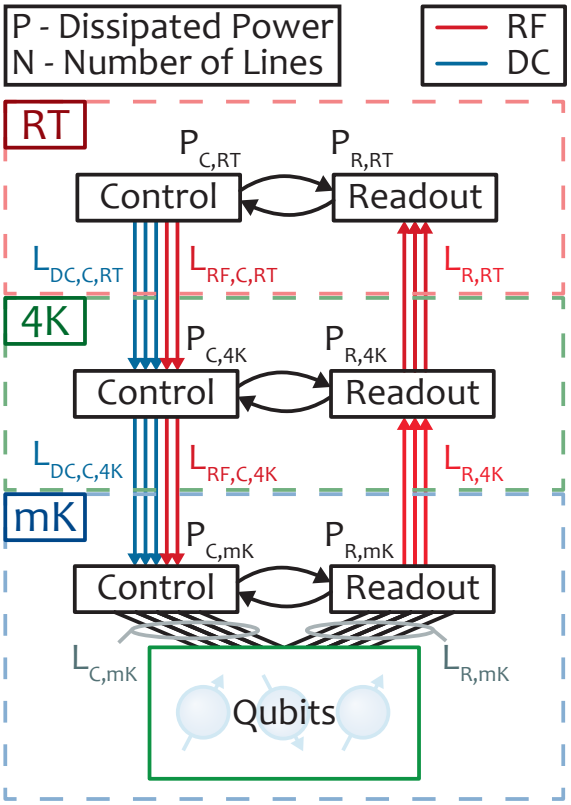

Figure 2.1: A generalized qubit architecture, broken into control and readout stages at each temperature stage of a cryostat. The architecture is characterized by number of lines which run between each stage, for example $L_{RF,C,RT}$ for the number of coaxial control lines running from room temperature to the 4 K stage of the cryostat, which will vary depending on the choice of a given architecture. In addition, each stage will dissipate a certain amount of power, for example $P_{R,4K}$ being the power dissipated at 4 K by the readout stage, caused either by active logic, such as an FPGA, amplifiers or off-the-shelf instrumentation, or by passive dissipation, for example due to attenuators.

			CryoCMOS Architecture (Section 2.3)	Prime-Lines Architecture (Section 2.2)	Frequency Multiplexed [143]	Naïve
Room Temp	Power	$P_{C,RT}$	100 W	$M \times 1000$ W	$N \times 1000$ W	$N \times 1000$ W
		$P_{R,RT}$	100 W	$N \times 100$ W	$N \times 100$ W	$N \times 100$ W
	Lines	$L_{DC,C,RT}$	3	N	N	N
		$L_{RF,C,RT}$	3	M	N	N
		$L_{RF,R,RT}$	2	2	2	N
4 K	Power	$P_{C,4K}$	1 W	1 W $+ M \times 100\,\mu$W	$N \times 100\,\mu$W	$N \times 100\,\mu$W
		$P_{R,4K}$	50 mW	50 mW	50 mW	$N \times 50$ mW
	Lines	$N_{DC,C,4K}$	3	N	N	N
		$L_{RF,C,4K}$	3	M	N	N
		$L_{RF,R,4K}$	2	2	2	N
mK	Power	$P_{C,mK}$	$N \times 6$ pW $+ 34\,\mu$W	$(N + M) \times 1\,\mu$W	$N \times 1\,\mu$W	$N \times 1\,\mu$W
		$P_{R,mK}$	40 nW	40 nW	40 nW	$N \times 40$ nW
	Lines	$L_{C,mK}$	N	N	N	N
		$L_{R,mK}$	N	N	N	N

Table 2.1: Order of magnitude power P and wiring L requirements for the CryoCMOS architecture, the Prime-Lines architecture, frequency multiplexed readout and a Naïve architecture. The number of lines is split between high-bandwidth coaxial lines (rf) and low-bandwidth (dc) lines. In each case, we trade off the complexity in the setup to reduce the wiring required down the fridge. The power consumption and number of lines is given in terms of the number of qubits N, and in the case of the Prime-Lines architecture, the number of pulse shapes M. Power consumption for control lines is calculated assuming a $1\,\mathrm{mV}$ pulse at the qubit through a $20\,\mathrm{dB}$ attenuator at the 4 K and mK stage. For the CryoCMOS architecture, a pulse frequency of $10\,\mathrm{MHz}$ was used. Readout power is calculated assuming a Caltech-style HEMP amplifier at the 4K stage, and utilizing rf-reflectometry techniques for readout (see Sec. 2.1.2). With a $-90\,\mathrm{dB}$ readout power, dissipation is dominated by passive thermal conduction up to ~ 1000 simultaneous channels.

qubits based on similar processes. While it is undoubtedly true that the miniaturization of transistors has translated into an ability to fabricate finer devices, the scalability of quantum computers based on such an argument is by no means clear. The problem, and indeed the main differentiator between a qubit and a transistor, it that while a transistor has the ability to drive other transistors, a qubit has no similar ability. All control of a qubit, to initialize and to drive single and two qubit rotations, must come from outside. This unfortunate fact is captured in Rent's rule, which relates the number of external terminals (or pins) T of an IC, to the number of internal components (or transistors) g:

$$T = tg^p \tag{2.1}$$

where t and p are constants of the system. For an integrated circuit, the value of p generally ranges from 0.5 to 0.8 [14], however for a quantum circuit, it is reasonably simple to see that this exponent must be 1! Each qubit must be driven by some number t gates, with no qubit able to drive another qubit without some external control.

The above statement captures the primary difficulty that we will run into when designing qubit chips. While classical ICs can rely on some fan-out to minimize the number of inputs required, the design of a quantum chip must be able to supply high density wiring with high bandwidth and low cross-talk. In addition, classical CMOS processes usually have only a few layers of high-density interconnects, used only for short-range connections [144], while qubit architectures generally require several layers of high-density interconnects over the length of an entire chip [17]. The question then is what sets the maximum pitch of a qubit on a chip, as this gives us the density of control lines that must be achieved. Then, given that pitch, how many lines could we bring in to such a device, given a 1D or a 2D grid of qubits?

The answer to the first question, the pitch of qubit devices, will be set by the length scale over which coupling can be achieved. For spin qubit devices based only on direct exchange for example, the pitch of qubits will be roughly the size of the qubit itself, as coupling only occurs when electrons can directly tunnel between neighbouring devices [145]. Work presented in this thesis uses elongated many-electron quantum dots to increase this to the micron-scale in Section 4.1, an approach which will likely be applicable Majorana devices that use quantum dots as couplers [146]. Finally, long distance coupling of spins via superconducting resonators [147] has recently been demonstrated [148], enabling coupling over mm length scales.

The next question is how many lines we can bring to a device. In a 1D array of qubits, that is for a single line of qubits, the answer is limited only by the physical size of the chip, and the size of pads (bond pads or bump pads) that we are able to make contact to. For example, a singlet-triplet qubit which requires 10 control lines, and pads of pitch 100×100μm will

require a chip with a 0.01 mm^2 area, assuming of course that we are able to make contact in 3D (i.e. overlapping bonds). In the case that we are only able to make contact in 2D, a chip of size 400×400μm at a minimum is required to break pads out to the edge of a device.

The situation is more difficult to evaluate in a 2D array. Firstly, a 2D array is not possible on a single planar grid, as control lines for inner qubits must be broken out. Therefore a sufficient distance between qubits must be possible to allow control lines to be brought in from upper layers. To allow fan-out of a dense grid leads to a problem very similar to that of routing a ball-grid array (BGA) package. There will be a relationship between number of layers, track pitch and via (inter-layer contact) pitch, which will set a hard density limit on qubit devices. Therefore increasing the pitch of qubit devices via long distance coupling may be necessary when moving to 2D grids. Furthermore, the design of qubit layouts allowing realistic wiring schemes will continue to be crucial moving forwards [149]. Finally, I point to the potential for multiplexing the control of many qubits onto single control lines, which may allow the definition of a quantum analog to Rent's rule [15] (Equation 2.1). Whether such an architecture is truly scalable remains an open question at this time.

On a single qubit chip it seems difficult to get around the problem of breaking all control lines out in order to allow qubit control. Alluding back to our generalized qubit architecture in Fig. 2.1, it should in general be possible to reduce the number of lines running between the 4 K stage and the control plane at mK. To understand the techniques for doing so, it is useful to separate control pulses into three general forms: microwave excitations, fast pulses and static confinement. The first two of these require high bandwidth rf wiring, while the latter requires only low bandwidth dc wiring. By the use of CryoCMOS switches, as detailed in Section 2.3, it is possible to multiplex a single dc control line to several gates, effectively locking a voltage onto those gates. Such switches do not dissipate power except when toggled, leading to extremely low power consumption. Similarly, fast pulses may similarly be generated, again, as detailed in Section 2.3, minimizing the parasitic capacitance and hence power dissipation, given by $P_{\text{diss}} = CV^2 f$, caused by the length of control lines. Note that in the limit where pulses are generated next to the qubit device we no longer use require the use of a matched transmission line, allowing calculation of dissipation using this formula. This in turn leads to the low power consumption of the CryoCMOS architecture in Table 2.1. The availability of CMOS at low temperature also gives us a possible solution to the high interconnect density previously discussed, as the pitch of bump-bonding technologies approaches a few μm (with the smallest I am aware of in use at the time of submission being 20 μm [150]). Similarly, the design of low-dissipation and highly integrated rf-switches as demonstrated in Section 2.2 allows the routing of a few microwave or

pulse lines, which provides a path to further reduction of the footprint of wiring between stages of the cryostat, as well as a reduction of the signal generation equipment required.

The thermal cost of high bandwidth control must also be considered. As qubits must be operated at low temperature and are highly susceptible to thermal noise, we must design wiring to attenuate the thermal photon population at the qubit plane. Primarily this is achieved through the use of dissipative attenuation at each stage, where the population of thermal photons at each stage can be calculated as [142]:

$$n_i(\omega) = \frac{n_{i-1}(\omega)}{A_i} + \frac{A_i - 1}{A_i} \frac{1}{\exp(\hbar\omega/k_B T_i) - 1} \tag{2.2}$$

where T_i is the temperature and A_i is the attenuation on the i-th stage of the cryostat. The first term of this equation gives the attenuation of thermal photons from the previous stage (n_{i-1}), while the second term gives the thermal photon flux spectral density generated by the attenuator itself. As such, to reduce thermal photons, attenuation must be used at the lowest temperature stages of the order of 20 dB, to achieve $n_{\mathrm{mK}}(6\,\mathrm{GHz}) \sim 0.002$. Therefore, even without considering the heat load due to the thermal conductivity of coaxial cables, a significant portion of our control pulse must be dissipated during the filtering of thermal photons from coaxial cables. In Table 2.1, the power dissipated at each stage of the cryostat is estimated, assuming each control line contains a 20 dB attenuator at both the 4 K and the mK stage, and that each qubit requires on average a 1 mV pulse for control. Here we've also assumed a repetition rate sufficiently fast that the pulses may be approximated by a continuous wave, a condition that is easily met for a repetition rate on the order of 200 MHz.

Finally we move up to room temperature, where two primary concerns remain: power consumption and latency (or phase matching), both of which place limits on the footprint of control electronics at room temperature. In particular, as the rotation rate of qubits is increased, finer tolerances for the phase match of control pulses is required. When utilizing long control lines, such a phase match is difficult to achieve. Furthermore, as the number of qubits is increased, the footprint of off-the-shelf electronics, which is in general not designed for simultaneous control of a large number of lines, becomes onerous. In Section. 2.2 we address some of these concerns using cryogenic hardware for control, which may allow the use of high density cryogenic interconnects [151], although the overall advantages of 4K control require further investigation.

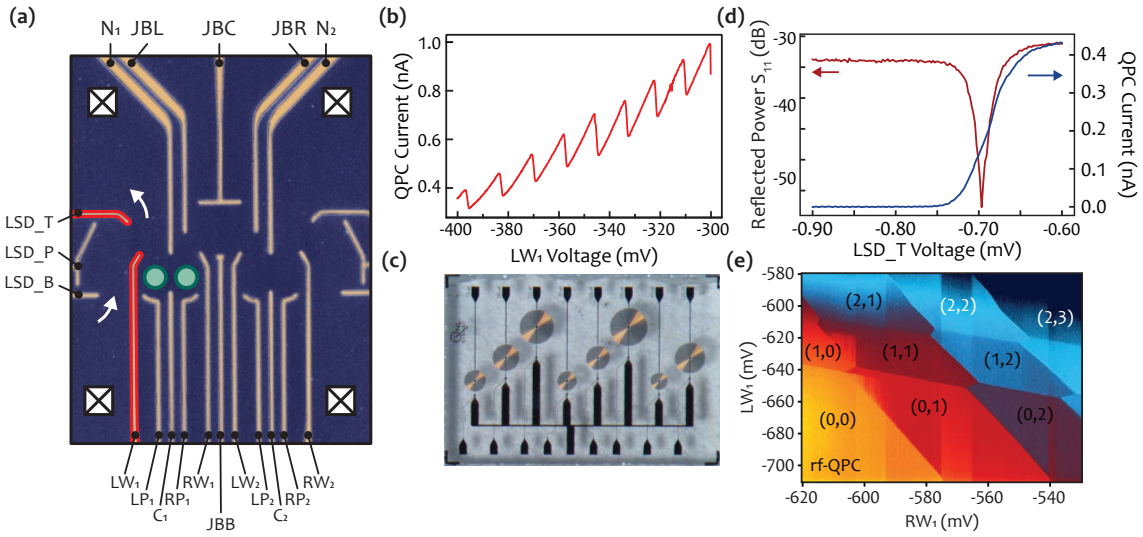

Figure 2.2: (a) False color SEM of a five-dot device, similar to the one presented in Sec. 4.1. Surface gates are labeled, and current is shown running through the charge sensor on the left of the device. (b) Charge sensing signal when the left sensor is tuned as a QPC (1d channel). Each step corresponds to a change in the charge occupancy of the quantum dot by 1. (c) Multiplexed readout chip with several resonators, used for performing rf readout. (d) Response of the charge sensor in current (right axis) and in reflected rf power (left axis) as the QPC is brought through pinch-off. (e) Sample of a charge stability diagram taken using rf charge sensing. Each distinctly colored region represents a unique charge configuration.

2.1.2 Readout

In addition to control, the high-fidelity readout of a fragile quantum state is a crucial element of a quantum computer, without which improvements we make to the control of our qubit are negated. This effect is particularly apparent when considering error correction schemes, which feed the results of measurements back into the qubits in order to correct errors, which is a futile endeavor without accurate readout results. Combining fast, high-fidelity readout with scalable design complicates the requirements for a quantum computer even further, particularly when we consider the most common designs for readout circuits. As before, I will begin the discussion of readout at the qubit chip level, and discuss scalability as we go.

For the majority of semiconductor qubit designs, readout is performed via sensing of the charge state of a quantum dot, or quantum dot like structure. For spin qubits, this is performed by spin-to-charge conversion, where the charge state of a quantum dot will depend on the spin states of its electrons [152, 153], and for Majorana fermions this occurs via the fusion of edge modes (see Sec. 5.2). Typically readout is performed via a proximal charge sensor, which may be formed by a quantum point contact (1D channel), or a sensing dot. A gate pattern with a sensing dot on the left and right is shown in Fig. 2.2 (a). The conductance

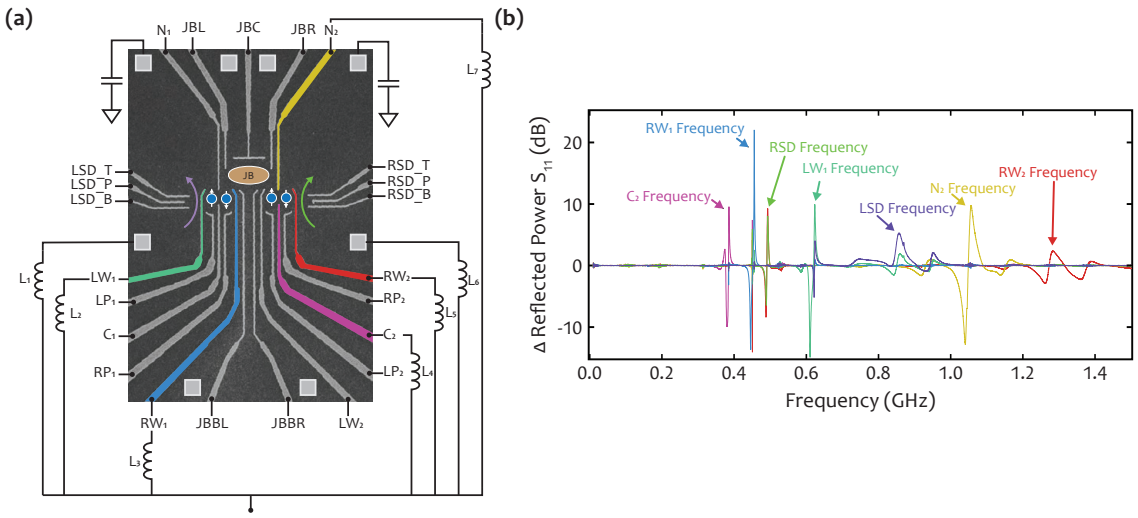

Figure 2.3: (a) False color SEM of a Five Dot device, identical to the one used in Sec. 4.1. A number of resonators are bonded to several gates including both charge sensors and dispersive gate sensors. (b) The frequency response of the multiplex chip when the voltage on each gate is changed. Distinct frequencies are observed for each gate on the sample.

of the QPC or sensing dot will depend sensitively on the charge state of the proximal double quantum dot. This is shown in Fig. 2.2 (b), where steps in the conductance of the QPC correspond to charges moving on and off the nearby quantum dot. The measurement of this conductance can either be done via a dc lockin measurement or via rf-reflectometry [154]. The dc measurement is limited by the RC-time constant of the wiring in the fridge, which due to the parasitic capacitance, filtering and high resistance of the sensor will in general limit bandwidth to a few kilohertz, far greater than the T1 times for spin qubits. rf measurement is performed by embedding the QPC in a resonator, where the quality factor of the resonator is set by the resistance of the charge sensor. The derivation of the matching condition is not given here, but I point the interested reader towards [155], where a complete derivation is given. Of course this immediately points towards the possibility of frequency multiplexing [143], allowing the readout of multiple resonators simultaneously, although the requirement for a proximal charge sensor means such a sensor design is unsuitable for 2-D architectures. For larger arrays of charge sensors, the presence of noise generated by the charge sensor can additionally become significant [156], creating an additional source of dephasing for proximal qubits which we may not wish to disturb.

An alternative to using a proximal charge sensor is to use the confining gates themselves as sensors [157], wherein the quantum capacitance of the system is measured. The

polarizability of a quantum dot is given by:

$$C_Q = -\frac{\partial^2 E}{\partial {V_g}^2} = -(\alpha\varepsilon)^2 \frac{\partial^2 E}{\partial \varepsilon^2} \tag{2.3}$$

where α is the lever arm and ε is the tilt, as shown in Fig. 1.10 and defined in Sec. 1.2.2. As we can see from the above equation the quantum capacitance is proportional to the band curvature, which allows us not only to detect charge transitions but also the spin state (since the triplet state has no curvature at 0 tilt), and hybridization. The latter effect may be used to detect the parity state of a Majorana zero mode coupled to a proximal quantum dot [146]. As with readout via a charge sensor, by embedding a gate in a resonant circuit, we are able to quickly sense changes in capacitance, with a sensitivity that is sufficient to perform single shot readout of spin states [158, 159]. A frequency multiplexed device with 7 resonators is shown in Fig. 2.3, combining both dispersive and charge-sensing modes of readout.

The potential for frequency multiplexing also allows us to imagine integrated methods of readout. While the idea of multi-channel qubit readout is certainly not new, the design of equipment that are able to handle large numbers of channels simultaneously is as yet an open problem. In particular, once multiple channels are multiplexed onto a single rf pair, the total power that must be transmitted for n channels is:

$$P_{\sum}(n) = P_0 + 10\log_{10}(n) \tag{2.4}$$

At the device level, this increases the isolation necessary between channels, as it is desirable to be able to select qubits to measure selectively. In addition, crosstalk may drive rotations of neighbouring qubits, reducing the fidelity of control, which is particularly problematic for error correction schemes where proximal ancilla qubits must be constantly read and corrected.

At this point, it is also worth covering noise in the readout circuit, as noise in the system is the limiting factor in readout time. Unfortunately, as alluded to in earlier sections, the fragile nature of the quantum state requires us to use low probe powers in order to ensure our readout does not destroy the quantum state. In quantum dots, we can generally place limits on the power of our probe signal P_{probe} using similar thermal arguments to those used when discussing bias, that is the power of the signal should be much less than the relevant energy scales of the system: $P_{\text{probe}} \ll \Delta E$. In the case of circuit-QED, the requirements

are even more strict, where operation in the single photon limit is necessary:

$$P_{\text{probe}} \sim \frac{\hbar\omega^2}{2}\frac{Q_c}{Q_l^2} \tag{2.5}$$

where Q_c is the coupling-Q and Q_l is the loaded-Q of the resonator. Unfortunately any quantum system will, at the very minimum, generate thermal noise and vacuum fluctuations. The thermal noise power spectral density, that is the noise power per unit bandwidth, for a system is given by [160][1]:

$$S(\omega) = \frac{\hbar\omega}{2}\coth\left(\frac{\hbar\omega}{2k_BT}\right) \tag{2.6}$$

from which we can define an effective noise temperature of the system:

$$T_{\text{eff}} = \frac{S(\omega)}{k_B} \tag{2.7}$$

We can therefore define the maximum signal-to-noise ratio of a system, that is the signal-to-noise of an ideal receiver at the output of our qubit, for a measurement bandwidth of 1 Hz:

$$\text{SNR}_{\text{max}} = \frac{P_{\text{probe}}}{S(\omega)} \tag{2.8}$$

In order to read a small signal, since any physical readout hardware will have a limited dynamic range and will itself add noise, additional amplification is necessary. We must therefore account for the noise added by any given amplifier, with the total effective system temperature:

$$T_{\text{sys}} = T_0 + \frac{T_1}{G_1} + \frac{T_2}{G_1G_2} + \ldots\frac{T_n}{G_1G_2\ldots G_n} \tag{2.9}$$

where T_0 is the noise temperature at the output of the qubit, and will include T_{eff}, the thermal noise of the qubit and any noise present on the probe signal, and T_k, G_k are the noise temperature and gain of each stage of amplification or attenuation in the chain. For a HEMT amplifier commonly used in spin qubit experiments, a gain on the order of 30 dB is common, with a noise temperature of $\sim$ 3 K[2], such that the system noise temperature after the first stage of amplification is $T_{\text{sys}} \approx 3000$ K. As long as the noise temperature of

[1]Note that this form of noise power spectral density is given by a quantum theory of noise. In the limit of large temperature ($\hbar\omega \ll k_BT$), using the approximation $\coth(x) \approx 1/x$ for small x, we recover the classical formula for noise power spectral density: $S(\omega) = k_BT$.

[2]For example the CITLF3 amplifier from Cosmic Microtech: `https://www.cosmicmicrowavetechnology.com/citlf3`

subsequent amplifier has $T_n \ll 3000$ K, the first stage amplifier will set the effective system temperature. As this temperature is well in the classical limit, we can define the system signal-to-noise ratio, for a bandwidth of 1 Hz, as:

$$\mathrm{SNR}_{\mathrm{sys}} = \frac{P_{\mathrm{probe}}}{k_B T_{\mathrm{sys}}} \tag{2.10}$$

The choice of first stage amplifier is therefore critical in designing a readout chain. The use of frequency multiplexing reduces the scaling of power and high-bandwidth lines to 4 K, as shown in Table 2.1, however it creates additional constraints. Namely we must balance the 1 dB compression point and the noise temperature of the amplifier to minimize the effective system temperature while maximizing the allowed probe power and the number of simultaneous channels that may be read. In particular for quantum limited amplifiers such as Josephson parametric amplifiers and or traveling-wave parametric amplifiers [161] where the dynamic range is limited, designs which specifically take into account the bandwidth and power requirements for multi-channel readout are required. In addition to this, the isolation of the amplification chain from the qubits must be considered. An attenuator can be considered an element with gain $G_k < 1$, and a temperature set by the stage it is on, such that any attenuation between qubit and the first stage amplifier can lead to a large increase in the effective signal temperature. For this reason, on spin or Majorana based systems, there is generally no isolation up to the first stage amplifier, however for circuit-QED type experiments, or those that require the use of parametric amplifiers, isolators with minimal losses must be used, significantly increasing the footprint of the readout chain. For this reason, in chapter 3, the use of the quantum Hall effect to form miniaturized isolators is explored.

Finally, we briefly touch on the topic of readout hardware at room temperature. The use of multiple simultaneous frequencies for readout creates several challenges for a typical analog homodyne detection architecture, due to the higher-order non-linearity and the inherent unscalability of analog signal generators and low-bandwidth digitizers. A schematic of a typical analog readout chain is shown in Fig. 2.4 (a). Due to the non-linearities present in the analog mixer, signals must be band-pass filtered and boosted prior to mixing to achieve optimal signal-to-noise. For the homodyne setup shown, an analog phase shifter is required, and does not allow phase information to be extracted. A second analog signal source may be added prior to the mixer to allow for heterodyne (I/Q) demodulation, however this significantly increases the resource requirements of the circuit. Therefore even with frequency multiplexing near the device, the scalability of an analog readout setup is still linear in the

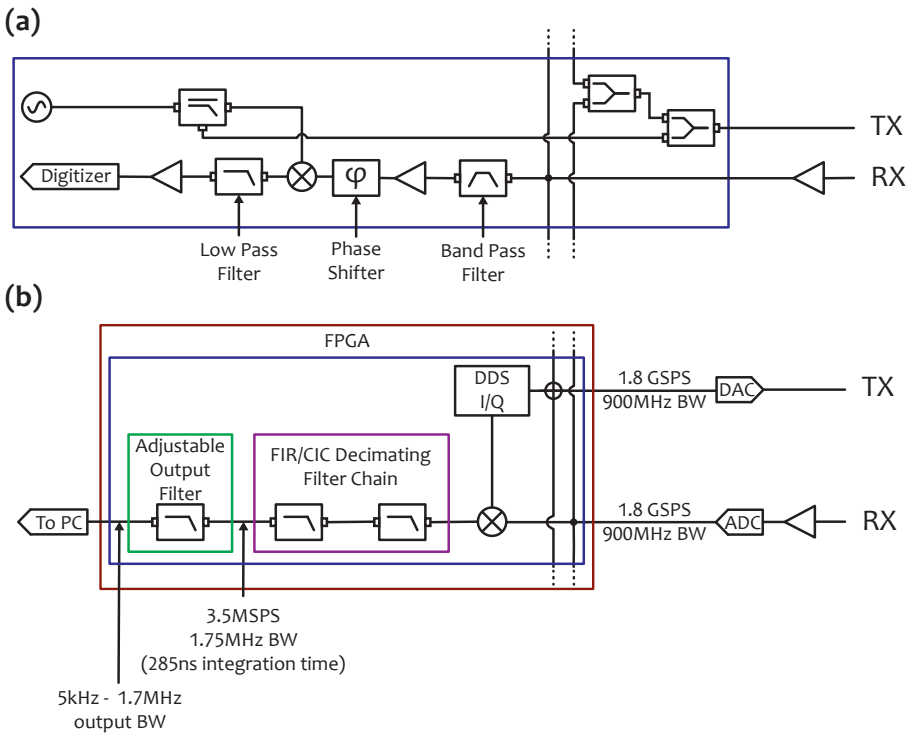

Figure 2.4: (a) Schematic of an analog homodyne multichannel readout setup. Elements contained within the blue block must be repeated for each channel. A high-isolation band-pass filter is required per channel due to large non-linearities in the mixer. The use of a heterodyne receiver (not shown) allows phase sensitive detection, however requires a second analog signal generator. (b) The equivalent digital multichannel readout setup. Again, repeated elements are contained in the blue box, however in this case, all repeated elements are digital, hence require no additional hardware. Bandwidths for components used in our lab are shown.

number of qubits. An equivalent digital circuit is shown in Fig. 2.4 (b). For such a read-out chain, all repeated elements are in digital logic, hence, up to the resource limits of the FPGA, no additional hardware is required to increase the channel count. Above around 32 channels, an alternative approach becomes necessary, which I flag in Sec. 2.3, however I will not present results here.

Having introduced the general structure of an architecture for a semiconductor based quantum computer, the remainder of this chapter deals with the practical implementation of some architectures, which progressively reduce the power dissipated and resource requirements at each stage of the architecture, at the expense of flexibility. Section 2.2 proposes an architecture for a quantum computer that reduces the need for high-bandwidth wiring to low temperature, covers the distribution of pulses at the qubit interface and introduces low power cryogenic switches to accomplish that goal. Section 2.3 proposes an architecture that utilizes CryoCMOS to drastically reduce the wiring requirements for a large scale quantum computer, and creates a platform for scalable control of large numbers of qubits.

2.2 Cryogenic Control Architecture for Large-Scale Quantum Computing

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Abstract

Solid-state qubits have recently advanced to the level that enables them, in principle, to be scaled-up into fault-tolerant quantum computers. As these physical qubits continue to advance, meeting the challenge of realising a quantum machine will also require the development of new supporting devices and control architectures with complexity far beyond the systems used in today's few-qubit experiments. Here, we report a micro-architecture for controlling and reading out qubits during the execution of a quantum algorithm such as an error correcting code. We demonstrate the basic principles of this architecture using a cryogenic switch matrix, implemented via high electron mobility transistors (HEMTs) and a new kind of semiconductor device based on gate-switchable capacitance. The switch matrix is used to route microwave waveforms to qubits under the control of a field-programmable gate array (FPGA), also operating at cryogenic temperatures. Taken together, these results suggest a viable approach for controlling large-scale quantum systems using semiconductor technology.

2.2.1 Introduction

Realising the classical control and readout system of a quantum computer is a formidable scientific and engineering challenge in its own right, likely requiring the invention of a suite of new devices with tailored physical properties. Already underway for this purpose is the development of near quantum-limited amplifiers [162, 163, 164, 165], small footprint circulators [166], ultra-low loss resonators [167, 168], cryogenic filters [169], and interconnect solutions [170, 171, 172]. The hardware for classical data conversion and processing however, has yet to be tightly integrated with the quantum technology. Such a classical control interface must be fast, relative to the timescales of qubit decoherence, low noise, so not to disturb the fragile operation of qubits, and scalable with respect to physical resources[173, 174, 175]. A particular challenge is ensuring that the footprint for routing signal lines or the operating power does not grow rapidly as the number of qubits increases[176, 40]. As solid-state quantum processors will likely operate below 1 kelvin[177, 178, 179, 58, 180], there are advantages to also locating components of the control system in a cryogenic environment, adding further constraints.

Similar challenges have long been addressed in the satellite and space exploration community[181], where the need for high-frequency electronic systems operating reliably in extreme environments has driven the development of new circuits and devices [182]. Quantum computing systems, on the other hand, have to date largely relied on brute-force approaches, controlling a few qubits directly via room temperature electronics that is hardwired to the quantum device at cryogenic temperatures.

Here we present a control architecture for operating a cryogenic quantum processor autonomously and demonstrate its basic building blocks using a semiconductor qubit. This architecture addresses many aspects related to scalability of the control interface by embedding multiplexing sub-systems at cryogenic temperatures and separating the high-bandwidth analog control waveforms from the digital addressing needed to select qubits for manipulation. Our demonstration makes use of a semiconductor switch matrix constructed using high electron mobility transistors and a new type of microwave switch element based on the gate-tuneable capacitive response of a heterostructure device. Under the control of a commercial, field-programmable gate array (FPGA) made to operate at 4 kelvin, the switch matrix is used to route microwave signals to selected quantum dot qubits at 20 mK. Bringing these sub-systems together in the context of our control architecture suggests a path for scale-up of control hardware needed to manipulate the large numbers of qubits in a useful quantum machine.

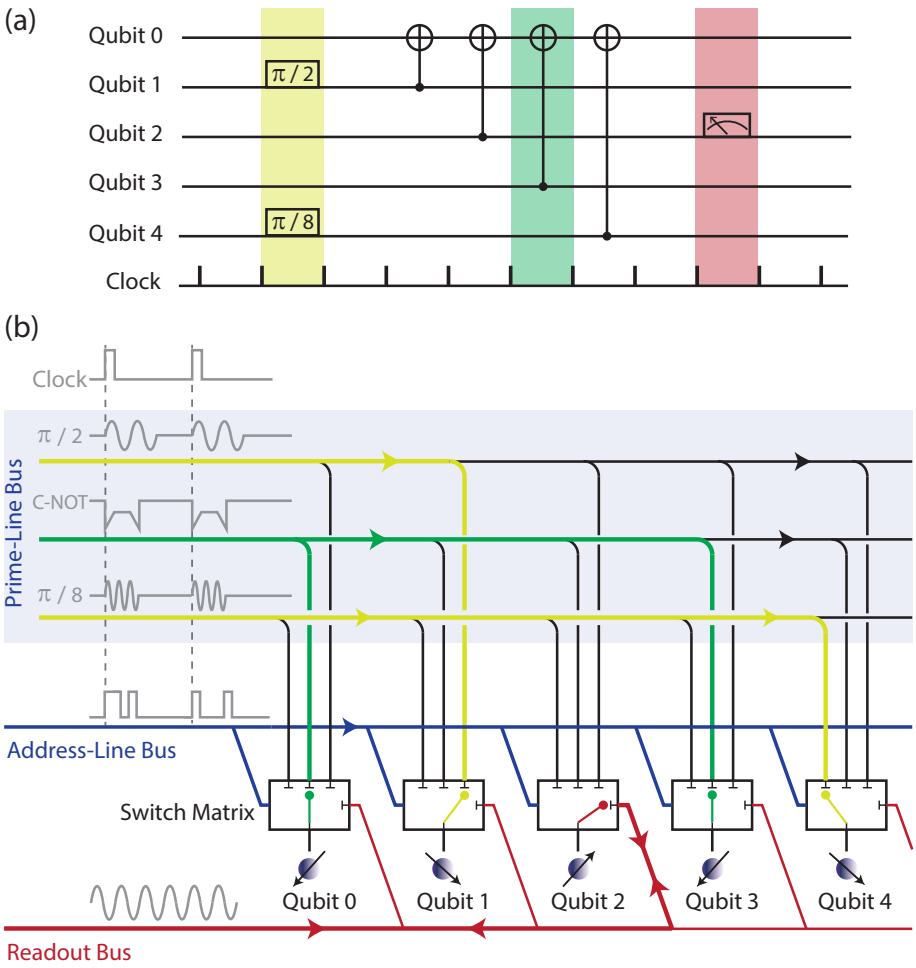

Figure 2.5: 'Prime-line / Address-line' (PL/AL) architecture that separates prime analog waveforms, used to manipulate qubits, from the addressing data used to select qubits. (a) An example sub-section of a quantum algorithm shown using quantum circuit notation. The highlighted clock cycles include single-qubit rotations (yellow), a two-qubit gate (green) and readout operation (red). Note that multiple operations are intended in a given clock cycle such that the required analog waveform for control or readout can be connected in parallel to any qubit. (b) Prime-lines corresponding to a universal gate set are routed to qubits via a switch matrix controlled by the address-lines. Coloured paths correspond to the highlighted clock cycles in (a). Vertical dashed lines indicate the clocking of the analog prime-waveforms which occurs at a rate that is 10-100 times slower than the clocking of the address bus. The clock rate of the address bus will depend on its width and qubit coherence times.

2.2.2 Control Micro-architecture

Our control micro-architecture executes a quantum algorithm by decomposing it into a sequence of universal quantum gates, allowing for arbitrary logic operations to be realized using a small set of repeated single- and two-qubit unitaries applied in sequence. At the level of physical qubits in the solid-state, whether they are spins [183], transmons [179, 177], or quasi-particles [99], these elemental gate operations amount to applying calibrated electrical waveforms to a particular set of qubits or pairs of qubits each clock cycle as determined by a quantum algorithm.

A key aspect of our control architecture is the separation of these analog 'prime waveforms', which are typically pulses at microwave frequencies, from the digital qubit addressing information that determines which waveform is directed to which qubit, at a particular point in the code. In comparison to brute-force approaches, this scheme lifts the need of having a separate waveform generator and transmission line for each qubit, taking advantage of a small universal gate set that uses the same analog waveforms over-and-over throughout the algorithm. As realistic qubits will inevitably include variations in their physical parameters, the control architecture must also incorporate means of calibrating and adjusting the response of the qubit to the control waveforms, as described below.

Our 'prime-line / address-line' (PL/AL) architecture is shown schematically in Fig. 2.5, where we have drawn part of a circuit for implementing a quantum error correcting surface code [184, 185]. Precisely timed analog prime waveforms, generated at cryogenic or room temperature, propagate cyclicly on a high-bandwidth prime-line bus that is terminated with a matched impedance at a location in the system where heat can be dissipated. The quantum algorithm is then executed exclusively via the digital address-line bus, selecting qubits and qubit pairs to receive the appropriate prime waveform at the correct clock cycle in the circuit. Readout proceeds in a similar way, with the digital address bus selecting a particular qubit (or readout device) for interfacing with multiplexing devices [186, 143] and analog readout circuitry such as a chain of amplifiers and data converters.

2.2.3 Implementation of the Control Architecture

Realising our PL/AL architecture requires integrating multi-component control and readout hardware with the quantum system of qubits fabricated on a chip. Owing to the large number of qubits that are likely to be needed for quantum computation and the timescales involved in their control, there are advantages to locating sub-systems of the control architecture at cryogenic temperatures, either on-chip with the physical qubits, or in close prox-

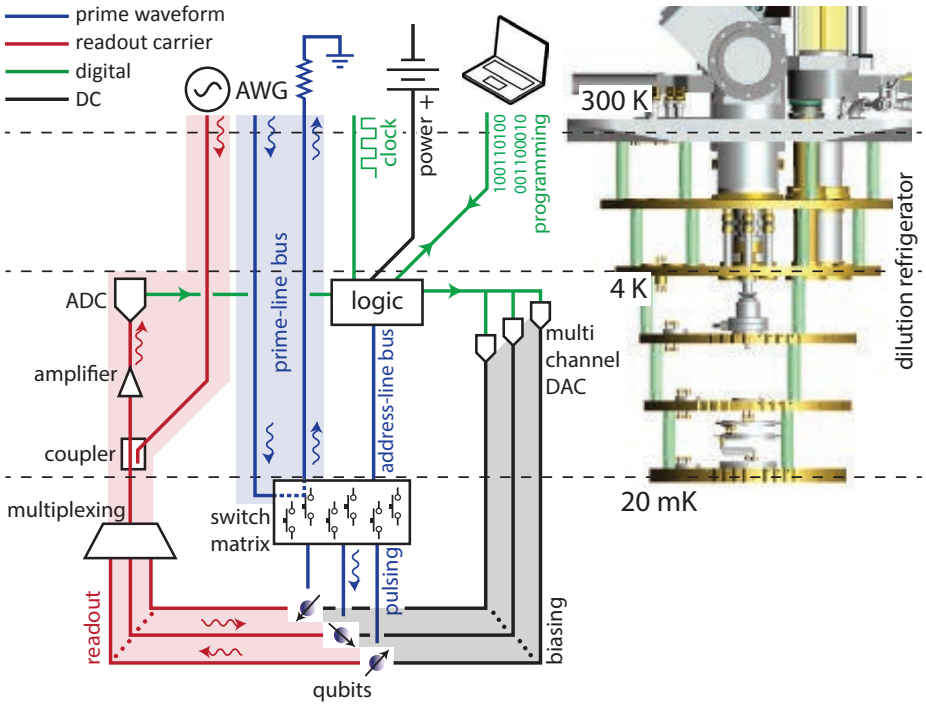

Figure 2.6: Schematic of a control micro-architecture that distributes sub-systems across the various temperature stages of a dilution refrigerator, depending on the available cooling power (image is of a Leiden Cryogenics CF450). A millikelvin switch matrix, on the same chip as the qubit device or close to it, steers a small number of control pulses to qubits using addressing information from cryogenic logic at 4 K. The matrix will incorporate a level of digital decoding to enable switch addresses to be transmitted on a relatively small number of serial lines.The cryogenic logic also interfaces with multiplexed readout and digital-to-analog converters. The 4 K stage typically has a cooling power $\sim$ 1 W, with the 20 mK stage having less than 10 μW.

imity and connected via integrated multi-chip modules [187] and compact transmission lines. Aspects of the control system will however, generate significant heat or fail to function at the millikelvin temperatures needed for qubit operation. The competing constraints of interconnect density, heat generation, signal latency, footprint, and noise performance suggest a control architecture that is distributed across a cryostat, taking advantage of the significantly different thermal budgets available at each temperature stage. This distributed architecture is illustrated in Fig. 2.6, where control sub-systems are positioned at different temperature stages of a cryogen-free dilution refrigerator. Below we describe and provide a basic demonstration of these sub-systems.

Switch Matrix

The key sub-system underpinning the control micro-architecture is a switch matrix, or routing technology that steers the prime waveforms to particular qubits based on a digital ad-

dress. This technology is ideally located in close proximity to the qubits to avoid latency and synchronization challenges that arise when signals propagate over length-scales comparable to the electromagnetic wavelength (typically centimetres for quantum control waveforms). Physically integrating the switch matrix and qubit system has the further advantage of significantly reducing the wiring and interconnect density by making use of lithography (or multi-chip module packaging) to provide connection fan-out. In this way we envisage a switch matrix that receives multiplexed data on a small number of transmission lines and decodes this address data to operate large numbers of parallel switches (see Fig. 2.6). Multiplexing of this kind will likely be essential for operation in cryogenic environments where large numbers of parallel transmission lines add a sizeable heat load when carrying signals between stages that are at different temperatures. The use of superconducting materials is key as these can dramatically reduce the cross-section and thereby thermal load of transmission lines without degrading electrical performance [187].

A switch matrix with elements that act as variable impedances can also be configured to enable the amplitude and phase of the prime waveforms to be individually adjusted before arriving at each qubit. By incorporating a calibration routine or feedback scheme, this approach can be used to account for the variation in physical parameters that will inevitably occur with systems comprising large numbers of qubits.

Various technologies appear suitable for constructing such a switch matrix, including semiconducting devices [188, 189, 190], mechanical systems [191, 192], and superconducting logic [193, 194]. For qubit technologies built from semiconductors [157, 180], field-effect based devices are ideally suited owing to their sub-nanosecond switching-speed, gigahertz transmission bandwidth, low dissipation, small footprint, cryogenic compatibility, and opportunity for integration with qubits. Below we demonstrate the operation of such devices using GaAs high electron mobility transistor (HEMT) circuits, configured as a switch matrix with variable amplitude and phase response. We note that complex circuits constructed from HEMTs demonstrate that these devices are well suited to extensive fan-out [195].

HEMT Switching Elements

A prototype HEMT-style microwave switch based on a GaAs/AlGaAs heterostructure is shown in Fig. 2.7(a,b). Fabrication of these switching elements follows a similar procedure to quantum dot qubit devices (allowing easy integration). The mesa is wet etched using dilute H_3SO_4, before Au/Ge/Ni ohmic contacts are thermally evaporated and annealed at 470 °C for 100 s. The final metal layer is thermally evaporated TiAu (10 nm / 100 nm).

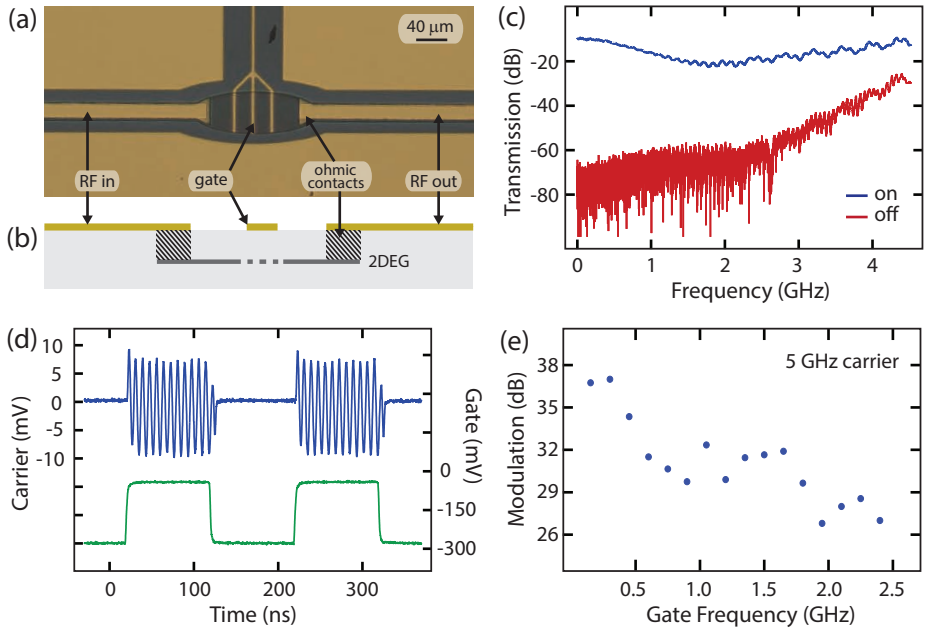

Figure 2.7: Characterisation of a HEMT switch as a building block for the PL/AL architecture. (a) Microscope photograph of the device fabricated on GaAs/$Al_{0.3}Ga_{0.7}As$ heterostructure. (b) Schematic cross-section showing the coplanar line diverted through the 2DEG. A negative voltage ($-300\,\mathrm{mV}$) on the top gate increases the impedance of the switch, reflecting the input signal. (c) Transmission as a function of frequency for the on (blue) and off (red) state. (d) Example of time-domain response. When the gate voltage (green) is zero, the $120\,\mathrm{MHz}$ sine wave provided at the switch input is propagated to the output (blue), and not otherwise. (e) Modulating a carrier signal through the 2DEG with a sinusoidal gate voltage creates sidebands. The amplitude of the sidebands as a function of frequency indicates a $1\,\mathrm{ns}$ to $2\,\mathrm{ns}$ switching time.

In the on-state, the switch is configured to have a characteristic impedance of $\sim 50\,\Omega$, owing to its coplanar waveguide (CPW) geometry. Prime waveforms are fed to and from the HEMT two-dimensional electron gas (2DEG) via eutectic ohmic contacts and TiAu planar transmission lines. In the off-state a negative voltage applied to the TiAu top gate pinches-off the electron gas channel, reflecting the prime waveform signal due to the large impedance of the HEMT relative to the characteristic impedance of the $\sim 50\,\Omega$ feedline. The transmission response of the switch is shown in Fig. 2.7(c), with an on/off ratio (OOR) above 40 dB in the frequency range 0 GHz to 2.5 GHz, suitable for control of spin qubits [196]. For these prototype devices a large insertion loss of 10 dB to 20 dB is observed, owing mostly to the resistance of the ohmic contacts, which is currently a few hundred ohms in our process. Precise control of the contact resistance and capacitance using ion-implantation can overcome this limitation and also dramatically shrink the footprint of these devices [197, 198].

The time-domain response of the switch is demonstrated by amplitude modulating an

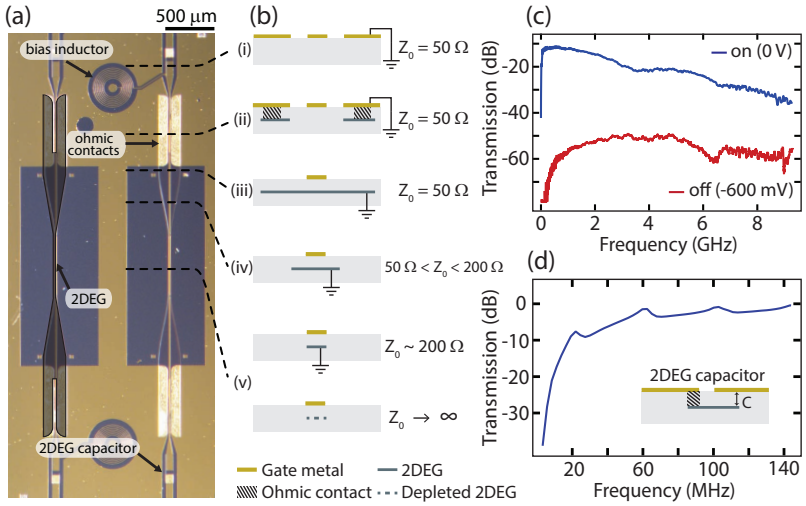

Figure 2.8: A switch design that produces an impedance mismatch by depleting the transmission line ground plane. Shown is an image (a) and cross-sections (b) of the device. The input is a coplanar line (i) which transitions to a microstrip using the 2DEG as the ground plane (ii,iii). The ground plane is tapered so that it lies beneath the signal track (iv,v). When a negative voltage is applied to the signal track, the ground plane is depleted (v) and the impedance mismatch reflects the input signal. (c) Transmission through the switch in the on (blue) and off (red) states. (d) Frequency response of capacitors formed using surface gates and 2DEG as a parallel plate (inset).

applied 120 MHz constant wave tone, as shown in Fig. 2.7(d). To determine the maximum switching time of the HEMT we modulate a 5 GHz carrier tone with a sinusoidal waveform applied to the gate and measure the depth of modulation as a function of gate frequency, as indicated in Fig. 2.7(e). For these prototype devices the switching time is of order 1 ns.

Capacitive Switching Elements

Microwave switching devices based on the depletion of an electron gas also enable a new capacitive mode of operation. In this configuration the CPW feedline transitions to a microstrip geometry by contacting the electron gas to the planar ground planes using ohmic contacts, as illustrated in Fig. 2.8(a,b). The two conductors in the microstrip transmission line are thus constructed using the top gate and electron gas as ground. This device can act as a reflective switch by depleting the effective ground plane using a negative bias on the gate. Depletion reduces the capacitance between the conductors of the microstrip and modulates the device impedance. Transmission through the switch is shown in Fig. 2.8(c) in the on (blue) and off (red) state, with an OOR greater than 25 dB for 0 GHz to 8 GHz. To the best of our knowledge, a switching device based on a depleted ground plane has not been reported previously.

The switch is capacitively coupled to the input and output ports, with a planar spiral

inductor at one port forming a bias tee to provide the dc gate voltage needed to deplete the electron gas. In place of a planar interdigitated capacitor, we make use of the GaAs heterostructure to provide a low footprint parallel plate capacitor, formed between the CPW central track and the electron gas, as shown in the inset to Fig. 2.8(d). The frequency response of this capacitor is shown in Fig. 2.8(d).

The capacitance-based switch has improved performance at higher frequency than the HEMT-based switch, although it has a larger footprint due to both the length of line needed for adiabatic tapering from 50 Ω to 200 Ω and for the coplanar-to-microstrip transition. Working with a characteristic impedance of $\sim 200\,\Omega$ minimises the area of electron gas and reduces ohmic loss. The improved frequency performance stems from the absence of a gate structure, which in the HEMT switch capacitively couples the source and drain contacts, even in the off state. The required footprint is reduced significantly in an all-microstrip circuit that is designed to operate at a characteristic impedance close to 200 Ω. In their current form the performance of both kinds of switches is better suited to controlling spin qubits, where the frequency of signals are of order 1 GHz. For superconducting qubits, we envisage extending the operation of these switches to frequencies in the 4 GHz to 12 GHz range by shrinking their footprint to suppress parasitic capacitances and inductances that lead to resonances in the present design.

2×2 Switch Matrix

We demonstrate cryogenic operation of a prototype routing matrix based on HEMT switches with two input and two output ports. A magnified image of the device is shown in Fig. 2.9(a) with associated schematic in (b). Each input port is split and connected to each output port via a switch so that the transmission parameters S_{ij} of the device are controlled by the respective gate voltages $V_{i,j}$. The output ports include bias tees, which are needed for use with qubits based on semiconductor quantum dots. Bias tees are constructed using planar spiral inductors and 2DEG-based capacitors as illustrated in the inset of Fig. 2.8(d).

Operation of this switch matrix is demonstrated by comparing the transmission of signals as a function of frequency for path A (blue) and path B (red), as indicated in Fig. 2.9(b). The response through both paths when path A is on ($V_{3,1} = 0\,\text{V}$) and path B is off ($V_{4,1} = -500\,\text{mV}$) is shown in Fig. 2.9(c). The corresponding time-domain response for a 1 GHz tone is shown in Fig. 2.9(d)(i). We observe a negligible (< 0.05 dB) change in the response of one path when the other is path is switched from the on state to the off state. An advantage of semiconductor-based switching elements is their ability to be configured as variable impedances, producing arbitrary amplitude output, as shown in Fig. 2.9(d)(ii).

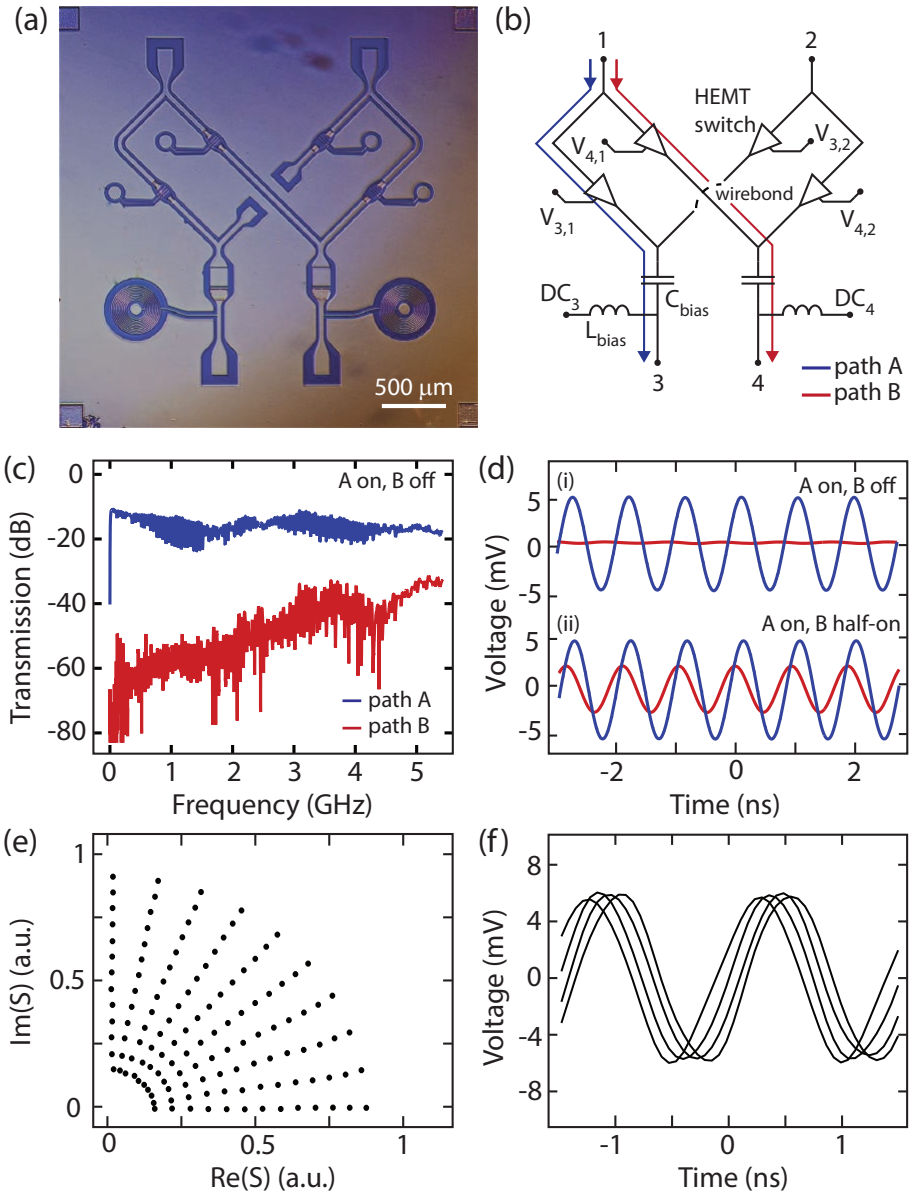

Figure 2.9: Small scale 2-input, 2-output switch matrix based on HEMT switches, with on-chip bias tees for quantum dot operation. Device image is shown in (a) with associated circuit diagram in (b). (c) Transmission measurement with path A (blue) in the on-state and path B (red) in the off-state. (d) Voltage output with a $1\,\mathrm{GHz}$ input tone where path A is in the on-state and path B is (i) off, and (ii) half-on. (e) An example of IQ modulation, implemented by feeding the input ports of the 2×2 matrix with signals that have a $90°$ phase offset. Arbitrary amplitude and phase is produced at the output (data shown in figure) by selecting the appropriate $V_{i,j}$ (see main text). (f) Example voltage output for one of the constant amplitude quarter circles in (e).

We also demonstrate basic IQ modulation using our switch matrix by applying rf tones at both inputs with a 90° phase offset between them. The 90° shift can be produced by a length of transmission line (with narrowband response) or as a separate quadrature prime waveform. The output waveform at angular frequency ω is $A\sin\omega t + B\cos\omega t = R\sin(\omega t + \phi)$, where the magnitude R and phase ϕ are determined by the amplitudes A and B, controlled by the gate voltages $V_{i,j}$. After the calibration function $R, \phi = \mathcal{F}(V_{i,j})$ is generated once, we can select the appropriate $V_{i,j}$ to produce a tone with arbitrary phase and amplitude in the first quadrant of the complex plane, as shown in Fig. 2.9(e). The corresponding voltage output along a quarter circle of constant amplitude is shown in Fig. 2.9(f). By controlling the amplitude and phase shift using the integrated switch matrix, the connection between each qubit and the prime line bus can be specifically adjusted to compensate for the inevitable variation in parameters between physical qubits[3].

Cryogenic Logic

For controlling and programming the switch matrix via the address bus, we envisage a layer of fast, classical logic that serves as an interface between the physical qubits and the compiled quantum algorithm (which will likely comprise mostly an error correcting code). This layer of classical logic is also needed for executing various automatic sequences associated with fast feedback for qubit stabilisation, readout signal conditioning, or open-loop error suppression[199, 75]. For controlling a large-scale quantum computer there are many advantages to locating this classical logic and associated data converters close to the qubits, inside a dilution refrigerator. In comparison to room temperature based control systems, cryogenic operation results in an enhanced clock speed, improved noise performance, reduced signal latency and timing errors, and larger bandwidth. Some of these aspects stem from the ability to make use of compact superconducting transmission lines and interconnects at cryogenic temperatures. We note that locating control electronics inside the vacuum space of the refrigerator allows it to be positioned physically close to qubit device, even if qubits and control systems are at moderately different temperatures.

The choice of technology for constructing this layer of classical control is largely dictated by the qubit coherence times, control signal bandwidth, and the number of simultaneous qubits under control. With a convergence of solid-state qubit coherence times now approaching 1 ms [200, 70, 201], present day CMOS-based FPGAs or application specific integrated circuits (ASICs) operating at 4 K are a viable control platform. Higher perfor-

[3]Calibration of the switch response and qubit can be performed at the same time, measuring the qubit evolution as a function of switch gate voltage

mance control systems that are likely to be realized in the longer term include technologies based on InP devices [202], SiGe BiCMOS [203, 204], and superconducting flux logic [193, 194].

For the basic demonstration of the PL/AL scheme considered here the classical logic is implemented using a commercial FPGA (Xilinx Spartan-3A) that we have made operational at the 4 K stage of a dilution refrigerator. To achieve cryogenic operation the FPGA chip was mounted on a custom, cryogenic printed circuit board that includes components which vary little in their parameters at cryogenic temperatures [171, 172]. Power and clock signals to the FPGA are adjusted for cryogenic operation using room temperature sources and a semi-rigid coax line is configured for sending serial commands, with reprogramming of the low temperature array occurring via a dedicated ribbon cable. With the FPGA mounted at the 4 K stage we measure an idle power dissipation of ~ 30 mW, with negligible increase during dynamic logic operations for the simple code executed here. We estimate a dynamic power dissipation of ~ 100 mW for computational operations that use most of the gates in the Spartan-3 array (further details of cryogenic operation of FPGAs are given elsewhere [205]). The FPGA is programmed to interpret serial communication and output a 3.3 V signal on selected pins to activate prime waveform routing in the switch matrix. These outputs are combined with a negative voltage provided from room temperature via a cold resistive adder so that the switch matrix gates receive -50 mV for the on-state and -380 mV for the off-state voltage.

2.2.4 Semiconductor Qubit Control

We combine the building-blocks of our micro-architecture described above, to demonstrate that a semiconductor qubit can feasibly be controlled autonomously without introducing additional noise or heating to the quantum system. The qubit is a GaAs double quantum dot configured as a charge or spin qubit in the few-electron regime (the heterostructure has a carrier density 2.4×10^{11} cm^{-2} and mobility 4.4×10^5 cm$^2/$(V s) at 20 K). These qubits are commonly controlled using dc-pulse waveforms on the gates to rapidly manipulate the energy levels of the quantum dots [206]. A typical setup connects a waveform generator to each gate using a separate high bandwidth coaxial cable and bias tee.

For this demonstration we connect a single coaxial cable from a waveform generator at room temperature to the input of the 2×2 switch matrix, with the two matrix output ports connected to the two plunger gates LP and RP of the double dot, as shown schematically in Fig. 2.10(a). The waveform generator produces a prime waveform consisting of a 100 kHz square wave (shown in Fig. 2.10(b)) which is then steered by the 4 K FPGA by opening

and closing switches in the matrix depending on commands sent from room temperature.

The charge state of the double dot is sensed using an rf quantum point contact [154, 143], which provides a readout signal V_{rf} as a function of the gate voltages V_L and V_R indicated in (c). With both switches of the matrix set to the off state, a standard charge stability diagram is detected indicating that the off state provides sufficiently high isolation between input and output ports, as shown in Fig. 2.10(d)[4]. In contrast to using the qubit decoherence time to detect additional noise sources from the control circuits, we note that the width and jitter of a quantum dot charge transition provides a broadband probe of electrical noise, including fluctuations that occur on timescales much longer than the qubit coherence.

Sending a command to the cold FPGA allows the prime waveform to be directed to the left, right, or both plunger gates, producing two copies of the charge stability diagram. These copies appear because, on the timescale of the readout, a square wave with 50% duty-cycle configures the double dot in two distinct charge states that are offset from one another by the voltage ΔV_R or ΔV_L, as shown in Fig. 2.10(e-g). We note that the shift measured in Fig. 2.10(g) is the vector sum of the shifts in (e) and (f), account for the cross capacitance between each gate and each dot [207]. In comparison to data taken on the bare quantum dot, we are unable to detect any additional noise or an increase in the electron temperature (which is of order 100 mK) when configuring the charge-state using the cryogenic FPGA and switch matrix.

2.2.5 Discussion

Our simple demonstration of a multi-component control architecture provides a path for scaling up the classical support system needed for operating a large-scale quantum computer. Aspects of this demonstration will also likely find immediate use in improving the performance of few-qubit experiments using electron spins in quantum dots. For example, in using the switch matrix to produce multiple out-of-phase copies of control waveforms, crosstalk can be suppressed by cancelling the voltage that is capacitively coupled to neighbouring surface gates [208]. Using the switch matrix as a high frequency cryogenic multiplexer will also enable the automated testing and characterisation of many devices in a given cool-down experiment. In the longer term, our micro-architecture can be extended to allow additional functionality of the switch matrix, providing qubit control frequency correction

[4]A very small amount of jitter in the charge transitions can be seen due to coupling of the rf-QPC carrier to the gates.

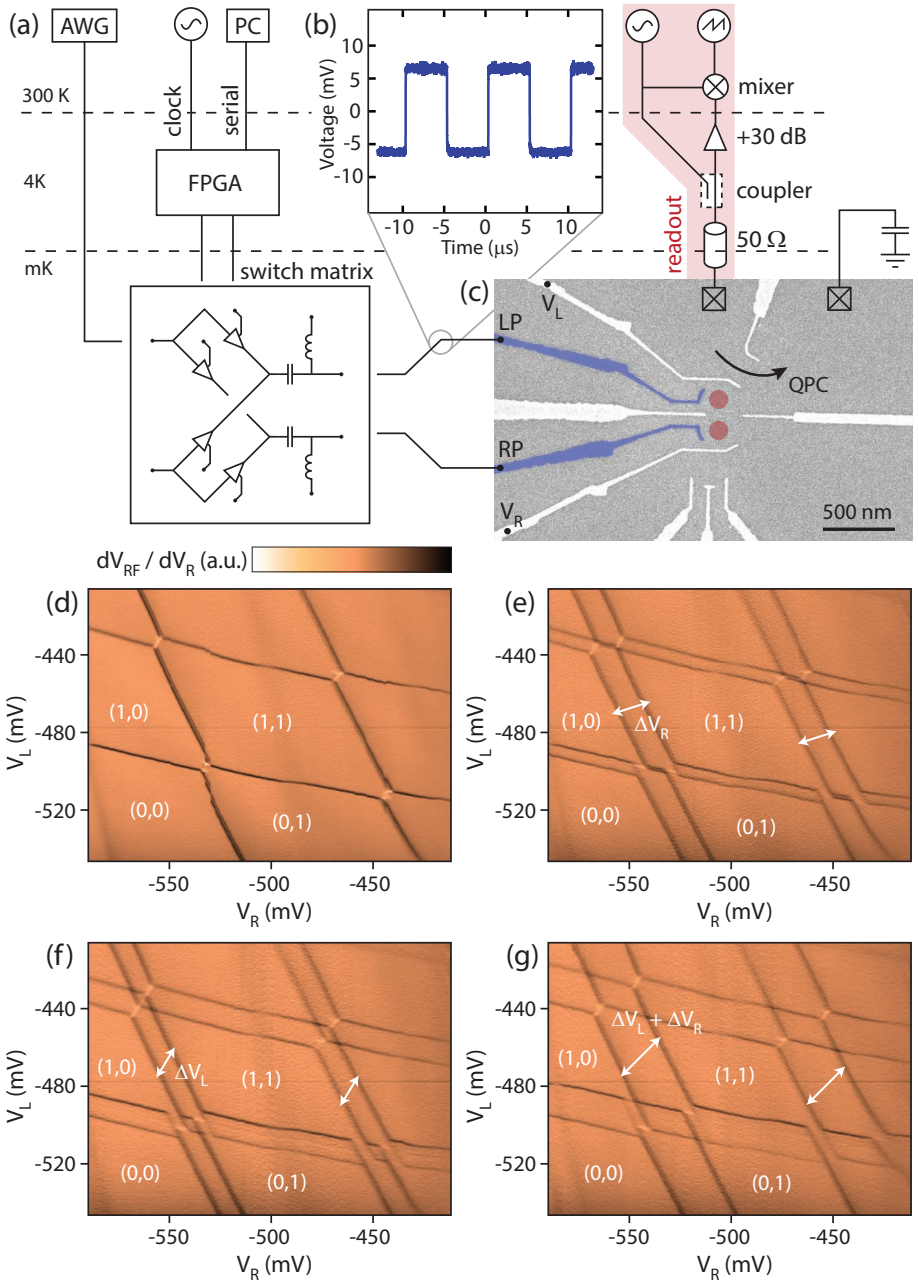

Figure 2.10: Simple implementation of the micro-architecture introduced in Fig. 2.6. (a) Experimental setup for measuring a double quantum dot, using a cryogenic FPGA to steer pulses via a millikelvin switch matrix. Charge-state readout is performed using an rf-QPC. (b) Switch matrix output showing a 100 kHz square wave directed to plunger gates of the quantum dot. (c) Micrograph of the quantum dot device. The shaded gates, labelled LP and RP, are connected to the switch matrix output. (d-g) Charge sensing of the double quantum dot in the few-electron regime, with electron occupancy indicated by the labels (m, n). The colour axis is the derivative of the sensing signal V_{rf} with respect to V_R. When the FPGA-controlled switch matrix blocks waveforms (d), a standard double dot stability diagram is detected. When the square wave is directed to either LP (e), RP (f) or both (g), copies of the stability diagram appear (see text). These measurements demonstrate that the double dot potential can be controlled autonomously by the switch matrix and cold FPGA.

by using the HEMTs as mixers, or as cryogenic adder circuits that reduce the complexity or resolution needed for biasing surface gates that define quantum dots.

We comment here also on the possibility of implementing our PL/AL control architecture using a switch matrix based on single flux quanta superconducting logic [194]. Such logic already appears well suited to control flux-based qubits at high speed and with low dissipation. To what extend these devices are compatible with magnetic fields and the need to generate and steer large voltage waveforms required in the operation of semiconductor qubits remains an open question.

At the layer of classical logic, our demonstration shows that commercial FPGA devices can be configured to work at cryogenic temperatures and are compatible with controlling qubits in close proximity. Beyond the control architecture presented here, the use of cold, low-latency classical logic will likely improve the performance of feedback systems generally needed for adaptive measurement, quantum state distillation, and error correction protocols. A further consideration is the heat generated by the switch matrix, which must operate at the mixing chamber stage of a dilution refrigerator. Given that these switches are reflective, rather than dissipative at microwave frequencies, heat generation will be dominated by the charging of the gate capacitance with each switch, as is the case for today's room temperature CMOS technology. For 1000 HEMT switches of the kind shown here operating at a clock frequency of 1 GHz, we estimate a total power dissipation 100 μW. Straightforward improvements in switch design, such as a reduction in sub-threshold voltage swing at low temperature, can likely reduce dissipation by a factor of 100. Even so, improvements in cryogenic refrigeration technology, both at the chip-level [209] and cryostat, similar to what has been achieved in rare-event physics [210], will likely be needed to enable large-scale quantum information processing.

2.2.6 Conclusion

We have proposed a micro-architecture for the control of a large-scale quantum processor at cryogenic temperatures. The separation of analog control prime waveforms from the digital addressing needed to select qubits offers a means of scaling this approach to the numbers of qubits needed for a computation. To demonstrate the feasibility of our scheme we have shown that a semiconductor qubit can be controlled using a cryogenic FPGA system and custom switch matrix for steering analog waveforms at low temperature. We anticipate that integrated, autonomous control systems of this kind will be increasingly important in the development and demonstration of fault tolerant quantum machines.

Acknowledgements

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2.3 A CryoCMOS Based Control Architecture for Scaling Quantum Computers

In Sec. 2.1.1 and Sec. 2.1.2, the requirements for control and readout of semiconductor qubits were discussed, including a discussion of where power is unavoidably dissipated in the system. These power requirements were summarized in Table 2.1. While experiments involving a single qubit, or even a few qubits, have been able to sidestep the issues associated with such power dissipation at the various temperature stages of the cryostat, moving past as few as 20 qubits quickly becomes impractical. This can be seen if one considers the typical cooling power of these stages. Using the BlueFors LD-400 system [211] as an example of a typical dilution refrigerator, and using a Cryomech PT420 pulse tube cryocooler [212] for cooling to 4 K, we find a cooling power of $\sim$ 100 μW at the mK stage and 2 W at the 4 K stage when operating at temperatures of 40 mK and 4.2 K on the mK and 4 K stages respectively. Under similar assumptions to those laid out in Sec. 2.1.1 we find a maximum capacity of only 20 control lines at the 4 K stage and 100 control lines at the mK stage. Using the Prime-Lines architecture presented in Sec. 2.2, the cooling requirements at 4 K are reduced. However, solutions for scaling control lines at mK remain open.

In this section, we propose a CryoCMOS based architecture to reduce the wiring requirements and power dissipation at the lowest stages of a dilution refrigerator. This architecture fixes the number of static lines required to define a semiconductor-based qubit to three, by providing a mechanism by which static voltages may be "locked" onto the gate, and for reducing the growth of power consumption at the mK stage of the dilution refrigerator by generating fast control pulses near the qubit interface. In this way, the power consumption is reduced from the dissipation through filters on the coaxial lines, to a $CV^2 f$ dissipation set by the length of the interconnect between the qubit and the pulse generator. This approach is validated using a quantum-dot based qubit device formed on a GaAs/(Al, Ga)As heterostructure, which is used to characterize the operation of our CryoCMOS architecture at a temperature of $\sim$ 40 mK. Bringing together the ideas of Sec. 2.2 with our CryoCMOS architecture, we demonstrate a path for scaling to 100's of qubits within the power budget of commercially available dilution refrigerators.

This section is based on unpublished work, and will include the following authors: S. J. Pauka, K. Das, R. Kalra, A. Moini, Y. Yang, J. D. Watson, G. C. Gardner, S. Fallahi, M. J. Manfra, D. J. Reilly

2.3.1 The CryoCMOS Architecture

Our proposed CryoCMOS architecture is shown in Fig. 2.11 (a). Here, a CryoCMOS chip (orange) acts as an interface to the qubit chip (green), multiplexing a small number of low-frequency dc lines from room temperature to the qubit chip. Control is provided by a microcontroller at the 4K stage of the dilution refrigerator. Readout multiplexing is provided by a series of resonators [143] following standard techniques for rf-reflectometry [154, 213]. Our CryoCMOS chip implementing this architecture is shown in Fig. 2.11 (b). Bond pads around the outside of the chip are used to interface with the microcontroller at 4K, and with the qubit device. Each qubit gate contains a charge-lock fast-gate cell, a simplified schematic of which is given in Fig. 2.11 (c).

Static voltages are provided for gates via a mechanism termed charge locking. In this technique, a high-precision room temperature DAC is used to set a voltage $V_{\mathrm{HOLD,N}}$ on a gate, selected by closing the switch $G_{\mathrm{LOCK,N}}$, shown in Fig. 2.11 (b). A capacitance C_{Σ} is charged and the switch $G_{\mathrm{LOCK,N}}$ is opened, leaving a voltage set on the gate. The total capacitance is set by the capacitance of the bond-wires and by parasitic capacitances on the gates of both the CryoCMOS device and the qubit device. Although similar schemes for locking charges on devices have been proposed in the literature [214, 190], they have suffered from gate voltage leakage rates of several mV per hour, limiting the applicability of such schemes for multiplexing large numbers of gates, as refresh times of several ms would be required.

Charge locking allows a large number of static gates on the qubit device to be operated from a minimal number of lines running from room temperature. However, the power or footprint required to bring down even thousands of dc lines is not prohibitive, nor is there a current limitation in connecting such a large number of lines to a qubit device. Instead, the principal limitation at present is the dissipation of power in high-bandwidth control lines. As given in Eq. 2.2, reducing the population of thermal photons necessarily involves attenuation or filtering at the mK stage. Hence, to decrease power consumption at this stage, either qubits must be built to be resilient to thermal noise, allowing the magnitude of the attenuation to be reduced, or signal routing and generation must occur at the mK stage, allowing a smaller number of coaxial lines to be used. Designing qubits that are immune to noise is an ongoing area of research [82, 83, 72], however, these approaches trade off insensitivity for large amplitude control pulses. Even for Majorana qubits, the excitation of quasiparticles in a superconductor, which acts as an error mechanism in these qubits, places limits on a minimum amount of filtering that is necessary [215]. It is, therefore, the second approach that we explore here, implementing a two-level fast pulse generator on-chip.

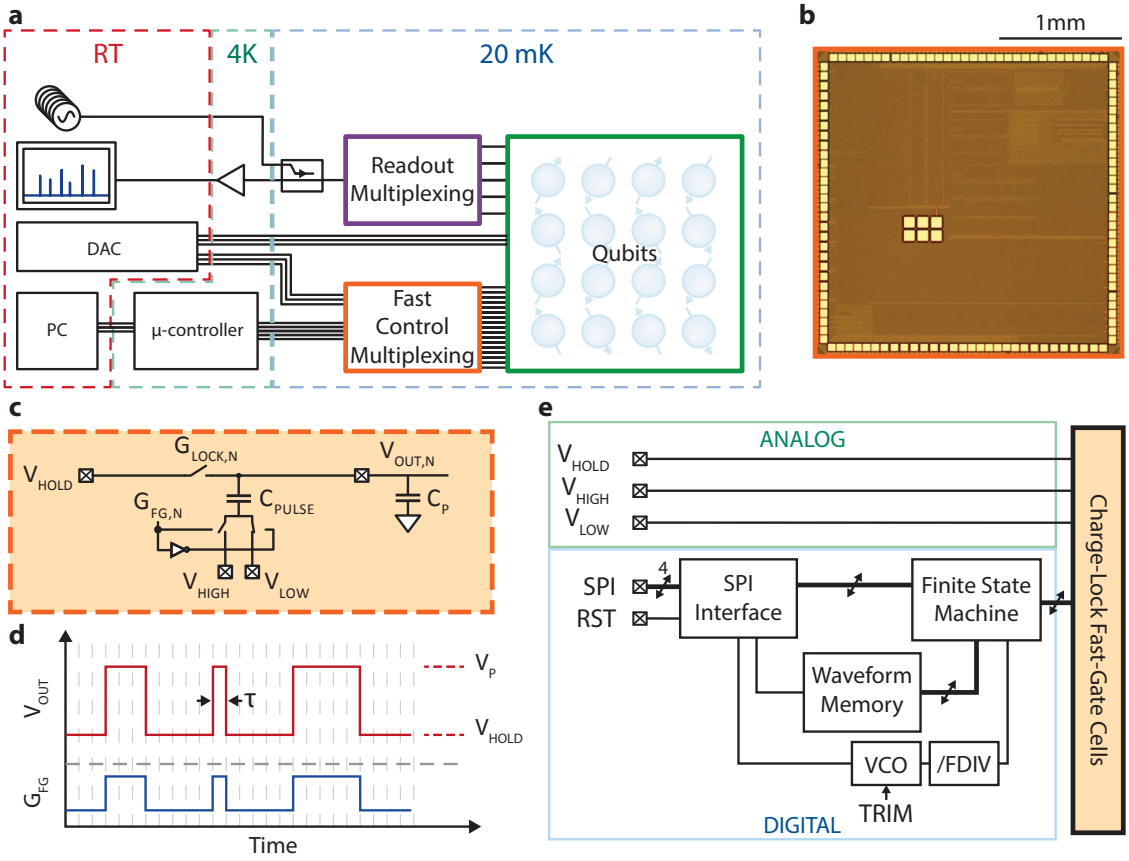

Figure 2.11: (a) Schematic of our proposed CryoCMOS architecture for qubit control. A fast control multiplexing chip allows a qubit chip to be controlled by a small number of digital control lines running from a microcontroller placed at $4\,\mathrm{K}$. Analog voltages are generated at room temperature using a low-noise, high-resolution DAC, and are multiplexed by the chip. Qubit readout is multiplexed using frequency multiplexing [143]. (b) Micrograph of the fast control multiplexing device. The chip has dimensions $2.5 \times 2.5\mathrm{mm}$. (c) Simplified circuit schematic of a single charge-lock fast-gate cell. One cell is connected to each gate of the qubit device. A description of the operation is given in the text. (d) Time trace showing the output waveform as G_{FG} is switched. The voltage at the output cell is pulsed between V_{P} and V_{HOLD}, with sample period τ. (e) Block diagram of the control circuitry inside the CryoCMOS chip. SPI is used for digital communication to a microcontroller at 4K, which allows waveforms to be loaded into memory and pulse generation to be controlled. A voltage controlled oscillator is used to generate a clock on-chip and controls the sample period τ.

Control pulses are generated on the CryoCMOS device using a method we term fast gating. A ground reference is set on the CryoCMOS chip, through the capacitor C_{PULSE}, referenced either to the voltage V_{LOW} or V_{HIGH}. To generate a control pulse on the charge-locked output voltage, the two switches controlled by $G_{\mathrm{FG,N}}$ are rapidly pulsed, pulling or pushing charges on the output gate, and causing a change in $V_{\mathrm{OUT,N}}$. A sketch of this operating principle is shown in Fig. 2.11 (d), where the magnitude of the pulse $\Delta V_{\mathrm{PULSE}} = V_{\mathrm{P}} - V_{\mathrm{HOLD}}$ is given by:

$$\Delta V_{\mathrm{PULSE}} = \frac{C_{\mathrm{PULSE}}}{C_{\mathrm{P}} + C_{\mathrm{PULSE}}}(V_{\mathrm{HIGH}} - V_{\mathrm{LOW}}) \tag{2.11}$$

Crucially, by placing the CryoCMOS chip in close proximity to the qubit chip, such that parasitic capacitance C_p is minimized, the power dissipated for a given pulse can be minimized. Assuming the system can be described by a lumped element model, valid in the limit that the qubit is near the CryoCMOS chip, the power dissipated in the system is given by:

$$P_{\mathrm{diss}} = \frac{C_{\mathrm{PULSE}} + C_{\mathrm{P}}}{C_{\mathrm{PULSE}} C_{\mathrm{P}}} \left(V_{\mathrm{HIGH}} - V_{\mathrm{LOW}}\right)^2 f \tag{2.12}$$

where f is the average rate of pulses at the device.

A block diagram of the control logic for the CryoCMOS architecture is given in Fig. 2.11 (e). An on-chip waveform memory stores up to 256-time steps of a waveform. An on-chip voltage controlled oscillator is used to drive waveforms, which can be enabled by a small finite state machine. The waveform sampling period can be changed in two ways, the first is by varying the value of TRIM, which changes the clock speed in 6 exponential steps between roughly 6 MHz and 140 MHz, the second is using the clock divider FDIV, which may be varied in linear steps from 2 to 256. The waveform sampling period τ can, therefore, be changed between roughly 23 kHz at (TRIM = 1, FDIV = 255), and 70 MHz at (TRIM = 6, FDIV = 2).

2.3.2 Benchmarking the CryoCMOS chip

The performance of the charge locking system for static control is benchmarked using a quantum-dot based qubit device, shown in Fig. 2.12 (a). The qubit device (green) is a comprised of six 5-dot devices, similar to the ones presented in Sec 4.1, although for the purposes of this test, only a single double-quantum dot is used in the top right of the chip. A scanning electron micrograph of the device is shown in Fig. 2.12 (b). Five of the confining gates, labeled LW, LP, C, RP, and RW, are connected to the CryoCMOS chip with bond-wires,

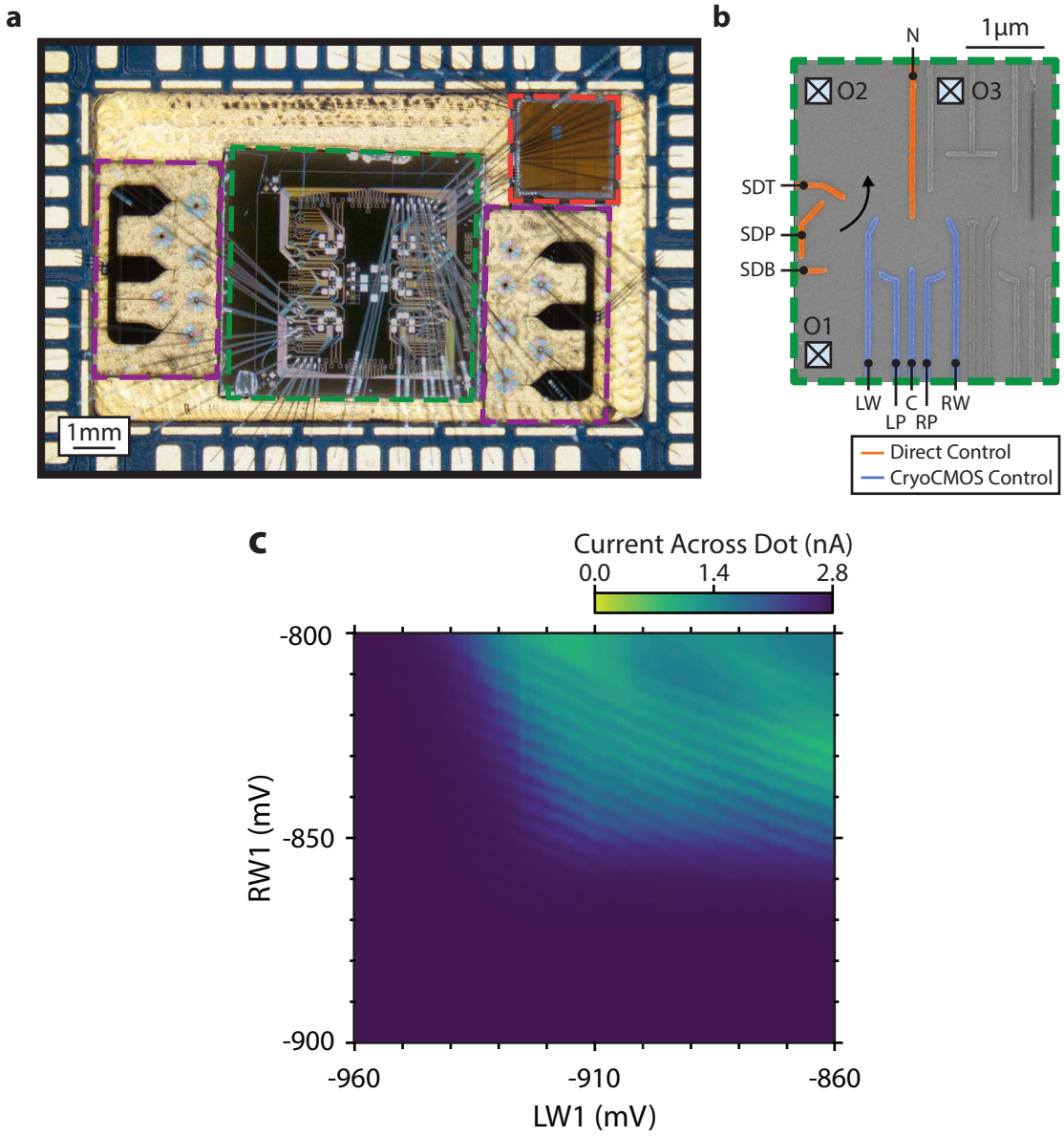

Figure 2.12: (a) Image of the test setup used to benchmark our CryoCMOS chip. A quantum-dot based qubit chip is shown in green, containing a total of 6 five-quantum-dot devices, similar to those introduced in Sec. 4.1. For the purposes of this test, a single double quantum dot is bonded to the CryoCMOS chip, while a second double quantum dot is bonded directly to static control lines. The CryoCMOS chip is shown in orange, while readout multiplexing chips are shown in purple. (b) False color micrograph of the double quantum dot structure. Orange colored gates are controlled directly by a room-temperature DAC, while blue colored gates are controlled by the CryoCMOS chip. Gates are labeled in black. (c) Coulomb blockade through a single quantum dot formed using the CryoCMOS chip to control all quantum dot gates (LW, LP, C, RP, RW), with C sufficiently low that a double quantum dot does not form.

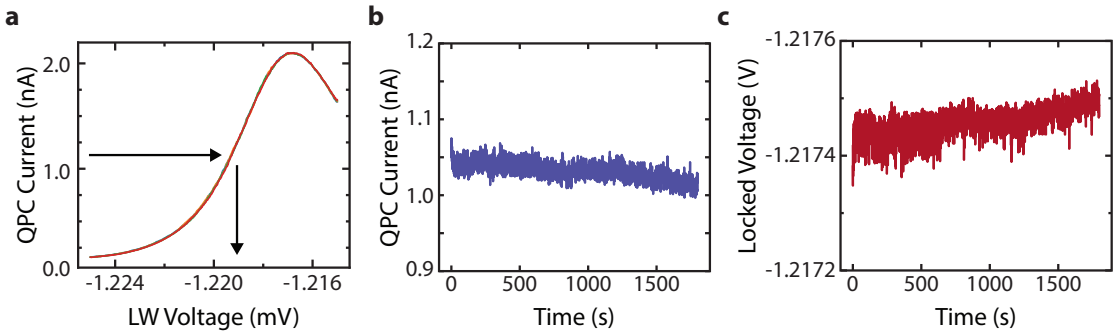

Figure 2.13: Calibration procedure to extract gate voltage. (a) Calibration curves are taken while sweeping LW with the G_{LOCK} switch closed, such that the gate is directly driven. Here four traces are overlaid, validating the stability of the device. Black arrows show how a current through the QPC is converted into a gate voltage. (b) Current through a QPC formed using the gate SDT and LW, once a voltage has been locked on the CryoCMOS controlled gate LW. (c) Extracted value for the CryoCMOS locked voltage on LW, after running the trace in (a) through the calibration curve in (b).

while the remaining gates, SDT, SDP, SDC, and N, are connected directly to the room temperature DAC. It is, therefore, possible to benchmark the CryoCMOS chip with only a single charge-locked gate, passing current through O1 to O2 and measuring a quantum point contact (QPC) formed with the gates SDT and LW, or to benchmark all 5 gates used to define a double quantum dot. As an initial validation of the concept, a single quantum dot is formed using all five CryoCMOS controlled gates and is shown in Fig. 2.12 (c). To take this plot, a static voltage of $-0.5\,\mathrm{V}$ is set on gates LP, C, and RP. For each column of data, a voltage is set and held on gate LW by toggling the switch $G_{\mathrm{LOCK,LW}}$, following which $G_{\mathrm{LOCK,RW}}$ is closed and the voltage V_{HOLD} on the right wall is swept.

To properly characterize the leakage rate of voltages held using the CryoCMOS switches, we form a QPC between the gates SDT and LW. The voltage on SDT is set to a constant value, and the value of V_{HOLD} is swept with $G_{\mathrm{LOCK,LW}}$ closed, while a current between ohmics O1 and O2 is measured. This measurement is repeated several times to ensure the device is stable and is shown in Fig. 2.13 (a). Following this, the voltage is tuned to the steepest point of the QPC pinch-off curve, around 1.1 nA in Fig. 2.13 (a), and held over a 30 minute period, yielding a slow drift in current as shown in Fig. 2.13 (b). Combining Fig. 2.13 (a) and Fig. 2.13 (b), a value for the voltage locked on the gate is extracted in Fig. 2.13 (c). Noise in the measurement is caused by low-frequency charge noise present in the 2DEG [48].

A full characterization of the leakage rate is performed following the procedure laid out in Fig. 2.13, with a hold time of 1 h, for a period of 65 h. Between subsequent sweeps, the QPC is retuned such that sweeps begin at the most sensitive starting point. The optimal

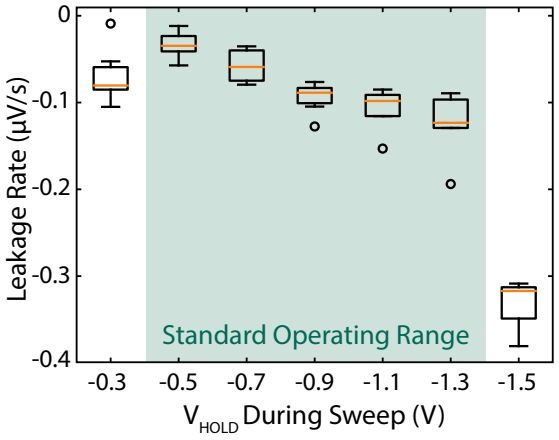

Figure 2.14: Leakage rate of charge locking as the value of V_{HOLD} is varied during the hold. For each datapoint the QPC is tuned to its most sensitive point, which occurs around $V_{\mathrm{LW}} = -0.83\,\mathrm{V}$, and the gate is held for 1 hour. At either extreme of the operating range ($-0.5\,\mathrm{V}$ to $-1.3\,\mathrm{V}$), the leakage rate is found to be unstable.

value of V_{LW} was found to vary between $-0.838\,\mathrm{V}$ to $-0.840\,\mathrm{V}$ over the course of measurements, due to low frequency drift in the device [48]. The resting value of V_{HOLD} during the hold sequence is varied to account for increased leakage when the voltage difference across the switch $G_{\mathrm{LOCK,LW}}$ is changed. The results of this sweep are shown in Fig. 2.14. Across the operating range of $-0.5\,\mathrm{V}$ to $-1.3\,\mathrm{V}$ the average leakage rate was found to be $-81.7\,\mathrm{nV\,s^{-1}}$ or $-294\,\mu\mathrm{V\,h^{-1}}$. Despite the voltage difference across the switch $G_{\mathrm{LOCK,LW}}$ changing from a value less than $V_{\mathrm{LOCK,LW}}$ to a value greater than $V_{\mathrm{LOCK,LW}}$, the leakage is uniformly found to be negative, suggesting it is occurring via the wells of the transistor which are biased to $-1.8\,\mathrm{V}$. To our knowledge, this is the lowest leakage rate for a charge locked device reported in the literature.

Finally, we highlight two sources of parasitic capacitance that must be compensated for in a real device. The first of these is the effect of charge injection [216], caused by the movement of electrons that form the conductive channel in the MOSFET into the source and drain leads, shown schematically in the top panel of Fig. 2.15 (a). When either of these leads is not driven, as is the case when a voltage is held on a gate, an offset in the voltage results after the switch is opened. This effect may be modeled as a simple gate-drain capacitance C_{GD}, with a correction for the quantum capacitance built into this value to account for the density of states in the channel, as given in Eq. 2.3. The offset in gate voltage caused by charge injection ΔV_{CI} is then given by:

$$\Delta V_{\mathrm{CI}} = \frac{C_{\mathrm{GD}}}{C_{\mathrm{GD}} + C_{\mathrm{P}} + C_{\mathrm{PULSE}}} 1.8\,\mathrm{V} \tag{2.13}$$

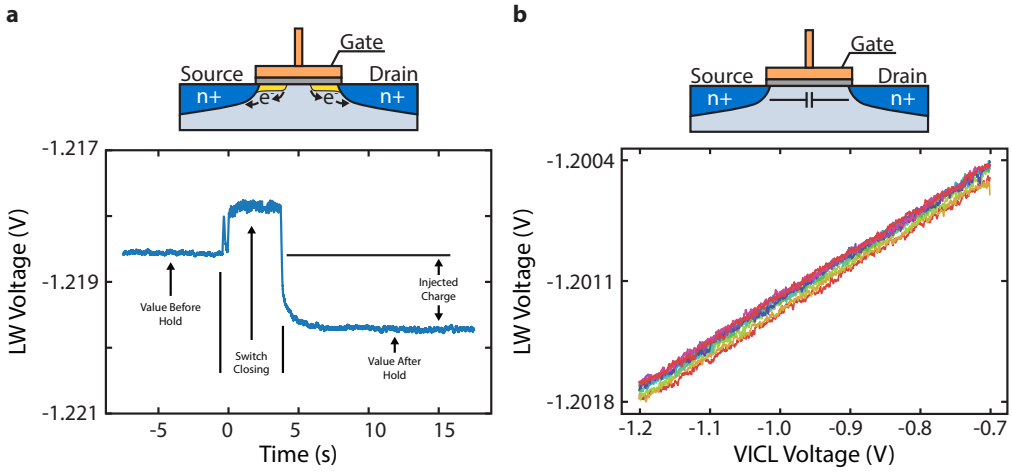

Figure 2.15: (a) Effect of charge injection when opening the switch G_{LOCK}. The charges that form the channel are pushed onto the gate, leading to an offset voltage before and after the switch is opened. This effect can equivalently be understood as a stray capacitance between the gate and drain leads of a transistor. (b) Stray capacitance across the switch, leading to a change in the voltage held on a gate as the disconnected value of V_{HOLD} is swept.

where 1.8 V is the operating voltage of the MOSFETs, and C_{P} and C_{PULSE} are the capacitances holding the voltage of the gate, as shown in Fig. 2.11 (c). The effect of charge injection is shown in Fig. 2.15 (a), and for a single gate is found to take a constant offset of $-1.12\,\mathrm{mV}$ which can be compensated prior to the locking of a charge on a gate. We also highlight that this effect may be compensated in the design stage of the CryoCMOS through techniques known in the literature [217].

The second source of parasitic capacitance that must be compensated is the source-drain capacitance C_{SD} across the charge locking switch, as shown schematically in the top panel of Fig. 2.15 (b). This capacitance leads to a small change ΔV_{SD} in the charge locked voltage, given by:

$$\Delta V_{\mathrm{SD}} = \frac{C_{\mathrm{SD}}}{C_{\mathrm{SD}} + C_{\mathrm{P}} + C_{\mathrm{PULSE}}}(V_{\mathrm{HOLD}} - V_{\mathrm{GATE}}) \tag{2.14}$$

For the LW gate, a change of $\Delta V_{\mathrm{SD}} = 2.8\,\mathrm{mV/V}$ is observed, as shown in Fig. 2.15 (b). Again, this effect may be trivially compensated prior to the locking of a charge on a gate by selecting a fixed value of V_{HOLD} during the operation of the qubit device.

2.3.3 Fast Gating

Finally, we move on to describe the generation of fast pulses at the level of the device. Having described the method used to generate pulses in Sec. 2.3.1, we utilize a quantum dot formed against the LW gate with three directly controlled gates, SDT, SDP, and SDB. In this way,

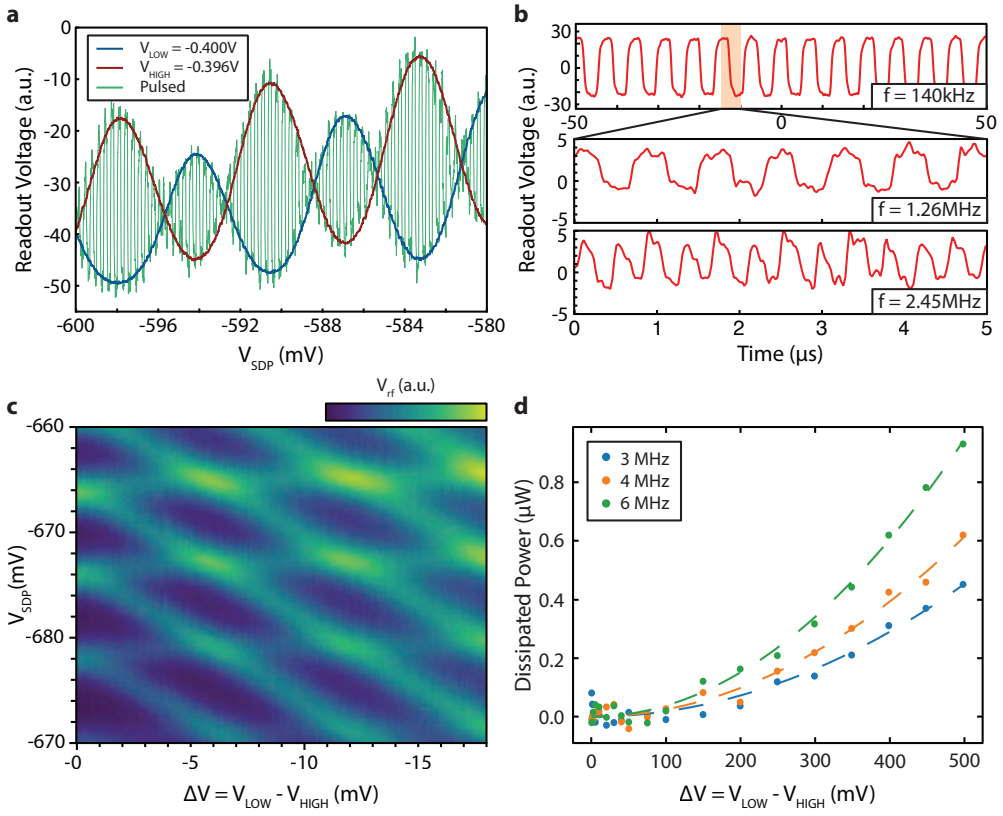

Figure 2.16: (a) Demonstration of fast gating. V_{LOW} is set to $-0.4\,\mathrm{V}$ and V_{HIGH} is set to $-0.396\,\mathrm{V}$. Before fast gating is enabled, $G_{\mathrm{FG,LW}}$ is set to V_{LOW} (blue trace) and V_{SDP} is swept on the room temperature DAC, followed by the same trace taken with $G_{\mathrm{FG,LW}}$ set to V_{HIGH}. Fast gating is then enabled while V_{SDP} is swept (green), showing a trace that pulses between the two slow traces. (b) Demonstration of the tunability of frequency. The top trace shows a square wave at 140 kHz, the middle trace at 1.26 MHz and the bottom trace at 2.45 MHz. (c) Tunability of the pulse amplitude by sweeping $V_{\mathrm{HIGH}} - V_{\mathrm{LOW}}$. Here V_{LOW} is held constant while V_{HIGH} is varied, such that one set of coulomb peaks remains horizontal, while the other moves to more negative voltages. (d) Power dissipated at the mixing chamber as $V_{\mathrm{HIGH}} - V_{\mathrm{LOW}}$ is swept, due to $CV^2 f$ dissipation. Dashed lines are parabolic fits to the data.

we can again characterize the behavior of our CryoCMOS architecture using only a single directly controlled gate. To first extract the expected behavior of fast gating, the value of V_{LOW} is set to $-0.4\,\mathrm{V}$ and V_{HIGH} is set to $-0.396\,\mathrm{V}$, and a 1D trace is taken and shown in Fig. 2.16 (a), sweeping V_{SDP}, with $C_{\mathrm{FG,LW}}$ first set to V_{LOW} in blue, followed by V_{HIGH} in red. Following this, a fixed frequency square waveform is loaded into the waveform memory and run, and the 1D sweep is retaken. The results are shown in green and show a square wave pattern that switches rapidly between the trace taken against V_{LOW} and taken against V_{HIGH}.

Having validated that pulse generation works, we now show that the frequency and amplitude of the pulses may be varied. As described in Sec. 2.3.1, the sample may be modified

in several ways, including by changing the tuning the VCO, through the clock divider and by appropriate choice of the waveform. In Fig. 2.16, we show the variation of the frequency of a square wave from 140 kHz, up to 2.45 MHz through alteration of the clock divider and waveform. Measurements above this frequency are limited by the readout setup; however, we note the potential for operation up to a sample period of 140 MHz.

Variation of the pulse amplitude is performed by changing the difference ΔV between the voltages V_{HIGH} and V_{LOW}. In general, as gates that are not intended to be pulsed have voltages set in reference to V_{LOW}, this value will remain fixed, while V_{HIGH} is varied. In Fig. 2.16 (c), the value of V_{HIGH} is varied on the bottom axis while V_{SDP} is swept. The pulse frequency is configured to be well above the bandwidth of the readout circuit, such that an averaged trace between V_{HOLD} and V_{P} is returned. As such, as ΔV is increased from zero, each coulomb peak splits into two, with one remaining at the same value of V_{SDP}, and the other decreasing towards more negative values of V_{SDP} as V_{HIGH} is increased to more positive values.

Combining these effects, we can extract the power dissipation of the entire circuit. The cooling power of the mixing chamber of the dilution refrigerator is first calibrated using a known resistance. Then, as various circuits on the CryoCMOS chip are enabled, the extra heating of the device is calculated. The static power dissipation for the circuit is extracted to be $\sim 0.1\,\mu$W based on the current drawn on the power rails. Upon enabling the clock, an additional 9 μW of static power dissipation and 2.5 μW/MHz of dynamic power is dissipated by the clock generation circuitry. We note that although this is a significant portion of the power budget at mK, this dissipation is static at a fixed frequency, as this clock is shared by all gates. To extract the heating due to pulses applied to gates, pulses at a known frequency are applied and ΔV is swept. As the total length of routing and bond-wires is on the order of millimeters, a lumped element model is sufficient to calculate dissipation, such that the aggregate dissipated power is given by Eq. 2.12. From this, a total capacitance to ground of 0.6 pF is extracted. The power per gate controlled, assuming a pulse amplitude of 1 mV at 10 MHz is therefore only 6 pW, on top of a static power dissipation of 34 μW, well within the cooling power of a typical dilution refrigerator.

2.3.4 Conclusion

We have proposed a CryoCMOS based architecture for scaling qubit devices up to the hundreds without a large increase in power dissipated at the mK stage of a dilution refrigerator. By placing a CryoCMOS pulse generator close to the qubit chip, the power dissipation per channel may be lowered to 10's of pico-watts. Using our CryoCMOS chip, we are also able

to lock static control voltages on gates with a leakage rate of $-294\,\mu V\,h^{-1}$, the lowest value reported in the literature, allowing the number of static control lines to be reduced to a minimum of three. For large scale quantum machines, we anticipate that some form of cryogenic pulse generation, such as the one presented here, will be crucial to allow large numbers of qubits to be controlled without unacceptable heat dissipation in high-bandwidth control lines.

Acknowledgments

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Chapter 3

Quantum (Anomalous) Hall Effect Circulators

While discussing architectural concerns in Chapter 2, we focused a great deal on the need to reduce the complexity of interconnects, particularly as 2D architectures are scaled up. In doing so, we discussed the need for attenuation in the control wiring of a quantum computer to reduce the thermal population of photons at the qubit interface. Similarly, there is a need for isolation in the readout chain, however as we explored in Sec. 2.1.2, the effective noise temperature T_{eff} is set by the first stage amplifier and by any attenuation which occurs between it and the qubit. As such, particularly for transmon-type experiments where any noise is known to limit qubit lifetimes [218], passive circulators with low loss must be used. These are non-reciprocal devices which route power in a single direction around their ports, i.e. from ports $1 \rightarrow 2$, $2 \rightarrow 3$ and $3 \rightarrow 1$, but not in the inverse direction $1 \not\rightarrow 3$, $3 \not\rightarrow 2$ and $2 \not\rightarrow 1$. Furthermore, when using quantum limited parametric amplifiers such as the traveling-wave parametric amplifier [219], isolators are necessary to limit the action of the pump tone on our qubits. An example of such a circuit is given in Fig. 3.1 (a), showing four circulators used for signal routing and isolation.

Circulators have traditionally been constructed using the Faraday effect in magnetic materials. This causes propagation to occur at different phase velocities in opposite directions through a magnetic material, however, as these devices operate based on the interference of counter-propagating paths, these devices must be constructed with a size on the order of the wavelength of the signal, often several tens of centimeters. An example of such a device is shown in Fig. 3.1 (b). It was proposed by Giovanni Viola and David DiVincenzo that slow, chiral charge density waves in the quantum Hall regime, called edge magnetoplasmons (EMPs), might be utilized to construct millimeter-scale circulators [166]. In the

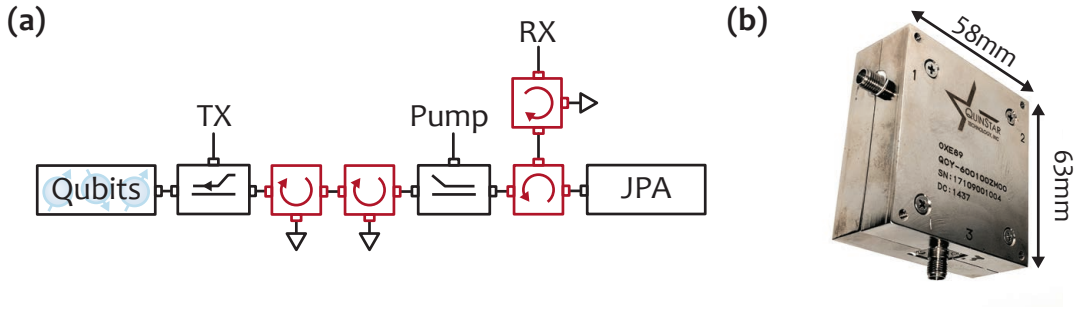

Figure 3.1: (a)Schematic of a standard transmon-like experiment. Circulators, outlined in red, are used to provide isolation between amplifiers and qubits, and to route signals in the circuit. (b) A conventional circulator based on the Faraday effect.

following chapter, I present work that implements this idea to form non-reciprocal devices and demonstrate strong isolation (up to 40 dB). The physics of EMP's is introduced originally in Sec. 1.3.3. In Sec. 3.1 the absorption of EMPs is explored in GaAs, and we use these EMPs to form a micron-scale circulator. In Sec. 3.2, we use the quantum anomalous Hall effect to create circulators that can operate at zero external magnetic field. The dissipation of power is investigated as a function of temperature and applied signal amplitude, although the nature of this dissipation remains an open question.

3.1 On-chip Microwave Quantum Hall Circulator

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Abstract

Circulators are non-reciprocal circuit elements integral to technologies including radar systems, microwave communication transceivers, and the readout of quantum information devices. Their non-reciprocity arises from the interference of microwaves over the centimetre-scale of the signal wavelength, in the presence of bulky magnetic media that breaks time-reversal symmetry. Here we realize a completely passive on-chip microwave circulator with size 1/1000th the wavelength by exploiting the chiral, 'slow-light' response of a 2-dimensional electron gas (2DEG) in the quantum Hall regime. For an integrated GaAs device with 330 μm diameter and approximately 1 GHz centre frequency, a non-reciprocity of 25 dB is observed over a 50 MHz bandwidth. Furthermore, the non-reciprocity can be dynamically tuned by varying the voltage at the port, an aspect that may enable reconfigurable passive routing of microwave signals on-chip.

3.1.1 Introduction

Miniaturized, non-reciprocal devices are currently of broad interest for enabling new applications in acoustics [220], photonics [221, 222], transceiver technology [223], and in the regime of near quantum-limited measurement [224, 225, 226, 227, 166], where they are needed to isolate qubits from their noisy readout circuits. Since the 1950s, passive circuit elements exhibiting non-reciprocity at microwave frequencies have been implemented using bulky magnetic devices that are comparable in scale to the centimetre wavelength of signals in their operating band. The footprint of these components poses a major limitation to integrating entire systems on a chip, such as what is required, for instance, to scale-up quantum computing technology.

A seemingly obvious means of realizing non-reciprocity on a semiconductor chip is to use the Hall effect, where an external magnetic field breaks the time reversal symmetry of electrical transport [228]. Hall-based devices were ruled out in 1954 however [229], since near the electrical contacts, where the current and voltage are collinear, dissipation is so significant that the usefulness of this approach is greatly limited. This dissipative mechanism has an analog in the quantum Hall regime where the two-terminal resistance of a device is always finite over a scale of the inelastic scattering length as carriers transition from their contacts to the dissipationless, one-dimensional (1D) edge-states that support transport [230]. Recently, Viola and DiVincenzo [166] have proposed a means of addressing the limitation imposed by 2-terminal dissipation, suggesting the possibility of coupling microwave signals to the edge of a quantum Hall device reactively, without using traditional ohmic contacts. In a geometry where the signal ports of the device are positioned orthogonal to an incompressible quantum Hall edge-state, microwave power is coupled capacitively and non-dissipative transport in one-direction appears possible [166].

Here we engineer, on-chip, a chiral microwave interferometer that yields a high degree of non-reciprocity and dynamic range, with the low-dissipation inherent to edge transport in the quantum Hall regime. Configured as a completely passive 3-port circulator, our device demonstrates non-reciprocal operation at frequencies and magnetic fields commonly used for the read out of spin qubits [154, 213, 157, 200], facilitating integration with such semiconductor technologies. In comparison to traditional ferrite-based microwave components, this quantum Hall circulator is reduced in size by a factor of $\sim$ 1/1000th the wavelength and exhibits a new mode of operation in which circulation can be dynamically reconfigured either by applying a dc voltage to the port electrodes, or by altering the strength of the magnetic field. A simple model based on a Fano-resonance mechanism [231] qualitatively accounts for the observed phenomena.

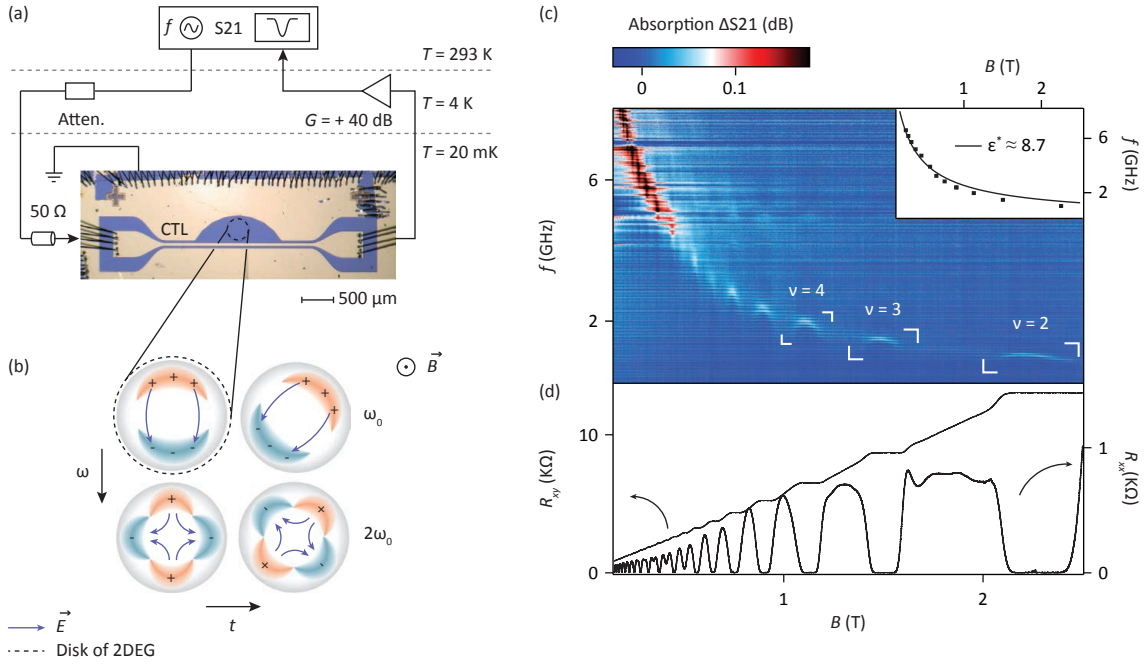

Figure 3.2: (a) Experimental setup including photograph of a coplanar transmission line device similar to that used to perform measurements coupled to a $330\,\mu\mathrm{m}$ etched disc of 2DEG (black dashed circle) at fridge temperature $T = 20\,\mathrm{mK}$. A vector network analyser is used to excite EMP modes across a wide frequency range and microwave absorption is measured as the ratio of the amplified output to input signal (S_{21}) from the CTL. (b) Illustration of the fundamental (top row) and first harmonic (bottom row) EMP modes as they evolve with time, where ω_0 is the fundamental mode and $2\omega_0$ the first harmonic (adapted from [109]). Charge distributions and electric fields $\vec{E}$ are indicated schematically. An external magnetic field B applied to the device points out of the page. (c) EMP spectrum of the quantum Hall disk showing absorbed microwave power as a function of frequency and magnetic field. Data has had a background, obtained at high field, subtracted. Inset shows the position of absorption dips at integer quantum Hall filling factors. Black line is a fit that allows an average effective dielectric constant of $\epsilon^* \approx 8.7$ to be extracted, consistent with excitations of an edge-state in GaAs (see Sec. C.4). (d) Transverse (R_{xy}) and longitudinal (R_{xx}) Hall resistance measurements taken at $T = 20\,\mathrm{mK}$ on a Hall bar proximal to the microwave disk. The 2DEG is $270\,\mathrm{nm}$ below the surface with carrier density $n_s = 1.1 \times 10^{11}\,\mathrm{cm}^{-2}$, and mobility $\mu = 5.2 \times 10^6\,\mathrm{cm}^2/(\mathrm{V\,s})$.

3.1.2 Experimental Setup and Results

Transmission line spectroscopy of EMP modes

Central to the operation of our device are edge magnetoplasmons (EMPs), resonant modes of the electron gas first observed in the classical response of electrons on the surface of liquid Helium [106, 232]. Such excitations have since been found to propagate along a quantum Hall edge in response to a capacitively coupled microwave excitation [109, 233, 234, 235, 236, 237, 238, 239]. These chiral excitations travel with a velocity $v_{EMP} \sim |\vec{E}|/|\vec{B}|$, set by the ratio of the electric field $\vec{E}$ at the sample boundary and the applied magnetic field $\vec{B}$ [234].

For a high mobility 2DEG formed at the interface of the semiconductors GaAs and AlGaAs (see Sec. C.1), the velocity of the EMP modes is typically $v_{EMP} \sim 10^5\,\mathrm{m\,s^{-1}}$ [240, 241], some 1000 times slower than the speed of light in the semiconductor dielectric. In order to exploit these EMPs to realize non-reciprocal microwave devices, we first detect their presence in a contactless etched disk of quantum Hall fluid by coupling to a proximal metallic coplanar transmission line (CTL) [242], as shown in Fig. 3.2 (a) and 3.2 (b). By measuring the transmitted microwave power through the CTL as a function of frequency f, a spectrum of discrete features is observed with applied magnetic field B (Fig. 3.2 (c)). We identify EMP modes in the data with frequencies set by the edge velocity and circumference of the disk, following the dependence $f \sim B^{-1}(\log(B^2) + \text{const.})$ [109], and extract the effective dielectric constant $\epsilon^* \approx 8.7$ consistent with the propagation medium [235, 243] (see Sec. C.4). Comparing the microwave spectrum to transport measurements from a Hall bar on the same chip (Fig. 3.2 (d)), we note that at high field (with only the last few Landau levels occupied) features resolve into discrete, crescent-shaped resonances that coincide with minima in the longitudinal resistance R_{xx}, where dissipation is suppressed.

3-Port circulator

To test if these edge magnetoplasmons support the non-reciprocal transmission of microwaves, we implement a standard circulator configuration, with 3 ports arranged at 120-degree intervals around a disk of 2DEG (330 μm diameter), as shown in Fig. 3.3 (a) and 3.3 (b). For a single edge at high magnetic field, a voltage applied to a port capacitance induces an orthogonal current in the edge-state, with an impedance of the order of the inverse conductance quantum ($\sim 26\,\mathrm{k\Omega}$). Given our present measurement setup uses electronic components with a characteristic impedance of $Z_0 \sim 50\,\Omega$, we have added an impedance matching circuit to enhance the response of each port. This network comprises a series chip-inductor $L = 47\,\mathrm{nH}$ in resonance with the stray capacitance C_{stray}. The impedance of the Hall edge could be lowered closer to Z_0 by connecting multiple 2DEG circulators in parallel [244], or by taking advantage of recently proposed 'self-matching' port configurations [245, 246] (see Sec. C.3 for detailed discussion). The circulator is also embedded in a reflectometry arrangement (Fig. 3.3 (c)) that enables a measurement of the port reflection as well as port transmission coefficient, from which dissipation can be estimated. As a control we first measure all microwave S-parameters at zero magnetic field, observing that all directions and ports are equivalent, as shown in Fig. 3.3 (d). An overall frequency-dependent, but reciprocal response can be associated with the impedance matching network, with matching frequency set to $1/\sqrt{LC_{\text{stray}}} \sim 1\,\mathrm{GHz}$. All subsequent measurements are normalized

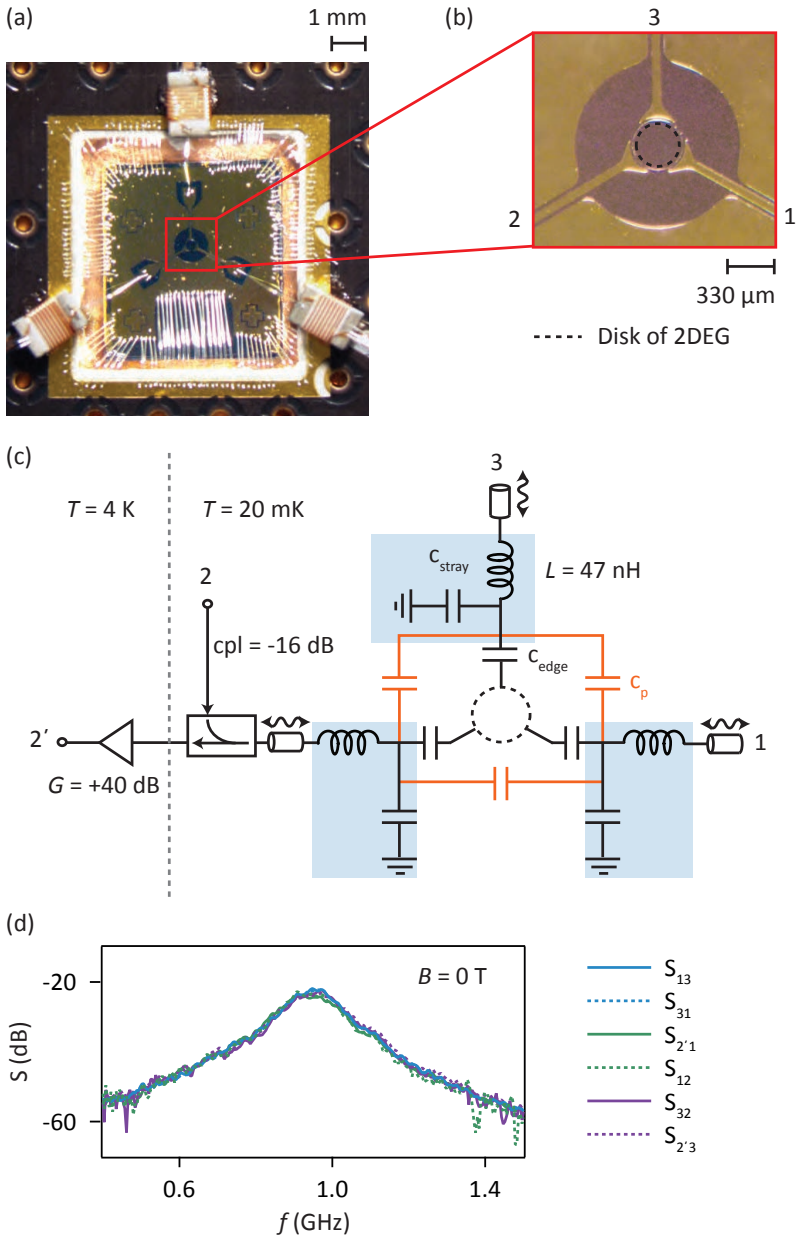

Figure 3.3: (a) Photograph of circulator device showing the three coplanar transmission lines connected to copper wire-wound chip inductors for impedance matching. (b) Close-up of false-coloured photo of the circulator showing $330\,\mu\mathrm{m}$ diameter 2DEG disc with a $20\,\mu\mathrm{m}$ gap to the metal defining the three signal ports. (c) Circuit schematic of the experimental setup indicating port-to-edge capacitive coupling C_{edge} and direct parasitic coupling between ports C_{p}. Resonant (LC_{stray}) matching circuits are indicated with blue boxes. The input of port 2 passes through a directional coupler, with the reflected signal coupled to the output line (denoted $2'$) and amplified at 4 K. (d) Full 6-way transmission response of the circulator at zero magnetic field, with S-parameter measurements indicating complete reciprocity and a frequency response that arises from the matching networks. For each port the measured response of the amplifiers, couplers and cold attenuators in the circuit have been subtracted.

relative to this zero-field transmission response.

Turning to our key result, Fig. 3.4 shows the full transmission response of the 3-port circulator in the presence of a magnetic field that breaks time-reversal symmetry. Similar to the EMP spectrum of Fig. 3.2 (c), we first observe the presence of EMPs which enhance the transmitted power at certain frequencies, broadly following an approximate $f \sim B^{-1}$ dispersion relation, as is seen in Fig. 3.4 (a) (S_{13}) and 3.4 (b) (S_{31}). Strikingly, there are regions of the spectrum where the transmitted power appears to flow in either a forward or reverse direction with respect to the chirality of the edge. Particularly apparent are the crescent-shaped features that switch from forward to reverse transmission at distinct frequencies. This phenomenon, with a peak near the fundamental frequency of the EMP mode and a dip near the first EMP harmonic, is seen for all S-parameters in the chiral (clockwise) direction of the 3-port device (see solid lines in Fig. 3.4 (d)).

To measure the extent of non-reciprocity in our circulator, Fig. 3.4 (c) shows the difference between forward and reverse power by subtracting S_{31} from S_{13}. Unlike the $B = 0$ data shown in Fig. 3.3 (d), we now observe a strong directional dependence in the isolation between ports, that approach 40 dB at particular frequencies and magnetic fields (Fig. 3.4 (f)). Alternatively, we can also test for non-reciprocity by comparing the response of signals from two different inputs of the circulator to a common output. Since the device is geometrically symmetric, the response from the separate paths $S_{2'1}$ and $S_{2'3}$ are the same at $B = 0$, (see Fig. 3.3 (d)). In the presence of a magnetic field however, Fig. 3.4 (g) shows that these paths are no longer equivalent, but depend rather on the direction of the field. This is evident in the data since blue and red features are not mirrored about $B = 0$.

Comparing the microwave response of the circulator to independent quantum Hall transport data suggests two distinct regimes. Between integer filling factors, where R_{xx} is maximised in transport, there is a large non-reciprocity in the microwave response, but also likely strong dissipation. Contrasting these broad regions are narrow crescent-shaped features that occur at fields corresponding to integer filling. These narrow features are particularly strong at frequencies near twice the fundamental EMP resonance. Again, overlaying these features with transport measurements indicates they align with minima in R_{xx}, where dissipation is suppressed. A direct and accurate measurement of the microwave dissipation is challenging in the regime where the impedance of the device is mismatched. Nevertheless, by accounting for the transmitted and reflected signal power we find the dissipation to be a few percent, consistent with the value of $\sim 1\%$ given by our model (discussed below).

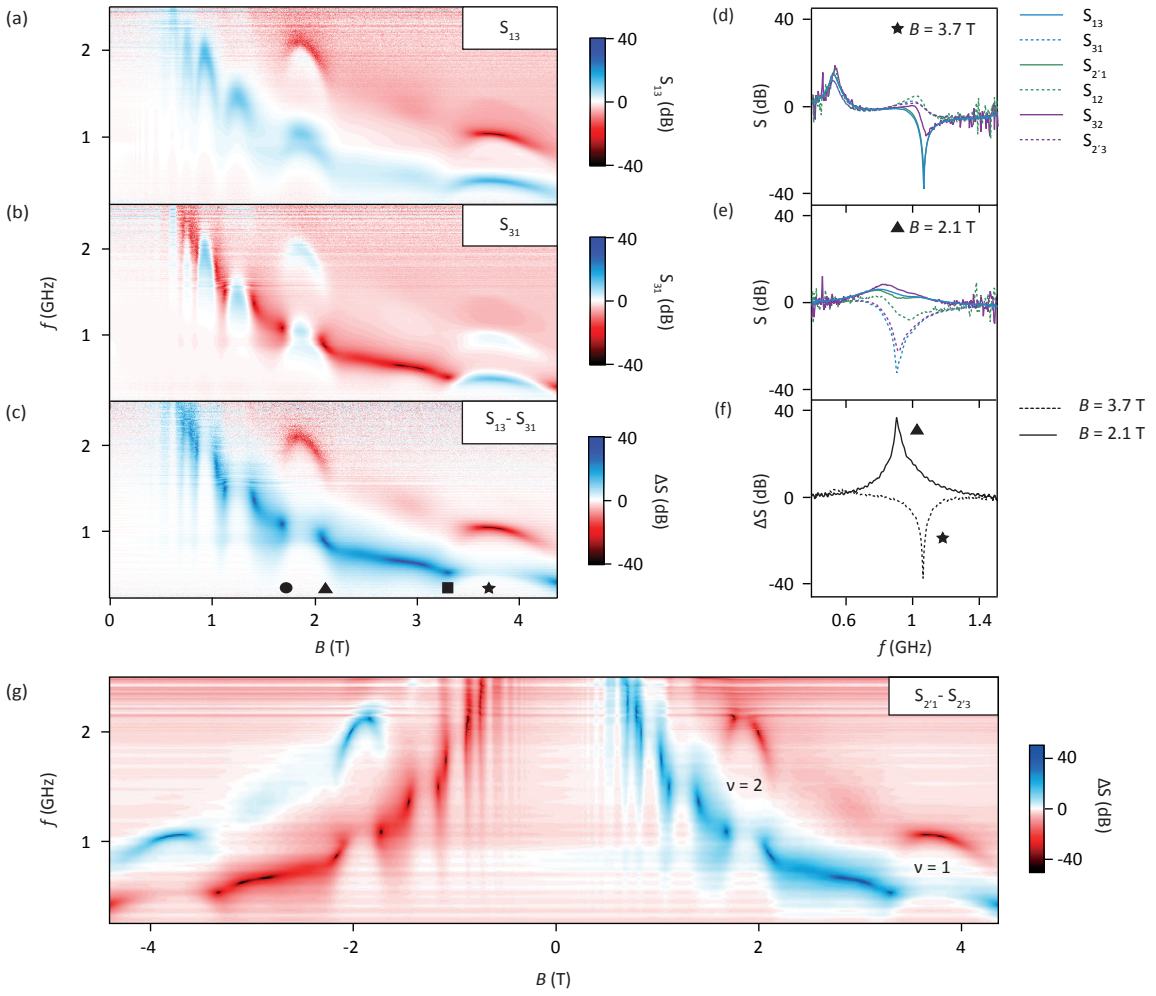

Figure 3.4: (a) and (b) Port transmission S_{13} and S_{31} with frequency and magnetic field. All measurements have been normalized to the gain-corrected background at $B = 0$ (shown in Fig. 2(d)), which defines the $0\,\mathrm{dB}$ point on the colour scale. (c) Microwave response $S_{13} - S_{31}$ showing strong frequency and B-dependent non-reciprocity. (d) and (e) Full combination of transmission S-parameters, taken at B-fields indicated by the symbols in (c). (f) Cuts through the colour scale data in (c), demonstrating forward and reverse circulation. (g) Isolation, $\Delta S = S_{2'1} - S_{2'3}$, measured at positive and negative magnetic fields. Note that the positions of features are symmetric about the $B = 0$ axis, but with opposite sign ΔS.

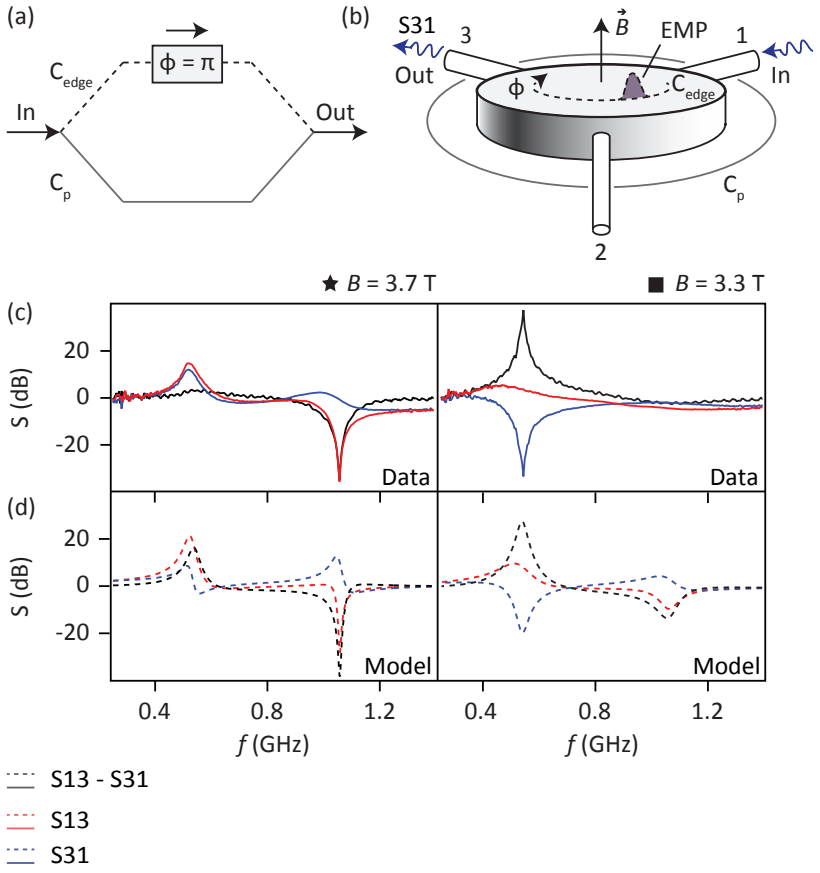

Figure 3.5: (a) and (b) Proposed interferometric mechanism underlying the operation of the quantum Hall circulator, with a slow plasmonic path, via C_{edge}, and a direct capacitive path, via C_{p}. A non-reciprocal response between ports is produced for frequencies where the two paths are out of phase by $\phi = \pi$ in the forward direction and $\phi = 2\pi$ in the reverse direction. (c) and (d) Comparison of a simple model that captures this physics (top graphs), with experimental data (bottom graphs), at two different magnetic fields indicated by the symbols (with respect to Fig. 3.4 (c)). The model is described in detail in the appendix with parameters set to values $Z_0 = 50\,\Omega$, $C_{\text{p}} = 315\,\text{fF}$, $C_{\text{edge}} = 127\,\text{fF}$, $R_{xy} = 5000\,\Omega$ with $R = 80\,\Omega$ in the centre of an EMP resonance (star symbol) and $R = 350\,\Omega$ off resonance (square symbol). Note that the impedance matching network transforms $R_{xy} = 25\,\text{k}\Omega$ towards a few $\text{k}\Omega$, consistent with the value used in the model.

3.1.3 Discussion and Model

We account for the distinct features in our measurements, as well as the phenomena of forward and reverse circulation via a simple picture of a Fano-like resonance. Figure 3.5 illustrates the phenomenology of the quantum Hall circulator. Similar to the operation of a traditional ferrite device, we consider a resonator structure with two interfering paths, as shown in Fig. 3.5 (a). The arms of this interferometer comprise a direct path, supported by the parasitic (geometric) capacitance C_{p} between ports, and an indirect path C_{edge}, that capacitively couples ports via the plasmonic excitation of a quantum Hall edge. Key to the operation of our circulator is this 'slow light' response of the EMP modes, which, traveling at velocities 1000 times slower than the microwaves in the direct path, acquire the same phase over a length scale that is 1000 times shorter than the microwave wavelength in the dielectric. Considering these two-paths we note that there will be a frequency near the EMP resonance, at which the phase acquired via the edge leads to complete destructive interference with the signal propagating via the direct path. Given the chirality of the EMP, the condition for destructive interference will be dependent on the direction of microwave transmission, producing a non-reciprocal response between adjacent ports. Take for instance, the case where signals from port 3 to 1 propagate clockwise via the edge capacitance C_{edge} and acquire a phase of π-radians with respect to the signal traveling via C_{p}. Interference of these signals isolates port 1, whereas reverse transport, from port 1 back to port 3 must continue in a clockwise direction, past port 2 and acquire a constructive phase of 2π over twice the length. Circulation in the opposite direction to the chirality of the edge can now be understood for frequencies in which a π-phase is acquired in the forward direction, but 2π-phase in reverse.

We construct a simple model based on this Fano-like picture of interfering paths [231], by modifying the standard response of a three-terminal Carlin circulator to account for transport via a quantum Hall edge (see Appendix). This yields an expression for the non-reciprocal admittance matrix of the edge, Y_{edge}, as was done in Ref. [166]. Extending the model in Ref. [166], we add an additional admittance term Y_{p} to account for a direct parasitic coupling C_{p} between terminals (see Fig. 3.3 (c)). We further include the possibility of dissipation R, either directly in the chiral EMP mode or elsewhere in the circuit. Given an admittance of the edge-state Y_{edge}, the total admittance is then given by:

$$Y_{\mathrm{total}} = (I + RY_{\mathrm{edge}})^{-1} Y_{\mathrm{edge}} + Y_{\mathrm{p}} \tag{3.1}$$

where I is the identity matrix and where

$$Y_{\mathrm{p}} = \begin{pmatrix} 2c & -c & -c \\ -c & 2c & -c \\ -c & -c & 2c \end{pmatrix} \tag{3.2}$$

with $c = i\omega C_p$ and ω is the angular frequency of the microwaves. Microwave S-parameters can then be calculated as a function of ω for a given characteristic impedance of the input port (Z_0).

This model qualitatively captures the mechanism of circulation as arising from the interference of the parasitic and quantum Hall edge paths. Despite its simplicity, we find it also accounts for many of the features seen in the experimental data, including forward and reverse circulation that occurs near the fundamental and first harmonic of the EMP mode, as shown in Fig. 3.5 (c) and 3.5 (d). For features that occur at fields corresponding to integer filling, we find good agreement with the data for parameter values that are consistent with the device geometry and independent transport measurements (see Fig. 3.5 caption for details). At magnetic fields slightly away from integer filling, increasing R in the model yields similar results to the observed phenomena.

3.1.4 Tunable non-reciprocity

Finally, having outlined the mechanism leading to non-reciprocity in our device, we turn to describe a new mode that has no analog in the operation of classical circulators but may enable reconfigurable passive routing of microwave signals on-chip using gate voltages to modulate the velocity of EMPs. To demonstrate this mode we make use of an alternate device (Fig. 3.6 (a)) where, in comparison to the previous device, the port electrodes are positioned to now overlap the edge and a grounded contact is added to the centre of the disk. Sweeping the magnetic field, we find this device exhibits regions of strong non-reciprocity, as shown in Fig. 3.6 (b). Tunable non-reciprocity is demonstrated at fixed negative B-field by sweeping the dc voltage applied to the port-2 gate V_{g2}. This adjusts the response between the source and sink ports 3 and 1 respectively, which tunes the frequency of isolation $\Delta S = S_{13} - S_{23}$ as shown in 3.6 (c) and 3.6 (d). Applying a voltage to a gate hardly modifies the total path length of the EMP in this geometry, but can lead to a significant modulation in its velocity by varying the carrier density, electric field, or extent of screening at the disk boundary [247, 237]. As a function of V_{g2}, Fig. 3.6 (c) shows that the non-reciprocal response of the circulator initially drops from $\sim 1.2\,\mathrm{GHz}$ to $\sim 0.8\,\mathrm{GHz}$ as the gate voltage

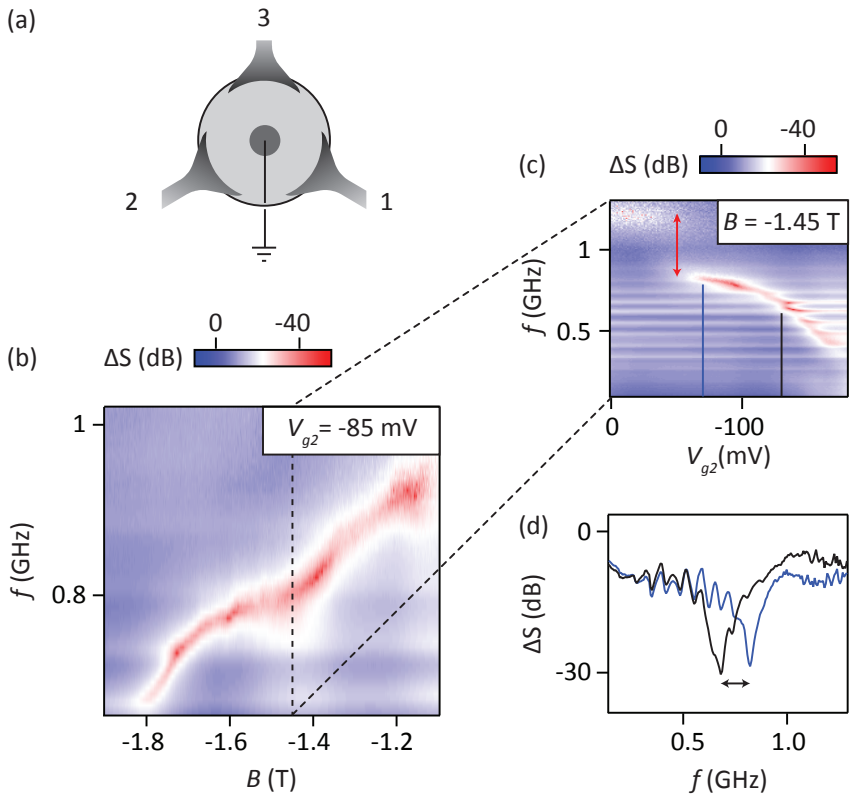

Figure 3.6: (a) Schematic of the gate-tunable device, with ports overlapping the edge of the disk and a grounded contact on the mesa. Bias tees enable the application of both rf and dc voltages. A large non-reciprocity $\Delta S = S_{13} - S_{23}$ is observed as a function of magnetic field, as shown in (b) for the case $V_{g2} = -85\,\mathrm{mV}$. At fixed negative magnetic field values, varying V_{g2} is found to affect the path from ports 3 to 1 and produces a significant modulation in the frequency response of the circulator (shown in (c) and (d)). This response is mirrored with a change of sign ΔS at positive magnetic field values, where the direction of EMP propagation is reversed and V_{g1} is varied (see Sec. C.5). Red arrow in (c) indicates a discontinuous jump in frequency as a gate voltage is first applied, while vertical lines show the positions of 1D cuts presented in (d). Horizontal striations in (c) are the result of small standing waves associated with an impedance mismatch between the amplifier and device.

is initially applied, followed by a more gradual decrease in the centre frequency as the gate is made increasingly negative. At present we do not understand why a modest gate voltage leads to a significant velocity modulation and therefore frequency response over such a large bandwidth (exceeding 1 GHz and many line-widths in this device). An alternate means of reconfiguring the device can be achieved by adjusting the external magnetic field (as shown in Sec. C.2). In this way the circulator can produce forward or reverse circulation, selectively routing microwave packets to alternate ports depending on the value of the magnetic field. For such an application, generating the magnetic field on-chip using a combination of micromagnets [248] and compact superconducting solenoids could be considered.

3.1.5 Conclusion

We have demonstrated a compact, on-chip microwave circulator based on the non-reciprocal response implicit to the quantum Hall effect. With better matching between the port impedance and impedance of the quantum Hall edge, these highly-compact devices can immediately compete with today's commercially available bulky circulators circulators for cryogenic applications. To this end, we draw attention to recent theoretical works [245, 246] that suggest new configurations for achieving "self-matching" of the circulator to the characteristic impedance of the ports. Beyond the simple circulator devices demonstrated here, we conclude by noting that an edge-state can be considered as a mesoscale delay-line with dynamic, and gate-tunable wideband response. Such a dependence opens the prospect of compact, parametric devices such as amplifiers, non-reciprocal filters and mixers based on the plasmonic and chiral response of the quantum Hall effect. Indeed, such modes can also likely be realized at zero magnetic field using topological insulator devices that exhibit the quantum anomalous Hall effect [249].

Acknowledgements

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3.2 Zero-Field Edge Plasmons in a Magnetic Topological Insulator

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Abstract

Incorporating ferromagnetic dopants into three-dimensional topological insulator thin films has recently led to the realisation of the quantum anomalous Hall effect. These materials are of great interest since they may support electrical currents that flow without resistance, even at zero magnetic field. To date, the quantum anomalous Hall effect has been investigated using low frequency transport measurements. However, transport results can be difficult to interpret due to the presence of parallel conductive paths, or because additional non-chiral edge channels may exist. Here, we move beyond transport measurements by probing the microwave response of a magnetised disk of $Cr-(Bi,Sb)_2Te_3$. We identify features associated with chiral edge plasmons, a signature that robust edge channels are intrinsic to this material system. Our results provide a measure of the velocity of edge excitations without contacting the sample, and pave the way for an on-chip circuit element of practical importance: the zero-field microwave circulator.

3.2.1 Introduction

It is now understood that ferromagnetism, by lifting spin degeneracy and breaking time reversal symmetry at zero magnetic field, can transform a topological insulator (TI) into a new phase of matter that hosts chiral edge states [250, 251, 252, 122, 253]. The signature of this phase is the quantum anomalous Hall effect (QAHE), in which the transverse conductance of a magnetised Hall bar remains quantised in units of the conductance quantum, even in the absence of an external magnetic field [116, 254]. Experimentally this has been demonstrated in $(Bi, Sb)_2Te_3$ using chromium [249, 255, 256] and vanadium [257] dopants. Given that bulk insulators and ferromagnets are commonplace at room temperature, there is optimism that the QAHE may not be limited to the cryogenic regimes of today's experiments. A room-temperature QAHE in which edge states propagate without dissipation could impact some of the challenges facing current-generation high speed integrated circuits.

The presence of robust edge states in these material systems opens up the prospect that they support plasmonic edge excitations, resonant drum-modes of the electron gas that are well-known in the context of the quantum Hall effect [109, 235, 258]. Beyond their fundamental interest, the velocity of edge plasmons excitations is typically reduced compared to the speed of light, making them ideal platforms for constructing on-chip delay networks, high-impedance transmission lines, and non-reciprocal devices such as gyrators and circulators needed for quantum information processing in present low temperature setups [166, 259, 245]. Recent theoretical work has also highlighted the potential of gapped Dirac materials to host chiral plasmons at optical frequencies, arising from the non-zero Bloch band Berry curvature [260, 261].

Here we investigate the zero-field plasmonic response of a magnetised, contactless disk of the ferromagnetic TI $Cr-(Bi, Sb)_2Te_3$. The fabrication of both Hall bars and resonant disk structures enables us to make a one-to-one comparison between transport data and the microwave excitation spectrum of the material. By implementing a three-port circulator configuration, we show that the low frequency plasmon response exhibits non-reciprocal behaviour, consistent with chiral edge plasmons. The existence of such plasmonic modes in the disk and their correspondence with a minimum in the longitudinal resistance of the Hall bar provide further convincing evidence that this system supports a robust edge state. Finally, we examine the dependence of circulation on excitation power and temperature, suggesting that microwave measurements can serve as a sensitive probe of the conditions at the edge.

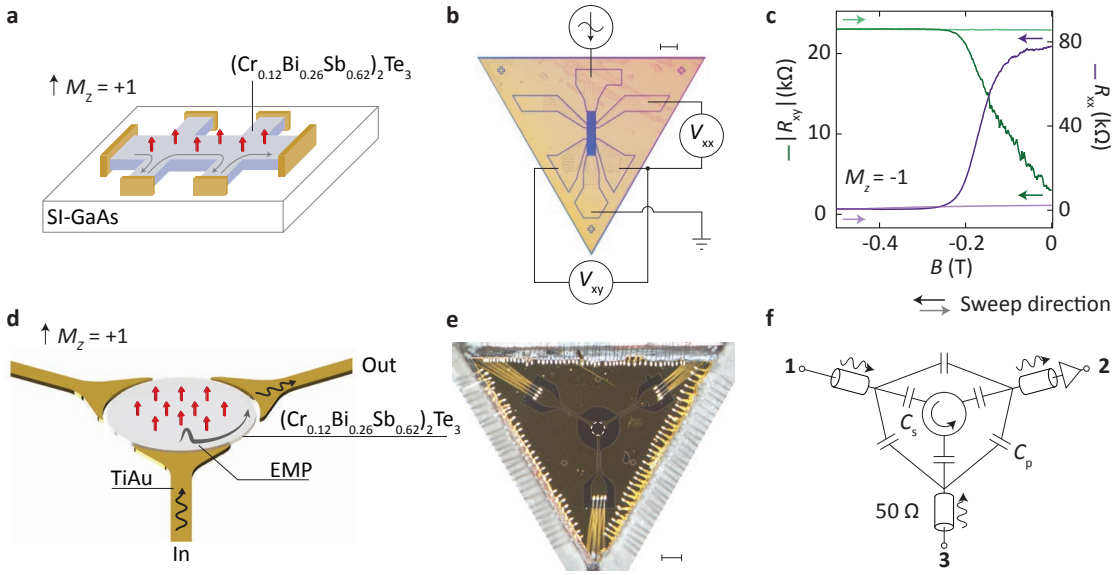

Figure 3.7: (a) Illustration of the quantum anomalous Hall effect in a three-dimensional topological insulator thin film with ferromagnetic dopants. (b) Photograph of a Hall bar fabricated on a device with seven quintuple layers of $((Cr_{0.12}Bi_{0.26}Sb_{0.62})_2Te_3$ grown epitaxially on a GaAs substrate. Scale bar is $100\,\mu\mathrm{m}$. Standard lock-in techniques are used to measure the transport properties of the material. (c) Transverse and longitudinal resistance (R_{xy}, green, and R_{xx}, purple) as the perpendicular magnetic field is swept out to $-0.5\,\mathrm{T}$ (dark coloured lines), and then back to zero field (light shaded lines). (d) Cartoon of a three-port circulator device with a magnetic topological insulator. (e) Photograph of the circulator device, scale bar is $500\,\mu\mathrm{m}$. (f) A circuit schematic for the experimental setup. The parasitic capacitances between port electrodes (C_p) and from the ports to the plasmonic modes (C_s) are indicated. Port 2 is connected to a low-noise cryo-amp operating at $4\,\mathrm{K}$, allowing measurement of S_{21} and S_{23} through a common output line.

3.2.2 Results

Device details

Turning to the experimental setup shown in Fig. 3.7, the magnetic three-dimensional (3D) TI used to make the circulator and corresponding Hall bar is seven quintuple layers of $(Cr_{0.12}Bi_{0.26}Sb_{0.62})_2Te_3$. The film is grown on a semi-insulating (111)B GaAs substrate by molecular beam epitaxy, then capped with alumina to protect the surface. To define the microwave circulator, we use photolithography to pattern a circular, 330 μm diameter mesa and etch away the remaining film via Ar ion milling. We next pattern capacitive contacts and a ground plane, depositing 120 nm Au by e-beam evaporation. The contacts are designed to be 20 μm away from the mesa edge.

Initial sample magnetisation

Starting at zero field, the transport data in Fig. 3.7(c) show the longitudinal and transverse resistances of the Hall bar, R_{xx} and R_{xy}, during the initial magnetisation sequence, sweeping the field from zero to $B = -0.5\,\mathrm{T}$ at the cryostat base temperature of $T = 20\,\mathrm{mK}$ (dark purple and green lines). As the field is applied for the first time we observe R_{xx} drop from $\sim 80\,\mathrm{k\Omega}$ to $\sim 500\,\Omega$ as R_{xy} increases towards h/e^2 (h is Planck's constant and e the electron charge). These resistance values are found to persist after waiting several hours at $-0.5\,\mathrm{T}$. The field is then swept back to $0\,\mathrm{T}$, with transport data in this direction shown as lightly-shaded lines in Fig. 3.7(c). Over this range, we observe that R_{xy} does not vary by more than 1%, while R_{xx} increases slowly to $2.3\,\mathrm{k\Omega}$ at $B = 0\,\mathrm{T}$. An accurate and precise measurement of R_{xy} requires accounting for possible geometric effects of the contacts and calibration using a known resistance standard, as was done in Ref. [262]. In the absence of these corrections, the measured resistance plateau value of $25\,750\,\Omega$ for this device is within the uncertainty expected for the quantum of resistance: $25\,813\,\Omega$ [249, 255, 256].

We compare these transport data with the microwave response of an etched TI disk on the same material, configured as a circulator as shown in Fig. 3.7(d-f). Similar designs comprising an rf excitation and detection port have been used to probe edge magnetoplasmons (EMPs) in the quantum Hall effect regime in GaAs semiconductors [241, 240, 259] and in graphene [238, 237, 239]. These EMP modes are charge density waves supported by edge channels at the boundary of the material. For traditional semiconductor samples, such as GaAs, the propagation velocity and therefore microwave frequency response of the EMP is set by the ratio of the electric and magnetic fields at the edge. In the case of ferromagnetic topological insulators, the existence of a robust edge is related to the electronic band

structure, and can persist in the absence of an external magnetic field.

In our setup, a 3-port design further allows the non-reciprocal character of the device to be probed by determining whether the signal traverses the TI disk via a left-handed or right-handed path [166, 259]. The experiment comprises S-parameter measurements in which the amount of microwave power transmitted from port 1 to port 2 (S_{21}), or port 3 to port 2 (S_{23}) is detected as a function of external magnetic field and magnetisation state ($M_z = M/|M| = \pm 1$) of the TI disk (see Fig. 3.8(a)). The two symmetrical paths, port 1 to 2 and port 3 to 2, are designed to be equivalent in the absence of chiral transport.

We note that for any measurement, microwave power can be coupled directly and reciprocally between the ports via the geometric (parasitic) capacitance that shunts the disk (C_p in Fig. 3.7(f)). In our sample geometry C_p is estimated to be in the vicinity of a few hundred femtofarads. The combination of a direct capacitive path in parallel with the conductive edge-channels in the disk creates an interferometer in which signals travel at the speed of light in the capacitive arm, and at a velocity in the other arm that is determined by the plasmonic response [259]. It is primarily the difference in velocities (and, to a lesser extent, path lengths) between the two paths of the interferometer that yields a phase offset between the two signals when they recombine at the receiving port. Further, the amplitude of the signals is set by the impedances of the two paths; if the edge plasmon resonator has a moderate Q-factor, these amplitudes can easily be made comparable by driving the circuit at a frequency slightly detuned from the resonant mode of the disk. Within this interference picture, the response of the circuit can be interpreted as a Fano resonance that depends on the length of path traveled by the edge plasmon, l or $2l$ depending on the excitation port and magnetisation direction [see Fig. 3.8(a)]. With port 2 always set to be the receiving port, transmitting power from port 1 or port 3 thus configures the edge length to be l or $2l$. The difference between the two paths' transmission, measured as $S_{21} - S_{23}$, determines the isolation or non-reciprocity of the circuit.

Microwave circulator response

We begin the presentation of the circulator data in a similar fashion to the transport measurements, starting at zero magnetic field and recording S_{21} and S_{23} as the external field is stepped out to $-0.5\,\mathrm{T}$. To enable a direct comparison between transport and the microwave response of the disk during the one-off magnetisation sequence, we acquire transport data as well as S_{21} and S_{23} at a fixed magnetic field before stepping the field (i.e., all data in Fig. 3.7(c) and Fig. 3.8 were obtained concurrently). All individual S_{21} and S_{23} data throughout the paper are normalised (denoted by Δ) by subtracting the initial frequency de-

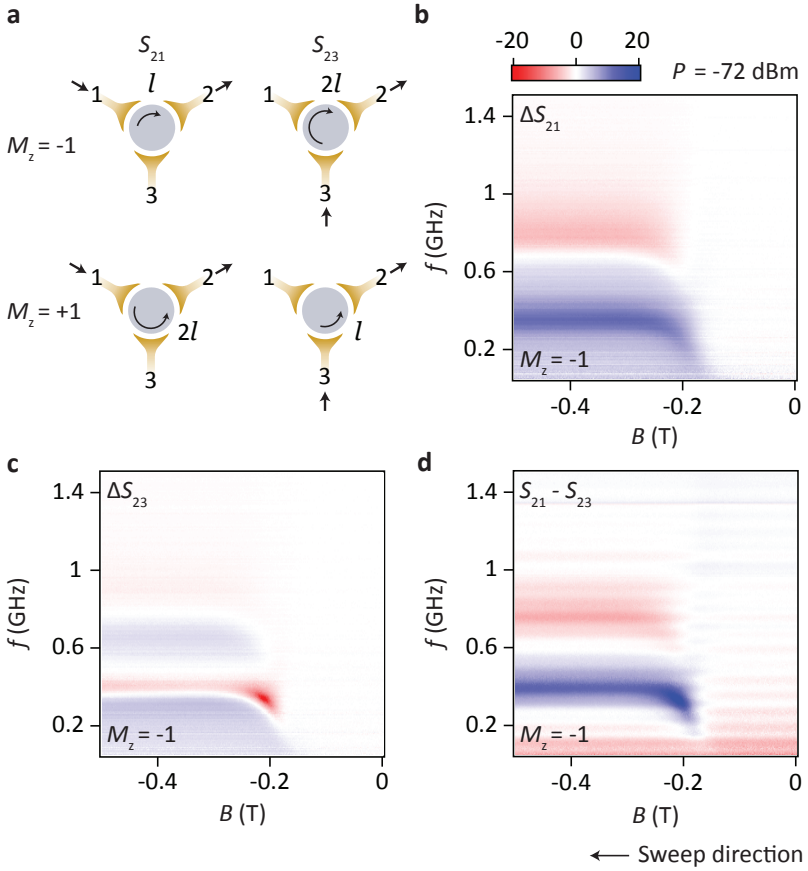

Figure 3.8: (a) Illustration of chiral edge transport in a circulator setup for different magnetisation and port configurations. Arc path lengths are denoted as l and $2l$. (b) and (c) show the microwave response of signals excited from ports 1 and 3 and amplified out of port 2, as the magnetic field is varied. These traces have been normalised to the reciprocal background prior to sample magnetisation, such that the colour bar represents ΔS in dB. In (d), the colour bar shows $S_{21} - S_{23}$ in dB, where the difference between the bare S-parameter traces is plotted without background normalisation. Past the coercive field of -0.16 T, strong non-reciprocity is observed at two distinct frequency bands, with opposite amplitudes.

pendence of the signal in logarithmic units (dB) in the unmagnetised state, $B = 0\,\mathrm{T}$ and $M_z = 0$, where the response is reciprocal. This calibration trace is taken at cryostat base temperature ($T \sim 20\,\mathrm{mK}$) and a port excitation power of $-72\,\mathrm{dBm}$. This normalisation alleviates frequency-dependent artefacts, for instance transmission oscillations due to line impedance mismatch that do not evolve with magnetic field (see Fig. D.1).

Forward transmission ΔS is shown in Figs. 3.8(b) and 3.8(c) as a function of frequency and magnetic field for the two paths S_{21} and S_{23}. As the sample begins to magnetise at the coercive field ($\sim -0.16\,\mathrm{T}$), we observe resonance-like dips and peaks in the frequency spectrum of the disk, evident as red and blue coloured horizontal bands appearing at the field strength where R_{xy} [Fig. 3.7(c)] approaches the resistance plateau h/e^2. This is the microwave signature of the QAHE. Compared with EMPs in 2 dimensional electron systems [259] where the frequency ω_{EMP} is proportional to $1/B$, in the TI we observe a flat frequency band as a function of magnetic field, centred at the fundamental mode of the edge plasmon, near 400 MHz. This is consistent with dc transport measurements of the Hall resistance which takes on a constant, quantised value after the sample is magnetised. Measuring the frequency at which these resonances occur in combination with the circumference of the TI disk gives a velocity at the fundamental mode of $\sim 4 \times 10^5\,\mathrm{m\,s^{-1}}$, similar to what is found in other structures comprising stacks of semiconductors [241, 240, 259].

The microwave response shows that the parameters S_{21} and S_{23} deviate from each other as the disk becomes magnetised. This is a result of the non-reciprocity of the system, evident in Fig. 3.8(d) where we have subtracted the bare S-parameters ($S_{21} - S_{23}$) from each other to show the difference between the two configurations of the circulator. Again, we interpret these measurements of S_{21} and S_{23} as characterising paths around the edge of the disk in the same (chiral) direction with arc length l and $2l$ [Fig. 3.8(a)]. Considering the measurement in Fig. 3.8(d), it is apparent that microwave power can both circulate near the fundamental edge plasmon frequency (blue frequency band) and counter circulate in an opposite direction near the first harmonic (red frequency band). This behaviour is also observed for GaAs devices in the quantum Hall regime [259] and is understood to arise from a Fano-like interference between the slow-velocity resonantly circulating edge mode and the parallel capacitive path [246]. We remark that the observation of circulation and counter-circulation is a further signature of the plasmonic response of the chiral edge state.

Sweeping the magnetic field

The quantum anomolous Hall effect is unique in that it supports a chiral edge state at zero applied field [262]. To examine the zero-field response of the magnetised TI system, we

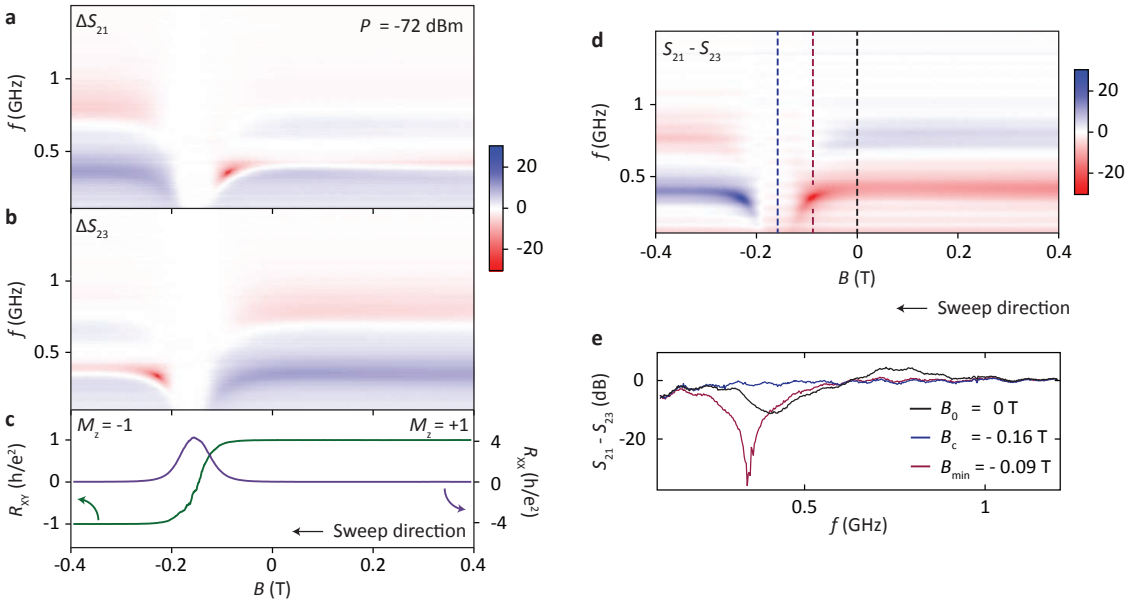

Figure 3.9: (a) and (b) Normalised ΔS_{21} and ΔS_{23} responses measured at the same time as transport data in (c). A pre-magnetisation frequency-dependent background has been subtracted from each of the traces in (a) and (b). The colour scale represents ΔS (dB). (c) Transverse (green) and longitudinal (purple) dc resistances measured on a Hall bar as the magnetisation direction is swept from positive to negative. Away from the coercive field, raw R_{xy} approaches the resistance quantum while R_{xx} measures $\sim 500\,\Omega$. In (d) we compare the difference between the bare S_{21} and S_{23} paths (indicated by the colour scale in dB), providing a measure of isolation in the system. (e) Line cuts through (d) at zero applied magnetic field (B_0, black line), the coercive field (B_c, blue) and at the point where a power minimum is observed ($B_{\min}$, mauve).

continue to take transport measurements on the Hall bar concurrent with S-parameter data on the circulator, as the system is swept from positive to negative field through zero, as shown in Figs. 3.9(a) and 3.9(b). The transport data in Fig. 3.9(c) show the familiar signature of the QAHE with R_{xx} peaking and R_{xy} switching sign at the coercive field indicated by the blue dashed line ($\sim -0.16\,\mathrm{T}$). At $B = 0\,\mathrm{T}$, the system remains magnetised with R_{xy} reaching a maximum value of 25.75 kΩ.

In comparison to the transport measurements, the microwave response of the TI reveals new information. The response of the disk for each of the signal configurations, characterised by ΔS_{21} in Fig. 3.9(a) and ΔS_{23} in Fig. 3.9(b), is strongly asymmetric about the coercive field. Symmetry is restored, however, if in addition to the sign of the magnetisation, the ports are also interchanged, so that the red band in ΔS_{21} on the left of the coercive field mirrors the red band in ΔS_{23} on the right, and vice versa for blue features. This strong non-reciprocity is most evident in the differential form of the data $S_{21} - S_{23}$, as shown in Fig. 3.9(d). At zero field the circulator continues to exhibit non-reciprocity $\sim 10\,\mathrm{dB}$ [Fig. 3.9(e)]. Intriguingly, the device is maximally non-reciprocal at a field approaching the coercive field, producing a 'hot-spot' feature in the S-parameter response [mauve dashed-line Fig. 3.9(d)]. As described below, we suggest these features are linked to enhanced dissipation.

Power and temperature dependence

Finally, we investigate the temperature and microwave power dependence of the edge plasmon spectra in an effort to better understand the details of the zero-field edge state. At $B = 0$ and with the TI magnetised ($M_z = -1$), ΔS_{21} and ΔS_{23} are measured as a function of applied microwave power P, as shown in Figs. 3.10(a) and 3.10(b). In addition to the usual non-reciprocity at constant power, we observe an evolution in the non-reciprocal features with increasing P that is dependent on the length of the edge segment. While the response of ΔS_{21} (characterised by arc length l) begins to fade out at high powers, the amplitude of ΔS_{23} ($2l$) changes sign near the fundamental frequency and exhibits a pronounced minimum or hot-spot near $P = -60\,\mathrm{dBm}$. Interchanging the ports and repeating the measurement at $M_z = +1$ and $B = 0\,\mathrm{T}$ produces similar features in accordance with a reversal of chirality (see Fig. D.2). Mirroring the dependence with power, increasing the cryostat temperature also produces a change of sign relative to the pre-magnetised state for the longer edge path ($2l$): raising T as in Fig. 3.10(c) and 3.10(d) leads to ΔS_{21} becoming gradually washed out, while ΔS_{23} produces a hot-spot around $T = 85\,\mathrm{mK}$. This effect is further illustrated in Fig. 3.10, where 1D cuts at constant power 3.10(e) or temper-

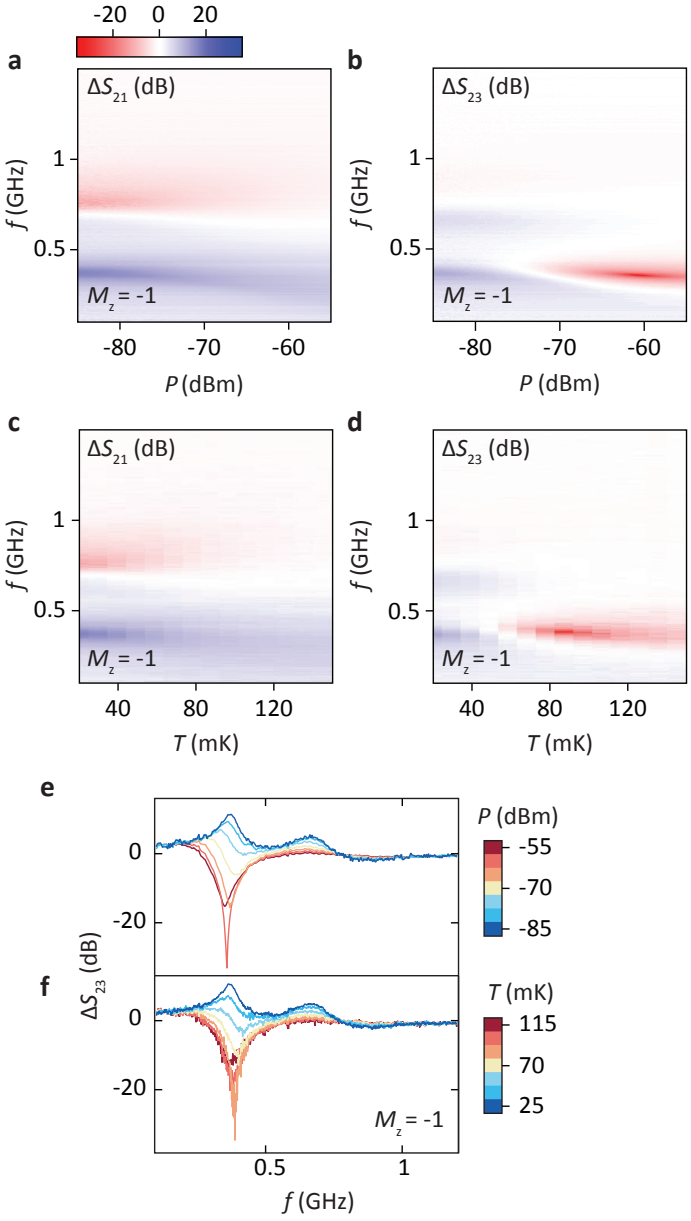

Figure 3.10: (a) and (b) Frequency response ΔS_{21} and ΔS_{23} with increasing microwave power applied to the excitation port. For these measurements $T \sim 20\,\mathrm{mK}$. In (c) and (d) the dependence of ΔS_{21} and ΔS_{23} is measured as a function of cryostat temperature while the applied port power is kept low at $-87\,\mathrm{dBm}$. In (a-f) all data are taken at zero applied magnetic field after the sample has been magnetised with $M_z = -1$. Akin to Figures 3.8 & 3.9, the same pre-magnetisation background taken at constant power and cryostat base temperature is subtracted from each of the 2D plots. The colour scale represents $\Delta S\,(\mathrm{dB})$. (e) and (f) 1D cuts through the colour plots of ΔS_{23} in (b) and (d). The colour bar in (e) shows power (dB), while the colour bar (f) indicated temperature (mK).

ature 3.10(f) are shown for ΔS_{23}.

3.2.3 Discussion

So-called hot-spots — characterised by a strong decrease in the microwave power transmitted between ports — occur at particular magnetic fields, powers, or temperatures. Appealing to the phenomenology of the interferometer pictured in Fig. 3.7(f), we note that the direction of power transmission between ports, either circulation or counter-circulation, is set by the relative phase and amplitude of the signals in the edge-state arm compared to the direct capacitive arm of the interferometer. In general, this picture accounts for the constructive interference of signals for the shorter edge path (l) and destructive interference for the longer ($2l$), when driving near resonance of the edge plasmon fundamental mode.

Extending this picture to include dissipation, we suggest that losses in either arm of the interferometer can adjust the relative amplitudes. As noted above, the relative phase of the two paths is naturally tuned by π upon crossing the edge plasmon resonance. At a frequency where the relative phase is π we might expect a sign change in the relevant S parameter response. In this way the hot-spots can be understood as regions where almost perfect cancellation between the two arms occurs. The appearance of dissipation in either path with increasing temperature, microwave power, or near the coercive field is perhaps not unexpected. Accounting for the microscopic mechanisms underlying such dissipation remains an open challenge [263, 264, 262, 265, 266, 267, 268], given that all measurements are well below both the Curie temperature of these ferromagnetic TIs (of order 10 K to 20 K) and the energy scale of the exchange gap as measured by ARPES (of order 10 meV). We note that the hot-spot onset temperature of 85 mK is consistent with experimentally determined activation gaps on similar growths [262], although we cannot rule out the possibility of parallel or counter-propagating paths.

3.2.4 Conclusion

To conclude, we have probed the plasmonic edge spectrum of a magnetic topological insulator, comparing its microwave response to transport data. The measurement setup can be understood as an interferometer with the disk of TI in one arm of the interferometer and a parasitic capacitance in the other. Within this picture, the response of the system exhibits resonances that can be explained by accounting for the slow velocity of edge plasmons as they traverse an arc-length of the TI disk's edge rather than the bulk. In addition to the device examined, we have studied a second circulator, fabricated from a separately-grown

wafer, and found it to exhibit strikingly similar behaviour in all aspects (see Fig D.3). We suggest that this similarity between devices is related to the robust properties of the edge state, set by the non-trivial topology of the material system rather than, for instance, the specific configuration of microscopic disorder. Taken together, our microwave measurements provide strong evidence that this material system indeed supports robust, chiral edge states at zero magnetic field, opening the prospect of compact microwave components based on magnetic topological insulators.

Acknowledgements

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Chapter 4

Spin Qubits and Readout

Up to this point, the results of my thesis have been focused on the architecture and instrumentation that surrounds a quantum computer. We switch tack at this point to focus on the bottom of the quantum computing stack; on the design of qubits, in particular the design of spin qubits in GaAs. Although, as we discussed in Sec. 1.2.3, there have been many successful attempts at forming spin qubits, one of the fundamental challenges facing all of the qubit designs in semiconductors is achieving strong two-qubit interactions. In the short range, direct exchange and capacitive coupling have generated two qubit fidelities that exceed 98% [91], however as we discussed in Chapter 2, a scalable qubit architecture will likely require both long-range and intermediate-range couplers in order to be feasible. The designs of progressively larger grids of quantum dots poses an additional challenge for the initialization of qubits located in the central regions of an array. Typically, initialization of a qubit is performed by loading a known spin state from proximal reservoirs [206], however for large arrays of quantum dots, such an approach is infeasible. Several recent papers suggest progressive loading of electrons from the center out [19, 54], however such schemes require a complete reset of the entire set of qubits. The first part of this chapter, Sec. 4.1, explores an architecture that addresses the issue of initialization and of intermediate-range coupling between singlet-triplet qubits.

On top of the coupling challenge, conventional charge-based readout techniques for spin qubits require bulky, proximal charge sensors, an approach which carries inherent challenges for a 2D qubit layout. Alternative approaches to readout based on dispersive gate sensing [157], while having now demonstrated single-shot readout [159], still achieve only 73% readout fidelity, well below the 99.86% level achieved using charge sensing [269, 270]. Understanding the limits of gate-based readout, including understanding the sources of anomalous error signals, will be crucial to utilizing gate-based sensors for scalable quantum

computers. This is the key problem we explore in the second part of this chapter, Sec. 4.2. I will also mention that the results of that chapter point towards a potential source of charge noise in semiconductor-based qubits, although the degree to which they might be eliminated by induced-electron device structures remains an open question.

4.1 Device Architecture for Coupling Spin Qubits Via an Intermediate Quantum State

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Abstract

We demonstrate a scalable device architecture that facilitates indirect exchange between singlet-triplet spin qubits, mediated by an intermediate quantum state. The device comprises five quantum dots, which can be independently loaded and unloaded via tunnelling to adjacent reservoirs, avoiding charge latch-up common in linear dot arrays. In a step towards realizing two-qubit entanglement based on indirect exchange, the architecture permits precise control over tunnel rates between the singlet-triplet qubits and the intermediate state. We show that by separating qubits by $\sim 1\,\mu$m, the residual capacitive coupling between them is reduced to $\sim 7\,\mu$eV.

4.1.1 Introduction

Entangling qubits by conditioning the state of one qubit on the state of another is a central requirement of universal quantum computing [271, 40]. Ideally, two-qubit interactions should be strong, such that entangling gates are fast with respect to single-qubit coherence times, and controllable, to prevent two-qubit interactions from interfering with single-qubit operations. Direct exchange coupling between neighbouring spins offers a straightforward means of realising fast two-qubit gates [272, 206, 273, 274], however such approaches are challenging since qubits must be positioned very close to each other [275] and operated in a way that avoids leakage from the logical qubit space [276, 277]. An alternative approach is to use the direct capacitive coupling between spin-dependent charge dipoles [183, 278, 279], although, at present, this capacitive interaction is relatively weak in comparison with the decohering charge noise of the qubit environment.

The need to overcome these challenges has created significant interest in alternative approaches to entangling gates with spin qubits. Proposals include the use of floating metallic structures [280], ferromagnets [281], cavity-mediated interactions [282, 61, 283], crossed Andreev reflection in superconductors [284], surface acoustic waves [285, 286, 287] and quantum Hall resonators [288, 289]. With many of these schemes, a major driver is the desire to separate qubits, thereby overcoming gate-crowding and unwanted single-qubit crosstalk whilst maintaining control over two-qubit interactions.

Here we demonstrate a device architecture that facilitates indirect exchange coupling between two spatially separated singlet-triplet qubits formed in double quantum dots (DQDs). Coupling is mediated by a multielectron quantum dot acting as a noncomputational, intermediate quantum state (IQS) [290, 291, 292, 275] as shown in Fig. 4.1 (a). Overcoming the challenge of loading and unloading electrons in linear arrays [293], we position accumulation gates over the tunnel barriers to the IQS, allowing transfer of electrons to and from the IQS independently of adjacent qubits, without charge latching. This architecture also enables qubit interactions to be controlled, either by the opening and closing of tunnel barriers to the IQS or by modulation of its chemical potential.

Mechanisms for coupling spin qubits via an IQS include direct exchange [275, 294], superexchange [295, 296], virtual population [297, 292] and the Ruderman-Kittel-Kasuya-Yosida (RKKY) interaction [294]. Regardless of the specific coupling mechanism, a key requirement is the independent loading of qubits and precise control over the tunnel rates between the IQS and adjacent quantum dots. In the present work our focus is coupling two-electron singlet-triplet qubits, although we note that our device can also be configured to couple single spins.

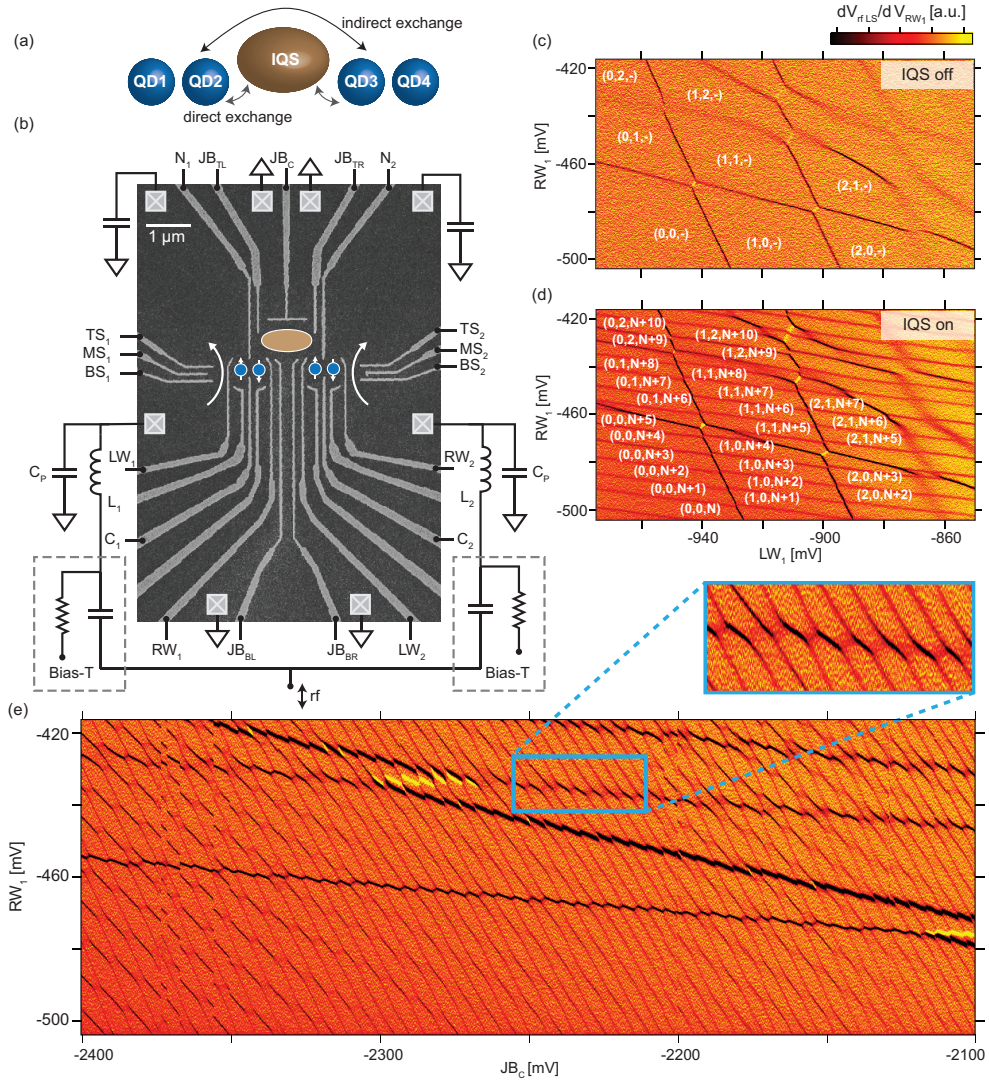

Figure 4.1: (a) Cartoon of our device architecture for coupling singlet-triplet qubits via an intermediate quantum state. (b) Electron micrograph and circuit schematic of the double quantum dots (blue circles) coupled by an intermediate quantum state (brown 'jellybean' ellipsoid). Crosses indicate Ohmic contacts. Inductors (L_1 and L_2), in resonance with the parasitic capacitance (C_p), form tank circuits for impedance matching. (c) Charge stability diagram measured with the left sensor as a function of the gates on the left double dot, and without the presence of the dot associated with the IQS, and (d) with the IQS configured with use of gates JB_C, JB_{BL}, JB_{BR} and N_2. Labels indicate the charge states (see the text). (e) The occupation of the intermediate quantum state can be controlled via JB_C. Transitions associated with the left double dot are seen as the two darker transitions with the shallowest slope. The inset shows transitions between QD2 and the IQS exhibit a curvature at their triple points, characteristic of level repulsion.

4.1.2 Methods

The DQDs and IQS are formed in a two dimensional electron gas located 91 nm below the surface of a GaAs/(Al,Ga)As heterostructure (with a density of 1.5×10^{11} cm^{-2}, and a mobility of 2.4×10^{6} cm$^2/(\mathrm{V\,s})$). Hafnium oxide, deposited using atomic layer deposition, separates TiAu gates from the heterostructure and enables positive voltages to be applied without gate leakage. Experiments are performed in a dilution refrigerator at a base temperature of 20 mK, with an electron temperature $T_e \sim 90$ mK. All data presented are taken in the presence of an applied in-plane magnetic field of $B = 100$ mT. A scanning electron micrograph of the device is shown in Fig. 4.1 (b). To define the DQDs [shaded blue in Fig. 4.1 (b)] we use a well-established gate configuration that is known to produce configurable qubits in isolation [143, 298]. This gate configuration allows each double dot to be tuned independently before coupling via the IQS.

The IQS is a large, multielectron quantum dot, configured with use of both depletion gates (N_1, N_2, JB_C, JB_{BL}, JB_{BR}), and accumulation gates (JB_{TL} and JB_{TR}). Positive voltages applied to the accumulation gates control the tunnel barriers between the leads and the IQS and ensure that coupling of the JB_C gate to the IQS-DQD tunnel barriers can be compensated, such that the barriers remain sufficiently transparent. Readout is performed via rf reflectometry [154], with use of an rf quantum point contact (rf-QPC) to sense the left DQD and an rf-sensing dot (rf-SET) to sense the right DQD with kilohertz bandwidths. The demodulated reflectometry signal, V_{rf}, is proportional to the conductance of the sensors, determined by the charge configuration of the multidot system.

4.1.3 Results and Discussion

Charge stability diagrams

We first independently tune both the left DQD and the right DQD into the single-electron regime, obtaining typical charge stability diagrams, such as that shown in Fig. 4.1 (c) for the left DQD, where the notation (n, m, k) refers to the number of electrons in each triplet-dot system, with k or n indicating the number in the IQS when referring to the left or right DQD respectively. We next bring up the IQS, and configure it in a regime where there is tunnelling into both the IQS and the DQDs. This is straightforward since both charge sensors, positioned at the ends of the array, are sensitive to charge transitions of the IQS as well as their proximal DQD, as seen in Fig. 4.1 (d) for the left sensor. Here, charge transitions of the IQS can be seen overlaying the familiar honeycomb charge stability diagram of the DQD. The presence of the IQS, when configured appropriately with accumulation

gates, hardly shifts the gate voltages needed to define the left DQD. Furthermore, the number of electrons in the IQS can be independently controlled with gate JB_C, as shown in Fig. 4.1 (e), which shows a plot of the left sensor signal as a function of the voltage applied to JB_C.

Close inspection of Fig. 4.1 (e) shows several near-horizontal lines that correspond to charge transitions on the left DQD, whereas the more vertical transitions correspond to the IQS. The IQS occupancy is tunable over a range of at least 50 electrons, and for certain values of JB_C, the transitions alternate between the signatures of a single dot and a double dot. In what follows we operate the IQS as a single quantum dot, but note the potential for more-complicated interactions when the IQS itself comprises a tunnel-coupled double dot.

The data in Figs. 4.1 (d) and (e) indicate that the charge transitions in the left DQD undergo level repulsion with the states of the IQS, although it is not clear from these data whether this interaction is simply capacitive or also involves tunnel coupling (i.e., quantum fluctuations) between the states of the DQD and the IQS, which is needed for exchange coupling of the spin states [299]. The picture is made more difficult to interpret since tunnel transitions between any of the dots and the leads will also modify the energy levels of the system. Separation of capacitive and tunnel contributions is possible by extraction of the width of the transitions, as well as by observation of how occupancy of the dots depends on the sweep direction of the gates that control the chemical potential.

Tunnel coupling between the IQS and DQDs

We first examine tunnelling between the right DQD and the IQS in the regime where direct tunnelling between the inner dot (QD3) and leads is suppressed. When the potential of QD3 is rapidly increased by our sweeping the gate at a rate of approximately 1 mV ms^{-1}, it is energetically unfavorable for electrons on QD3 to tunnel to the reservoirs, except by inelastic or co-tunnelling processes as shown in diagram (i) in Fig. 4.2 (b). When the rates of co-tunnelling and inelastic processes are low compared to the gate sweep rate, tunnelling out to the lead will be suppressed for QD3 until the effective triple dot is configured such that the IQS excited state is accessible, as indicated in (ii) in Fig. 4.2 (b). Similarly, depending on whether the energy level of the inner dot is increasing or decreasing, the conditions for loading or unloading electrons via the IQS will differ, as shown in diagrams (iii) and (iv) of Fig. 4.2 (b). We look for the signatures of these conditions in the charge stability diagrams for both the left DQD and the right DQD, making use of the corresponding left and right charge sensors.

We acquire the stability diagrams for both the left DQD and the right DQD are ac-

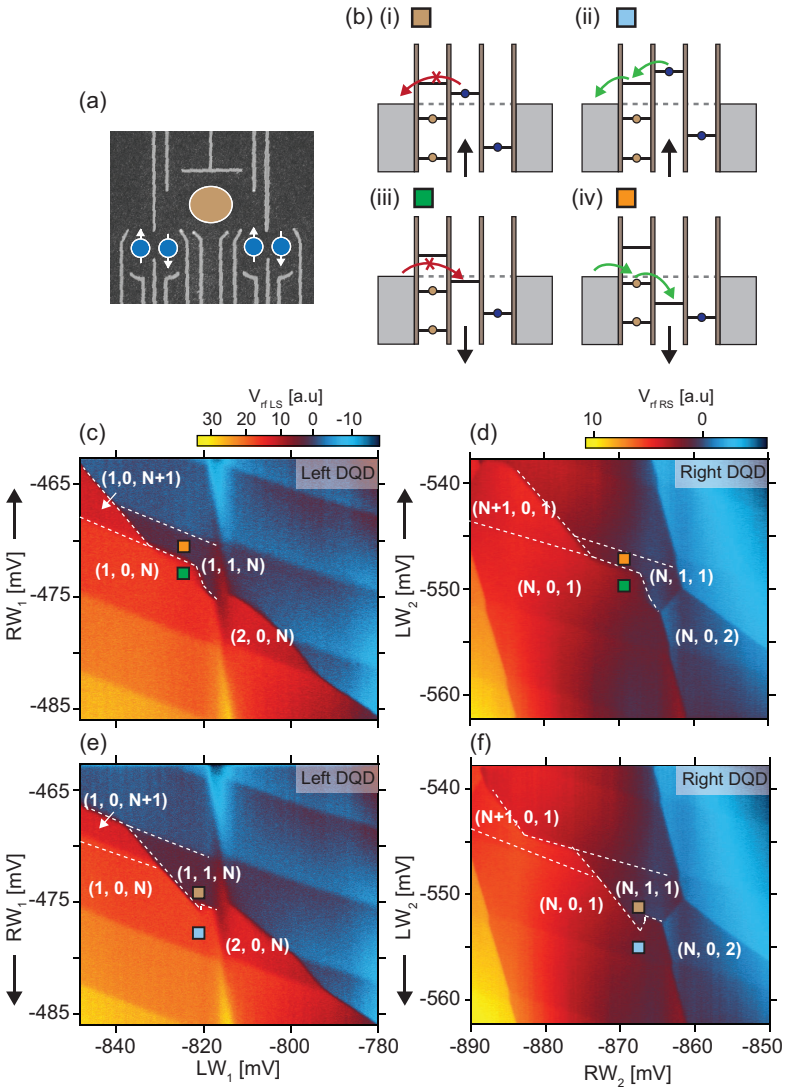

Figure 4.2: (a) Micrograph of the device is displayed for reference. (b) Chemical potentials of the multidot system when electrons can tunnel directly from the IQS or DQD to a reservoir. (i)-(iv) In the case that the IQS and DQD are tunnel coupled and the barriers are sufficiently opaque, the inner dots (QD2 and QD3) unload via the IQS or outer dot. When the potential of an inner dot is rapidly swept (approximately $1\,\mathrm{mV\,ms^{-1}}$), its charge state depends on whether it is being loaded or unloaded. Unloading [(i) and (ii)] is facilitated by tunnelling through excited or empty states on the IQS, while loading [(iii) and (vi)] can occur once the inner dot potential falls below the IQS potential. (c), (e) Charge stability diagram for the left double dot (sensed with the left sensor), as RW_1 is swept from more (less) to less (more) negative. Coloured boxes correspond to the potential configurations in (b). (d), (f) Charge stability diagram for the right double dot (sensed with the right sensor), with LW_2 swept from more (less) to less (more) negative.

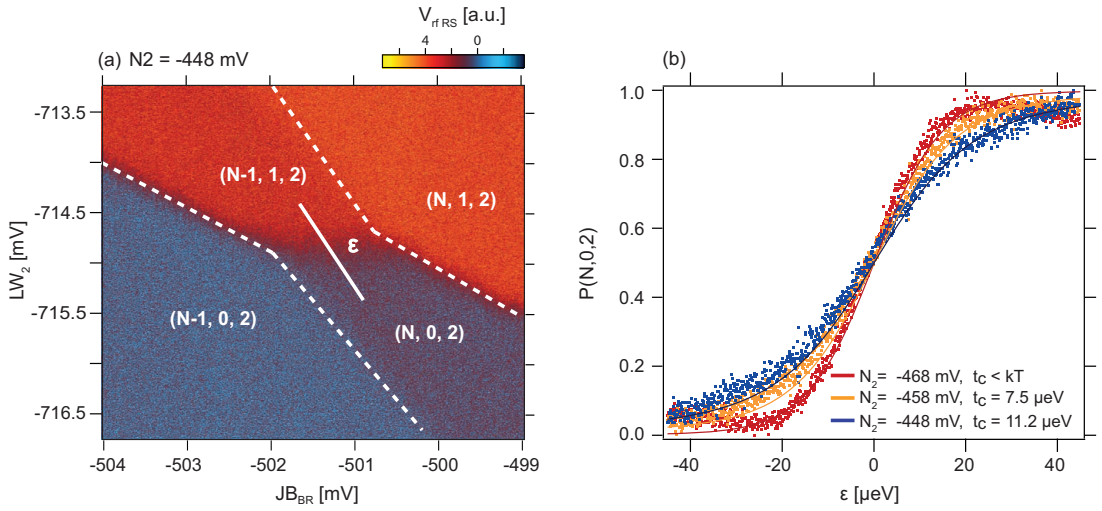

Figure 4.3: (a) Charge stability diagram of the IQS and right DQD detected with the right charge sensor. (b) Line cuts taken through the interdot transition along the axis of detuning ϵ for different voltages applied to gate N_2. Tunnel couplings t_c are extracted.

quired using fast charge sensing by rapidly sweeping the gate that corresponds to the vertical axis of each data set from negative to positive [Figs. 4.2 (c) and (d)] and from positive to negative [Figs. 4.2 (e) and (f)]. The gate indicated on the vertical axis couples most strongly to the respective inner dot. Comparing Figs. 4.2 (c) and (d) for the left DQD and the right DQD respectively, we see that IQS transitions modify the bare DQD charge stability diagram such that it resembles the diagram expected for a triple-dot system [300]. Furthermore, we find that this triple-dot pattern now appears different for opposite directions of the gate sweep. This directional dependence arises when we consider the different gate-bias conditions under which the dots will be in a stable occupancy configuration, loading and unloading via tunnelling through states in the IQS [as indicated in Fig. 4.2 (b)].

Tunable coupling the between IQS and theright DQD

Having demonstrated that the system can be configured such that tunnelling occurs between the DQDs and the IQS, we now turn to controlling and estimating the strength of this tunnel rate, which determines the magnitude of qubit-qubit coupling [292, 295, 275]. The tunnelling rates between the inner dots and the IQS can be tuned by modifying local gate voltages. A transition from the $(N, 0, 2)$ state to the $(N-1, 1, 2)$ state is shown in the enlargement of the charge stability diagram in Fig. 4.3 (a), where the diagonal line indicates the axis of detuning ϵ between the two states. Plotting the normalized probability P of occupying the $(N, 0, 2)$ state as a function of detuning, we see from Fig. 4.3 (b) how the width

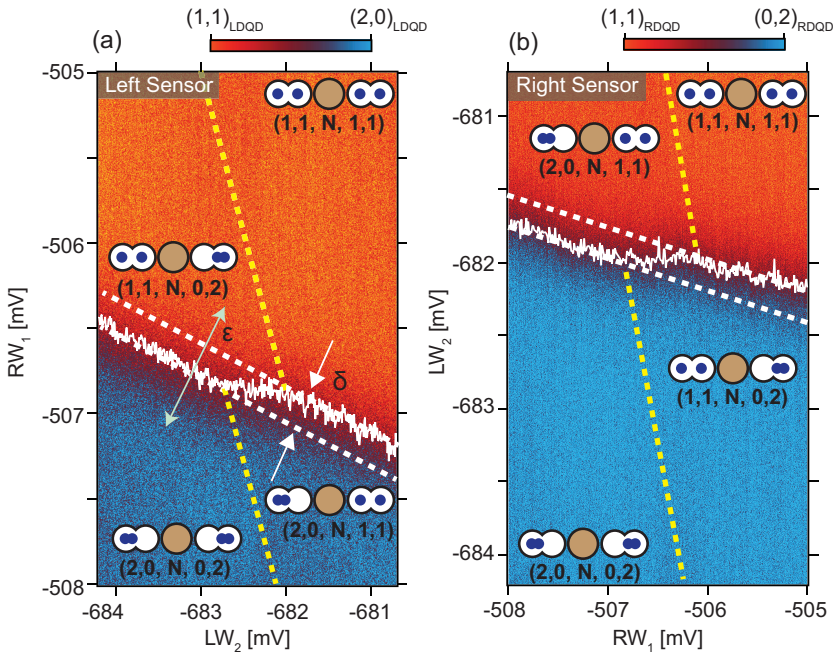

Figure 4.4: (a) Transition of the target DQD, from $(1,1)$ (red) to $(0,2)$ (blue) as the control DQD is configured to switch state from (1,1) to (2,0). DQD configuration detected with the left sensor. The white line corresponds to the position, in gate space, where $\epsilon = 0$. Dashed yellow and white lines are guides for the eye: dashed white lines indicate the continuation of $\epsilon = 0$ in the absence of a second DQD, while dashed yellow lines indicate the approximate $\epsilon = 0$ coordinates on the opposite double dot. (b) Same as (a) but on the right DQD, measured with the right charge sensor. Using lever arms from both double dots, and appropriate projections, we estimate an electrostatic coupling energy of $6.0\,\mu\text{eV}$ on the left DQD, and $7.7\,\mu\text{eV}$ on the right DQD.

of the transition is controllable by our altering the bias applied to gate N_2. Fitting to these transitions [55], we extract the tunnel couplings between the IQS and the DQD, which range from 2.7 GHz (11.2 μeV) to less than kT with a 20 mV change in gate N_2[1]. These values are consistent with previous demonstrations of interdot tunnel couplings [295, 206] and imply that for direct-exchange-coupled spin qubits, a $\sqrt{\text{SWAP}}$ gate can be produced in a few tens of picoseconds. For more-complex indirect-exchange mechanisms, for instance, those involving superexchange [292, 295], this two-qubit gate time is likely to be slower (on the order of nanoseconds) but still significantly faster than spin dephasing.

[1]Some uncertainty in our estimate of the lever-arm is likely since we have assumed that it is comparable to lever-arm extracted for the right DQD. This is a reasonable assumption given the similar sizes and geometries of the dots.

Residual Capacitance between DQDs

For singlet-triplet qubits coupled via direct exchange, the requirement of tunnel coupling necessitates that quantum dots are in close proximity, where their charge dipoles will also couple via the bare capacitive interaction. In our indirect-exchange architecture, the use of the IQS allows the qubits to be separated by a distance that diminishes their electrostatic coupling such that two-qubit interactions can be effectively switched off via gate control of the IQS. To further evaluate our architecture, we measure the residual capacitive coupling when the DQDs are separated by approximately 1 μm, 10 times the typical distance of qubits engineered with intentionally strong capacitive coupling [278, 183]. Tuning the IQS into the Coulomb blockade regime, we configure both DQDs as singlet-triplet qubits operating on the two-electron system that spans the (0,2) and (1,1) charge states. To measure the capacitive coupling, Figs. 4.4 (a) and 4(b) show the response of each sensor, with the colour scale normalised to configurations of the two-electron charge states of each DQD.

The transition, from orange to blue in Fig. 4.4 (a), corresponds to the left target DQD switching its charge state from (1,1) to (2,0) with detuning ϵ, as measured by the left sensor. Figure 4.4 (b) shows the equivalent transition for the right DQD, from (1,1) to (0,2), now measured with the right sensor. To determine the capacitive coupling between the two dipoles, we look for a shift in the position of this transition δ on the left target DQD, as the right control DQD switches between its two charge states. Fitting of the position of the transitions with gate voltage (the gate values for which $\epsilon = 0$) is shown in white in the stability diagrams in Figs. 4.4 (a) and (b) [55]. Finally, the shift in position of the target transition δ can be converted to an effective electrostatic energy with use of the lever arms separately extracted from bias-spectroscopy measurements of the DQDs. Using this approach we measure a differential cross-capacitive interaction of 1.5 GHz (6.0 μeV) when the left DQD is configured as the target and 1.9 GHz (7.7 μeV) when the target is the right DQD. These energies can be compared with measurements reported in ref. [278], where a 100 nm DQD separation yields an interaction energy of approximately 25 μeV. We presume that in our device the presence of the IQS, populated with some tens of electrons, accounts for the enhanced capacitive coupling over what may be expected from consideration of the linear scaling of the bare-device geometry.

4.1.4 Summary

In summary, we present a device architecture that enables independent loading and unloading of electrons across five quantum dots using both depletion and accumulation gates to

control tunnel barriers. Fast charge sensors, positioned at the ends of the device structure, are shown to be sufficiently sensitive to allow tuning of both DQDs and the quantum dot that is host to the intermediate quantum state. The platform alleviates the burden of spatial crowding suffered by qubits that are coupled via direct exchange, and opens a means of scaling spin qubits beyond linear arrays.

Acknowledgements

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4.2 Gate-Sensing Charge Pockets in the Semiconductor-Qubit Environment

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Abstract

Dispersive gate sensing (DGS) uses radio frequency (rf) reflectometry to locally probe the quantum capacitance of a gate electrode. Applying DGS to heterostructure-based qubit devices, we report the repeated observation of anomalous signals that we attribute to pockets of charge in the potential-landscape likely under, and surrounding, the surface gates that define quantum dot qubits. Interestingly, these charge pockets appear to evade detection with conventional charge sensors but manifest strongly in the response of the gate sensor. Configuring a quantum point contact (QPC) as a highly-localised heat source, we show how these charge pockets likely form close to the end of the gate electrodes, in close proximity to gate-defined qubits. The presence of uncontrolled charge may lead to offsets in gate-voltage, and further contribute to charge-noise that produces decoherence in semiconductor qubits.

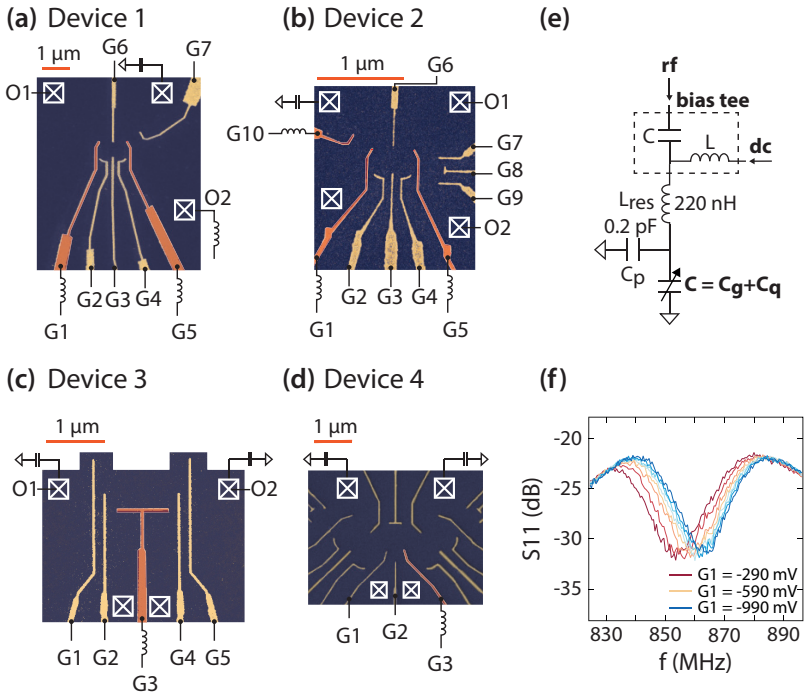

Figure 4.5: (a-d) False-coloured micrographs of the four devices examined. Each device is fabricated from a unique GaAs/(Al,Ga)As heterostructure with mobilities of 3.9×10^6, 0.44×10^6, 2.4×10^6 and 4.8×10^6 cm^2 V^{-1} s^{-1}, densities 1.2×10^{11}, 2.4×10^{11}, 1.5×10^{11} and 1.3×10^{11} cm^{-2}, and 2DEG depths of 91 nm, 110 nm, 91 nm and 91 nm for device 1, 2, 3, and 4, respectively. White crossed boxes indicate ohmic contacts. Resonators, required for dispersive gate sensing, are indicated by the inductor symbols, with equivalent-circuit model shown in (e), including the parasitic capacitance C_p and the classical gate capacitance C_g. (f) The reflection coefficient (S11) as a function of frequency of a typical resonator (attached to gate G1 of device 1) as the gate is biased from -290 mV to -990 mV.

4.2.1 Introduction

The on-chip resources needed to read out semiconductor qubits can be significantly lowered by using a single compact gate electrode as a detector [157]. Configured to probe the local density of states by sensing the charge response to a small ac voltage, gate-based read-out has recently been shown to have sufficient sensitivity to enable the state of a qubit to be determined in a single shot [159]. Despite recent advances [158, 301, 302], it is not obvious that gate read-out can be deployed in all sensing regimes where single-electron transistors (SETs) or quantum point contacts (QPCs) have been used to detect the charge configuration of a nanoscale device [154, 303]. In particular, since dispersive gate sensing (DGS) effectively detects a change in the local capacitance, its signal and noise spectrum can be different from those of conventional sensors that detect the total charge.

Here, we use DGS to investigate charge dynamics in the two-dimensional (2D) potential landscape of gate-defined qubit devices constructed from high-mobility heterostructure

materials. Over the course of examining many different devices, we routinely observe reproducible but anomalous signals in the response of gate sensors as a function of the gate bias. Although not fully understood, we present data consistent with the interpretation that these anomalous signals originate from weakly bound pockets of charge that remain when the electron channel under or near a gate is only partially depleted. In this interpretation, large shallow quantum dots that are inadvertently trapped by inhomogeneities in the potential at low density [304] undergo Coulomb blockade at low temperature. The rf voltage associated with the DGS technique can then induce tunnelling between trapped pockets of charge, leading to anomalous signals in the capacitive response of a gate. Surprisingly, these signals do not correlate with standard charge-detection measurements based on a QPC charge detector [305]. In what follows we propose an explanation to account for this discrepancy between DGS and charge sensing and present further evidence that these charge pockets are located reasonably close to the end of the gate electrodes.

The presence of such charge pockets has long been known, although directly probing them usually requires methods such as scanned-probe techniques [306] that can, for instance, image electron-hole puddles [307] at the surface of materials such as graphene [308]. Puddles of charge have also been detected by measuring velocity shifts in the propagation of surface acoustic waves in low-density 2D systems [309] or via the use of capacitive bridges [310] and local electrometers [311]. Our use of gate sensing to probe the potential landscape extends this toolkit of techniques, opening the prospect of pinpointing unaccounted sources of noise and offset charge that limit the performance of qubits and read-out devices [69, 183, 273].

4.2.2 Experimental Setup

Turning to the details of our experiments, Fig. 4.5 (a-d) show four separate GaAs/(Al,Ga)As devices with distinct gate patterns fabricated using electron-beam lithography and TiAu metallization for the gate electrodes. The growth of the heterostructure material spans separate molecular-beam epitaxy machines, and each device has been examined over multiple cooldowns and in different dilution refrigerators. The devices are also different in terms of their carrier density, mobility, and the depth of the two-dimensional electron gas (2DEG) from the surface (for details see the caption of Fig. 4.5). In the case of devices 3 and 4, the TiAu gate electrodes are separated from the GaAs surface by an 8 nminsulating barrier of halnium oxide (HfO), deposited using atomic layer deposition. Devices 1 and 3 were cooled with positive bias [47]. Despite all of these differences, anomalous oscillatory signals routinely appear in the response of the gate sensors, without any clear correlation to the device

geometry or heterostructure material characteristics.

Gates coloured orange in Fig. 4.5 (a-d) are wire-bonded to radio-frequency (rf) LC tank circuits to enable DGS using rf reflectometry [157, 143]. In this configuration, the capacitive component of the resonator comprises parasitic C_p, gate C_g, and quantum C_q contributions, as shown in Fig. 4.5 (e). A typical response of a resonator with frequency, shown in Fig. 4.5 (f), depends strongly on the gate voltage, which alters the capacitance in the region of the gate electrode. With all other gates held at 0 mV, stepping gate G1 from low bias to a bias that fully depletes the 2DEG underneath the gate shifts the resonant frequency as the reactance of the circuit changes. For subsequent figures the phase response is detected by mixing down the reflected rf carrier to baseband, yielding a voltage V_{DGS} proportional to the change in resonator reactance at a fixed frequency.

Examining now the anomalous signals in the DGS response, Fig. 4.6 presents representative data sets in which the response of the gate sensor (the red coloured gate in the Fig. 4.6 insets) exhibits oscillatory patterns under various configurations of gate bias (see the caption for detailed explanation). Although the particular gate pattern was designed to produce quantum-dot qubits with tunnel coupling to the source-drain reservoirs, for the present study we intentionally do not bias the gates to values that would typically form a quantum dot in the centre region. Focusing on device 1, Fig. 4.6 (a) shows the response of the gate sensor V_{DGS} as a function of the gates G1 and G5, with the other gates held at constant bias. In this regime, the DGS response exhibits a complex pattern of lines that do not resemble the signal expected for an intentional quantum dot [157]. Instead, the pattern of lines changes amplitude, period, and slope with the gate bias. A small variation in the bias of G3 dramatically alters the pattern [see Fig. 4.6 (b)], providing the first clue that the signal originates from the electron gas, likely close to the end of the gates. To make it easier to see the fine details in these complex patterns, we plot the derivative of the sensing signal with respect to the gate voltage, as shown in Figs. 4.6 (c) and (d), now as a function of G2 and G5.

4.2.3 Discussion

Breaking with our presentation of the data and moving to our interpretation, we suspect that these anomalous signals stem from charge transitions, not from an intentional quantum dot but from electrons tunnelling between disorder-induced charge pockets in the potential landscape. The sketch in Fig. 4.6 2(e) illustrates this interpretation, showing how as the electron density is reduced by gate depletion, the homogeneous 2DEG breaks up into shallow puddles of charge, separated by tunnel barriers. The spatial distribution of such puddles

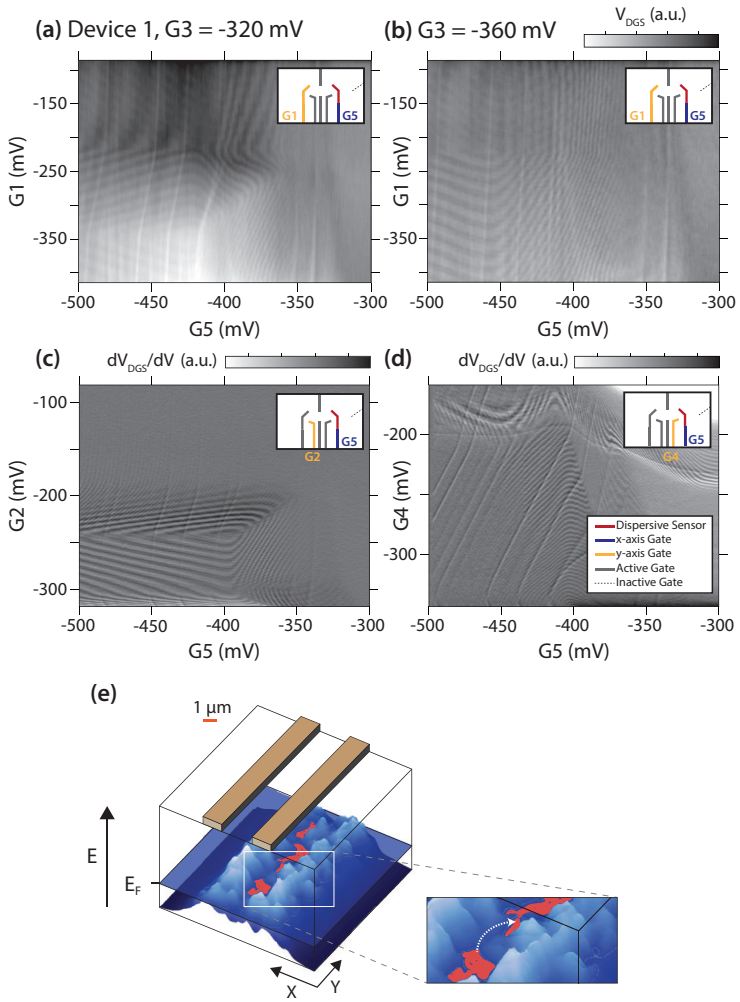

Figure 4.6: (a) and (b) The complex, oscillatory pattern in the DGS response for device 1, as a function of gates G1 and G5, adjusting G3 by $40\,\mathrm{mV}$ between (a) and (b). This pattern does not resemble a typical DGS signal for a quantum dot. (c), (d) The derivative of V_{DGS} with respect to the gate bias, now as a function of G2 and G4. Active gates are held at constant potential and inactive gates at zero [see legend in (d)]. (e) A sketch illustrating our interpretation: charge pockets form underneath the gate when electrons are partially depleted, giving rise to Coulomb-blockade oscillations in the DGS readout signal.

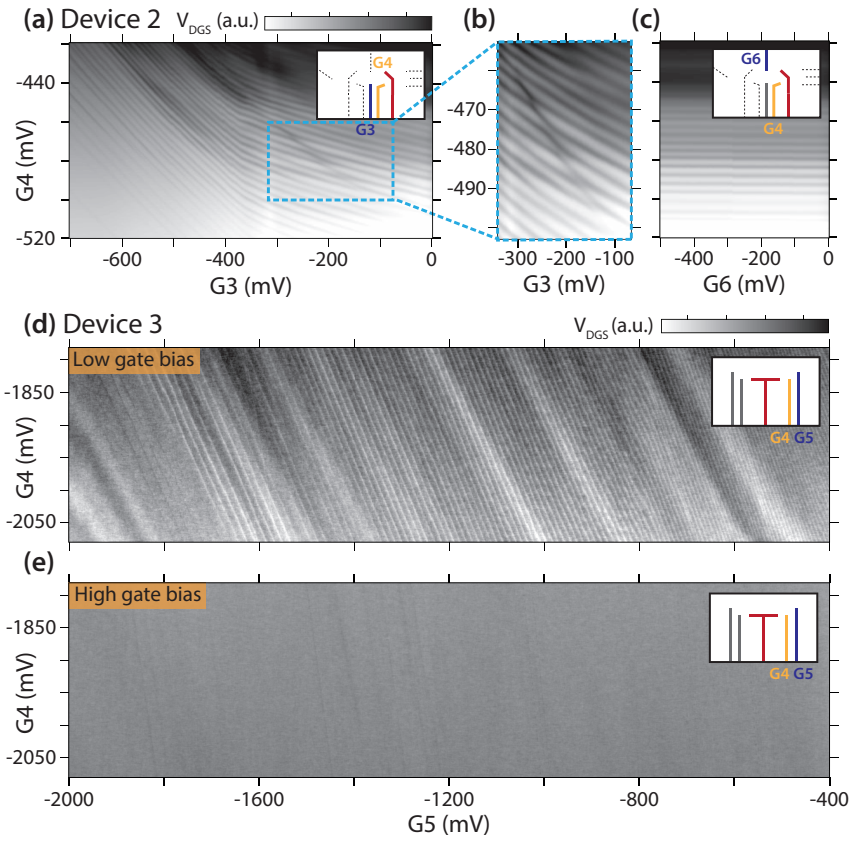

Figure 4.7: (a) The DGS response for device 2, as a function of the bias on G3 and G4, with G1, G2 and G6 held at 0 V to ensure that a quantum dot is not intentionally formed. (b) Close inspection of (a) reveals an avoided crossing. (c) The DGS signal as a function of G6 and G4. The response is insensitive to the bias applied to G6. (d), (e) For device 3, a comparison between the DGS response (d) when all gates are biased to low negative gate voltages and (e) at high negative gate voltages, where the oscillations are suppressed.

is well understood [304, 311] to reflect the configuration of partially ionized silicon donor sites in the Al(Ga,As), surface-charge arrangement, and crystal disorder at the heterostructure interface. Likely, as the gate bias is varied, the presence of these disorder-induced charge pockets leads to tunnelling transitions which can be detected with the dispersive gate sensing technique. Although not completely understood, we suggest that the curvature and changing slope of the lines relates to the complicated shape of the charge pocket and its response to fields from the gates, as well as the distance, orientation, and direction of tunnelling, relative to the gate sensor [311].

In what follows, we pursue this charge-pocket interpretation as an explanation for the complex patterns observed with gate sensing, gathering further evidence from measurements on additional devices. Switching to device 2, for instance, we again observe oscillatory structure in the gate-sensor response, as shown in Fig. 4.7 (a). In an effort to further

pinpoint the source of this signal, we limit the gate bias to three gates, holding the other gates at zero to ensure that a quantum dot cannot be formed in the central region. Nevertheless, even with three gates, close inspection of the data in Fig. 4.7 (a) [see the enlarged region in Fig. 4.7 (b)] reveals the presence of avoided crossings in the DGS signal and provides additional evidence that we are detecting interacting charge pockets in the potential landscape. Of interest, application of a voltage to the upper gate, G6, is seen to have no effect on the data, as shown in Fig. 4.7 (c).

The strongest evidence that the anomalous patterns in the DGS response are associated with charge pockets is presented in Figs. 4.7 (d) and (e), with data now taken on yet another device (device 3). Here, we compare the gate-sensor response, first with all other gates at low bias [Fig. 4.7 (d)] and then with all other gates set to highly negative voltages [Fig. 4.7 (e)], well past the typical bias required to deplete the electron gas. In the data taken in the high gate-bias regime, nearly all of the anomalous signals appear to vanish, again consistent with our interpretation that the signals arise from charge pockets that can be expelled with sufficient gate bias. Finally, we note that in the case of device 3, the surface gates are insulated from the GaAs by a thin layer of HfO. Despite the presence of the HfO, the oscillatory structure in the readout persists at low gate voltage, discounting explanations based on surface charge states or gate leakage, which would otherwise likely be modified by the addition of an insulating layer.

Given our suspicion that the anomalous DGS signals arise from charge pockets under or near the gates, an obvious check is to look for comparable signals with conventional charge detectors such as an SET or QPC configured as a sensor, by monitoring its conductance close to pinch-off. Measurements with device 4 enable such a direct comparison, as shown in Fig. 4.8. Here, we form a QPC by pinching off the electron gas between gates G2 and G3 and measuring the transport current between ohmic contacts, as shown in Fig. 4.8 (a). Although this QPC does not exhibit clean quantized conductance plateaus, it pinches off steeply near zero bias to make a good charge sensor. We then compare the transport response of the QPC to the signal from the DGS sensor [Fig. 4.8 (b)], both measured as a function of source-drain bias V_{SD}. Clear in the DGS response is the presence of an oscillatory pattern around $V_{\mathrm{SD}} = 0\,\mathrm{V}$, typical of the signal that we interpret as tunnelling between charge pockets in Coulomb blockade. Interestingly, this oscillatory signal begins to weaken as the QPC opens up (the lighter, diamond-like features near G2 $\sim -400\,\mathrm{mV}$ relate to the DGS detecting the first QPC subband edge [312]). Comparing the response of the two detectors at zero bias, Fig. 4.8 (c) displays a strong oscillatory signal in the DGS response (blue) that extends well past the gate bias at which the QPC pinches-off. In contrast, the

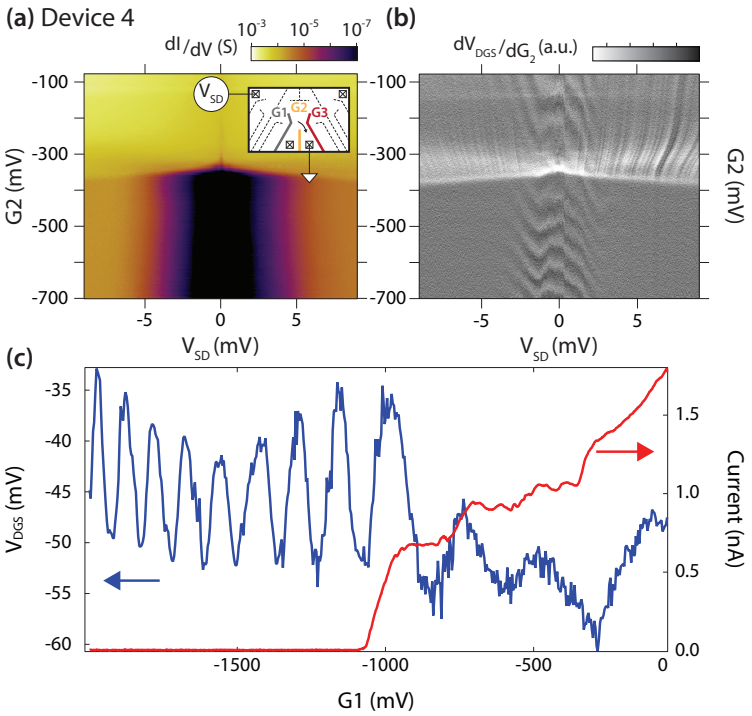

Figure 4.8: A comparison of QPC-based charge sensing and DGS. (a) The differential conductance dI/dV of a QPC formed with device 4, as a function of the gate and source-drain bias. (b) The corresponding response of the gate sensor for the same region of the gate and source-drain bias, V_{SD}. Note the appearance of the oscillatory structure around $V_{\mathrm{SD}} = 0\,\mathrm{V}$, which is absent in the transport measurement. (c) The data at $V_{\mathrm{SD}} = 0\,\mathrm{V}$, showing a strong oscillatory response in DGS (left axis) that does not correlate with features in the QPC transport (right axis), even near pinch-off where the QPC acts as a charge sensor.

QPC transport signal (red) does not show any discernible features that correspond to the oscillatory structure in the DGS signal.

We suggest two explanations to account for the discrepancy between the signals from the two detectors. First, the location of the charge pockets is likely under, or very close to, the gate, since this is where the electrons are depleted by the gate bias. In this picture, a charge pocket could be far from the QPC and strongly screened by the gate metal to the extent that it is undetectable by the QPC sensor. Alternatively, if the pocket is under the gate it is always closely coupled to the gate and can alter its quantum capacitance. In fact, screening by the gate metal constitutes the DGS signal. Second, we note that in the case of DGS the oscillating rf voltage on the gate induces the tunnelling transitions, which are detected synchronously, i.e., in relation to the phase of the rf signal, whereas the QPC charge sensor makes a time-average measurement of the induced charge.

We next examine the temperature dependence of the patterns seen in the DGS response, and in keeping with our interpretation that they arise from charge pockets, extract their charging energy. Taking device 2 as an example, Fig. 4.9 (a) shows the amplitude of the anomalous DGS oscillations [measured as the magnitude of their fast Fourier transform (FFT)] as a function of the cryostat temperature. Raising the temperature above $T \sim 300\,\mathrm{mK}$ rapidly suppresses the oscillations in the DGS signal, presumably as the thermal energy becomes comparable to the charging energy of the pocket, that is, on the order of a few tens of microelectronvolts, an order of magnitude smaller than the typical charging energies measured for intentional, gate-defined quantum dots used as a qubits [9]. Such a small charging energy is consistent with a large capacitance between the charge pocket and the gate, as could be expected if the pocket is underneath or very closely coupled to the gate.

Finally, in an effort to better pinpoint the location of the charge pockets we make use of a QPC as a highly local source of joule heating. By controlling the bias across the QPC, this approach allows a very small amount of heat to be generated at the micron-scale region surrounding the QPC, as opposed to elevating the temperature of the whole chip, essentially creating a local temperature gradient. Biasing gates G7 and G5 to configure a QPC, we control the dc voltage across ohmic contacts O1 and O2 and perform DGS readout from gate G5, as shown in Figs. 4.9 (b) and (c). At low gate bias, with the QPC open and low resistance, the presence of current between O1 and O2 has little effect on the oscillations in the DGS signal. When the QPC is partially closed, however, the presence of a source-drain bias, V_{SD}, leads to suppression in the oscillatory pattern measured by the gate sensor, as indicated by comparing Fig. 4.9 (b) ($V_{\mathrm{SD}} = 0\,\mathrm{mV}$) to Fig. 4.9 (c) ($V_{\mathrm{SD}} = -2\,\mathrm{mV}$). The oscillations are restored when the QPC is fully pinched off and the current drops to zero.

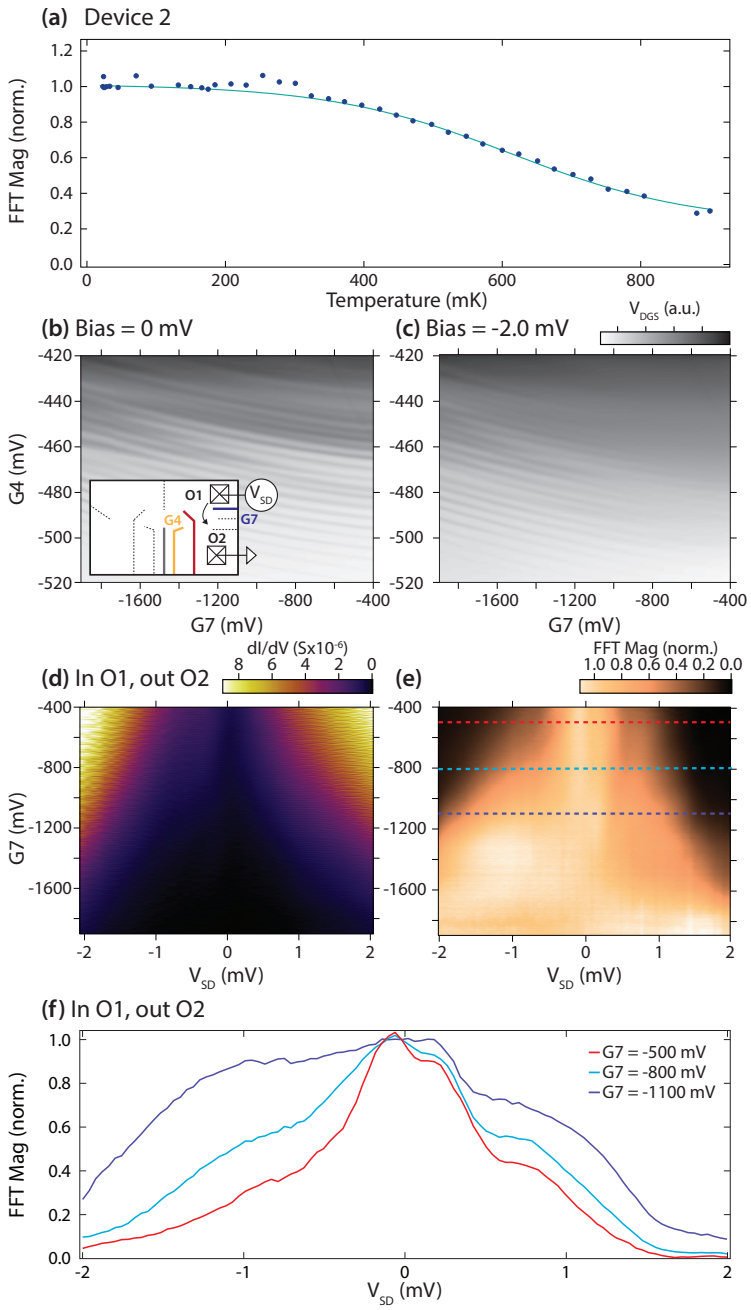

Figure 4.9: (a) The temperature dependence of the DGS oscillations, as quantified by their Fourier amplitude, normalised with respect to their amplitude at a base temperature of approximately $20\,\mathrm{mK}$. The line is a guide to the eye. (b) The DGS response as a function of G7 and G4, without a source-drain bias across the QPC. (c) DGS oscillations with a QPC bias of V_{SD} = - 2.0 mV. (d) The differential conductance of the QPC as a function of the source-drain bias V_{SD}. (e) The amplitude of the DGS oscillations, quantified as the magnitude of their Fourier component, as a function of the gate bias G7 and V_{SD}. (f) Horizontal one-dimensional line cuts of the data in (e) at positions indicated by dashed lines.

Investigating further, we make a more detailed examination of this effect by first measuring the QPC differential conductance, as shown in Fig. 4.9 (d). As the QPC is nearly pinched off, appreciable conductance only appears at high V_{SD}. Next, we quantify the amplitude of the DGS oscillations by taking their FFT magnitude as a function of V_{SD} and the gate bias, G7, as shown on the intensity axis in Fig. 4.9 (e) and as 1D line cuts in Fig. 4.9 (f). In this way, we are making use of the anomalous DGS signal from the pockets as a highly local thermometer. We can calibrate this (Coulomb-blockade) thermometer using the data in Fig. 4.9 (a), which gives the FFT magnitude of the oscillations as a function of the cryostat temperature. With this calibration in hand, we determine that the presence of a modest source-drain bias across the QPC, say 0.5 mV, dissipates only picowatts of power, but surprisingly heats the charge pockets to a temperature of the order of approximately 700 mK. Given that the cryostat has a cooling power of hundreds of microwatts at this temperature, and given crude estimates for the thermal conductivity of the chip, we conclude that the QPC creates a hot spot that returns to the bulk equilibrium temperature over a scale of the order of the electron scattering length l_ϕ. This reasoning, although somewhat tentative, is again consistent with our interpretation that the location of the charge pockets is within a few microns of the QPC hot spot, likely not at the very tip of the gates but, rather, under the wider sections of the gates as they taper out and are partially depleted.

4.2.4 Conclusion

Throughout this paper, we present data consistent with our interpretation that electron tunnelling between unintentional charge pockets leads to oscillatory signals in the dispersive response of gate sensors. Summarising, this evidence includes the following: the sensitivity of the oscillatory patterns to the bias of nearby gates (Fig. 4.6); the presence of avoided crossings (Fig. 4.7 (b)); and the suppression of signals when gates are fully depleted (Fig. 4.7 (d)). Carrying this argument further, the data in Fig. 4.8 show that these signals are not detectable with a QPC charge sensor, presumably because screening from the gate metal makes them difficult to detect using standard charge sensing — in contrast to DGS, where the pockets contribute directly to the quantum capacitance of the gate. Finally, the data in Fig. 4.9 suggest that the charge pockets are reasonably localized to the vicinity of the QPC, and, given their small charging energy, it is likely that such pockets correspond to shallow micron-scale quantum dots that form directly under the gates as the electron gas is partially depleted. Counting the number of Coulomb-blockade oscillations, we estimate these pockets contain tens of electrons or more.

Drawing attention to the possibility that these shallow pockets may be perturbed by

proximal QPC transport and considering that qubits are operated by rf gate pulses or microwaves, it is likely that their presence can lead to charge fluctuations during qubit readout and control. The extent to which these pockets can be alleviated via the use of bipolar induced-electron device structures [313, 19] is an open direction for mitigating noise and offset charges in semiconductor qubits.

Acknowledgments

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Chapter 5

Majoranas and InAs

As we discussed in Sec. 1.1.3, qubits of all forms are subject to decoherence, which leads to a loss of information from the quantum state. This leads to a limited lifetime for quantum states, and errors in the outputs of our quantum computations. The discovery of the quantum threshold theorem [4, 5] allowed for errors to be theoretically corrected at a rate faster than they occur, however, to implement this in practice, information must be spread out over many qubits and constant error-correcting operations must be applied. The number of extra qubits and the number of operations that must be performed increases rapidly near the minimum error threshold for a given error correction algorithm, and even for state-of-the-art qubit fidelities of 10^{-5}, up to 10,000 physical qubits are required to form a single logical qubit, and up to 40,000 error correction operators must be applied per logical gate operation [89]. The higher the qubit fidelity, the lower the error correcting overhead [314]. Although there is continued improvement in the fidelities of most qubits, coupling to the environment, either via electric or magnetic fields, is inevitable, as qubits are traditionally controlled by either electric or magnetic fields, or both. A fundamentally different approach to building a qubit, one which distributes the qubit state over pairs of neutral fermions, called non-abelian anyons, was introduced in [93]. The computational states are part of an extended, degenerate ground state and operations are performed by moving particles around each other, with the information stored in qubits insensitive to any local perturbations. In particular, one non-abelian anyonic system is that of Majorana zero modes (MZMs), the theory of which we covered in Sec. 1.2.4.

These MZMs are not fundamental particles, they don't exist in nature as far as we know[1], hence we must engineer them as an emergent quasiparticle. The theory of forming MZMs

[1]There is a theory that neutrinos may, in fact, be Majorana fermions. Unfortunately, even if they were, they interact so weakly that we would not be able to control them in a quantum computer.

is covered in Sec. 1.3.6. Briefly, the method by which we find these particles in this thesis is to use semiconductor-superconductor hybrid materials, which requires:

- Large Landé g-factor
- Large spin-orbit interaction
- High mobility
- A hard superconducting gap

These requirements are generally met by using heavy-element III-V semiconductors, using either nanowires grown by the VLS method [129, 315], or using shallow quantum wells [316], both of which are proximitized using an epitaxially grown Aluminum layer. The use of a 2DEG allows for scalable device designs, however, the quality of the 2DEG is compromised by charged surface states, which, due to the shallow depth at which the quantum well is formed, it is highly sensitive to. In Sec. 5.1, we explore techniques for treatment of the surface to try and repair these surface impurities.

Having formed Majorana zero modes, we must also read them out in a reliable way. One way of performing readout is to project the state of a pair of MZMs into a charge state in a process termed parity-to-charge conversion [317]. This technique is in many ways analogous to the spin-to-charge conversion process discussed in Sec. 2.1.2 and in [206, 9]. However, this requires a charge sensor, which, for nanowire-based devices cannot be formed in the ways previously discussed. In Sec. 5.2, we discuss techniques for creating charge sensors using nanowires capacitively coupled to qubit devices, thereby inventing a method by which a topological qubit may be read, and characterize their performance.

5.1 Repairing the Surface of InAs-based Topological Heterostructures

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Abstract

Candidate systems for topologically-protected qubits include two-dimensional electron gases (2DEGs) based on heterostructures exhibiting a strong spin-orbit interaction (SOI) and superconductivity via the proximity effect. For InAs- or InSb-based materials, the need to form shallow quantum wells to create a hard-gapped p-wave superconducting state often subjects them to fabrication-induced damage, limiting their mobility. Here we examine scattering mechanisms in processed InAs 2DEG quantum wells and demonstrate a means of increasing their mobility via repairing the semiconductor-dielectric interface. Passivation of charged impurity states with an argon-hydrogen plasma results in a significant increase in the measured mobility and reduction in its variance relative to untreated samples, up to 45 300 $\mathrm{cm}^2/(\mathrm{V\,s})$ in a 10 nm deep quantum well.

5.1.1 Introduction

Interest in proximitized InAs- and InSb-2DEGs has intensified recently due to their potential application in spintronics [318] and topological quantum computation [97, 21]. These materials can exhibit superconductivity via the proximity effect, induced by the presence of aluminum deposited on their surface, which strongly couples to the quantum well. The induced superconductivity combined with strong SOI (and a large Landé g-factor) results in the formation of Majorana zero modes (MZMs), now observed in both nanowires [99, 319] and 2DEGs [50, 320], at the boundaries of the topological superconductor [122, 95, 123]. Interest in MZMs, which are emergent quasi-particles hypothesized to have non-abelian exchange statistics, stems from their potential to provide topological protection to quantum information [93].

Early experimental platforms for realizing MZMs in both nanowires and 2DEGs utilized superconductors deposited ex-situ, however these systems demonstrated a a significant density of states sub-gap that obscured the signatures of the MZM [321, 322]. Alternatively, in-situ deposition of a superconductor, such as epitaxially growing aluminum directly after semiconductor growth, results in a significant improvement in the quality of the superconducting gap [129, 323], and the realization of a quantized zero-bias peak [132]. In-situ deposition poses additional fabrication challenges however, as the Al must be removed to define the topological region of the device. Removal via a wet-etch solution selective to Al is a highly exothermic reaction that results in damage to the surface of the semiconductor. This damage manifests as increased roughness and induced impurities, lowering the mobility of the 2DEG [2] and compromising the fragile induced p-wave superconducting pairing [326, 327]. Further, since the length scale over which hard-gap superconductivity is maintained across a clean interface is set by the height and thickness of the barrier [322] burying the 2DEG deep in the heterostructure is not feasible [316]. Taken together these aspects point to a need to develop new fabrication techniques that maintain or repair defects introduced at the surface.

Here we investigate the scattering mechanisms that reduce mobility in shallow InAlAs/InAs/InGaAs 2DEG heterostructures following wet-etch of the proximitizing superconductor. By studying Hall mobility as a function of density, we show that surface scattering is the dominant mechanism for reduced mobility in shallow 2DEG samples. We demonstrate that the mobility can be increased and the variance of mobility reduced by exposing the sample to an in-situ Ar-H plasma, prior to deposition of a protective ALD-

[2] From 44 000 $\mathrm{cm}^2/(\mathrm{V\,s})$ [324] down to 1000 to 2000 $\mathrm{cm}^2/(\mathrm{V\,s})$ [323, 325]

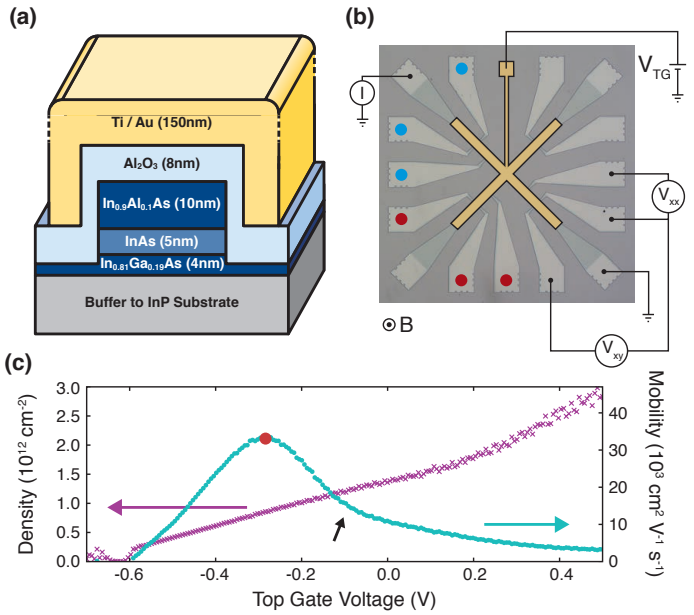

Figure 5.1: (a) Cross section of a shallow InAlAs/InAs/InGaAs quantum well after removal of epitaxially grown Aluminum. A protective layer of Al_2O_3 is grown, along with a 150 nm Ti/Au surface gate which is used to tune the electron density. (b) False color micrograph and schematic of the experimental setup showing one combination of current and voltage contacts. Red and blue dots indicate alternative measurement points. (c) The density (violet) and mobility (cyan) of sample B are extracted from magnetoconductance measurements as the top gate is swept. The red mark indicates the location of peak mobility. The black arrow indicates the location of the onset of second subband filling.

grown Al_2O_3 coating. We compare the mobility of these to control samples exposed to an in-situ trimethylaluminum (TMA) pre-treatment, or to samples without any pre-treatment, prior to oxide growth.

5.1.2 Experiment

The devices are fabricated from a InAlAs/InAs/InGaAs quantum well grown 10 nm below the surface on a 2" (100) InP substrate [131]. An 8 nm Al layer is grown epitaxially on the surface of the heterostructure directly following the semiconductor growth. On each sample, a Hall bar geometry is defined using a dilute phosphoric acid etch, and Al is selectively removed over the Hall bar with an Aluminum wet etch (Transene type-D). Contact to the 2DEG is made using sections of un-etched Al, which forms an ohmic contact. The surface is then treated using either TMA as a reducing agent to remove the native oxide [328, 329] or with a ArH plasma to terminate charged impurity states [330], and without breaking vacuum, a 10 nm Al_2O_3 oxide is grown via ALD at 200 °C, using a TMA precursor and either H_2O or O_3 as an oxidizing agent. Finally, a 150 nm Ti/Au gate is evaporated on the

Table 5.1: A full listing of sample growth parameters that were tested. Two surface treatments (TMA Reduction and H_2 Passivation) and two oxidizers (H_2O and O_3) are tested to find their effect on sample mobility. Each treatment and oxidizer pair are measured on two chips, one taken from the center of the growth wafer, the other from near the edge, in order to account for the effect of distance from the center of the wafer on mobility.

Sample	Treatment	Precursor/Oxidizer
A	No Treatment	TMA/H_2O
B	TMA Reduction	TMA/H_2O
C	TMA Reduction	TMA/O_3
D	H_2 Passivation	TMA/H_2O
E	H_2 Passivation	TMA/O_3

surface of the Hall bar to allow the electron density of the samples to be varied. Further details of the fabrication are contained in the Supplementary Information. A cross-sectional schematic of the Hall bar is given in Fig. 5.1 (a). For each treatment/oxidizer pair, we fabricate two samples, one taken from within 1" of the center of the wafer (denoted 'near'), the other taken from the outer 1" ring (denoted 'far'), in order to account for variation in mobility as a function of distance from the center of the wafer [331]. A full list of tested sample parameters is given in Table 5.1. We note that despite the higher quality of ALD oxides grown at higher temperatures, at temperatures higher than 250 °C, diffusion of In and As occurs, and above 300 °C In begins to precipitate out of the substrate due to the desorption of As [332].

Measurements were carried out in a dilution refrigerator with a base temperature of 7 mK. A Cryo-CMOS based multiplexer is used to allow simultaneous measurement of up to 10 Hall bars in a single cool-down [333]. Magnetotransport measurements were performed to extract electron densities and mobilities using conventional AC lock-in techniques, with a 10 nA constant current. A representative Hall bar is shown in Fig. 5.1 (b), with longitudinal (R_{xx}) and transverse (R_{xy}) resistance measured simultaneously. Three measurement points are defined around the edge of the Hall bar, indicated with blue, red and black dots, allowing multiple independent measurements of mobility and density to be made on each sample, from which statistics on each treatment are gathered. Hall bars were oriented at 45° to the (011) and $(01\bar{1})$ plane to remove effects of any anisotropy along different crystallographic axes [334, 335]. For each sample, density and mobility are extracted as the top gate is swept. A representative measurement is shown for sample B, taken from near the center of the growth wafer, in Fig. 5.1 (c). Mobility is extracted at 0.05 T, which is a sufficiently large offset to ensure we are no longer on the weak-antilocalization peak. For this sample, a peak value for mobility is extracted of 33 400 $\mathrm{cm}^2/(\mathrm{V\,s})$ at a density of

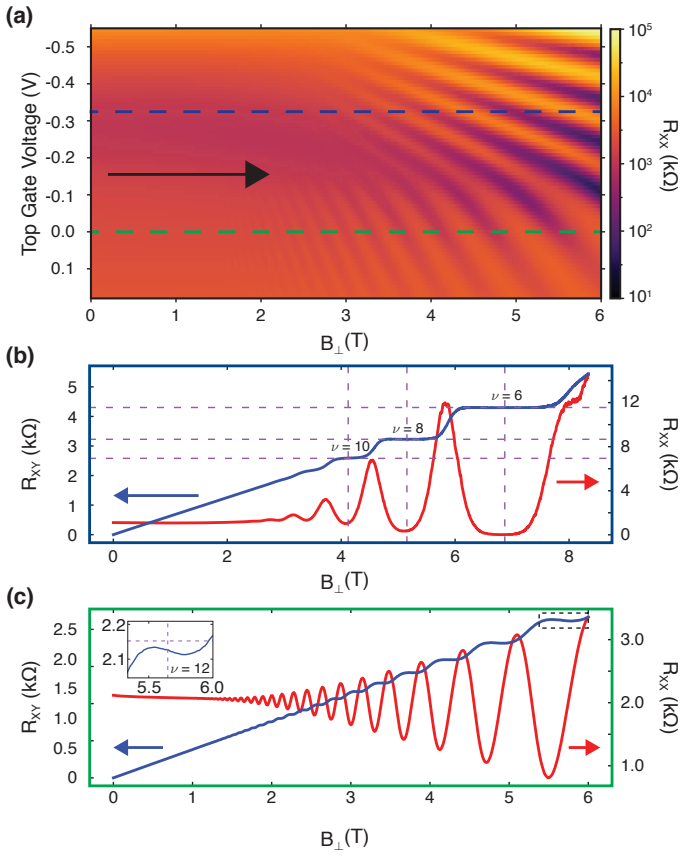

Figure 5.2: (a) The Landau fan for sample B. The black arrow marks the onset of second subband population, indicated by a change in slope of the Landau levels as a function of magnetic field and top gate voltage. The location of peak mobility is indicated by the blue dashed line. (b) Magnetoresistance taken at the point of highest mobility on sample B. Well resolved hall plateaus are observed, starting from $\nu = 10$ (see main text for details). (c) Magnetoresistance measurements of sample B to high field, taken at $V_{TG} = 0\,\mathrm{V}$. Hall plateaus show an oscillation characteristic of parallel conduction paths.

$8.73 \times 10^{11}\,\mathrm{cm}^{-2}$, corresponding to a gate voltage of $V_{TG} = -0.27\,\mathrm{V}$, indicated by the red point in Fig. 5.1 (c).

We can attribute different dominant scattering mechanisms to various ranges of the density [336, 337, 338]. As the density increases from zero, scattering is predominantly caused by scattering off background impurities distributed through the heterostructure [339]. Increased screening of impurities as the density is increased leads to an increase in mobility. As the gate voltage and density is further increased, the mobility is seen to peak, before reducing with increasing density. Increasing top gate voltage causes the the distribution of electrons in the quantum well to shift towards the surface [340, 341], and surface scattering becomes dominant over the increased impurity screening with higher density, leading to the decrease in mobility observed at higher densities.

The subband occupation can be extracted from magnetotransport measurements at high magnetic fields. Fig. 5.2 (a), shows a Landau fan for sample B measured in a second cooldown, plotting R_{xx} as V_{TG} and B are swept. The onset of second subband population is marked by the arrow and occurs at $V_{TG} = -0.16\,\mathrm{V}$, denoted by the change in the slope of the location of Landau levels as a function of gate voltage and magnetic field [342, 343]. The onset of second subband population is also visible as a kink in the mobility as a function of V_{TG}, indicated by the black arrow in Fig. 5.1 (c), caused by a reduction in the rate of filling of the first subband N_{S1} relative to the total density $N_T = N_{S1} + N_{S2}$.

The sample shows significantly different magnetotransport behavior when the first and second subbands are occupied. When the top gate is tuned to the value that maximizes mobility at low magnetic fields and only a single subband is occupied, well resolved Hall plateaus are observed from $\nu = 10$ onwards, with the Hall resistivity quantized to within 0.11% of the theoretical value at $\nu = 6$, and a vanishing longitudinal resistance of $R_{xx} = 2.4\,\Omega/\square$. No Shubnikov-de Haas oscillations are observed. In contrast, when the second subband is occupied at $V_{TG} = 0\,\mathrm{V}$ (Fig. 5.2 (c)), clear Shubnikov-de Haas oscillations are visible from 1.5 T to 6 T, despite the much lower mobility of the sample at this point. This is caused by the increased screening of the impurity potential by the electrons of the second subband, and has been observed in measurements of low-mobility GaAs 2DEGs [344]. Further evidence of second subband population is seen in the Hall plateaus which are not well quantized and exhibit an oscillatory behaviour (inset Fig. 5.2 (c)), an effect attributed to parallel transport in the second subband.

5.1.3 Surface Treatments and Oxide Growth

The native oxide layer in both GaAs and InAs is known to contain a large number of charged defects [345, 346], caused by unpaired As atoms within the oxide formed by an excess of As during the oxidation of In and Ga [347, 348]. These defects act as scattering sites at the surface of the wafer, and limit the mobility of samples above a certain density. Reducing the concentration of surface scattering sites through chemical treatment prior to dielectric deposition provides a clear pathway to increasing the sample mobility.

The first approach that we examine is the removal of the native oxide through reduction by TMA[349, 350, 351]. TMA is known to remove the surface oxides of InAs via the following reaction [329]:

$$2\,\mathrm{Al(CH_3)_3} + \mathrm{In_2O_3} \longrightarrow 2\,\mathrm{In(CH_3)_3} + \mathrm{Al_2O_3} \tag{5.1}$$

$$2\,\mathrm{Al(CH_3)_3} + \mathrm{As_2O_3} \longrightarrow 2\,\mathrm{As(CH_3)_3} + \mathrm{Al_2O_3} \tag{5.2}$$

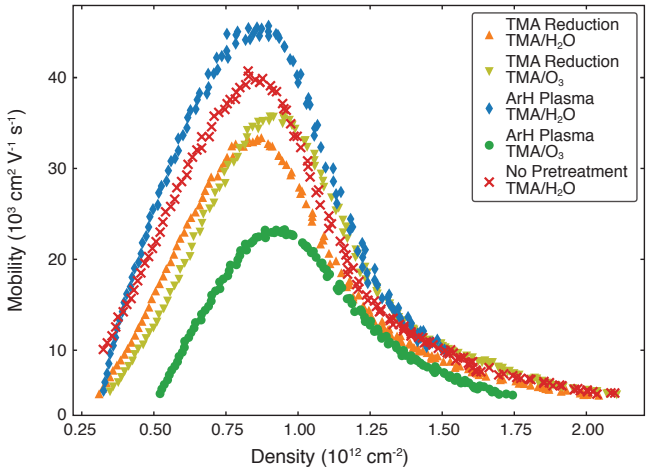

Figure 5.3: Representative mobility vs. density traces for each treatment, taken from samples near the center of the wafer. Samples oxidized with O_3 show a shifted peak mobility relative to those oxidized with H_2O. A peak mobility of $45\,300\,\mathrm{cm}^2/(\mathrm{V\,s})$ is extracted for a sample treated with a Hydrogen plasma.

For TMA treated samples, a 1 s pulse of TMA is applied to the surface in the ALD chamber, followed by a 30 s purge with N_2 gas, at a 200 °C process temperature. This pulse cycle is repeated 18 times to maximize the reaction time, prior to the growth of the dielectric.

The second approach that we examine is the removal of surface oxides and the passivation of charged impurities at the surface via the application of an ArH plasma to the chip [351, 330, 352]. For this process, a remotely generated ArH plasma is applied to the surface of the samples for a total of 120 s before the growth of the dielectric layer. Atomic hydrogen is known to bond to As atoms and saturate the dangling bonds, passivating the surface [330]. A hydrogen plasma is also known to selectively remove the surface oxide via dry etching, again leading to an abrupt semiconductor-dielectric interface [353, 354].

In Fig. 5.3 we plot mobility as a function of density for each treatment, with samples taken from near the center of the wafer. The use of ArH plasma in combination with oxide growth using TMA and H_2O as an oxidizer was found to increase the measured mobility relative to an untreated sample, showing the highest peak mobility for both near and far samples. In contrast, oversaturation with TMA causes a decrease in mobility compared to a single TMA exposure before Al_2O_3 growth. Finally, we note that the use of O_3 as a precursor does not seem to be effective for the creation of a clean dielectric interface – both ozone samples show a decreased quality relative to no treatment, however the peak mobility shifts to a higher density. Measurements are taken on both samples near the center of the growth wafer (near) and samples taken far from the center of the growth wafer (far), across

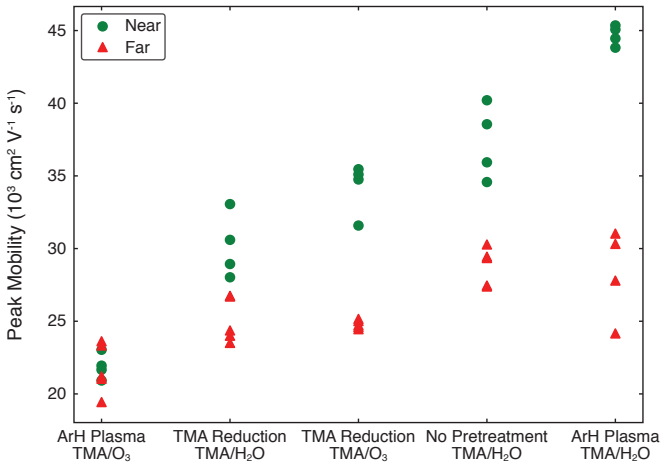

Figure 5.4: Peak mobility achieved for different treatment and oxidizers. Measurements are made across different two samples, taken from near the center of the growth wafer (green) and from near the edge of the growth wafer (red), and at multiple locations on each Hall bar. Each point represents the peak mobility extracted from a sweep of gate voltage, as shown in red in Fig. 5.1 (c), which were collected over multiple cooldowns, and at multiple measurement points.

multiple measurement points and multiple cooldowns, as shown in Fig. 5.4. While there exists a significant difference in the mobility of samples taken from different parts of the growth wafer, there remains a definite trend amongst similarly treated samples. The use of ArH plasma in combination with oxide growth using TMA and H_2O as an oxidizer results in a significant reduction in variance in mobilities for the highest quality samples.

5.1.4 Scattering Mechanisms

Finally, we turn to a detailed examination of scattering mechanisms across different density ranges and surface treatments. Unlike semiconductors such as GaAs where the Fermi level is pinned in the band gap, the location of the Fermi level in InAs has been shown to depend sensitively on surface states. Even in nominally undoped heterostructures, an electron density in the quantum well at zero gate voltage is induced by charged impurities at the surface [355, 348]. As the concentration of charged impurities is decreased, the electron density in the quantum well at zero gate voltage is decreased towards zero. Fig. 5.5 shows the density at zero gate voltage against the peak mobility. We observe an inverse relationship, with the samples that have the highest mobility also having the lowest intrinsic electron density. Atomic hydrogen plasma is thus an effective method for terminating these charged impurities prior to dielectric growth.

In contrast, samples treated with TMA see either no significant change in the density

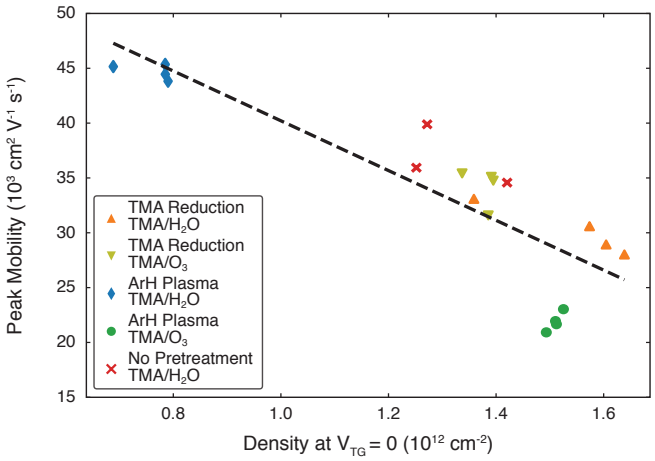

Figure 5.5: Scatter plot of density at zero gate voltage against the peak mobility, for samples taken near the center of the growth wafer. Samples with the lowest density at zero gate voltage have the highest measured peak mobility. The dashed black line is a linear fit, and is a guide to the eye.

of charged surface states or see an increase relative to no pre-treatment. Although TMA treatment has been demonstrated to be effective in removing the surface oxide, such studies largely investigate the optical properties of the cleaned surface, using either X-ray photoemission spectroscopy [349, 350, 351] or infra-red spectroscopy [356], rather than the electrical properties. We suggest that the inconsistency between previous studies and our result can be explained by the growth of an Al_2O_3 layer. This acts as a diffusion barrier at 200 °C and terminates the native oxide removal process before completion [357], which in this case limits the effectiveness of the treatment.

To understand the reduced mobility observed when using ozone as the oxidizer in the ALD process, we examine the relationship between density and mobility when peak mobility is achieved (See supplementary for additional data). The peak mobility in O_3 samples is shifted towards higher densities compared to those samples that use H_2O. Previous studies have found that the AlO_x grown by ozone is oxygen-rich relative to the optimal stoichiometry for aluminum oxide [328, 358]. The increased incorporation of oxygen in the oxide will appear as remote charged impurity scatterers distributed throughout the dielectric [339], and therefore a higher electron density has to be reached before these are fully screened.

5.1.5 Conclusion

In summary, we find scattering off charged surface impurities at the Al_2O_3 interface is a limiting factor in mobility in the current generation of shallow InAs quantum wells. For a quantum well 10 nm from the surface, the application of an ArH plasma prior to dielectric

growth is effective in increasing the peak mobility to $\sim 45\,300\,\mathrm{cm}^2/(\mathrm{V\,s})$, and reduces the variance in mobility compared to untreated samples or samples exposed to TMA saturation. For all samples, we find that the second subband is occupied at $V_{TG} = 0\,\mathrm{V}$. This is a complicating factor in the search for MZM in InAs 2DEGs, as an odd number of filled subbands are then required for their formation [21]. For the current generation of samples, this condition can only be met with a single populated subband whilst achieving sufficiently high mobility. Due to pinning of the Fermi level in InAs, we find that a significant negative gate voltage will be necessary to tune into this regime.

Acknowledgments

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5.2 Radio-Frequency Methods for Majorana-Based Quantum Devices

Fast Charge Sensing and Phase-Diagram Mapping[3]

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Abstract

This section presents an extract from the above paper. Radio-frequency (rf) reflectometry is implemented in hybrid semiconductor-superconductor nanowire systems designed to probe Majorana zero modes. Nanowire devices are capacitively coupled to a nearby RF single-electron transistor made from a separate nanowire, allowing RF detection of charge, including charge-only measurement of the crossover from $2e$ inter-island charge transitions at zero magnetic field to $1e$ transitions at axial magnetic fields above 0.6 T, where a topological state is expected. Single-electron sensing yields signal-to-noise exceeding 3 and visibility 99.8% for a measurement time of 1 μs.

[3] This section is an extract from the paper [359].

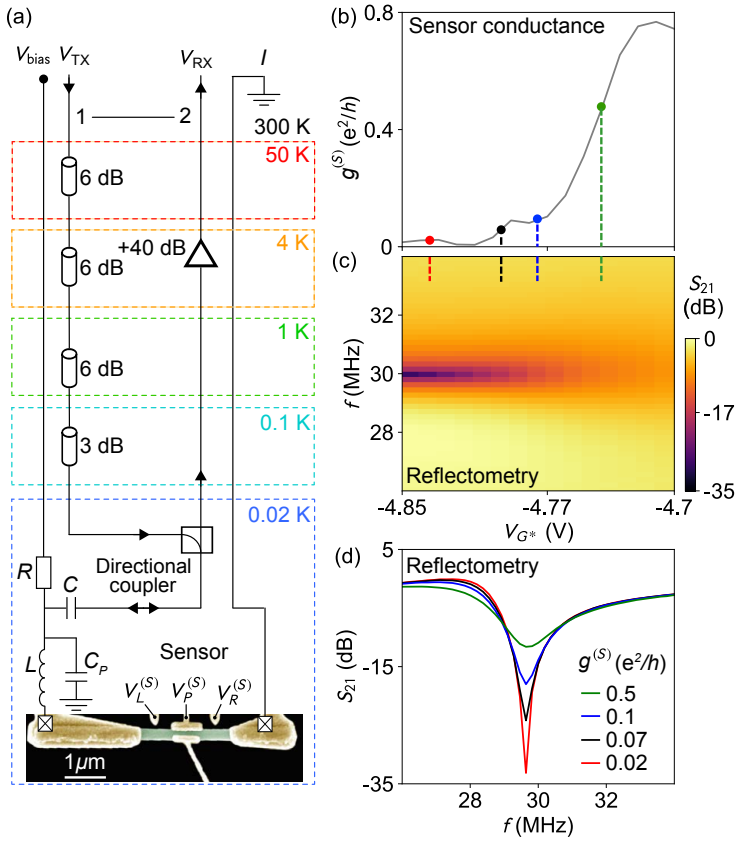

Figure 5.6: (a) A circuit diagram of a nanowire (sensor) embedded in a resonant circuit allowing conductance by measuring current $I(V_{\text{bias}})$ or reflectometry measurement (by measuring reflected signal V_{RX}), respectively (see the main text). (b) The sensor conductance, $g^{(S)}$, as a function of the sensor gate voltage, $V_{G^*} = V_L^{(S)} = V_P^{(S)} = V_R^{(S)}$. (c) The scattering parameter, S_{21}, as a function of the carrier frequency f, and V_{G^*} acquired simultaneously with (b). $S_{21}(f)$ develops a dip at $f_{\text{res}} \sim 30\,\text{MHz}$, indicating that the matching condition of the resonator is approached toward low sensor conductance. (d) Vertical cuts of (c) for the gate voltages indicated in (b). The on-resonance reflectometry signal acts as an alternative measure of $g^{(S)}$.

5.2.1 Introduction

Solid-state quantum computation schemes that involve repeated measurement and feedback, including topological schemes [317, 360, 361, 146] with potentially long coherence times [362, 96], nonetheless require fast read-out of charge or current in order to operate on reasonable time scales [141]. For topological qubits based on Majorana modes in nanowires (NWs) with proximity-induced superconductivity, quasiparticle poisoning of Majorana modes constrains read-out times to microseconds or faster [363], as has already been demonstrated for superconducting [364, 365, 366, 367] and spin qubits [368, 369, 206, 9].

Here, we report the realization of radio-frequency (rf) reflectometry in various config-

urations of InAs nanowires (NWs) with epitaxial Al, fabricated to form single or coupled Majorana islands, with proximal NW charge sensors. The device geometries are inspired by recent theoretical proposals for demonstrating elementary topological qubit operations in these systems [317, 360, 361, 146]. A resonator is capacitively coupled to a proximal NW charge sensor configured for both LF and rf charge read-out. The overall charge sensitivity is investigated as a function of the measurement time and is found to yield a signal-to-noise ratio (SNR) for single-charge detection exceeding 3 and a visibility of 99.8% for an integration time of 1 μs, with correspondingly higher values for longer integration times. Proximal NW charge sensors are found to be compatible with magnetic fields exceeding 1 T, the range needed to reach the topological regime [99, 370, 132, 319]. All measurements are carried out in a dilution refrigerator (Oxford Instruments Triton 400) a base temperature of approximately 20 mK, equipped with a 6-1-1 T vector magnet.

5.2.2 Experimental setup

The reflectometry signal is optimized by matching the circuit impedance Z, including the device resistance R_{dev}, to the characteristic impedance of the transmission line, $Z_0 = 50\,\Omega$. Near matching, the reflection coefficient of the resonant circuit, $(Z - Z_0)/(Z + Z_0)$, is sensitive to small changes in R_{dev} [154, 371]. To enable multiple simultaneous measurements, four rf resonant circuits with different discrete inductances in the range L =1.2 μH to 4.7 μH are coupled to a single-directional coupler via a coupling capacitor, C. One such resonant circuit is depicted in Fig. 5.6 (a). It consists of a ceramic-core chip inductor[4], a parasitic capacitance, C_P, from bond wires and on-chip metal electrodes, and the device, with R_{dev} tuned by the gate voltages. The parasitic capacitance is found to be unchanged over several cool-downs.

LF lock-in measurements of differential conductance $g = \mathrm{d}I/\mathrm{d}V|_{V_{\text{bias}}}$ of either the device or the sensor are carried out in a two-wire voltage-bias configuration using a transimpedance (current-to-voltage) amplifier[5] connected to the drain of the device, providing voltage input to a lock-in amplifier (Stanford Research SR830). The voltage bias consists of a dc component, V_{bias}, and a LF component in the range of 4 μV to 10 μV at frequencies below 200 Hz.

Reflectometry measurements of the sensor are performed as follows. A rf carrier at frequency f with amplitude V_{TX} is applied to the source lead following a series of attenuators

[4]Electronic Access: https://www.coilcraft.com

[5]Low Noise, High Stability I to V Converter (SP 983). Electronic access: https://www.physik.unibas.ch

at various temperature stages [Fig. 5.6 (a)], giving a total of 21 dB of attenuation, with an additional 15 dB of attenuation from the directional coupler, mounted below the mixing chamber plate. After reflection from the device, the signal passes back through the directional coupler into a cryogenic amplifier (Caltech CITLF3; noise temperature $T_n = 4\,\mathrm{K}$ from 10 MHz to 2 GHz) with 40 dB of gain. The output signal, V_{RX}, is then detected using one of three methods: (1) using a network analyzer to measure $S_{21} \equiv 20\log(V_{\mathrm{RX}}/V_{\mathrm{TX}})$ [Fig. 5.6 (c)]; (2) using discrete analog components to demodulate by standard homodyne detection, followed by a fast-sampling oscilloscope (for details see Appendix F.1); (3) using a rf lock-in amplifier (Zurich Instruments UHFLI[6]). Each method has its advantages. Method (1) is convenient for quickly determining if a change in device resistance has an effect on the circuit impedance, which shows up as a change in the magnitude of S_{21}. Method (2) provides fast acquisition of phase maps at different gate configurations, particularly if the device is tuned into the regime of small charging energies. For these applications, methods (2) and (3) are comparable. Method (3) has advantages in simultaneously measuring the phase and magnitude of the reflected signal and is used to quantify SNR of the proximal NW sensors and to detect charge occupancy of Majorana islands tuned to low barrier transmission.

Figures 1(b-d) show a comparison of the LF lock-in measurement and the reflectometry measurement, $S_{21}(f)$, of conductance $g^{(S)}$ of a charge sensor as it is pinched off using electrostatic gates. In the reflectometry measurement, V_{RX} varies rapidly near the resonance frequency $f_{\mathrm{res}} \sim 30\,\mathrm{MHz}$, yielding a dip in $S_{21}(f)$ that depends on the common gate voltage. Line cuts of S_{21} at different values of V_{G^*} are shown in Fig. 5.6 (d). The depth of the resonance changes by approximately 21 dB as the sensor conductance, $g^{(S)}$, is decreased from 0.5 e^2/h to 0.02 e^2/h. In this case, an increasing R_{dev} moves the resonator impedance toward matching.

5.2.3 RF Charge sensing

The charge sensing of a Majorana island is accomplished by placing a second NW (sensor wire), without a superconducting layer, next to the hybrid-NW Majorana device, and capacitively coupling the two NWs with a floating metallic gate [372]. Charge sensing complements conductance and is the basis of parity read-out in several theoretical proposals (e.g., Ref. [317]). The approach is similar to schemes used for spin qubit read-out [280, 373, 374]. In the context of topological qubits, one can generalize the idea used in spin

[6]Electronic Access: https://www.zhinst.com/products/uhfli

qubits known as "spin-to-charge conversion", where a well-isolated quantum variable (spin) is read out projectively by mapping the relevant qubit state onto charge and then detecting charge [206, 9]. In a similar way, the parity of a Majorana island grounded via a trivial superconductor, a well-isolated quantum state, can be read out projectively as a charge state if the island is gated into isolation, forming a topological Coulomb island [317], a process that we denote "parity-to-charge conversion".

A double-Majorana-island (white dashed boxes indicate Al islands) device motived by Ref. [317] is shown in Fig. 5.7 (a). Near the main device, two bare InAs NWs, capacitively coupled to each of the islands via floating gates, serve as independent charge sensors of the two islands. Each sensor is part of an independent RF circuit, with $L_1 = 3.3\,\mu\text{H}$ ($f_{\text{res}} \sim 60\,\text{MHz}$) and $L_2 = 4.7\,\mu\text{H}$ ($f_{\text{res}} \sim 40\,\text{MHz}$). Data acquisition used method (3), described above. Gates V_L, V_M, and V_R were each set to the tunneling regime. Voltages applied to plunger gates LP and RP affect both the carrier density in the semiconductor and the charge offset of each island (see Appendix F.3). Fig. 5.7 (b) shows the charge sensing signal of a $2e$-$2e$ periodic superconducting double-island at $B = 0\,\text{T}$, measured using the right charge sensor (S2), with a plane subtracted to remove cross-coupling of the plungers to the three barrier gates, V_L, V_M and V_R. Periodic $1e$-$1e$ double-island plane-fitted data, measured using the left charge sensor (S1) at finite magnetic field ($B = 0.8\,\text{T}$) parallel to NW axis, is shown in Fig. 5.7 (c). A hexagonal pattern, characteristic of a double-island devices, is readily seen at both zero field and $B = 0.8\,\text{T}$ [Fig. 5.7 (b) and Fig. 5.7 (c)]. Magnetic field B evolution of the right $2e$ periodic island into the $1e$ periodic island regime, with the left island tuned into a Coulomb valley, is shown in Fig. 5.7 (d). The data is differentiated along V_{RP} to improve visibility of the charge transitions.

Previous works [319, 375] investigated nearly $1e$ periodic island charge occupancy, consistent with an emerging topological phase, using conductance. Using reflectometry and charge instead has the advantage of not require electron transport through the device itself. As seen from Fig. 5.7 (d), sensing is consistent with these previous transport studies [319]. We will not focus on peak spacing and motion here, to keep the focus on measurement methods.

Fast charge measurement and signal-to-noise ratios in the $1e$ regime

The signal-to-noise ratio (SNR) for detecting the transfer of a single electron between islands of the double-island device in Fig. 5.7 (a) was investigated as a function of measurement time using the pulsed gate sequence shown in Fig. 5.8 (a). Measurements were done in an applied axial magnetic field $B = 0.6\,\text{T}$, where the charge-stability diagram shows

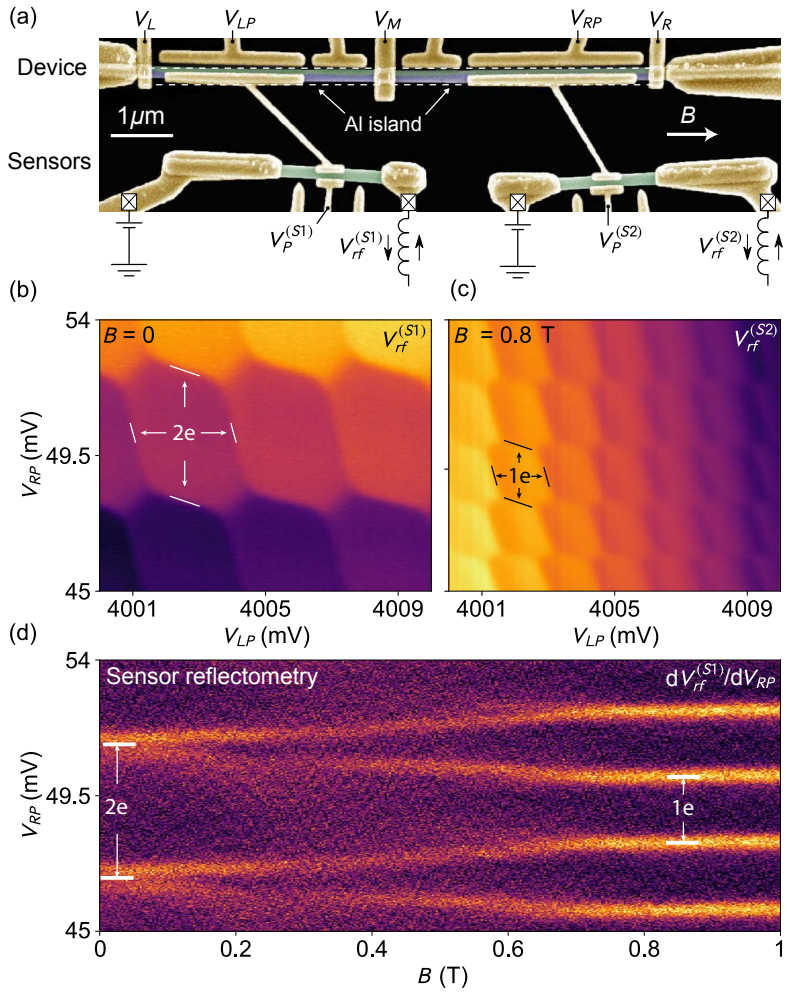

Figure 5.7: (a) Scanning electron micrograph of the device (white dashed boxes indicate Al islands). The voltage tunable tunnel barriers are labeled as V_L, V_M and V_R. Island plunger gates are labeled as V_{LP} and V_{RP} for the left and right island respectively. (b) $2e$-$2e$ periodic superconducting double-island charge stability diagram measured at $B = 0\,\mathrm{T}$ by RF charge sensing with a right sensor. (c) $1e$-$1e$ periodic double-island charge stability diagram measured at $B = 0.8\,\mathrm{T}$ with a left sensor. (d) Charge occupancy of the right island (controlled by V_{RP}) evolution as a function of B. The color map shows the measured RF demodulated signal from the right sensor ($V_{rf}^{(S2)}$) and is differentiated along the V_{RP} axis. Periodicity change from $2e$ to $1e$ in V_{RP} direction is observed as B is increased.

$1e$-$1e$ hexagons. However, in contrast to the tuning in Fig. 5.7 (c), V_L and V_R were set to isolate the double-island, with negligible coupling to the source and drain. Only inter-island transitions [white and red dashed lines in Fig. 5.8 (a)] were measurable in this configuration.

A cyclic pulse sequence was applied to gates LP and RP using an arbitrary waveform generator (Tektronix 5014C), placing the system in three configurations, Initialization (I) for 150 µs, Preparation (P) for 200 µs, and Measurement (M) for a range of times from 1 µs to 50 µs [see Fig. 5.8 (a) inset and Appendix F.2 for details]. The preparation position and duration were chosen to yield roughly equal populations of relaxed and exited populations, which also depended sensitively on the inter-island barrier gate voltage, V_M. Results of the measurement, integrated over the measurement time, were then binned to form histograms showing the distinguishability of N and $N+2$ charge-difference states ($N = N_L - N_R$ is the charge difference, where N_L and N_R are the occupancies of the left and right islands). Note that the number of cycles used to gather histogram statistics does not affect the distinguishability of the two states. More cycles yield a convergence of the histogram to a stable, smooth bimodal distribution. On the other hand, distinguishability of the two populations is affected by the duration at the measurement (M) point. We note that only during the measurement point (M) readout was done by triggering the waveform digitizer card [see Appendix F.2 for details].

The resulting histogram after 10^8 cycles was fit with a sum of two gaussians,

$$P(V_{\mathrm{rf}}^{(S2)} = A_N \exp\left(-\frac{\left(V_{\mathrm{rf}}^{(S2)} - \mu_N\right)^2}{2\sigma_N^2}\right) + A_{N+2} \exp\left(\frac{-\left(V_{\mathrm{rf}}^{(S2)} - \mu_{N+2}\right)^2}{2\sigma_{N+2}^2}\right) \quad (5.3)$$

where A, μ, σ are the amplitudes, means, and standard deviations of the N and $N+2$ charge differences. Measured distributions and best fits to Eq. (5.3) for measurement times $\tau = 1\,\mu\mathrm{s}$ and $\tau = 5\,\mu\mathrm{s}$ are shown in the Fig. 5.8 (b). Separation of the two peaks, ΔV, reflects the sensitivity of the charge sensor, while peak widths σ_N and σ_{N+2} result from measurement noise. We define:

$$\mathrm{SNR} = \frac{\Delta V}{\sigma} \qquad (\text{where } \sigma^2 = \sigma_N^2 + \sigma_{N+2}^2) \quad (5.4)$$

Note that Eq. (5.3) does not include relaxation from N to $N+2$ during the measurement. A more complicated form that includes relaxation during measurement was investigated in Ref. [213]. In the present case, where τ is much shorter than the charge relaxation time, as set by V_M, Eq. (5.3) is valid. The measured SNR as a function of measurement time τ is

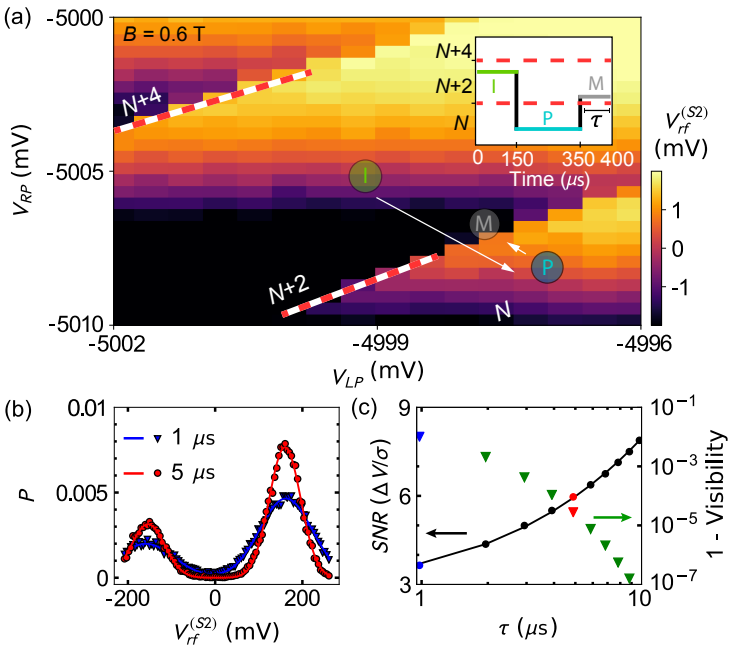

Figure 5.8: (a) $1e$-$1e$ periodic double-island charge stability diagram at $B = 0.6\,\mathrm{T}$ measured using the right proximal charge sensor. The main device was configured such that tunneling to the left/right lead reservoirs is negligible. Only the inter-island transitions are visible with red and white dashed lines. The relative charge occupancy of the islands is marked as N, $N + 2$ and $N + 4$. The pulse sequence used to characterize signal-to-noise ratio is shown in the inset (see main text and Appendix F.2 for description), with positions I, M and P indicated on the charge stability diagram that pulsed gates LP and RP move the system to different gate space positions for a given amount of time. (b) Probability of single shot readout outcomes, P, of demodulated voltage signal $V_{rf}^{(S2)}$ for two different measurement times: $\tau = 1\,\mu\mathrm{s}$ (blue) and $\tau = 5\,\mu\mathrm{s}$ (red), at the measurement point (M) showing a bimodal relative charge state distribution. c) Signal-to-noise ratio (left axis) at the measurement point (M) together with theory fit. Extracted visibility (right axis) from the double gaussian fits (see main text) as a function of measurement time.

shown on the left axis of Fig. 5.8 (c). An SNR > 3 with an integration time of 1 µs was achieved.

Fig. 5.8 (c) shows that SNR increased with measurement time, τ, as expected. The simplest model of this dependence, assuming uncorrelated noise [369], is:

$$\mathrm{SNR}(\tau) = \frac{\Delta V}{\sigma(1\,\mu\mathrm{s})} \left(\frac{\tau + \tau_0}{1\,\mu\mathrm{s}} \right)^{1/2} \tag{5.5}$$

By using fit parameter $\Delta V = 175.3\,\mathrm{mV}$, $\tau_0 = 1.5\,\mu\mathrm{s}$ and $\sigma(1\,\mu\mathrm{s}) = 74.8\,\mathrm{mV}$, the model yields the curve shown in Fig. 5.8 (c), which compares well with the experimentally measured SNR(τ) in the range 1 µs to 10 µs. Another quantity that characterizes the quality of detection is the visibility, *V*, defined as the probability of correctly identifying excited and ground states (N and $N+2$) and is expressed as $V = F_N + F_{N+2} - 1$, where F_N and F_{N+2} are the fidelities calculated following [213] (see Appendix F.2 for details). The resulting dependence of visibility on measurement time, $V(\tau)$, is shown in Fig. 5.8 (c), where again effect of relaxation during measurement are neglected. We find $\sigma(1\,\mu\mathrm{s}) = 0.998$. These results are comparable to previously reported charge detection studies [376, 377, 378, 379, 380].

5.2.4 Conclusions

In summary, we have investigated RF charge sensing and readout of various InAs/Al nanowire devices relevant for Majorana qubits. Charge sensing via a second nanowire capacitively coupled via floating gate to the device allowed charge occupancy in the device to read-out non-invasively and even when visible transport is suppressed through the device. As an application, we followed the evolution of Coulomb charging from $2e$ periodicity to $1e$ periodicity as an axial magnetic field was increased from 0 to 0.6 T, complementing previous conductance measurement of Majorana signatures, without needing to run current through the device. Sensor quality as a function of measurement time was investigated using a pulse sequence that cycled the charge occupancies of the islands. Signal to noise ratio exceeding 3 can be achieved for integration times of 1 µs with visibility $V = 99.8\%$. Presented results show that rf resonant circuits coupled to proximal capacitive sensors can be used for fast and detailed characterization.

Acknowledgments

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Chapter 6

Conclusions

The lofty goal set out at the beginning of this thesis was to develop the architecture of a quantum computer. Unfortunately, as I hope has become clear throughout the course of your reading, reaching the goal of a universal quantum computer is not yet within our grasp. However, what I have aimed to do here is to have made progress towards a general-purpose quantum machine at each level of the quantum computing stack, from the high-level architecture in Chapter 2, to the low level of designing materials for qubits in Chapter 5. As I come to the close of this thesis, I will reflect on the outstanding challenges of realizing a quantum computer, including on areas where I think there is significant risk moving forwards.

6.1 Controlling Qubits

At the top of the stack, in Chapter 2, I discussed the challenges of designing quantum devices that can scale up to a large number of control and readout lines that a useful quantum machine would require. I also presented architectures that lower the requirements on both the number of dc and rf lines and on the power dissipation required to control a quantum device. Today, the effort to build CryoCMOS architectures for controlling qubits has been joined by several companies and groups, including Google [381], Intel and Delft university [382], who are well and truly in the race to build components for scalable cryogenic operation of both superconducting and semiconducting qubits. The aims of each of these efforts are twofold, firstly to bring the footprint of the qubit-classical interface under control, the second being to tame the rapid growth of power consumed at each part of the stack.

In Sec. 2.1, the requirement for control and readout fidelity was also given alongside

the requirements for footprint and power. Pointedly, these two requirements are not listed with the above, since the reality of the modern quantum physics experiment is that the bulky room temperature readout and control hardware is mostly superior to hardware we build for cryogenic operation. This is not surprising, much of the equipment that is currently used for readout and control, be it oscilloscopes, network analyzers, vector sources and so forth, trade-off power and size for flexibility and performance, which are unfortunately not what is needed to scale quantum systems. The challenge for each of the architectures listed in Chapter 2, and for those being developed externally, is to match their classical counterparts with a limited subset of the features available in room temperature hardware. The challenge for physicists, both theoretical and experimental, is to design the next generation of qubit architectures in such a way that they can be easily controlled by cryogenic control hardware which has a limited amount of flexibility. In the medium term, this may mean trading off the best qubit performance for more uniform qubits, or slowing down qubits to relax stringent timing requirements.

Chapter 3 looks at the miniaturization of microwave circulators, touching on the topic of controlling the footprint of the qubit-classical interface. In particular, in Sec. 2.1.2, we discussed the need to isolate qubits from the noise generated by classical readout hardware without adding additional losses into the circuit, as any loss between the qubit and first stage amplifier contributes directly to the SNR of our readout, as per Eq. 2.10. For the qubits presented in this thesis (spin qubits and Majorana based topological qubits), the footprint problem is particularly stark, as readout frequencies of a few hundred MHz would require conventional circulators on to order of 30 cm to 70 cm. Utilizing the slow-traveling edge-magnetoplasmons (EMPs) in the quantum (anomalous) Hall effect, circulators with a size of order a few hundred μm were realized. While isolation of 25 dB was achieved, the insertion loss of this first generation of circulators was not sufficient to be generally useful in qubit experiments. The source of this loss is caused largely by the impedance mismatch between the EMP ($\sim 25\,\mathrm{k}\Omega$) and the $50\,\Omega$ transmission line.

Understanding the source of this insertion loss, however, gives us several solutions towards improving these systems. One obvious, though perhaps not particularly useful answer, is to operate at higher filling factors where multiple parallel paths lead to a reduction in the impedance of the edge, as given by Eq. 1.94. This solution would require either a larger Hall droplet or operation at higher frequencies, nor would this solution be possible for samples using the quantum anomalous Hall effect. Alternatively, as the problem is impedance matching, we can use conventional matching techniques to improve the insertion loss, for example, the use of an LC matching network. A promising approach given in [245] is to

use an intrinsic matching effect in the edges to achieve self-matching at specific frequencies. Such a device geometry promises nearly perfect transmission at these frequencies.

6.2 Scalable Qubit Designs

Designing scalable gate layouts for qubit devices remains an open challenge. In Chapter 4 this is exactly the challenge that we aim to tackle, in two ways. First is the design of a modular layout that allows for a design element to be tiled directly, and is presented in Sec. 4.1. A tiling of this design is shown in Fig. 6.1. For such a technique to be genuinely scalable, several additional technical developments must be made. The first is reliable dispersive gate sensing, as the use of proximal charge sensors in such a design is infeasible. Here such sensors are marked in green. There has been significant progress in the field towards the use of such sensors for spin readout, with many demonstrations of single-shot readout using dispersive gate sensing appearing in the past year [159, 376], albeit with fidelities below what would be necessary for a scalable qubit device. Further work to investigate sources of noise in dispersive gate sensing will be required to scale the technique. The work presented in Sec. 4.2 investigates one such source of noise, however additional work will be necessary to improve the fidelity of gate-based readout techniques.

As gate density is increased, there is an additional difficulty in breaking out the required control lines, as was discussed in Sec 2.1.1. The need for couplers that operate over intermediate and long length scales is partially solved by the use of an intermediate quantum state. Since the publication of the initial work in Sec. 4.1, coherent manipulation of spins via the intermediate quantum state has been demonstrated [20], validating the concept and clearing the path towards large-scale devices. Over long length scales, work performed to couple spin to resonators should allow coherent coupling over mm-length-scales. Although preliminary results demonstrating strong coupling to resonators have been published [61, 148], coherent manipulation of two spins over large length scales has not been shown at the time of publication. In a similar vein, there exists theoretical work suggesting coupling via quantum Hall edge states [289]. However, an experimental demonstration of such a technique has not yet been performed.

In Fig. 6.1 (b), a chip design is shown with the on-chip routing of a total of 168 control lines. The device presented there contains 6 sets of two-qubit devices, each of which is coupled by an intermediate quantum state. As devices grow larger, the requirements for on-chip routing of signals becomes more acute, particularly while wire-bonding is used to interface to the qubit chip. On this device, routing was performed manually with the

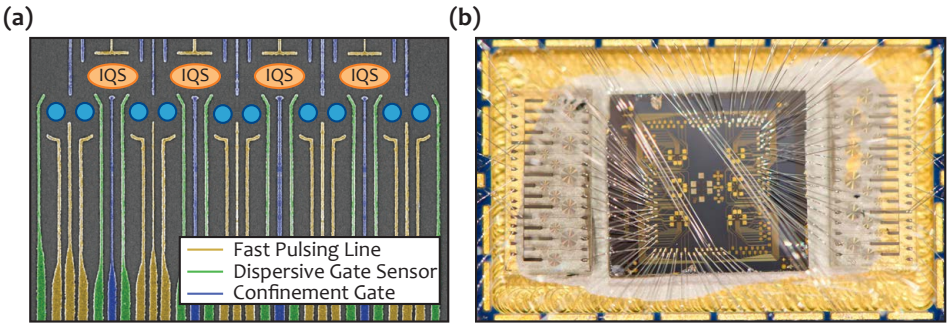

Figure 6.1: (a) The design for a 5 quantum dot device, as presented in Sec 4.1, showing a path towards creating a 1D chain of singlet-triplet qubits. (b) A qubit chip with 6 5-dot devices, controlled by a total of 168 control lines. Superconducting resonators are used for fast, frequency multiplexed charge and gate-based readout. A total of 32 readout channels are bonded on this device.

assistance of the Altium EDA tool, with readout and fast pulsing lines broken out to the edges of the device, to make the bonding of such a device feasible, and to reduce the stray inductance and capacitance of bond-wires. A device with the same design was used in Sec. 2.3 to validate the design of the CryoCMOS architecture, demonstrating the feasibility of on-chip routing for larger devices. Moving forward, the existence of more advanced EDA tools will allow far more of the design process to be automated, which will be crucial as the number of gates on single devices grows.

Built into the discussion about scaling a quantum computer is the need to error correct noisy qubits. The number of operations per gate that must be performed to correct errors, as well as the number of physical qubits required to form an error-corrected logical qubit is a sensitive function of the qubit error rate and snowballs as the fault-tolerance threshold if approached [89, 314]. The construction of qubits with improved error rates is therefore highly desirable, and may, in fact, be necessary for universal quantum computation with as few as 1000 logical qubits. To run Shor's algorithm on a 1024-bit number, for example, would require on the order of 50-million physical qubits with an error rate of 10^{-5}. The use of topologically protected qubits [93], such as Majorana zero modes [21], is the most promising path to realizing qubits with a significantly improved fidelity; however, the materials and techniques challenges, as laid out in Chapter 5 are formidable. Nonetheless, continuing advances in the growth of high-quality materials with large spin-orbit interaction, and high-quality superconductivity [50], and improved designs for scalable Majorana-based devices [146, 361] present exciting opportunities for building truly scalable quantum machines. Some of these issues are explored in Chapter 5, including the design of charge sensors in Sec. 5.2, and the development of fabrication techniques in Sec. 5.1. Moving forward, it is clear that there are some fundamental scientific problems to solve with such

devices to prove that they are indeed possible. Without them, however, it is difficult to see how with current error rates and control schemes, any scalable quantum machine will be possible.

6.3 Closing Remarks

The field today is focused on achieving quantum supremacy, that is to run an algorithm on a quantum computer that could not feasibly be simulated on a classical machine. The consensus at the time of writing is that this will be some variant of Boson sampling [136], performed on approximately 50 qubits [383, 384, 385], with companies such as Google, IBM, Rigetti and Ion-Q each having announced their intention to reach this goal imminently. However, even though IBM announced its 50 qubit processor in November 2017 [386], Google announced its Bristlecone chip containing 72 qubits at the March Meeting of the American Physical Society in 2018 [381, 387] and Intel announced its 49 qubit quantum processor in January at CES 2018 [388], the goal of quantum supremacy lies tantalizingly just out of reach. From a scientific standpoint, this is perhaps not surprising. There is plenty of evidence that even for the problem of Boson sampling, the quality of qubits must be higher than expected [389, 390], the connectivity of qubits must be relatively high [135], and that the number of qubits might be larger than thought [391]. From the standpoint of a quantum physicist and engineer, this represents an exciting challenge, one that calls for further incremental improvement of qubits, for new designs that extend the connectivity of qubits and for improved methods of readout and control. From the perspective of the public and the community, however, there lies some danger, wherein we run the risk of hitting a "Quantum Winter." This would be a period analogous to the "AI Winter" [392], a period in the history of artificial intelligence, where persistent hype and an over-selling of the promise of AI, followed by a failure to deliver on these promises, led to a period of reduced funding and interest in the field. The reason that quantum supremacy has not yet been achieved may not be surprising to those in the field but has regularly been a source of surprise to members of the public.

If we assume, however, that we reach the goal of quantum supremacy in the reasonably near future, there are two roadmaps to a general-purpose quantum machine, one which presents great opportunities for quantum computing researchers, the other which presents a risk that we must confront to ensure that development continues sustainably. These two roadmaps are shown in Fig. 6.2, and relate to the demonstration of quantum advantage, that is the solution of a problem with a quantum computer that would not have been possible

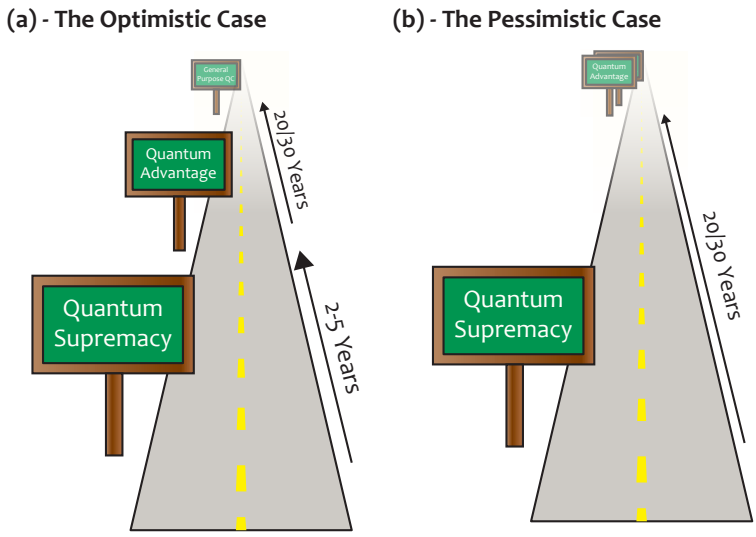

Figure 6.2: The possible paths by which a quantum computer is achieved. (a) In the optimistic case, a few years after quantum supremacy is reached, an algorithm demonstrating quantum advantage is achieved, leading to continued interest in the field. (b) In the pessimistic case, even though quantum supremacy is reached, the demonstration of an algorithm that shows quantum advantage doesn't occur until a general-purpose quantum machine is available.

without one. Equivalently, the question is "what is interesting in the NISQ era" [134]? In Fig. 6.2 (a), the answer is "something." This may be Variational Quantum Eigensolvers (VQEs) [138], it may be some form of machine learning [393], however there is yet every chance that even these algorithms may turn out to be classically tractable [394, 395], or require error correction to the extent that we are pushed to the realm of needing a general-purpose quantum machine [141]. In this case, we may live in a world where Fig. 6.2 (b) is true, and there is a long period where a quantum computer is simply a toy. Such a situation would require continued long term investment, and is not a future that we should ignore in our current push to build a quantum computer.

Despite the risk, it is also true that at no other point in the history of quantum computing has there been such high awareness of the magnitude of the problems that must be solved. There is constant development in all areas of the stack, from proposals for quantum programming languages to improved equipment for quantum experiments to even new types of qubits. Together, all of this convinces me that, barring an extraordinary no-go result, a useful quantum computer is not only achievable but will be realized in the next 20 or so years. I can't predict the form of such a quantum computer, nor how it will be used, however regardless of its final form, it will confer benefits on all of humanity.

Appendix A

Nanofabrication

In this appendix, I will briefly outline the steps followed to fabricate the devices presented in this thesis. Although there are several types of devices presented, including quantum dots, nanowire devices, and Hall bars, in each case the techniques used for each chip are adapted from the steps laid out below. The significant differences in cleanroom tooling and safety protocols in each cleanroom mean that several procedures will likely need to be adapted to gain similar results, however, where possible I've tried to include all the details that would be necessary to tailor the process to your cleanroom.

A.1 Fabrication Overviews

A.1.1 Quantum Dot Nanofabrication

1. **Cleave Chips** (Sec. A.2.1)
2. **Gallium Removal**: Remove gallium on the backside of wafer. (Sec. A.2.2)
3. **Chip Clean and Bake**: Remove any organic solvents and adsorbed moisture. (Sec. A.2.3)
4. **Alignment Mark Deposition**: Deposit TiAu alignment marks which will be our reference for all future fab steps. (Sec. A.2.9)
5. **Mesa Etch**: Define the active region of the device by etching away the 2DEG using a dilute H_3PO_4 solution. (Sec. A.2.7)
6. **Ohmics Deposition**: Deposit AuGe ohmics and anneal into wafer. This step should be performed as soon as possible after the etch, preferably on the same day. (Sec. A.2.10)

7. **Ohmic Contact Deposition**: Deposit bondpads for ohmic contacts. (Sec. A.2.9)
8. **Global Oxide Deposition**: Deposit a global Al_2O_3 or HfO_2 oxide using ALD as a insulating barrier. (Sec. A.2.11)
9. **Gate Deposition**: Deposit surface gate pattern. (Sec. A.2.9)
10. **Gate Contact Deposition**: Deposit bondpads for surface gates. (Sec. A.2.9)

A.1.2 InAs Hall Bar Nanofabrication

1. **Cleave Chips** (Sec. A.2.1)
2. **Chip Clean and Bake**: Remove any organic solvents and adsorbed moisture. (Sec. A.2.3)
3. **Mesa Etch**: Define the active region of the device by etching away the 2DEG. Note that if Al is grown on the surface, this must be removed (Sec. A.2.8) prior to the mesa etch. (Sec. A.2.7)
4. **Al Removal**: Etch away excess Al from the surface of the hall bar. (Sec. A.2.8)
5. **Global Oxide Deposition**: Deposit a global Al_2O_3 or HfO_2 oxide using ALD as a insulating barrier. (Sec. A.2.11)
6. **Gate Deposition**: Deposit surface gate pattern. (Sec. A.2.9)

A.1.3 GaAs Hall Bar and Circulator Nanofabrication

1. **Cleave Chips** (Sec. A.2.1)
2. **Gallium Removal**: Remove gallium on the backside of wafer. (Sec. A.2.2)
3. **Chip Clean and Bake**: Remove any organic solvents and adsorbed moisture. (Sec. A.2.3)
4. **Mesa Etch**: Define the active region of the device by etching away the 2DEG using a dilute H_3PO_4 solution. (Sec. A.2.7)
5. **Ohmics Deposition**: Deposit AuGe ohmics and anneal into wafer. This step should be performed as soon as possible after the etch, preferably on the same day. (Sec. A.2.10)
6. **Gate Contact Deposition**: Deposit bondpads for surface gates. (Sec. A.2.9)

A.2 Detailed Process Recipes

A.2.1 Cleave Chips

In the following section, I will only describe the process for manual cleaving of chips using a diamond tip pen. For more precise jobs, I recommend the use of a scribing tool which can better align and scribe chips. For most III-V materials (100 orientation), you will only be able to scribe parallel to or perpendicular to the wafer flat. Note that all steps should be performed on a cleanroom wipe which is to be disposed of in a contaminated (III-V) waste bin once the process is complete, due to the hazardous nature of III-V materials.

1. Find wafer in fabrication logbook. Note previously scribed pieces and orientation. Select a piece to scribe. Record selected chip orientation and position in fabrication logbook.

2. Line up the chip with the edge of a metal ruler. Using a diamond pen, make a small scratch (< 1 mm) to the wafer edge.

3. Balance the chip on the edge of a glass side with the scratch aligned to the edge of the slide.

4. Press the overhanging section of the chip with filter paper or a cleanroom wipe to cleave the chip. The cleave should be clean and along the scratch direction.

5. Choose a corner of the chip as a reference for future steps. Make a drawing of the scratches/features of the chip relative to the corner in the fabrication of logbook. Note the wafer orientation relative to the chip for future reference.

6. Put contaminated filter paper/wipes in the contaminated waste bin, and glass slides into the sharps disposal.

A.2.2 Gallium Removal

Ga metal is used as a sticking layer and thermal contact in the MBE chamber during heterostructure growth. When wafers arrive from growers they often have this sticking layer still on their backsides, which must be removed before further processing as it has a melting point of 29 °C and tends to contaminate process equipment and coat the surface of glassware. We use the low melting point of Ga to physically remove it using q-tips followed by an optional HCl dip to etch away any remnants. The HCl dip is useful to obtain the lowest possible ohmic resistances and is used more for Hall chips than quantum dots.

1. Heat a small amount of NMP to 80 °C in the designated NMP-(Gallium) beaker. It should be sufficiently full to cover the chip that will be placed in step 3. Prepare a small amount of NMP in an NMP-(Clean) beaker.

2. Deposit 1-2 drops of PMMA onto the bottom third of a clean glass slide.

3. Carefully place the GaAs chip face down on the PMMA droplet, attempting to keep the back dry and free of resist.

4. Place the glass slide on a 95 °C hotplate for at least 1 min.

5. Using a cleanroom q-tip, gently wipe the Ga from the back of the chip, replacing the q-tip as necessary. Ensure that the chip does not move during this process as movement may damage the chip surface. The chip may be placed on the hotplate for an extra 20 s to 30 s if the Ga has dried.

6. Place the glass slide in the heated NMP-(Gallium) beaker such that it is covered. Gently nudge the chip after 30 s until it is free of the slide and discard. Transfer the chip into the second NMP-(Clean) beaker.

7. **Optional:** If at this point the gallium is sufficiently removed we may proceed directly to the chip clean and bake (Sec. A.2.3). Otherwise, transfer the chip to an IPA-(Clean) beaker with a small amount of IPA and sonicate for 1 min.

8. Spin and bake AZ6612, PMMA, or a similar photoresist (Sec. A.2.5). In general, ZEP or CZAR should be avoided for acid etches.

9. Stir the chip in a 37 % HCl solution for 2 min to 3 min.

10. Rinse the chip in distilled H_2O for 30 s.

11. Proceed to chip clean and bake (Sec. A.2.3)

A.2.3 Clean and Bake

The clean and bake step is used to remove any surface contaminants that may have been introduced in shipping and handling, as well as to remove any surface moisture. Each solvent step should include some sonication during the 5 min soak. Sonication may be performed for the full 5 min if desired. Tweezers should be washed in between each transfer step to prevent cross-contamination.

Note: NMP easily damages Al if the solvent has absorbed any moisture from the air. For materials with thin-film epitaxially grown Al, use an alternative solvent such as 1,3-Dioxolane.

1. Place chip, face-up, in a small amount of NMP at 80 °C, in an NMP-(Clean) beaker for at least 5 min, with sonication.

2. Transfer the chip to Acetone in an Acetone-(Clean) beaker for at least 5 min, with sonication.

3. Transfer the chip to IPA in an IPA-(Clean) beaker for at least 5 min, with sonication.

4. Remove the chip from the IPA and dry with nitrogen on a fresh cleanroom wipe.

5. Bake the chip at 200 °C for 5 min.

A.2.4 Resist Strip

This process is used to strip resist of the surface of a chip, either due to a failed processing step or after a mesa etch (Sec. A.2.7). In the case that the strip is being performed during spinning and before the resist has been baked, it is usually sufficient to perform a quick 30 s Acetone/NMP dip rather than the longer times prescribed below, as the resist will not be hardened. Sonication may be used to assist with the strip as long as fine gates have not been evaporated. Otherwise, sonication often damages these gates.

Note: ZEP, CZAR and other styrene-based resists are *NOT* compatible with Acetone. For these samples, NMP or an alternative solvent must be used.

Note: NMP easily damages Al if the solvent has absorbed any moisture from the air. For materials with thin-film epitaxially grown Al, use an alternative solvent such as 1,3-Dioxolane.

1. Place chip, face-up, in a small amount of NMP at 80 °C, in an NMP-(Clean) beaker, or Acetone in an Acetone-(Clean) beaker for at least 3 min.

2. Transfer the chip to IPA in an IPA-(Clean) beaker for at least 30 s.

3. Remove the chip from the IPA and dry with nitrogen on a fresh cleanroom wipe.

Process	PMMA A3	ZEP520A	AZ6612	LOR 5B
Step 1 (rpm)-(s)-(rpm s^{-1})	500-5-1000	500-5-1000	500-5-1000	500-5-1000
Step 2 (rpm)-(s)-(rpm s^{-1})	9000-5-4000	9000-5-4000	10000-20-4000	10000-4-4000
Step 3 (rpm)-(s)-(rpm s^{-1})	4000-45-4000	4000-120-4000	4000-20-4000	4000-60-4000
Bake (°C)-(s)	180-60	180-120	95-60	170-300
Approx. Thickness (nm)	80	220	800 - 1000	600 - 800

Table A.1: Spin recipes for various resists. Each step gives a spin speed, a spin time, and an acceleration, separated by dashes. Thicknesses quoted are approximate and will vary depending on chip size and resist age and temperature.

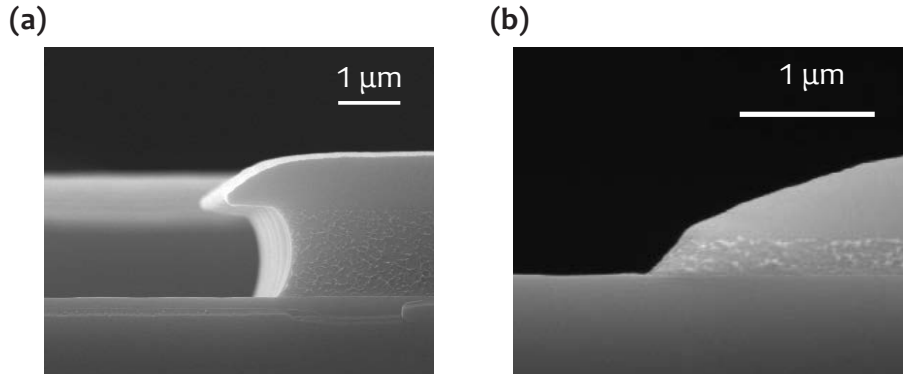

Figure A.1: Edge profiles of LOR 20B/AZ6612 (a) or LOR 5A/AZ6612 (b). The left image shows a significant undercut, suitable for deposition of thick metal layers, while the right image shows a smooth edge profile suitable for etching, and caused by the low solubility of LOR 5A relative to exposed AZ6612 in MIF300 developer.

A.2.5 Resist Spin

Spinning resist aims to create a uniform thin film of a photoresist or electron-beam resist. Depending on the sort of process we wish to run, with the developed resist, we may have different requirements for the edge profile. For evaporation of a metal stack with a liftoff process, we aim to create an undercut such that there is a break in the metal, with a height larger than the metal thickness we wish to evaporate. This can be achieved using a single, thick resist layer, which will, in general, have an undercut profile due to the scattering of electrons or light through the resist, or by the use of a bi-layer resist stack, with a soluble polymer such as LOR-B or MMA as the underlayer. An example of a suitable undercut is shown in Fig. A.1 (a).

For an acid etch, we would, in general, prefer a smooth edge profile with no undercut to ensure the continuous flow of fresh acid over the surface of the wafer and to ensure that acid is easily rinsed away once the etch is complete. This is achieved by a post-development bake which will reflow resist at the edges of the developed region, and re-adhere resist to the surface of the wafer. An example of a smooth edge profile is shown in Fig. A.1 (b).

Spin parameters for various resists are given in Table A.1, which are valid only for small (2.5×5 mm or 5×5 mm) samples. A high-speed spin is used at the beginning of the spin to minimize the effect of the edge bead, which is a thick region of resist around the edges of the sample caused by surface tension. However, this spin is unsuitable for large samples or wafers and will lead to variable resist thickness across the wafer, or, in the worst case, the wafer being flung from the chuck.

Hint: Squeezing the sides of the rubber puck makes it easier to move chips around. If the chip is not moving after the spin, try squeezing the puck in a few locations and try again.

Note: If a resist was refrigerated, it must be allowed to warm to room temperature before use. Apart from the viscosity changing with temperature, leading to an unpredictable resist thickness, the cold resist will condense moisture from the air, contaminating the resist for future users.

1. Clean the small rubber puck for chips with Acetone on a cleanroom wipe.
2. Attach your chip to the small rubber puck. Attempt to center it as much as possible.
3. Take a few drops of resist with a pipette from the small resist bottle, making sure to not take from the bottom of the bottle.
4. Dispense 2/3 drops of resist on the surface of the chip and begin the spin as soon as possible.

Process	PMMA A3	ZEP520A	AZ6612
Solvent	MIBK:IPA 1:3	o-Xylene	MIF-300 (TMAH)
Develop Time (second)	40	50	50
Rinse	IPA	MIBK:IPA 1:3	H_2O
Rinse Time (second)	20	10	30
Second Rinse	-	IPA	-
Rinse Time (second)	-	10	-

Table A.2: Development Recipes for various resists.

5. After the spinning is complete, inspect the chip for a uniform spin. If the spin is not uniform or has picked up particulates, clean the resist (Sec. A.2.4).

6. Bake the chip for the appropriate time.

7. Clean the small rubber puck before finishing. Dispose of the pipette, do not replace remaining resist.

A.2.6 Resist Develop

Developing resist is the process of dissolving exposed (or unexposed for a negative tone resist) regions of resist to create a mask on the surface of your sample. Depending on the chemistry of the process, the solvent and times vary. For the resist we've used, development times are summarized in Table A.2.

Note: Plasma ashing samples after the deposition of fine gates has been known to cause static damage.

1. Prepare beakers for each of the solvents necessary for that resist. There should be a dedicated, labeled beaker for each one.

2. Place chip into each solvent for the requisite time, swirling the chip continuously. Try to move the chip between beakers quickly but smoothly at each step.

3. Dry the sample with the N_2 blowgun for ~ 30 s.

4. If possible, plasma ash the sample for between 5 min to 25 min for a photoresist, or 20 s to 60 s for an e-beam resist, immediately before the next processing step.

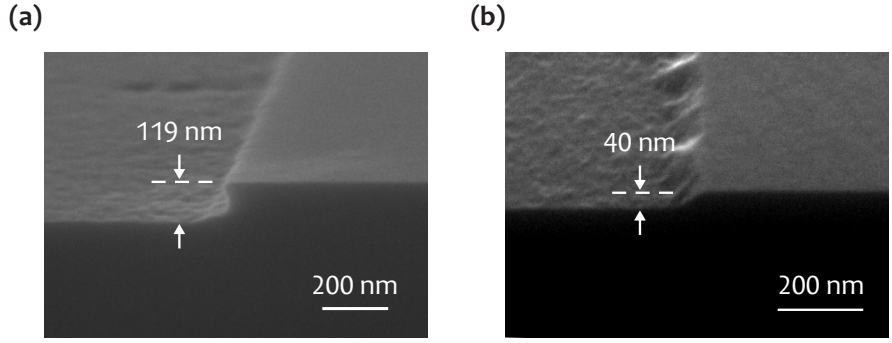

Figure A.2: A comparison of the etch profiles of H_2SO_4 in (a) and H_3PO_4 (b). While H_2SO_4 leads to an anisotropic etch and a significant undercut, the H_3PO_4 leads to an isotropic etch and a smooth sidewall.

Material	Etch Rate (Å s^{-1})
Intrinsic GaAs	12.1
GaAs Heterostructure	15.9
InAs Heterostructure	18.7

Table A.3: Dilute phosphoric acid (5:1:50 H_3PO_4:H_2O_2:H_2O) etch rates

A.2.7 Mesa Etch

It is often necessary to define the sections where the 2DEG exists. For Hall measurements, this is used to define the shape of the Hall bar. For quantum dots, this is used to isolate devices from each other when multiple devices exist on a single chip, and to reduce parasitic capacitance along readout or pulsing gates. It is also possible to reduce crosstalk between gates by removing the 2DEG below as much of the length of the gate as possible[208].

The use of a weaker phosphoric acid solution was chosen after several years of using a sulphuric acid solution as we found that the strength of the sulphuric acid was leading to an anisotropic etch with a significant undercut. This had, in past devices, led to issues making continuous gates over the edge of the mesa. The use of phosphoric acid in comparison leads to an isotropic edge with a smoothly sloping sidewall, making the formation of continuous gates over the mesa edge easier. A comparison of the etch profiles of H_2SO_4 and H_3PO_4 is given in Fig. A.2.

An additional bake is included in the processing after development to remove any undercut that may have developed in the resist during development. In addition, the drying of the developer has been known to cause the resist to lift from the surface of the wafer near

features, which is repaired by this post-baking step. The addition of this step creates both smoother etch edges and better-controlled edge thicknesses.

1. Spin and bake AZ6612, PMMA, or a similar resist (Sec. A.2.5). In general, ZEP or CZAR should be avoided for acid etches.

2. Expose the mesa pattern using the optical mask aligner or electron-beam lithography. Develop using the appropriate recipe (Sec. A.2.6).

3. Postbake the resist using the same bake as the initial bake (see Table A.1) to remove any undercut and re-adhere the resist to the surface of the chip.

4. Prepare a solution dilute phosphoric acid solution of H_3PO_4:H_2O_2:H_2O in a 5:1:50 ratio. Remember that acids should always be added to water, not the other way around. Stir thoroughly with PTFE (acid) tweezers, and leave to thermalize for ~ 30 min.

5. Measure the resist height with a surface profilometer (Dektak in our case). Record in several locations.

6. Pour some of the dilute phosphoric acid solution into a small etch beaker. Etch the chip for the appropriate time (use Table A.3 for standard etch rates) using Teflon tweezers and stirring continuously. I usually aim $\sim$ 10 nm below the depth of the 2DEG. Etching too deeply can make it challenging to run gates to the surface of the 2DEG.

7. Rinse in distilled H_2O for a minimum of 30 s and dry with nitrogen on a clean wipe.

8. Measure the new height of the resist using a surface profilometer in the same locations as before. The etch depth is the difference between the two measurements. If the depth is insufficient, repeat steps 5-7.

9. Strip resist (Sec. A.2.4).

A.2.8 Al Etch

For InAs devices, aluminum must be selectively etched away to define device geometries. This is accomplished using a Transene-D based wet etch. This process is highly sensitive to both temperature and etch time, and hence, care must be taken when performing this

step if you wish to achieve reproducible results. For this reason, a PID controller, glass thermometer, and stirrer are necessary for high quality etches.

For a thin (8 nm) layer of epitaxially grown Al, we have had success using a 11 s etch followed by two 11 s H_2O rinses, however, this process must be optimized for local conditions.

Note: Transene-D will begin to degrade at temperatures above $\sim 50\,^{\circ}C$. Care must be taken while heating to ensure this temperature is not exceeded, including at the base of the beaker. As such heating must be quite slow.

Note: Transene-D oxidizes if stirred too vigorously. The stirrer should be set to the lowest possible speed and should not visibly agitate the surface of the etch solution.

1. Spin and bake AZ6612, PMMA, or a similar resist (Sec. A.2.5). In general, ZEP or CZAR should be avoided for acid etches.

2. Expose the mesa pattern using the optical mask aligner or electron-beam lithography. Develop using the appropriate recipe (Sec. A.2.6).

3. Postbake the resist using the same bake as the initial bake (see Table A.1) to remove any undercut and re-adhere the resist to the surface of the chip.

4. Prepare a solution of Transene-D, heated to 47.5 °C with a PID controller, and stirred at low speed. Ensure this temperature is stable before beginning the etch.

5. Prepare two beakers of DI-water for the rinse. Prepare a beaker of Acetone to strip the resist as soon as the etch is complete.

6. Immediately before commencing the etch, stop the stirrer.

7. Dip the sample in Transene using PTFE tweezers, agitating continuously. Once complete, immediately transfer to first water beaker, again agitating continuously, followed by the second water beaker.

8. Transfer the chip as soon as possible to Acetone to strip the resist. Restart the stirrer.

9. Follow the steps for stripping resist to finish (Sec. A.2.4).

A.2.9 Metal Deposition

Deposition of metals is a repeated step for several of the processes. For all of the work presented in this thesis, we use a liftoff based process; however, I will note that for sputtered metals or ultra high-Q resonators such a process may be unsuitable.

Ohmics

Step	Metal	Thickness (Å)	Deposition Rate (Å s^{-1})
Layer 1	Ni	50	2
Layer 2	Ge	x (350)	5
Layer 3	Au	$2x$ (700)	5
Layer 4	Ni	180	2
Layer 5	Au	500	5

Fine Surface Gates

Step	Metal	Thickness (Å)	Deposition Rate (Å s^{-1})
Layer 1	Ti	80	2
Layer 2	Au	120	5

Contact Gates and Alignment

Step	Metal	Thickness (Å)	Deposition Rate (Å s^{-1})
Layer 1	Ti	120	2
Layer 2	Au	1000 - 2000	5

Table A.4: Evaporator recipes for various processes. Note that for ohmics, the depth of the middle two layers should be varied depending on the depth of the 2DEG, such that $3x \approx d$. Values used successfully for a 91 nm are given in brackets.

For thin gates, it is necessary to evaporate metals at a reasonably high rate, as slower deposition rates lead to larger grain sizes, which can cause discontinuities to appear in small gates. Although in general, a faster deposition is preferable, there are limits to how fast various metals will evaporate with a stable rate. Some recommendations are given in the Table A.4, however, these should be based tools (and the experiences of others using it) and tuned accordingly.

Metal compatibility should also be considered when choosing the tool to use for various evaporations. For tools handling CMOS processes, for example, the use of gold is unsuitable. For evaporators focused on ultra high-Q resonators, nickel, and other magnetic materials will decrease transition temperature, but this may not be a limiting factor for your process.

Metal thicknesses for several processes are given in Table A.4.

Note: ZEP, CZAR and other styrene-based resists are *NOT* compatible with Acetone. For these samples, NMP or an alternative solvent must be used.

Note: After deposition of fine gates, the use of sonication can cause damage to gates. Limit sonication to about 15 s at low power and use only if necessary.

Note: Drying your sample before liftoff is complete will cause unwanted sections of metal to adhere to the surface of your chip, making them very difficult (if not impossible) to remove.

1. Spin and bake photoresist or e-beam resist (Sec. A.2.5).
2. Expose the pattern using the optical mask aligner or electron-beam lithography. Develop using the appropriate recipe (Sec. A.2.6).
3. Mount samples in the evaporator. You can optionally mount samples to a glass slide if features exist close to edges along all 4 sides of the chip. In this case, use a drop of PMMA A3 on a glass slide, place the chip on the drop and bake for 60 s at 90 °C or until the resist is dried. Avoid higher temperatures for risk of reflowing resist and melting the undercut.
4. Pump evaporator until sufficiently low pressure and evaporate according to the given procedure for your evaporator.
5. Allow chip to cool for $\sim$ 5 min before venting. Remove samples.
6. Place a small amount of NMP into the NMP-(Liftoff) beaker and heat to 80 °C. Leave for 30 min to 60 min.
7. Sonicate for $\sim$ 30 s to clear remaining metal of the surface. Visually inspect while wet, leaving for additional time if liftoff is not complete.
8. A spray with Acetone or IPA from a squeeze bottle may assist you in removing stubborn sections of metal.
9. After liftoff is complete, place the chip in the IPA-(Liftoff) beaker for 3 min.
10. Remove chip and dry with N_2 blowgun on a cleanroom wipe.

A.2.10 Ohmics Deposition

Ohmic contacts are used to make contact to the 2DEG from the surface of the chip and are formed using a eutectic stack of AuGe. Nickel is used as a sticking layer to the surface of the GaAs and a diffusion barrier which allows only Ge to diffuse into the semiconductor, followed by Au:Ge in a 2:1 ratio, which forms our eutectic alloy. A further Ni and Au cap is used to prevent oxidation. The exact stack for a 91nm 2DEG is given in Table A.4. Modify

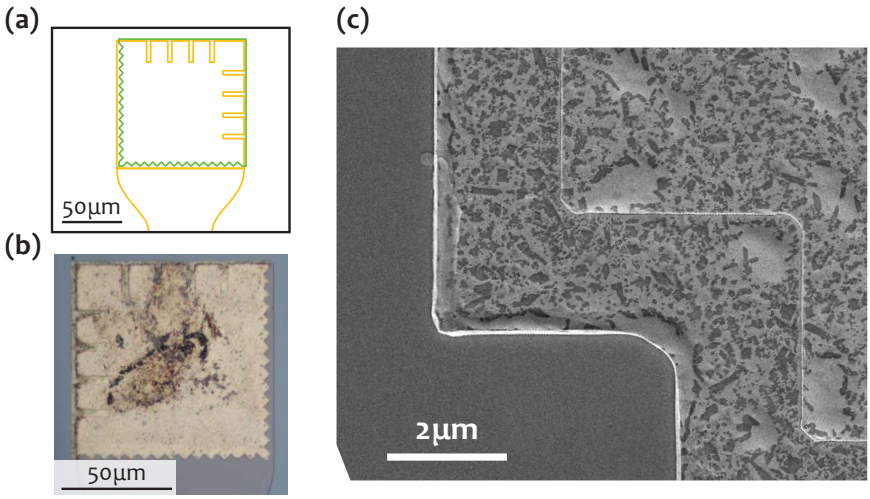

Figure A.3: (a) Sample ohmic design, showing the mesa in yellow and the ohmic metal stack in green. The mesa contains slices to increase the ohmic contact with the edge along multiple crystallographic orientations, and the ohmic metal extends past the edge. (b) Optical micrograph of a low resistance ohmic. Note the bubbly appearance of the surface. An ovoid mark is visible in the center of the pad where a bond was placed while testing the contact. (c) SEM image of an annealed ohmic.

the thickness of the central Ge and Au layers if using a shallower or deeper 2DEGs. The contact to the 2DEG is made by a degenerately Ge doped section of semiconductor that forms under the metal stack [396, 197].

The design of ohmics is particularly crucial for quantum Hall samples, where making good contact to the edge along multiple crystallographic orientations is crucial, particularly at high field. Also, to obtain the lowest possible ohmic resistance, we have found it necessary to make the ohmic stack extend over the edge of the mesa. This allows the ohmic to anneal in along the sidewall to improve the area of the contact. We use a design adapted from [397]. A sample of such an ohmic is given in Fig. A.3.

Annealing is performed in a rapid thermal annealer, in our case, the MILA-5000, in an atmosphere of forming gas (4% H_2:96% N_2). We have found it necessary to place samples on a SiC heat spreader, which contains an integrated thermocouple to measure the temperature of chips during the annealing process accurately. For devices with a deeper 2DEG (i.e., 400nm for high mobility Hall samples) it may be necessary to increase the anneal time to account for the increased depth.

Good ohmics appear uniformly bubbly after annealing, with no dark spots. The surface of the sample should not change, and color change may indicate contamination on the surface of the chip before annealing. I have found a round of plasma ashing immediately preceding the anneal may be necessary to remove contamination.

Step	Temperature (°C)	Time (s)
Step 1 (Ramp)	130	8
Step 2 (Hold)	130	130
Step 3 (Ramp)	450	20
Step 4 (Hold)	450	90

Table A.5: Recipe for the ULVAC MILA-5000 rapid thermal annealer, using a forming gas (4% H_2:96% N_2) atmosphere. Note that the PID parameters must be appropriately tuned to ensure temperatures are reached rapidly without overshoot.

1. Evaporate and lift off ohmics pattern (Sec. A.2.9). Ensure the surface is clear of contaminants. If in doubt, the chip may be plasma ashed prior to loading into the annealer.

2. Vent the annealer with nitrogen for 3 min before loading sample. Following sample loading, purge the chamber with forming gas for 3 min before beginning the process.

3. Anneal chips in an atmosphere of forming gas (4% H_2:96% N_2), following instructions for the local tool. A sample set of parameters is given in Table A.5, which has been found to give low resistance ohmics in our lab.

4. After the anneal is complete, immediately purge the chamber with nitrogen gas at high flow to assist with cooling. Allow the sample to cool to 50 °C before unloading.

A.2.11 Oxide Deposition (ALD)

ALD is deposited on samples as an insulating dielectric, either to minimize leakage to the donor layer which is hypothesized to be a source of charge noise [47], or as an insulating layer for multi-layer devices. The addition of this step to spin qubit devices is a reasonably recent addition to our fabrication process, and over time, this process has been optimized to increase the quality of the dielectric that is grown. Initially, we had been using a liftoff process [398], however, such a process was found to grow measurably worse quality oxide films, due to the low temperature of growth required for resist compatibility (90 °C to 150 °C), and contamination due to resist in the process chamber.

Our current process, therefore, deposits a global oxide, grown at a minimum temperature of 200 °C. We make contact to lower layers either by bonding through the oxide or using a selective Al etchant to remove sections of the oxide. In general, the highest possible growth temperature will result in the highest oxide quality, where materials compatibility is taken into account (In will precipitate out of InAs above 250 °C for example).

For devices in this thesis, we've grown both Al_2O_3 and HfO_2 oxides using TMA and TDMA-Hf as precursors and H_2O as an oxidizing agent. In general, we've not had success with O_3 as an oxidizer, with the quality of film grown lowered relative to H_2O. Although there will be variance by tool and growth temperature, as a rule of thumb, we've found 100 cycles of TMA at 200 °C to grown approximately 8 nm of oxide.

Note: Avoid placing samples with resist in the growth chamber as it leads to significantly decreased oxide quality.

1. Set the chamber temperature to the correct growth temperature for the growth. Allow the chamber temperature to settle before loading your sample.

2. Set the correct number of cycles for your oxide growth. The thickness of oxide grown per cycle with vary depending on the tool and the temperature of the growth.

3. Load your sample, and a blank silicon piece, into the growth chamber. For load locked tools, allow the stage to reach the correct temperature before beginning the process.

4. Run the ALD growth program. It is usually worth checking that there are pressure spikes for the first few cycles to ensure precursors have not been depleted.

5. Once the process is complete, unload the samples. Check the depth of deposited oxide using an ellipsometer on the blank Si chip and record this value.

Appendix B

Wiring and Setup

In this appendix, I briefly go through the critical components of the wiring of a dilution refrigerator. Throughout my Ph.D., I have been lucky enough to see the lab grow from one to seven fridges. This has given me plenty of opportunities to optimize the wiring of a refrigerator to minimize the electron temperatures seen by devices. It has also allowed me to test a large selection of hardware and confirm that it does or does not work cold. The fridge wiring I present in Fig. B.1 is a setup optimized for operation on spin qubits, however, for other types of experiments, the values of the attenuators and filtering may be tweaked to trade-off heating and thermal photon population [142].

High-frequency coaxial lines are used in both the readout circuit and for pulsing qubits. These are fed into the fridge with Huber & Suhner hermetic feedthroughs, rated to 18 GHz (H & S 34_SMA-50-0-3/111_NE), and are in my experience the highest quality hermetic connectors around. On the 4K stage, as the o-ring will pass through its transition temperature, the connectors must be soldered into place, or run down a dedicated port directly into the inner vacuum chamber. On BlueFors or Oxford fridges where there is no inner vacuum chamber, this is not an issue.

For most fridges that we've wired ourselves, we've used 0.086-inch diameter coax, with differing inner and outer conductors depending on the location. Between temperature stages, the choice of material for coaxial cables is crucial to minimize heat transfer. In my experience, a stainless steel outer with a beryllium-copper inner conductor is sufficiently insulating (UT-085-B-SS), although stainless steel inner conductor coax is available and used on some setups (UT-085-SS-SS). Premade cable assemblies are generally more reliable and can be ordered from rf-coax or Rojone, (see for example the part numbers given in Fig. B.1). In the case that manual assembly is required, the Radiall 9401-1583-010 SMA connectors do not require soldering of the inner contact and are highly reliable. On readout lines where

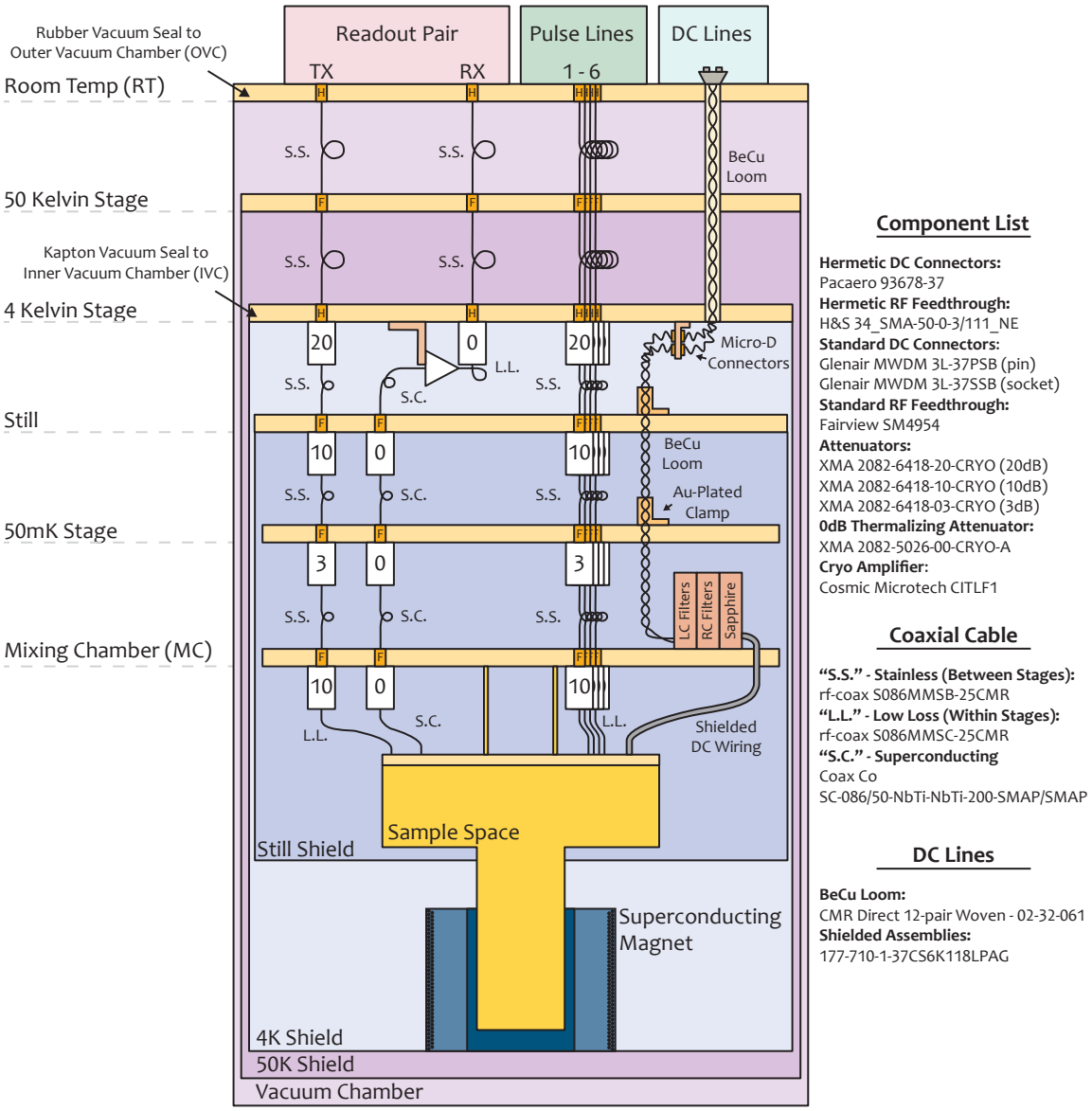

Figure B.1: The standard fridge wiring for a spin qubit experiment. Values for attenuators are chosen to trade-off power dissipation from pulses and the thermal photon population. Components which are known to work cryogenically are given on the right of the figure, although the list is by no means exhaustive.

	LC Filter	RC Filter
Stage 1	Minicircuits LFCN-5000	Minicircuits LFCN-80
Stage 2	Minicircuits LFCN-1450	R = 500 Ω, C = 2200 pF
Stage 3	Minicircuits LFCN-80	R = 1200 Ω, C = 1000 pF

Table B.1: Component values for dc filtering. The LC filter has a cutoff of 80 MHz, while the RC filter has a cutoff of $\sim$ 70 kHz.

any attenuation of the signal leads to an increased noise temperature (see Sec. 2.1.2), superconducting coaxial lines are used. Soldering NbTi is unfortunately almost impossible; in this case, premade assemblies are used exclusively. These are available from CoaxCo and have a narrow 0.85 mm diameter. Part number (SC-086/50-NbTi-NbTi-200-SMAP/SMAP) is commonly ordered and is a 20 cm SMA male to SMA male assembly.

In terms of attenuators, we have begun using only XMA corp cryogenic attenuators, part no. 2082-6418-XX-CRYO, where XX is replaced with the required attenuation. These are used on each temperature stage to thermalize the inner contact through the resistive link (which would otherwise make no contact to each temperature stage) and reduce the population of thermal photons. Again for readout lines, where losses must be minimized, XMA corp 0 dB attenuators are used (2082-5026-00-CRYO-A), which contain a thermally conductive stripline to thermalize the inner conductor.

The amplifiers we use are either SiGe resistive feedback amplifiers from Cosmic Microwave (formerly the Weinreb group at Caltech) or amplifiers from Low Noise Factory. The CITLF1 or CITLF3 from Cosmic Microwave are used interchangeably in low-frequency experiments, while in transmon-type experiments typically use a Low Noise Factory amplifier. All of these amplifiers have $\sim$ 4 K noise temperature in their respective operating frequency ranges.

DC lines are typically BeCu loom wire from CMR-direct. Lines are clamped at each temperature stage and are optionally covered in GE-varnish to improve thermal contact. An image of such a clamp is shown in Fig. B.2 (a). Filtering of dc lines is performed on the mixing chamber and consists of three stages. The first two stages, an LC and RC filter, are used to remove any high-frequency noise, as shown in Fig. B.2 (c). This is followed by a sapphire stripline filter, as shown in Fig. B.2 (d). A Ti/Au meander line is fabricated on a sapphire chip and is used to reduce the electron temperature to $\sim$ 50 mK, based on designs from the Marcus lab at Harvard. A zoom-in of the track is shown in Fig. B.2 (e). Component values for the LC and RC filter boards are shown in Table B.1.

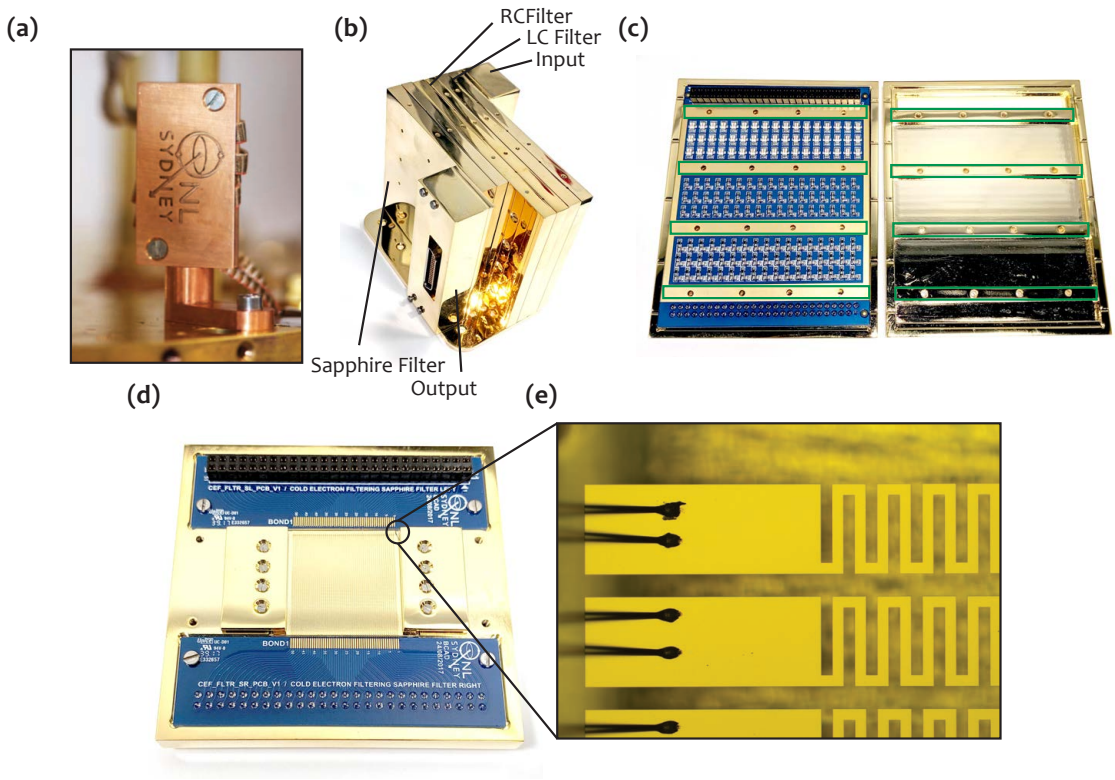

Figure B.2: (a) A thermalization clamp used on each temperature stage of the dilution refrigerator. BeCu loom wire is wrapped and clamped between the two plates. (b) An image of the assembled dc filtering setup. Each stage is labeled. Input and output occur via Micro-D connectors. (c) Disassembled RC filter stage. Green boxes highlight struts used to isolate each stage of the filter. (d) Disassembled sapphire filter stage. The sapphire chip is mounted in the center of the block and connected to PCBs at either end by bond-wires. (e) Zoom in of one corner of the sapphire filter. Here a meandering Ti/Au track is visible, as well as the ends of bond-wires used to connect it to the PCB.

Appendix C

Supplementary Material for On-chip Microwave Quantum Hall Circulator

C.1 Devices and Circuit Details

All devices are fabricated on GaAs/AlGaAs heterostructure with a 2-dimensional electron gas (2DEG) located 270 nm below the surface. From dc Hall transport measurements on the chip shown in Fig. 3.2, an electron density of $n_s = 1.1 \times 10^{11}$ cm^{-2} is extracted, along with carrier mobility of $\mu = 5.2 \times 10^6$ cm$^2/(\mathrm{V\,s})$. Small variation in these values are observed for the different devices measured, likely due to density variations across the wafer and effects of chemical processing. Circular mesa disks are etched using a $H_2O/H_2O_2/H_2SO_4$ solution to a depth of ~ 320 nm.

Metallic Ti/Au is evaporated on top of the devices to form the waveguide and circulator port structures. For the transmission-line device shown in Fig. 3.2, a coplanar transmission line geometry is employed using a 50 μm wide signal track with ground planes on either side. The distance to these ground planes measures 30 μm, ensuring a coupling impedance of $\sim 50\,\Omega$ within the frequency range of operation. The 350 μm diameter disc is situated equidistant between the signal line and ground plane, with a gap of 20 μm at either side. The data in Fig. 3.2(c) is taken on a device with an additional 100 μm diameter ohmic contact placed in the center of the mesa to assist in thermalization of the isolated disk of electron gas. This contact does not intersect the edge and as such we find that the overall dispersion spectrum (Fig. 3.2(c)) is qualitatively the same for devices without a center ohmic contact.

For the three-port device introduced in Fig. 3.3, a 330 μm diameter disk is placed at the center of the structure, with metallic ports separated by 20 μm from the mesa. The edges of the ports form 250 μm long curved arcs, and a surrounding ground plane is separated back

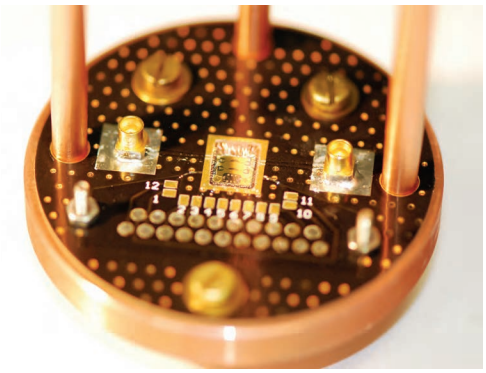

Figure C.1: Photograph of a 2-port transmission line device, wire-bonded to a PCB. The PCB is in thermal contact with a copper stage that is mounted to the mixing chamber of a dilution refrigerator.

from the disc by 385 µm. The device in Fig. 3.6 comprises a 500 µm diameter mesa, along with three Ti/Au ports with 250 µm long curved arcs that overlap the disc by 10 µm. An Au/Ge contact with 100 µm diameter is annealed in the center of the mesa. As the droplet is otherwise floating, we are unable to measure the resistance to the 2DEG. The contact is bonded to the ground plane of the PCB.

Chip-inductors (47 nH copper wire-wound, Coilcraft 0805HT series) are bonded to each of the three ports of the circulator to form an impedance matching network. The inductors are found to resonate with the stray parasitic capacitance in the setup C_{stray}, at a frequency of ~ 1 GHz in the absence of a magnetic field. All measurements are performed at the base temperature $T \sim 20$ mK of a cryo-free dilution refrigerator (Leiden Cryogenics CF500).

Devices are connected to two layer copper printed circuit boards (PCBs) constructed from Rogers 6006 high frequency laminate. These are mounted flat on a copper stage, which is thermally anchored to the mixing chamber plate of the dilution refrigerator (Fig. C.1). A cut-out in the PCBs enables devices to be silver pasted directly onto the copper beneath, ensuring good thermal contact. The ground planes of the devices are electrically connected to the ground of the PCB using numerous aluminum bondwires.

C.2 Experimental Methods

For the circulator shown in Fig. 3.3, the return line $2'$ is amplified at the 4 K stage of the fridge with a low-noise, resistive-feedback, cryogenic amplifier (CITLF1, Weinreb group, Caltech) with a noise temperature of $\sim$ 5 K and gain of 40 dB. The return signals are further amplified at room temperature. The applied microwave power at the device is in the range -90 dBm to -60 dBm. Features appear sharper at lower microwave power, but

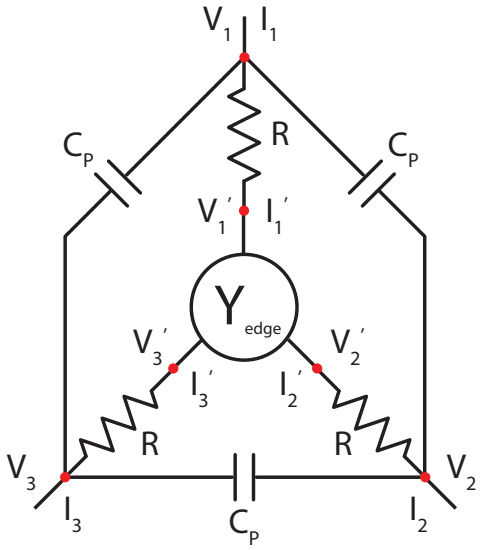

Figure C.2: Theoretical circuit model of a three port circulator including dissipation R and direct parasitic capacitive coupling C_p between port terminals. Nodes where I/I′ and V/V′ are calculated are shown in red.

with a decrease in signal to noise. S-parameter measurements are taken with a Keysight N5245A PNA-X network analyzer.

In Fig. 3.6 and Fig. C.4, each of the three circulator arms are connected to bias tees, while directional couplers are used on the rf sides of ports 1 and 2 to allow for amplification of the return signal at 4 K. This enables us to compare the signal outputs from a common input port. As in Fig. 3.4, the isolation plots in Fig. 3.6 are normalized relative to the transmission background at $B = 0\,\mathrm{T}$, and in the absence of dc gate biasing. Striations in the data are attributed to standing waves arising from an impedance mismatch between the device, cryo-amp, and passive components in the rf setup.

In a separate experimental cooldown, we demonstrate reconfigurable routing of a microwave packet by changing the value of the external magnetic field (Fig. C.3). An E8267D vector signal generator is used to output a 1 GHz continuous wave which is modulated with a Gaussian envelope via an AWG 5014C arbitrary waveform generator before being directed to port-1 of the device. In this particular setup, a mechanical switch (Radiall DPDT series) is installed and mounted on the mixing chamber stage of the fridge, which enables the output lines 2 and 3 to be selectively directed through a common return line that is amplified by the cryogenic amplifier. The resultant signal is measured with a digital sampling oscilloscope, and a fast Fourier transform (FFT) is performed in post-processing.

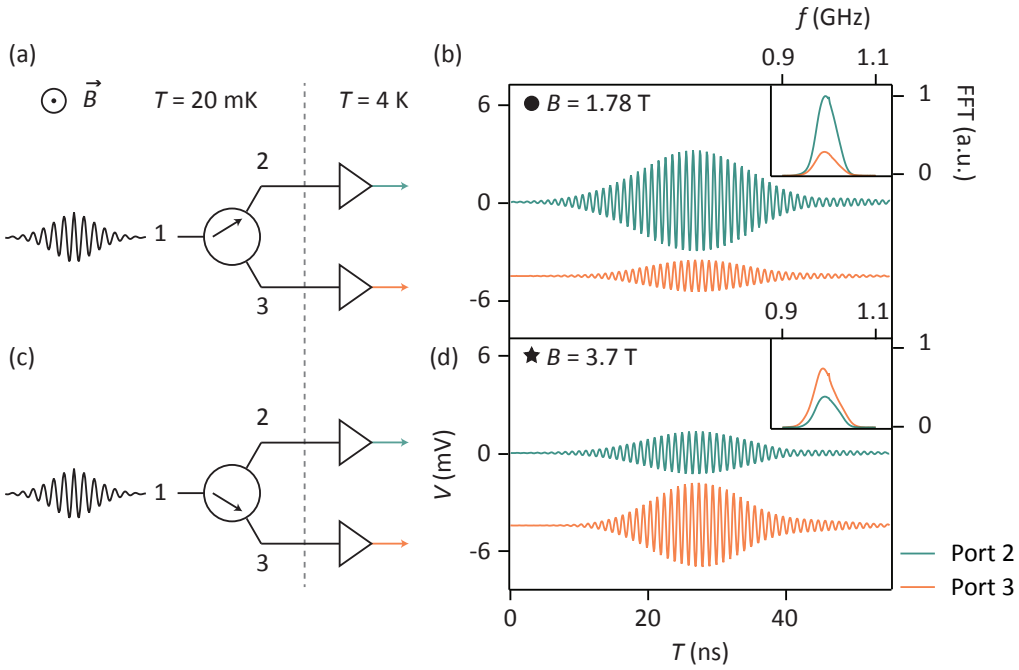

Figure C.3: (a) and (c) Schematic showing the experimental configuration for reconfigurable routing of microwave signals on-chip. A wavepacket is directed to port 1 of the circulator, and the resultant signals are measured after amplification at ports 2 and 3. (b) and (d) Output signal, as configured by adjusting the amplitude of the magnetic field to direct wave packets to the required port. Insets show normalized fast Fourier transform (FFT) amplitudes.

C.3 Lowering the Circulator Insertion Loss

In the current configuration of our circulator, while the edge-states are essentially dissipationless, the device presents an insertion loss due to the impedance mismatch between the Hall edge and the conventional 50 Ω impedance electrical circuit. This is in no way an intrinsic limitation. For the demonstration reported in the paper, we show the full response of the circulator with B-field, measuring across several GHz. With the general response of the circulator characterized, it is then possible to make use of standard microwave engineering approaches to impedance match the circulator to the arbitrary impedance of a transmission line over a narrow band. This is commonly done with devices such as the rf-SET or rf-QPC where an "L-match" is used to transform the $\sim 100\,\mathrm{k}\Omega$ device impedance towards the 50 Ω impedance of a transmission line over 10 MHz [154, 213].

Given that the circulator impedance acts like a load of order 25 kΩ (for $\nu = 1$) in series with the port capacitance, additional approaches to engineer a better match include:

1. Decreasing the size of the Hall droplet, thereby increasing the frequency of the resonant EMP modes and lowering the complex impedance from the ports to the edge.

2. Operating at higher (quantum Hall) filling factors and lower magnetic fields where the impedance of the edge is closer to $Z_0 = 50\,\Omega$, see Ref. [246].

3. Altering the characteristic impedance of on-chip transmission lines, alleviating the constraint of working with $Z_0 = 50\,\Omega$.

Working with layered 3D semiconductor stacks may also produce a similar reduction in the impedance [244]. We emphasize that the insertion loss of our device stems from the choice of coupling to cables with a characteristic impedance of 50 Ω, leading to a reflection of power rather than dissipation. In addition, a recent theoretical proposal has suggested a new configuration whereby a self-matched three-terminal gyrator can be achieved by grounding one of the port electrodes [245].

C.4 Extracting the Dielectric Permittivity

The overall dispersion curve of the fundamental edge magnetoplasmon (EMP) mode is extracted from the position of the features in the 2D data, as shown in the inset of Fig. 3.2 (c). Black markers plot the center frequency for which the features occur, measured at magnetic field values corresponding to integer filling factors ν, down to $\nu = 2$, (errors are within the

square marker bounds). The black solid line shows a fit to the resulting 1D data using the nonlinear dispersion relation for the fundamental mode:

$$\omega = \frac{\sigma_{\text{edge}} q}{2\pi\varepsilon^*\varepsilon_0}\left[\ln\frac{2}{ql} + c\right] \tag{C.1}$$

Here $\omega = 2\pi f$, σ_{edge} is the transverse conductivity of the edge, ε^* and ε_0 are the dielectric constant and permittivity of free space respectively, $c = 1$ for a sharp (etched) edge, and $q = \frac{2\pi}{p}$, where p is the sample perimeter (see [109] for details of this expression, and also [238, 239, 243]). The parameter l gives the physical extent of the EMP away from the etched edge of the mesa and is approximated by:

$$l = \frac{n_s m^*}{2\varepsilon^*\varepsilon_0 B^2} \tag{C.2}$$

where $n_s = 1.1 \times 10^{11}\,\text{cm}^{-2}$ is the carrier density, and m^* is the effective electron mass in GaAs of 0.067 m_e. We extract the free parameter $\varepsilon^* \approx 8.7$ from the fit, consistent with [243]. This value of ε^* corresponds to an average of the dielectric constant of GaAs and the vacuum, since the capacitive response of the system includes the edge-state, etched trench, and metallic structure that defines the microwave port.

C.5 Tuning Non-Reciprocity with Gate Voltage

In Fig. 3.6, tunable non-reciprocity is demonstrated on a device with three overlapping gate ports and a grounded centre contact. Both gates 1 and 2 are connected via couplers to individual cryogenic amplifiers. In Fig. C.4, isolation $\Delta S = S_{13}$-S_{23} is measured at $B = 1.45$ T while the dc bias V_{g1} is varied. The direction of magnetic field is reversed with respect to Fig. 3.6 (c). Varying the dc bias on port 1 tunes the response between source and sink ports 3 and 2 respectively (as observed by a peak in ΔS), producing a qualitatively similar isolation frequency response to that shown in Fig. 3.6 (c).

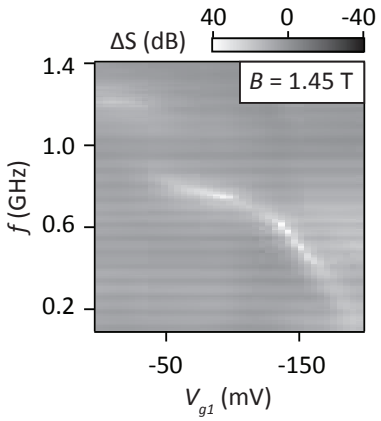

Figure C.4: $\Delta S = S_{13}$-S_{23} frequency response with port-1 gate voltage V_{g1}. Data is taken at constant magnetic field $B = 1.45$ T.

Appendix D

Supplementary Material for Zero-Field Edge Plasmons in a Magnetic Topological Insulator

D.1 Fabrication Details

The film used to make the circulator and corresponding Hall bar is seven quintuple layers of $(Cr_{0.12}Bi_{0.26}Sb_{0.62})_2Te_3$. We use photolithography to pattern a circular mesa with a diameter of 330 μm. We bake the Megaposit SPR 3612 photoresist at 80 °C (to avoid possible damage to the film from overheating), and develop with MF CD-30 after exposure. To define the mesa, we etch the surrounding film via Ar ion milling. After patterning the contacts and ground plane with the same photolithographic procedure, we deposit a 5 nm Ti sticking layer followed by 120 nm Au using e-beam evaporation. The capacitive contacts are designed to be 20 μm from the edge of the circular mesa. For the primary device discussed in this work, the relative misalignment of the mesa and contacts is approximately 5 μm.

D.2 Supplementary Figures

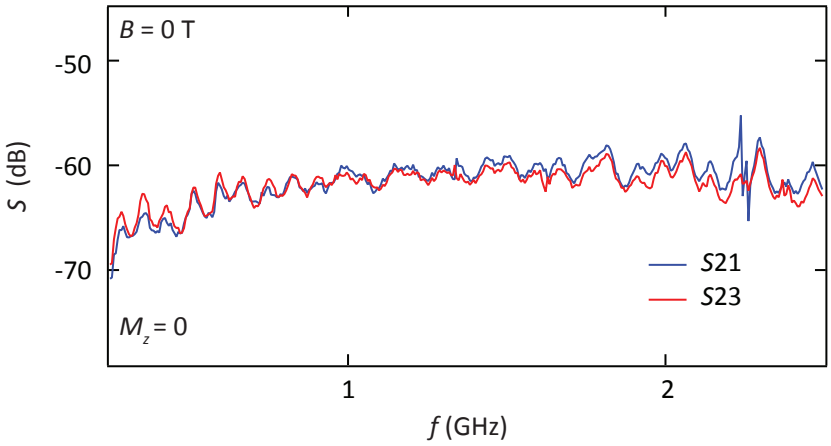

Figure D.1: Microwave transmission prior to sample magnetisation. S-parameter transmission measurements taken prior to device magnetisation at cryostat base temperature of $\sim 20\,\mathrm{mK}$, and applied port power of $-72\,\mathrm{dBm}$. Traces have been corrected for amplification and attenuation added to the setup in order to provide a measure of insertion loss. Subtracting the bare S-parameter responses S_{23} from S_{21} (as shown in Fig. 3.8 (d)) yields a small residual response at $B = 0\,\mathrm{T}$ about $0\,\mathrm{dB}$, attributed to slight differences in the line impedances of the two rf setups.

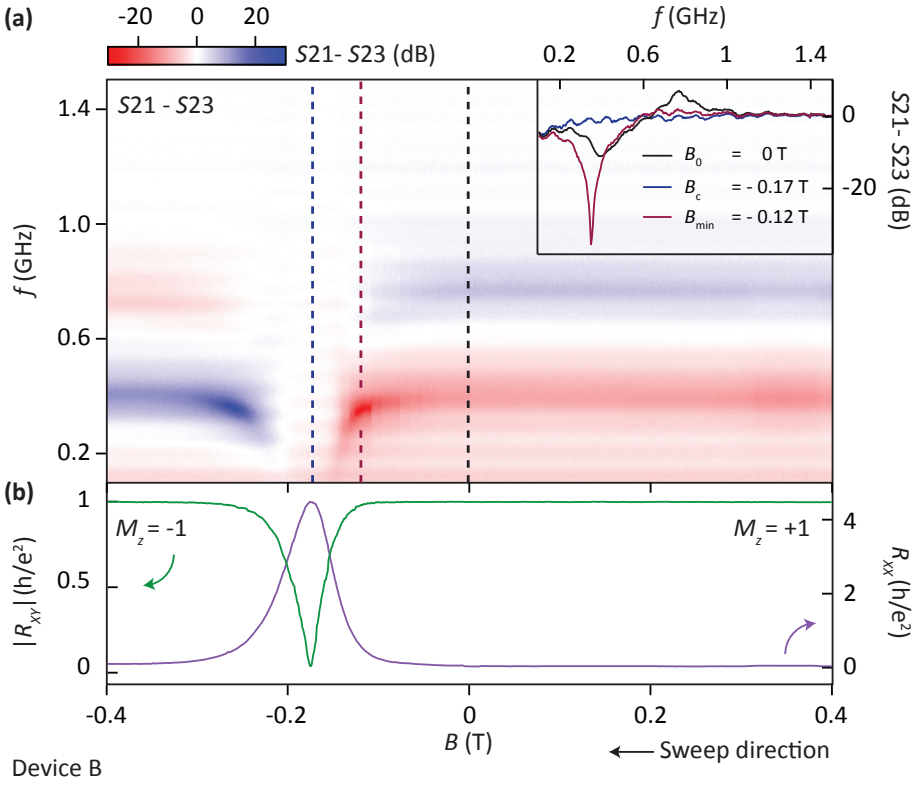

Figure D.2: Power and temperature dependence at $M_z = +1$ (a) - (d) Show the effect of temperature and applied microwave port power on S_{21} and S_{23} at $B = 0\,\mathrm{T}$ once the sample has been magnetised in the positive direction, $M_z = +1$. The direction of magnetisation has been reversed with respect to the data in Fig. 3.10. In accordance with a reversal of chirality, hot-spots are observed in the normalised ΔS_{21} plots with both power and cryostat base temperature, corresponding to the $2l$ path in this configuration. Colour bar represents $\Delta S\,(\mathrm{dB})$.

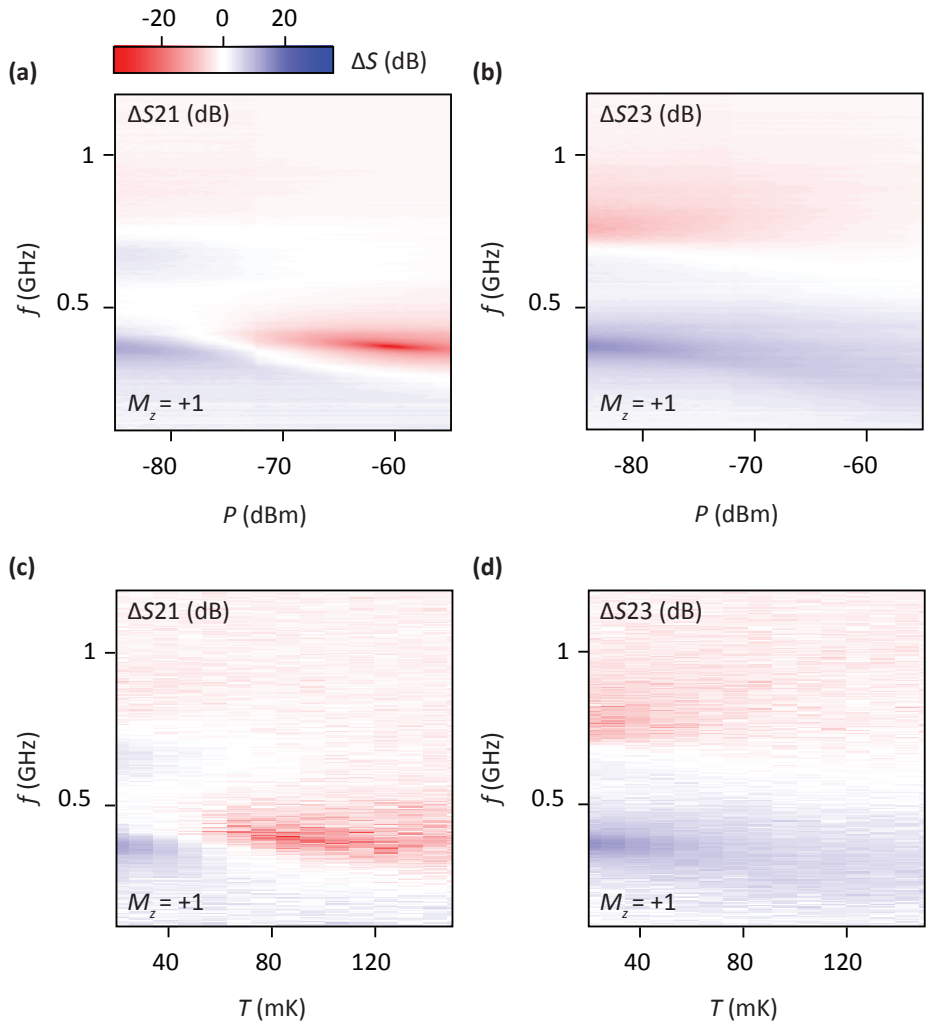

Figure D.3: Secondary device. S_{21}-S_{23} microwave spectrum is shown in (a), while Hall bar transport measurements are presented in (b) for a secondary device on a separate growth. Colour bar shows S_{21}-S_{23} in dB. The material comprises 8 quintuple layers of $(Cr_{0.12}Bi_{0.26}Sb_{0.62})_2Te_3$, with fabrication methods and circulator geometry nominally identical to the device outlined in Sec.3.2. Inset shows cuts taken at constant magnetic field values corresponding to dashed lines in (a).

Appendix E

Supplementary Material for Repairing the Surface of InAs-based Topological Heterostructures

E.1 Fabrication Details

All devices presented here were from a single wafer, grown via molecular beam epitaxy with a 10 nm aluminum cap grown *in-situ*. Hall bars are defined in PMMA using electron-beam lithography. Mesas were etched using a chemical wet etch process, which includes an Al etch using Transene-D, heated to 47.8 °C, and etched for 11 s, followed by three 11 s rinses in DI water. The InAs is then etched in dilute phosphoric acid (50:5:1 H_2O:H_3PO_4:H_2O_2) for 95 s, to a depth of $\sim$ 180 nm, again followed by three 11 s rinses in DI water. Finally, a 6 s Transene-D dip is used to remove any overhanging Al, followed by three 11 s rinses in DI water. The resist was stripped quickly after completion of the final etch using Acetone.

Aluminum is removed from the surface of the mesa, except at contacts, using Transene-D heated to 47.8 °C and etched for 11 s, followed by three 11 s rinses in DI water. The resist was stripped quickly after completion of the final etch using Acetone.

Surface treatment and oxide growth is performed in the Picosun R200 ALD tool, fitted with a load-lock, a remote plasma source and an ozone generator. The stage temperature is set to 200 °C and a constant flow of N_2 gas is used to purge the tool, including during the treatment steps.

For the ArH plasma treatment, the ArH plasma is generated with an Advanced Energy Litmas™ RPS 3001 remote plasma source at 1000 W source power, and a 20 s pulse is applied 6 times, with a 30 s gap between each run. We note that during this process N_2 gas

continues to flow through the process chamber.

For the TMA reduction treatment, TMA is pulsed for 1.0 s, with a 30 s purge between cycles. This is repeated 10 times prior to oxide growth.

Oxide growth is performed *in-situ* using 170 cycles of TMA and either H_2O or O_3, following a standard recipe for oxide growth.

E.2 Measurement

Measurements are taken in a BlueFors LD400 dilution refrigerator, fitted with a wide-bore 2 T solenoid, with a base temperature of 7 mK. A custom Cryo-CMOS based multiplexer is used to map each of 32 input DC lines to 5 outputs, for a total of 160 DC lines, and is used to allow measurement of up to 10 Hall bars in a single cool-down. The CMOS is fabricated commercially on the AMS 0.35 µm process. A schematic of this setup is shown in Fig. E.1.

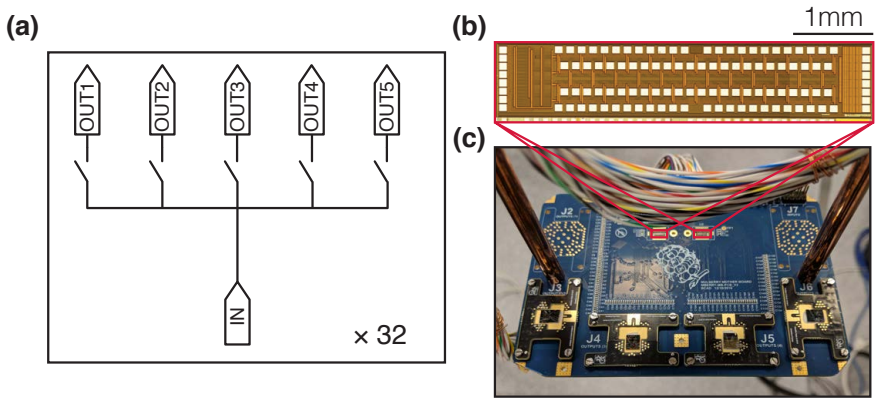

Figure E.1: (a) Schematic of a single cell of the multiplexing chip. Each input is multiplexed to 5 outputs, allowing for a total of 160 DC lines to be measured using 32 lines. (b) Image of the multiplexing chip. (c) Mounted measurement board, with four samples mounted around the bottom of the board.

Measurements are taken with a lockin, with a 10 nA constant current applied across the device through a 100 MΩ resistor. The top gate voltage is applied using a Yokogawa GS200 voltage source.

E.3 Density and Mobility for all Treatments

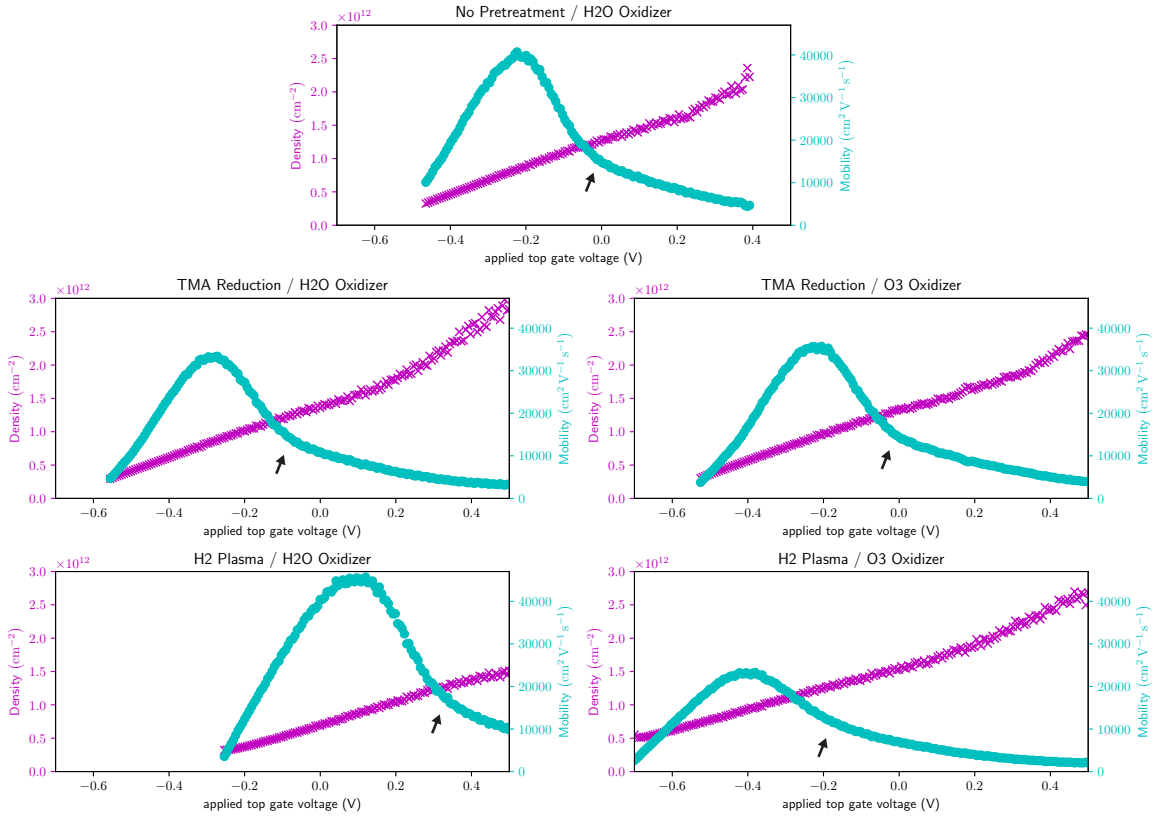

Figure E.2: The density and mobility traces as gate voltage is swept for all surface treatments. The location of second subband population is marked with an arrow on each trace.

E.4 Density at Peak Mobility

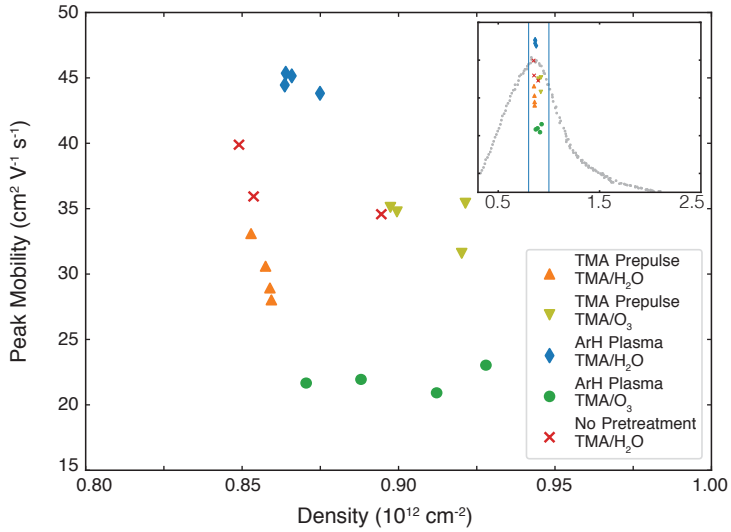

Figure E.3: The location in density that peak mobility occurs, for samples taken near the center of the growth wafer. Samples grown with ozone are shifted to the right relative to samples grown with water.

Appendix F

Supplementary Material for Radio-Frequency methods for Majorana-Based Quantum Devices

F.1 Instruments

Below we list electronic equipment used in the experiments.

1. Demodulation unit used for reflectometry measurements in Fig. 5.7 and Fig. 5.8: Zurich Instruments, Ultrafast Lock-in Amplifier (600 MHz)[1]
2. Current-to-voltage converter: University of Basel, Electronics Lab, Low Noise/High stability I/V converter, SP 983 with IF3602
3. Voltage sources: 48-channel QDAC, custom digital-to-analog converters, QDevil ApS[2]
4. Lock-in: Stanford Research SR830 DSP Lock-in amplifier
5. Waveform generator: Keysight 33500B
6. Arbitrary waveform generator: Tektronix 5014 C, 1.2 GS/s
7. Vector network analyser: Rohde & Schwarz - ZVB8

[1] Electronic Access: https://www.zhinst.com/products/uhfli

[2] Electronic Access: https://www.qdevil.com

8. Directional coupler: Minicircuits ZEDC-15-2B (1 MHz - 1 GHz)
9. Microwave switch Minicircuits ZASWA-2-50DR+ (DC - 5 GHz)
10. Cryogenic 4 K amplifier: Caltech Weinreb CITLF3
11. Digitizer: AlazarTech ATS9360 - 12 bit, 1.8 GS/s

F.2 Signal-to-Noise Ratio and Visibility

The extraction of signal-to-noise ratio (SNR) and visibility was accomplished with the following pulse sequence cycle [Fig. 5.8 (a) inset]. The pulse sequence starts with a fixed amplitude voltage pulse on gates RP (positive voltage pulse) and LP (negative voltage pulse) bringing the system to a point I for a duration of $\tau_I = 150\,\mu s$ for initialization into a relative charge state $N+2$. Then, the gates LP (positive voltage pulse) and RP (negative voltage pulse) bring the system into a relative charge N state (point P) for a time $\tau_P = 200\,\mu s$. Finally, gates LP (negative voltage) and RP (positive voltage) bring the system close to intra-island degeneracy point M (between N and $N+2$ relative charge states) which we denote as measurement position. V_{TX} excitation was controlled with microwave switch (ZASWA-2-50DR+), in order to avoid disturbances in the system during the manipulation phase (I and P). The readout was performed only at the measurement point (M) by triggering the ATS9360, 12 bit waveform digitizer card for a total time duration of $\tau = 50\,\mu s$. To build statistics $N_{\text{cycles}} = 10^8$ experimental runs of the pulse sequence were performed. From histograms of $V_{rf}^{(S2)}$ measurements (with 2 mV bin size), the probability, $P_{V_{rf}^{(S2)}}$ of singe-shot outcomes can be estimated for each value of measurement time τ.

For the sake of simplicity, all denoted V_{rf} here will refer to demodulated voltage with the right charge sensor ($V_{\text{rf}}^{(S2)}$). Visibility is defined as [213]:

$$V = F_N + F_{N+2} - 1 \tag{F.1}$$

where F_N and F_{N+2} are the fidelities of relative charge state N and $N+2$, respectively. The fidelity of a charge state, N, is defined by $F_N = 1 - \text{erf}(N)$, where $\text{erf}(N)$ is an probability of measuring an $N+2$ charge state when in the N state. The $N+2$ state fidelity is similarly expressed as $F_{N+2} = 1 - \text{erf}(N+2)$. This error is calculated by evaluating cumulative normal distribution function up to the threshold voltage V_T, which for $N+2$ state is:

$$\text{erf}(N+2) = \int_{-\infty}^{V_T} n_{N+2}(V_{\text{rf}})\text{d}V_{rf} \tag{F.2}$$

where V_T is the threshold voltage calculated from the center of the means of the two Gaussians:

$$V_{\text{rf}} = \frac{\mu_N + \mu_{N+2}}{2} \tag{F.3}$$

and $n_{N+2}(V_{\text{rf}})$ is the probability density function for the relative charge state $N+2$:

$$n_{N+2}(V_{\text{rf}}) = \frac{e^{(V_{\text{rf}}-\mu_{N+2})^2/2\sigma^2_{N+2}}}{\sqrt{2\pi}\sigma_{N+2}} \tag{F.4}$$

Similarly the value of erf(N) is calculated as:

$$\text{erf}(N) = \int_{V_T}^{\infty} n_N(V_{\text{rf}})\text{d}V_{rf} \tag{F.5}$$

and $n_N(V_{\text{rf}})$ is the probability density function for the relative charge state N:

$$n_N(V_{\text{rf}}) = \frac{e^{(V_{\text{rf}}-\mu_N)^2/2\sigma^2_N}}{\sqrt{2\pi}\sigma_N} \tag{F.6}$$

Minimizing the function of two errors (erf(N) and erf$(N+2)$) and then inserting found fidelities we calculate the visibility

$$V = 1 - \text{erf}(N) + 1 - \text{erf}(N+2) - 1 \tag{F.7}$$

This yields a visibility $V = 99.8\%$ for an integration time of 1 µs.

F.3 Fabrication

All devices presented have nanowire (NW) diameter $\sim$ 100 nm. NWs were grown using the vapor-liquid-solid technique in a molecular beam epitaxy system with the InAs [111] substrate crystal orientation [315]. Following the NW growth, Al is deposited epitaxially *in situ* on several facets of the NW with an average thickness of 10 nm [315, 370]. The NW is then positioned on a chip with a homebuilt micro-manipulator tool (Zaber XYZ-Theta stage with Eppendorf micromanipulator (model 4r) and large-working-distance Leica microscope), which allows micrometer precision in placement. The Al was selectively etched using wet etchant Transene D. All patterning was performed using an Elionix ELS-7000 EBL. Next we present the details specific to fabrication of all three devices:

The InAs/Al NW has Al shell on two of its facets and is fabricated on Si chip covered with 200 nm of SiO_2. The TiAu contacts (5 nm + 150 nm) were evaporated after performing RF milling to remove the oxide from the NW. Then, 5 nm of HfO_2 was deposited by atomic layer deposition. Finally the last set of Ti-Au gates (5 nm + 150 nm) was evaporated.

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