Electronically Controlled Capacitive Energy Storage Element for DC Grids

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Abstract: A major and very important challenge in dc grid development is maintaining continuous converter operation under dc faults. This paper proposes a novel capacitive energy storage device which improves security of dc grids by avoiding terminal blocking. The device provides current from the capacitor bank during dc faults, reducing fault current contribution and voltage drop of dc grid converters. Moreover, the device also helps in balancing pole voltages which is of particular significance during pole-to-ground faults in symmetrical monopole systems. Other benefits like improved transient grid stability are also demonstrated. Device's design and performance is assessed using theoretical analysis and verified on a three-terminal offshore dc grid model in PSCAD. The cost of the device's electronics is minimized and the total cost and weight estimation are also shown.

Keywords: Energy storage, dc grid protection, MMC, VSC

1. Introduction

Increased offshore wind power penetration has heightened interest in dc grids worldwide because of benefits they bring compared to point-to-point dc systems. These include, among others, increased redundancy and security of power transfer. However, dc grid protection remains one of the main challenges in dc grid development [1]. Dc faults result in voltage collapse at the fault point which quickly spreads throughout the grid and causes a rapid increase in dc current of modular-multilevel converters (MMCs). In order to prevent damage to insulated gate bipolar transistors (IGBTs), MMCs are blocked by overcurrent or undervoltage self-protection. Practical blocking thresholds are 2-3 p.u. for arm current and 0.8 p.u. for dc voltage. Because of these tight margins, converter blocking is expected to occur in majority of fault scenarios and forms a premise for conventional dc grid protection strategies [2].

When blocked, MMC's control loops are disabled and MMC goes through several transient states, ending in diode bridge rectifier operation. This negatively impacts both the ac and dc grid. On the dc side, it causes a loss in capacity which hinders dc grid's ability to balance power. This is a serious issue for smaller dc grids where dc voltage may deviate significantly [3], exposing equipment to dangerous overvoltages or leading to further loss of terminals due to dc voltage collapse. On the ac side, reactive power control is lost which deteriorates the ac voltage profile. The most severe impact on the ac system is the loss of dc power exchange. The extent of frequency deviations in ac system depends on the duration of dc contingencies, the system inertia and the amount of power loss [4].

Normally, MMC blocking involves immediate tripping of converter ac circuit breaker (ACCB) in order to prevent thermal destruction of converter diodes. The restart of MMC is associated with long delays because of slow ACCB operation and synchronization delays. A recent research [5, 6] proposes temporary blocking of MMC without tripping the associated ACCB, resulting in faster restoration of terminal power. However, this method requires re-evaluation of diode ratings and suffers from higher peak current and voltage stress on both the ac and dc grid components in addition to reduced stability margins.

Lot of recent research has been centred on maintaining MMC converter operation under dc faults and multiple solutions have been investigated [7–10]. Dc grid with FB (full bridge) MMCs is shown to operate through all dc faults [7] but the cost and losses of a FB MMC are substantially higher compared to HB (half bridge) MMC. The use of LCL filters on the ac side for MMC fault ride-through is a proposed in [8] but has the drawback of reduced efficiency at partial loadings. Reference [9] considers radial network topology in which only the converter connected to the faulted cable is blocked while the others remain in operation. However, radial systems lack inherent redundancy of dc grids. MMC blocking can be prevented on multi-converter buses [10] but this is also limited to specific grid topologies.

References [11, 12] investigate the sizing of inductive current slope limiters (ICSLs) in series with dc circuit breakers (DCCBs) to prevent converter blocking. While simple and cost-effective, the downside

of this approach is that the ICSL size increases with DCCB opening time. With mechanical DCCBs (MDCCBs), the opening times are 5-10 ms [13, 14] and impractically large ICSLs would be required. This can cause stability and energy balancing issues [15] and may require overrating of some components. Fast-acting hybrid DCCBs (HDCCBs) [16] can open in 2 ms and require large but acceptable ICSLs, however, their cost is considerably higher [1] because of high number of semiconductor components.

Another important challenge with dc grid protection, which motivates this study, are overvoltages in some fault scenarios. With symmetrical monopole systems, pole-to-ground faults do not result in high fault currents, however, voltage of the non-faulted pole increases to 2 p.u. which can be destructive for cable insulation (typically rated for 1.85 p.u. [17]). Ac transformer is also stressed as its secondary phase-to-ground voltages are offset by half the dc bus voltage. There is no known method of preventing MMC blocking under pole-to-ground faults [18, 19]. Reference [20] proposes fast dc voltage reduction (only possible with point-to-point systems), however, this results in increased converter current.

This paper introduces an electronically controlled dc grid protection device based on capacitive energy storage. It is postulated that such a component brings multiple benefits:

1. Delaying or avoiding MMC blocking under dc faults.
2. Reduced pole voltage deviations, which is particularly important for symmetrical monopole grids.
3. Improved transient stability.

2. Device description and operating principle

2.1 Components and placement

The proposed Controlled Capacitive Energy Storage element (CCES) and its placement in a dc system is shown in Fig. 1 while the basic parametric analysis is presented in [21]. One CCES is installed per dc bus. Only a single dc line is shown for simplicity, however, it is assumed that there will be multiple lines connected to the bus. CCES has two symmetrical poles (even if MMC is monopolar) and its main component is a capacitor bank with total capacitance of C_B. Each pole also consists of anti-parallel thyristors T_1 and T_2, surge arrester SA, RL filter with components R_F and L_F and mechanical switch S_M. Index p refers to the positive pole and index n refers to the negative pole. Middle point of the device is grounded through resistor R_G.

CCES operates by connecting the pre-charged capacitor bank to the dc bus when a dc voltage deviation is detected (a fault or a large transient). CCES supplies positive or negative current to the dc bus when required which reduces bus voltage deviations and is expected to result in lower fault current from the MMC. Because C_B is quite large, it is unlikely to cause resonance problems.

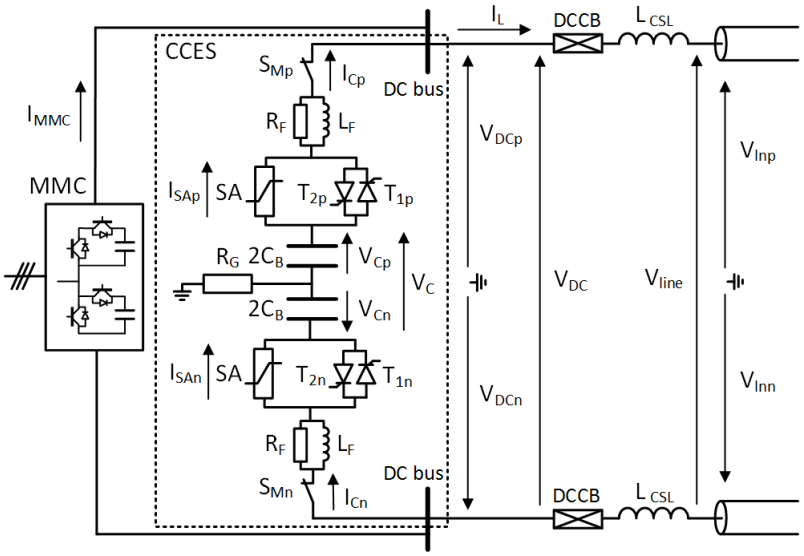

Fig. 1. CCES and its placement on a dc bus

2.2 Operation under normal loading

In normal operation, capacitor bank is pre-charged to dc bus voltage. Both mechanical switches are closed but none of the thyristors are fired so the capacitor bank is connected to the dc bus through surge arresters SA_p and SA_n. RL filters are optional components introduced to block switching transients but they can be neglected in further study because of small R and L values (few ohms/millihenries).

A simple arrester model can be assumed, with large resistance $R_{SA,unsat}$ in the voltage range below saturation point $V_{SA,sat}$ and low resistance $R_{SA,sat}$ above the saturation point. CCES is thus effectively disconnected from the power system for bus voltage variations below $V_{SA,sat}$ which minimizes its dynamic impact in normal operation. In case of a significant dc bus voltage deviation when the difference between V_C and V_{DC} exceeds $V_{SA,sat}$, surge arrester saturates and capacitor current of either pole is described by

$$I_C - 2C_B R_{SA,sat} \frac{dI_C}{dt} = C_B \cdot \frac{dV_{DC}}{dt} \qquad (1)$$

Since $R_{SA,sat}$ is very low, from (1) it follows that capacitor bank current (and consequently surge arrester current) is proportional to the rate of change of bus voltage. Therefore, when arrester saturates, capacitor bank voltage closely follows dc bus voltage so that $|V_C - V_{DC}| \lesssim V_{SA,sat}$. As dc voltage is controlled directly or indirectly (droop control) in normal operation, its rate of change is limited and so is the arrester current. However, during events that produce significant voltage disturbances such as short circuits or converter blocking, arresters are at risk of thermal overload. Thyristors T_1 and T_2 are fired to protect surge arresters if high arrester current is detected while in turn arresters protect thyristors against overvoltage. A particularly beneficial property of this arrangement (thyristor in parallel with arrester) is that thyristor voltage stress and arrester current

stress are very low. Since $V_{SA,sat}$ will be rated for only several percent of nominal system voltage, voltage rating of T_1 and T_2 will be comparably low which minimizes the cost, size and weight of electronics. It is recommended that thyristor voltage rating is between 130 and 150 % of $V_{SA,sat}$.

Lastly, mechanical switches S_{Mp} and S_{Mn} are used to isolate CCES from the bus. This may be required for maintenance or if thyristor or surge arrester failure is detected. Since both failures usually result in a short circuit, V_C and V_{DC} equalize and transient current decays naturally. As a result, the switches do not require high current breaking capability and can be implemented as low-cost mechanical disconnectors or ac circuit breakers.

2.3 Control system

CCES control system is shown in Fig. 2. It has simple structure and consists of two subsystems – fault detection subsystem and arrester bypass. The two poles are controlled independently but use identical control system layout.

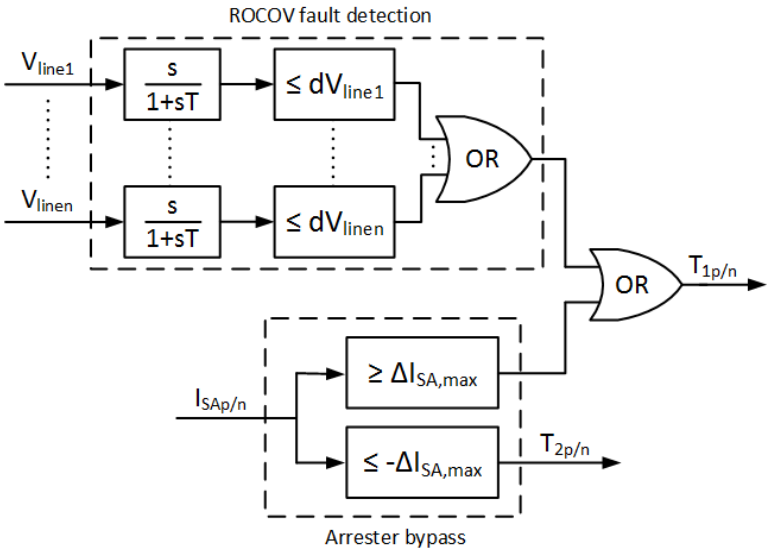

Fig. 2. CCES control system schematic (per pole)

Fault detection will in most cases be performed by external relays because of the need to coordinate CCES operation with DCCBs on the same bus. CCES is activated if a fault is detected on any of the connected lines. In order to minimize activation time, fast method such as rate-of-change-of-voltage (ROCOV) [22] is recommended. Arrester bypass operates by firing thyristors whenever arrester current exceeds a predefined threshold ($\Delta I_{SA,max}$), for example during capacitor charging. In addition to protecting surge arresters against thermal overload, this logic provides redundancy in case of fault detection failure as high arrester current would trigger T_1 firing under a dc fault.

2.4 Operation under pole-to-pole faults

Under a solid pole-to-pole fault on the line side of L_{CSL}, MMC responds like a series LC circuit consisting of equivalent capacitance and inductance given by [23]

$$C_{MMC} = \frac{6C_{SM}}{N} \tag{2}$$

$$L_{MMC} = \frac{2}{3}L_{arm} \tag{3}$$

where C_{SM} is submodule capacitance, N is number of submodules per arm and L_{arm} is inductance of arm inductors. When a fault is detected, thyristors T_{1p} and T_{1n} are fired which connects C_B directly to the dc bus with an equivalent circuit (under a zero-impedance pole-to-pole fault) shown in Fig. 3. I_{MMC}, I_L and I_C represent fault current components superimposed on their pre-fault values. The impact of RL filters and resistive components is neglected for simplicity.

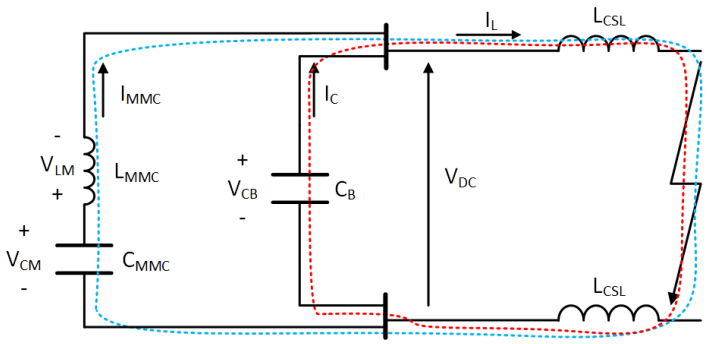

Fig. 3. Equivalent circuit of CCES and MMC under a pole-to-pole fault

The basic parametric analysis of CCES in [21] illustrates that the addition of parallel capacitor C_B only marginally increases line inductor current I_L. This is assuming that the MMC operates continuously under the fault and therefore V_{DC} does not reduce much (capacitor current depends on the voltage differential). It is also shown in [21] that the MMC's fault current reduces by the current provided by the CCES, since I_L is now shared between the two sources (C_{MMC} and C_B):

$$I_{MMC} = I_L - I_C \tag{4}$$

In the current study, the detailed dynamic equations of this circuit are derived:

$$V_{CM}(0) - \frac{1}{C_{MMC}}\int I_{MMC}\, dt - L_{MMC}\frac{dI_{MMC}}{dt} = V_{DC} \tag{5}$$

$$V_{CB}(0) - \frac{1}{C_B}\int I_C\, dt = V_{DC} \tag{6}$$

$$2L_{CSL}\frac{dI_L}{dt} = V_{DC} \tag{7}$$

Solving (4)-(7) yields a fourth-order differential equation for I_{MMC}:

$$\frac{d^4 I_{MMC}}{dt^4} + \frac{d^2 I_{MMC}}{dt^2}\left(\frac{1}{L_{MMC}C_B} + \frac{1}{L_{MMC}\,C_{MMC}} + \frac{1}{2L_{CSL}C_B}\right) + \frac{I_{MMC}}{2L_{CSL}L_{MMC}C_B C_{MMC}} = 0 \tag{8}$$

Applying Laplace transformation to (8) and using $V_{CM}(0) = V_{CB}(0) = V_{DC}(0)$ as initial conditions, time-domain response for I_{MMC} is obtained as

$$I_{MMC}(t) = \hat{I}_1 \sin(\omega_1 t) - \hat{I}_2 \sin(\omega_2 t) \tag{9}$$

where

$$\omega_{1,2} = 2\Big[2L_{CSL}C_B + C_{MMC}(2L_{CSL} + L_{MMC}) \mp \sqrt{(2L_{CSL}C_B + C_{MMC}(2L_{CSL} + L_{MMC}))^2 - 8L_{CSL}C_B L_{MMC}C_{MMC}}\Big]^{-\frac{1}{2}} \tag{10}$$

$$\hat{I}_1 = \frac{V_{DC}(0)}{2L_{CSL}C_B L_{MMC}} \cdot \frac{1}{\omega_1(\omega_2^2 - \omega_1^2)} \tag{11}$$

$$\hat{I}_2 = \frac{V_{DC}(0)}{2L_{CSL}C_B L_{MMC}} \cdot \frac{1}{\omega_2(\omega_2^2 - \omega_1^2)} \tag{12}$$

With C_B in the system, MMC's fault current response is a combination of two sinusoids with different frequencies initially opposing each other. In comparison with the case when $C_B = 0$ (corresponding to a system without CCES), it is evident from (10) that the increase in C_B leads to a reduction in both characteristic frequencies, allowing more time for the protection system to operate. CCES also reduces MMC fault current magnitude. This can be seen in Fig. 4 which shows numerical values of $\hat{I}_1$, $\hat{I}_2$, ω_1 and ω_2 for fixed power system parameters (640 kV, 1 GW MMC) and a range of C_B.

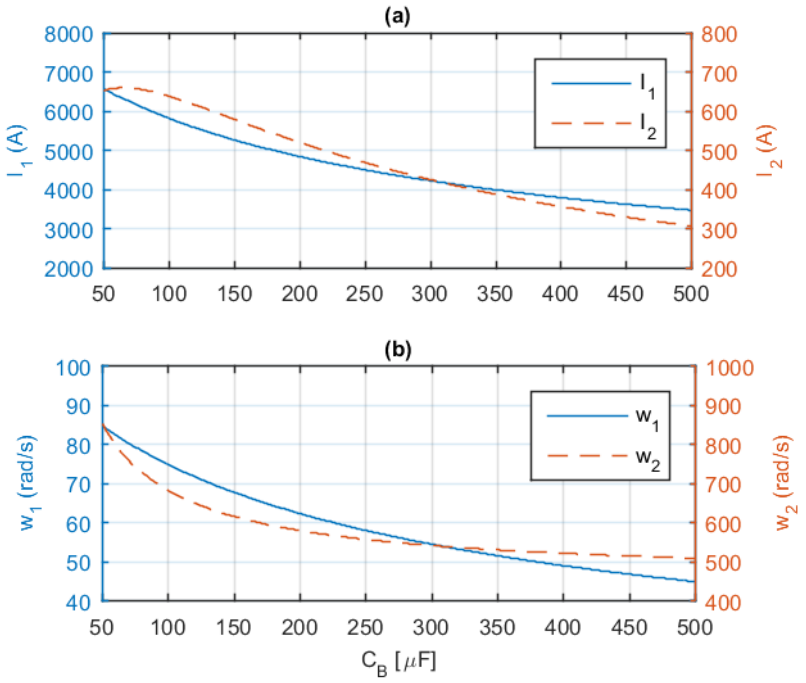

Fig. 4. Amplitude and frequency of MMC fault current components versus C_B

Differentiating (9) yields the formula for MMC's fault current slope:

$$\frac{dI_{MMC}(t)}{dt} = \frac{V_{DC}(0)}{2L_{CSL}C_B L_{MMC}} \cdot \frac{1}{\omega_2^2 - \omega_1^2} \cdot [\cos(\omega_1 t) - \cos(\omega_2 t)] \quad (13)$$

From (11) it follows that fault current slope at fault inception ($t = 0$) is zero which differs from the fault response of a sole MMC where the initial current slope is $V_{DC}(0)/(L_{MMC} + 2L_{CSL})$. This property of CCES protection is particularly beneficial for shorter fault neutralization times since it results in very small MMC fault current increase. Fig. 5 shows time-domain responses for several C_B values and compares them with the response of a standalone MMC. It is visible that CCES substantially reduces MMC fault current in the operating timeframe of dc grid protection, as well as that the initial current slope is zero which leads to a negligible current increase in the first 2 ms.

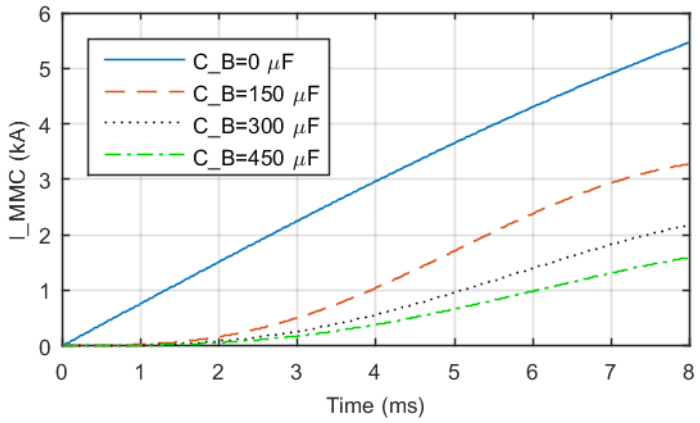

Fig. 5. MMC fault current increase for different capacitor bank sizes

2.5 Operation under pole-to-ground faults

Equivalent circuit for pole-to-ground faults with symmetrical monopoles is shown in Fig. 6. Without CCES, only C_{line} provides reference to ground for V_{DCp}. Under a pole-to-ground fault, C_{line} discharges rapidly as its current is only limited by stray inductance of the cable. Dc bus on the other hand does not have its own reference to ground so C_{MMC} does not discharge under the fault (even though some transient currents appear through MMC's arms). Consequently, voltage across the bus remains constant and voltage of the non-faulted pole rises to 2 p.u. which can damage cable insulation.

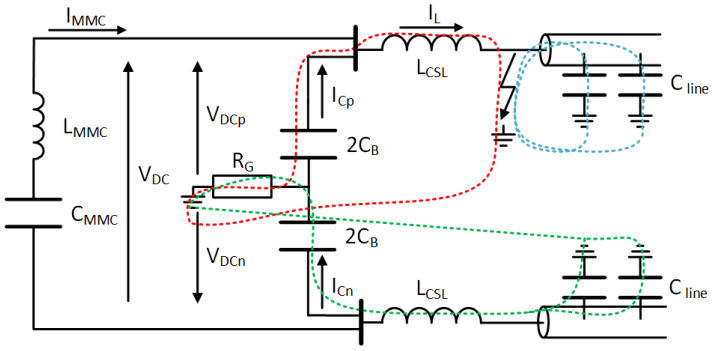

Fig. 6. Equivalent circuit of CCES and MMC under a pole-to-ground fault

With CCES installed and grounded through R_G, dc bus is provided with a large capacitive reference to ground. In order to change V_{DCp} or V_{DCn}, each half of C_B needs to be charged or discharged. For a pole-to-ground fault occurring on the positive pole, upper arm of CCES needs to discharge through L_{CSL} before V_{DCp} drops to zero. Given the large value of L_{CSL}, this greatly slows down the decay of pole voltage. Without CCES, L_{CSL} is not in the discharge path of C_{line} and hence the inductor does not help in maintaining pole voltage.

The downside of CCES-based protection is that DCCBs open under higher currents than they normally would under pole-to-ground faults. While these currents are lower than for pole-to-pole faults and hence do not impact breaker dimensioning, they do increase DCCB energy absorption and prolong energy dissipation time. This could be problematic in dc grids with overhead lines where multiple reclosing attempts are made as the total amount of energy absorbed by DCCB's surge arresters could increase significantly. For this purpose, resistor R_G can be used to reduce CCES current under pole-to-ground faults. In an idealized case where $I_{MMC} = 0$ and cross-coupling between CCES poles is neglected (valid if R_G is low), current of the fault loop (red line) is given by

$$I_{Cp}(t) = \frac{V_{DC}(0)}{2\omega_3 L_{CSL}} \cdot e^{-\frac{R_G}{2L_{CSL}}} \cdot \sin(\omega_3 t) \tag{14}$$

where

$$\omega_3 = \sqrt{\frac{1}{2L_{CSL}}\left(\frac{1}{C_B} - R_G^2 C_B\right)} \tag{15}$$

From (14) and (15) it is visible that R_G decreases both the amplitude and frequency of CCES current. On the downside, this speeds up the decay of bus pole voltage and reduces effectiveness of CCES protection. In dc grids with cables where all faults are permanent, CCES' middle point is solidly grounded ($R_G = 0$).

3. Test system description

Test system shown in Fig. 7 is developed in PSCAD. It represents a three terminal dc grid connecting two offshore wind farms with the onshore ac grid. MMCs 1 and 2 are rated for 1000 MW while MMC 3 is rated for 2000 MW. The system is a symmetrical monopole with nominal voltage of ± 320 kV. Each MMC is connected to its corresponding ac system through a 360/372 kV step-up transformer. MMC 3 regulates dc voltage while MMCs 1 and 2 regulate ac voltage. Wind farms are represented by controllable power sources while the onshore ac grid is represented by an ideal voltage source with series RL impedance (SCR=10, X/R=10). Positive sign of power and current indicates power transfer from the ac system to the dc grid. For per-unit analysis, base power, voltage and current are 1000 MVA, 640 kV and 1.6 kA respectively.

In order to reduce costs and represent worst-case scenario, all DCCBs are of mechanical type with opening time of 8 ms and breaking capability of 16 kA [14, 24]. Each DCCB has a series inductor and a dv/dt relay employing ROCOV fault detection method. Overcurrent protection blocks MMCs at twice the rated arm current which equals 3.3 kA for MMCs 1 and 2 and 6.4 kA for MMC 3. Undervoltage protection activates around the peak of diode bridge voltage which equals 510 kV or 0.8 p.u.

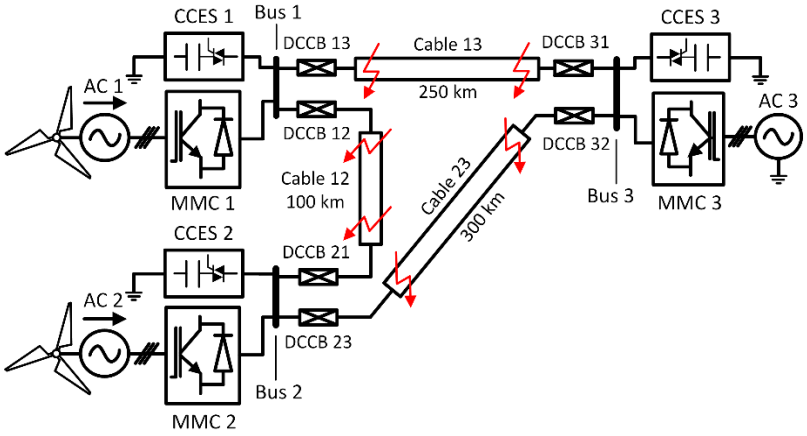

Fig. 7. Test system schematic

Detailed study of CCES dimensioning and the impact of C_B on fault responses, including peak fault current increases (PFCIs) of the MMC and DCCB, critical inductor size and critical DCCB opening time, is given in [21]. PFCI is maximum value of fault current, expressed as an increase over steady-state value. For completeness, Fig. 8 is reproduced from the same study, showing the relationship between minimal C_B and DCCB 13 inductor (L_{13}) size required to prevent MMC 1 blocking (red curve). C_B supplements L_{13} so the inductor can be reduced at the cost of larger capacitor bank. The blue curve shows DCCB 13 PFCI for each set of L-C parameters. Decreasing the inductor size results in increased DCCB PFCI but it remains within the operating limits of DCCBs.

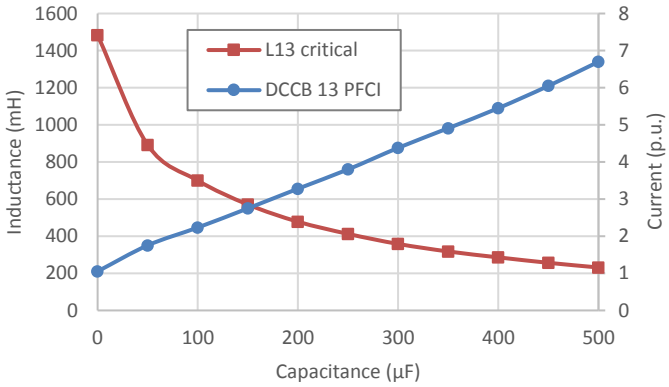

Fig. 8. Critical inductor size and DCCB 13 PFCI versus CCES 1 capacitance

Three protection system configurations are developed for comparison, as shown in Table 1.

1. The “Basic” configuration is based on conventional protection strategies where MMCs are blocked under (most) dc faults and ICSLs are dimensioned purely by DCCB current rating and

protection selectivity. Utilizing the given DCCB current breaking capability of $I_{DCCB,max} = 16\ kA$ and opening time of $T_{DCCB} = 8\ ms$, and assuming firm dc voltage of $V_{DC}(0) = 640\ kV$ with peak magnitude of 1.05 p.u. in normal operation [3], the minimal DCCB inductor size for the basic case is calculated using

$$L_{CSL} = \frac{1.05 \cdot V_{DC}(0)}{2\, I_{DCCB,max} \cdot T_{DCCB}} \tag{16}$$

which yields 168 mH for the given parameters. Applying a slight margin, 180 mH is taken as the final value.

2. The "Large inductance" configuration ensures fault ride-through of MMCs using sufficiently large ICSLs. The final values are determined through iterative simulations, considering the defined overcurrent and undervoltage blocking thresholds. This case is used solely for demonstration purposes and is not expected to be practically feasible.

3. The "CCES" configuration uses a combination of ICSLs and CCES's to avoid MMC blocking. For a given ICSL, the CCES's are dimensioned by selecting the corresponding bank capacitance in Fig. 8.

Iterative simulations are used in all three cases to verify and finalize component section. Without CCES, buses 1 and 2 require impractically large ICSLs to avoid MMC blocking. With CCES, the inductor size is reduced to much more acceptable values, comparable to those used in some LCC projects [1]. Bus 3 on the other hand requires lower-sized inductors as a consequence of MMC 3 having twice the current rating and negative load current. There is little benefit in utilizing CCES on bus 3 for protection against pole-to-pole faults so it is added primarily for protection against pole-to-ground faults. For simplicity, same capacitor bank size is used as on the other buses. The remaining CCES parameters are $R_F = 2.5\ \Omega$, $L_F = 5\ mH$, $V_{SA,sat} = 20\ kV$ and $R_G = 0\ \Omega$. For the selected $V_{SA,sat}$, only three 8.5 kV thyristors [25] are required per pole, resulting in thyristor voltage rating of 25.5 kV.

Table 1. Protection system configuration parameters

		Protection system configuration			
Component location		**Basic (MMC blocking)**	**Large inductance**	**CCES**	
Bus	**DCCB**	**L_{CSL} [mH]**	**L_{CSL} [mH]**	**L_{CSL} [mH]**	**C_B [µF]**
1	12	180	1200	400	250
	13	180	1600		
2	21	180	1200	400	250
	23	180	1600		
3	31	180	300	250	250
	32				

4. Simulation results

4.1 Operation with no faults

CCES operation under normal grid conditions is demonstrated in Fig. 9. Power output of AC 1 is varied in the full range from 0 to 1 to 0 p.u. Because MMC 1 controls ac voltage, it is unable to contribute to dc voltage stability and some minor transient dc voltage oscillations are visible.

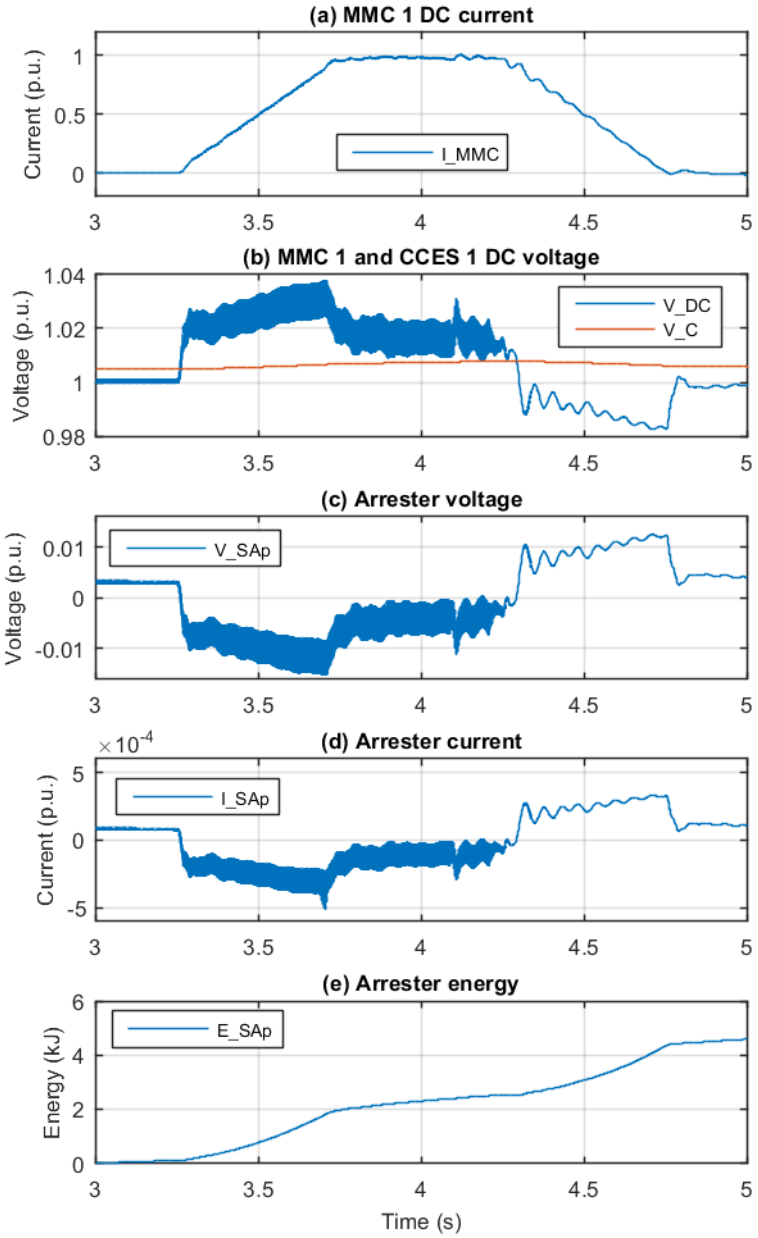

Fig. 9 MMC 1 and CCES 1 currents and voltages for 1 p.u. MMC power variation

Despite the presence of high-order harmonics and the fact that DC bus voltage changes within ±0.04 p.u., C_B voltage stays fairly constant, as visible from Fig. 9 (b). The voltage difference between V_C and V_{DC} is reflected in surge arrester voltage in Fig. 9 (c). Since the arrester does not saturate, only small leakage current is observed during transients. Fig. 9 (d) and (e) show that the energy exchange

between the CCES and MMC, as well as energy dissipation in the arrester, are very low. This demonstrates the advantages of surge arrester coupling.

4.2 Pole to pole faults

Fig. 10 shows MMC 3, DCCB 31 and bus 3 variables for a pole-to-pole fault on cable 13 in proximity of DCCB 31. Two cases are examined – when CCES is on and when CCES is off (S_{Mp} and S_{Mn} open). In the first few milliseconds after fault inception, DCCB 31 current rises at an almost identical slope. This demonstrates that the addition of CCES does not increase the fault current level for fixed ICSL. Since the dc bus voltage decreases faster without CCES, undervoltage protection blocks MMC 3 before DCCB 31 neutralizes the fault. MMC 3 blocking manifests itself as a sudden collapse of bus 3 voltage.

Following MMC 3 blocking, active power transfer between the MMC 3 and AC 3 stops (as seen from Fig. 10 (d)) which leads to a steep increase in dc bus voltage (MMCs 1 and 2 continue exporting power). The voltage in this case is limited to 1.5 p.u. by the bus surge arresters which are discussed in section 4.3. Without any overvoltage protection, bus 3 voltage would reach 2.2 p.u. at 1.14 s which is destructive for dc grid equipment. With CCES 3 operational, MMC 3 blocking is avoided. Pre-fault power transfer is re-established approximately 140 ms after fault inception and dc grid voltage stabilizes. This illustrates a major advantage of preventing MMC blocking in dc grids. Fig. 10 (c) and (e) show that the voltage difference between CCES 3 and bus 3 remains low at all times. Thyristors are fired around zero crossings of CCES current which minimizes the energy dissipation of surge arresters.

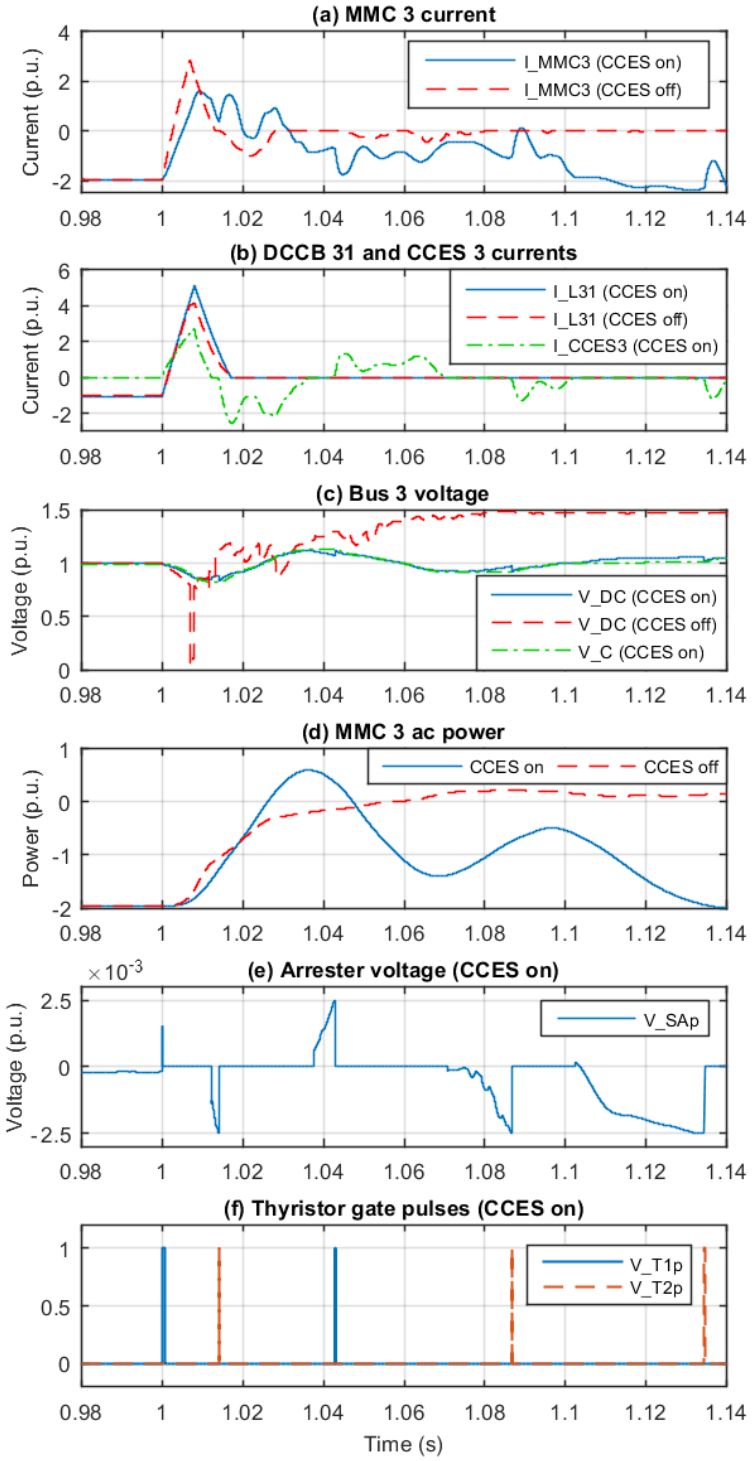

Fig. 10. MMC 3, DCCB 31 and CCES 3 variables for a pole-to-pole fault on cable 13

Fig. 11 shows bus 1 variables under a pole-to-pole fault next to DCCB 31. Undervoltage protection activates before overcurrent protection in this case and therefore, in order to simulate the worst-case scenario (lowest dc voltage leads to earliest MMC blocking), MMC 1 and 2 power references are set to 0.01 p.u. In the basic case, dc fault triggers blocking of all three converters and the whole grid goes out of function. Since MMC 1 controls ac voltage, its blocking initially appears as a three-phase short circuit on the ac side and dc fault current declines. MMC 1's antiparallel diodes provide a path for load

current of wind generators which continues to flow after fault interruption. This property can be observed as rising voltage in Fig. 11 (c) and is highly undesirable since dangerous overvoltages can appear at higher power outputs, as previously demonstrated in Fig. 10.

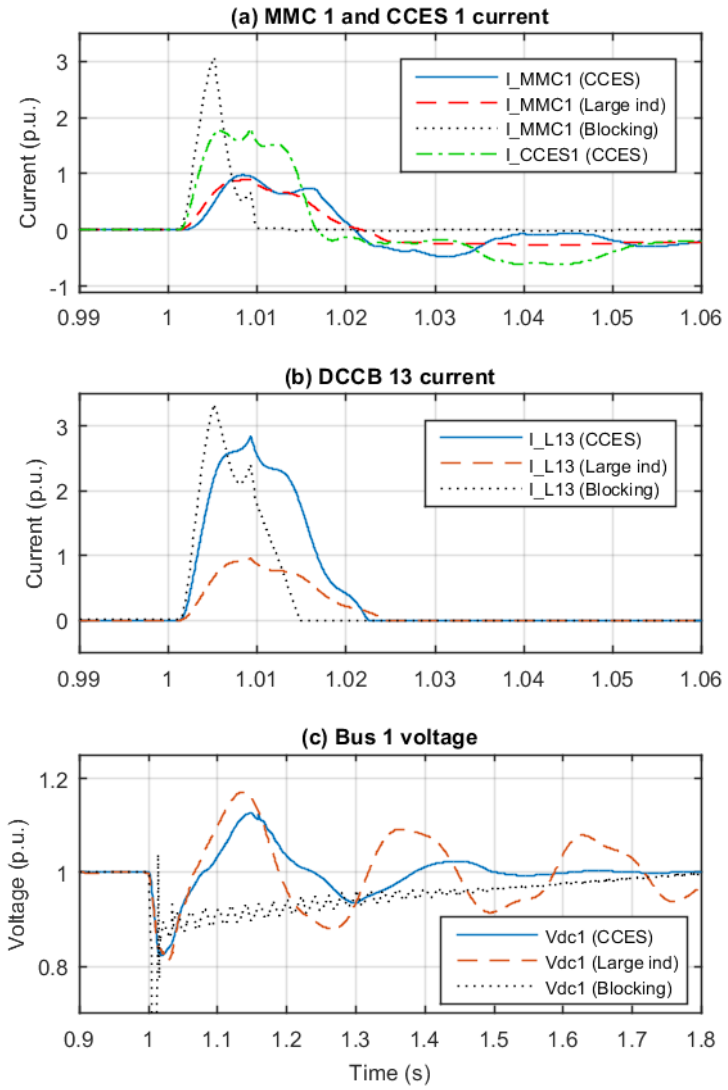

Fig. 11. Bus 1 voltages and currents under a pole-to-pole fault on cable 13

With CCES or large inductors, dc grid successfully rides through the fault and returns to stable state. However, voltages and currents take a lot longer to settle when large inductors are used (as seen in Fig. 11 (c)) which highlights why such arrangement is highly unlikely in practice. Basic CCES' operating principle is best demonstrated in Fig. 11 (a) where MMC 1 current peaks at the same value despite L_{13} being reduced to 1/4. This translates into the same voltage drop (Fig. 11 (c)) as dc voltage mainly depends on the amount of charge connected to the bus. On the downside, DCCB current is much higher when CCES is used, as seen in Fig. 11 (b).

Similar pole-to-pole faults are applied at all locations shown in Fig. 7. MMC and DCCB currents and DCCB energy dissipation are recorded for each case with the overall peak values (indicated with hat) shown in Table 2. For brevity, the results are only presented for MMCs 1 and 3 and DCCBs 13 and 31,

however, these can be interpolated to remaining components because of almost symmetrical grid layout. It is important to note that these values are merely indicative and further optimization may improve performance.

With CCES, MMCs experience substantially lower currents than in blocking case. Current ratings of DCCBs remain the same, however, arrester energy rating is increased. The increase is a lot more prominent in case of DCCB 13 which benefits from initial current decline following MMC 1 blocking. In case of blocked MMC 3, onshore grid continues to feed the fault through antiparallel diodes so arrester energy absorption of DCCB 31 is much higher.

Table 2. Protection system's performance indicators

		Protection system configuration		
Bus	**Indicator**	**Basic (MMC blocking)**	**Large inductance**	**CCES**
1	$\hat{I}_{MMC1}$ [p.u.]	4.15	2.23	2.30
	$\hat{I}_{L13}$ [p.u.]	4.51	2.01	5.03
	E_{13} [MJ]	17.42	51.90	52.50
3	$\hat{I}_{MMC3}$ [p.u.]	5.68	4.70	3.61
	$\hat{I}_{L31}$ [p.u.]	6.44	4.94	6.18
	E_{31} [MJ]	34.59	39.74	49.66

4.3 Pole to ground faults in symmetrical monopoles

Fig. 12 depicts the test case performed in this section and relevant measurements for a pole-to-ground fault on cable 13. The fault is detected and cleared in the same way as pole-to-pole faults. MMC's self-protection blocks the converter if pole voltage exceeds 1.5 p.u. [19]. Fig. 13 shows pole voltages for buses 1 and 3 and both ends of cable 13 when the surge arresters are not in function. Basic case is omitted as it gives a similar response as the system with large inductors.

Without CCES, pole voltages collapse very quickly despite the size of L_{13} and L_{31} and MMC blocking occurs. This is in line with explanation given in section 2.5. Particularly high overshoot of -2.88 p.u. is observed on V_{1n}. With CCES operational, blocking is avoided as V_{1n} peaks at only -1.30 p.u. This implies that bus arresters may not be required and voltage rating of all station equipment could be lowered. Bus voltages settle within 15 % of their nominal value, greatly simplifying post-fault pole rebalancing. If symmetrical monopole dc grids are built, pole-to-ground faults are expected to be the most frequent fault type and this illustrates a major benefit of CCES.

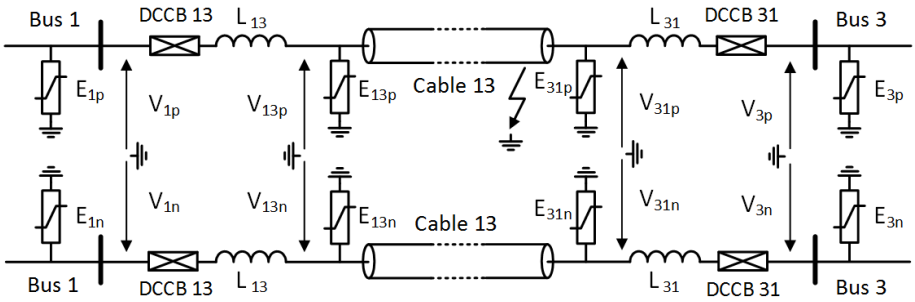

Fig. 12. Arrester placement and measurements for a pole-to-ground fault

Cable voltage profile is improved as well, albeit to a lesser extent. With typical XLPE cable impulse voltage rating of 1.85 p.u., cable arresters should limit the voltage below 1.8 p.u. Because V_{31n} briefly reaches 2.1 p.u. with CCES in operation, cable arresters are still required. The above test cases are repeated with all surge arresters in place. Absorbed energy of each arrester is measured and presented in Table 3. With CCES, total energy absorption is reduced from 28.34 MJ to 2.69 MJ so bus and cable arresters can be de-rated. This can offset the cost of greater DCCB energy absorption.

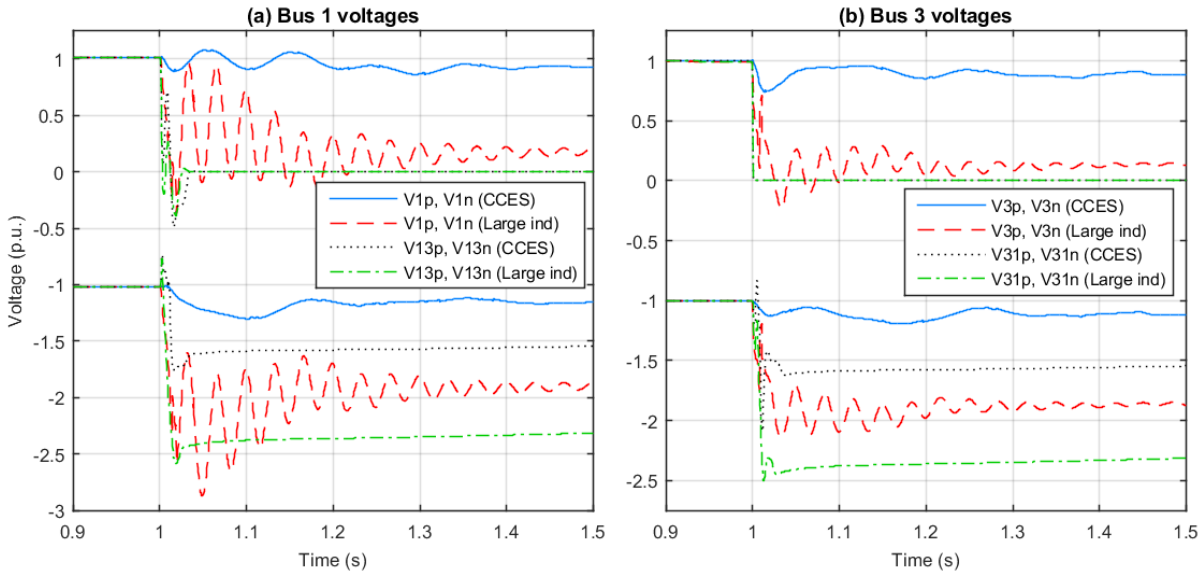

Fig. 13. Bus 1 and 3 and cable 13 pole voltages under a pole-to-ground fault without arrester protection

Table 3. Energy absorption of surge arresters under a pole-to-ground fault on cable 13

Arrester energy label	Arrester energy without CCES [MJ]	Arrester energy with CCES [MJ]
E_{1p}	2.36	0
E_{1n}	15.19	0
E_{3p}	0	0
E_{3n}	4.89	0
E_{13p}	0	0
E_{13n}	1.62	0.63

E_{31p}	0	0
E_{31n}	4.28	2.06
$\sum$	28.34	2.69

4.4 Transient stability

This section investigates if CCES could improve dc grid's transient stability. Fig. 14 shows bus voltages following MMC 1 blocking at full power as this is considered one of the worst transient disturbances. The most significant dc voltage profile improvement is achieved on bus 1. The addition of CCES completely eliminates transient overvoltages and drastically improves dv/dt. When large inductors are used, dv/dt is very high and there is risk of false fault detection by DCCB relays. Voltage profile of buses 2 and 3 remains overall similar with slightly reduced voltage drop. It is concluded that there is potential to improve transient stability of dc grids with the right choice of C_B and L_{CSL}.

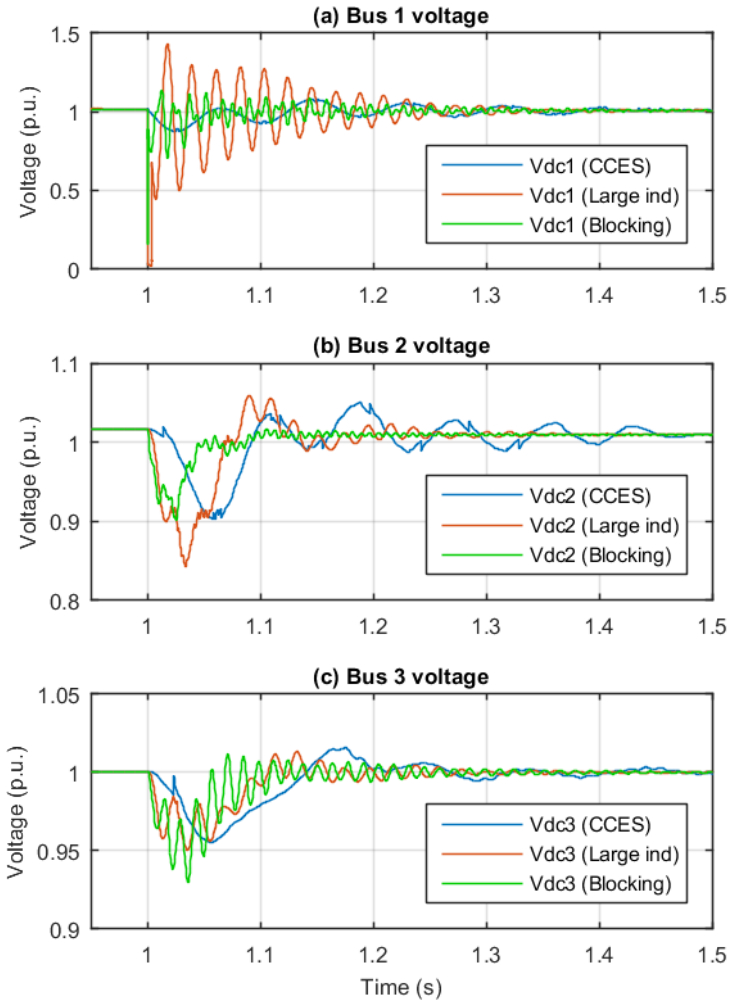

Fig. 14. Bus voltages following blocking of MMC 1

5. CCES weight and cost analysis

5.1 Key components

Table 4 shows the ratings of key CCES components. The ratings are given per pole since a CCES is bipolar. It is seen that the power ratings of thyristors, arresters and residual switch are low and therefore it is expected that the CCES cost will be dominated by the cost of the capacitor bank. Therefore, only the size and cost of C_B is evaluated further.

Table 4. Current and voltage ratings of key CCES components

Component	Capacitor bank	Thyristors	Surge arrester	Residual switch
Voltage rating	320 kV (nominal)	25.5 kV (peak)	20 kV (peak)	320 kV (nominal)
Current rating	> 10 kA (surge)	> 10 kA (surge)	< 100 A (surge)	< 10 A (breaking)

5.2 Weight and cost of the capacitor bank

Weight and cost analysis is carried out with the assistance from General Atomics, a manufacturer of specialized capacitors. The required electrostatic energy storage of CCES is calculated using

$$E_B = \frac{C_B}{2}\left(\frac{K_V}{K_{V0}}V_{DCn}\right)^2 \tag{17}$$

where V_{DCn} is nominal pole-to-pole voltage, K_V is the ratio between maximum allowed and nominal dc bus voltage and K_{V0} accounts for intrinsic overvoltage capability of the material at particular energy density. Once E_B is known, mass of the capacitor bank is calculated using

$$m_B = \frac{E_B}{E_0} \tag{18}$$

where E_0 represents specific energy (J/kg) of the chosen material. Total cost of the capacitor bank is obtained using

$$C_M = m_B \cdot C_0 \tag{19}$$

where C_0 represents the cost of manufacturing per unit of mass. E_0 and C_0 highly depend on the capacitor material. High energy density materials bring multiple benefits as they reduce the size, weight and cost. The reduction in cost might seem counterintuitive as the cost of material per unit of volume is higher. However, the reduction in total volume offsets the cost of material and labour. The real limitation comes from design life which decreases with energy density. For the given application, metalized film and film foil capacitors are considered as they offer dc life above 100 000 h (11.4 years) [26].

Capacitor lifetime can be extended by reducing electric field strength inside the capacitor. Empirical formula linking operating voltages V_1 and V_0 (which are proportional to electric field strength) to capacitor's dc life (T_1 and T_0) is [27]

$$T_1 = T_0 \left(\frac{V_1}{V_0}\right)^{\alpha} \tag{20}$$

α is an empirical constant representing property of the material, in the range between -12 and -18 for metalized and -6 to -8 for foil design [28]. Reducing the electric field strength reduces the energy density. From the basic formula for capacitor energy ($CV^2/2$), relationship between specific energy and capacitor lifetime is obtained as

$$E_1 = E_0 \left(\frac{T_1}{T_0}\right)^{2/\alpha} \tag{21}$$

Metalized film capacitors have specific energy up to 500 J/kg and production cost of 85-210 €/kg. Film foil capacitors have specific energy up to 50 J/kg and production cost of 20-60 €/kg. Production costs refer to manufacturers in the US and EU. Metalized film design is selected for this application, having lower cost-per-Joule and higher specific energy. Input parameters for weight and cost analysis are given in Table 5.

Fig. 15 shows the impact of overvoltage coefficient K_V and capacitor lifetime on device's weight and cost. It is visible that capacitor lifetime has fairly low impact on the cost of CCES while the impact of overvoltage coefficient is a lot more prominent. This indicates potential economic benefit of decreasing the voltage rating of bus's surge arresters below standard 1.8 p.u. to reduce the cost of CCES. For the given input parameters, the proposed device is suitable for protection of a 1000 MW MMC. Typical energy-to-power ratio of MMCs of that scale is 30-40 kJ/MVA [1] which implies 30-40 MJ of total stored energy. The proposed CCES stores 51.2 MJ at nominal voltage which is comparable to the MMC. Projected weight is around 150 t which is substantially lighter than the corresponding converter transformer [29].

Table 5. Input parameters for weight and cost analysis

Parameter	Label	Value
Nominal dc voltage	V_{DCn}	640 kV
Target capacitance	C_B	250 µF
Nominal dc life	T_0	100 000 h
Nominal specific energy	E_0	500 J/kg
Lifetime constant	α	-15
Material overvoltage constant	K_{V0}	1.15

Manufacturing cost	C_0	168 €/kg

Volume estimation of the CCES is out of the scope of this paper because it depends on the voltage and energy rating of unit capacitors and can vary significantly between implementations. Volume of capacitors alone is estimated at 50-100 m^3 (energy density of 0.5-1.0 J/cc), however, insulator (air) is likely to take up majority of space. Additional components such as grading resistors might also be required. Since the energy exchange between the CCES and the rest of the dc grid is very low under normal grid conditions (as demonstrated in Fig. 9), the choice of grading resistors is expected to notably influence the steady-state power dissipation of the capacitor bank C_B.

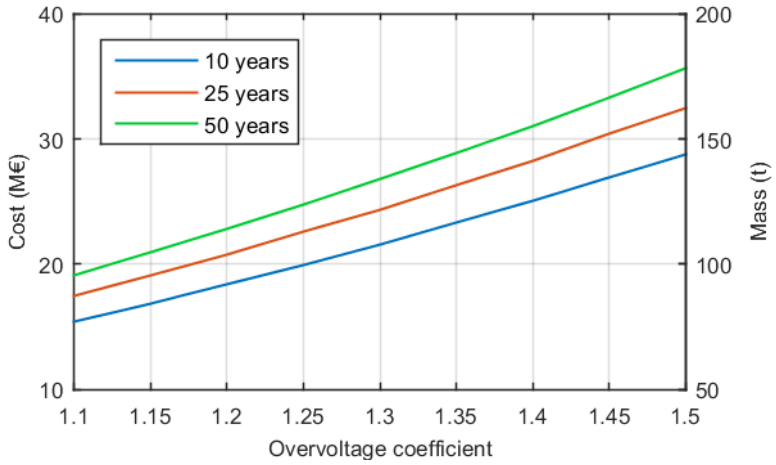

Fig. 15. Cost and mass of the capacitor bank versus overvoltage coefficient

5.3 Cost comparison with alternative protection strategies

Cost comparison between the CCES and other dc grid components (rated for 1 GW) is given in Table 6 [1, 7, 30]. Table 7 compares the cost of three protection system configurations with fault ride-through capability. The first protection system utilizes hybrid DCCBs and oversized DCCB inductors to prevent MMC blocking while the second protection system employs fault-tolerant FB MMC in combination with mechanical DCCBs. The third protection system is based on CCES, as demonstrated in this article.

There is evident economic benefit in using a CCES-based protection system over hybrid DCCBs or FB MMC, primary reason being lower semiconductor count. Fault-blocking cell topologies with reduced number of semiconductors are proposed [31] but the overall converter cost of these converters is expected to be comparable to a FB MMC. Relative protection system costs may differ for offshore installations with CCES requiring increased platform size but a substantial margin for error is provided. A major benefit in using mechanical DCCBs instead of hybrid ones is fairly fixed protection system cost with respect to the number of cables connected to the dc bus. As multiple MMCs become connected to a dc bus and the grid expands with new power flow paths, the benefit of CCES becomes more pronounced as only a single CCES is required per dc bus. In general, CCES will offer more economic inventive as dc grids increase in complexity.

Table 6. Cost comparison between dc grid components rated for 1 GW

Component	Cost [p.u.]	Cost [M€]
HB MMC	1	110 M€
FB MMC	1.8	200 M€
CCES	0.15 – 0.35	15 – 35 M€
Hybrid DCCB	0.25 – 0.35	27 – 38 M€
Mechanical DCCB	0.009 – 0.018	1 – 2 M€

Table 7. Cost comparison between protection system configurations (per bus)

Configuration	Cost (2 cables) [p.u.]	Cost (3 cables) [p.u.]
HB MMC + HDCCBs	1.5 – 1.7	1.75 – 2.05
FB MMC + MDCCBs	1.82 – 1.84	1.83 – 1.86
HB MMC + CCES + MDCCBs	1.17 – 1.39	1.18 – 1.41

6. Conclusion

CCES is a simple and relatively low-cost device. The detailed simulations concluded that is brings multiple benefits to dc grids:

1. It prevents MMC blocking under dc faults by reducing the fault current contribution and voltage drop of the MMC. As a result, DCCB inductors can be reduced and cost-effective mechanical DCCBs can be employed.
2. It prevents MMC blocking under pole-to-ground faults in symmetrical monopole grids.
3. It improves transient stability.
4. It significantly reduces dc overvoltages, implying savings in costs of overvoltage protection.

Estimated cost of a 640 kV, 250 µF CCES for 1 GW MMC station is around 30 M€ while the projected weight is 150 tons. The design includes thyristors in parallel with surge arresters which minimizes the size and cost of these components. On the downside, some increase in DCCB energy absorbers may be required but this is partially offset by the reduced energy rating of the cable and bus arresters. Large capacitor bank size is another disadvantage of the proposed solution, considering all the construction and maintenance challenges. The failure rates of unit capacitors in particular could significantly reduce the reliability of CCES-based protection compared to the alternatives.

7. Acknowledgements

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